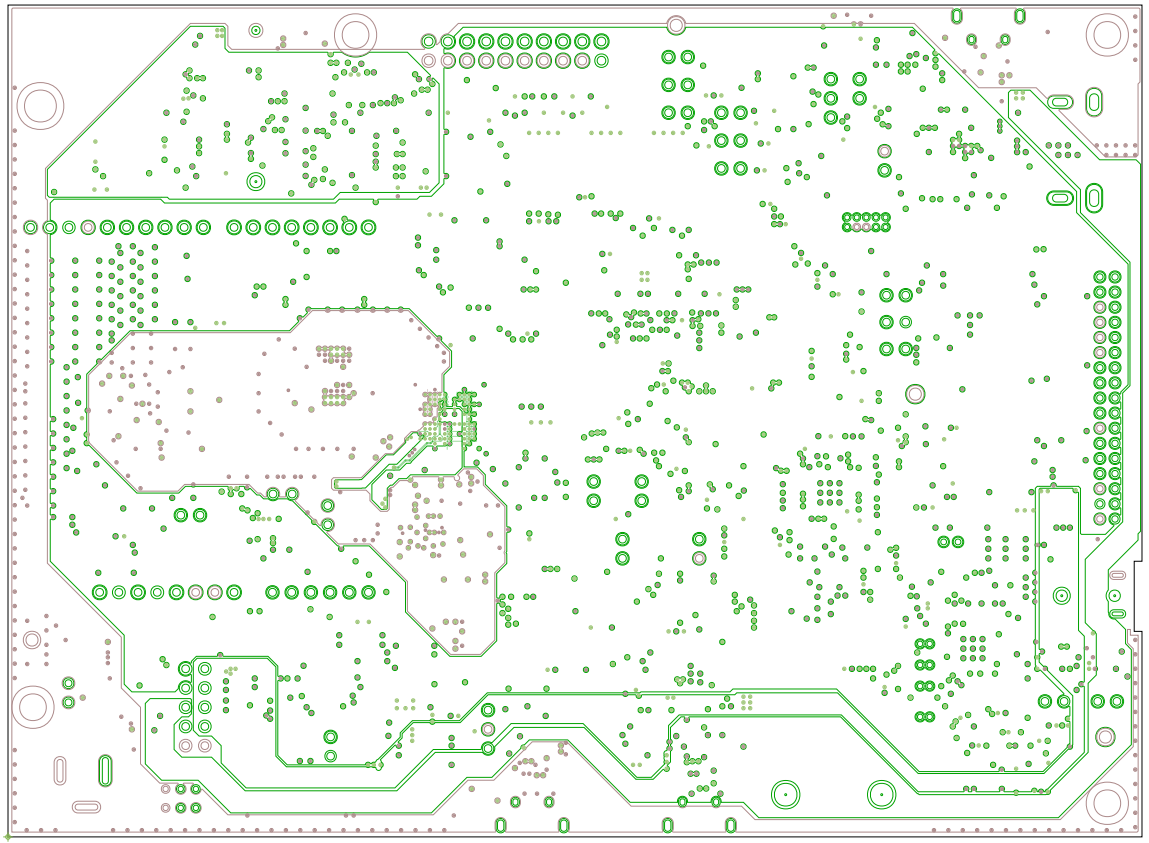
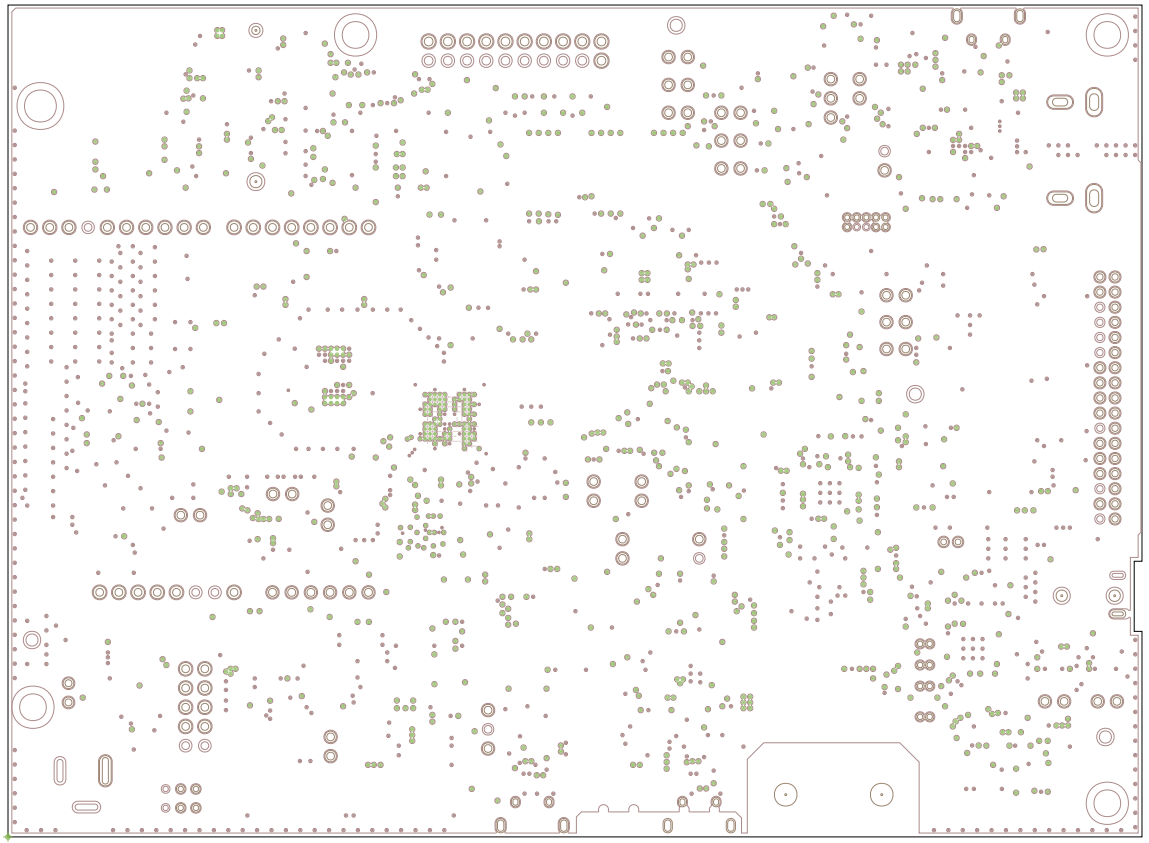


| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET<br>6 OF 10 | FILM<br>ARTWORK LAYER03 | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |



| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET<br>5 OF 10 | FILM ARTWORK LAYER02 | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |

NOTES (UNLESS OTHERWISE SPECIFIED):

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |
| | A | ORIGINAL RELEASE | 11-27-20 | D.A. |
| | B | DESIGN UPDATED | 03-17-21 | D.A. |

## DETAIL A
## LAYER STACKUP
SCALE: NONE

.062" THK +/- 10%

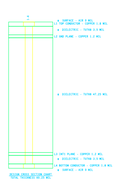
| | | FINISHED Cu WEIGHT |
|---|---|---|
| LAYER 1 | COMPONENT SIDE | 1/2oz+plating |
| LAYER 2 | GROUND PLANE | 1 oz. |
| LAYER 3 | POWER PLANE | 1 oz. |
| LAYER 4 | SOLDER SIDE | 1/2oz+plating |

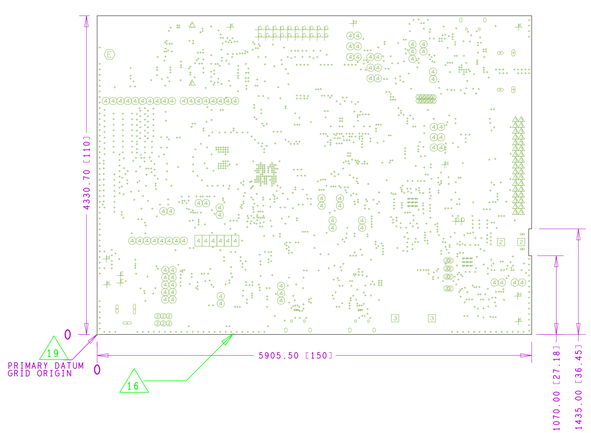
## DETAIL B
## IMPEDANCE REQUIREMENTS
## IMPEDANCE TOLERANCE IS 10%

| Layers | Single Ended | | Differential | | | Differential | | |
|---|---|---|---|---|---|---|---|---|
| | Trace Width (Mils) | Impedance (Ohms) | Trace Width (Mils) | Trace Spacing "Airgap" (Mils) | Impedance (Ohms) | Trace Width (Mils) | Trace Spacing "Airgap" (Mils) | Impedance (Ohms) |
| L1 | 5.00 | 50 | 4.2 | 6.00 | 100 | 4.70 | 5.00 | 90 |
| L4 | 5.00 | 50 | | | | 4.70 | 5.00 | 90 |

DRILL CHART: TOP to BOTTOM
ALL UNITS ARE IN MILS

| FIGURE | FINISHED_SIZE | ROTATION | TOLERANCE_DRILL | TOLERANCE_TRAVEL | PLATED | QTY |
|---|---|---|---|---|---|---|
| 8 22 | 8.0 | - | +0.0/-8.0 | - | PLATED | 1718 |
| | 8.1 | - | +0.0/-8.1 | - | PLATED | 22 |
| | 26.0 | - | +2.0/-2.0 | - | PLATED | 10 |
| | 28.0 | - | +2.0/-2.0 | - | PLATED | 14 |
| | 30.0 | - | +3.0/-3.0 | - | PLATED | 2 |
| | 33.0 | - | +2.0/-2.0 | - | PLATED | 34 |
| | 36.0 | - | +3.0/-3.0 | - | PLATED | 2 |
| | 40.0 | - | +3.0/-3.0 | - | PLATED | 84 |
| | 41.0 | - | +3.0/-3.0 | - | PLATED | 6 |
| | 45.0 | - | +3.0/-3.0 | - | PLATED | 20 |
| | 63.0 | - | +3.0/-3.0 | - | PLATED | 4 |
| | 139.0 | - | +3.0/-3.0 | - | PLATED | 4 |
| | 166.0 | - | +3.0/-3.0 | - | PLATED | 1 |
| | 43.0 | - | +2.0/-2.0 | - | NON-PLATED | 1 |
| | 59.0 | - | +2.0/-2.0 | - | NON-PLATED | 2 |
| | 63.0 | - | +2.0/-2.0 | - | NON-PLATED | 1 |
| | 118.0 | - | +2.0/-2.0 | - | NON-PLATED | 2 |
| | 34.0x26.0 | 90.000 | +3.0/-3.0 | +3.0/-3.0 | PLATED | 6 |
| | 59.0x20.0 | 0.000 | +2.0/-2.0 | +2.0/-2.0 | PLATED | 2 |
| | 59.0x33.0 | 90.000 | +3.0/-3.0 | +3.0/-3.0 | PLATED | 6 |
| | 79.0x40.0 | 0.000 | +2.0/-2.0 | +2.0/-2.0 | PLATED | 2 |
| | 86.61x47.24 | 90.000 | +2.0/-2.0 | +2.0/-2.0 | PLATED | 2 |
| | 118.0x31.0 | 0.000 | +2.0/-2.0 | +2.0/-2.0 | PLATED | 1 |
| | 118.0x31.0 | 90.000 | +2.0/-2.0 | +2.0/-2.0 | PLATED | 1 |
| | 137.8x31.5 | 90.000 | +2.0/-2.0 | +2.0/-2.0 | PLATED | 1 |






1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE. WITH SPECIFICATION IPC-6012 CLASS 2 (LATEST REVISION).

2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 260 DEGREES CELSIUS FOR 10 SECONDS.

3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101D-26, 83 or 98
   Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
   Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.

4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL 'A'

5. CHARACTERISTIC IMPEDANCE - SEE DETAIL 'B'

6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .0042"/.005X'

7. PLATING FINISH: A. BOTH SIDES ENIG: TO MEET THE REQUIREMENTS OF IPC-4552 (LATEST REVISION).

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - TO MEET THE REQUIREMENTS OF IPC-SM-840E (OR LATEST REVISION).
   GREEN COLOR, BOTH SIDES. MODIFICATION OF SOLDERMASK IS NOT ALLOWED WITHOUT WRITTEN PERMISSION FROM NXP.
   TYPE: LPI OR EQUIVALENT.
   A. LOCATION = +/-.002" OF PLATED PADS.
   B. DIAMETER OR SIZE = +/-.002 OF ORIGINAL DATA

10. SILKSCREEN - WHITE EPOXY OR ACRYLIC INK, BOTH SIDES. NO SILKSCREEN ON ANY EXPOSED COPPER FEATURE.

11. ELECTRICAL TEST - 100% IPCD356. PCB FABRICATOR TO PERFORM A NET COMPARE AGAINST THE IPCD356 NETLIST PROVIDED BY NXP.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DFM CHECK MUST BE RUN ON BOARD DATA BEFORE BUILDING BOARDS, UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY NXP.

14. TEARDROPS MAY BE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

16. SUPPLIER MARKINGS - ON SECONDARY SIDE ONLY, WHERE SHOWN.
   - MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

17. THE PWB WILL BE MARKED AS LEAD FREE BY USE OF AN INK STAMP (P6)

18. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

19. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP. ALL HOLE LOCATION TOLERANCES ARE TO BE +/-.002 IN REFERENCE TO THE PRIMARY DATUM UNLESS OTHERWISE SPECIFIED.

20. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS. THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.

21. THE MANUFACTURE HAS THE OPTION TO ADD COPPER THIEVING ON OUTER AND INNER LAYERS, KEEP A MINIMUM DISTANCE OF .100" FROM ANY BOARD FEATURES.

22. THIS BOARD USES VIA-IN-PAD: SEE FAB_VIAFILL.ART
   A. ALL VIAS USING X.1 DRILL SIZES ARE TO BE FILLED WITH NON-CONDUCTIVE VIA FILL. LACKWERKE-PETERS PP2795 OR EQUIVALENT AND MADE PLANAR TO THE PADS.
   B. OVERPLATE THE FILLED VIA AND APPLY FINISH METAL TREATMENT.
   C. DIMPLE OR PROTRUSION ON VIA-IN-PADS MUST BE NO GREATER THAN .001".

___ COMPANY PUBLIC
X_ COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

PART NO. 170-47858

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN, PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL MEET THE RoHS COMPLIANCE "DELEGATED DIRECTIVE (EU) 2015/863 OF 31 MARCH 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU". A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL NOT CONTAIN ANY OF THE SUBSTANCES OF VERY HIGH CONCERN (SVHC) ABOVE THE THRESHOLD VALUE PER 1907 CURRENT ECHA LIST OF SVHC'S AND WITH ANNEX XIV AND ANNEX XVII OF REACH DIRECTIVE 1907/2006. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS .XX .01 .XXX .005
ANGLES .0-30"
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

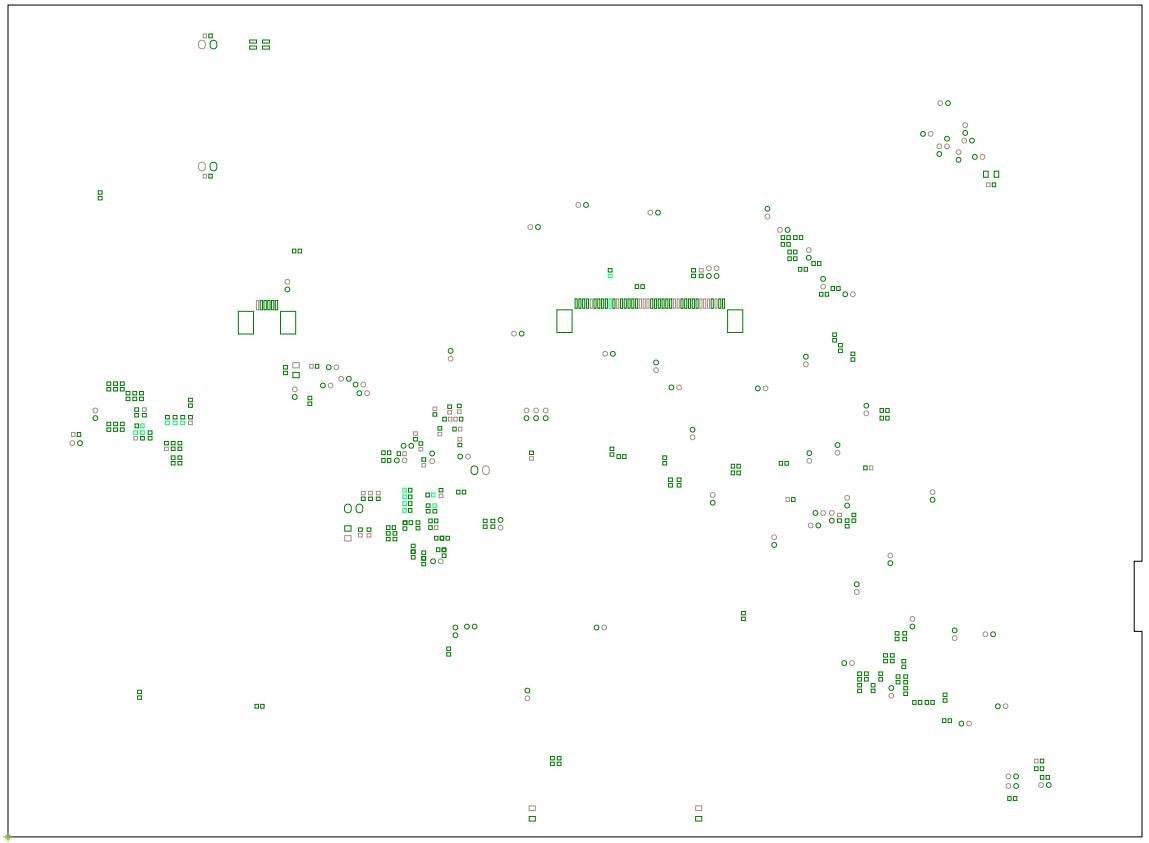
| APPROVALS | DATE |
|---|---|
| DRAWN XIAOWEI XU | 03-17-21 |
| CHECKED DAFNE ARIAS | 03-17-21 |
| DESIGN ENGINEER ALBERT LI | 03-17-21 |

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

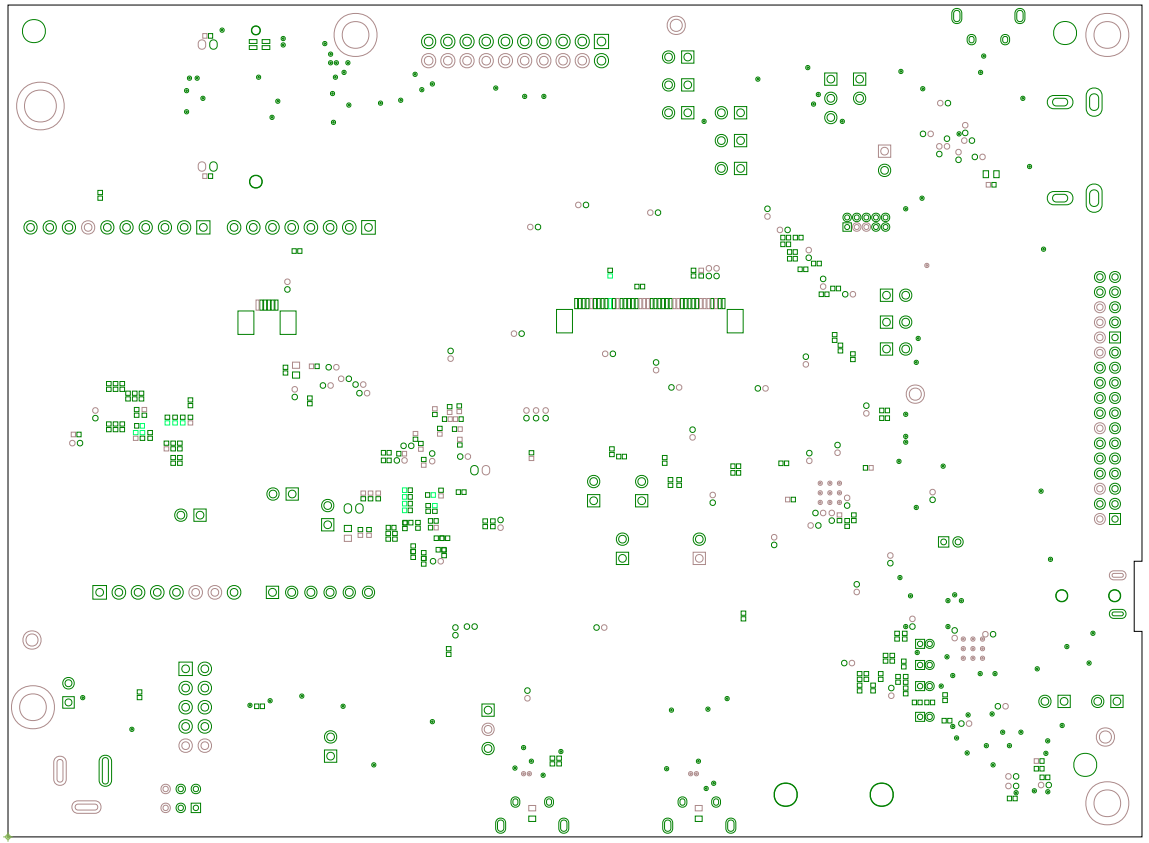
TITLE: PRINTED WIRING BOARD MIMXRT1060-EVKB

| SIZE | CAD FILE NAME | DWG. NO. | REV |
|---|---|---|---|
| D | LAY-47858 | FAB-47858 | B |

SCALE DO NOT SCALE DRAWING SHEET 1 OF 2



| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET<br>10 OF 10 | FILM<br>PASTEMASK_BOTTOM | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |



| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
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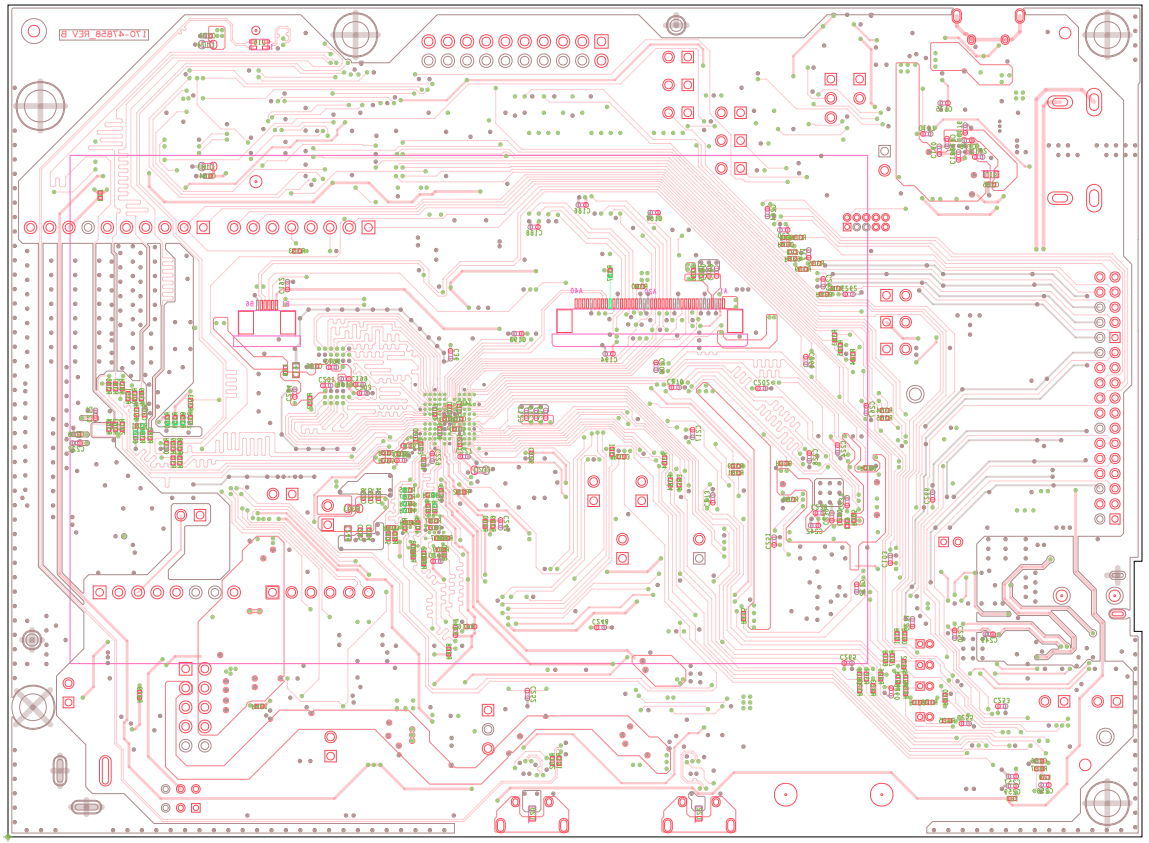
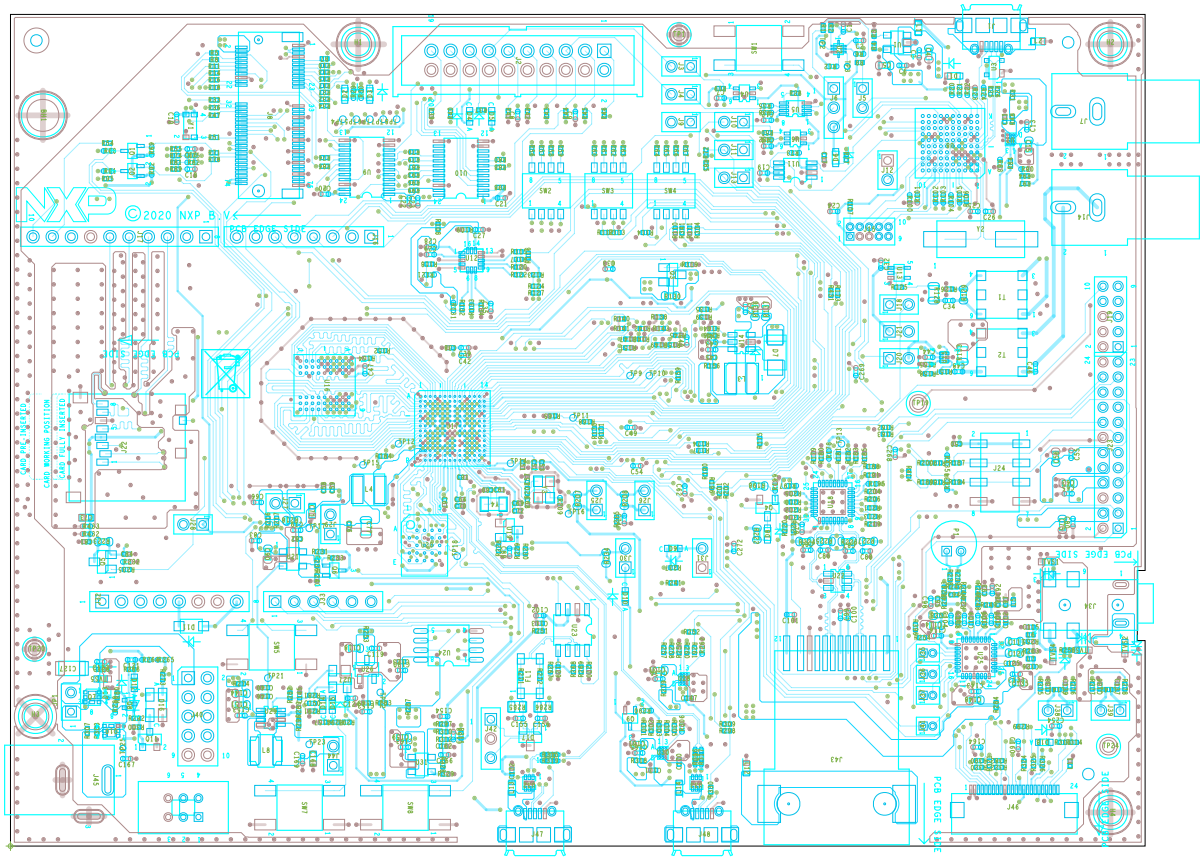
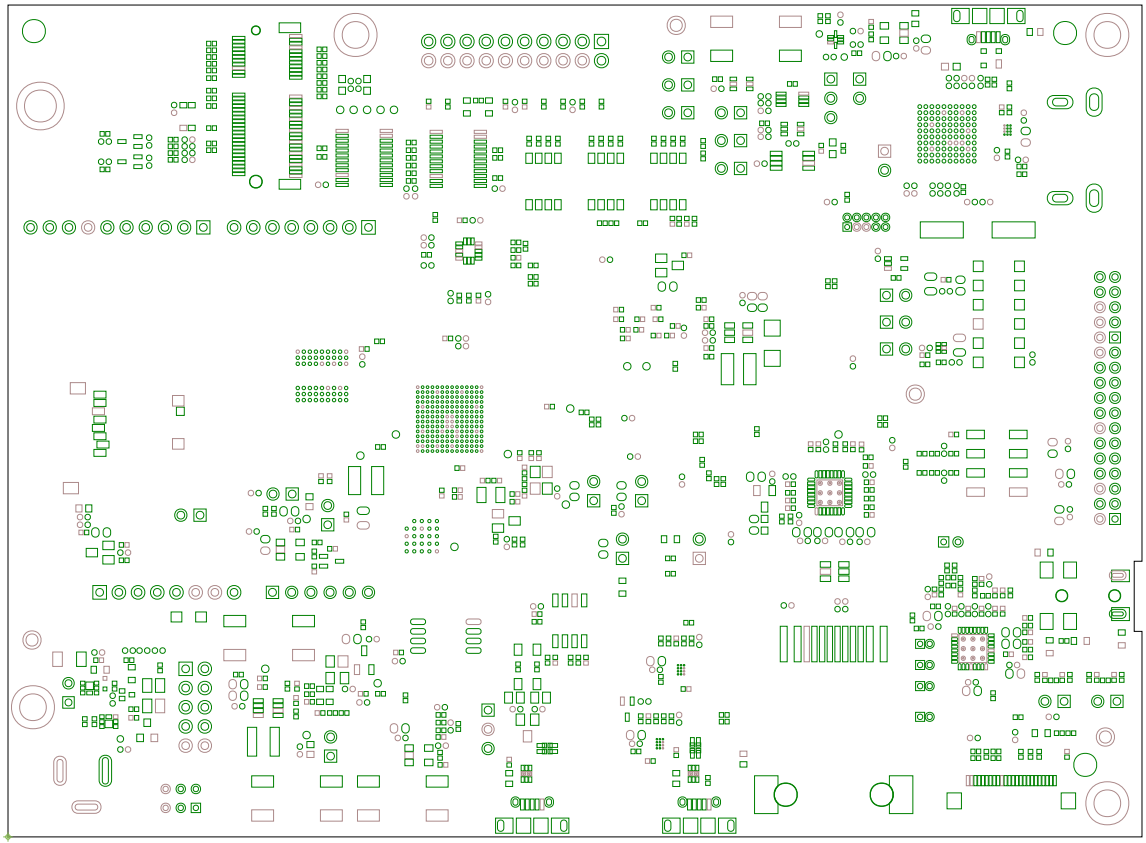
| SHEET<br>8 OF 10 | FILM<br>SOLDMASK BOTTOM | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |



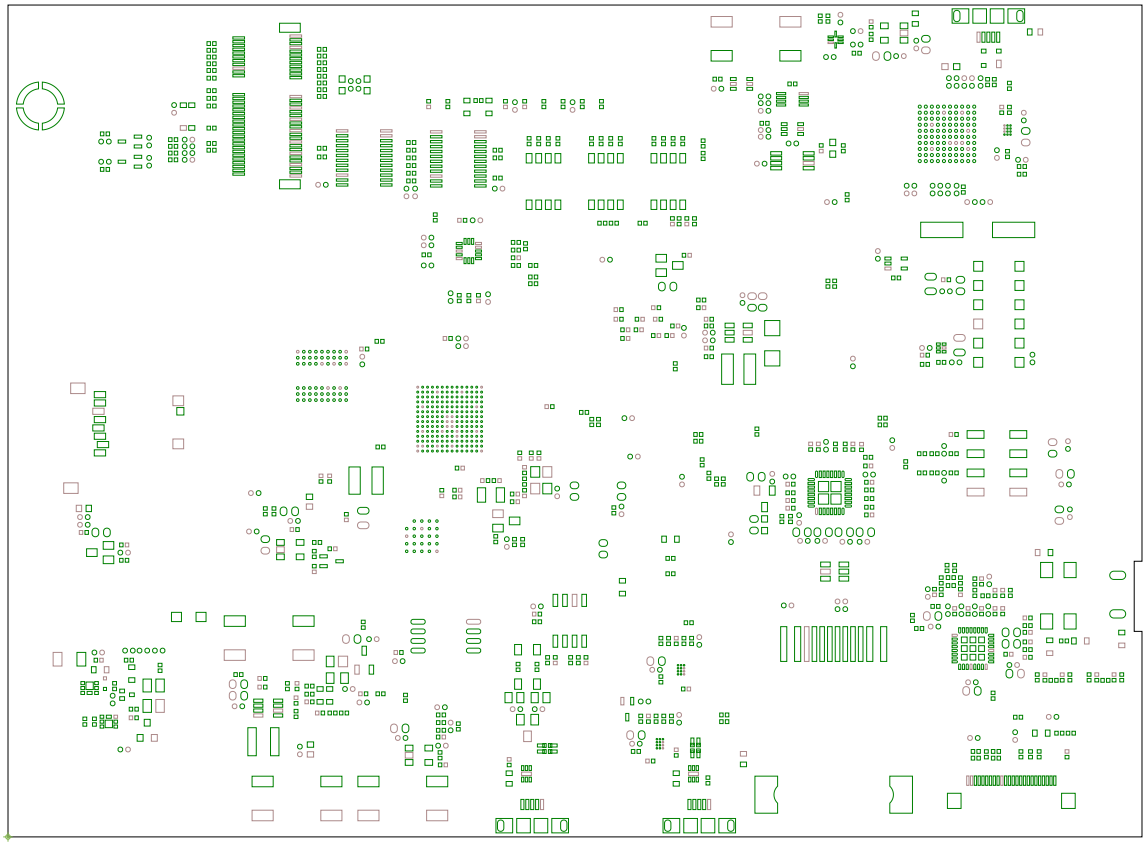
| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET<br>7 OF 10 | FILM<br>ARTWORK BOTTOM | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |



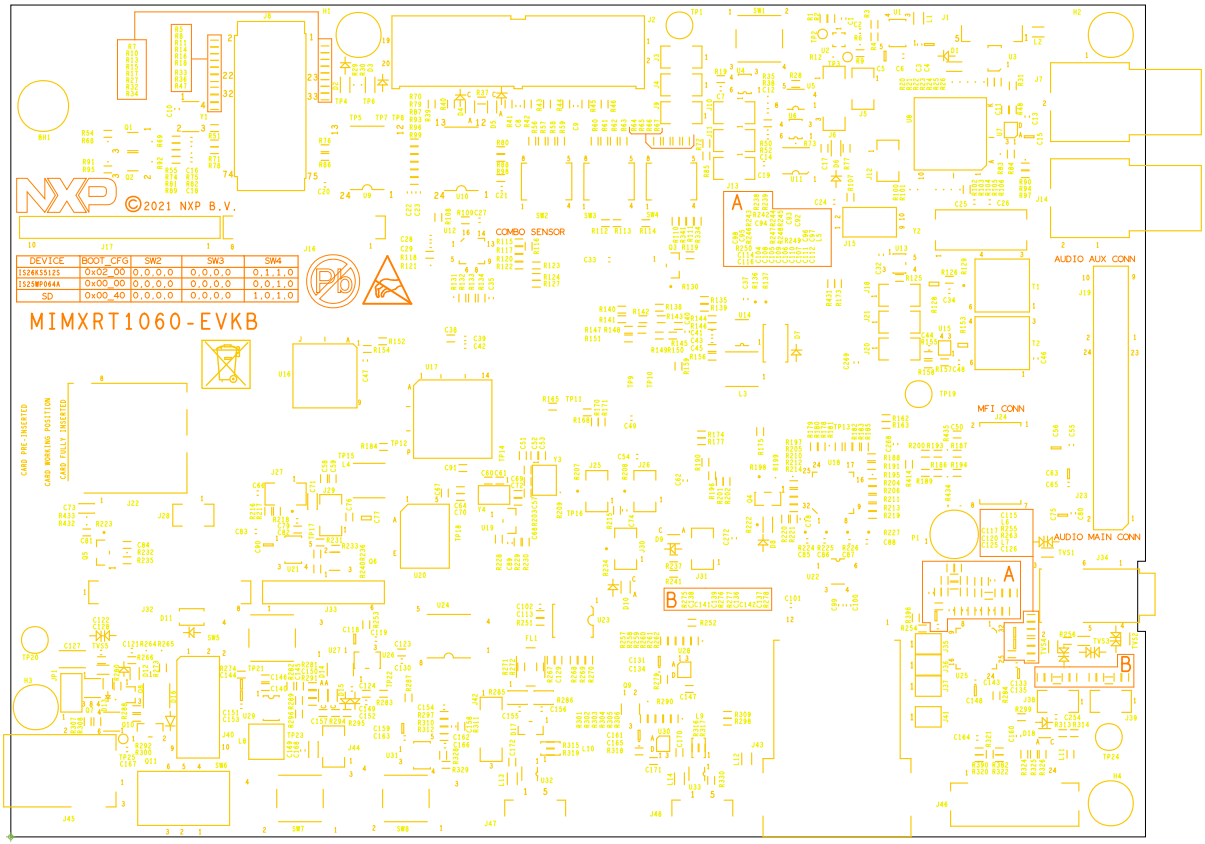

| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET 4 OF 10 | FILM ARTWORK TOP | DATE 03-17-21 | NUMBER 170-47858 REV B |



| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET<br>3 OF 10 | FILM<br>SOLDMASK TOP | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |

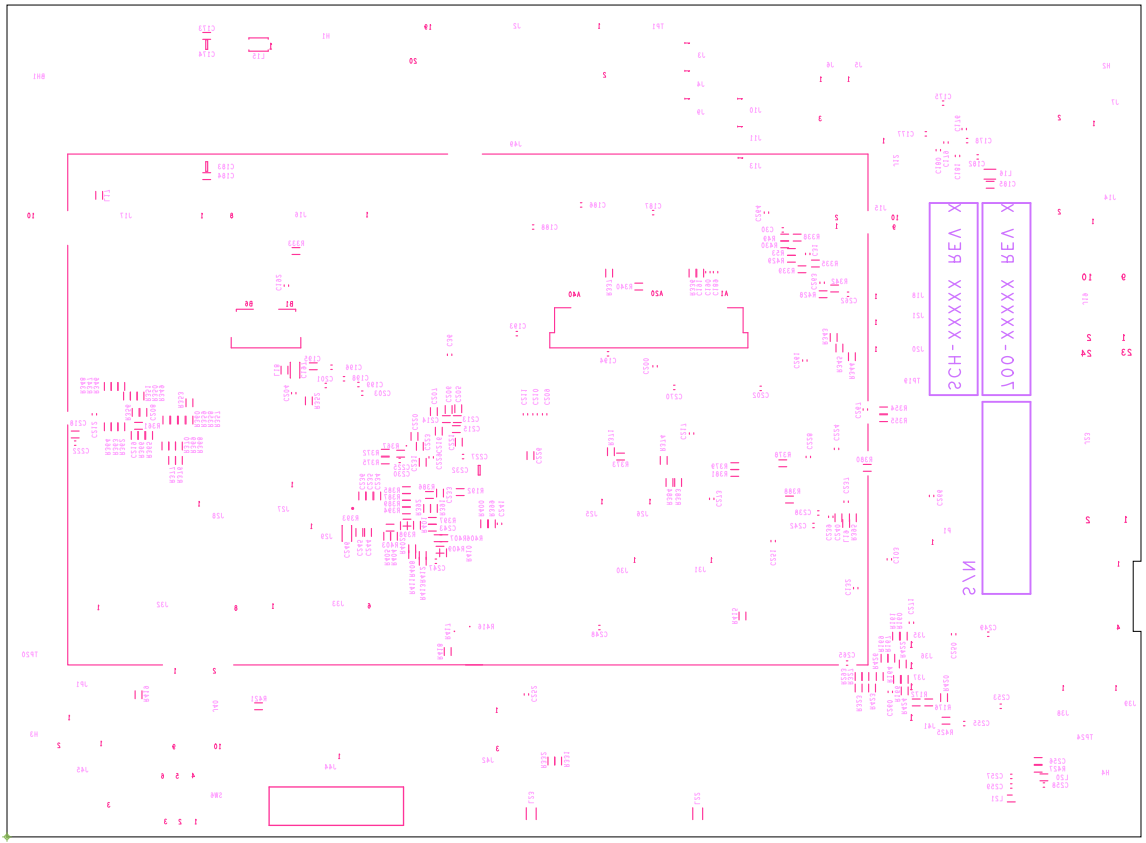


| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME<br>MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET<br>1 OF 10 | FILM<br>PASTEMASK_TOP | DATE<br>03-17-21 | NUMBER<br>170-47858 REV B |

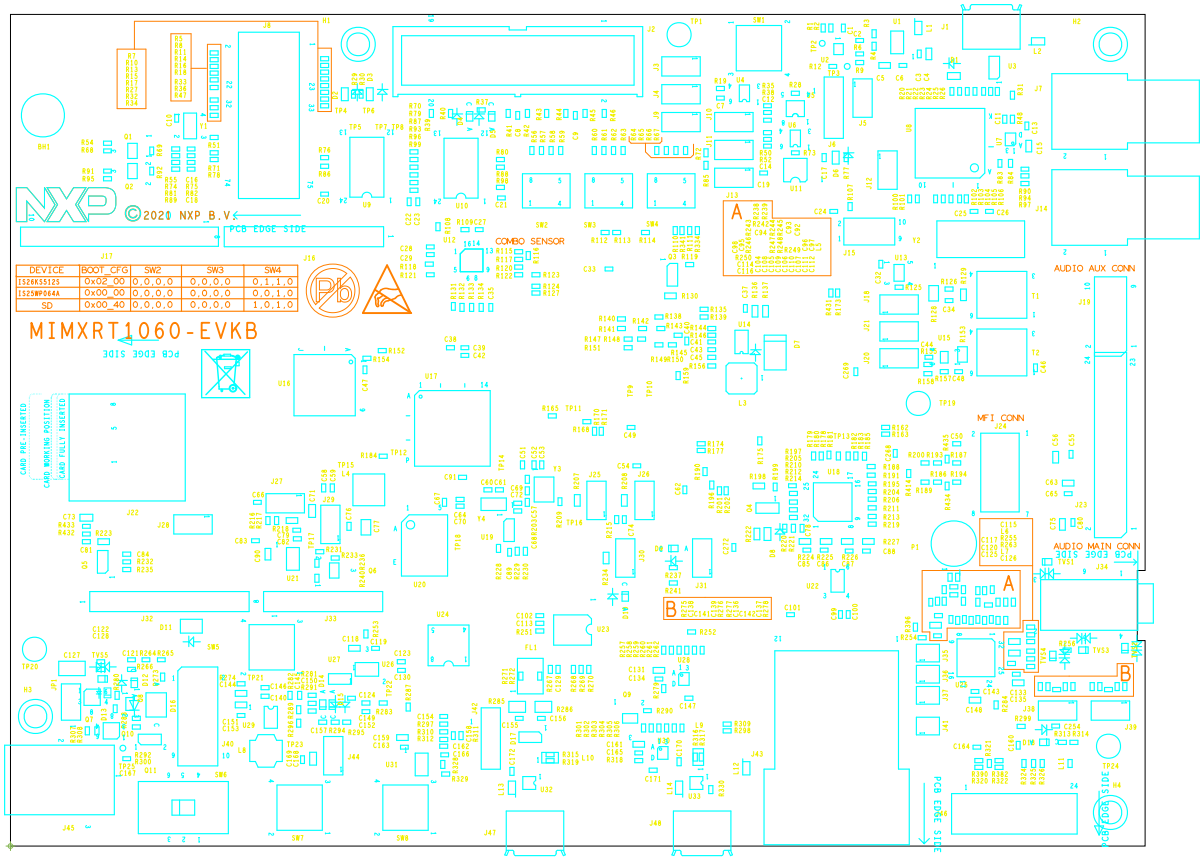



| DEVICE | BOOT_CFG | SW2 | SW3 | SW4 |
|---|---|---|---|---|
| 1S26KS5125 | 0x02_00 | 0,0,0,0 | 0,1,1,0 | |
| 1S25MP064A | 0x00_00 | 0,0,0,0 | 0,0,1,0 | |
| SD | 0x00_40 | 0,0,0,0 | 0,0,0,0 | 1,0,1,0 |

| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | NAME MIMXRT1060_EVKB | | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | | |
| SHEET 2 OF 10 | FILM SILKSCREEN TOP | DATE 03-17-21 | NUMBER 170-47858 REV B |




| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | | NAME MIMXRT1060_EVKB | |
| THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO FREESCALE AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP. | | ___ PUBI (PUBLIC INFORMATION)<br>_X_ FIUO (NXP INTERNAL USE ONLY)<br>___ FCP (NXP CONFIDENTIAL PROPRIETARY) | |
| SHEET 9 OF 10 | FILM SILKSCREEN BOTTOM | DATE 03-17-21 | NUMBER 170-47858 REV B |




| DEVICE | BOOT_CFG | SW2 | SW3 | SW4 |
|---|---|---|---|---|
| IS26KS512S | 0x02_00 | 0,0,0,0 | 0,0,0,0 | 0,1,1,0 |
| IS25WP064A | 0x00_00 | 0,0,0,0 | 0,0,0,0 | 0,0,1,0 |
| SD | 0x00_40 | 0,0,0,0 | 0,0,0,0 | 1,0,1,0 |

| | | | |
|---|---|---|---|
| NXP SEMICONDUCTOR<br>6501 WILLIAM CANNON DRIVE WEST<br>AUSTIN, TEXAS 78735 USA | NAME MIMXRT1060_EVKB | | |
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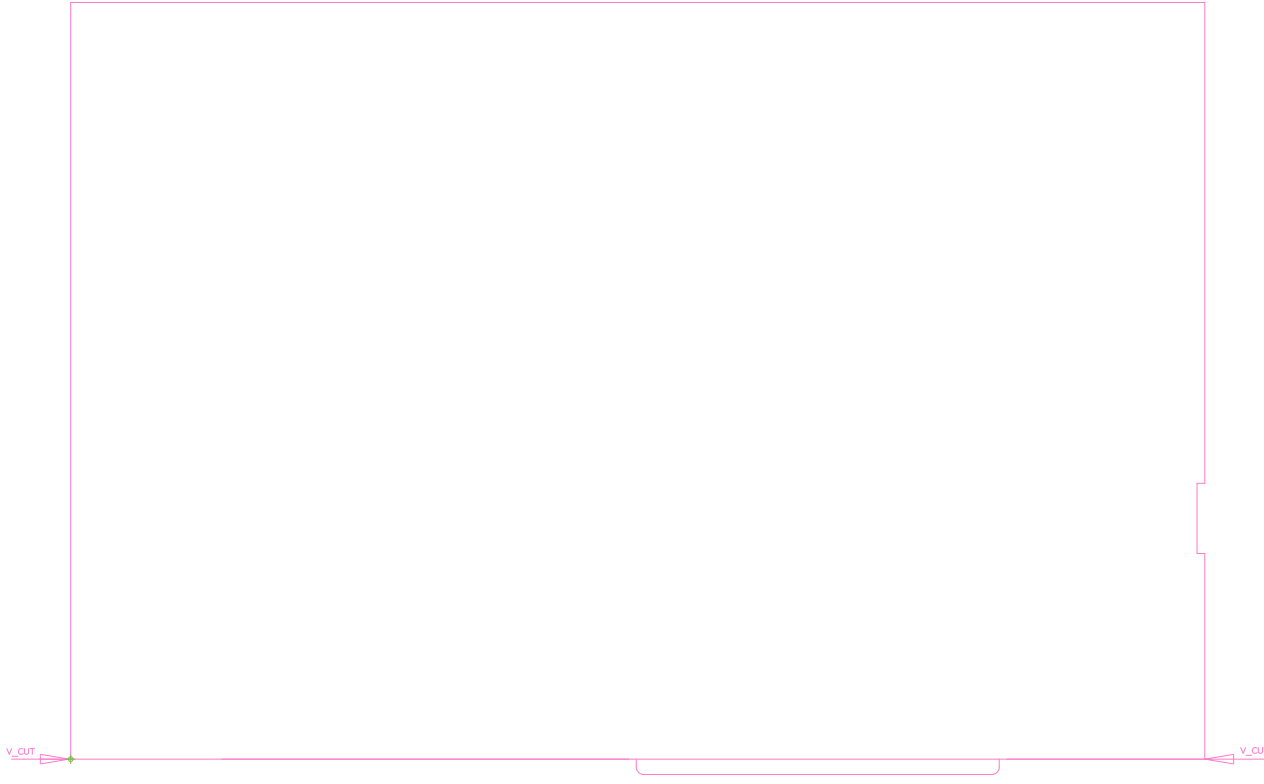
| SHEET OF 10 | FILM | DATE 03-17-21 | NUMBER 170-47858 REV B |

ART FILM - PANEL




ART FILM - PANEL

NOTES (UNLESS OTHERWISE SPECIFIED):

| REVISIONS | | | | |
|---|---|---|---|---|
| ZONE | REV | DESCRIPTION | DATE | APPROVED |
| | A | ORIGINAL RELEASE | 11-27-20 | D.A. |
| | B | DESIGN UPDATED | 03-17-21 | D.A. |

# THIS FAB_VIAFILL.ART SHOWS LOCATIONS OF VIA-IN-PAD TO BE FILLED

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL BE RoHS COMPLIANT ACCORDING DIRECTIVE (EU) 2015/863 OF 31 MARCH 2015 AMENDING ANNEX II TO DIRECTIVE 2011/65/EU. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

ALL PARTS, MATERIALS AND FINISHED ASSEMBLY SHALL BE NON-REACH SUBSTANCES. NO SUBSTANCES CONCERN LSVHC ABOVE THE THRESHOLD VALUE PER THE CURRENT CHALLIST OF SVHC AND WITH ANNEX XIV AND ANNEX XVII OF REACH DIRECTIVE 1907/2006/EC. A CERTIFICATE OF COMPLIANCE IS REQUIRED UPON REQUEST.

___ COMPANY PUBLIC
X_ COMPANY INTERNAL
___ COMPANY CONFIDENTIAL

UNLESS OTHERWISE SPECIFIED
DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
DECIMALS ANGLES
.XX ±.01 ±0°30'
.XXX ±.005
√ RMS ALL MACHINED SURFACES
BREAK ALL SHARP EDGES AND CORNERS.
REMOVE BURRS.
UNDERLINED DIM. NOT TO SCALE.
THIRD ANGLE ORTHOGRAPHIC PROJECTION IS USED.

PART NO. 170-47858

THIS DOCUMENT CONTAINS INFORMATION PROPRIETARY TO NXP AND SHALL NOT BE USED FOR ENGINEERING DESIGN PROCUREMENT OR MANUFACTURE IN WHOLE OR IN PART WITHOUT THE CONSENT OF NXP.

| APPROVALS | DATE |
|---|---|
| DRAWN XIAOWEI XU | 03-17-21 |
| CHECKED DAFNE ARIAS | 03-17-21 |
| DESIGN ENGINEER ALBERT LI | 03-17-21 |

NXP SEMICONDUCTORS
6501 WILLIAM CANNON DRIVE WEST AUSTIN, TEXAS 78735 USA

TITLE: PRINTED WIRING BOARD
MIMXRT1060-EVKB

| SIZE | CAD FILE NAME | DWG. NO. | REV |
|---|---|---|---|
| D | LAY-47858 | FAB-47858 | B |

SCALE DO NOT SCALE DRAWING SHEET 2 OF 2