MIMXRT1060-EVK

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Revision History

Rev. Code	Date	By	Description
X1	2018-2-25	Shawn Shi	For BOM preparation
X2	2018-3-12	Shawn Shi	Initial Release
A	2018-5-2	Shawn Shi	Delete U47 for JTAG_RESET
A1	2018-5-17	Shawn Shi	Rename LPC JTAG_TDI signa to JTAG_TDI_L
A2	2018-6-15	Shawn Shi	Change RT1050 symbol to RT1060, Change oscillator load capacitor value C42 and C43.

1. Unless Otherwise Specified:

   All resistors are in ohms, 1/16 Watt,0402
   All capacitors are in uF,0402
   All voltages are DC
   All polarized capacitors are aluminum electrolytic

2. Interrupted lines coded with the same letter or letter combinations are electrically connected.

3. Device type number is for reference only. The number varies with the manufacturer.

4. Special signal usage:
   _B Denotes - Active-Low Signal
   <> or [] Denotes - Vectored Signals

5. Interpret diagram in accordance with American National Standards Institute specifications, current revision, with the exception of logic block symbology.

ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: MIMXRT1060-EVK

Page Title: COVER

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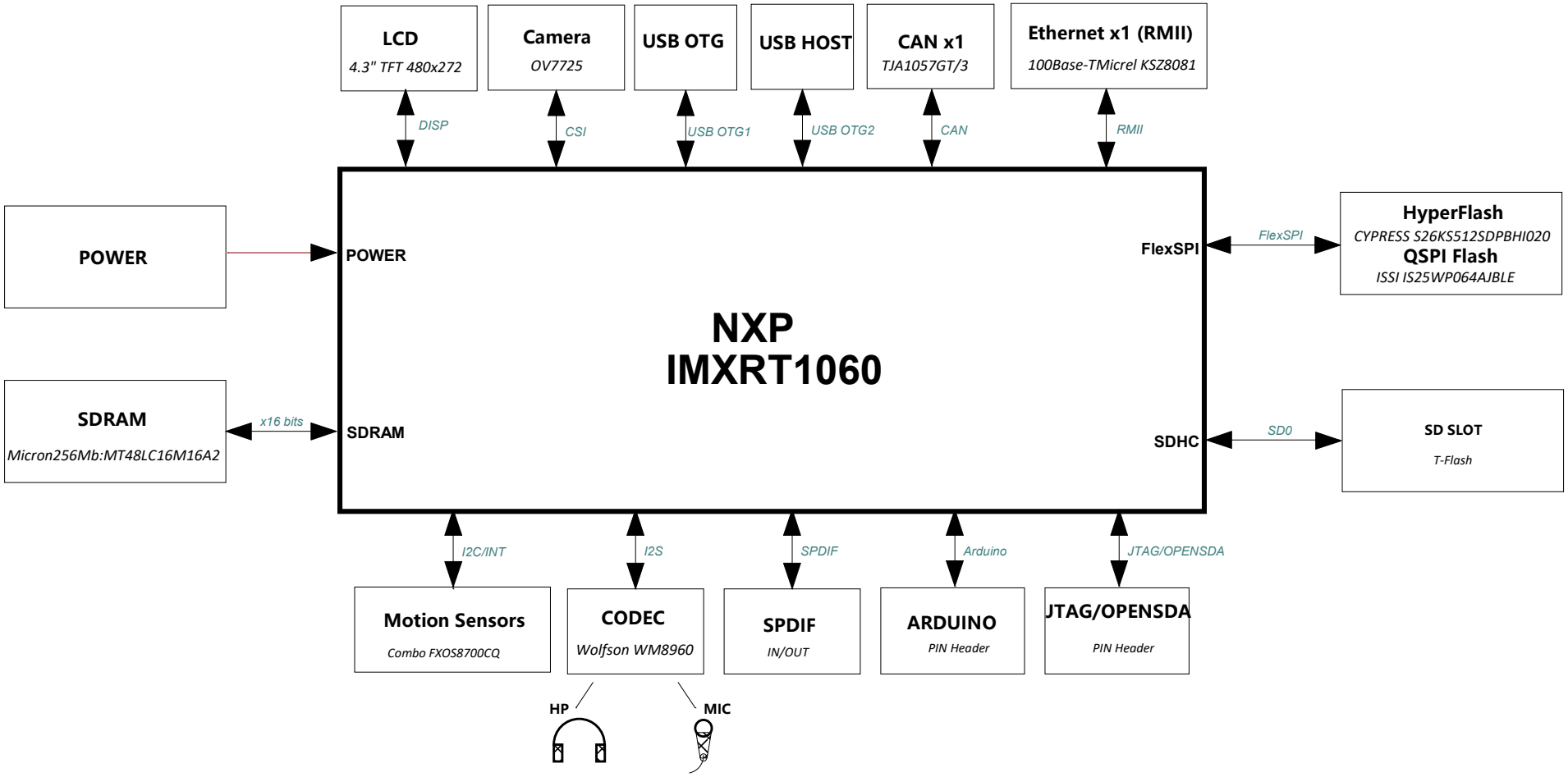
Blcok Diagram Rev A2#####

MIMXRT1060-EVK



ICAP Classification: CP: ___ IUO: X PUBI: ___

Drawing Title: MIMXRT1060-EVK

Page Title: BLOCK DIAGRAM

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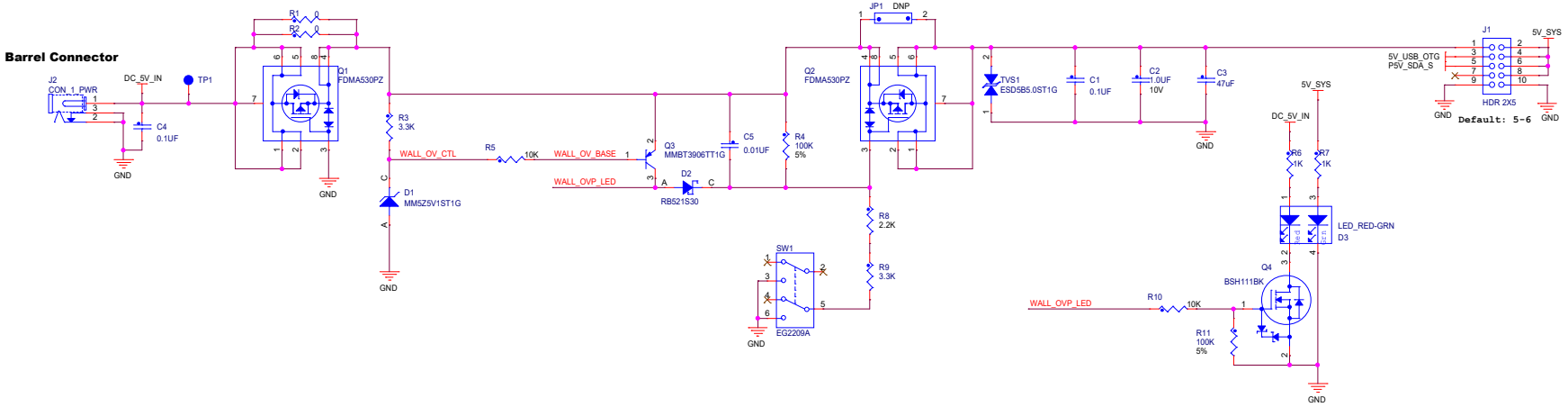
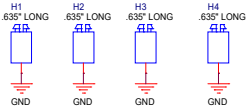
Main Power



Board Mounting Holes



Ground TPs

Layout Note: Place Ground TPs
to assist signal measurement.

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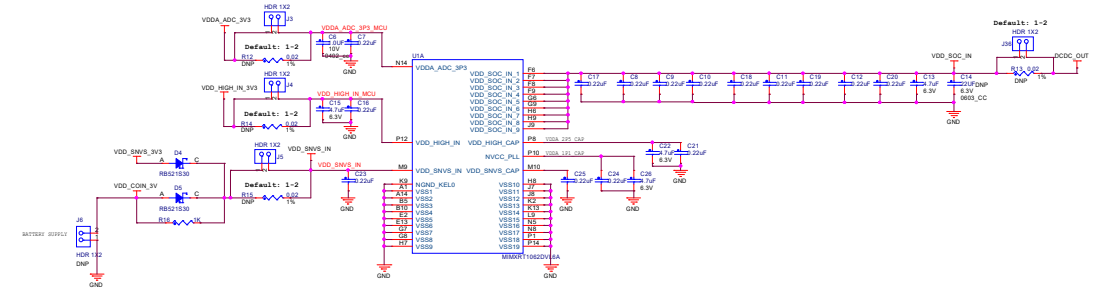
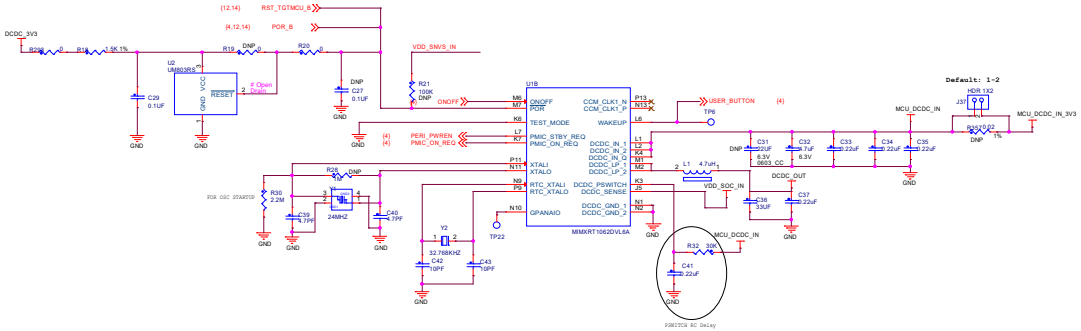
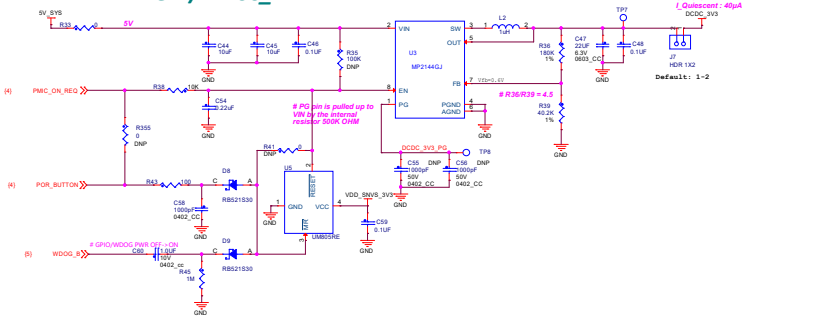


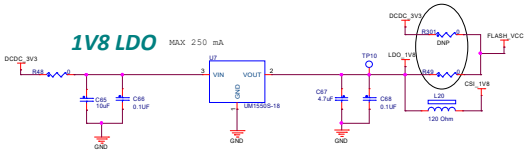




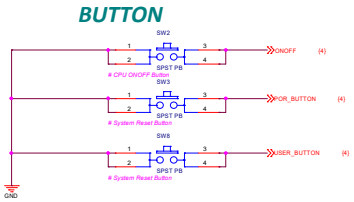
VDDHIGH / NVCC_xxx

FLASH VCC

1V8 LDO MAX 250 mA

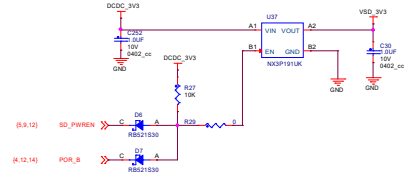


BUTTON

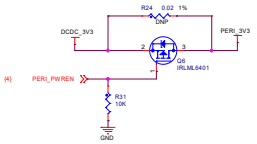


USER LED

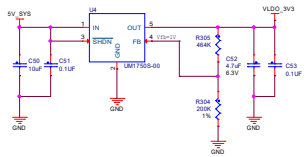
SD CARD POWER SWITCH



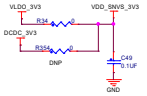
LCD 3V3 POWER SWITCH



3V3 LDO for SNVS

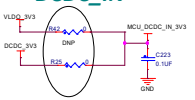


SNVS

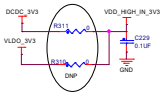


ADC

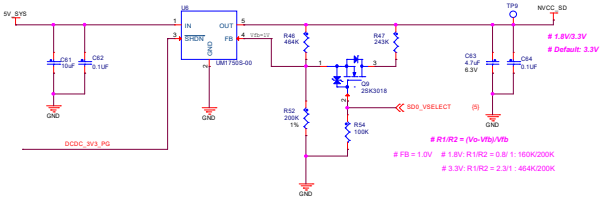
DCDC_IN



VDD_HIGH_IN



NVCC_SD <SD3.0> MAX 350 mA



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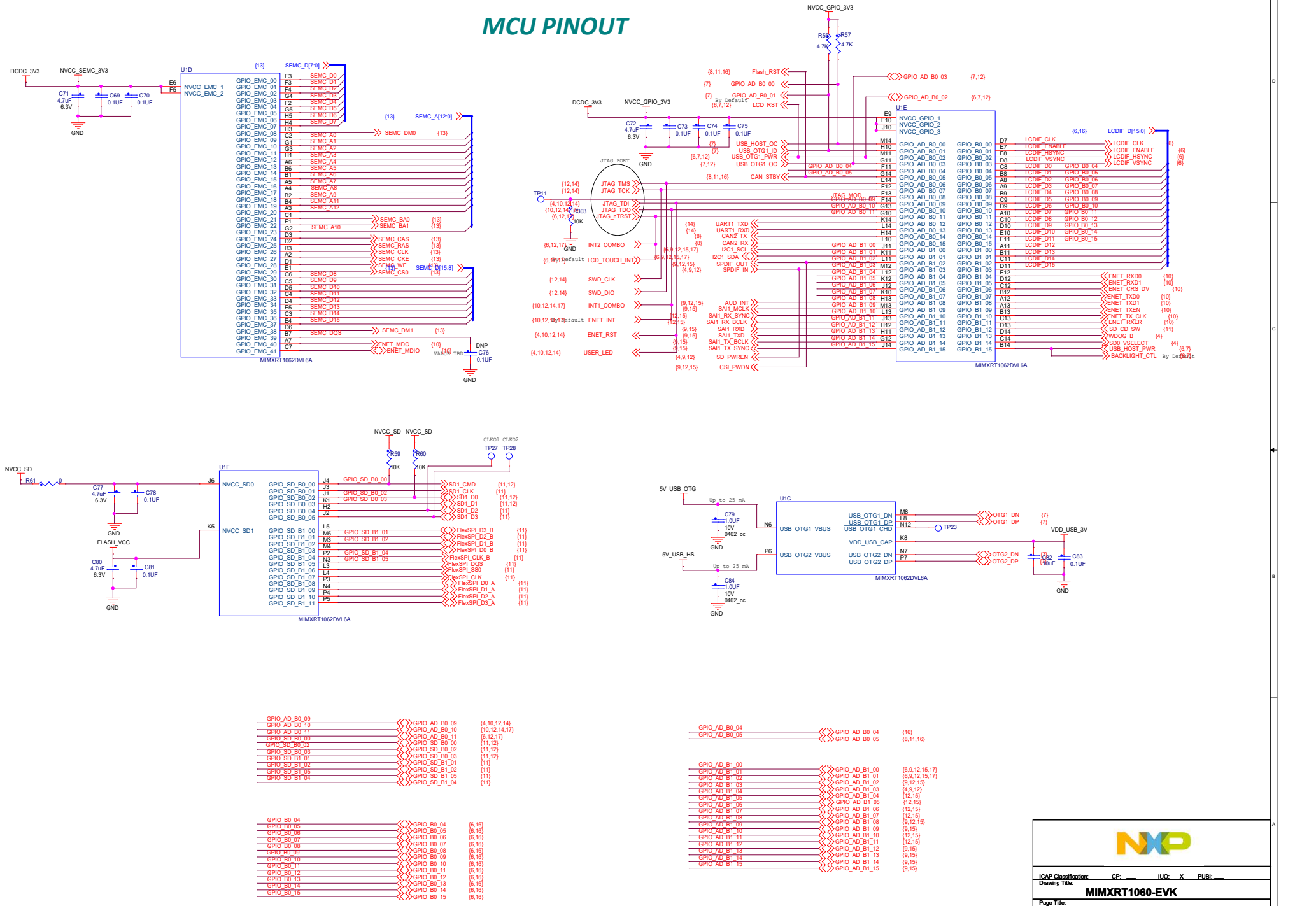
MCU PINOUT


U1D
MIMXRT1062DVL6A
U1E
MIMXRT1062DVL6A
U1F
MIMXRT1062DVL6A
U1C
MIMXRT1062DVL6A
JTAG_PORT
DCDC_3V3
NVCC_SEMC_3V3
NVCC_GPIO_3V3
NVCC_SD
5V_USB_OTG
5V_USB_HS
FLASH_VCC
GND
SEMC_D[7:0]
SEMC_A[12:0]
SEMC_BA0
SEMC_BA1
SEMC_CAS
SEMC_RAS
SEMC_CLK
SEMC_CKE
SEMC_WE
SEMC_CS0
SEMC_DQS
SEMC_DM0
SEMC_DM1
SEMC_A10
SEMC_B1[15:8]
ENET_MDC
ENET_MDIO
DNP
LCDIF_D[15:0]
LCDIF_CLK
LCDIF_ENABLE
LCDIF_HSYNC
LCDIF_VSYNC
Flash_RST
LCD_RST
CAN_STBY
USB_HOST_OC
USB_OTG1_ID
USB_OTG1_PWR
USB_OTG1_OC
JTAG_TMS
JTAG_TCK
JTAG_TDI
JTAG_TDO
JTAG_nTRST
JTAG_MOD
INT2_COMBO
LCD_TOUCH_INT
SWD_CLK
SWD_DIO
INT1_COMBO
ENET_INT
ENET_RST
USER_LED
UART1_TXD
UART1_RXD
CAN2_TX
CAN2_RX
I2C1_SCL
I2C1_SDA
SPDIF_OUT
SPDIF_IN
AUD_INT
SAI1_MCLK
SAI1_RX_SYNC
SAI1_RX_BCLK
SAI1_RXD
SAI1_TXD
SAI1_TX_BCLK
SAI1_TX_SYNC
SD_PWREN
CSI_PWDN
ENET_RXD0
ENET_RXD1
ENET_CRS_DV
ENET_TXD0
ENET_TXD1
ENET_TXEN
ENET_TX_CLK
ENET_RXER
SD_CD_SW
WDOG_B
SD0_VSELECT
USB_HOST_PWR
BACKLIGHT_CTL
SD1_CMD
SD1_CLK
SD1_D0
SD1_D1
SD1_D2
SD1_D3
FlexSPI_D3_B
FlexSPI_D2_B
FlexSPI_D1_B
FlexSPI_D0_B
FlexSPI_CLK_B
FlexSPI_DQS
FlexSPI_SS0
FlexSPI_CLK
FlexSPI_D0_A
FlexSPI_D1_A
FlexSPI_D2_A
FlexSPI_D3_A
USB_OTG1_VBUS
USB_OTG2_VBUS
USB_OTG1_DN
USB_OTG1_DP
USB_OTG1_CHD
VDD_USB_CAP
USB_OTG2_DN
USB_OTG2_DP
OTG1_DN
OTG1_DP
OTG2_DN
OTG2_DP
VDD_USB_3V
TP23
TP11
TP27
TP28
CLKO1
CLKO2
R55
R57
R59
R60
R303
R61
C71
C69
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C75
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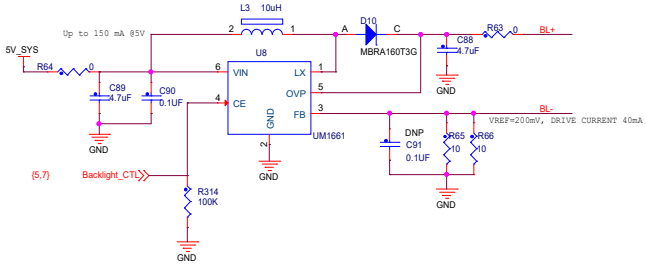
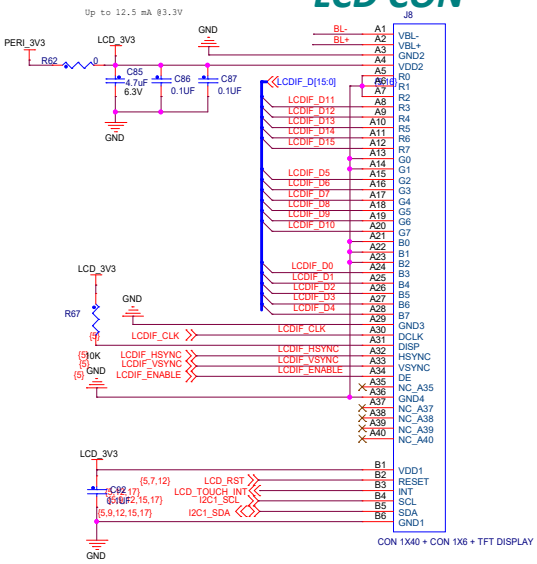
Backlight Control



LCD CON



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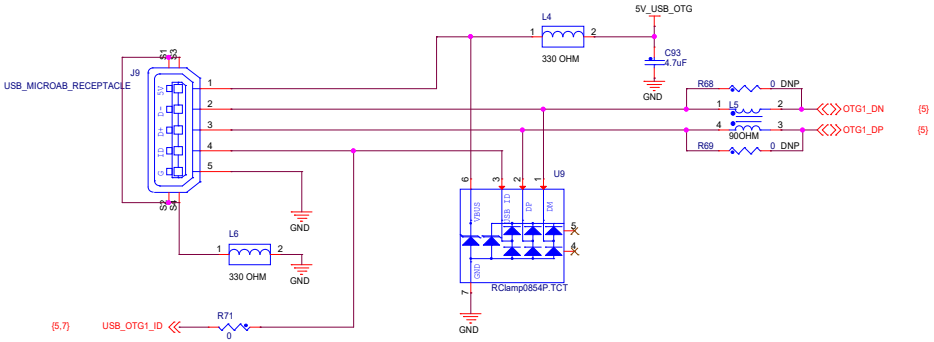
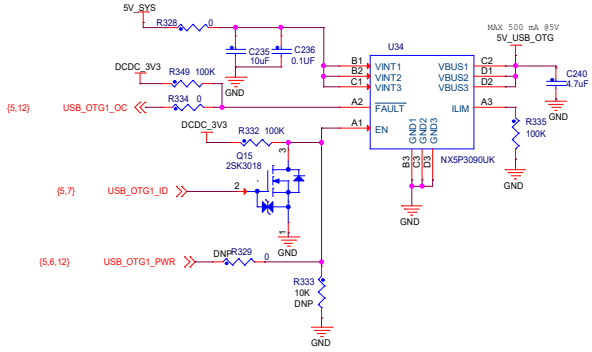
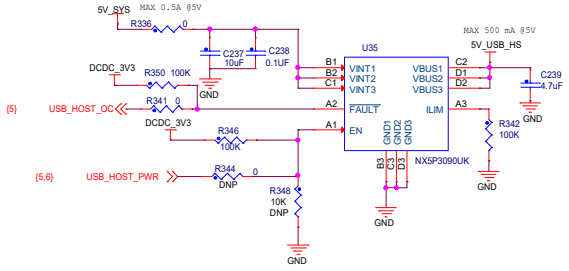
USB OTG

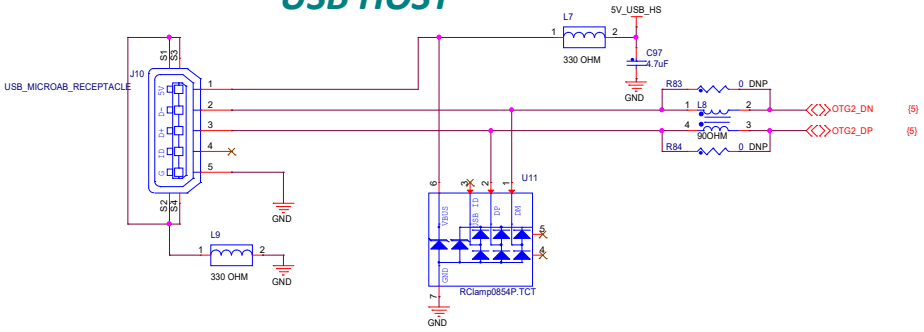


USB POWER





USB HOST



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Drawing Title:	MIMXRT1060-EVK	
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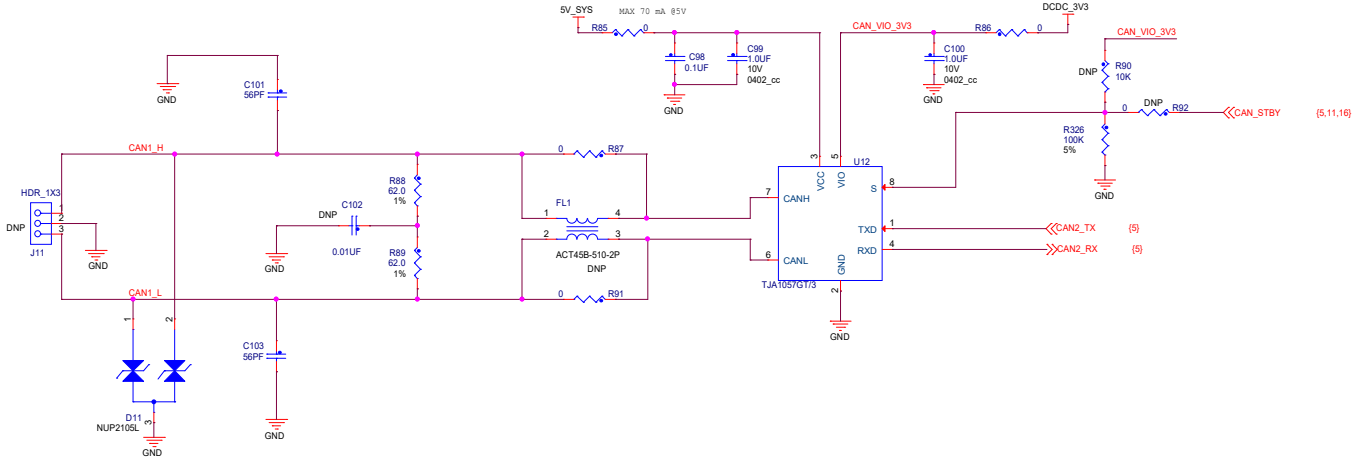
CAN BUS



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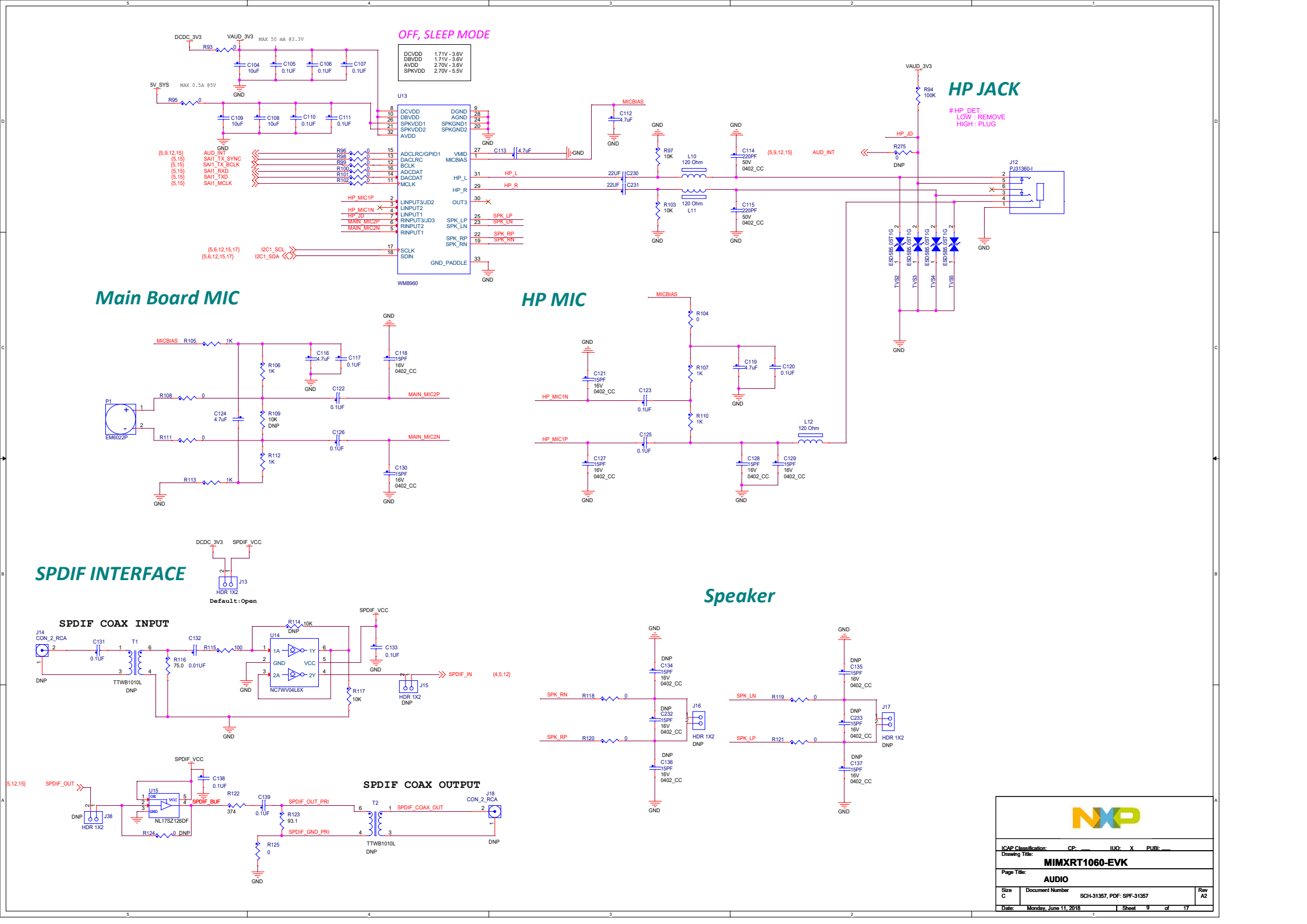
OFF, SLEEP MODE
DCVDD 1.71V - 3.6V
DBVDD 1.71V - 3.6V
AVDD 2.70V - 3.6V
SPKVDD 2.70V - 5.5V
WM8960
HP JACK
HP_DET:
LOW : REMOVE
HIGH : PLUG
Main Board MIC
HP MIC
SPDIF INTERFACE
SPDIF COAX INPUT
SPDIF COAX OUTPUT
Speaker
Default:Open
DNP
MIMXRT1060-EVK
AUDIO
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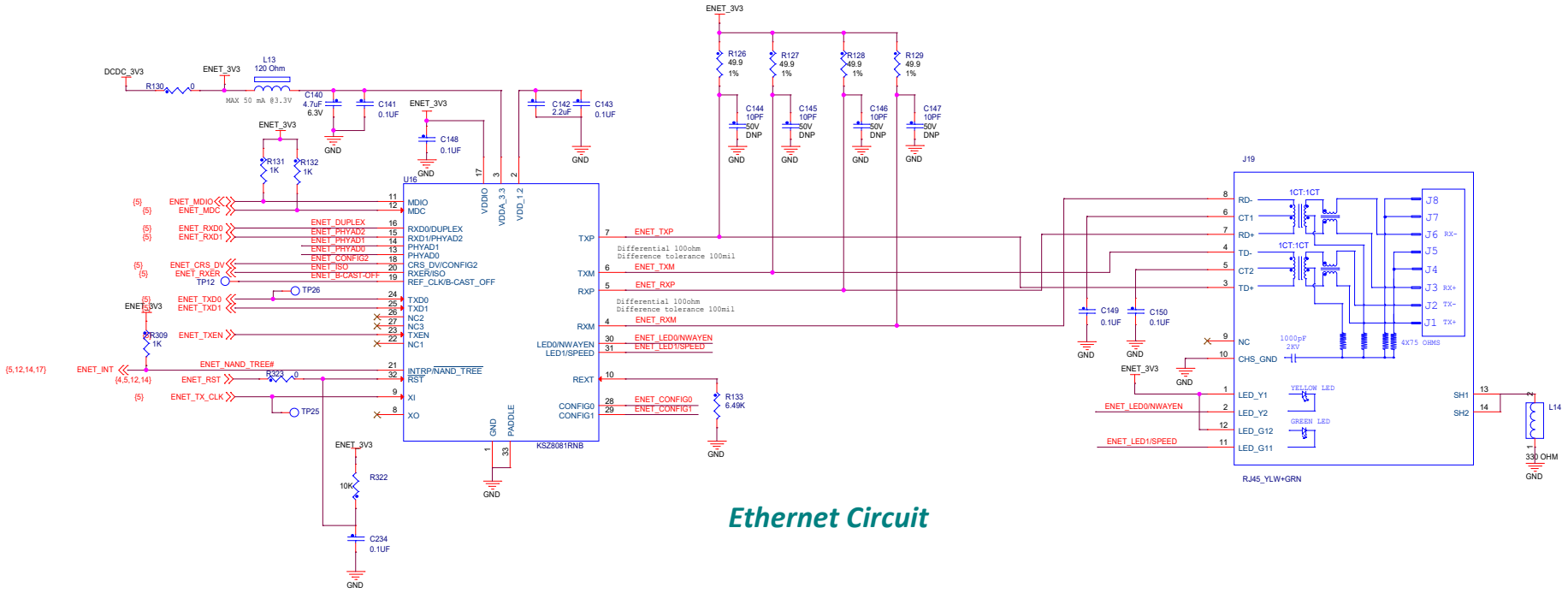
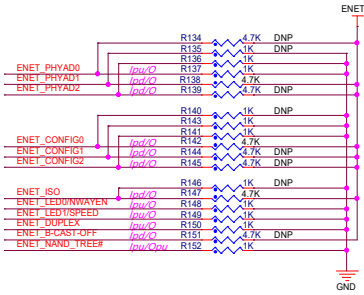


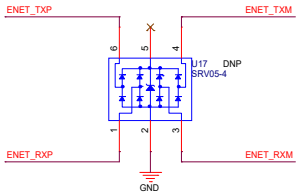
Ethernet Circuit



# CFG	Description
PHYAD[2:0]	PHY ADDR 00-XXX (00010 DEFAULT)
CONFIG[2:0]	IF MODE 001 RMII 101 RMII Back-to-Back xxx Reserved-not used
ISO	ISOLATE mode Pull-up = Enable Pull-down (default) = Disable
SPEED	SPEED mode Pull-up (default) = 100Mbps Pull-down = 10Mbps

# CFG	Description
DUPLEX	DUPLEX mode Pull-up (default) = Half Duplex Pull-down = Full Duplex
NWAYEN	Nway Auto-Negotiation Pull-up (default) = Enable Pull-down = Disable
B_CAST_OFF	Broadcast Off - for PHY Address 0 Pull-up = PHY Address 0 set as unique PHY addr Pull-down (default) = PHY Address 0 set as broadcast PHY addr
NAND_TREE#	NAND Tree Mode Pull-up (default) = Disable Pull-down = Enable

ESD PROTECTION



ICAP Classification: CP: ___ IUO: X PUBI: ___

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Page Title: **ETHERNET**

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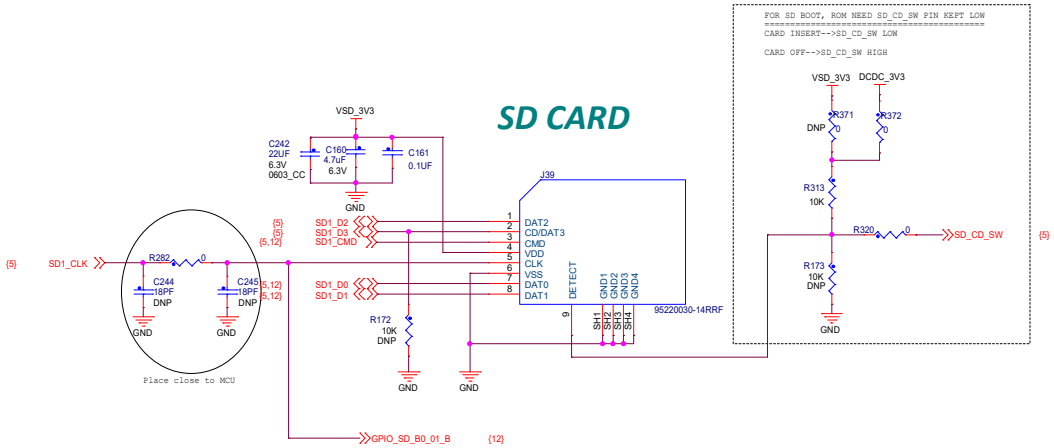
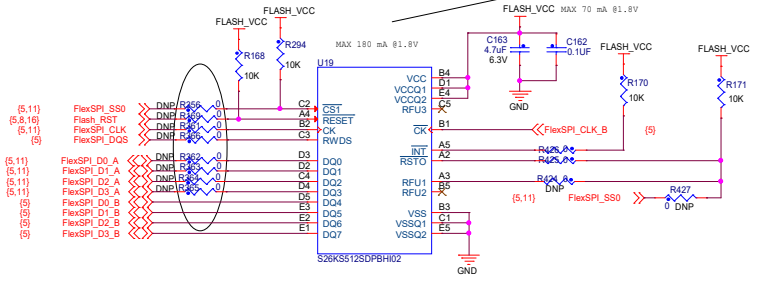
SD CARD



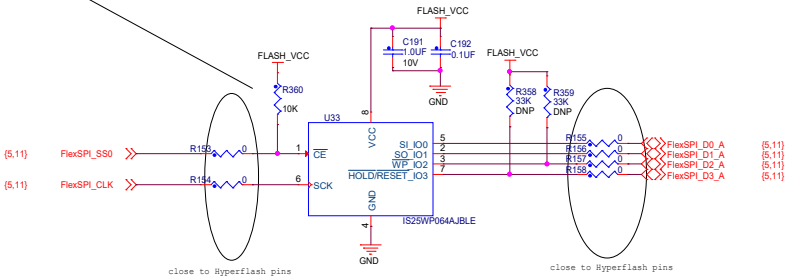
OPTION1: USE Hyperflash(DNP R153~R158, Mount R356,R361~R366)
OPTION2: USE QSPI FLASH(Mount R153~R158, DNP R356,R361~R366)

1V8 HyperFlash



Share the same package with S27KS0641DPBHI023
(if HYPERRAM is replaced, then DNP R425,R426,Mount R424,R427)

1V8 QSPI Flash



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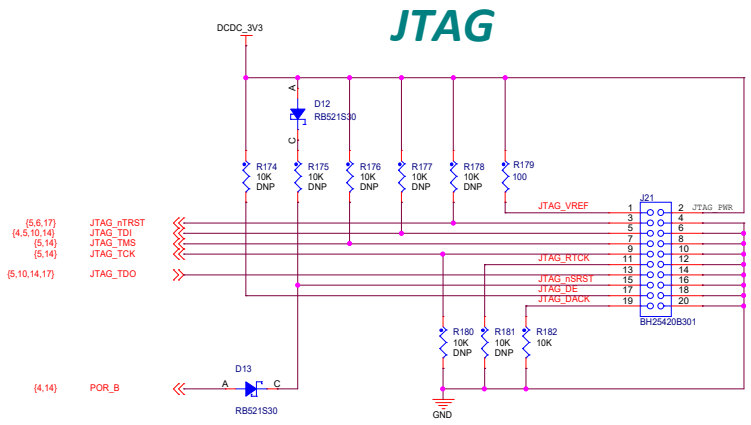
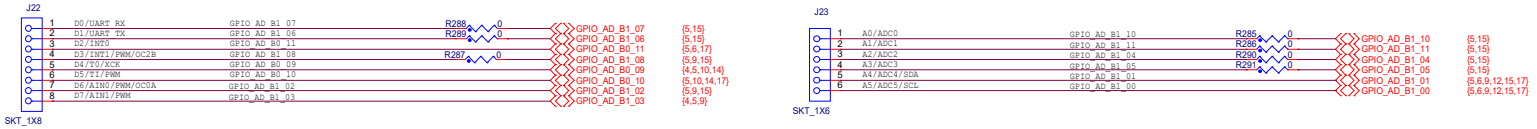
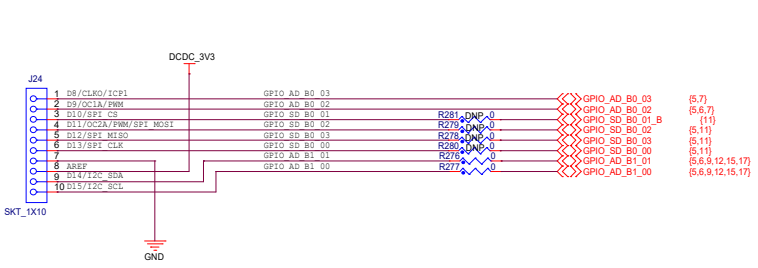
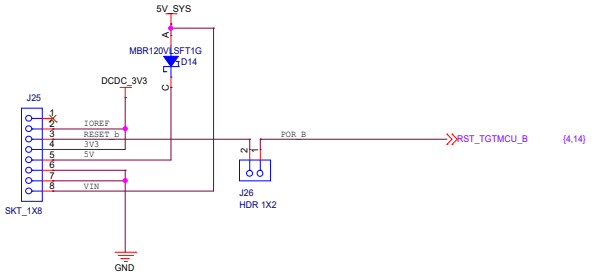


Arduino Interface







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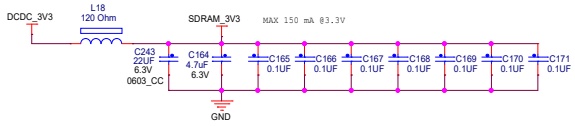
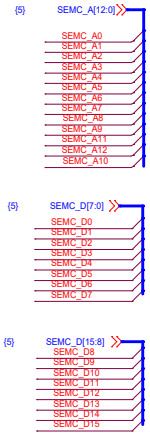
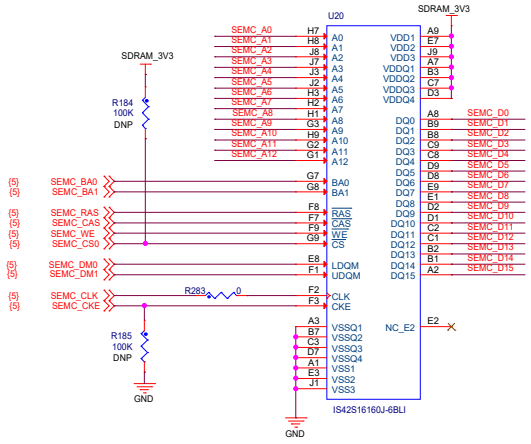
SDRAM







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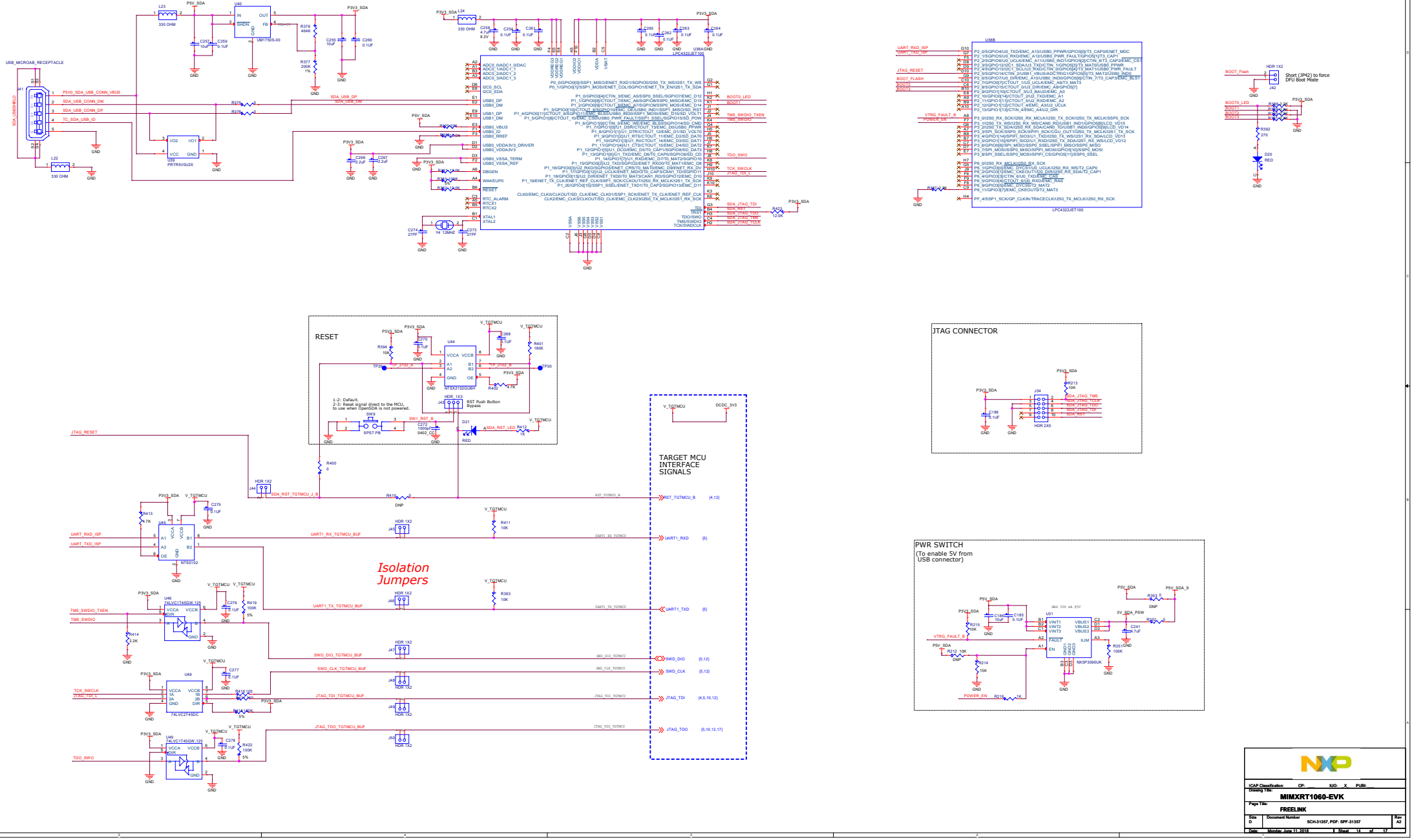
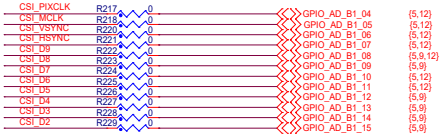
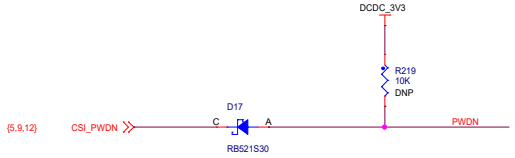
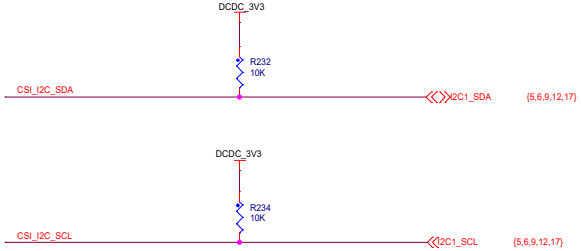
Freelink Interface



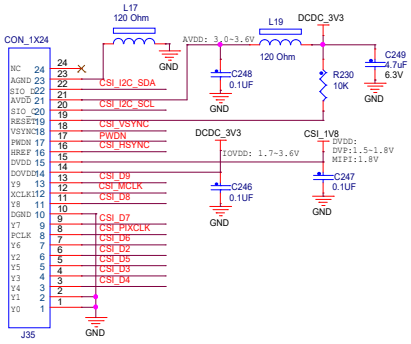
Camera Signals

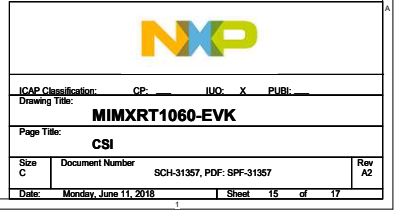






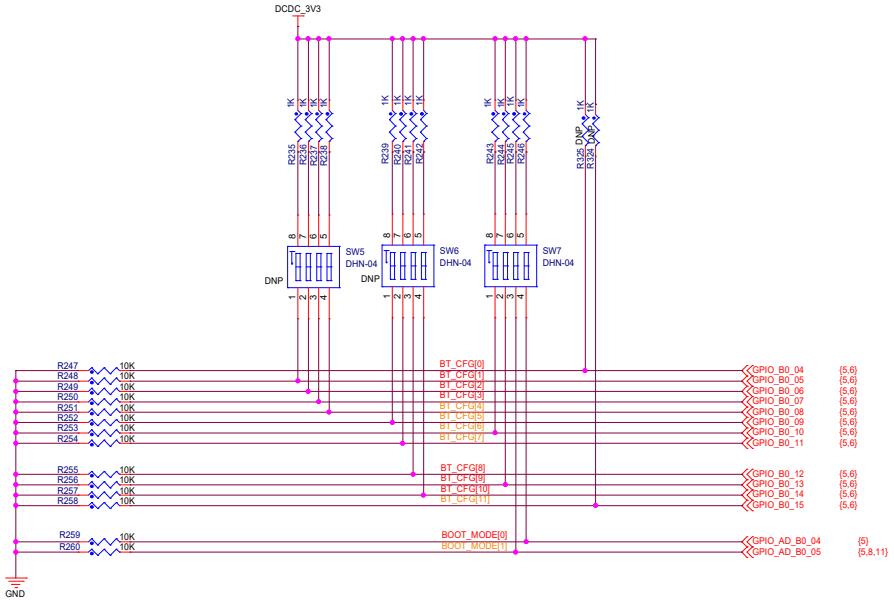
FPC FOR MT9M114/OV7725 MODULE





FUSE MAP

	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1	0/1
TYPE	**BOOT_CFG[11]**	**BOOT_CFG[10]**	**BOOT_CFG[9]**	**BOOT_CFG[8]**	**BOOT_CFG[7]**	**BOOT_CFG[6]**	**BOOT_CFG[5]**	**BOOT_CFG[4]**	**BOOT_CFG[3]**	**BOOT_CFG[2]**	**BOOT_CFG[1]**	**BOOT_CFG[0]**
FlexSPI1 - Serial NOR	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*FLASH_TYPE 000-Device supports 3B read by default 001-Device supports 4B read by default 010-HyperFlash 1V8 011-HyperFlash 3V3 100-MXIC Octal DDR*			*0*	*0*	*0*	*0*	*HOLD TIME: 00 - 500us 01 - 1ms 10 - 3ms 11 - 10ms*		*EncryptedXIP 0 - Disabled 1- Enabled*	*Reserved*
SD	*Infinit-Loop: (Debug USE only) 0 - Disable 1- Enable*	*Reserved*	*Bus Width: 0 - 1-bit 1 - 4-bit*	*SD1 VOLTAGE SELECTION: 0 - 3.3V 1 - 1.8V*	*0*	*1*	*SD/SDXC Speed: 00 - Normal/SDR12 01 - High/SDR25 10 - SDR50 11 - SDR104*		*SD Power Cycle Enable: '0' - No power cycle '1' - Enabled via USDHC_RST pad*	*SD Loopback Clock Source Sel: (for SDR50 and SDR104 only) '0' - through SD '1' - direct*	*Port Select: 0 - eSDHC1 1 - eSDHC2*	*Fast Boot: 0 - Regular 1 - Fast Boot*



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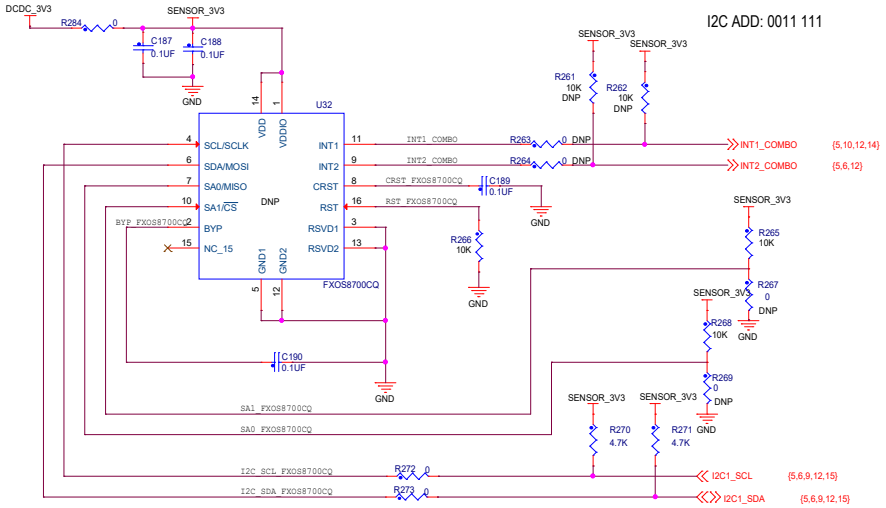
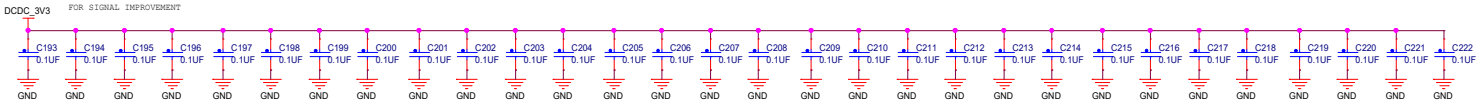
COMBO SENSOR



FXOS8700CQ COMBO SENSOR



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