ECE 111: RLE Project

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Part A:

1. Summary Page:

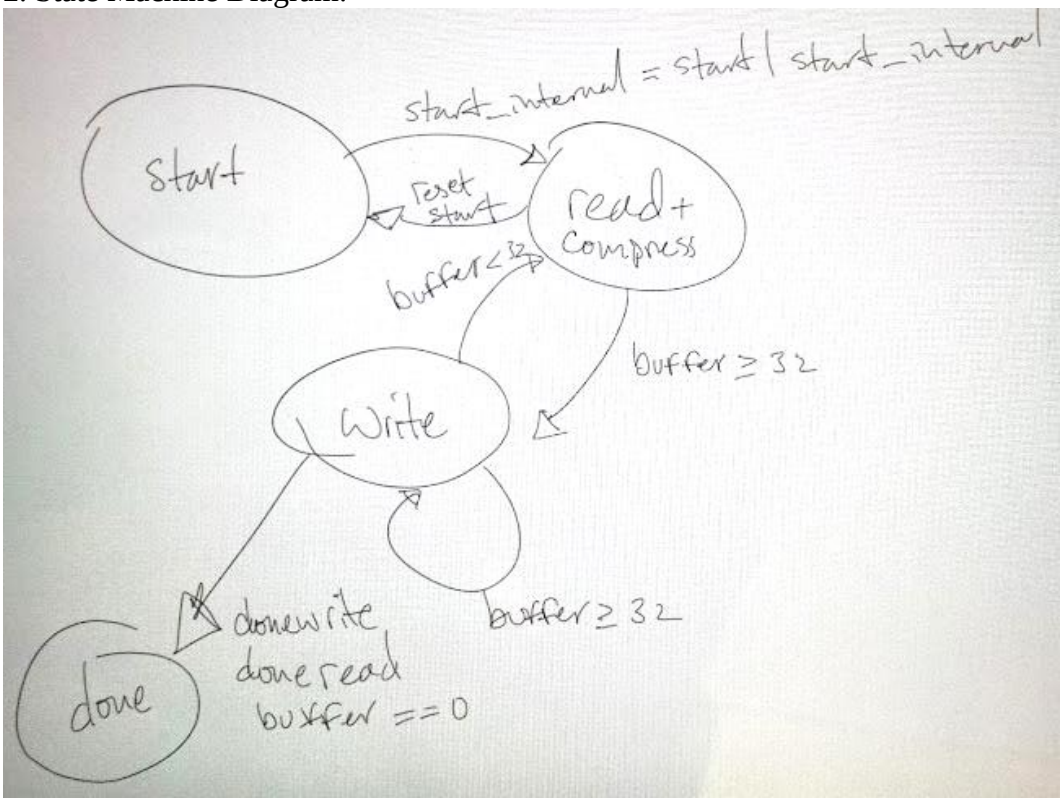
area: 1184 (1019 ALUTs + 165 regs)

#cycles: 55

clock period: 4.121ns (100C), 3.979ns (-40C)

total: 268.360e3 (100C), 259.112e3 (-40C)

2. State Machine Diagram:



3. Verilog Code: (see .v files in Part A folder)

4. ModelSim transcript and waveforms: (see Part A folder)
   a) rle_testbench.v
   b) rle_testbench2.v

5. Area and timing reports: (see .flow and .sta files in Part A folder)

Part B:

1. Summary Page:

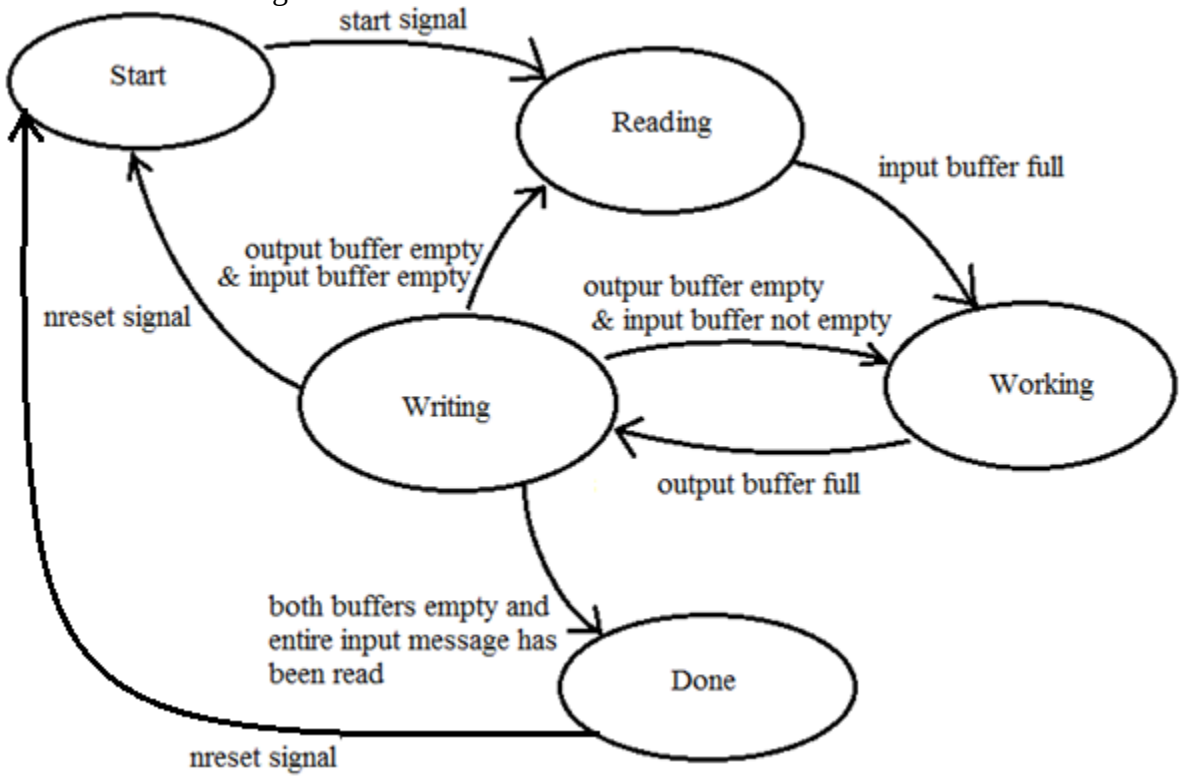
area: 335 (202 ALUTs + 133 regs)

#cycles: 153

clock period: 3.286ns

total: 168.424e3

2. State Machine Diagram:



3. Verilog Code: (see .v files in part B folder)

4. ModelSim transcript and waveforms: (see part B folder)
   a) rle_testbench.v
   b) rle_testbench2.v

5. Area and timing reports: (see .flow and .sta files in part B folder)