ECE 260C: SV-UVM based Verification Environment Development for YAPP Router

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Project Overview:

This project aims at developing a verification environment for a router design. The design under test (DUT) is called yapp router, where yapp stands for “yet another packet protocol”. Due to the limited time period of a month for this project, our focus was development of a well-structured and detailed UVM verification environment, instead of thorough testing and coverage. Mentioned below are the details of this design:

High level diagram of YAPP-Router:

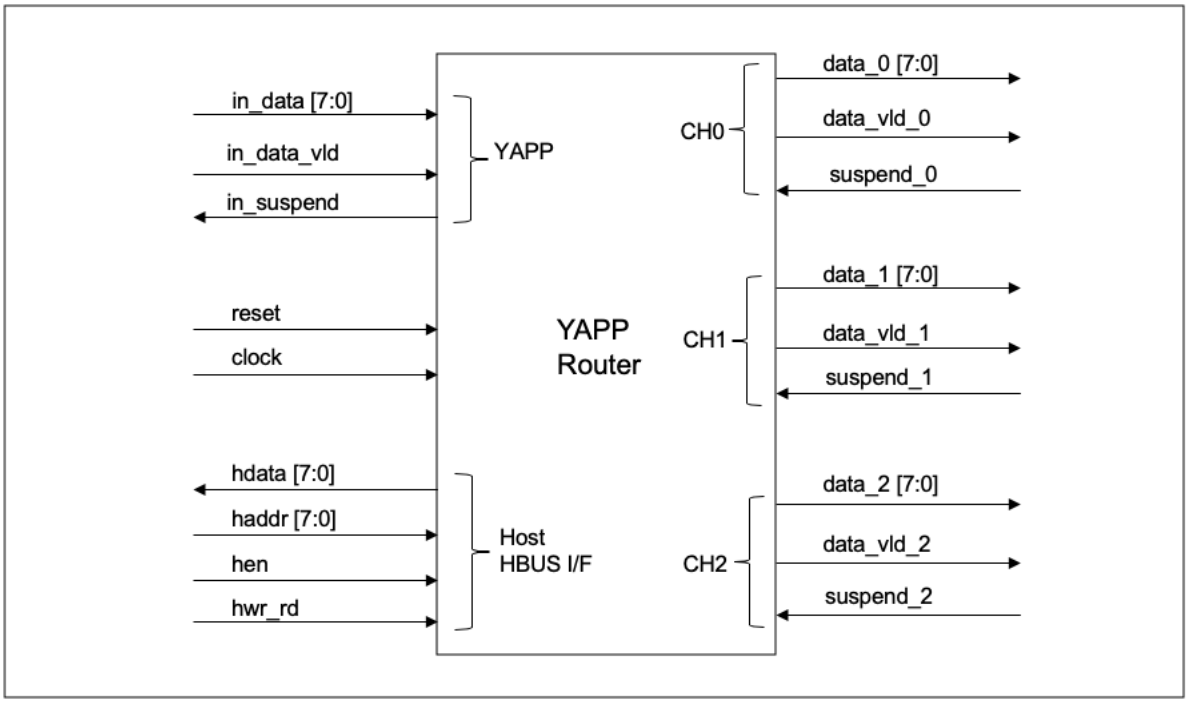


Fig1: YAPP Router DUT

Packet router description:

The packet router accepts data packets on a single input port, in_data, and routes the packets to one of three output channels: channel 0, channel 1 or channel 2. The input and output ports have slightly different signal protocols. The router also has a host interface for programming registers that are described next.

Packet data specification:

A packet is a sequence of bytes with the first byte containing a header, the next variable set of bytes containing payload, and the last byte containing parity.
The header consists of a two-bit address field and six-bit length field. The address field is used to determine which output channel the packet should be routed to, with the address 3 being illegal. The length field specifies the number of data bytes (payload). A packet can have a minimum payload size of 1 byte and maximum of 63 bytes.

The parity is a byte of even, bitwise parity, calculated over the header and payload bytes of the packet.

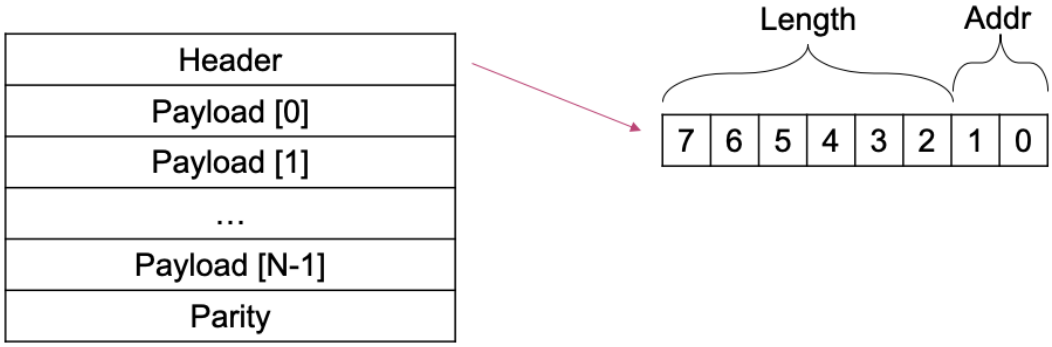
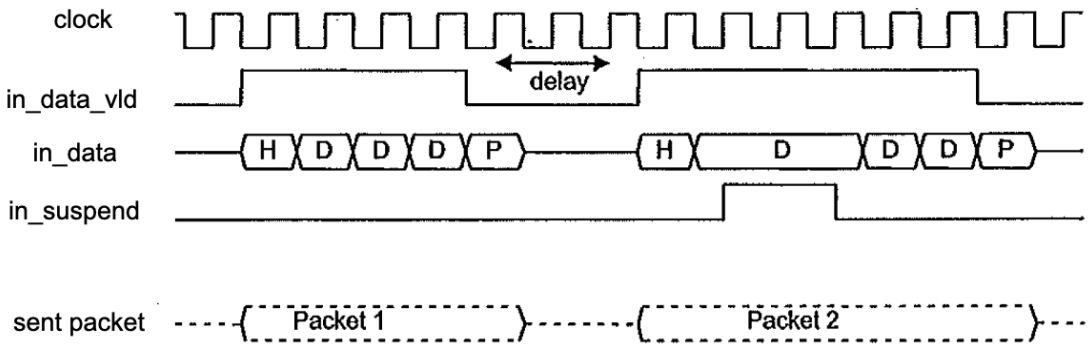


Fig2: YAPP Packet Structure

Input Port Protocol:

All input signals are active high and are to be driven on the falling edge of the clock. The in_data_valid signal must be asserted on the same clock when the first byte of the packet (the header byte), is driven onto the in_data bus. As the header byte contains the address, this tells the router to which output channel the packet needs to be routed. Each subsequent byte of data needs to be driven on the data bus with each falling clock.

After the last payload byte has been driven, on the next falling clock, the in_data_valid signal must be de-asserted, and the packet parity byte needs to be driven. The input data cannot change while in_suspend signal is active (indicating FIFO full).



H = Header, D = Data, P = Parity

Fig3: Input Port Protocol

Output Port Protocol (Channel Ports):

All output signals are active high and are to be sampled on the falling edge of the clock. Each output port is internally buffered by a FIFO of depth 16 and a width of 1 byte. The router asserts the data_valid_x signal when valid data appears on the data_x output bus. The suspend_x input signal must then be de-asserted on the falling clock edge in which data is read from the data_x bus. As long the suspend_x signal remains inactive, the data_x bus drives a new valid packet byte on each rising clock edge.

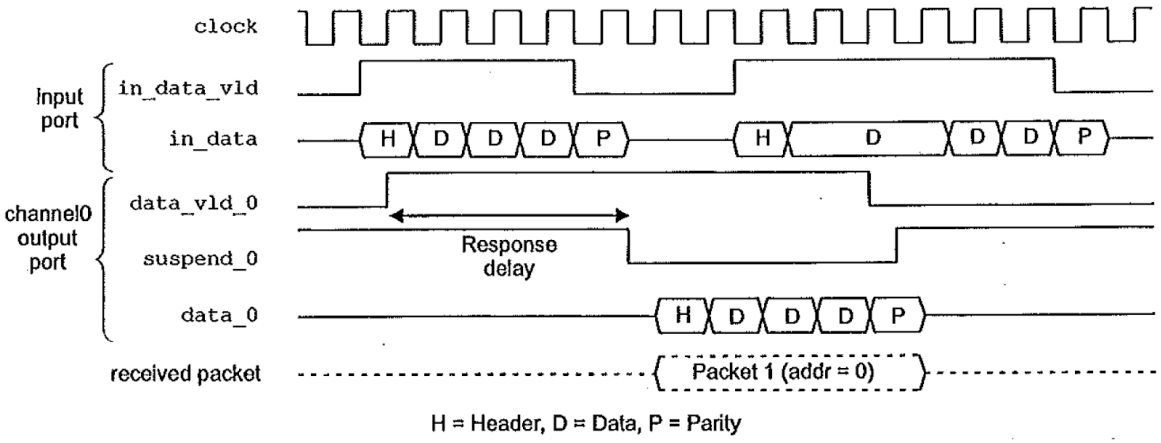


Fig4: Output Port Protocol

Host Interface Port Protocol (HBUS):

All input signals are active high and are to be driven on the falling edge of the clock. The host port provides synchronous read/write access to program the router.

A WRITE operation takes one cycle as follows:

- hwr_rd and hen must be 1. Data on hdata is then clocked on the next rising clock edge into the register based on haddr decode.
- hen is driven to 0 in the next cycle.

A READ operation takes two cycles as follows:

- hwr_rd must be 0 and hen must be 1. In the first clock cycle, haddr is sampled and hdata is driven by the design (DUT) in the second clock cycle.
- hen is then driven to 0 after the cycle 2 ends.

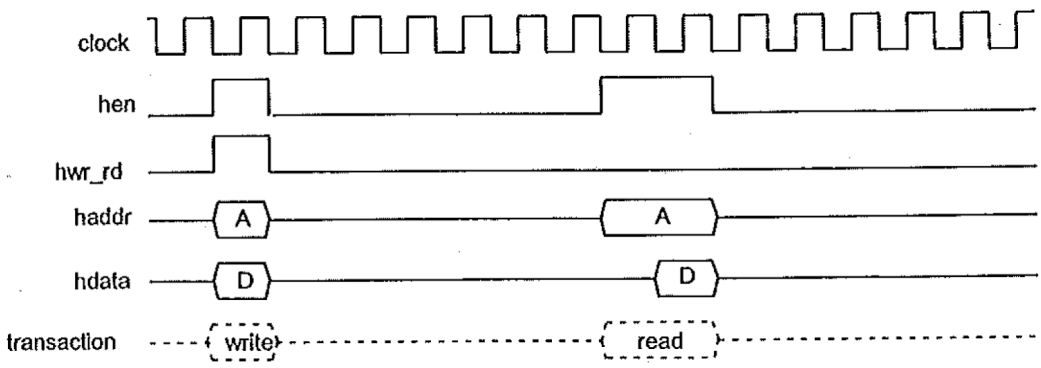


Fig5: HBUS Protocol

Verification Environment Plan:

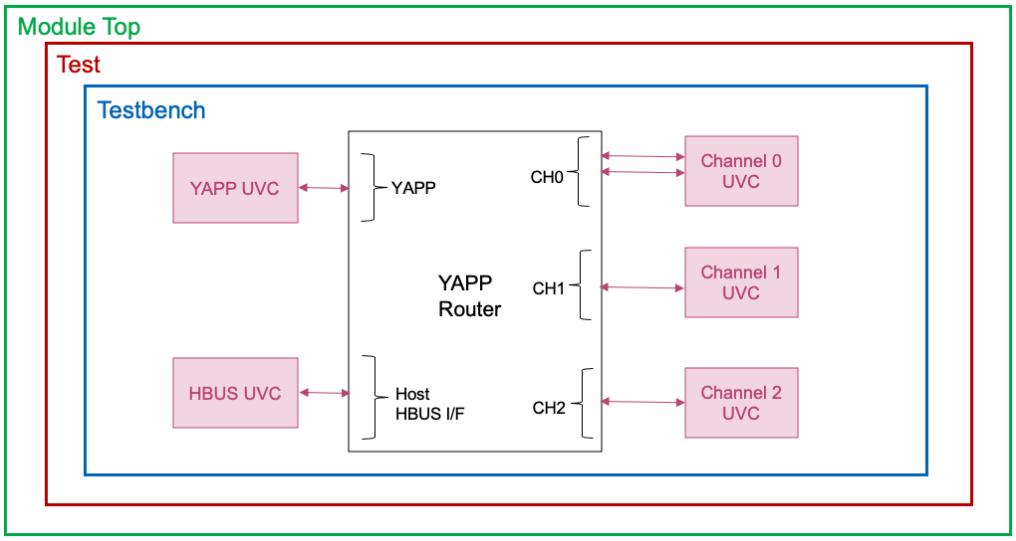


Fig6: Verification Environment for YAPP Router DUT

UVM Verification Component:

UVM Verification Component (UVC) emulates a design. It is an abstraction of the stimulus and monitoring needed to verify a design component, interface or protocols. It is defined by a set of classes and methods in the UVM library. It is mainly developed by uvm_components, uvm_env & uvm_test.

Env instantiates and configures ***agents. Agent*** contains three subcomponents: a ***driver, sequencer***, and ***monitor.*** If the agent is active, subtypes should contain all three subcomponents. If the agent is passive, subtypes should contain only the monitor.

Sequence is a series of ***transactions/packets*** which is of the type uvm_sequence_item. ***Sequencer*** is responsible for the coordination between sequence and driver. Sequencer sends the transaction to the driver and gets the response from the driver.

Driver drives stimulus into the signals of DUT and ***Monitor*** observes/samples the signal interface of DUT.

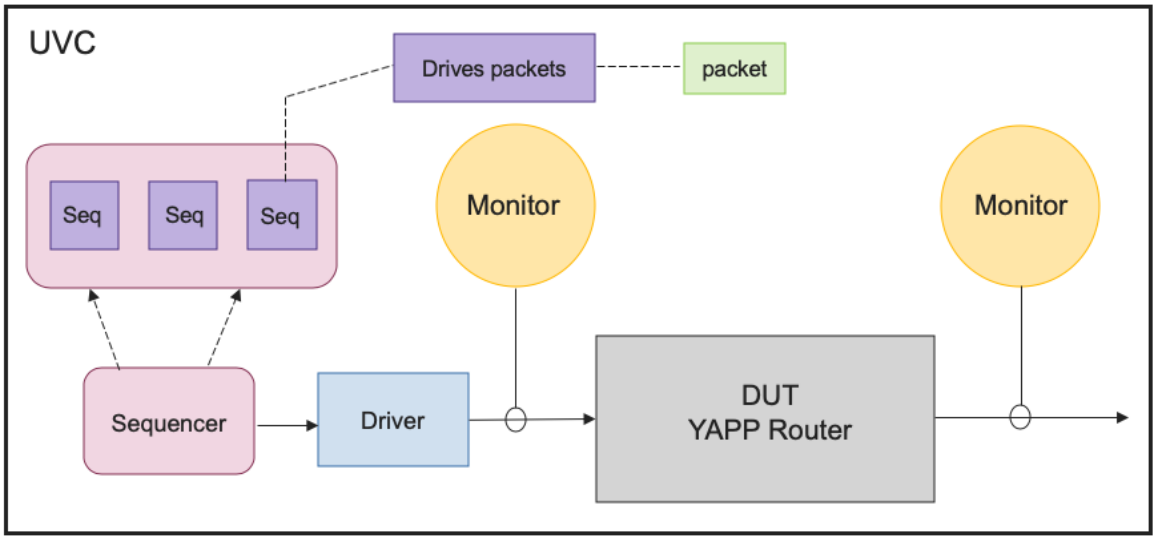


Fig7: Generic UVM Verification Component

Milestones:

We have completed all of the milestones provided in the project objectives.

Milestone 1	Understanding the design under test and building a plan for development of the verification environment from it.
Milestone 2	Development of UVC for YAPP to drive & monitor the input channel of router
Milestone 3	Development of UVC for Channels, to monitor & drive the output channels of the router
Milestone 4	Development of UVC for HBUS Interface
Milestone 5	Connecting the UVCs to the DUT & development of testbench
Milestone 6	Development of top module
Milestone 7	Development of test which calls uvm sequences of different UVCs

Grading:

Assigned grades for milestone:

Grade	Milestones
B+	1, 2
A-	1, 2, 3, 4
A	1, 2, 3, 4, 5, 6
A+	1, 2, 3, 4, 5, 6, 7

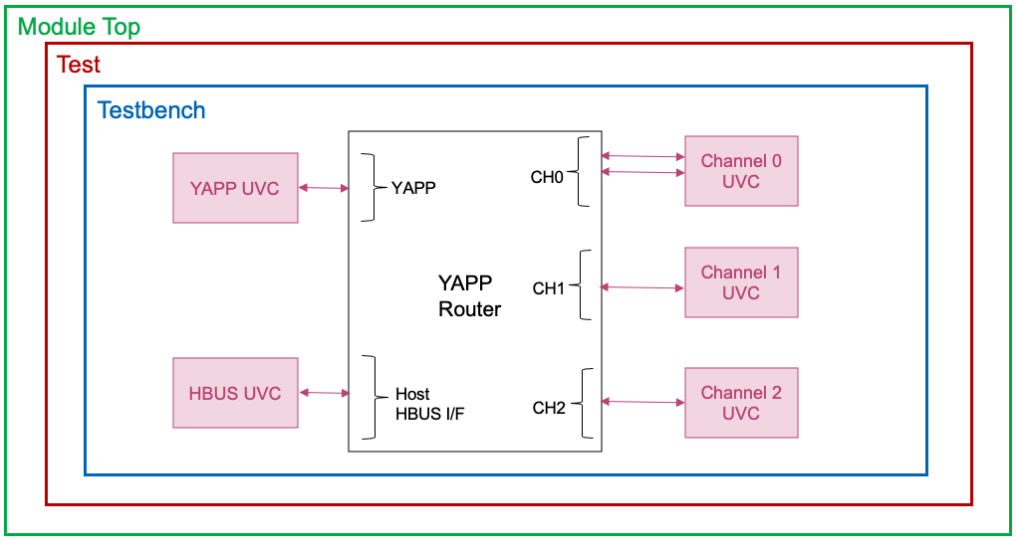
Code:

https://www.edaplayground.com/x/pYq

Results:

Build Result:

Successful and accurate build result is displayed below along with a block diagram for reference.



```
# ----------------------------------------------------------------------
# Name                          Type                        Size  Value
# ----------------------------------------------------------------------
# uvm_test_top                  simple_test                 -     @485
#   tb                          router_tb                   -     @499
#     chan0                     channel_env                 -     @530
#       monitor                 channel_monitor             -     @561
#         item_collected_port   uvm_analysis_port           -     @569
#         resp_collected_port   uvm_analysis_port           -     @577
#         instance_id           string                      9     Channel_0
#         checks_enable         integral                    1     'h1
#         coverage_enable       integral                    1     'h1
#       rx_agent                channel_rx_agent            -     @554
#         driver                channel_rx_driver           -     @699
#           rsp_port            uvm_analysis_port           -     @714
#           seq_item_port       uvm_seq_item_pull_port      -     @706
#         sequencer             channel_rx_sequencer        -     @590
#           rsp_export          uvm_analysis_export         -     @597
#           seq_item_export     uvm_seq_item_pull_imp       -     @691
#           arbitration_queue   array                       0     -
#           lock_queue          array                       0     -
#           num_last_reqs       integral                    32    'd1
#           num_last_rsps       integral                    32    'd1
#         monitor               channel_monitor             -     @561
#         is_active             uvm_active_passive_enum     1     UVM_ACTIVE
#       has_tx                  integral                    1     'h0
#       has_rx                  integral                    1     'h1
#       checks_enable           integral                    1     'h1
#       coverage_enable         integral                    1     'h1
#     chan1                     channel_env                 -     @537
#       monitor                 channel_monitor             -     @734
#         item_collected_port   uvm_analysis_port           -     @742
#         resp_collected_port   uvm_analysis_port           -     @750
#         instance_id           string                      9     Channel_1
#         checks_enable         integral                    1     'h1
#         coverage_enable       integral                    1     'h1
#       rx_agent                channel_rx_agent            -     @727
#         driver                channel_rx_driver           -     @872
#           rsp_port            uvm_analysis_port           -     @887
#           seq_item_port       uvm_seq_item_pull_port      -     @879
#         sequencer             channel_rx_sequencer        -     @763
#           rsp_export          uvm_analysis_export         -     @770
#           seq_item_export     uvm_seq_item_pull_imp       -     @864
#           arbitration_queue   array                       0     -
#           lock_queue          array                       0     -
#           num_last_reqs       integral                    32    'd1
#           num_last_rsps       integral                    32    'd1
#         monitor               channel_monitor             -     @734
#         is_active             uvm_active_passive_enum     1     UVM_ACTIVE
#       has_tx                  integral                    1     'h0
#       has_rx                  integral                    1     'h1
#       checks_enable           integral                    1     'h1
#       coverage_enable         integral                    1     'h1
#     chan2                     channel_env                 -     @544
```

```
#       monitor                channel_monitor          -     @907
#         item_collected_port  uvm_analysis_port        -     @915
#         resp_collected_port  uvm_analysis_port        -     @923
#         instance_id          string                   9     Channel_2
#         checks_enable        integral                 1     'h1
#         coverage_enable      integral                 1     'h1
#       rx_agent               channel_rx_agent         -     @900
#         driver               channel_rx_driver        -     @1045
#           rsp_port           uvm_analysis_port        -     @1060
#           seq_item_port      uvm_seq_item_pull_port   -     @1052
#         sequencer            channel_rx_sequencer     -     @936
#           rsp_export         uvm_analysis_export      -     @943
#           seq_item_export    uvm_seq_item_pull_imp    -     @1037
#           arbitration_queue  array                    0     -
#           lock_queue         array                    0     -
#           num_last_reqs      integral                 32    'd1
#           num_last_rsps      integral                 32    'd1
#         monitor              channel_monitor          -     @907
#         is_active            uvm_active_passive_enum  1     UVM_ACTIVE
#       has_tx                 integral                 1     'h0
#       has_rx                 integral                 1     'h1
#       checks_enable          integral                 1     'h1
#       coverage_enable        integral                 1     'h1
#     hbus                     hbus_env                 -     @523
#       masters[0]             hbus_master_agent        -     @1089
#         driver               hbus_master_driver       -     @1209
#           rsp_port           uvm_analysis_port        -     @1224
#           seq_item_port      uvm_seq_item_pull_port   -     @1216
#           random_delay       integral                 1     'h0
#           master_id          integral                 32    'h0
#         sequencer            hbus_master_sequencer    -     @1100
#           rsp_export         uvm_analysis_export      -     @1107
#           seq_item_export    uvm_seq_item_pull_imp    -     @1201
#           arbitration_queue  array                    0     -
#           lock_queue         array                    0     -
#           num_last_reqs      integral                 32    'd1
#           num_last_rsps      integral                 32    'd1
#         monitor              hbus_monitor             -     @1073
#         is_active            uvm_active_passive_enum  1     UVM_ACTIVE
#         master_id            integral                 32    'h0
#       monitor                hbus_monitor             -     @1073
#         item_collected_port  uvm_analysis_port        -     @1080
#         checks_enable        integral                 1     'h1
#         coverage_enable      integral                 1     'h1
#       num_masters            integral                 32    'h1
#       num_slaves             integral                 32    'h0
#       checks_enable          integral                 1     'h1
#       coverage_enable        integral                 1     'h1
#     yapp                     yapp_env                 -     @516
#       tx_agent               yapp_tx_agent            -     @1239
#         driver               yapp_tx_driver           -     @1366
#           rsp_port           uvm_analysis_port        -     @1381
#           seq_item_port      uvm_seq_item_pull_port   -     @1373
#         monitor              yapp_tx_monitor          -     @1250
```

```
#         sequencer            yapp_tx_sequencer        -     @1257
#           rsp_export         uvm_analysis_export      -     @1264
#           seq_item_export    uvm_seq_item_pull_imp    -     @1358
#           arbitration_queue  array                     0     -
#           lock_queue         array                     0     -
#           num_last_reqs      integral                  32    'd1
#           num_last_rsps      integral                  32    'd1
#         is_active            uvm_active_passive_enum  1     UVM_ACTIVE
# ----------------------------------------------------------------------
```

Simulation Results:

YAPP Packet sent to Channel 0

```
#  UVM_INFO  yapp_tx_monitor.sv(59)  @  500  ns:  uvm_test_top.tb.yapp.tx_agent.monitor
[yapp_tx_monitor] Packet Collected :
# ---------------------------------------------
# Name              Type          Size  Value
# ---------------------------------------------
# packet_collected  yapp_packet   -     @1403
#   length          integral      6     'h12
#   addr            integral      2     'h0
#   payload         da(integral)  18    -
#     [0]           integral      8     'h19
#     [1]           integral      8     'h4a
#     [2]           integral      8     'h63
#     [3]           integral      8     'hbf
#     [4]           integral      8     'he1
#     ...           ...           ...   ...
#     [13]          integral      8     'h30
#     [14]          integral      8     'h29
#     [15]          integral      8     'hfc
#     [16]          integral      8     'hd
#     [17]          integral      8     'h81
#   parity          integral      8     'h23
#   packet_delay    integral      32    'd0
#   begin_time      time          64    120 ns
#   end_time        time          64    500 ns
# ---------------------------------------------


#   UVM_INFO   channel_monitor.sv(173)   @   640   ns:   uvm_test_top.tb.chan0.monitor
[channel_monitor] Channel_0 Packet collected :
# ---------------------------------------------
# Name              Type          Size  Value
# ---------------------------------------------
# packet_collected  yapp_packet   -     @1450
#   length          integral      6     'h12
#   addr            integral      2     'h0
#   payload         da(integral)  18    -
#     [0]           integral      8     'h19
#     [1]           integral      8     'h4a
#     [2]           integral      8     'h63
#     [3]           integral      8     'hbf
#     [4]           integral      8     'he1
#     ...           ...           ...   ...
#     [13]          integral      8     'h30
#     [14]          integral      8     'h29
#     [15]          integral      8     'hfc
#     [16]          integral      8     'hd
#     [17]          integral      8     'h81
#   parity          integral      8     'h23
#   packet_delay    integral      32    'd0
#   begin_time      time          64    240 ns
#   end_time        time          64    640 ns
# ---------------------------------------------
```

YAPP Packet sent to Channel 1

```
# UVM_INFO yapp_tx_monitor.sv(59) @ 1020 ns: uvm_test_top.tb.yapp.tx_agent.monitor
[yapp_tx_monitor] Packet Collected :
# ---------------------------------------------
# Name              Type          Size  Value
# ---------------------------------------------
# packet_collected  yapp_packet   -     @1403
#   length          integral      6     'h11
#   addr            integral      2     'h1
#   payload         da(integral)  17    -
#     [0]           integral      8     'h69
#     [1]           integral      8     'h18
#     [2]           integral      8     'h97
#     [3]           integral      8     'ha3
#     [4]           integral      8     'hcb
#     ...           ...           ...   ...
#     [12]          integral      8     'h52
#     [13]          integral      8     'h3a
#     [14]          integral      8     'he2
#     [15]          integral      8     'h1c
#     [16]          integral      8     'h67
#   parity          integral      8     'h37
#   packet_delay    integral      32    'd0
#   begin_time      time          64    660 ns
#   end_time        time          64    1020 ns
# ---------------------------------------------


# UVM_INFO channel_monitor.sv(173) @ 1240 ns: uvm_test_top.tb.chan1.monitor
[channel_monitor] Channel_1 Packet collected :
# ---------------------------------------------
# Name              Type          Size  Value
# ---------------------------------------------
# packet_collected  yapp_packet   -     @1435
#   length          integral      6     'h11
#   addr            integral      2     'h1
#   payload         da(integral)  17    -
#     [0]           integral      8     'h69
#     [1]           integral      8     'h18
#     [2]           integral      8     'h97
#     [3]           integral      8     'ha3
#     [4]           integral      8     'hcb
#     ...           ...           ...   ...
#     [12]          integral      8     'h52
#     [13]          integral      8     'h3a
#     [14]          integral      8     'he2
#     [15]          integral      8     'h1c
#     [16]          integral      8     'h67
#   parity          integral      8     'h37
#   packet_delay    integral      32    'd0
#   begin_time      time          64    860 ns
#   end_time        time          64    1240 ns
# ---------------------------------------------
```

YAPP Packet sent to Channel 2

```
#  UVM_INFO  yapp_tx_monitor.sv(59)  @  1320  ns:  uvm_test_top.tb.yapp.tx_agent.monitor
[yapp_tx_monitor] Packet Collected :
# ------------------------------------------------
# Name               Type          Size  Value
# ------------------------------------------------
# packet_collected   yapp_packet   -     @1403
#   length           integral      6     'h7
#   addr             integral      2     'h2
#   payload          da(integral)  7     -
#     [0]            integral      8     'h6c
#     [1]            integral      8     'h93
#     [2]            integral      8     'h8a
#     [3]            integral      8     'h33
#     [4]            integral      8     'h99
#     [5]            integral      8     'h2
#     [6]            integral      8     'h76
#   parity           integral      8     'hb5
#   packet_delay     integral      32    'd0
#   begin_time       time          64    1160 ns
#   end_time         time          64    1320 ns
# ------------------------------------------------


#   UVM_INFO   channel_monitor.sv(173)   @   1520   ns:   uvm_test_top.tb.chan2.monitor
[channel_monitor] Channel_2 Packet collected :
# ------------------------------------------------
# Name               Type          Size  Value
# ------------------------------------------------
# packet_collected   yapp_packet   -     @1420
#   length           integral      6     'h7
#   addr             integral      2     'h2
#   payload          da(integral)  7     -
#     [0]            integral      8     'h6c
#     [1]            integral      8     'h93
#     [2]            integral      8     'h8a
#     [3]            integral      8     'h33
#     [4]            integral      8     'h99
#     [5]            integral      8     'h2
#     [6]            integral      8     'h76
#   parity           integral      8     'hb5
#   packet_delay     integral      32    'd0
#   begin_time       time          64    1340 ns
#   end_time         time          64    1520 ns
# ------------------------------------------------
```

Erroneous Packet

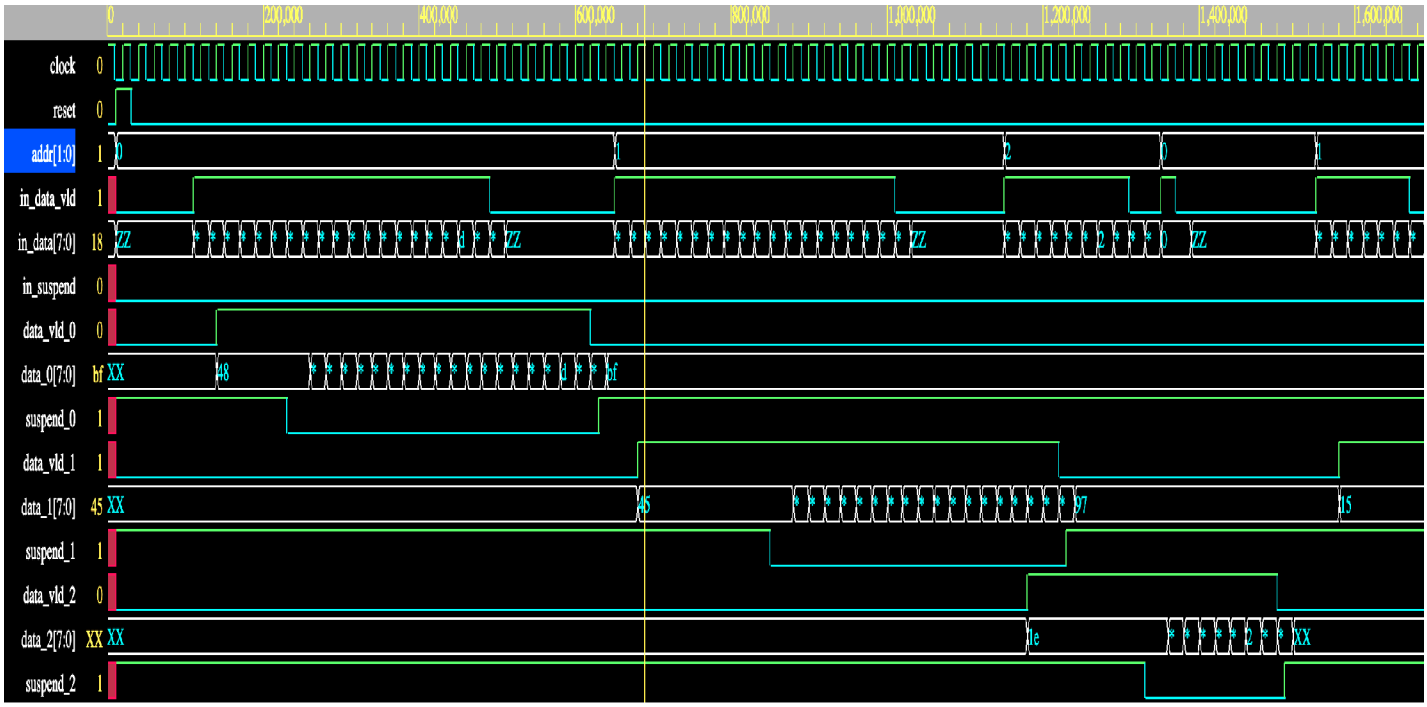
```
# UVM_INFO yapp_tx_seqs.sv(58) @ 1330 ns:
uvm_test_top.tb.yapp.tx_agent.sequencer@@yapp_012_seq.addr_1_seq [yapp_1_seq]
Executing yapp_1_seq sequence

# yapp_tx_seqs.sv(59): randomize() failed due to conflicts between the following
constraints:
#      yapp_packet.sv(37): default_addr { (addr != 3); }
#      yapp_tx_seqs.sv(59): (addr == 3);
# Where:
#      addr = 2'h3 /* random  */

# ** Note: (vsim-7130) Enabling enhanced debug (-solvefaildebug=2) may generate a more
descriptive constraint contradiction report.

# ROUTER DROPS PACKET - LENGTH is 0, MAX is 63
```

Final Results

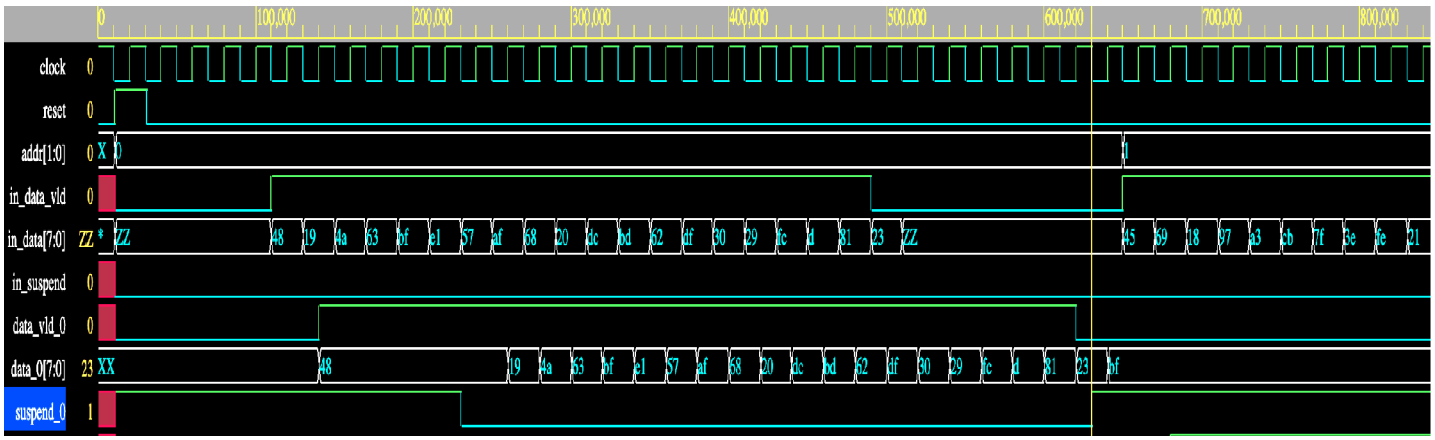
```
# UVM_INFO yapp_tx_seqs.sv(19) @ 1690 ns:
uvm_test_top.tb.yapp.tx_agent.sequencer@@yapp_012_seq [yapp_012_seq] drop objection

# UVM_INFO verilog_src/uvm-1.1d/src/base/uvm_objection.svh(1267) @ 1690 ns: reporter
[TEST_DONE] 'run' phase is ready to proceed to the 'extract' phase

# UVM_INFO channel_monitor.sv(208) @ 1690 ns: uvm_test_top.tb.chan0.monitor
[channel_monitor] Report: Channel_0 Monitor Collected 1 Packets and 1 Responses

# UVM_INFO channel_rx_driver.sv(116) @ 1690 ns: uvm_test_top.tb.chan0.rx_agent.driver
[channel_rx_driver] Report: Channel_0 RX Driver Sent 1 Responses

# UVM_INFO channel_monitor.sv(208) @ 1690 ns: uvm_test_top.tb.chan1.monitor
[channel_monitor] Report: Channel_1 Monitor Collected 1 Packets and 1 Responses

# UVM_INFO channel_rx_driver.sv(116) @ 1690 ns: uvm_test_top.tb.chan1.rx_agent.driver
[channel_rx_driver] Report: Channel_1 RX Driver Sent 1 Responses

# UVM_INFO channel_monitor.sv(208) @ 1690 ns: uvm_test_top.tb.chan2.monitor
[channel_monitor] Report: Channel_2 Monitor Collected 1 Packets and 1 Responses

# UVM_INFO channel_rx_driver.sv(116) @ 1690 ns: uvm_test_top.tb.chan2.rx_agent.driver
[channel_rx_driver] Report: Channel_2 RX Driver Sent 1 Responses

# UVM_INFO hbus_monitor.sv(136) @ 1690 ns: uvm_test_top.tb.hbus.monitor [hbus_monitor]
Report: HBUS Monitor Collected 0 WRITE and 0 READ Transactions

# UVM_INFO yapp_tx_driver.sv(93) @ 1690 ns: uvm_test_top.tb.yapp.tx_agent.driver
[yapp_tx_driver] Report: YAPP TX driver sent 5 packets

# UVM_INFO yapp_tx_monitor.sv(65) @ 1690 ns: uvm_test_top.tb.yapp.tx_agent.monitor
[yapp_tx_monitor] Report: YAPP Monitor Collected 5 Packets

#
# --- UVM Report Summary ---
#
# ** Report counts by severity
```

```
# UVM_INFO :    57
# UVM_WARNING :     1
# UVM_ERROR :     0
# UVM_FATAL :     0
```

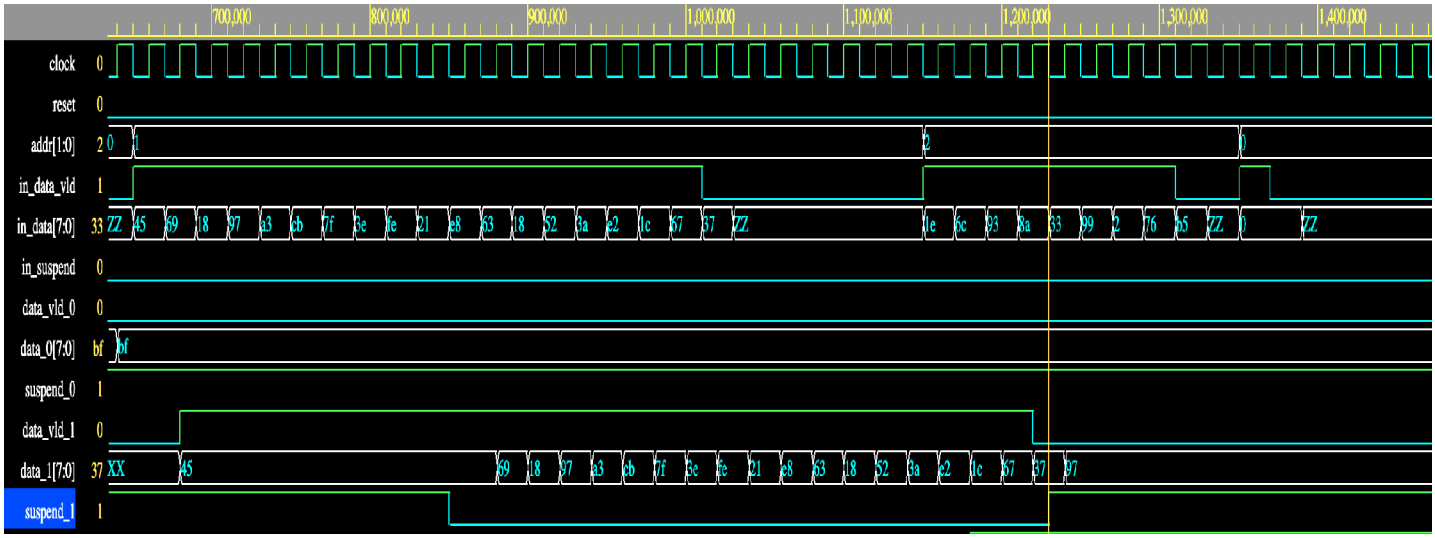
Waveforms:



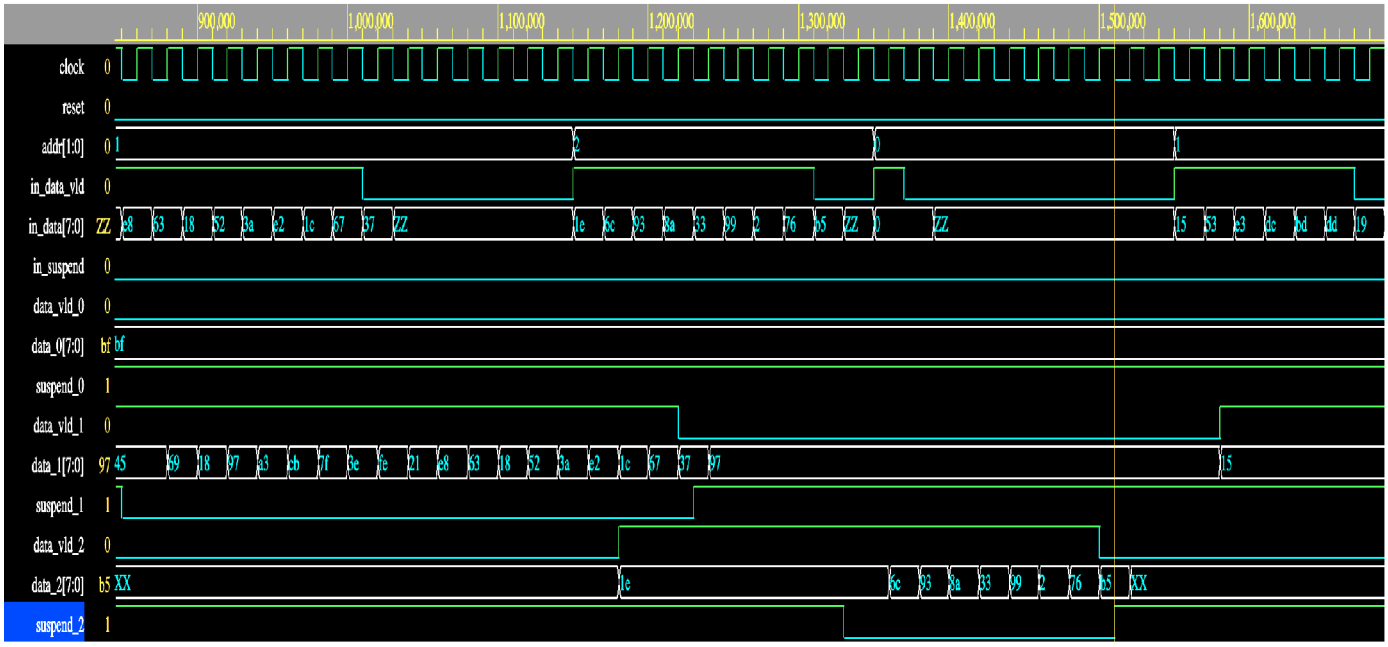
Channel 0



Channel 1



Channel 2



EDA playground link : https://www.edaplayground.com/x/5HBj