Advanced BCD Technology for Analog IC Design

1. Introduction to BCD Process
The BCD (Bipolar-CMOS-DMOS) process technology is a cornerstone of modern power management IC (PMIC) design. It integrates three distinct distinct device types onto a single die: **Bipolar** transistors for precise analog functions (bandgaps, sensors), **CMOS** for digital logic and control, and **DMOS** (Double-Diffused MOS) for high-voltage power switching. A key challenge in 180nm BCD generation is the trade-off between the Specific On-Resistance (R_on,sp) and the Breakdown Voltage (BV_dss). Designers must utilize Shallow Trench Isolation (STI) to minimize latch-up risks in high-noise environments.

2. Key Figure of Merit (FOM)

The efficiency of the LDMOS device is often evaluated using the Baliga Figure of Merit (BFOM), defined as:

$$BFOM = \frac{V_{BR}^2}{R_{on,sp}}$$

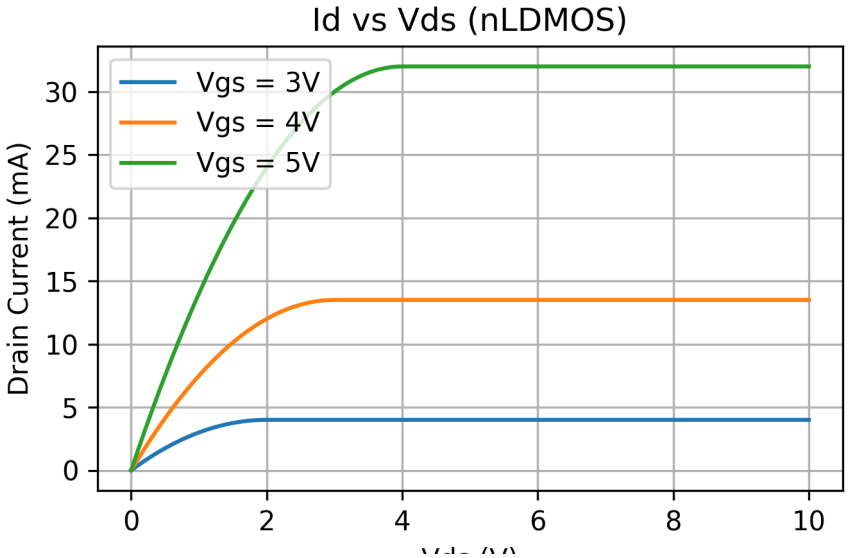
Where V_BR is the breakdown voltage and R_on,sp is the specific on-resistance.

3. Process Node Comparison

Parameter	0.35um BCD	0.18um BCD	0.11um BCD
Gate Oxide Thickness (A)	70 / 250	35 / 120	28 / 60
Max Logic Density (kGates/mm2)	15	85	220
Power Device (LDMOS) BV	12V - 60V	5V - 100V	5V - 80V
Mask Layers (Typical)	18	24	32

4. LDMOS Output Characteristics

The following chart illustrates the saturation behavior of the n-type LDMOS at different Gate voltages (Vgs).


Id vs Vds (nLDMOS)
Vgs = 3V
Vgs = 4V
Vgs = 5V
Drain Current (mA)
0
5
10
15
20
25
30
0
2
4
6
8
10