IPC-7351 Naming Convention for Standard SMT Land Patterns

Surface Mount Land Patterns

Component, Category

Land Pattern Name

Ball Grid Array's, Inch Based (1.27mm / 0.05" Pitch)	150P + Number of Pin Columns X Number of Pin Rows - Pin Qty 100P + Number of Pin Columns X Number of Pin Rows - Pin Qty 180P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1875P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1865P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1865P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1870P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1870P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1870P + Number of Pin Columns X Number of Pin Rows - Pin Qty 1870P + Body Size in Metric
Capacitors, Chip, Array, Flat (Pins on 2 sides)	CAPCAF + Body Size in Metric
Capacitors, Chip, Polarized	
Capacitors, Chip, Wire Rectangle	
Capacitors, Molded, Non-polarized	
Capacitors, Molded, Polarized	
Ceramic Flat Packages	
Column Grid Array's	CGA + Number of Pin Columns X Number of Pin Rows - Pin Oty
Diodes, Molded (JEDEC Standard Package)	
Diodes, MELF	
Inductors, Chip	
Inductors, Chip, Array, Concave (Pins on 2 or 4 sides)	
Inductors, Chip, Array, Convex, E-Version (Equal Pin Sizes)	
Inductors, Chip, Array, Convex, S-Version (End Pins Larger)	
Inductors, Chip, Array, Flat (Pins on 2 sides)	
Inductors, Molded	
Inductors, Precision Wire WoundPlastic Leaded Chip Carriers Square (JEDEC Standard Package)	
Plastic Leaded Chip Carriers Square (JEDEC Standard Package)	
Plastic Leaded Chip Carrier Sockets Square	PI CCS- Pin Oty
Plastic Leaded Chip Carrier Sockets Rectangular	
Plastic Quad Flat Packages, 0.635mm Pitch, Pin 1 Side	
Plastic Quad Flat Packages, 0.635mm Pitch, Pin 1 Center	
Bumper Quad Flat Packages, 0.635mm Pitch, Pin 1 Side	
Bumper Quad Flat Packages, 0.635mm Pitch, Pin 1 Center	BQFPC- Pin Qty
Quad Flat Packages, 1.00mm Pitch	
Quad Flat Packages, 0.80mm Pitch	QFP80P + Lead Span L1 X Lead Span L2 Nominal - Pin Qty
Quad Flat Packages, 0.65mm Pitch	
Shrink Quad Flat Packages, 0.50mm Pitch	
Shrink Quad Flat Packages, 0.40mm Pitch	
Thin Quad Flat Packages, 0.80mm Pitch, Height ≤ 1.60mm	
Thin Quad Flat Packages, 0.65mm Pitch, Height ≤ 1.60mm	
Thin Quad Flat Packages, 0.50mm Pitch, Height ≤ 1.60mm	
Thin Quad Flat Packages, 0.40mm Pitch, Height ≤ 1.60mm	
Thin Quad Flat Packages, 0.30mm Pitch, Height ≤ 1.60mm	
Ceramic Quad Flat Packages, 1.27mm Pitch	
Ceramic Quad Flat Packages, 0.80mm Pitch	
Ceramic Quad Flat Packages, 0.635mm Pitch	
Quad Flat No Lead Packages 0.80mm Pitch	
Quad Flat No Lead Packages 0.65mm Pitch	
Quad Flat No Lead Packages 0.50mm Pitch	+ Body Width X Body Length in Metric - Pin Qty + Thermal Pad
Quad Flat No Lead Packages 0.40mm Pitch	
Quad Leadless Ceramic Chip Carriers (JEDEC Standard Package Quad Leadless Ceramic Chip Carriers (Pin 1 on Side)	LCCS + Body Width X Body Length in Metric - Pin Qty

IPC-7351 Naming Convention for Standard SMT Land Patterns

Surface Mount Land Patterns (continued)

Component, Category

Land Pattern Name

Resistors, Chip	
Resistors, Chip, Array, Concave (Pins on 2 or 4 sides)	RESCAV + Body Size in Metric
Resistors, Chip, Array, Convex, E-Version (Equal Pin Sizes)	
Resistors, Chip, Array, Convex, S-Version (End Pins Larger)	
Resistors, Chip, Array, Flat (Pins on 2 sides)	
Resistors, Molded	RESM + Body Size in Metric
Resistor, MELF	RESMELF + Body Size in Metric
Small Outline IC, J-Leaded 300, 350, 400, 450 mil Body Width (Pitch 1.27mm)	SOJ127P + Lead Span Nominal - Pin Qty
Small Outline IC, J-Leaded (Pitch 0.65mm)	SOJ65P + Lead Span Nominal - Pin Qty
Small Outline Integrated Circuit, 1.27mm Pitch (Standard 50 mil Pitch SOIC)	
Small Outline Packages, 1.27mm Pitch (Non-Standard 50 mil Pitch SOIC)	
Small Outline Packages, 1.00mm Pitch	
Small Outline Packages, 0.80mm Pitch	
Small Outline Packages, 0.65mm Pitch	
Small Outline Packages, 0.635mm Pitch	
Shrink Small Outline Packages, 0.50mm Pitch	SSOP50P + Lead Span Nominal - Pin Qty
Shrink Small Outline Packages, 0.40mm Pitch	
Shrink Small Outline Packages, 0.30mm Pitch	
Thin Small Outline Packages, Height is ≤ 1.60mm, 1.27mm Pitch	
Thin Small Outline Packages, Height is ≤ 1.60mm, 1.00mm Pitch	
Thin Small Outline Packages, Height is ≤ 1.60mm, 0.80mm Pitch	
Thin Small Outline Packages, Height is ≤ 1.60mm, 0.65mm Pitch	TSOP65P + Lead Span Nominal - Pin Qty
Thin Shrink Small Outline Packages, Height is ≤ 1.60mm, 0.55mm Pitch	TSSOP55P + Lead Span Nominal - Pin Qty
Thin Shrink Small Outline Packages, Height is ≤ 1.60mm, 0.50mm Pitch	TSSOP50P + Lead Span Nominal - Pin Qty
Thin Shrink Small Outline Packages, Height is ≤ 1.60mm, 0.40mm Pitch	TSSOP40P + Lead Span Nominal - Pin Qty
Thin Shrink Small Outline Packages, Thin (Height is ≤ 1.60mm) 0.30mm Pitch	TSSOP30P + Lead Span Nominal - Pin Qty
Very Small Outline Packages, 0.762mm Pitch (0.30" Pitch)	
SOD (Example: SOD3705 = SOD123)	SOD + Lead Span Nominal + Body Width
SON - Dual No Lead Packages 0.3 - 0.8mm PitchSON + Pitch P + Bo	ody Width X Body Length - Pin Qty + Thermal Pad
SOT89 (JEDEC Standard Package)	SOT89
SOT143 (JEDEC Standard Package)	
SOT343 (JEDEC Standard Package)	
SOT143 Reverse (JEDEC Standard Package)	
SOT343 Reverse (JEDEC Standard Package)	
SOT223 (JEDEC Standard Package) (Example: SOT230P700-4N)	SOT + Pitch P + Lead Span Nominal - Pin Qty
SOT Generic Package 0.65mm Pitch	
SOT Generic Package 0.95mm Pitch	
TO (Generic DPAK - Example: TO228P970-3N)	TO + Pitch P + Lead Span - Pin Qty

IPC-7351 Naming Convention for Standard SMT Land Patterns

SYNTAX EXPLANATIONS:

The + (plus sign) stands for "in addition to" (no space between the prefix and the body size)

The _ (under score) is the separator between the Prefix and the Mfr Part Number.

The - (dash) is used to separate the pin qty.

The **X** (capital letter X) is used instead of the word "by" to separate two numbers such as height **X** width like "Quad Packages". Connector Series Number:

In these libraries such as AMP & MOLEX the "Series Number" is used and the pin qty. Molex Example: **90663-60** The other connector libraries will just contain the manufacturer's part number. We did a study and could not find any overlapping manufacture part numbers for 20 different connector manufacturers, so it's safe to use it.

SUFFIXES For Every Common SMT Land Pattern to Describe Environment Use (This is the last character in every name) Note: This excludes the BGA component family as they only come in the Nominal Environment Condition

- M Most Material Condition (Level A)
- N...... Nominal Material Condition (Level B)
- L.....Least Material Condition (Level C)

SUFFIXES for Alternate Components that do not follow the JEDEC, EIA or IEC Standard

- A................ Alternate Component (used primarily for SOP & QFP when Component Tolerance or Height is different)
- B..... Second Alternate Component

SUFFIXES for JEDEC and EIA Standard parts that have several alternate packages

AA, AB, AC. JEDEC or EIA Component Identifier (Used primarily on Chip Resistors, Inductors and Capacitors)

GENERAL SUFFIXES

_HS HS = Land Pattern with Heat Sink attachment requiring additional holes or pads
Example: TO254P1055_HS-6N

_BEC BEC = Base, Emitter and Collector (Pin assignments used for three pin Transistors)

_SGD SGD = Source, Gate and Drain (Pin assignments used for three pin Transistors)

Example: SOT95P280 BEC-3N

_213 213 = Alternate pin assignments used for three pin Transistors

IPC-7351 Surface Mount Land Patterns

IPC-735* Component Family Breakdown:

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IPC-7351 = IEC 61188-5-1, Generic requirements - Attachment (land/joint) considerations - General Description
IPC-7352 = IEC 61188-5-2, Sectional requirements - Attachment (land/joint) considerations - Discrete Components
IPC-7353 = IEC 61188-5-3, Sectional requirements - Attachment (land/joint) considerations - Gull-wing leads, two sides (SOP)
IPC-7354 = IEC 61188-5-4, Sectional requirements - Attachment (land/joint) considerations - J leads, two sides (SOJ)
IPC-7355 = IEC 61188-5-5, Sectional requirements - Attachment (land/joint) considerations - Gull-wing leads, four sides (QFP)
IPC-7356 = IEC 61188-5-6, Sectional requirements - Attachment (land/joint) considerations - J leads, four sides (PLCC)
IPC-7357 = IEC 61188-5-7, Sectional requirements - Attachment (land/joint) considerations - Post leads, two sides (DIP)
IPC-7358 = IEC 61188-5-8, Sectional requirements - Attachment (land/joint) considerations - Area Array Components (BGA)
IPC-7359 = NO IEC Document, Sectional requirements - Attachment (land/joint) considerations - No Lead Components (LCC)
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Component Zero Orientations Pin 1 Location for CAD Library Construction:

- 1) Chip Capacitors, Resistors and Inductors (RES, CAP and IND) Pin 1 (Positive) on Left
- 2) Molded Inductors (INDM), Resistors (RESM), Tantalum Capacitors (CAPT) Pin 1 (Positive) on Left
- 3) Precision Wire-wound Inductors Pin 1 (Positive) on Left
- 4) MELF Diode Pin 1 (Cathode) on Left
- 5) SOD Diodes Pin 1 (Cathode) on Left
- 6) Aluminum Electrolytic Capacitors Pin 1 (Positive) on Left
- 7) SOT Devices (SOT23, SOT23-5, SOT223, SOT89, SOT143, etc.) Pin 1 Upper Left
- 8) TO252 & TO263 (DPAK Type) Devices Pin 1 Upper Left
- 9) Small Outline Gullwing ICs (SOIC, SOP, TSOP, SSOP, TSSOP) Pin 1 Upper Left
- 10) Ceramic Flat Packs (CFP) Pin 1 Upper Left
- 11) Small Outline J Lead ICs (SOJ) Pin 1 Upper Left
- 12) Quad Flat Pack ICs (PQFP, SQFP) Pin 1 Upper Left
- 13) Ceramic Quad Flat Packs (CQFP) Pin 1 Upper Left
- 14) Bumper Quad Flat Pack ICs (BQFP Pin 1 Center) Pin 1 Top Center
- 15) Plastic Leaded Chip Carriers (PLCC) Pin 1 Top Center
- 16) Leadless Chip Carriers (LCC) Pin 1 Top Center
- 17) Quad Flat No-Lead ICs (QFN) QFNS & QFNRV, QFNRH Pin 1 Upper Left
- 18) Ball Grid Arrays (BGA) Pin A1 Upper Left