Problem 3: Y86 (17 points)

- 1. [1] 30f4000200000000000 [2] 6300
 - [3] rrmovq %rdi, %rdx [4] mrmovq (%rdx), %rdx
 - [5] 6222 [6] .pos 0x300
 - [7] 0x310
- 2. % rax = 0x2

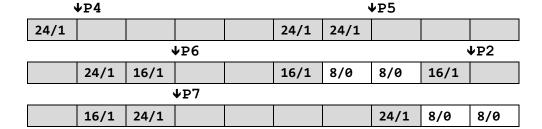
Problem 4: Memory Allocation (16 points)

1. (Whether marking out pointers or not are both correct)

₩ ₽5				V P /					
24/1					24/1	24/1			
↓ P4									∳ P2
	24/1	24/1					24/1	16/1	
↓ P6									
	16/1	16/1			16/1	16/0			16/0

2. (Whether marking out pointers or not are both correct)

```
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```

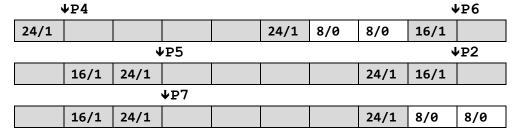


3. Consider the following operation sequence:

```
p = malloc(5);
free(p);
p = malloc(5);
free(p);
p = malloc(5);
```

Assume the allocated block of p is adjacent to another free block. In such situation, every time we free pointer p will cause a coalescing operation, which will dramatically influence the performance.

4. (Whether marking out pointers or not are both correct)



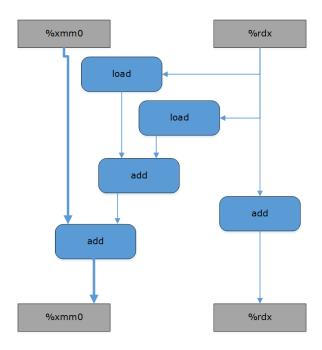
Problem 5: Optimization (16 points)

1

```
1.
    void copy_array(array_t *new, array_t *old) {
2.
      // Eliminating loop inefficiency
      long len = get length(old);
3.
      // reduce function calls
4.
5.
      long cap = get_capacity(new);
      // remove unneeded memory references
6.
7.
      float *old data = old->data;
      float *new data = new->data;
8.
      long niters = (len < cap) ? len : cap;</pre>
9.
10.
      // loop unrolling and enhancing parallelism
      for (long i = 0; i + 1 < niters; i += 2) {
11.
12.
       new_data[i] = old_data[i];
13.
       new data[i + 1] = old data[i + 1];
14.
      }
15.
      if (i < niters)
```

```
16.     new_data[i] = old_data[i];
17.     new->length = niters;
18. }
```

2.



3.

We have two **load** and two **add** operations. **After the modification**, both **add** operations form a dependency chain between loop registers. While **before the modification**, only one of the **add** operations forms a data-dependency chain between loop registers. The first addition within each iteration can be performed without waiting for the accumulated value from the previous iteration. Thus, we reduce the minimum possible CPE by a factor of around 2.

Problem 6 : Processor (35 points)

```
1. Load/use hazard: 6
   misprediction of jle: 6
  misprediction of jg: 2
2. Loop: mrmovq
                  (%rdi), %r10
         rmmovq
                   %r10, (%rsi)
                   %r10, %r10
         andq
         ckillle
         iaddq
                   $1, %rax
         iaddq
                   $8, %rdi
         iaddq
                   $8, %rsi
                   $-1, %rdx
         iaddq
                   Loop
         jg
   Load/use hazard: 6
   misprediction of ckillle: 3
   misprediction of jg: 2
```

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- 3. [1] E_icode == ICKILLXX && e_Cnd
 - [2] normal [3] normal [4] bubble
- 4. solution1: [1] normal [2] normal [3] bubble [4] normal
 - solution2: [1] stall [2] bubble [3] bubble [4] normal
- 5. No. Because the third instruction is not loaded when ckill3xx is in E stage/Because you can't insert bubble in F

Solution 1:

Delay the handle to M stage, so we could insert 3 bubbles at once. Be careful with CC!!

```
D_bubble = ... || (M_icode == ICKILL3XX && M_Cnd)
E_bubble = ... || (M_icode == ICKILL3XX && M_Cnd)
```

set_cc = ... && !(M_icode == ICKILL3XX && M_Cnd)

Solution 2:

Insert 2 bubbles when detected in E, and insert one more in M.

6. Pros:

Instruction is shorter No label is needed

Cons:

One more bubble