Clock Generator

+5V X1
SG-531
OSCILLATOR
8 Vcc
OE OUT 5 — clk
4 GND
GNDREF

Reset Circuit

+5V
R3 10k
U11 MC34064P
R6 10k
TP3 HLT/RST
n6
2 IN RESET 1
3 GND
C23 0.1u
hlt_rst
SW1 RESET
GNDREF

GNDREF
0.1u C29   C30 0.1u C10
1u C9   1u
+5V

clk 15 CLK
hlt_rst 19 HALT
20 RESET

14 VCC   52 VCC

{as,uds,lds,rw,dtack,berr}
as 6 AS
uds 7 UDS
lds 8 LDS
rw 9 R/W
dtack 10 DTACK
berr 24 BERR

{ipl0,ipl1,ipl2,fc0,fc1,fc2}
ipl0 27 IPL0
ipl1 26 IPL1
ipl2 25 IPL2
fc0 30 FC0
fc1 29 FC1
fc2 28 FC2

U1
MC68000FN
MICROPROCESSOR

A1 32 addr0
A2 33 addr1
A3 34 addr2
A4 35 addr3
A5 36 addr4
A6 37 addr5
A7 38 addr6
A8 39 addr7
A9 40 addr8
A10 41 addr9
A11 42 addr10
A12 43 addr11
A13 44 addr12
A14 45 addr13
A15 46 addr14
A16 47 addr15
A17 48 addr16
A18 49 addr17
A19 50 addr18
A20 51 addr19
A21 53 addr20
A22 54 addr21
A23 55 addr22

addr[0..22]

data[0..15]
D0 5 data0
D1 4 data1
D2 3 data2
D3 2 data3
D4 1 data4
D5 68 data5
D6 67 data6
D7 66 data7
D8 65 data8
D9 64 data9
D10 63 data10
D11 62 data11
D12 61 data12
D13 60 data13
D14 59 data14
D15 58 data15

21 VMA
22 E
n0 23 VPA
11 BG
R1 10k
12 BGACK
+5V 13 BR

GND 57 GND 56 GND 16 GND 17
GNDREF

XC9572XL — ADDRESS ROUTER

GNDREF
0.1u C27 1u C28 0.1u C20 1u C21 0.1u C11 1u C12
+3.3V

Vcc-INT-3.3V 21   Vcc-INT-3.3V 41   Vcc-io-3.3V 32

{ipl0,ipl1,ipl2,fc0,fc1,fc2}
ipl0 1 P1   P24 24 addr15
ipl1 2 P2   P25 25 addr16
ipl2 3 P3   P26 26 addr17
fc0 4 P4   P27 27 addr18
clk 5 P5/GCK1   P28 28 addr19
fc1 6 P6/GCK2   P29 29 addr20
fc2 7 P7/GCK3   P33 33 addr21
as 8 P8   P34 34 addr22
uds 9 P9   P35 35
lds 11 P11   P36 36
rw 12 P12   P37 37
dtack 13 P13   P38 38
berr 14 P14   P39/GSR 39 hlt_rst
duart_cs 18 P18 P40/GTS2 40
duart_iack 19 P19 P42/GTS1 42
duart_dtack 20 P20 P43 43
duart_irq 22 P22 P44 44

U3
XC9572XL
ADDRESS ROUTER

addr[0..22]

{as,uds,lds,rw,dtack,berr}

GND 10 GND 23 GND 31
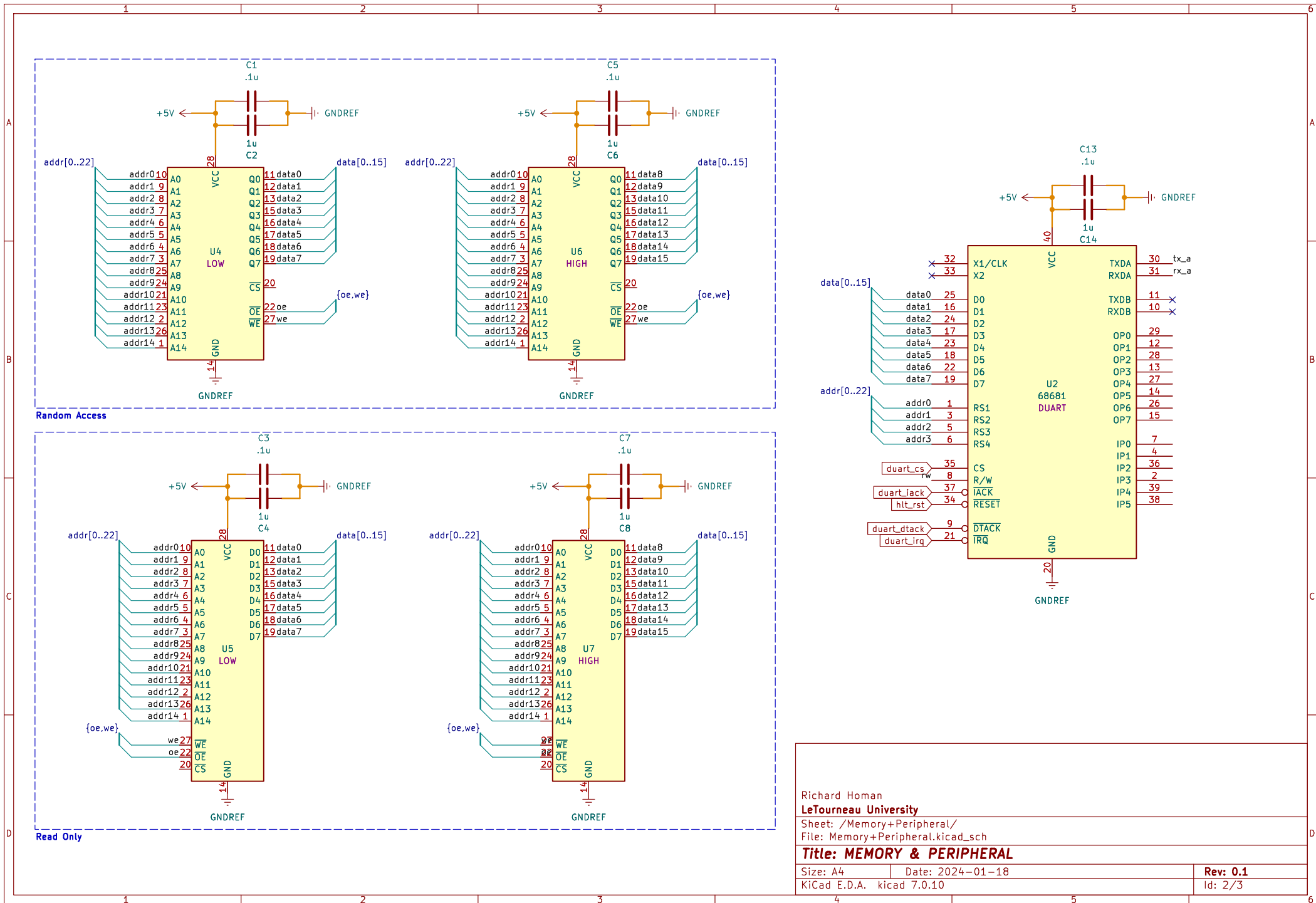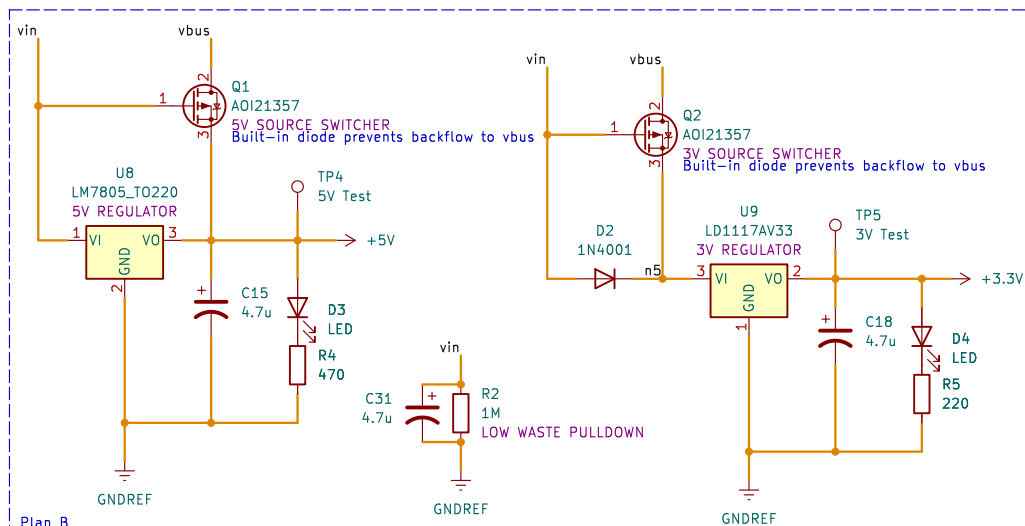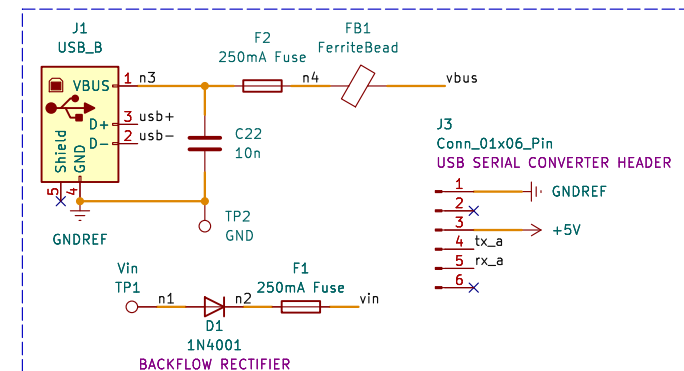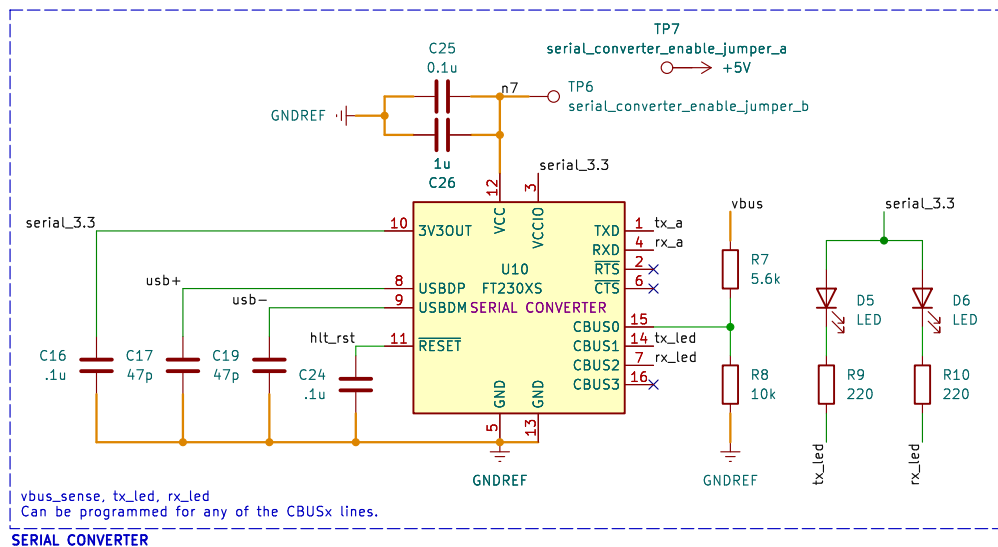TDI 15 TMS 16 TCK 17 TDO 30
tdi tms tck tdo
GNDREF

GCK=Global clock
GTS=Global output enable
GSR=Global set/reset CPLD control signals

GTS 1 and 2 do the same thing

Random Access

C1 .1u
+5V GNDREF
1u C2

addr[0..22]

U4 LOW
data[0..15]

addr0 10	A0	Q0 11 data0
addr1 9	A1	Q1 12 data1
addr2 8	A2	Q2 13 data2
addr3 7	A3	Q3 15 data3
addr4 6	A4	Q4 16 data4
addr5 5	A5	Q5 17 data5
addr6 4	A6	Q6 18 data6
addr7 3	A7	Q7 19 data7
addr8 25	A8	
addr9 24	A9	CS 20
addr10 21	A10	
addr11 23	A11	OE 22 oe
addr12 2	A12	WE 27 we
addr13 26	A13	
addr14 1	A14	

VCC 28
GND 14
{oe,we}
GNDREF

C5 .1u
+5V GNDREF
1u C6

addr[0..22]

U6 HIGH
data[0..15]

addr0 10	A0	Q0 11 data8
addr1 9	A1	Q1 12 data9
addr2 8	A2	Q2 13 data10
addr3 7	A3	Q3 15 data11
addr4 6	A4	Q4 16 data12
addr5 5	A5	Q5 17 data13
addr6 4	A6	Q6 18 data14
addr7 3	A7	Q7 19 data15
addr8 25	A8	
addr9 24	A9	CS 20
addr10 21	A10	
addr11 23	A11	OE 22 oe
addr12 2	A12	WE 27 we
addr13 26	A13	
addr14 1	A14	

VCC 28
GND 14
{oe,we}
GNDREF

Read Only

C3 .1u
+5V GNDREF
1u C4

addr[0..22]

U5 LOW
data[0..15]

addr0 10	A0	D0 11 data0
addr1 9	A1	D1 12 data1
addr2 8	A2	D2 13 data2
addr3 7	A3	D3 15 data3
addr4 6	A4	D4 16 data4
addr5 5	A5	D5 17 data5
addr6 4	A6	D6 18 data6
addr7 3	A7	D7 19 data7
addr8 25	A8	
addr9 24	A9	
addr10 21	A10	
addr11 23	A11	
addr12 2	A12	
addr13 26	A13	
addr14 1	A14	

VCC 28
{oe,we}
we 27 WE
oe 22 OE
20 CS
GND 14
GNDREF

C7 .1u
+5V GNDREF
1u C8

addr[0..22]

U7 HIGH
data[0..15]

addr0 10	A0	D0 11 data8
addr1 9	A1	D1 12 data9
addr2 8	A2	D2 13 data10
addr3 7	A3	D3 15 data11
addr4 6	A4	D4 16 data12
addr5 5	A5	D5 17 data13
addr6 4	A6	D6 18 data14
addr7 3	A7	D7 19 data15
addr8 25	A8	
addr9 24	A9	
addr10 21	A10	
addr11 23	A11	
addr12 2	A12	
addr13 26	A13	
addr14 1	A14	

VCC 28
{oe,we}
we 27 WE
oe 22 OE
20 CS
GND 14
GNDREF

C13 .1u
+5V GNDREF
1u C14

U2 68681 DUART

32 X1/CLK		TXDA 30 tx_a
33 X2		RXDA 31 rx_a
data0 25 D0		TXDB 11
data1 16 D1		RXDB 10
data2 24 D2		
data3 17 D3		OP0 29
data4 23 D4		OP1 12
data5 18 D5		OP2 28
data6 22 D6		OP3 13
data7 19 D7		OP4 27
addr0 1 RS1		OP5 14
addr1 3 RS2		OP6 26
addr2 5 RS3		OP7 15
addr3 6 RS4		
duart_cs 35 CS		IP0 7
r/w 8 R/W		IP1 4
duart_iack 37 IACK		IP2 36
hlt_rst 34 RESET		IP3 2
duart_dtack 9 DTACK		IP4 39
duart_irq 21 IRQ		IP5 38

VCC 40
GND 20
GNDREF

data[0..15]
addr[0..22]

Richard Homan
LeTourneau University
Sheet: /Memory+Peripheral/
File: Memory+Peripheral.kicad_sch
Title: MEMORY & PERIPHERAL
Size: A4 Date: 2024-01-18 **Rev: 0.1**
KiCad E.D.A. kicad 7.0.10 Id: 2/3

SERIAL CONVERTER

C25
0.1u

TP7
serial_converter_enable_jumper_a → +5V

GNDREF

n7
TP6
serial_converter_enable_jumper_b

1u
C26

serial_3.3

C12 C3

U10
FT230XS
SERIAL CONVERTER

VCC VCCIO

10 3V3OUT
serial_3.3

TXD 1 tx_a
RXD 4 rx_a
RTS 2
CTS 6

8 USBDP
usb+
9 USBDM
usb−

hlt_rst
11 RESET

CBUS0 15
CBUS1 14 tx_led
CBUS2 7   rx_led
CBUS3 16

GND GND
5   13

vbus
R7
5.6k

R8
10k

GNDREF

serial_3.3

D5 LED
D6 LED

R9 220
R10 220

C16 C17 C19
.1u 47p 47p

C24
.1u

GNDREF

tx_led rx_led

vbus_sense, tx_led, rx_led
Can be programmed for any of the CBUSx lines.

External Interface

J1
USB_B

VBUS 1 n3
D+ 3 usb+
D− 2 usb−
Shield GND
5 4

GNDREF

F2
250mA Fuse
n4

FB1
FerriteBead

vbus

C22
10n

TP2
GND

J3
Conn_01x06_Pin
USB SERIAL CONVERTER HEADER

1 GNDREF
2
3 +5V
4 tx_a
5 rx_a
6

Vin
TP1
n1

D1
1N4001
BACKFLOW RECTIFIER

n2

F1
250mA Fuse

vin

Power Source & Switching Circuits

vin vbus

Q1
AOI21357
5V SOURCE SWITCHER
Built−in diode prevents backflow to vbus

U8
LM7805_TO220
5V REGULATOR

VI VO
1   3
GND
2

TP4
5V Test

+5V

C15
4.7u

D3
LED

R4
470

GNDREF

vin

C31
4.7u

R2
1M
LOW WASTE PULLDOWN

GNDREF

vin vbus

Q2
AOI21357
3V SOURCE SWITCHER
Built−in diode prevents backflow to vbus

D2
1N4001

n5

U9
LD1117AV33
3V REGULATOR

VI VO
3   2
GND
1

TP5
3V Test

+3.3V

C18
4.7u

D4
LED

R5
220

GNDREF

Plan B
If power switching does not work, can still power system with vbus only. Remove
Vin fuse and MOSFETS, then jump Source and Drain on each MOSFET footprint. For
self−powered configuration, remove MOSFETS only.