

Design and Layout of Two Level Shifting Printed Circuit Boards

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Abstract – This report describes the progress made during the Fall 2022 semester in Dr. Snider's research group and focuses specifically on my contributions. The projects described consist of two distinct printed circuit boards (PCBs) designed to interface a Virtex-7 VC707 Field Programmable Gate Array with a mother board or probe card for chip testing.

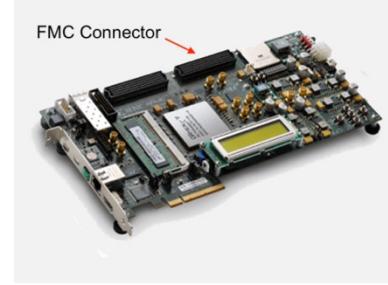


Figure 1. Virtex-7 VC707

I. INTRODUCTION

This semester I had the opportunity to continue working with Dr. Snider's research group and contribute to their efforts. My contributions consisted of designing and laying out two circuits required for analyzing several test chips and a full microprocessor without interlocked pipelined stages (MIPS). In the following sections, I will discuss the processes for these contributions and the results obtained.

II. Bidirectional Level Shifting Circuit for Implementation with Mother Board

A. Background

This project was required to interface the Virtex-7 VC707 FPGA with an adiabatic MIPS housed within a motherboard for testing. The 88-pin MIPS requires polar voltage levels of +/-0.7v while the input/output (I/O) pins located within the high-density FPGA Mezzanine Card (FMC) connector, shown in figure 1, require voltage levels of 0v to 1.8v. Therefore, a level shifting stage shown in the block diagram of figure 2 is required for effective testing of the adiabatic MIPS.

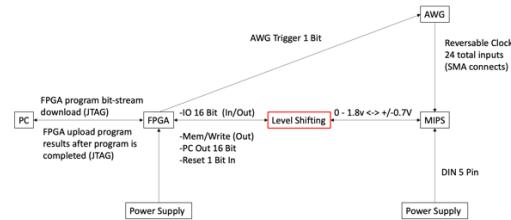


Figure 2. Block Diagram of Microprocessor Testing

During testing, the MIPS will be powered by an external power supply and receive clock signals from two external arbitrary waveform generators (AWGs). Additional documentation on the generation of these clock signals by the two AWGs can be found in *Arbitrary Waveform Generator Python Programming and Peltier Module Test Environment*, my final report from the Fall 2021 semester.

The Virtex-7 FPGA provides numerous functionalities for the MIPS. Most notably, the FPGA will send the instructions to the MIPS, wait for execution, and then save the output for observation. The FPGA interfaces with a PC via the FPGA's joint test action group (JTAG) port, shown in figure 3, using a universal serial bus (USB) cable. This interface allows for programming and observing the outputs of the microprocessor during testing.

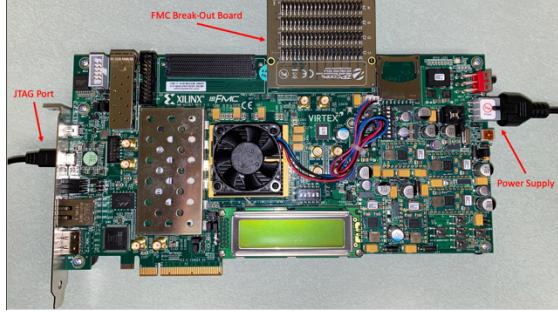


Figure 3. Labeled FPGA Connections

B. Circuit Design

Dr. Orlov designed the bidirectional level shifting circuitry used in this project during the Spring semester of 2022. The circuit, shown in figure 4, utilizes two comparators, one for shifting voltages down and one for shifting voltages up. The direction of voltage shift is determined by a discrete metal-oxide semiconductor field effect transistor (MOSFET) shown in figure 4 as CPH3355.

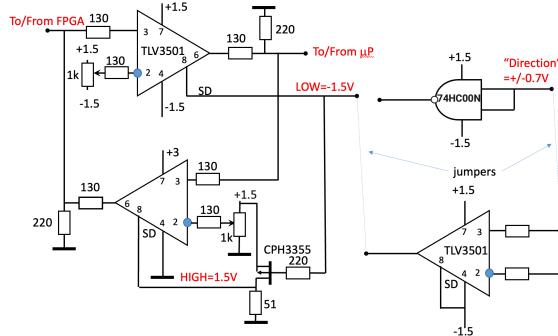


Figure 4. Bidirectional Level Shifting Circuit

C. Previous Circuit Boards

Previously, through collaboration with Indiana Integrated Circuits (IIC), a board layout was generated to test the functionality of this bidirectional level shifting circuit using only one channel. This board, shown in figure 5, demonstrated the viability of Dr. Orlov's circuit design and supported efforts toward the design of a multi-channel board.



Figure 5. Single Channel Bidirectional Level Shifting Board

D. Circuit Design using EDA Tools

While a previous one-bit board had been generated, the files for this board were not available. Needing to generate a schematic from scratch, libraries and part files were compiled for the components shown in figure 4 from distributors such as Digikey and Mouser. It was chosen to use Design Spark for layout as it was the EDA tool the group felt most experienced with.

A single channel schematic, shown in figure 6, was generated in accordance with Dr. Orlov's circuit design. From this schematic, the layout shown in figure 7 was created.

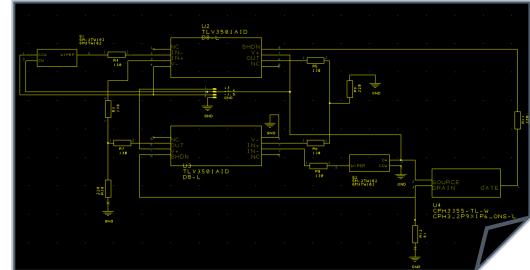


Figure 6. Single Channel Schematic

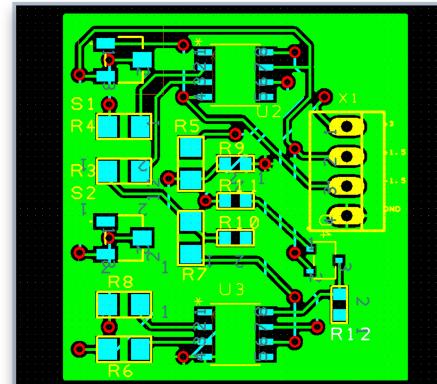


Figure 7. Single Channel Layout

Originally, it was thought this schematic and layout could serve as building blocks and could be easily repeated for the multi-channel design. However, it was later discovered hierarchical design, necessary for effective repetition of circuits, required a license for Design Spark Pro. An attempt was made to repeat the circuit manually but was soon determined too difficult to manage. This attempt is shown in figure 8.

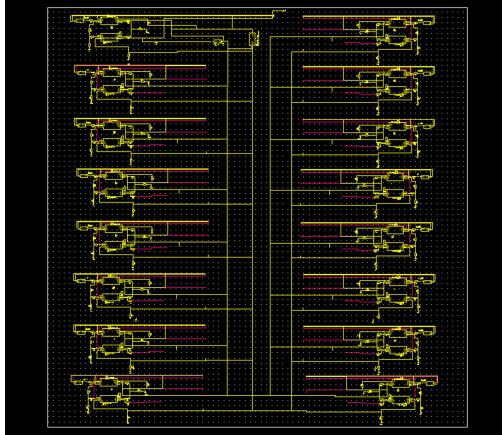


Figure 8. Multi-Channel Schematic – First Attempt

With Design Spark no longer a viable option, Autodesk Eagle was chosen to continue the project. After recreating the single channel schematic to be compatible with Eagle, a multi-channel schematic was created. This schematic, shown in figure 9, utilized Eagle's Hierarchical design to generate repetitive level shifting modules. The schematic utilized 16 level shifting modules, 1 power module, 2 ribbon cable connectors, and a discrete MOSFET. The level shifting module schematic is shown in figure 10.

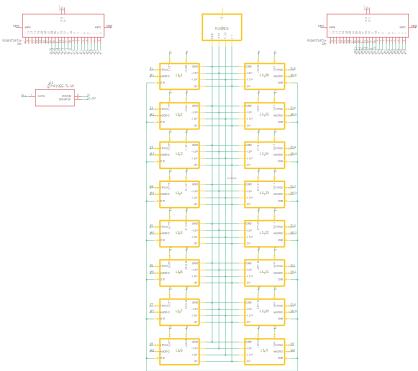


Figure 9. Multi-Channel Schematic using Eagle's Hierarchical Design

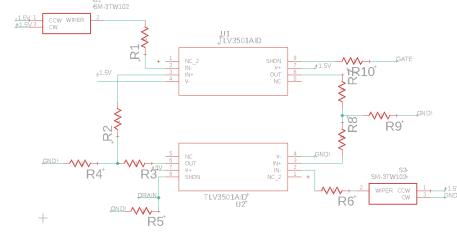


Figure 10. Level Shifting Module Schematic

After this progress was made, an additional project, described below, required efforts to be shifted away from this design.

III. FMC to Card Edge Connector Board with Integrated Level Shifting

A. Background

In addition to the MIPS, the group designed several other chips requiring testing. An 88-pin probe card was chosen to breakout the chip signals for testing. The probe card selected utilized an 88-pin card edge connector for I/O. To interface this card edge connector with the FPGA FMC connector, a conversion board was required.

B. Design of Board

As shown in figure 11, the board was designed to receive signals from the Virtex-7 VC707 FPGA via an FMC cable. Additional level shifting was required to lower the FPGAs 1.8V high signal to 1.2V for the test chips. Simple voltage dividers were chosen for this purpose.

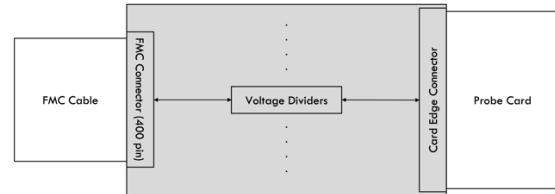


Figure 11. FMC to Card Edge Connector Board Design

C. Design using Eagle

An eagle library was available from the distributor for the FMC Connector; however, no such library was available for the card edge connector. Due to this, the component footprint and symbol were generated manually. After, the board schematic was created in accordance with the design shown in figure 11. This schematic is shown in figure 12.

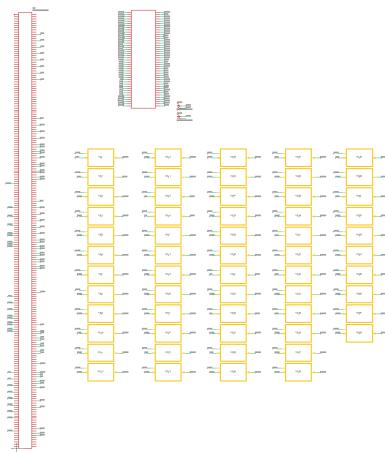


Figure 12. FMC to Card Edge Connector Schematic

As shown in figure 12, the schematic uses 58 voltage divider modules for integrated level shifting. The schematic view for these modules is shown in figure 13.

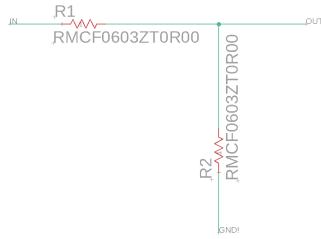


Figure 13. Voltage Divider Module Schematic

The layout shown in figure 14 was generated from the schematic in figure 12. The layout utilizes a two-layer board with top and bottom ground pours. Eagle's autorouter tool was used to route the 143 required signals on the board.

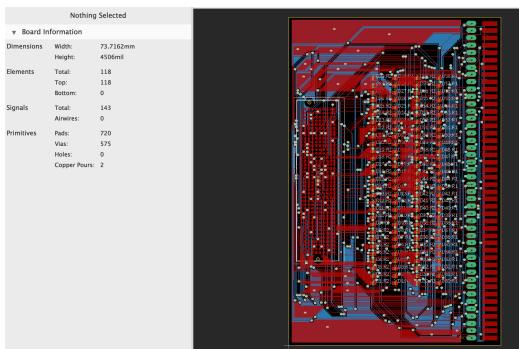


Figure 14. FMC to Card Edge Connector Layout

It was later determined a revised design of the board would make the mechanical setup for interfacing the FPGA to probe card simpler. This revised design,

shown in figure 15, reoriented the FMC connector to be positioned at a right angle. Additionally, ground and power subminiature version A (SMA) connectors were added to provide flexibility.

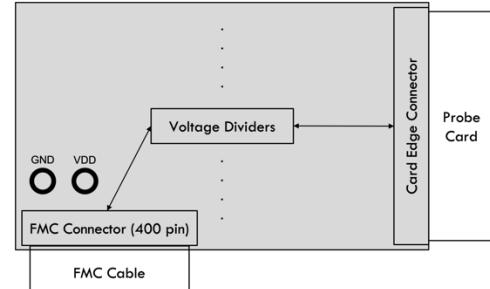


Figure 15. Revised FMC to Card Edge Connector Board Design

A layout, shown in figure 16, was created in accordance with this revised design.

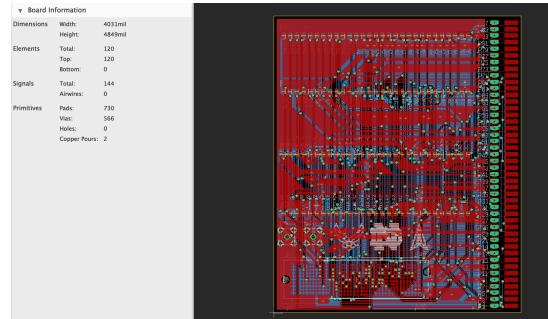


Figure 16. Revised FMC to Card Edge Connector Layout

D. Fabrication

After finalization of the FMC to Card Edge Connector Layout, fabrication was sourced from third party companies. OSH Park was utilized for PCB fabrication and OSH Stencils for solder paste stencil fabrication. Renders of the fabricated board are shown in figures 17 and 18. A render of the fabricated stencil is shown in figure 19.

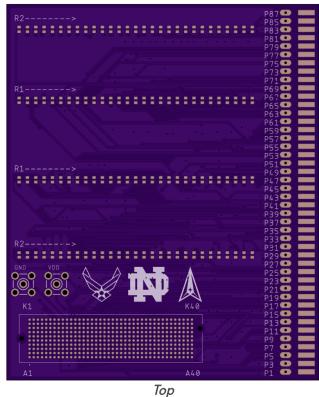


Figure 17. Render of Fabricated FMC to Card Edge Connector Board - Top



Figure 18. Render of Fabricated FMC to Card Edge Connector Board – Bottom

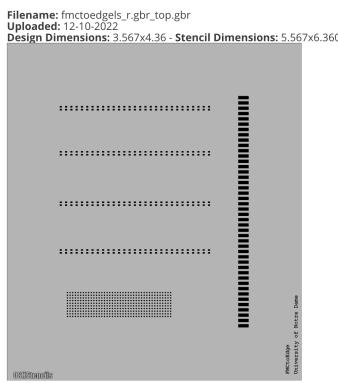


Figure 19. Render of Fabricated FMC to Card Edge Connector Stencil

III. Next Steps

Upon receiving the fabricated boards and stencil, the resistors and FMC connector will require soldering

using a reflow oven. The SMA connectors and card edge connector will need to be soldered by hand. With this complete, the board will be fully assembled and ready for implementation during testing.

REFERENCES

<https://oshpark.com>

<https://www.oshstencils.com/#>