RICHI DUBEY

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www.rtemswithrichi.wordpress.com (Technical Blog)

EDUCATION

Birla Institute of Technology & Science, Pilani (BITS Pilani) Goa, India
B.E., Computer Science | Overall GPA: **8.84**/10 (in only CS Courses: **9.3**/10) *Aug 2017 - June 2021*

- *Thesis*: Next-Generation Embedded Development Tools and Technologies – Virtualisation and Automation [Link]
- *Key Courses*: Operating Systems (A-Grade), Computer Networks (A-Grade), Data Structures and Algorithms, Real-Time Systems (in top 5/30, graduate-level course), Computer Programming (in top 7/850)

AWARDS

Merit-Need Scholarship — BITS Pilani *2017 - 2021*
40% - 80% fee waiver for consistent & exemplary performance (top **10%** of class by the last semester)

HERCULES Prize - edition 2019/2020 — University of Modena and Reggio Emilia, Italy *February 2021*
Awarded €4500 to work with Prof. Marko Bertogna on High-Perf. Architecture for Low-Power Embedded Systems

Google Summer of Code (GSoC) 2020 — Google *May 2020*
Awarded $4000 to implement Strong APA Scheduler on RTEMS. Details here

McGill Summer Undergraduate Research in Engineering (SURE) — McGill University (Cancelled due to COVID)
Awarded $5,625 to work with Prof. Liboiron-Ladouceur on Photonic Hardware for AI in summer 2020.

PUBLICATIONS

R. Dubey, V. Banerjee, S. Hounsinou, G. Bloom, *Strong APA scheduling in a real-time operating system: work-in-progress*, International Conference on Embedded Software (EMSOFT), 2021. [DOI], [Talk], [Poster]

WORK EXPERIENCE

Fellow - CERN *October 2022 – Present*
Health Safety and Environment (HSE) Department *Geneva, Switzerland*

- Part of 3-member team responsible for the management of a distributed and redundant SCADA system called REMUS that manages **1000+** diverse sensors deployed in accelerator, experimental, and surface areas at CERN.
- Developed novel communication protocols for real-time communication with 300+ radioactive and environmental sensors. Implemented the protocols using Linux and Windows sockets.
- Developed multi-threaded device drivers in C++ for REMUS and state-aware fault-tolerant networking programs for devices with outdated OSes, thus enabling robust networking capabilities

Member Technical Staff - Oracle *July 2021 – September 2022*
Oracle Cloud Infrastructure | *Oracle Process Cloud Team* *Bangalore, India*

- Implemented new features and fixed production bugs in a multi-tenant cloud application, Oracle Process Automation, with microservice architecture on Oracle Cloud.
- Wrote terraform code to create and manage the deployment of infrastructure required for the application on the cloud. Deployed these codes in a part of 5 member team across **50+** OCI data centers worldwide.
- Worked with a diverse tech stack, including Java, Spring, Spring Boot, SQL, Terraform, Docker, and Kubernetes.

Research Intern - High-Performance Real-Time (HiPeRT) Lab *Jan 2021 – April 2021*
Bachelor's Thesis at the University of Modena and Reggio Emilia, Modena, Italy *Remote*

- Implemented a system for remote benchmarking of workloads in embedded systems by integrating the Workload Automation (WA) tool by ARM with the Jailhouse partitioning hypervisor on a custom Linux kernel.

- Wrote jailhouse recipes for deploying custom kernels with Cache Coloring, which enhanced workload execution predictability and mitigated contention in the shared memory hierarchy. Using Cache Coloring is proven to provide a maximum speedup up to **77.4%** in certain cases.
- Wrote a bachelor thesis on the implementation, supervised by Prof. Marko Bertogna.

Student Developer - RTEMS Real-Time Operating System *May 2020 – August 2020*

Google Summer of Code | *More details here* *Remote*

- Contributed to RTEMS, a POSIX compliant real-time operating system extensively utilized in various domains, including NASA/ESA satellites, sports bikes, and particle accelerators across CERN and US DoE national labs.
- Implemented the Strong Arbitrary Processor Affinity (APA) scheduler, a state-of-the-art scheduler that has not been implemented in a real-world operating system.
- The Strong APA scheduler introduced the ability to dynamically relocate higher-priority tasks among processors, optimizing resource allocation by accommodating lower-priority tasks constrained by affinity requirements. The scheduler is proven to schedule roughly **20%** more task sets than other schedulers for certain utilization.

Undergraduate Research Projects

Approaches towards Censorship Circumvention BITS Pilani

Worked with Prof. Vinayak Naik, head of CS Department *September 2020 – November 2020*

- Conducted a comprehensive review of network vulnerabilities in modern network infrastructure, namely in Encrypted Server Name Indication (ESNI) in TLS 1.3 and in DNS over HTTPS (DoH).
- Used Noctilucent to explore means of circumventing censorship using ESNI on Microsoft Azure. Notably, TLS 1.3 is employed by nearly **30%** of all websites on the Internet and **59%** of the websites hosted on Cloudflare.

Review of Scheduling in Mixed-Criticality Systems BITS Pilani

Worked with Prof. Biju K Raveendran *September 2019 – November 2019*

- Reviewed various scheduling algorithm like Global Preemptive EDF, Criticality Based EDF (CBEDF), etc. and various resource sharing protocols like Priority Ceiling Protocol (PCP), Priority Inheritance Protocol (PIP), etc.
- Implemented the Earliest Deadline First with Virtual Deadline (EDF-VD) Scheduling Algorithm by Prof. Baruah et al. in C and released it on GitHub.

Teaching Experience

Teaching Assistant - Department of CS & IS BITS Pilani

Designed and conducted tutorials, graded papers, and provided guidance to students for the core courses:

- Data Structure and Algorithm (Semester II, 2019 - 2020)
- Computer Programming (Semester II, 2019 - 2020)
- Logic in Computer Science (Semester I, 2019 - 2020)

Open Source Contributions

RTEMS: Code Contributions, Documentation Contributions | **Siemens S7200 C++ Driver**: Code Contributions

Skills

Programming Languages: C, C++, Java, Python 3, SQL

Systems: Linux Kernel, RTEMS Real Time Kernel