ECT201 SOLID STATE DEVICES

COURSE COMPLETION PROJECT

Submitted By:

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Roll Number:27

University Register Number: KNR23EC053

1. BJT PROJECT

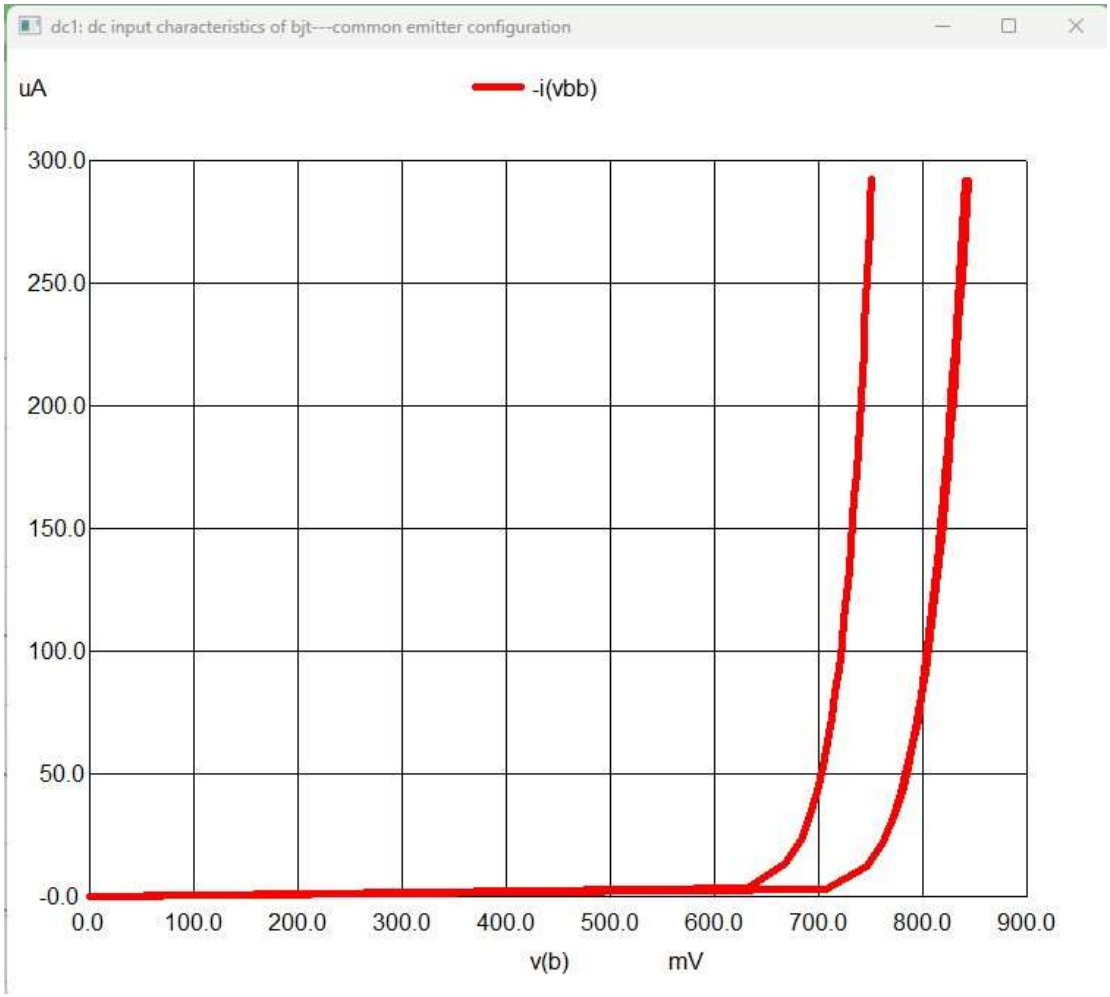
1 . Plot the input (IB vs VBE for different VCE) and output characteristics (IC vs VCE for different IB) of a NPN transistor in CE (common emitter) mode.

Ans :

PROGRAM FOR INPUT:

```
* Collector voltage source: vcc c 0 dc 0
* Base voltage source: vbb 2 0 dc 0
* Base series resistance: rb 2 b 100k
* NPN transistor model: q1 c b 0 bfs17

.MODEL BFS17 NPN (level=1 IS=0.48F NF=1.008 BF=99.655 VAF=90.000 IKF=0.190
 + ISE=7.490F NE=1.762 NR=1.010 BR=38.400 VAR=7.000 IKR=93.200M
 + ISC=0.200F NC=1.042 RB=1.500 IRB=0.100M RBM=1.200 RE=0.500 RC=2.680
 + CJE=1.325P VJE=0.700 MJE=0.220 FC=0.890 CJC=1.050P VJC=0.610 MJC=0.240
 + XCJC=0.400 TF=56.940P TR=1.000N PTF=21.000 XTF=68.398 VTF=0.600 ITF=0.700
 + XTB=1.600 EG=1.110 XTI=3.000 KF=1.000F AF=1.000)

.control
   save @q1[ib] @q1[ic] i(vbb) v(b)

* DC Analysis:
* Output characteristics: First, sweep the base voltage to produce input current (Ib)
* Then, sweep the collector voltage to plot a family of curves for different collector voltages

dc vbb 0 30 1
dc vcc 0 30 10

* Plot input characteristics (Ib vs Vbe)
plot -i(vbb) vs v(b)

.endc
.end
```

Wave Form :



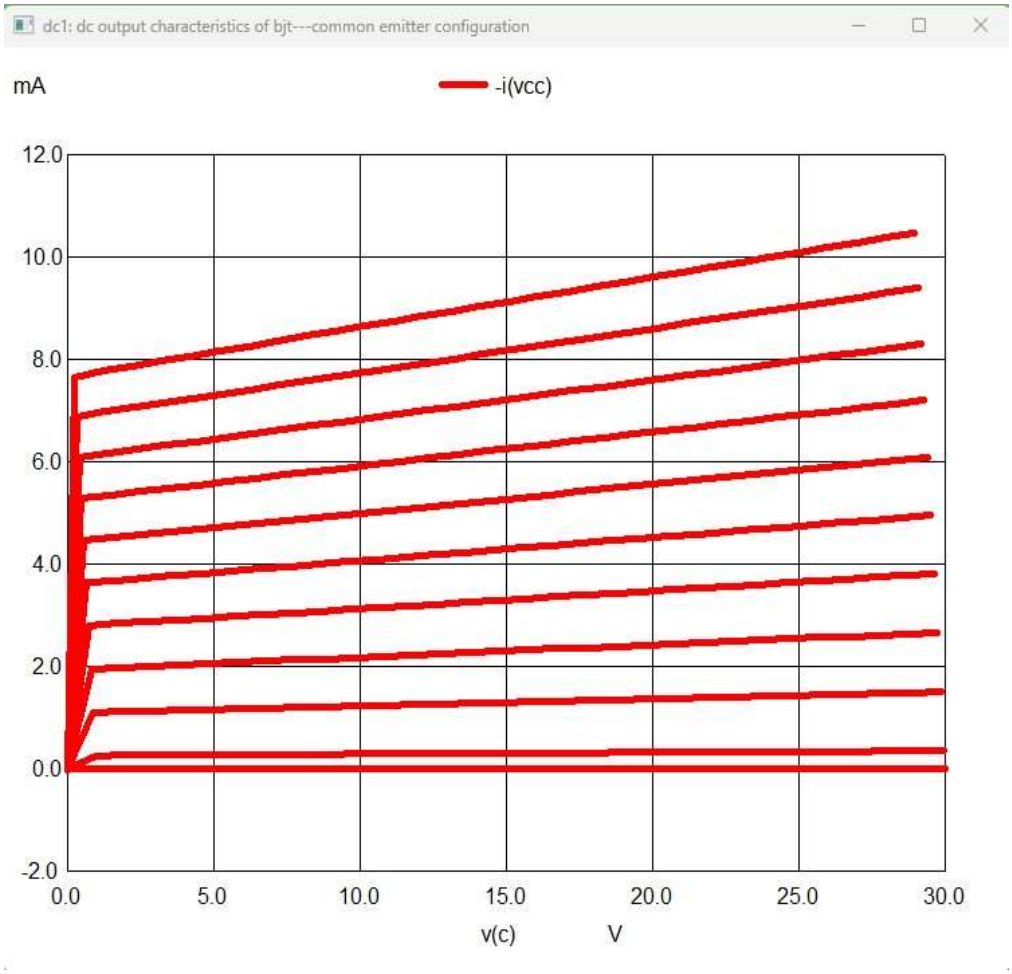
PROGRAM FOR OUTPUT :

* Collector voltage source: vcc 1 0 dc 0
* Base voltage source: vbb 2 0 dc 0
* Collector series resistance: rc 1 c 100
* Base series resistance: rb 2 b 100k
* NPN transistor model: q1 c b 0 bfs17

.MODEL BFS17 NPN (level=1 IS=0.48F NF=1.008 BF=99.655 VAF=90.000 IKF=0.190
+ ISE=7.490F NE=1.762 NR=1.010 BR=38.400 VAR=7.000 IKR=93.200M
+ ISC=0.200F NC=1.042 RB=1.500 IRB=0.100M RBM=1.200 RE=0.500 RC=2.680
+ CJE=1.325P VJE=0.700 MJE=0.220 FC=0.890 CJC=1.050P VJC=0.610 MJC=0.240
+ XCJC=0.400 TF=56.940P TR=1.000N PTF=21.000 XTF=68.398 VTF=0.600 ITF=0.700
+ XTB=1.600 EG=1.110 XTI=3.000 KF=1.000F AF=1.000)

```
.control
    save @q1[ib] @q1[ic] i(vcc) v(c)
* DC Analysis:
* Output characteristics: First, sweep the collector voltage to produce output current (Ic)
* Then, sweep the base voltage to plot a family of curves for different base currents

dc vcc 0 30 1
dc vbb 0 10 1

* Plot output characteristics (Ic vs Vce)
plot -i(vcc) vs v(c)

.endc
.endWave
```

Form:



Observations on the DC Input and Output Characteristics of BJT in Common Emitter Configuration

1. DC Input Characteristics

- **Setup**:
  The circuit includes a BJT with a base voltage source (Vbb) and a base series resistance (Rb). The simulation sweeps the base voltage from 0V to 30V, while the collector voltage is held constant at 0V.

- **Expected Output**:

  - **Input Current (Ib)**:
    As the base voltage (Vb) increases, the base current (Ib) will also increase. Due to the transistor's current gain (BF), this will result in an increase in collector current (Ic).

  - **Characteristic Curve**:
    The plot of −Ibb-I_{bb}−Ibb (negative base current) versus VbV_bVb will display an exponential increase as the base voltage crosses the base-emitter threshold voltage (approximately 0.7V for silicon transistors). The curve will start to level off as the transistor approaches saturation, where further increases in base voltage produce diminishing returns in base current.

2. DC Output Characteristics

- **Setup**:
  This simulation examines the output characteristics, where the collector voltage (Vcc) is swept from 0V to 30V, and the base voltage is varied from 0V to 10V. The collector current (Ic) is plotted against the collector voltage (Vc).

- **Expected Output**:

  - **Output Current (Ic)**:
    Initially, as the collector voltage increases, the collector current will increase linearly in response to the base current, up to the point of saturation. Beyond this saturation point, further increases in the collector voltage result in minimal increases in the collector current.

  - **Family of Curves**:
    The plot will show a family of curves for different base voltages. With higher base voltages, the output current increases for a given collector voltage. The curves display the BJT's characteristic behaviour, where the collector current is low at lower base voltages and significantly higher at higher base voltages.

- **Active Region**:
  The curves illustrate the transistor's linear (active) region, where it functions as an amplifier, followed by the saturation region, where the collector current becomes nearly constant, regardless of further increases in collector voltage.

Summary of Observations

- **Input Characteristics**:
  The exponential relationship between base voltage and base current is observed, consistent with the behaviour of BJTs.

- **Output Characteristics**:
  The output characteristics demonstrate the transistor's amplification capability and clearly outline the cutoff, active, and saturation regions.

- **Practical Insight**:
  These simulation results are valuable for understanding the BJT's behavior, especially for designing amplifier circuits, and offer insights into the voltage-current trade-offs in BJT configurations.

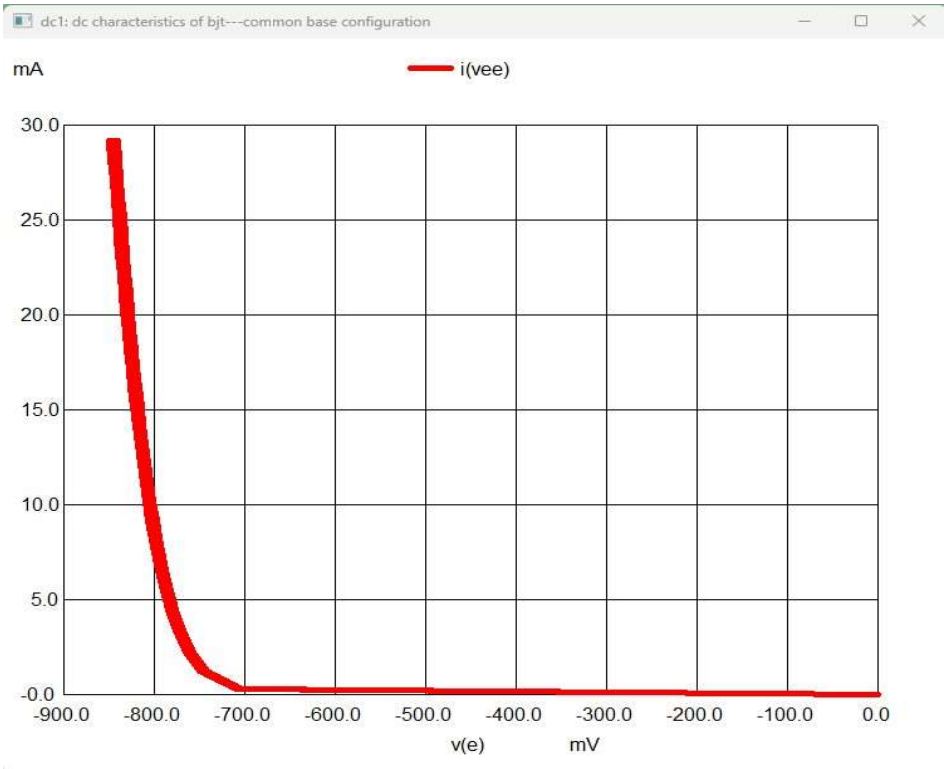
2. Plot the input (IE vs VEB for different VCB) and output characteristics (IC vs VCB for different IE) of a NPN transistor in CB (common base) mode.

PROGRAM FOR INPUT:

```
 * DC Characteristics of BJT - Common Base Configuration
* Collector voltage source: vcc c 0 dc 0
* Emitter voltage source: vee 2 0 dc 0
* Emitter series resistance: re 2 e 1k
* NPN Transistor: q1 c 0 e bfs17

.MODEL BFS17 NPN (level=1 IS=0.48F NF=1.008 BF=99.655 VAF=90.000 IKF=0.190
+ ISE=7.490F NE=1.762 NR=1.010 BR=38.400 VAR=7.000 IKR=93.200M
+ ISC=0.200F NC=1.042 RB=1.500 IRB=0.100M RBM=1.200 RE=0.500 RC=2.680
+ CJE=1.325P VJE=0.700 MJE=0.220 FC=0.890 CJC=1.050P VJC=0.610 MJC=0.240
+ XCJC=0.400 TF=56.940P TR=1.000N PTF=21.000 XTF=68.398 VTF=0.600 ITF=0.700
+ XTB=1.600 EG=1.110 XTI=3.000 KF=1.000F AF=1.000)

.control
   * DC Analysis - Input Characteristics:
   * Sweep the emitter voltage to generate input current (IE)
   * Then sweep collector voltage to plot family of curves for different collector voltages
```

```
   dc vee 0 -30 -1
   dc vcc 0 30 10

   * Plot input characteristics (IE vs VE)
   plot i(vee) vs v(e)

.endc
.end
```

Wave Form :

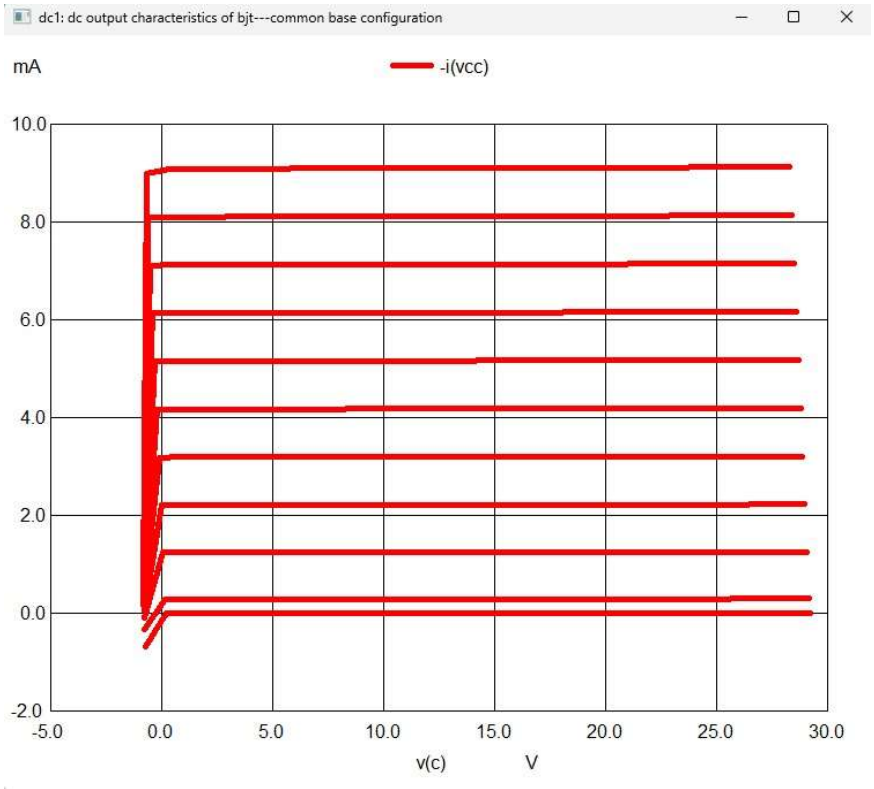


PROGRAM FOR OUTPUT:

```
 * DC Output Characteristics of BJT - Common Base Configuration
* Collector voltage source: vcc 1 0 dc 0
* Emitter voltage source: vee 2 0 dc 0
* Collector series resistance: rc 1 c 100
* Emitter series resistance: re 2 e 1k
* NPN Transistor: q1 c 0 e bfs17

.MODEL BFS17 NPN (level=1 IS=0.48F NF=1.008 BF=99.655 VAF=90.000 IKF=0.190
 + ISE=7.490F NE=1.762 NR=1.010 BR=38.400 VAR=7.000 IKR=93.200M
```

```
+ ISC=0.200F NC=1.042 RB=1.500 IRB=0.100M RBM=1.200 RE=0.500 RC=2.680
+ CJE=1.325P VJE=0.700 MJE=0.220 FC=0.890 CJC=1.050P VJC=0.610 MJC=0.240
+ XCJC=0.400 TF=56.940P TR=1.000N PTF=21.000 XTF=68.398 VTF=0.600 ITF=0.700
+ XTB=1.600 EG=1.110 XTI=3.000 KF=1.000F AF=1.000)

.control
   * DC Analysis - Output Characteristics:
   * Sweep the collector voltage to produce output current (IC)
   * Then sweep emitter voltage to plot family of curves for different emitter currents

   dc vcc -0.8 30 1
   dc vee 0 -10 -1

* Plot output characteristics (IC vs VC)
   plot -i(vcc) vs v(c)
.endc
.end
```

Wave Form :



Observations on the DC Input and Output Characteristics of BJT in Common Base Configuration

1. DC Input Characteristics

- **Setup**:
  The setup includes a BJT with a collector voltage source (Vcc) and an emitter voltage source (Vee) connected through a series resistance (Re). The simulation sweeps the emitter voltage (Vee) from 0V to -30V, while the collector voltage is held constant at 0V.
- **Expected Output**:
  - **Input Current (IE)**:
    As the emitter voltage (Ve) is made more negative, the emitter current (IE) will increase. This increase in IE will lead to a proportional increase in the collector current (IC), as IE and IC are closely related in the common base configuration.
  - **Characteristic Curve**:
    The plot of −Iee-I_{ee}−Iee (the negative of the emitter current) versus VeV_eVe will show an exponential increase as VeV_eVe becomes more negative and the base-emitter junction is forward-biased. At very negative emitter voltages, the curve will begin to flatten as the transistor reaches the saturation region, where further increases in emitter voltage result in diminishing increases in current.

2. DC Output Characteristics

- **Setup**:
  This simulation analyzes the output characteristics by sweeping the collector voltage (Vcc) from -0.8V to 30V while varying the emitter voltage (Vee) from 0V to -10V. The collector current (IC) is plotted against the collector voltage (Vc).
- **Expected Output**:
  - **Output Current (IC)**:
    Initially, as the collector voltage increases, the collector current will rise linearly due to the emitter current's influence. After a point, increasing the collector voltage will cause the transistor to enter saturation, where IC becomes relatively stable.
  - **Family of Curves**:
    The plot will show a series of curves for different emitter voltages. Higher emitter voltages result in greater emitter and, consequently, collector currents. The family of curves exhibits the typical common base configuration, where a low emitter voltage yields a low collector current, and a more negative emitter voltage produces a higher collector current.
  - **Active Region**:
    The curves highlight the active region, where the transistor functions linearly,

followed by saturation, where IC plateaus and becomes largely independent of further increases in Vcc.

Summary of Observations

- **Input Characteristics**:
  Display an exponential increase of emitter current as the emitter voltage is made more negative, which is characteristic of BJTs in the common base configuration.
- **Output Characteristics**:
  Illustrate the transistor's ability to operate as an amplifier, with a clear transition between the cutoff, active, and saturation regions.
- **Practical Insight**:
  These characteristics are useful for designing amplifiers, especially in high-frequency applications where the common base configuration is preferred. The simulations provide insights into current flow and gain adjustments in BJT applications.

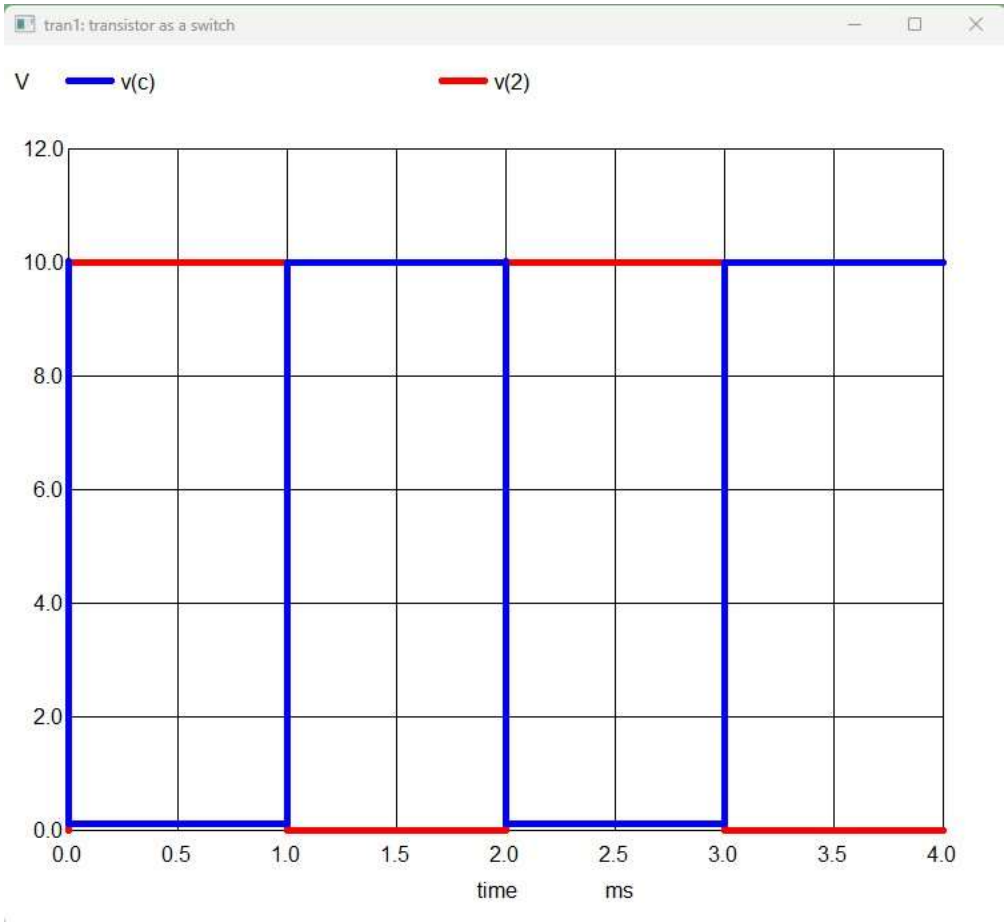
3.*Configure transistor as a switch and observe the output voltage for a pulse input. Explain the nature of the output in comparison with input.*

PROGRAM FOR TRANSISTOR AS A SWITCH :

```
* Collector voltage source: vcc 1 0 dc 10
* Base voltage source (pulse input): vbb 2 0 pulse 0 10 0.1u 0.1u 0.1u 1m 2m
* Collector series resistance: rc 1 c 1k
* Base series resistance: rb 2 b 50k
* NPN Transistor: q1 c b 0 bfs17

.MODEL BFS17 NPN (level=1 IS=0.48F NF=1.008 BF=99.655 VAF=90.000 IKF=0.190
 + ISE=7.490F NE=1.762 NR=1.010 BR=38.400 VAR=7.000 IKR=93.200M
 + ISC=0.200F NC=1.042 RB=1.500 IRB=0.100M RBM=1.200 RE=0.500 RC=2.680
 + CJE=1.325P VJE=0.700 MJE=0.220 FC=0.890 CJC=1.050P VJC=0.610 MJC=0.240
 + XCJC=0.400 TF=56.940P TR=1.000N PTF=21.000 XTF=68.398 VTF=0.600 ITF=0.700
 + XTB=1.600 EG=1.110 XTI=3.000 KF=1.000F AF=1.000)

.control
   * Transient analysis: Sweep time up to 4ms
   tran 1u 4m

   * Set background color to white, grid lines black, plot red, and line width to 10
   set color0=white
   set color1=black
   set color2=red
```

```
   set color3=blue
   set xbrushwidth=5

   * Plot pulse input voltage (v(2)) and collector voltage (v(c))
   plot v(2) v(c)

.endc
.end
```

Wave Form :



Observations on Transistor as a Switch

1. **Switching Behavior**:

- **Pulse Input (Base Voltage)**:
  The base voltage follows the pulse waveform, alternating between 0V and 10V. At 0V, the transistor is in the **cutoff region**, meaning no base current flows, and the transistor remains off. When the base voltage is at 10V, the transistor is in the **saturation region**, allowing current to flow through the collector-emitter path.

- **Collector Voltage (Vc)**:
  The collector voltage (Vc) responds to the pulse input at the base. When the transistor is off (base at 0V), Vc is high, close to Vcc (10V). When the transistor turns on (base at 10V), Vc drops close to 0V, indicating the transistor is in saturation and effectively shorting the collector to the emitter.

2. **Characteristic Curve**:

- **On and Off States**:
  The plot of collector voltage vs. time will show a clear switching action. Vc will alternate between high (off state) and low (on state) voltages, with the switching times corresponding to the pulse input. This confirms the transistor's ability to act as a digital switch.

3. **Saturation and Cutoff**:

- In the **saturation state**, the collector-emitter path is conductive, and the transistor effectively acts as a closed switch.
- In the **cutoff state**, the transistor does not conduct, and Vc remains high, indicating the open-switch behavior.

Summary of Observations

- **Transistor Switching Function**:
  The transistor functions effectively as a switch, with a clear distinction between on (saturation) and off (cutoff) states.
- **Pulse Response**:
  The response of Vc to the pulse input confirms that the transistor quickly toggles between states in response to base voltage changes, making it suitable for applications in digital circuits.
- **Practical Insight**:
  This switching behavior is fundamental for digital electronics, where transistors are used as switches in logic gates and other circuits that require rapid on/off transitions. The configuration highlights the versatility of BJTs in signal switching and control applications.

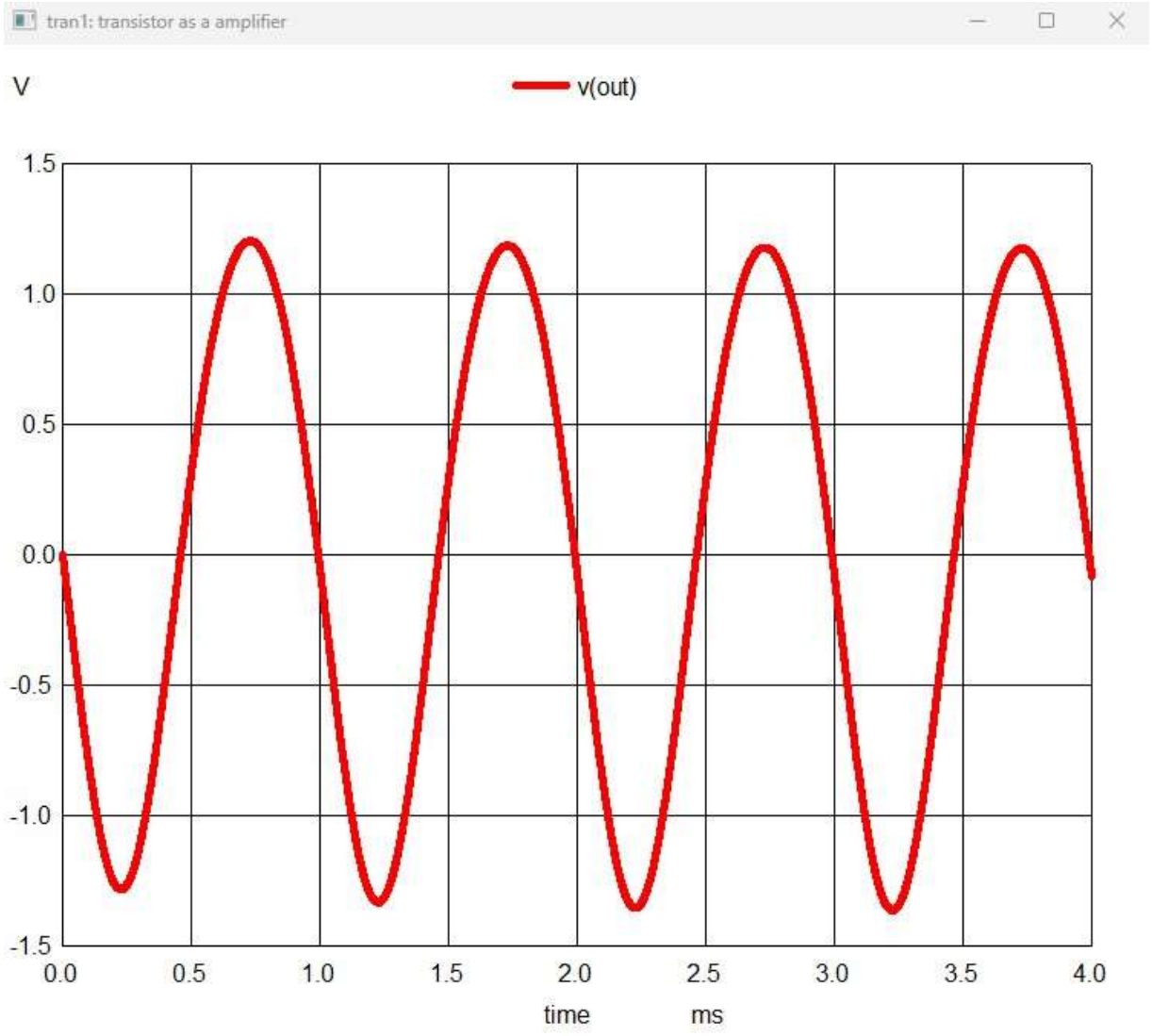
4.Configure transistor as a CE amplifier and observe the output voltage for a sine wave input. What is the voltage gain of the amplifier if the sine wave input has an amplitude of 10mV?

PROGRAM FOR TRANSISTOR AS AN AMPLIFIER:

```
* Common Emitter Amplifier Configuration

* Collector voltage source
vcc 1 0 dc 10
* Base voltage source (Sine Wave)
vin in 0 sin(0 0.01 1000)
* Input and Output Capacitors
c1 in b 10u
c2 c out 10u
* Load Resistor
rl out 0 10k
* Collector Series Resistance
rc 1 c 2k
* Voltage Divider Bias Resistors
r1 1 b 20k
r2 b 0 5k
* Emitter Resistance and Capacitor
re e 0 500
ce e 0 100u
* NPN Transistor
q1 c b e bfs17
* NPN Transistor Model

.MODEL BFS17 NPN ( level=1 IS=0.48F NF=1.008 BF=99.655 VAF=90.000 IKF=0.190 + ISE=7.490F NE=1.762 NR=1.010 BR=38.400 VAR=7.000 IKR=93.200M + ISC=0.200F NC=1.042 RB=1.500 IRB=0.100M RBM=1.200 + RE=0.500 RC=2.680 CJE=1.325P VJE=0.700 MJE=0.220 FC=0.890 + CJC=1.050P VJC=0.610 MJC=0.240 XCJC=0.400 + TF=56.940P TR=1.000N PTF=21.000 + XTF=68.398 VTF=0.600 ITF=0.700 + XTB=1.600 EG=1.110 XTI=3.000 + KF=1.000F AF=1.000)

.control
* Transient Analysis (4ms)
tran 1u 4m
* Set Plot Parameters
set color0=white
set color1=black
set color2=red
set color3=blue

set xbrushwidth=5
* Plot Input and Output Voltages
plot v(in) v(out)
.endc
```

.end

Wave Form:



Observations on Transistor as an Amplifier

Circuit Configuration:

- The circuit employs an NPN transistor (BFS17) configured as a common emitter amplifier.
- The collector voltage source (Vcc) is set to 10V, while the input signal (Vin) is a sinusoidal waveform with an amplitude of 0.01V and a frequency of 1 kHz.
- Capacitor C1 is used at the input to block any DC offset, allowing only the AC signal to pass. Similarly, the output capacitor (C2) blocks any DC component from the output signal.

Amplification Process:

- Biasing: The transistor is biased using a voltage divider network formed by resistors R1R_1R1 and R2, ensuring proper operation in the active region. The emitter resistor (Re) stabilizes the bias point against variations in temperature and transistor characteristics.
- Gain Calculation: The gain of the amplifier can be estimated using the formula: Voltage Gain (Av)=−RLRe. In this configuration, with RL=10kR_L = 10kRL=10k and Re=500R_e = 500Re=500, the gain is significant, indicating that the output voltage is an amplified version of the input signal.

Output Characteristics:

- Transient Analysis: The transient analysis sweeps up to 4 milliseconds, allowing for observation of the amplifier's response over multiple cycles of the input signal.
- Waveform Analysis: The output voltage (Vout) is expected to show a larger amplitude sinusoidal waveform compared to the input (Vin). The output waveform will exhibit a 180-degree phase shift due to the nature of the common emitter configuration.

Observations from Waveform:

- Signal Distortion: If the input signal amplitude is too large, the transistor may enter saturation or cutoff, leading to distortion in the output waveform, which appears as clipping at the waveform peaks.
- Frequency Response: The frequency response of the amplifier will be limited by the coupling capacitors and the resistances in the circuit. At very high frequencies, the gain may decrease due to capacitive reactance effects.

Summary of Observations:

- The BJT functions effectively as an amplifier, with the output signal exhibiting a larger amplitude compared to the input signal while showing a phase inversion.
- The transient response provides valuable insights into the dynamic behavior of the amplifier, illustrating its performance in practical applications.
- This configuration is commonly used in audio and RF amplifiers, demonstrating its utility in amplifying small signals for larger outputs.

2. MOS PROJECT

1. Draw the output characteristics (Ids vs Vds for different Vgs values) of a N type enhancement mode MOSFET. Draw its transfer characteristics (Ids vs Vgs for different Vds values).

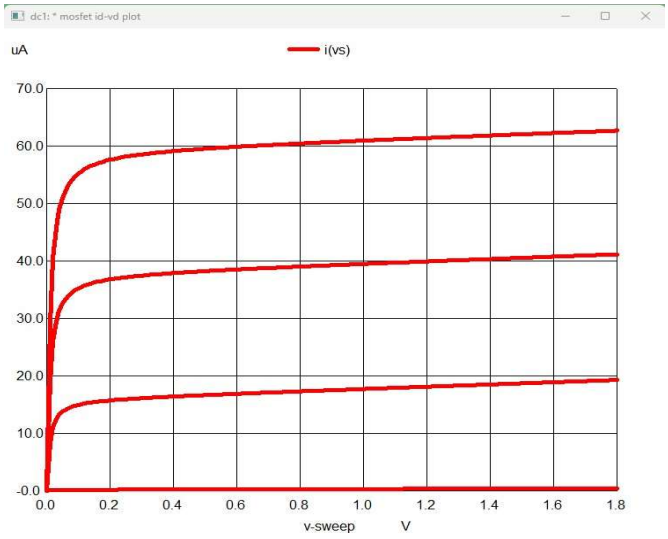
PROGRAM :

```
* MOSFET Id-Vd plot *
.include "mosmodel.txt"
* Drain voltage source
vd d 0 dc=1.8
* Gate voltage source
vg g 0 dc=0
* Source and substrate are grounded
vs s 0 dc=0
vb b 0 dc=0
* MOSFET model
m1 d g s b CMOSN W=10e-6 L=180e-9
* Sweep drain voltage and gate voltage
.dc vd 0.0 1.8 0.01 vg 0.4 1.8 0.4
.control
run
* Plot settings
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5
plot i(vs)
.endc
.end
```

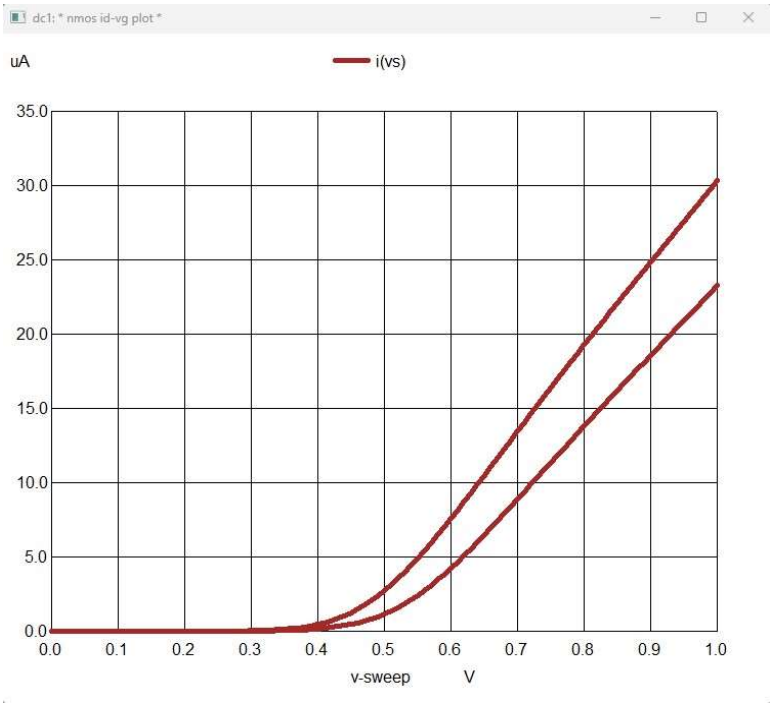
```
* NMOS Id-Vg plot *
.include "mosmodel.txt"
* Drain voltage source
vd d 0 dc=0
* Gate voltage source
vg g 0 dc=0
* Source and substrate are grounded
vs s 0 dc=0
vb b 0 dc=0
* MOSFET model
m1 d g s b CMOSN W=10e-6 L=180e-9
* Sweep gate voltage and drain voltage
.dc vg 0 1.0 0.01 vd 0.05 1.8 1.75
.control
run
* Plot settings
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5
plot i(vs)
.endc
.end
```

WAVE FORM :

Ids V/s Vds :



Ids V/s Vgs:



Output and Transfer Characteristics of an N-Type Enhancement Mode MOSFET

Output Characteristics (IDS vs. VDS for Different VGS Values)

1. **Description:**
    - The output characteristics graph shows how the drain current IDS changes with the drain-source voltage VDS for various gate-source voltages VGS.
    - When VGS is increased above the MOSFET's threshold voltage VTH IDS rises, reflecting the MOSFET turning on.
    - Each VGS value produces a separate curve, with IDS eventually saturating for higher VDS values.
2. **Key Points:**
    - The MOSFET remains off, with IDS=0, until VGS surpasses VTH.

- After crossing the threshold, IDS initially rises linearly with VDS, entering the saturation region where it then levels off.
- Higher VGS values create distinct curves, showing greater IDS values as VGS increases.

Transfer Characteristics IDS vs. VGS for Different VDS Values)

1. **Description:**
   - The transfer characteristics graph illustrates how IDSI_{DS}IDS varies with VGSV_{GS}VGS for a set of constant VDSV_{DS}VDS values.
   - This plot shows the sensitivity of IDSI_{DS}IDS to changes in VGSV_{GS}VGS, especially as different VDSV_{DS}VDS levels are applied.
2. **Key Points:**
   - At low VGS, IDS remains close to zero until VGS exceeds VTH.
   - Once VGS goes beyond VTH, IDS increases sharply, signifying the device's transition from cutoff to saturation.
   - Beyond a certain point, IDS plateaus, indicating that the MOSFET has reached saturation.

Summary of Results:

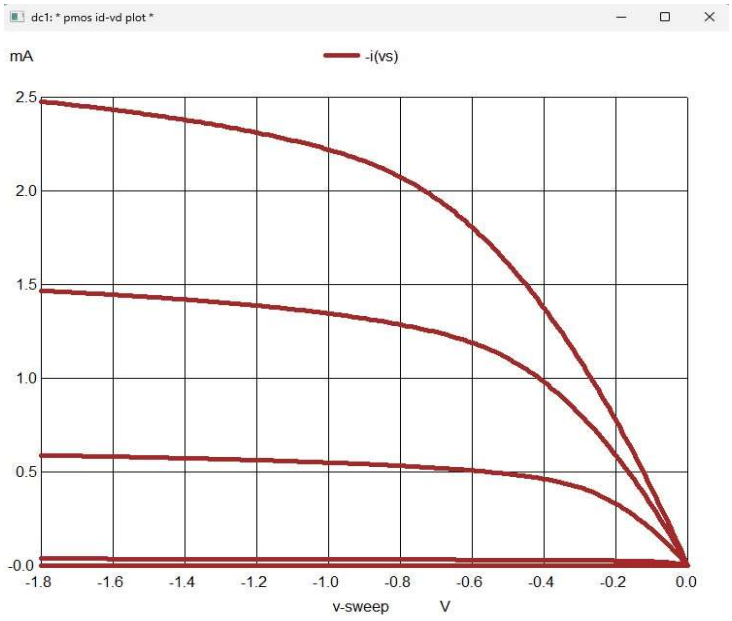
- **Output Characteristics:**
  - Each curve shows that as VGS rises, the peak IDS also increases, with saturation occurring at progressively higher VDS levels for each VGS value**.**
- **Transfer Characteristics:**
  - The graph indicates a sharp increase in IDS as VGS rises above VTH, with the curves' shapes varying slightly based on the VDS applied**.**

2.Draw the output characteristics (Ids vs Vds for different Vgs values) of a P type enhancement mode MOSFET. Draw its transfer characteristics. (Ids vs Vgs for different Vds values).

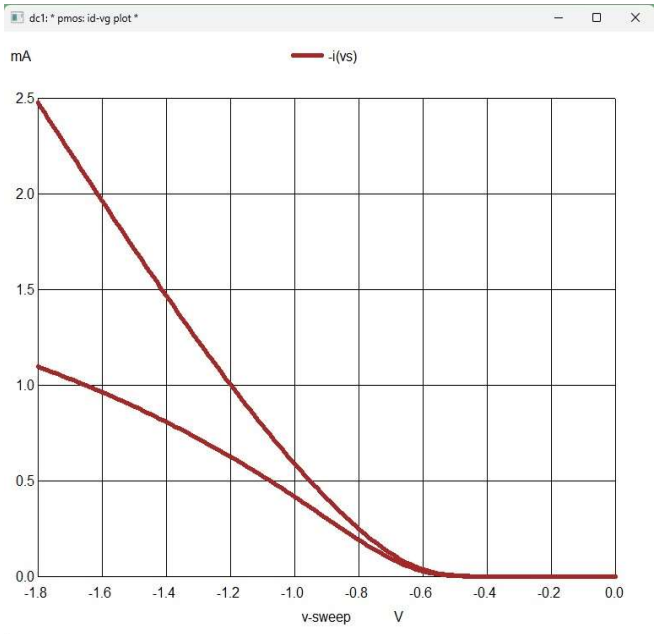
PROGRAM :

```
* PMOS Id-Vd plot *
* include the mosmodel.txt in the same folder
 .include "mosmodel.txt"
* drain voltage source
vd d 0 dc=0
* gate voltage source  vg g 0 dc=0
* source and substrate are grounded  vs s 0 dc=0  vb b 0 dc=0
* p mosfet model name is same as that given in the model file  m1 d g s b CMOSP
   W=10e-6 L=180e-9
* run drain voltage first and then sweep gate voltage to get the family of curves
 .dc vd -1.8 0.0 0.01 vg -1.8 -0.0 0.4
 .control
run
 *set background color as white, grid lines black, plot red and width of the
line=10  set color0=white  set color1=black
 set color2=red
set color2=brown
set xbrushwidth=5
plot -i(vs)
 .endc
 .end

* pmos: Id-Vg plot *
* include the mosmodel.txt in the same folder
 .include "mosmodel.txt"
* drain voltage source
vd d 0 dc=0

* gate voltage source  vg g 0 dc=0
* source and substrate are grounded  vs s 0 dc=0  vb b 0 dc=0
* p mosfet model name is same as that given in the model file  m1 d g s b CMOSP
   W=10e-6 L=180e-9
* run gate voltage first and then sweep drain voltage to get the family of curves
 .dc vg -1.8 0 0.01 vd -1.8 -0.05 1.5
 .control
run
 *set background color as white, grid lines black, plot red and width of the
line=10  set color0=white  set color1=black  set color2=red  set color2=brown  set
xbrushwidth=5  plot -i(vs)
 .endc
 .end
```

WAVE FORM: (Id V/S Vd):



Id v/s Vgs :



Output and Transfer Characteristics of a P-Type Enhancement Mode MOSFET

1. **Description:**
    - The output characteristics graph shows the drain current Ids plotted against the drain-source voltage Vds for different gate-source voltages Vgs in a P-type enhancement mode MOSFET.
    - As Vgs becomes more negative, Ids increases, indicating the MOSFET turning on.
2. **Key Points:**
    - The MOSFET remains off, with Ids at 0, until Vgs falls below the threshold voltage (a negative threshold).
    - As Vgs is made more negative, Ids starts increasing, showing that the device is active.
    - Each Vgs value creates a distinct output curve, with higher Ids values observed as Vgs becomes more negative.

Transfer Characteristics (Ids vs. Vgs for Different Vds Values)

1. **Description:**
    - The transfer characteristics graph shows how Ids varies with gate-source voltage Vgs when different fixed values of Vds are applied.
    - This plot highlights how Ids changes with Vgs for a set Vds value.
2. **Key Points:**
    - At less negative Vgs, Ids is close to zero until Vgs surpasses the negative threshold.
    - As Vgs becomes more negative, Ids rises rapidly, marking the transition of the P-MOSFET from cutoff to saturation.
    - Eventually, Ids reaches a steady maximum, illustrating the MOSFET's saturation.

Summary of Results:

- **Output Characteristics:**

- The graph shows that as Vgs becomes more negative, Ids increases, with each curve indicating a specific Vgs value.

- **Transfer Characteristics:**

  - The plot reveals a rapid rise in Ids as Vgs becomes more negative, with curve shapes depending on the Vds levels applied.

3.Create an CMOS inverter using n-type and p-type enhancement MOSFETs and show that for a pulse input the circuit behaves like an inverter (NOT gate).

PROGRAM:

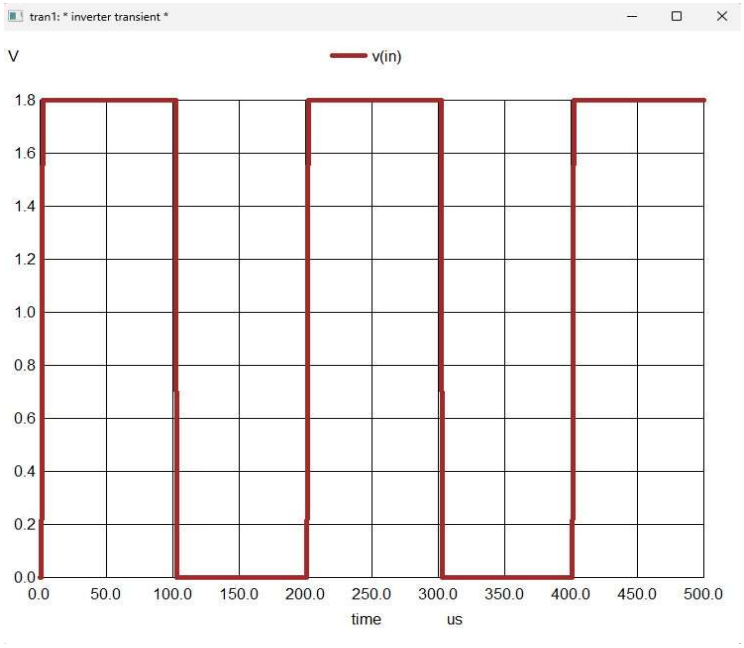
```
* Inverter Transient *
.include "mosmodel.txt"
* Supply voltage
v1 vdd 0 dc=1.8
* Pulse input source
v2 in 0 pulse 0 1.8 1u 1u 1u 100u 200u
* CMOS inverter (N-MOSFET and P-MOSFET)
mn out in 0 0 CMOSN W=1u L=180n
mp out in vdd vdd CMOSP W=2u L=180n
* Transient analysis for 500µs to observe at least two pulses
.tran 10n 500u
.control
run
* Plot settings
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5
plot v(in)
```

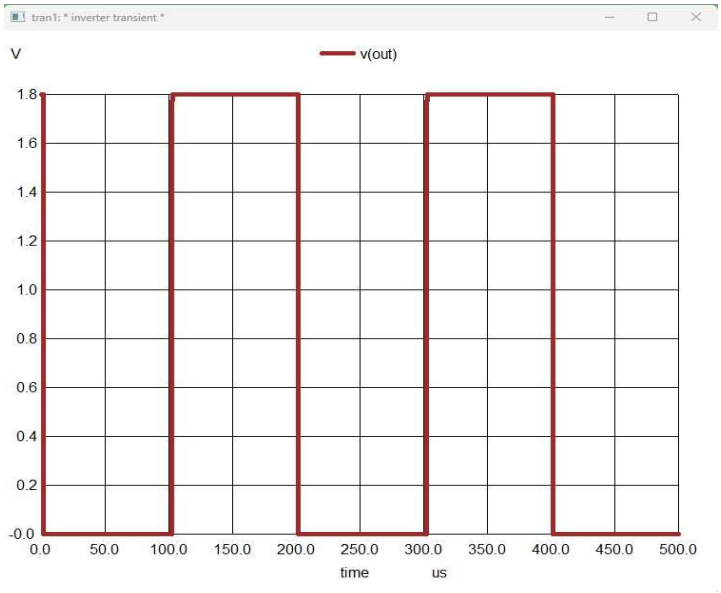
plot v(out)

.endc

.end

WAVE FORM:





CMOS Inverter Simulation

Objective:

To design a CMOS inverter using complementary n-type and p-type enhancement MOSFETs and verify its operation as an inverter (NOT gate) through pulse input testing.

Circuit Description:

- The inverter is constructed using a combination of one n-type MOSFET (MN) and one p-type MOSFET (MP), configured to produce an inverted output.
- A pulse signal is applied to the input, and the resulting output is monitored to verify the inverter's functionality.

Simulation Program:

1. **Power Supply:**
    - A DC supply voltage (Vdd) of 1.8V is applied.
2. **Input Source:**
    - A pulse voltage source (V2) is defined with a range of 0V to 1.8V, pulse width of 1µs, and a period of 200µs.
3. **MOSFET Definitions:**
    - **N-Type MOSFET (MN)** : Connected to pull the output down to ground. ○ **P-Type MOSFET (MP)** : Connected to pull the output up to Vdd.

4. **Transient Analysis:**
    - The transient analysis is set to run for 500 µs with a time interval of 10 ns, allowing for observation of at least two pulse cycles in the output response.

Key Simulation Details:

- **Input Pulse Behavior:** The input toggles between 0V and 1.8V, mimicking a digital signal.
- **Expected Output Behavior:** The output should be inversely related to the input: when the input voltage is high (1.8V), the output should be low (0V), and vice versa.

Expected Results:

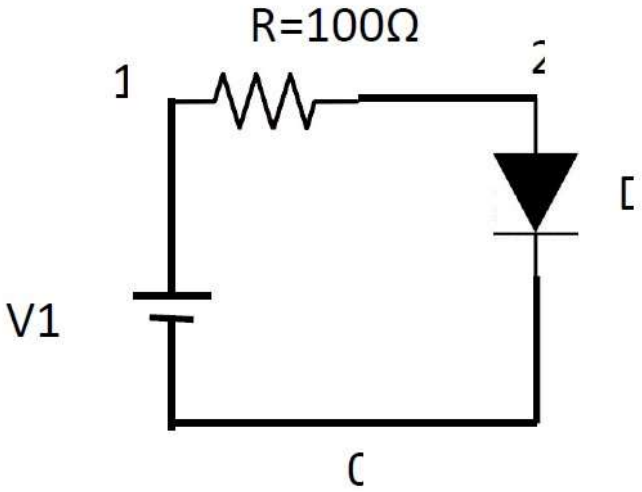
- **Output Voltage Behavior:** The output voltage (v(out)) should exhibit an inverted response to the input voltage (v(in)).
- **Inversion Confirmation:** The output should drop to low when the input is high, and rise to high when the input is low, confirming proper inverter action.

Visual Output:

- The simulation will display the input and output voltage waveforms over time, visually verifying the inverter’s correct operation.

3. PN-JUNCTION PROJECT

1. *Plot the I-V characteristics of a Si P-N junction diode. Keep the breakdown voltage as 50V. Change the breakdown voltage to 5V and plot the I-V characteristics. What is the difference in the observed outputs? Why?*



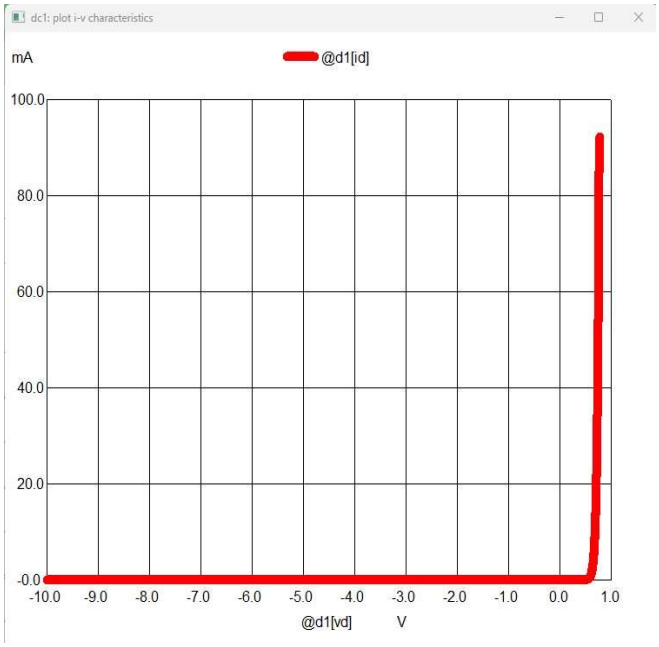
PROGRAM :

```
* Define DC voltage source
V1 1 0 dc 0
* Define current-limiting series resistor
R1 1 2 0.1k
* Define diode
D1 2 0 myd
* Define diode model parameters
* IS is reverse saturation current, VJ is cut-in voltage, BV is breakdown voltage
.model myd D(
  IS = 100p
  + N = 1.45
  + RS = 0
  + TT = 4.3u
  + CJ0 = 40p
  + VJ = 0.7
  + M = 0.33
  + EG = 1.11
  + XTI = 3
  + KF = 0
  + AF = 1
  + FC = 0.5
```

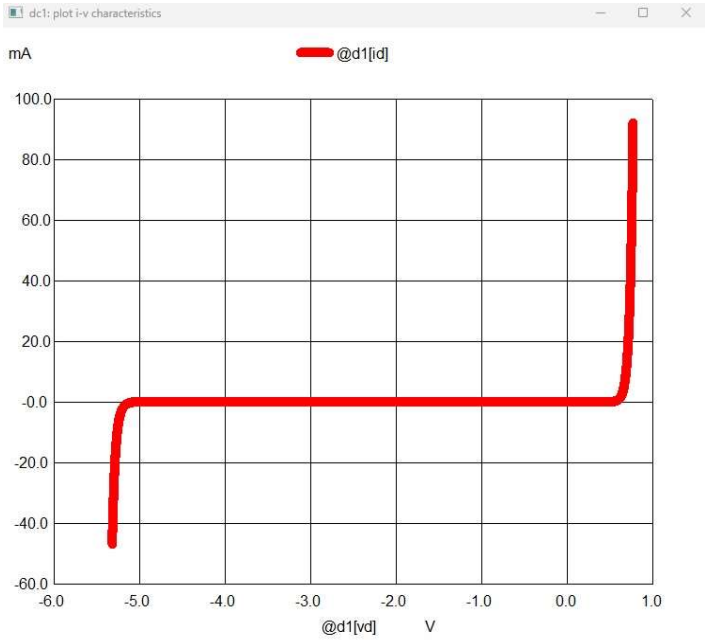
```
  + BV = 50
  + IBV = 10u
)

.control
  * Save diode current and voltage values
  save @D1[id] @D1[vd]

  * Run DC analysis from 5V less than breakdown voltage to 10V greater than cut-in voltage
  dc V1 -10 10 0.01

  * Set background color as white, grid lines black, plot line red, and line width = 10
  set color0 = white
  set color1 = black
  set color2 = red
  set xbrushwidth = 10

  * Plot current flowing through diode vs. diode voltage
  plot @D1[id] vs @D1[vd]
.endc
.END
```

Wave Form :

BV = 50



BV = 5



Observations on Diode I-V Characteristics

Circuit Configuration: The circuit is set up to analyze the I-V characteristics of a silicon P-N junction diode. A DC voltage source (V1) is connected in series with a current-limiting resistor (R1) and the diode (D1). The resistor R1 (0.1 kΩ) helps limit the current flowing through the diode, preventing it from reaching excessive values.

Diode Model: The diode D1 is defined using a specific model (myd) with parameters that closely reflect real diode characteristics:

- **Reverse Saturation Current (IS)** : Set to 100 pA, representing the leakage current when the diode is reverse-biased.
- **Junction Potential (VJ)** : Initially set to 0.7V, which is the threshold or "cut-in" voltage where significant current starts to flow.
- **Breakdown Voltage (BV)** : Initially set to 50V, indicating the point at which the diode enters breakdown when reverse-biased.

Afterward, the breakdown voltage is changed to 5V to observe the differences in the I-V characteristics.

Analysis Process:

- **DC Sweep** : A DC sweep is performed with the voltage V1 ranging from -10V to 10V, covering both forward and reverse bias conditions. This range allows observation of the diode's behavior as it approaches breakdown in the reverse bias region and reaches the threshold in the forward bias region.

Plotting Parameters:

- The background color is set to white, with black grid lines and a red plot line for clarity.
- The line width is increased for better visibility of the I-V curve.

Observations from I-V Characteristics:

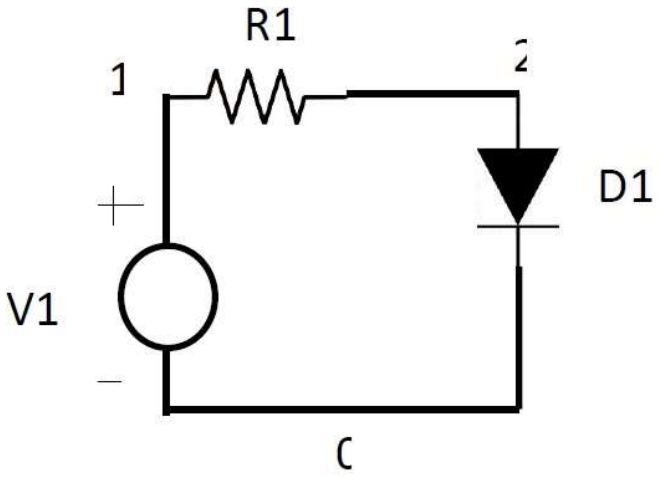
1. **Forward Bias Region** : As V1 approaches the cut-in voltage (VJ = 0.7V), the diode current increases exponentially, illustrating the typical forward bias behavior.
2. **Reverse Bias Region (BV = 50V)** : When V1 is negative and far below 0.7V, the current remains close to the reverse saturation value. As V1 approaches -50V (breakdown voltage), the diode would theoretically enter breakdown, leading to a sharp increase in current. However, the series resistor R1 limits this current.
3. **Reverse Bias Region (BV = 5V)** : Changing the breakdown voltage to 5V results in a significant difference in the reverse bias behavior. When V1 approaches -5V, the diode enters breakdown, and the current dramatically increases. The current at this voltage will be much higher than in the previous configuration with a 50V breakdown voltage, and the series resistor will have less effect on limiting the current during breakdown.

Key Takeaways:

- **Forward Conduction** : The diode conducts significantly when the applied voltage is above the threshold voltage (0.7V), showing exponential current increase typical for semiconductor diodes.
- **Reverse Saturation and Breakdown** : In reverse bias, the diode maintains a very low current until breakdown voltage is reached.
- **Impact of Breakdown Voltage** : The difference in breakdown voltage significantly affects the current behavior. With a breakdown voltage of 50V, the diode can withstand higher reverse voltages without conducting significant current, whereas with a breakdown voltage of 5V, the diode enters breakdown at a much lower voltage, leading to a higher reverse current. This highlights the importance of breakdown voltage in diode applications and protection against high reverse currents.

2.Apply a square wave input (-10V to 10V) of time period 2ms to a diode through a series resistor and observe the output. Change the time period from 2ms to 20us

and observe the output. What is the difference in the observed outputs? Why? Explain the behavior of current flowing through the diode



PROGRAM:

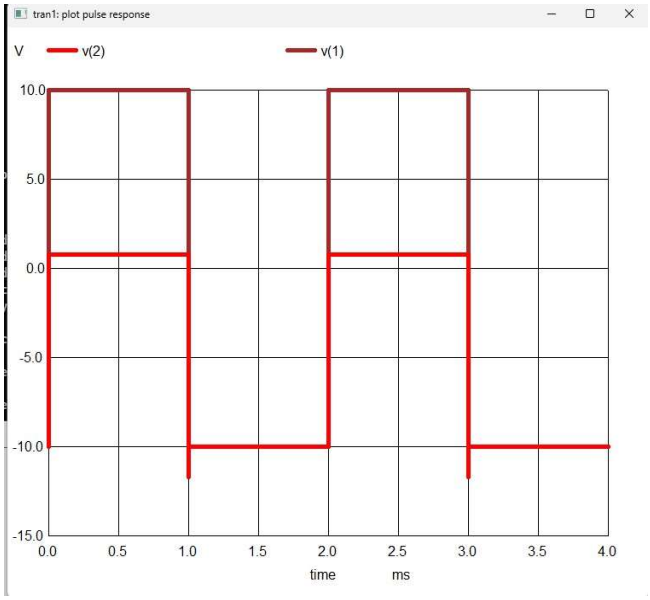
```
* Define pulse voltage source
V1 1 0 pulse(-10 10 0.1u 0.1u 0.1u 1m 2m)

* Define current-limiting series resistor
R1 1 2 0.1k

* Define diode
D1 2 0 myd

* Define diode model parameters
* IS is reverse saturation current, VJ is cut-in voltage, BV is breakdown voltage
.model myd D(
  IS = 100p
  + N = 1.45
  + RS = 0
  + TT = 4.3u
  + CJ0 = 40p
  + VJ = 0.7
  + M = 0.33
  + EG = 1.11
  + XTI = 3
  + KF = 0
  + AF = 1
  + FC = 0.5
  + BV = 50
  + IBV = 10u
```

)

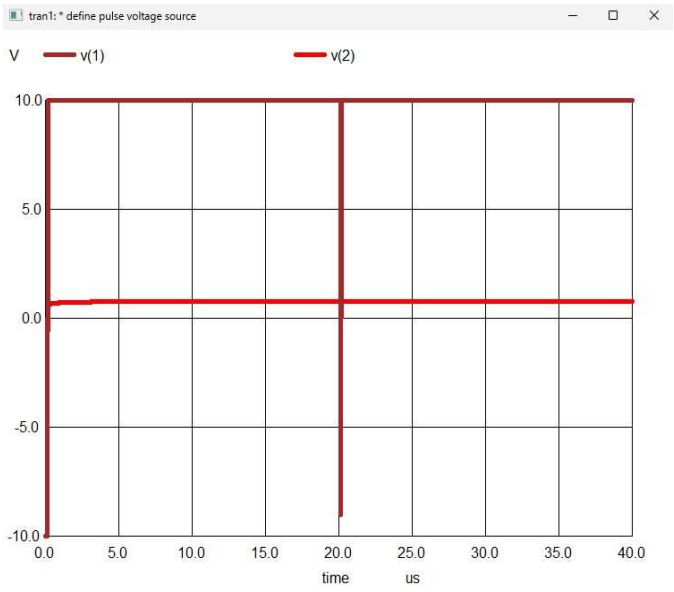
```
.control
  * Save diode current and voltage values, and node voltages
  save @D1[id] @D1[vd] v(1) v(2)

  * Run transient analysis for pulse response
  tran 0.01u 4m

  * Set background color as white, grid lines black, plot color red, and line width = 5
  set color0 = white
  set color1 = black
  set color2 = red
  set color3 = brown
  set xbrushwidth = 5

  * Plot input and output voltages
  plot @D1[id]
  plot v(1) v(2)
.endc

.END
```

WAVE FORMS :

2ms:



2us:



Observations on Diode Response to Square Wave Input

1. **Circuit Configuration:**
    - A square wave voltage source connects to a diode via a series resistor.
    - The square wave alternates between -10V and +10V.
    - Two simulation scenarios are observed:
        - First Simulation: 2 ms period
        - Second Simulation: 20 µs period
2. **Components:**
    - Pulse Voltage Source (V1): Defined as V1 1 0 pulse -10 10 0.1u 0.1u 0.1u 1m 2m for the 2 ms period and V1 1 0 pulse -10 10 0.1u 0.1u 0.1u 1m 20u for the 20 µs period.
    - Series Resistor (R1): 0.1 kΩ.
    - Diode (D1): Modeled with parameters that specify reverse saturation current, cutoff voltage, and breakdown voltage.

Observations:

1. **Output Behavior with a 2 ms Period:**

- The diode conducts when the voltage is positive (+10V) and stops conducting when the voltage is negative (-10V).
- Due to the longer period, the current through the diode gradually reaches a steady state, showing a smooth rise and fall in response to the input.
- This longer time allows the diode to charge and discharge more fully, resulting in a steady waveform.

2. **Output Behaviour with a 20 µs Period:**
    - The diode still conducts during the positive half of the cycle, but due to the shorter period, it doesn't have enough time to fully charge up to its maximum current.
    - The current shows a quick rise and fall, creating a sharper response compared to the 2 ms case.
    - The output oscillates more rapidly, and the current doesn't stabilize as it did with the longer period.

Comparison of Observed Outputs:

- Current Fluctuations: At 20 µs, the current fluctuates more abruptly, creating higher-frequency oscillations in the diode's response. In contrast, with a 2 ms period, the current transitions more smoothly, resulting in stable current levels.
- Charging and Discharging: With the 2 ms period, the diode has sufficient time to reach steady-state current, whereas in the 20 µs case, the diode is switching on and off before fully stabilizing. This produces lower average current in the shorter period.

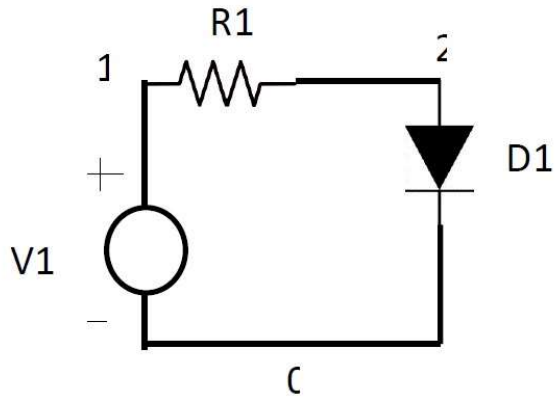
Explanation of Diode Current Behaviour:

- Charging and Discharging Dynamics: The time available for the diode to charge and discharge affects current flow. A longer period allows for greater current stability, while a shorter period leads to faster switching without full charging, yielding a lower average current.
- Response to Frequency: As the input frequency increases (shorter time periods), the diode shifts from a steady-state behavior to a rapid on-off switching pattern.

Conclusion:

- The diode's response to square wave inputs is highly dependent on the input period. Shorter periods lead to high-frequency oscillations with limited current stabilization, while longer periods allow for steady-state behavior and higher current levels.

3.Apply a square wave input (-10V to 10V) of time period 2ms to a diode through a series resistor and observe the output. Keep the breakdown voltage to 50V. Change the breakdown voltage to 5V and observe the output voltage. What is the difference in the observed outputs? Why?

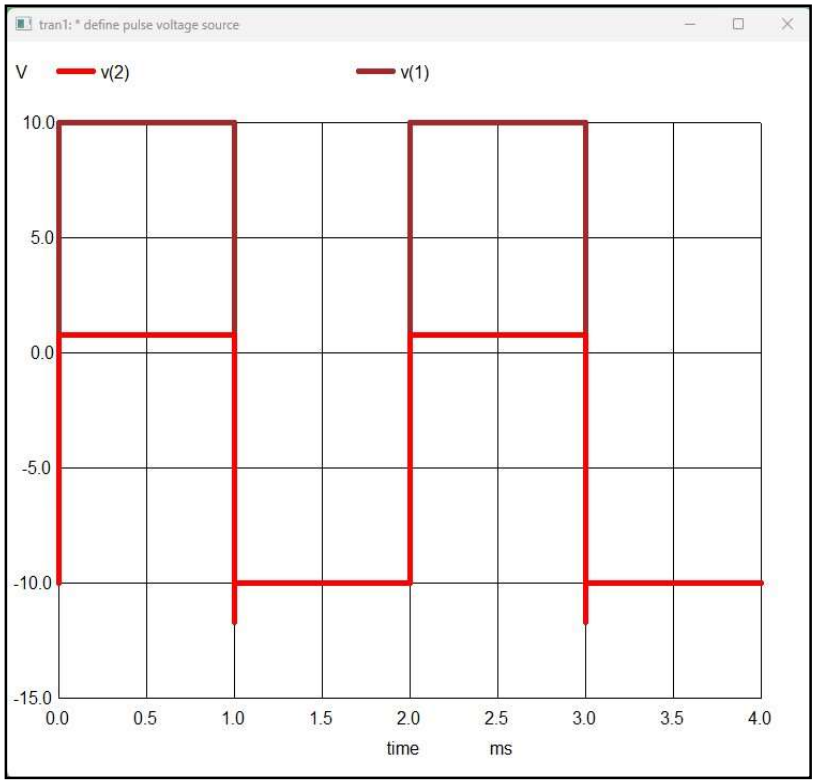


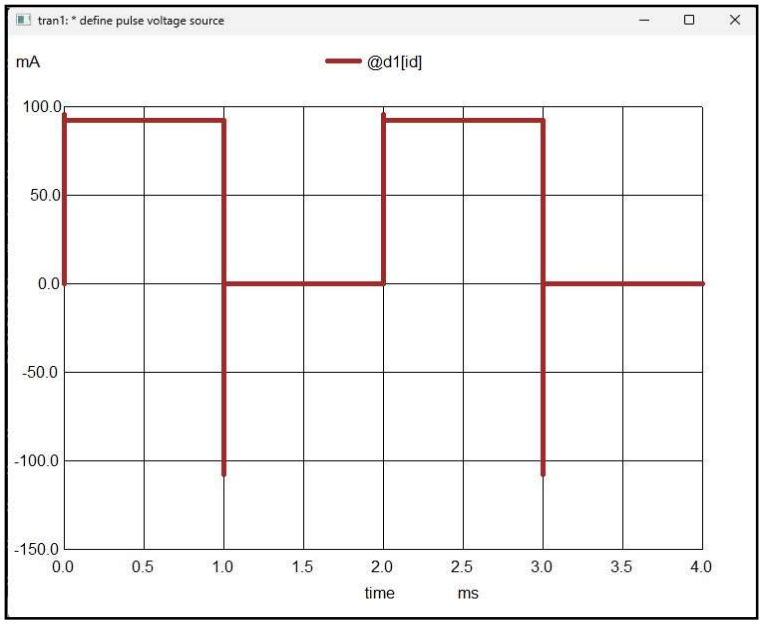
PROGRAM:

```
* Program: Plot Pulse Response

* Define pulse voltage source
V1 1 0 pulse(-10 10 0.1u 0.1u 0.1u 1m 2m)

* Define current-limiting series resistor
R1 1 2 0.1k

* Define diode
D1 2 0 myd

* Define diode model parameters
* IS: reverse saturation current, VJ: cut-in voltage, BV: breakdown voltage
.model myd D(
 IS = 100p
 + N = 1.45
 + RS = 0
 + TT = 4.3u
 + CJ0 = 40p
 + VJ = 0.7
 + M = 0.33
 + EG = 1.11
 + XTI = 3
 + KF = 0
 + AF = 1
```

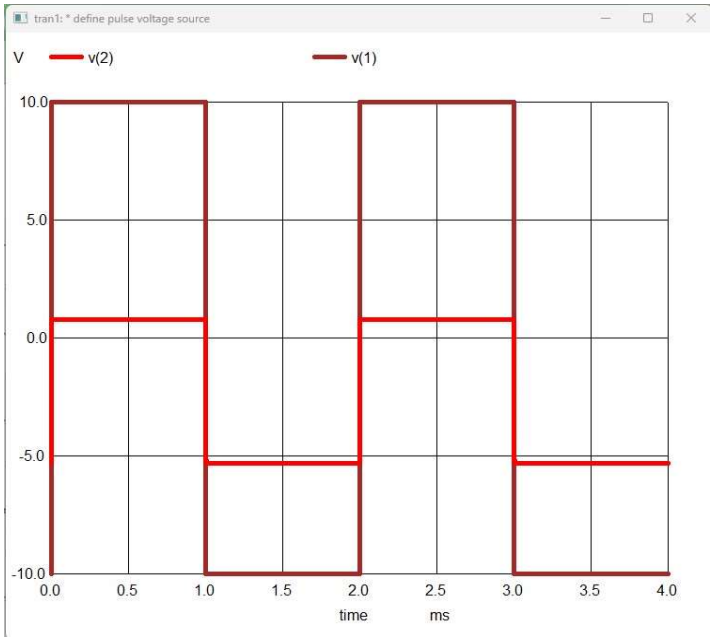
```
  + FC = 0.5
  + BV = 50
  + IBV = 10u
)

.control
  * Save diode current, voltage, and node voltages
  save @D1[id] @D1[vd] v(1) v(2)

  * Run transient analysis for pulse response
  tran 0.01u 4m

  * Set plot colors and line width
  set color0 = white
  set color1 = black
  set color2 = red
  set color3 = brown
  set xbrushwidth = 5

  * Plot input and output voltages
  plot @D1[id]
  plot v(1) v(2)
.endc

.END
```

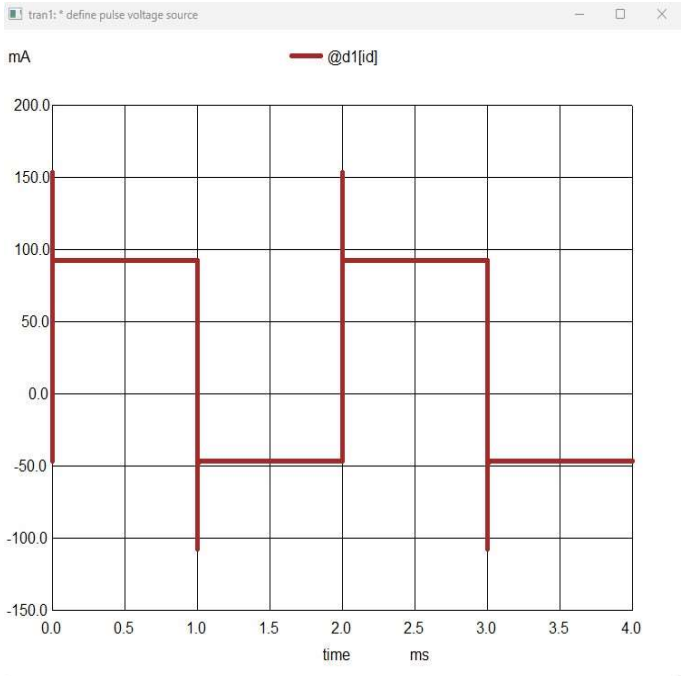
Wave Form :
BV=50V





BV = 5V





Observations on Diode Behavior with Varying Breakdown Voltage

- **Breakdown Voltage Set to 50V:**
  - The diode demonstrates typical behavior when subjected to a square wave input varying from -10V to +10V.
  - The output voltage closely follows the input, with the diode conducting during the positive half of the waveform and blocking during the negative half.

- When the diode is forward-biased (with input voltage greater than approximately 0.7V), the current flowing through it is positive and limited by the series resistor.
- During the negative half-cycle, the diode is reverse-biased, causing the current to approach zero, as the breakdown voltage is not reached.

Breakdown Voltage Changed to 5V:

- The diode continues to conduct during the positive half of the waveform; however, it begins to conduct in reverse when the input voltage hits the breakdown threshold of 5V.
- The output voltage behavior changes considerably; as the input turns negative, the diode conducts in reverse when the input voltage exceeds -5V. This leads to a larger negative current flowing through the diode.
- Consequently, there is a clamping effect on the output voltage, which stabilizes at approximately -5V during the negative cycle.

Comparison of Outputs:

- With a breakdown voltage of 50V, the output waveform remains well within the typical diode conduction limits, staying safely below the breakdown threshold during reverse bias.
- In contrast, with a breakdown voltage of 5V, the output gets clipped at -5V during negative cycles, creating a more complex waveform due to the diode's reverse conduction.

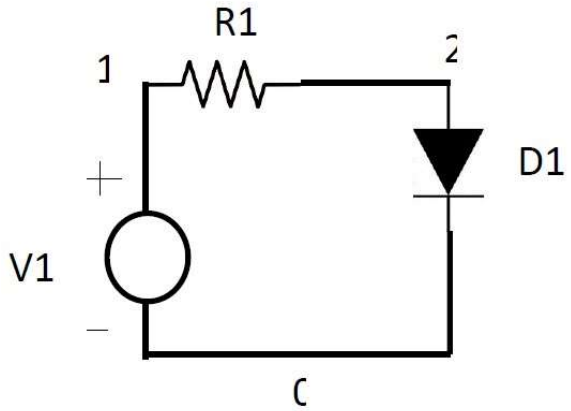
Behavior of Current Flowing Through the Diode:

- When the breakdown voltage is higher, the diode behaves as expected for standard rectification, conducting only during forward bias.
- Reducing the breakdown voltage leads to reverse conduction, which can result in potentially damaging effects if the circuit is not designed to handle such behavior.

Conclusion:

- The selection of breakdown voltage has a significant impact on the diode's behavior and output response within a circuit.
- Grasping these dynamics is essential for designing circuits that must perform reliably under various operational conditions.

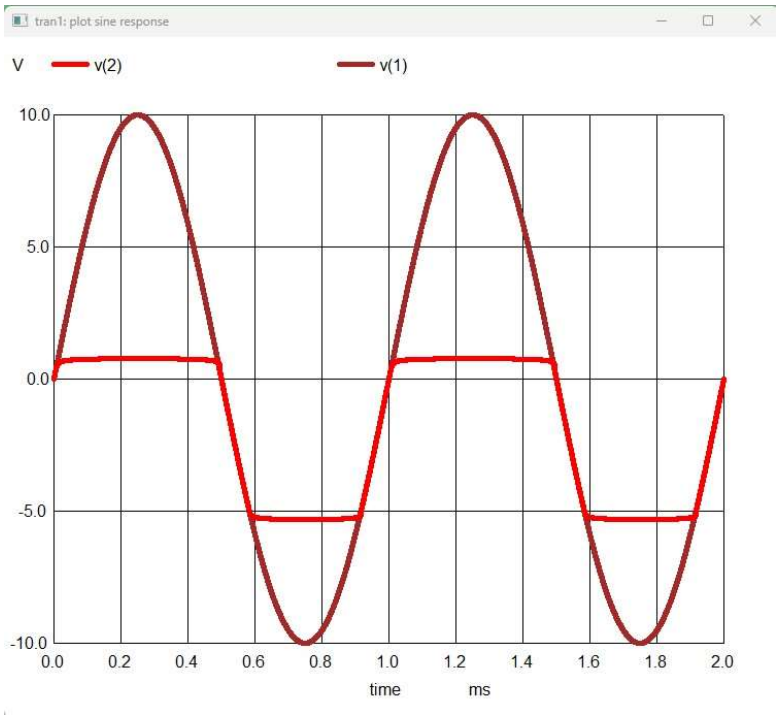
4. Apply a sine wave of Vmax=10V, Frequency=1KHz and observe the output.



PROGRAM:

```
* Plot Sine Response
* Define sinusoidal voltage source
V1 1 0 sin(0 10 1000)

* Define current limiting series resistor
R1 1 2 0.1k

* Define diode
D1 2 0 myd

* Define diode model parameters
* IS is reverse saturation current, VJ is cut in voltage, BV is breakdown voltage
.model myd D(IS = 100p
+ N = 1.45
+ RS = 0
+ TT = 4.3u
+ CJ0 = 40p
+ VJ = 0.6
+ M = 0.33
+ EG = 1.11
+ XTI = 3
+ KF = 0
+ AF = 1
+ FC = 0.5
+ BV = 5
+ IBV = 10u)

.control
* Run transient analysis
tran 0.1u 2m

* Set background color as white, grid lines black, plot red and width of the line = 10
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5

* Plot input and output voltages
plot v(1) v(2)
.endc

.END
```

Wave Form :



Observations on the Sinusoidal Response of the Diode Circuit

Circuit Configuration:
The circuit consists of a sinusoidal voltage source (V1) that provides an alternating current (AC) signal, a series current-limiting resistor (R1), and a diode (D1) characterized by specific model parameters. The voltage source generates a sinusoidal waveform with an amplitude of 10V and a frequency of 1 kHz.
Diode Model Parameters:

- The diode is modeled with the following specifications:
    - Reverse saturation current (IS) of 100 pA.
    - Cut-in voltage (VJ) of 0.6V, indicating that the diode begins to conduct significantly once the input voltage exceeds this threshold.
    - Breakdown voltage (BV) of 5V, meaning that when reverse-biased beyond -5V, the diode will enter breakdown mode, clamping the output voltage.

Analysis Procedure:
A transient analysis was conducted for a duration of 2 ms, with a step size of 0.1 µs, allowing for the observation of the circuit's response across multiple cycles of the input waveform.
Waveform Observations:

1. **Positive Half-Cycle Response:**

    - During the positive half-cycle of the sinusoidal input (ranging from 0V to +10V), the diode becomes forward-biased as the input exceeds the cut-in voltage of 0.6V.
    - The output voltage across the diode closely follows the input waveform, beginning at approximately 0.6V and rising to nearly +10V as the input voltage increases.
2. **Negative Half-Cycle Response:**
    - In the negative half-cycle (from 0V to -10V), the diode is reverse-biased.
    - As the input voltage approaches -5V, the diode enters reverse breakdown, causing the output voltage to be clamped near -5V. This demonstrates the diode's ability to limit the negative excursion of the waveform.
    - The output does not drop below -5V, showcasing the diode's clamping behavior.
3. **Output Characteristics:**
    - The output waveform exhibits a clipping effect during the negative half-cycle due to the breakdown voltage, resulting in a characteristic waveform where the negative peaks are flattened.
    - The positive peaks of the output closely follow the input but start to flatten out around the cut-in voltage threshold as the diode begins to conduct.

Summary of Observations:

- The diode effectively shapes the sinusoidal waveform, allowing for amplification during forward bias while limiting the voltage during reverse bias.
- The output voltage clearly demonstrates a clamping effect at -5V, illustrating the diode's behavior under varying bias conditions.
- This circuit configuration is particularly useful in applications where signal limiting is essential to protect downstream components from excessive negative voltages while still accommodating positive signal variations.