ECT201 SOLID STATE DEVICES

COURSE COMPLETION PROJECT

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MOS PROJECT

1. Draw the output characteristics (Ids vs Vds for different Vgs values) of a N type enhancement mode MOSFET. Draw its transfer characteristics (Ids vs Vgs for different Vds values).

PROGRAM :

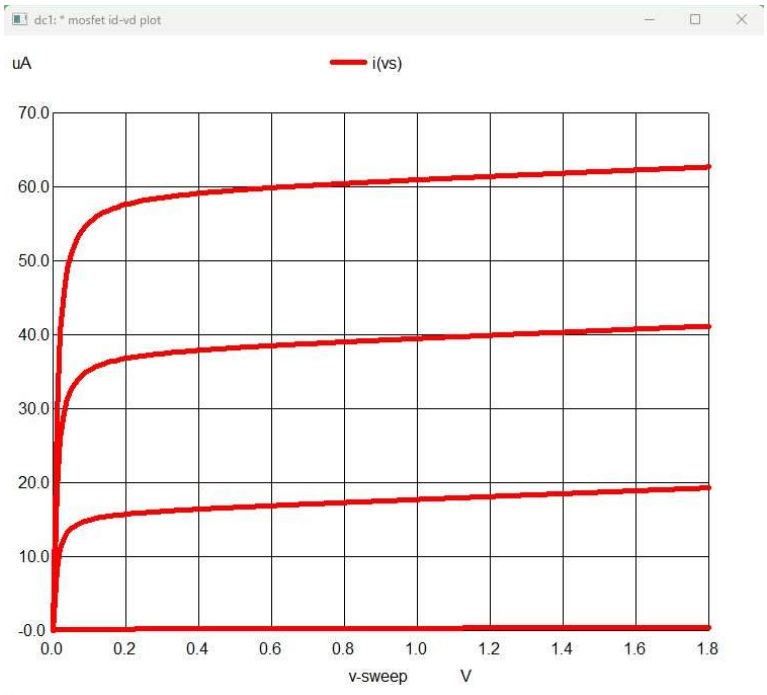
```
* MOSFET Id-Vd plot *
.include "mosmodel.txt"
* Drain voltage source
vd d 0 dc=1.8
* Gate voltage source
vg g 0 dc=0
* Source and substrate are grounded
vs s 0 dc=0
vb b 0 dc=0
* MOSFET model
m1 d g s b CMOSN W=10e-6 L=180e-9
* Sweep drain voltage and gate voltage
.dc vd 0.0 1.8 0.01 vg 0.4 1.8 0.4
.control
run
* Plot settings
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5
plot i(vs)
.endc
.end
```

```
* NMOS Id-Vg plot *
.include "mosmodel.txt"
* Drain voltage source
vd d 0 dc=0
* Gate voltage source
vg g 0 dc=0
* Source and substrate are grounded
vs s 0 dc=0
vb b 0 dc=0
```

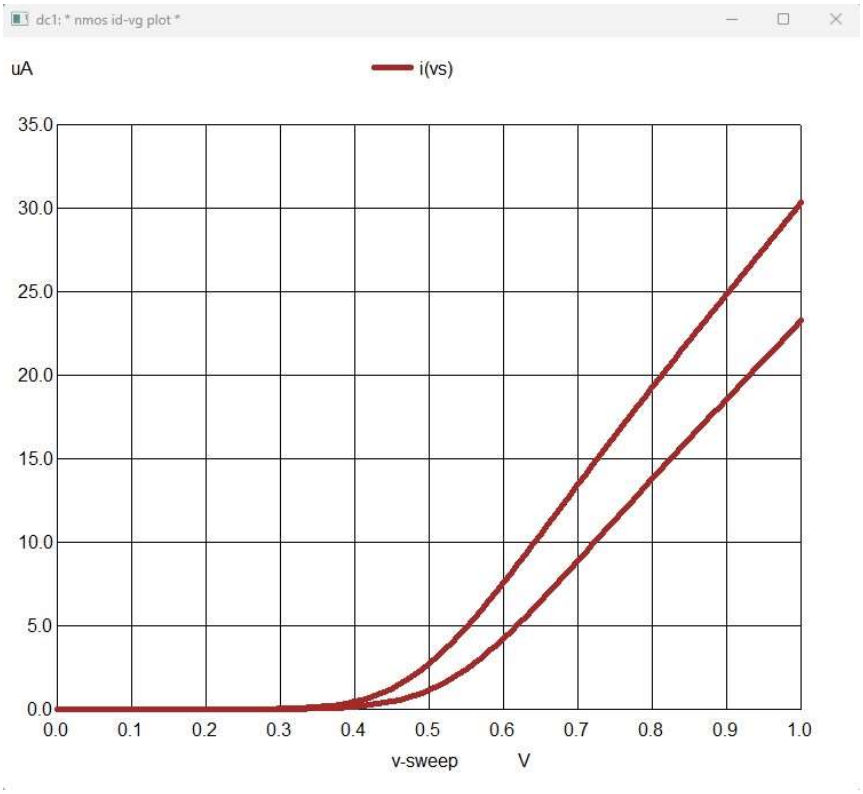
```
* MOSFET model
m1 d g s b CMOSN W=10e-6 L=180e-9
* Sweep gate voltage and drain voltage
.dc vg 0 1.0 0.01 vd 0.05 1.8 1.75
.control
run
* Plot settings
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5
plot i(vs)
.endc
.end
```

WAVE FORM :

Ids V/s Vds :



Ids V/s Vgs:



Output and Transfer Characteristics of an N-Type Enhancement Mode MOSFET

Output Characteristics (IDS vs. VDS for Different VGS Values)

1. **Description:**
    - The output characteristics graph shows how the drain current IDS changes with the drain-source voltage VDS for various gate-source voltages VGS.
    - When VGS is increased above the MOSFET's threshold voltage VTH IDS rises, reflecting the MOSFET turning on.
    - Each VGS value produces a separate curve, with IDS eventually saturating for higher VDS values.
2. **Key Points:**
    - The MOSFET remains off, with IDS=0, until VGS surpasses VTH.
    - After crossing the threshold, IDS initially rises linearly with VDS, entering the saturation region where it then levels off.

- Higher VGS values create distinct curves, showing greater IDS values as VGS increases.

Transfer Characteristics IDS vs. VGS for Different VDS Values)

1. **Description:**
    - The transfer characteristics graph illustrates how IDSI_{DS}IDS varies with VGSV_{GS}VGS for a set of constant VDSV_{DS}VDS values.
    - This plot shows the sensitivity of IDSI_{DS}IDS to changes in VGSV_{GS}VGS, especially as different VDSV_{DS}VDS levels are applied.
2. **Key Points:**
    - At low VGS, IDS remains close to zero until VGS exceeds VTH.
    - Once VGS goes beyond VTH, IDS increases sharply, signifying the device's transition from cutoff to saturation.
    - Beyond a certain point, IDS plateaus, indicating that the MOSFET has reached saturation.

Summary of Results:

- **Output Characteristics:**
    - Each curve shows that as VGS rises, the peak IDS also increases, with saturation occurring at progressively higher VDS levels for each VGS value**.**
- **Transfer Characteristics:**
    - The graph indicates a sharp increase in IDS as VGS rises above VTH, with the curves' shapes varying slightly based on the VDS applied**.**

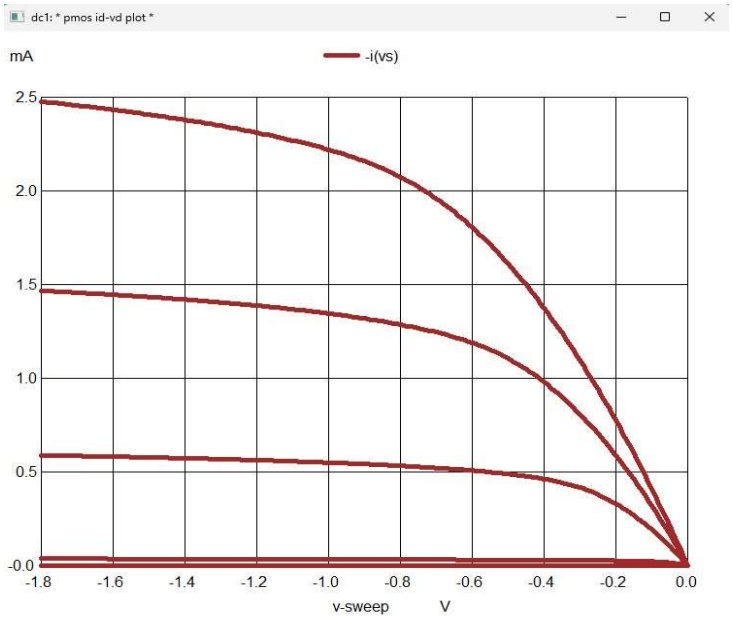
2.Draw the output characteristics (Ids vs Vds for different Vgs values) of a P type enhancement mode MOSFET. Draw its transfer characteristics. (Ids vs Vgs for different Vds values).

PROGRAM :

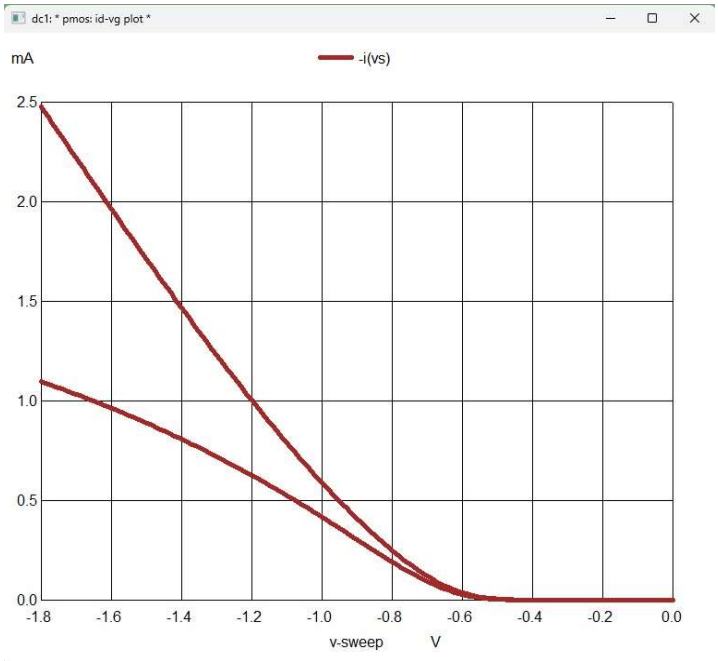
```
* PMOS Id-Vd plot *
* include the mosmodel.txt in the same folder
```

```
 .include "mosmodel.txt"
* drain voltage source
vd d 0 dc=0
* gate voltage source  vg g 0 dc=0
* source and substrate are grounded  vs s 0 dc=0  vb b 0 dc=0
* p mosfet model name is same as that given in the model file  m1 d g s b CMOSP
   W=10e-6 L=180e-9
* run drain voltage first and then sweep gate voltage to get the family of curves
 .dc vd -1.8 0.0 0.01 vg -1.8 -0.0 0.4
 .control
run
 *set background color as white, grid lines black, plot red and width of the
line=10  set color0=white  set color1=black
 set color2=red
set color2=brown
set xbrushwidth=5
plot -i(vs)
 .endc
 .end

* pmos: Id-Vg plot *
* include the mosmodel.txt in the same folder
 .include "mosmodel.txt"
* drain voltage source
vd d 0 dc=0

* gate voltage source  vg g 0 dc=0
* source and substrate are grounded  vs s 0 dc=0  vb b 0 dc=0
* p mosfet model name is same as that given in the model file  m1 d g s b CMOSP
   W=10e-6 L=180e-9
* run gate voltage first and then sweep drain voltage to get the family of curves
 .dc vg -1.8 0 0.01 vd -1.8 -0.05 1.5
 .control
run
 *set background color as white, grid lines black, plot red and width of the
line=10  set color0=white  set color1=black  set color2=red  set color2=brown
set xbrushwidth=5  plot -i(vs)
 .endc
 .end
```

WAVE FORM: (Id V/S Vd):



Id v/s Vgs :



Output and Transfer Characteristics of a P-Type Enhancement Mode MOSFET

1. **Description:**
    - The output characteristics graph shows the drain current Ids plotted against the drain-source voltage Vds for different gate-source voltages Vgs in a P-type enhancement mode MOSFET.
    - As Vgs becomes more negative, Ids increases, indicating the MOSFET turning on.
2. **Key Points:**
    - The MOSFET remains off, with Ids at 0, until Vgs falls below the threshold voltage (a negative threshold).
    - As Vgs is made more negative, Ids starts increasing, showing that the device is active.
    - Each Vgs value creates a distinct output curve, with higher Ids values observed as Vgs becomes more negative.

Transfer Characteristics (Ids vs. Vgs for Different Vds Values)

1. **Description:**
    - The transfer characteristics graph shows how Ids varies with gate-source voltage Vgs when different fixed values of Vds are applied.
    - This plot highlights how Ids changes with Vgs for a set Vds value.
2. **Key Points:**
    - At less negative Vgs, Ids is close to zero until Vgs surpasses the negative threshold.
    - As Vgs becomes more negative, Ids rises rapidly, marking the transition of the P-MOSFET from cutoff to saturation.
    - Eventually, Ids reaches a steady maximum, illustrating the MOSFET's saturation.

Summary of Results:

- **Output Characteristics:**

- The graph shows that as Vgs becomes more negative, Ids increases, with each curve indicating a specific Vgs value.

- **Transfer Characteristics:**
    - The plot reveals a rapid rise in Ids as Vgs becomes more negative, with curve shapes depending on the Vds levels applied.

3.Create an CMOS inverter using n-type and p-type enhancement MOSFETs and show that for a pulse input the circuit behaves like an inverter (NOT gate).

PROGRAM:

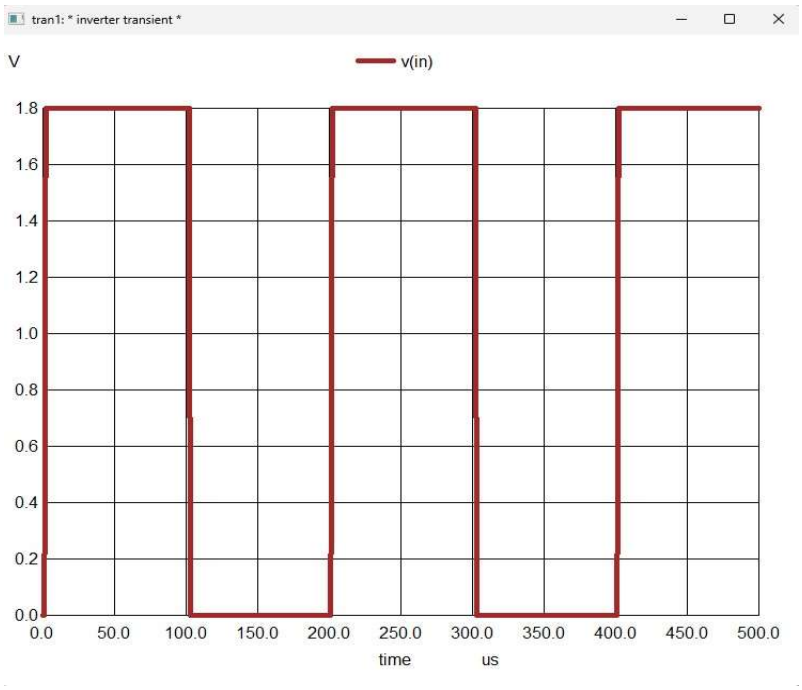
```
* Inverter Transient *
.include "mosmodel.txt"
* Supply voltage
v1 vdd 0 dc=1.8
* Pulse input source
v2 in 0 pulse 0 1.8 1u 1u 1u 100u 200u
* CMOS inverter (N-MOSFET and P-MOSFET)
mn out in 0 0 CMOSN W=1u L=180n
mp out in vdd vdd CMOSP W=2u L=180n
* Transient analysis for 500µs to observe at least two pulses
.tran 10n 500u
.control
run
* Plot settings
set color0=white
set color1=black
set color2=red
set color2=brown
set xbrushwidth=5
plot v(in)
```

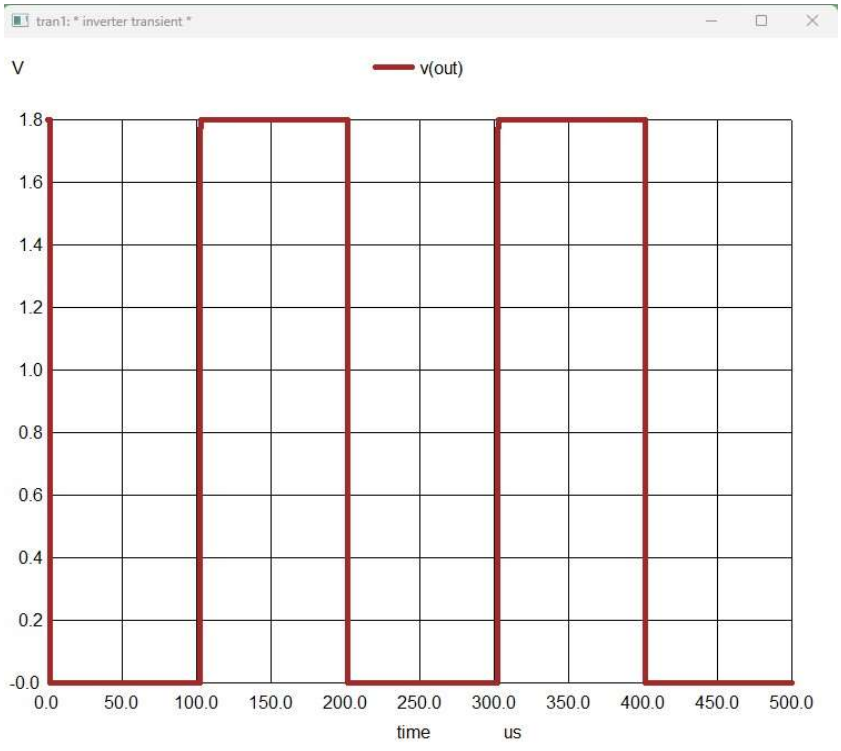
plot v(out)

.endc

.end

WAVE FORM:





CMOS Inverter Simulation

Objective:

To design a CMOS inverter using complementary n-type and p-type enhancement MOSFETs and verify its operation as an inverter (NOT gate) through pulse input testing.

Circuit Description:

- The inverter is constructed using a combination of one n-type MOSFET (MN) and one p-type MOSFET (MP), configured to produce an inverted output.
- A pulse signal is applied to the input, and the resulting output is monitored to verify the inverter's functionality.

Simulation Program:

1. **Power Supply:**
    - A DC supply voltage (Vdd) of 1.8V is applied.
2. **Input Source:**

- A pulse voltage source (V2) is defined with a range of 0V to 1.8V, pulse width of 1µs, and a period of 200µs.

3. **MOSFET Definitions:**
   - **N-Type MOSFET (MN)** : Connected to pull the output down to ground. ○ **P-Type MOSFET (MP)** : Connected to pull the output up to Vdd.

4. **Transient Analysis:**
   - The transient analysis is set to run for 500 µs with a time interval of 10 ns, allowing for observation of at least two pulse cycles in the output response.

Key Simulation Details:

- **Input Pulse Behavior:** The input toggles between 0V and 1.8V, mimicking a digital signal.
- **Expected Output Behavior:** The output should be inversely related to the input: when the input voltage is high (1.8V), the output should be low (0V), and vice versa.

Expected Results:

- **Output Voltage Behavior:** The output voltage (v(out)) should exhibit an inverted response to the input voltage (v(in)).
- **Inversion Confirmation:** The output should drop to low when the input is high, and rise to high when the input is low, confirming proper inverter action.

Visual Output:

- The simulation will display the input and output voltage waveforms over time, visually verifying the inverter's correct operation.

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