Department of Computer Science and Engineering
Monsoon Semester – 2024
CS2092E: Hardware Laboratory

Assignment – 1

This assignment focuses on implementing hardware components using Verilog HDL and acting as a prerequisite for the hardware lab

Design and implement the following logic functions using Verilog with behavioural modelling:

1) An 8-bit adder with sum and carry as output
2) An 8-bit subtractor with a difference and borrow as output
3) An 8-bit ALU that can perform addition, subtraction, bitwise XOR, and left shift operation
4) An 8-bit D latch with enable an active low reset

Subsequently, simulate and verify all the given logic functions using **ModelSim integrated with Intel Quartus software**. You are supposed to write the test bench with all the cases for every design.

Naming Conventions for Submission

- You should create two files for each question: one for the source code (the hardware implementation) and the other for the testbench
- The source code and testbench must be named
  <ROLLNO>_<FIRSTNAME>_<QNUBMER>.v and
  <ROLLNO>_<FIRSTNAME>_<QNUMBER>_tb.v, respectively.
  (Example: BxxyyyyCS_LAXMAN_1.v and BxxyyyyCS_LAXMAN_1_tb.v)
- Submit a single zip file containing all the files. The name of this file should be <ROLLNO>_<FIRSTNAME>.zip (Example BxxyyyyCS_LAXMAN.zip)

Policies for Submission and Evaluation

- You must submit your assignment on the EduServer course page on or before the submission deadline: August 08, 2024, 23:59 hrs
- During the evaluation, failure to execute programs may lead to zero marks for the evaluation
- Detection of any malpractice related to the lab course can lead to an ‘F’ grade in the course
- If any candidate does not submit the assignment, they are not eligible for the corresponding evaluation
- The assignment zero is mandatory and carries the marks

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