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Rachit Jain

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Digital System.

GYAN GANGA COLLEGE OF TECHNOLOGY JABALPUR

Digital System Lab Manual

Contents

GYAN GANGA COLLEGE OF TECHNOLOGY JABALPUR

Mission and Vision of the Institution

Vision of Institute:

Initially to seek autonomy and eventually grow the Institute into a renowned University by:

- Imparting the best technical and professional education to the students of the Institute.
- Developing all the Departments of the Institute as Centers of Excellence.
- Creating the most congenial and cordial environment of Teaching, Learning and Research in the Institute.
- Conceiving world - class Education, Ethics and Employability for students in global perspective.

Mission of Institute

To explore and ensure the best environment to transform students into creative, knowledgeable, principled engineers and managers compatible with their abilities in ever-changing socio-economic and competitive scenario by:

- Imparting intensive teaching and training through latest technology
- Motivating the teachers for higher learning and innovative research activities with social services.
- Generating maximum opportunities for placement of students in National, Multi-National companies and nurturing entrepreneurship quality.
- Producing highly intellectual citizens through technical education to constitute an elegant society and meeting social challenges.

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Mission and Vision of the Department

Vision

To be center of excellence in teaching-learning and employability in various fields of Electronics and Communication Engineering to produce globally competent, innovative and socially responsible citizen.

Mission

1. To offer high quality graduate and post graduate programs in Electronics and Communication with strong fundamental knowledges and to prepare students for professional career or higher studies
2. To discover and disseminate knowledge through learning, teaching, sharing, training, research, engagement and creative expression.
3. To foster spirit of innovation and creativity among students, faculty and staff, promote environment of growth, participation in conferences, technical and community services and lifelong learning for all.

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Program Education Objectives

I. The graduates will have ***strong fundamentals*** in mathematics, science and engineering so that they can meet industrial and global challenges and excel in the field of Electronics and Communication Engineering and also will be motivated to excel in professional career and higher education.

II. The graduates will have good **scientific and engineering breadth** to analyze, design and develop systems/ components, problem-solving skills and aptitude for innovation.

III. The graduates will exhibits ***leadership qualities*** with strong communication skills, competence to function effectively in multi disciplinary orientation teams, capability to assess and relate engineering issues to ethical, environmental and broader societal context

Program Objectives

1. An ability to demonstrate knowledge of mathematics, science and Engineering
2. An ability to identify, formulate, analyze and solve complex engineering problems using engineering sciences and research based knowledge.
3. An ability to design a system component or process to meet desired needs within realistic constrains such as economic, environmental, social, political, ethical, health and safety, manufacturability, and sustainability.
4. An ability to use the technique, resources, skills and modern engineering tools necessary for engineering practice.
5. An ability to function affectively as an individual and as a member or leader in culturally diverse teams and in multi disciplinary settings.
6. An ability to apply ethical principles and commit to professional ethics and responsibilities.
7. An ability to effectively communicate technical information in speech, presentation, and in writing.
8. Recognition of the need for, and an ability to engage in life-long learning.
9. An ability to apply engineering and management principles to one's own work, as a member and leader in a team to manage projects.

LABORATORY REGULATIONS AND SAFETY RULES

The following Regulations and Safety Rules must be observed in all concerned laboratory locations.

1. It is the duty of all concerned parties who use any electrical laboratory to take all reasonable steps to safeguard the HEALTH and SAFETY of themselves and all other users and visitors.
2. Make sure that all equipment is properly working before using them for laboratory exercises. Any defective equipment must be reported immediately to the Lab. Instructors or Lab. Technical Staff.
3. Students are allowed to use only the equipment provided in the experiment manual or equipment used for senior project laboratory.
4. Power supply terminals connected to any circuit are only energized with the presence of the Instructor or Lab. Staff.
5. Students should keep a safe distance from the circuit breakers, electric circuits or any moving parts during the experiment.
6. Avoid any part of your body to be connected to the energized circuit and ground.
7. Switch off the equipment and disconnect the power supplies from the circuit before leaving the laboratory.
8. Observe cleanliness and proper laboratory housekeeping of the equipment and other related accessories.
9. Wear proper clothes and safety gloves or goggles required in working areas that involves fabrications of printed circuit boards, chemicals process control system, antenna communication equipment and laser facility laboratories.
10. Double check your circuit connections specifically in handling electrical power machines, AC motors and generators before switching “ON” the power supply.
11. Make sure that the last connection to be made in your circuit is the power supply and first thing to be disconnected is also the power supply.
12. Equipment should not be removed, transferred to any location without permission from the laboratory staff.
13. Software installation in any computer laboratory is not allowed without the permission from the Laboratory Staff.
14. Computer games are strictly prohibited in the computer laboratory.
15. Students are not allowed to use any equipment without proper orientation and actual hands on equipment operation.

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INDEX

S NO.	NAME OF EXPERIMENT	DATE	GRADE/MARKS	SIGN	REMARK
1	To verify the truth table of EX-OR and EX-NOR gate using universal gate.				
2	To design and verify the operation of half adder and full adder.				
3	To verify the truth table of half subtractor and full subtractor.				
4	To design and verify the decimal to BCD Encoder.				
5	To verify the operation of BCD to Decimal Decoder.				
6	To verify the operation of 4:1 Multiplexer.				
7	To verify the operation of 1:4 Demultiplexer.				
8	To design and verify the operation of Binary to gray code converter.				
9	To design and verify the truth table of SR flip-flop, JK flip-flop, T- flip-flop, D-flip-flop..				
10	To verify the operation of Serial in Serial out (SISO) shift register.				
11	To Verify different arithmetic and logical operations by using 4 bit ALU 74LS181 IC.				
DATA SHEET OF ALL IC USED IN MANUAL PAGE NO. 42- 56					

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EXPERIMENT NO: -1

AIM: - To verify the truth table of EX-OR and EX-NOR gate using universal gate.

APPRATUS REQUIRED: - Multisim .

THEORY: -

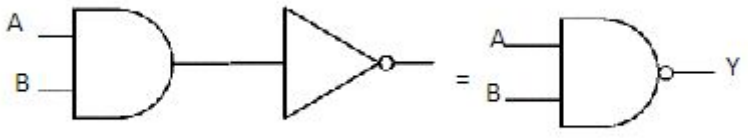
UNIVERSAL GATE: - NAND and NOR Gate are called Universal gates because both can be used to implement any gate like AND, OR, NOT, EX-OR and EX-NOR Gate or any combination of these basic gates.

NAND GATE: - NAND Gate is a contraction of the NOT-AND gates. It has two or more inputs and only one output. When all inputs are high the output is low. If any one or both the inputs are low, then the output is high. The small circle or bubble represents the operation of inversion.

$$Y = \overline{AB}$$

TRUTH TABLE: -

Inputs		Output
A	**B**	**$Y = \overline{AB}$**
0	**0**	**1**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

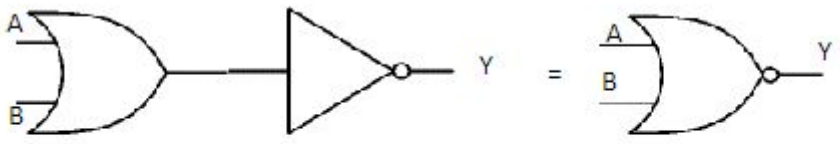


NOR GATE: - NOR Gate is a contraction of NOT-OR gates. It has two or more inputs and only one output. The output is high only when all the inputs are low. If any one or both the inputs are high, then the output is low. The small circle or bubble represents the operation of inversion. Output is

$$Y = \overline{A + B}$$

TRUTH TABLE: -

Inputs		Output
A	**B**	**Y= $\overline{A+B}$**
0	**0**	**1**
0	**1**	**0**
1	**0**	**0**
1	**1**	**0**



Implementation of XOR and XNOR Gate using Universal gate:

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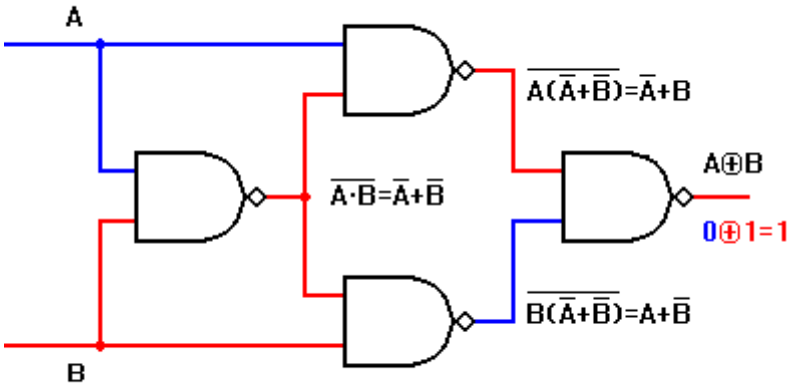
TRUTH TABLE OF EX-OR GATE: -

Inputs		Output
A	**B**	**Y**
0	**0**	**0**
0	**1**	**1**
1	**0**	**1**
1	**1**	**0**

Circuit Diagram: -



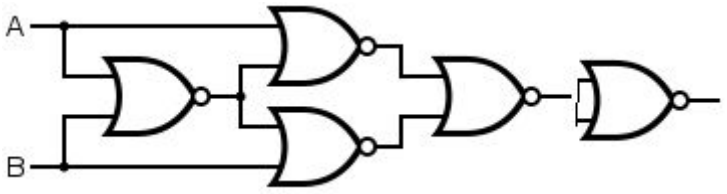


Fig: - Realisation of EX-OR Gate Using NAND and NOR Gate

TRUTH TABLE OF EX-NOR GATE: -

Inputs		Output
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	1

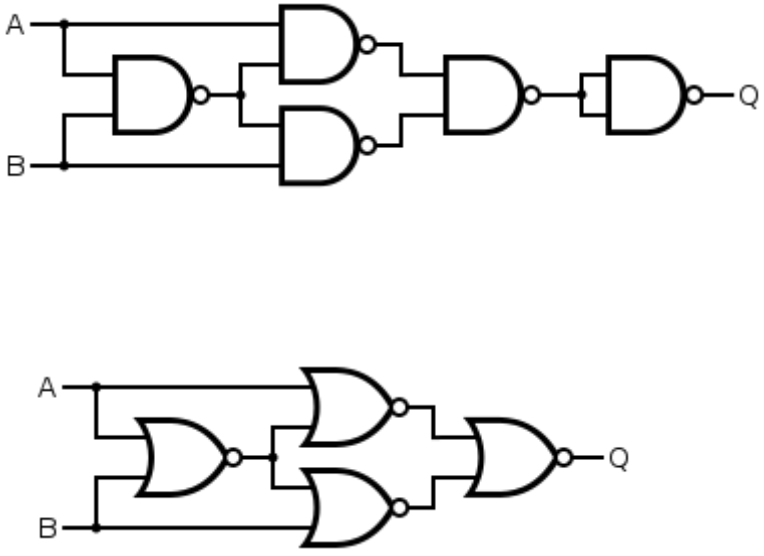


Fig: - Realisation of EX-NOR Gate Using NAND and NOR Gate.

PROCEDURE:

1. Connect the Input terminal of the circuit to the Input logic.
2. Connect the Output terminal to the logic Indicator.
3. Switch ON the power supply.
4. Verify the Truth Table.

RESULT: -Thus, we have verified the truth table of EX-OR and EX-NOR gate using Universal gates.

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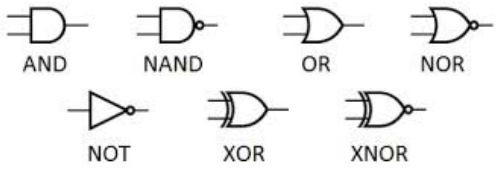
VIVA QUESTIONS

Q.1 What is a logic gate?

Logic gates are the basic building blocks of any digital system. It is an electronic circuit having one or more than one input and only one output. The relationship between the input and the output is based on a certain logic. Based on this, logic gates are named as AND gate, OR gate, NOT gate etc.

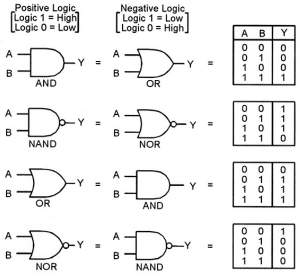
Q.2 Draw symbol of OR, NOT, AND , NAND NOR and EX-OR gate?



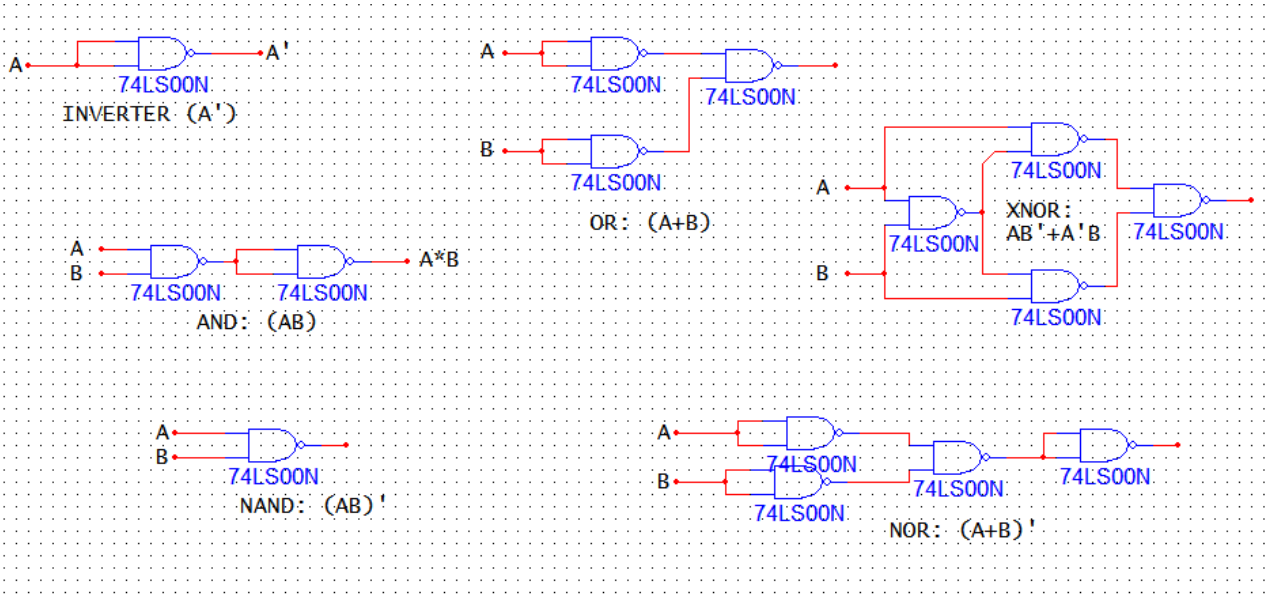
Q.3 What are the Universal gates?

A universal gate is a gate which can implement any Boolean function without need to use any other gate type. The NAND and NOR gates are universal gates. In practice, this is advantageous since NAND and NOR gates are economical and easier to fabricate and are the basic gates used in all IC digital logic families.

Q.4 Write truth table for 2 i/p OR, NOR, AND, and NAND gate?



Q.5 Implement all the logic gates using Universal gate



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EXPERIMENT NO.- 2

AIM: - To design and verify the operation of half adder and full adder.

APPRATUS REQUIRED: - Multisim .

THEORY: -

HALF ADDER: - It is combinational circuits that perform addition of two bits. This circuit has two inputs A and B (augend and added) and two outputs- Sum (S) and Carry (C).The sum is a 1 when A and B are different and carry is a 1when A and B are 1.The truth table for a half adder can be constructed using the addition table for binary
numbers,

INPUTS		OUTPUTS	
		Carry	Sum
A	B	C	S
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

Fig: - (a) Functional diagram of Half Adder **(b) Truth Table**.

From the truth table, we can write logical expression for S and C outputs as

Implementation of Half Adder: - Half Adder the sum is implemented using XOR gate while carry is implemented using AND gate.

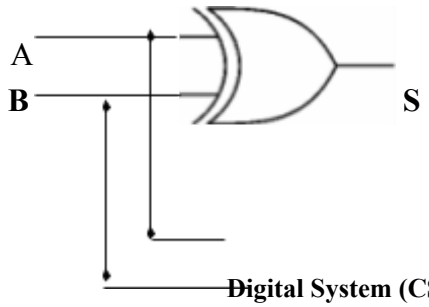
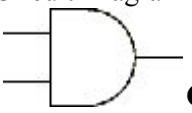


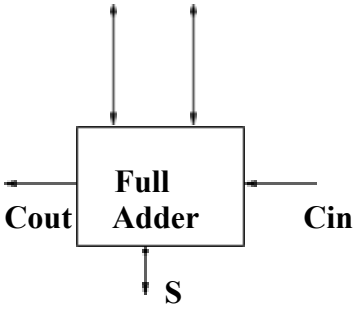
Fig:(c)Logic Circuit Diagram of Implementation of Half Adder



FULL ADDER: - half adder can only add two inputs and has no provision to add carry coming from the lower order bits when multiple additions is performed. For this purpose a third input terminal is added and this circuit is used to add augend, addend and carry generated from previous addition. The full adder is a combinational circuit that performs sum of three inputs bits. This circuit has three inputs and two outputs. Two of the inputs, denoted by **A** and **B,** represent the two bits to be added. The third inputs **Cin** represent the carry from the previous lower significant position. The two **outputs** are denoted by the symbols **S** for the **sum** and **Cout** for **carry.**

B A

Inputs			**Outputs**	
A	**B**	**Cin**	**Cout**	**S**
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1



(d)

(e)

Fig: - (d) Functional diagram of Full Adder **(e) Truth Table**

From the truth table, we can write logical expression for S and C outputs as

$$S = \overline{A}\,\overline{B}Cin + ABCin + \overline{A}B\overline{Cin} + A\overline{B}\,\overline{Cin}$$

S=A *EXOR* B *EXOR* Cin

$$S=Cin(\overline{A}\,\overline{B}+AB)+\overline{Cin}(\overline{A}B+A\overline{B})$$

$$Cout= \overline{A}BCin + A\overline{B}Cin + AB\overline{Cin} + ABCin$$

Cout = AB + ACin + BCin

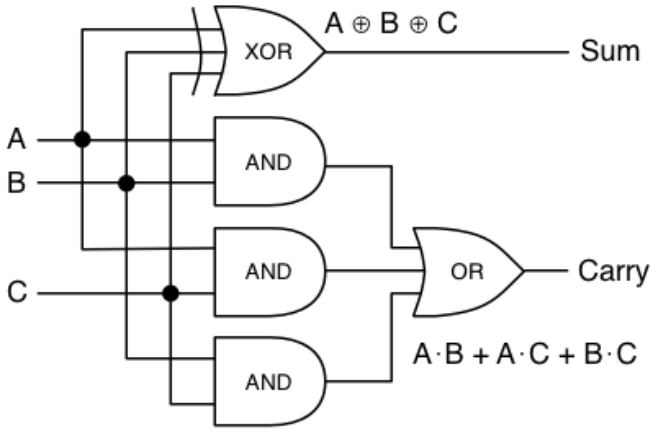


Fig:- (f) Logic Circuit Diagram of Full ADDER.

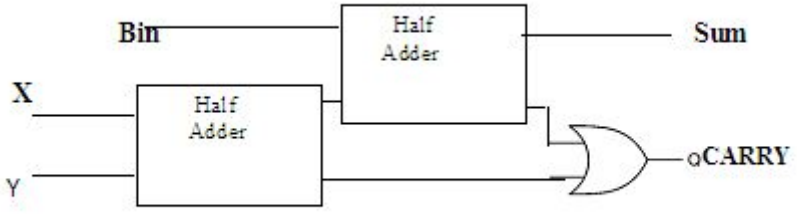


Fig: - (g) Full Adder using Half Adder.

PROCEDURE:-

1. Connect the Input terminal of the circuit to the Input logic.
5. Connect the Output terminal to the logic Indicator.
6. Switch ON the power supply.
7. Verify the Truth Table.
8.

RESULT:- Thus ,we have verified the truth table of Half and Full Adder.

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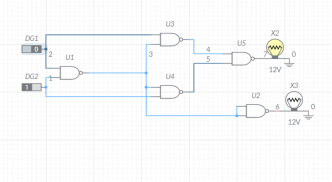
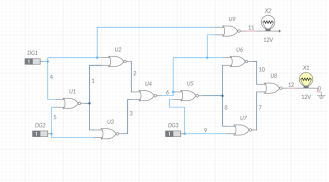
VIVA QUESTIONS

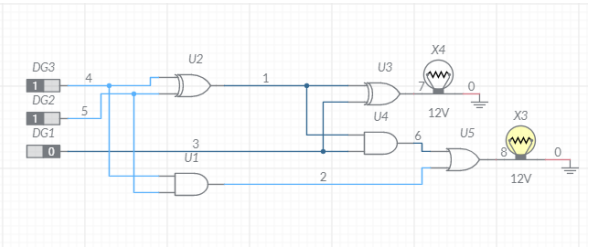
Q.1 Draw circuit diagram of Half Adder using NAND gate ?



Q.2 Draw circuit diagram of Full Adder using NOR gate?



Q.3 Draw Full Adder circuit by using Half Adder circuit and minimum no. of logic gates?



Q.4 Write application of Half Adder?

1) The ALU (arithmetic logic circuitry) of a computer uses half adder to compute the binary addition operation on two bits.
2) Half adder is used to make full adder as a full adder requires 3 inputs, the third input being an input carry i.e. we will be able to cascade the carry bit from one adder to the other.
3) Ripple carry adder is possible to create a logical circuit using multiple full adders to add N-bit numbers. Each full adder inputs a C(in), which is the C(out) of the previous adder. This kind of adder is called RIPPLE CARRY ADDER, since each carry bit "ripples" to the next full adder. Note that the first full adder (and only the first) may be replaced by a half adder

Q.5 Write application of Full Adder?

Ripple carry adder, it adds n-bits at a time.
carryout Multiplication -the dedicated multiplication circuit uses it.
ALU- Arithmetic Logic Unit (one of the circuit is a full adder).
to generate memory addresses inside a computer and to make the Program Counter point to next instruction, the ALU makes use of this adder.
For graphics related applications, where there is a very much need of complex computations, the GPU uses optimized ALU which is made up of full adders, other circuits as well….

EXPERIMENT NO. -3

AIM: To verify the truth table of half subtractor and full subtractor.

APPRATUS REQUIRED: - Multisim .

THEORY: -

Half Subtractor: - The half subtractor is a combinational circuit, which is used to perform subtraction of two bits. It has two inputs, X (minuend) and Y (subtrahend) and two outputs D (difference) and Bout (borrow out). Half subtractor the difference output is 0 if X = Y and 1 if X ≠ Y, the borrow output Bout is 1 whenever X < Y. If X is less than Y, then subtraction is done by borrowing 1 from the next higher order bit.

TRUTH TABLE:-

Minuend X	Subtrahend Y	Difference D	Borrow B
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

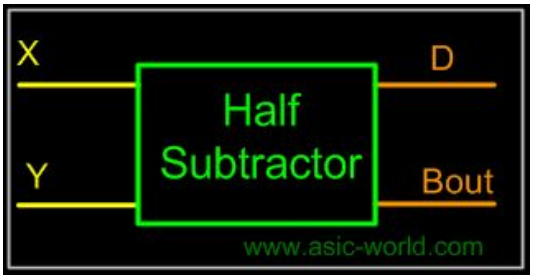


Fig: (a) Symbolic Block Diagram

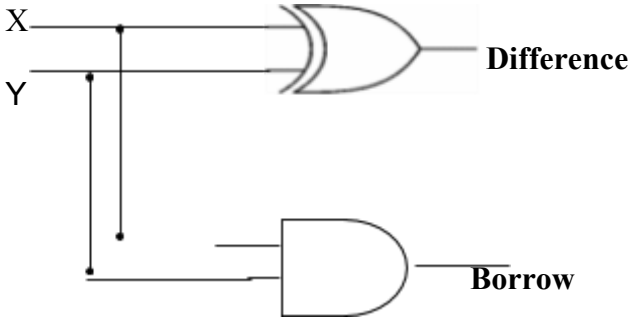


Fig:(b) Logic Diagram of Half Subtractor.

FULL SUBTRACTOR: - A full subtractor is a combinational circuit that performs subtraction involving three bits, namely minuend bit, subtrahend bit and the borrow from the previous stage. It has three inputs, X (minuend), Y (subtrahend) and Bin (borrow from previous stage), and two outputs D (difference) and Bout (borrow out).The full subtractor can be implemented using two half subtractor and an OR gate.

TRUTH TABLE:-

Inputs			**Outputs**	
Minuend X	**Subtrahend Y**	**Borrow in Bin**	**Difference D**	**Borrow out Bout**
0	**0**	**0**	**0**	**0**
0	**0**	**1**	**1**	**1**
0	**1**	**0**	**1**	**1**
0	**1**	**1**	**0**	**1**
1	**0**	**0**	**1**	**0**
1	**0**	**1**	**0**	**0**
1	**1**	**0**	**0**	**0**
1	**1**	**1**	**1**	**1**

The output function of Full subtractor is as follows

$$\mathbf{D} = \bar{X}\bar{Y}Bin + X\bar{Y}\bar{B}in + \bar{X}Y\bar{B}in + XYBin$$

Simplifying the above expression,

$$\mathbf{D} = (\bar{X}\bar{Y} + XY)\,Bin + (\bar{X}Y + X\bar{Y})\,\bar{B}in$$

$$\mathbf{D} = (\overline{X + Y})\,Bin + (X + Y)\,\overline{Bin}$$

$$\mathbf{D = X \ \textit{EXOR}\ Y \ \textit{EXOR}\ Bin}$$

$$\mathbf{Bout} = \underline{X}\underline{Y}Bin + \underline{X}Y\underline{Bin} + X\underline{Y}Bin + XYBin$$

$$\boxed{\mathbf{Bout} = \overline{X}Y + Y\,Bin + \overline{X}\,Bin}$$

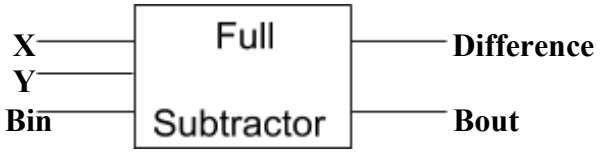


Fig: - (c) Symbolic Block Diagram

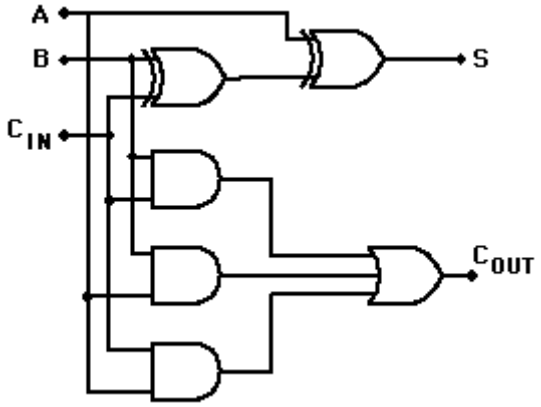
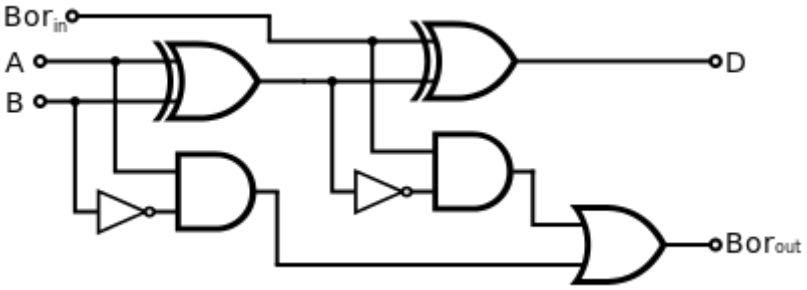


Fig:- (d) Logic Diagram of Full Subtractor.



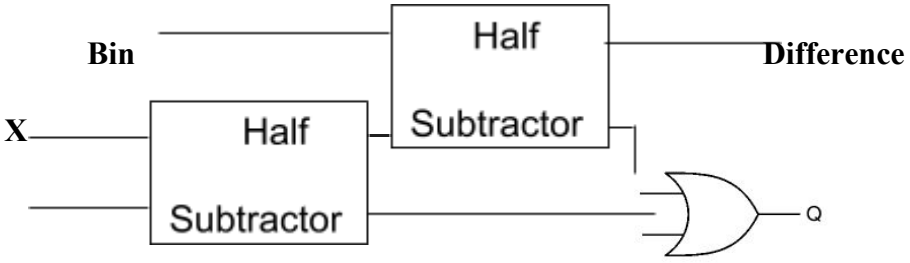


Fig: - (e) Full Subtractor is using Half Subtractor.

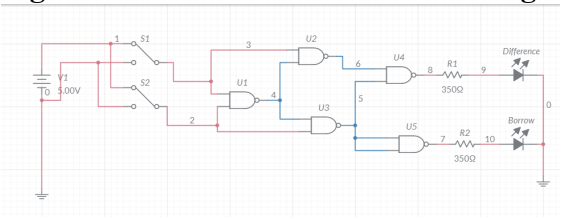
PROCEDURE:-

1 Connect the Input terminal of the circuit to the Input logic.
2 Connect the Output terminal to the logic Indicator.
3 Switch ON the power supply.
4 Verify the Truth Table.

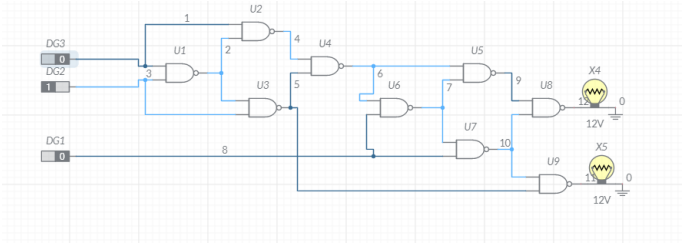
RESULT:- Thus ,we have verified the truth table of Half and Full Subtractor.

VIVA QUESTIONS

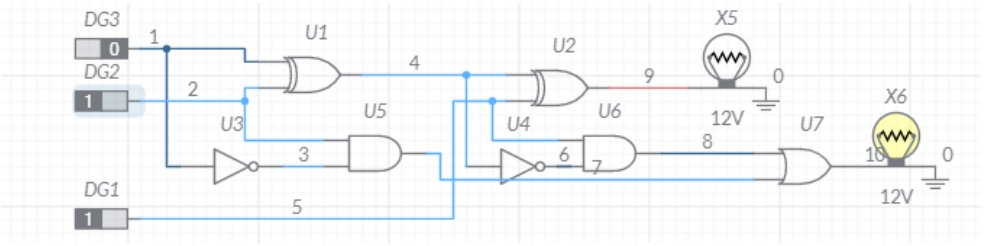
Q.1 Draw logic diagram of half subtractor circuit using NAND gate?



Q.2 Draw logic diagram of full subtractor circuit using NAND gate?



Q.3 Draw full subtractor circuit by using half subtractor circuit and minimum no. of logic gates?



Q.4 Write application of half subtractor?

Half subtractor is used to reduce the force of audio or radio signals
It can be used in amplifiers to reduce the sound distortion
Half subtractor is used in ALU of processor
It can be used to increase and decrease operators and also calculates the addresses
Half subtractor is used to subtract the least significant column numbers. For subtraction of multi-digit numbers, it can be used for the LSB.

Q.5 Write application of full subtractor?

To perform the Arithmetic operation of subtraction that is in the ALU units these subtractors are preferred.
The microcontrollers understand well the language of binary. Hence the operations performed by microcontrollers require the circuit of full subtractor to perform binary subtraction.
In gadgets like calculators and other electronics devices where it involves binary numbers, these circuits are preferred.
The systems based on Networking prefer this kind of circuitry.

EXPERIMENT NO.- 4

Aim:- To design and verify the decimal to BCD Encoder.

Apparatus Required:- Multisim .

THEORY:-
An encoder performs a function which is inverse to the function performed by a decoder.An encoder has 2n input lines and n output lines. The output lines generate the binary code for the 2 n input variables .In an encoder it is assumed that only one input line can be equal to 1 at any time.

Priority Encoder: -
In a simple encoder it is assumed that only one input line is equal to 1 at any given time. If a situation arises whether more than one i/p is high then the encoder will not function properly. To tackle such a situation a priority encoder is used. These encoders establish an input priority to insure that only the highest priority input line is encoded. Thus if a priority is given to an input with a higher subscript number over the one with a lower subscript number. Then if both D2 and D5 at logic1 simultaneously, the output will be 101 because D5 has higher priority over D2. IC 74147 is a active low IC .Therefore when logic 0 is applied to any input that input will be active and corresponding output is obtained which is compliment of usual output.

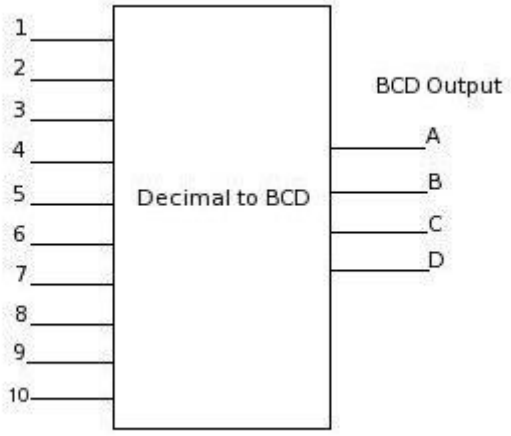


Fig block diagram of Decimal to BCD encoder

Truth Table :-

Input										Output			
D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	Y3	Y2	Y1	Y0
1	0	0	0	0	0	0	0	0	0	1	0	0	1
0	1	0	0	0	0	0	0	0	0	1	0	0	0
0	0	1	0	0	0	0	0	0	0	0	1	1	1
0	0	0	1	0	0	0	0	0	0	0	1	1	0
0	0	0	0	1	0	0	0	0	0	0	1	0	1
0	0	0	0	0	1	0	0	0	0	0	1	0	0
0	0	0	0	0	0	1	0	0	0	0	0	1	1

0	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**	**1**
0	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**0**

PROCEDURE:-

1.Connect the Input terminal of the circuit to the Input logic.
2.Connect the Output terminal to the logic Indicator.
3.Switch ON the power supply.
4.Verify the Truth Table.

RESULT:- Thus ,we have verified the operation of Decimal to BCD encoder.

VIVA QUESTIONS

Q.1 What do you understand by Encoder?

An encoder is a device or process that converts data from one format to another. In position sensing, an encoder is a device which can detect and convert mechanical motion to an analog or digital coded output signal. More specifically, it measures the position, while velocity, acceleration and direction can be derivated from the position in either linear or rotary movement.

Q.2 Explain about BCD number?

A binary-coded decimal (BCD) is a type of binary representation for decimal values where each digit is represented by a fixed number of binary bits, usually between four and eight.

The norm is four bits, which effectively represent decimal values 0 to 9. This writing format system is used because there is no limit to the size of a number. Four bits can simply be added as another decimal digit, versus real binary representation, which is limited to the usual powers of two, such as 16, 32 or 64 bits.

Q.3 Write application of Encoder?

Encoders are very common electronic circuits used in all digital systems.

Encoders are used to translate the decimal values to the binary in order to perform the binary functions such as addition, subtraction, multiplication, etc.

Other applications especially for Priority Encoders may include detecting interrupts in microprocessor applications.

Q.4 Draw a truth table of 3 bit Binary to Decimal converter?

Q.5 What is the advantage of BCD representation?

Binary codes are suitable for the computer applications.

Binary codes are suitable for the digital communications.

Binary codes make the analysis and designing of digital circuits if we use the binary codes.

Since only 0 & 1 are being used, implementation becomes easy.

EXPERIMENT NO.- 5

Aim:- To verify the operation of BCD to Decimal Decoder.

Apparatus Required:- Multisim .

Theory:-

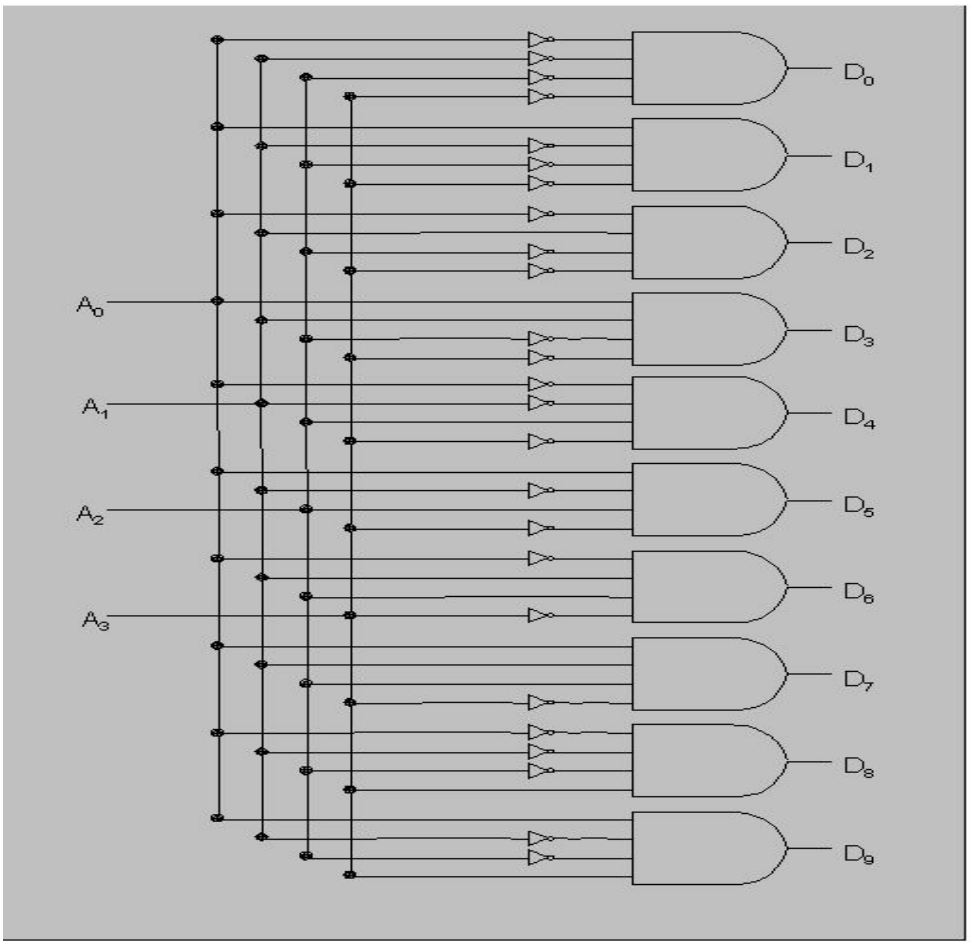
A decoder is a logic circuit that converts on n bit binary input code into 2" output lines such that each output line will be activated for only the possible combination of input in a decoder. The number of output is greater than the no. of input circuit capable of covering a code is called decoder. Decoder is a circuit similar to demultiplexer but without any data input most digital

system require the decoding of data. Decoding is necessary in application such as data multiplexing, digital displays, digital analog converter and memory addressing.

A decoder that takes a four-bit BCD as the input code and produces 10 outputs corresponding to the decimal digits is called a BCD to decimal decoder. Hence each output goes high when, its corresponding BCD code is applied at its input.

Decimal Digit	Binary Inputs				Logic Function
0	0	0	0	0	$\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$
1	0	0	0	1	$\overline{A_3}\,\overline{A_2}\,\overline{A_1}\,A_0$
2	0	0	1	0	$\overline{A_3}\,\overline{A_2}\,A_1\,\overline{A_0}$
3	0	0	1	1	$\overline{A_3}\,\overline{A_2}\,A_1A_0$
4	0	1	0	0	$\overline{A_3}\,A_2\,\overline{A_1}\,\overline{A_0}$
5	0	1	0	1	$\overline{A_3}\,A_2\,\overline{A_1}\,A_0$
6	0	1	1	0	$\overline{A_3}\,A_2A_1\,\overline{A_0}$
7	0	1	1	1	$\overline{A_3}\,A_2\,A_1\,A_0$
8	1	0	0	0	$A_3\,\overline{A_2}\,\overline{A_1}\,\overline{A_0}$
9	1	0	0	1	$A_3\,\overline{A_2}\,\overline{A_1}\,A_0$

Truth table of BCD to decimal decoder



Logic diagram of BCD to decimal decoder

PROCEDURE:-

1. Connecting the input terminal of the circuit to the input logic
2. Connect the output terminal to the logic indicator.
3. Switch ON the power supply
4. Verify the truth table.

RESULT:- Thus, we have verified the truth table of BCD to decimal decoder.

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VIVA QUESTIONS

Q.1 What do you understand by Decoder?

Decoder is a combinational circuit that has 'n' input lines and maximum of 2n output lines. One of these outputs will be active High based on the combination of inputs present, when the decoder is enabled. That means decoder detects a particular code. The outputs of the decoder are nothing but the min terms of 'n' input variables lines, when it is enabled.

Q.2 What is the difference between by Demultiplexer and Decoder?

Definition of Decoder and Demultiplexer– The key difference between a decoder and a Demultiplexer is that the former is a logic circuit that decrypts an encoded bit stream from one format into another, while the latter is a combination circuit that routes a single input line to multiple digital output lines.

Function of Decoder and a Demultiplexer – Decoder is the inverse function of an encoder, which is to translate coded digital input signals into equivalent coded output signals. Demultiplexer, on the other hand, does exactly the opposite of what a multiplexer does, which is to consolidate several data streams into a single stream of media or information.

Q.3 What is the difference between Encoder and Decoder?

Encoder: Is a device able to convert an ANALOG input (usually Audio and Video) form its original source to a digital data stream. In the case of digital video an Encoder is a device with analog inputs like RCA connectors and digitalize this video to a MP4 file or live stream.

A Decoder is a device that makes the oposite process, turns a DIGITAL data stream into a ANALOG output.

In the case of digital video, a Decoder is the Set top box you use to watch TV, receives a digital input from Satellite or Cable and decodes it into audio and video.

Q.4 Write application of decoder?

The Decoders were used in analog to digital conversion in analog decoders.

Used in electronic circuits to convert instructions into CPU control signals.

They mainly used in logical circuits, data transfer.

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EXPERIMENT NO.- 6

AIM: - To verify the operation of 4:1 Multiplexer.

APPRATUS REQUIRED: - Multisim .

THEORY: - A multiplexer is a circuit which has a number of inputs but only 1 output or we can say multiplexer is a circuit which transmits a large number of information signals(inputs) over a small number of signal lines(output).Digital multiplexer is a combinational logic circuit and its function is to select information in binary from one of many inputs and outputs the information along a single selected output. These circuits are especially useful when a complex logic circuit is to be shared by a number of input signals. The information to be outputted is selected by the address line. In case of 4:1 multiplexer, it has four input lines having a signals as I0,I1,I2 AND I3.For selecting one of the four input signals we require address which can be a two bit word. The address lines are designated as S1 and S0.For each combination of selection signals (S1 and S0) one of the inputs is outputted.

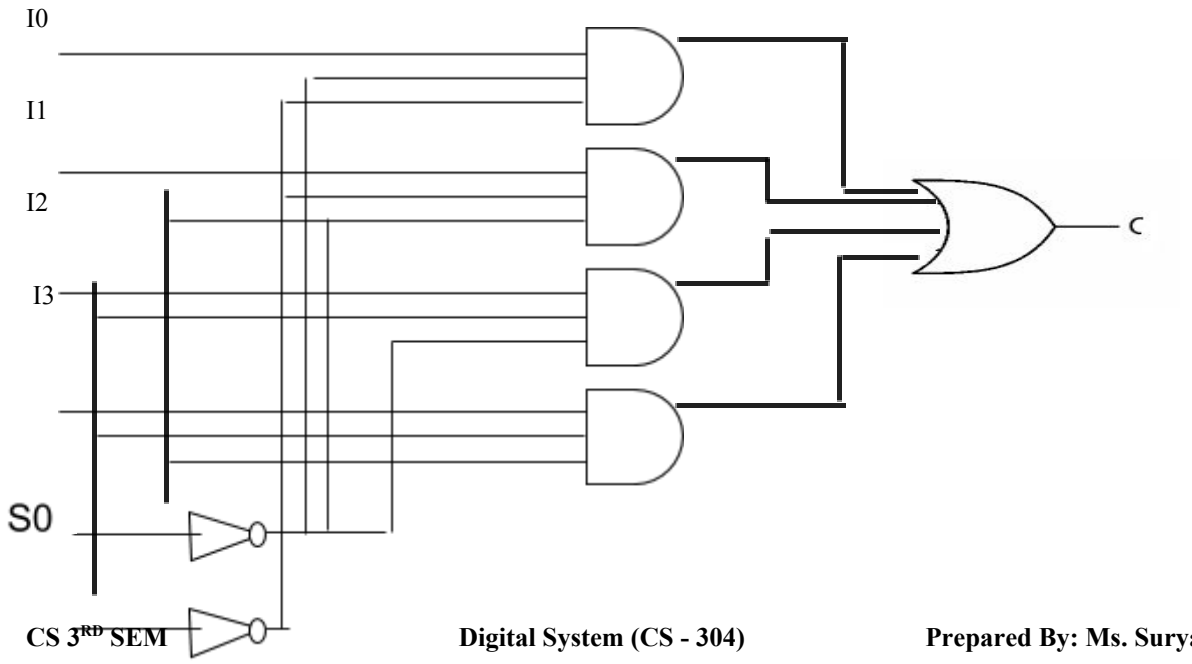
Truth Table:

S1	S0	Y
0	0	I0
0	1	I1
1	0	I2
1	1	I3

This truth table can be expressed by the following Boolean expression.

$Y = I0\bar{S1}\bar{S0}+I1\bar{S1}S0+I2S1\bar{S0}+I3S1S0$

I0, I1, I2 and I3 are Boolean variables and will have a value of 0 or 1.A 0 will mean that particular I is 0 or it is not at the output while a 1 will mean that a particular I appears at the output. Sometimes a multiplexer works as a data selector by working as a circuit which selects one of many inputs and transmits that information along a pre-selected line and that is why it is also called as data selector.



Logic Diagram of 4:1Multiplexer:

OCEDURE:-

S1

PROCEDURE –

1 Connect the Input terminal of the circuit to the Input logic.
2 Connect the Output terminal to the logic Indicator.
3 Switch ON the power supply.
4 Verify the Truth Table.

RESULT:- Thus ,we have verified the operation of 4:1 multiplexer.

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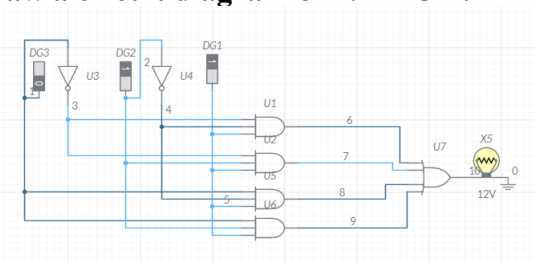
VIVA QUESTIONS

Q.1 Explain the Multiplexer?

Multiplexer is a combinational circuit that has maximum of 2n data inputs, 'n' selection lines and single output line. One of these data inputs will be connected to the output based on the values of selection lines. Since there are 'n' selection lines, there will be 2n possible combinations of zeros and ones. So, each combination will select only one data input. Multiplexer is also called as Mux.

Q.2 Draw a circuit diagram of 4:1 MUX?



Q.3 What are the advantages and disadvantages of MUX?

Advantages:

1] It reduces ckt complexity and cost.

2] We can implement many combinations logic ckts using multiplexer.

3] It does not need K-maps and simplification.

4] On the advance level the ability of MUX to switch directed s/g can be extended to smter video. s/g, audio s/g, etc.

Disadvantages:

1] Added delays in switching ports.

2] Limitations on which ports can be used simultaneously.

3] Extra IO many require to control multiplexer.

4] Added delays in I/O signals propagating through the multiplexer.

Q.4 Write application of MUX?

Communication System

– A Multiplexer is used in communication systems, which has a transmission system and also a communication network. A Multiplexer is used to increase the efficiency of the communication system by allowing the transmission of data such as audio & video data from different channels via cables and single lines.

Computer Memory

– A Multiplexer is used in computer memory to keep up a vast amount of memory in the computers, and also to decrease the number of copper lines necessary to connect the memory to other parts of the computer.

Telephone Network

– A multiplexer is used in telephone networks to integrate the multiple audio signals on a single line of transmission.

Transmission from the Computer System of a Satellite:

A Multiplexer is used to transmit the data signals from the computer system of a satellite to the ground system by using a GSM communication.

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EXPERIMENT NO.- 7

AIM: - To verify the operation of 1:4 Demultiplexer

APPRATUS REQUIRED: - Multisim .

THEORY: - The word "Demultiplex"means one into many.Demultiplexing is the process of taking information from one input and transmitting the same over one of several outputs. A demultiplexer is a logic circuit that receives information on a single input and transmits the same over the same information over one of several (2^n)output lines. The circuit has one input signal m select signal and n output signals. The select inputs determine to which output the data input will be connected. As the serial data is changed to parallel data, i.e. the input caused to appear on one of the n output lines, the demultiplexer is also called a distributor or a serial to parallel converter.

A 1-to-4 demultiplexer which has a single input (D), four outputs (Y0 to Y3) and two select inputs (S1 and S0).The truth table of the 1-to-4 demultiplexer are as shown bellow:

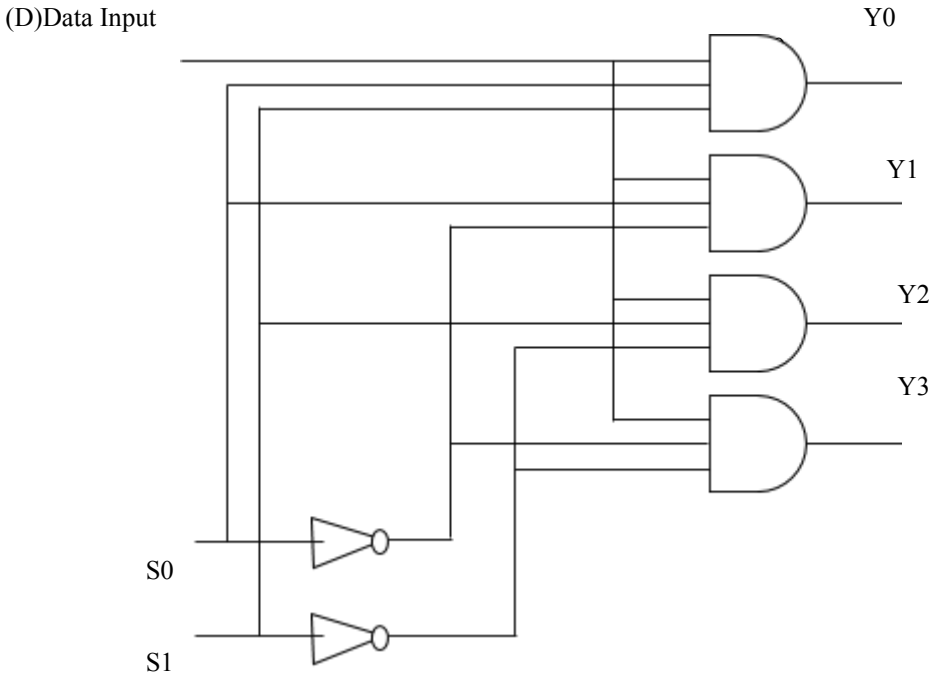
Truth Table:

Data Input	Select Inputs		Outputs			
D	S1	S0	Y3	Y2	Y1	Y0
D	0	0	0	0	0	D
D	0	1	0	0	D	0
D	1	0	0	D	0	0
D	1	1	D	0	0	0

From the truth table ,it is clear that the data input is connected to output Y0 when S1=0 and S0=0and the data input is connected to output Y1 when S1=0 and S0=1. Similarly the data input is connected to output Y2 when S1=1 and S0=0 and when S1=1 and S0=1, respectively.The expressions for outputs can be written as follows:

$$Y0 = \bar{S}1\bar{S}0D$$
$$Y1 = \bar{S}1S0D$$
$$Y2 = S1\bar{S}0D$$
$$Y3 = S1S0D$$

Here , the input data line is connected to all the AND gates. The two select lines S1S0 enable only one gate at a time and the data that appears on the input line passes through the selected gate to the associated output line.



Logic Diagram of 1:4 DeMultiplexer:

PROCEDURE:-

1. Connect the Input terminal of the circuit to the Input logic.
2. Connect the Output terminal to the logic Indicator.
3. Switch ON the power supply.
4. Verify the Truth Table.

RESULT:- Thus ,we have verified the operation of 1:4 Demultiplexer.

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VIVA QUESTIONS

Q.1 Explain about Demultiplexer?

A demultiplexer (or demux) is a device that takes a single input line and routes it to one of several digital output lines. A demultiplexer of 2n outputs has n select lines, which are used to select which output line to send the input. A demultiplexer is also called a data distributor.

Q.2 What is the difference between Multiplexer and Demultiplexer?

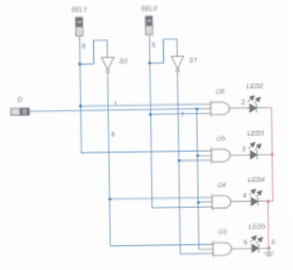
The major factor that differentiates multiplexer and demultiplexer is their ability to accept multiple input and single input respectively. The multiplexer also known as a MUX operates on several inputs but provide a single output. As against demultiplexer also known as DEMUX simply reverses the operation of MUX and operates on single input but transmits the data to multiple outputs.

Q.3 Write application of Demultiplexer?

Communication System – Multiplexer and Demultiplexer both are used in communication systems to carry out the process of data transmission. A De-multiplexer receives the output signals from the multiplexer; and, at the receiver end, it converts them back to the original form.

Arithmetic Logic Unit – The output of the arithmetic logic unit is fed as an input to the De-multiplexer, and the o/p of the demultiplexer is connected to a multiple registers. The output of the ALU can be stored in multiple registers.

Q.4 Draw a logic diagram of 1:4 Demultiplexer?



Q.5 What are the applications of Demultiplexer?

- To enable the different rows of memory chips depends on the address.
- To chose different banks of memory.
- To enable different functions unit in the system
- To select different IO devices fro data transfer
- Demux also used for synchronous data transmission systems
- Boolean function implementation
- Data acquisition systems
- Combinational circuit design
- Automatic test equipment systems
- Security monitoring systems

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EXPERIMENT NO.: - 8

AIM: - To design and verify the operation of Binary to gray code converter.

APPRATUS REQUIRED: - Multisim

THEORY: - In digital system can be expressed in various codes and it is quite often required to convert coded number to some another system. A circuit capable of converting a code is called Decoder. A decoder is a multi input multi output combinational circuit. The decoder that is converting a binary code into gray code is called Binary to Gray Code Converter. For converting a binary code into gray code, the most significant bit is noted. This MSB is added to the bit in the next position. The sum is recorded and carry if any generated is neglected. This procedure is repeated till the last bit of the binary number is noted. Let us consider that the equivalent of a binary number is B0 B1 B2 B3and the Gray code is G0 G1G2 G3.Each bit of gray code G0, G1, G2 OR G3 will be a function of B0, B1, B2 and B3.The truth table of Binary to Gray code Converter is as follows:

TRUTH TABLE:-

Decimal	Binary				Gray			
	B0	B1	B2	B3	G0	G1	G2	G3
0	0	0	0	0	0	0	0	0
1	0	0	0	1	0	0	0	1
2	0	0	1	0	0	0	1	1
3	0	0	1	1	0	0	1	0
4	0	1	0	0	0	1	1	0
5	0	1	0	1	0	1	1	1
6	0	1	1	0	0	1	0	1
7	0	1	1	1	0	1	0	0
8	1	0	0	0	1	1	0	0
9	1	0	0	1	1	1	0	1
10	1	0	1	0	1	1	1	1
11	1	0	1	1	1	1	1	0
12	1	1	0	0	1	0	1	0

13	**1 1 0 1**	**1 0 1 1**
14	**1 1 1 0**	**1 0 0 1**
15	**1 1 1 1**	**1 0 0 0**

The Boolean function for Binary to Gray code converter is as follows:

G0=B0

G1=B0B1+B0B1=B0 + B1

G2=B1B2+B1B2=B1 + B2

G3=B2B3+B2B3= B2+B3

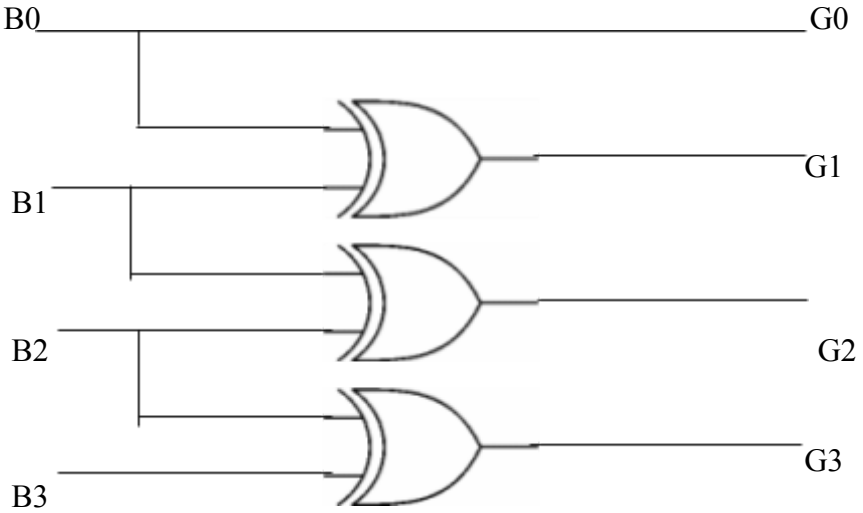

Fig:- Circuit Diagram of Binary to Gray code converter.

PROCEDURE:-

1.Connect the Input terminal of the circuit to the Input logic.
2.Connect the Output terminal to the logic Indicator.
3.Switch ON the power supply.
4.Verify the Truth Table.

RESULT:- Thus ,we have verified the operation of Binary to Gray code Converter.

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VIVA QUESTIONS

Q.1 What is a code converter?

The code converters are used to convert the information in to the code which we want. These are basically encoders and decoders which converts the data in to an encoded form. The below explains some digital codes used in digital electronics.

Q.2 What is the gray code?

Gray Code system is a binary number system in which every successive pair of numbers differs in only one bit. It is used in applications in which the normal sequence of binary numbers generated by the hardware may produce an error or ambiguity during the transition from one number to the next.

Q.3 How the binary code convert in to gray code ?

The MSB (Most Significant Bit) of the gray code will be exactly equal to the first bit of the given binary number.
The second bit of the code will be exclusive-or (XOR) of the first and second bit of the given binary number, i.e if both the bits are same the result will be 0 and if they are different the result will be 1.
The third bit of gray code will be equal to the exclusive-or (XOR) of the second and third bit of the given binary number.
Thus the binary to gray code conversion goes on.

Q.4 Write name of any 5 code converters?

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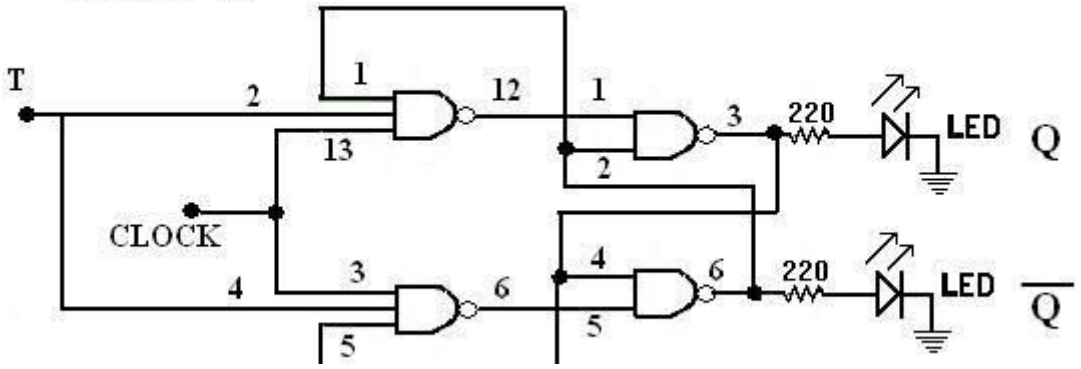
EXPERIMENTS NO:-9

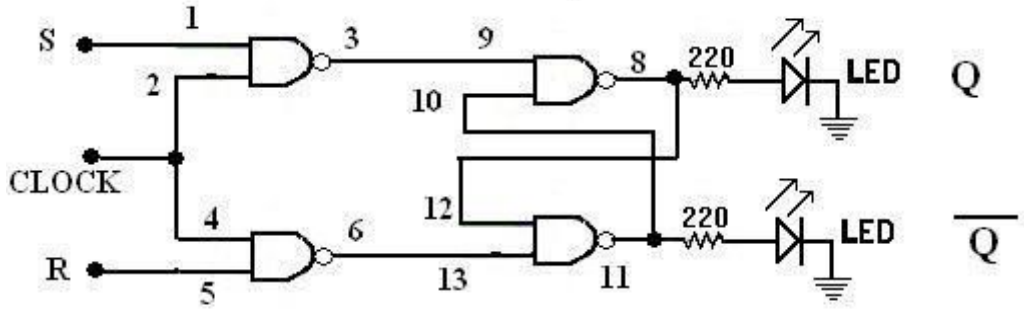
Aim: To design and verify the truth table of SR flip-flop, JK flip-flop, T- flip-flop, D-flip-flop.

Apparatus: Multisim

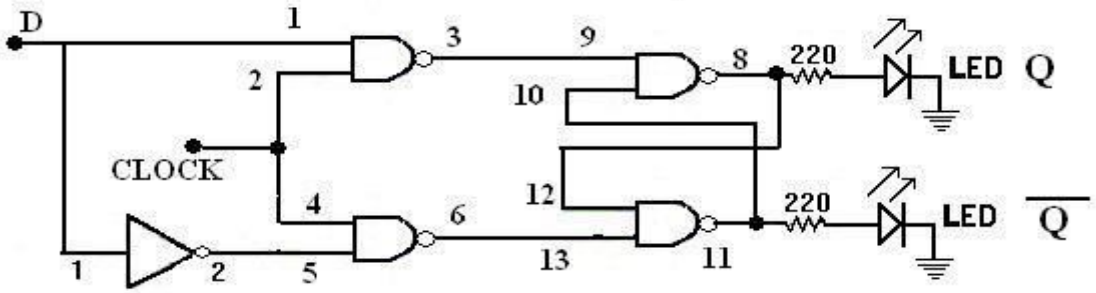
T FLIP FLOP



S-R FLIP FLOP



D FLIP FLOP



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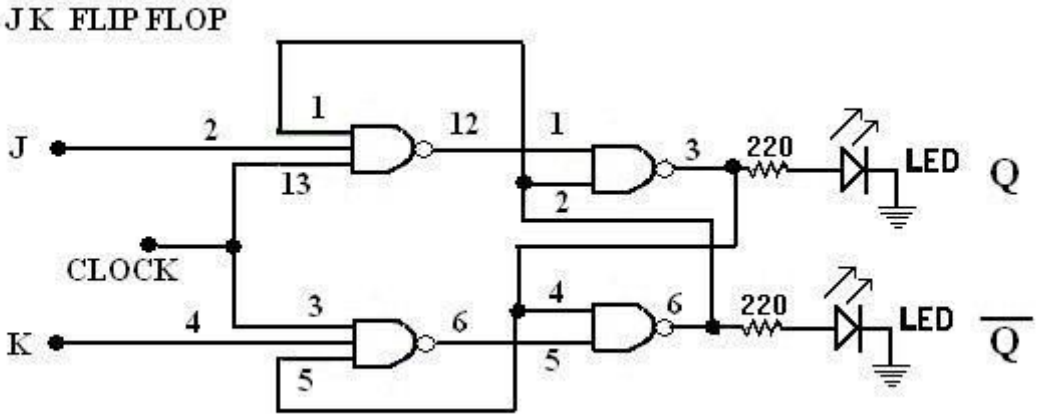

Theory: A flip-flop is a bistable electronic circuit that has two stable states i.e. its output is either 0 or +5Vdc. The main difference between the analog and digital circuit is that, the digital circuits are designed for two state operations. That means the O/p of the digital circuit
has only two states (values), either low or high. In other words the O/p of the digital circuit changes when the I/p changes. However, there are requirements for a digital device or circuit. Whose O/P will remain unchanged, once set, even if there is a change in input. A flip-flop is one such circuit, whose O/p will remain unchanged once set.
There are basic three types of Flip-Flops

1. SR Flip-Flop
2. D Flip-Flop
3. JK Flip-Flop

A flip-flop is a bistable electronic circuit that has two stable states i.e. its output is either 0 or +5Vdc. One of the easiest methods to construct a flip-flop is to connect two inverters in series. But basic flip-flop can be improved by replacing two inverters with either NAND or NOR gate. The additional input of these gates provides a conventional means for application of input signals to switch the flip-flop from one stable state to another.
Two input NAND gate are connected to from flip-flop circuit. These two inputs are R& S. The flip-flop has two outputs terms as Q and Q. If flip-flop is put into one state it will remain in that state as long as power is applied or until tit is changed. In digital circuit, flip-flops are used in variety of storage, counting, sequencing and timing application.

1. R- S Flip-Flop:-

The R-S flip-flop is the simplest. It has two inputs, S & R input; it will put the latch into one state or the other. When a flip-flop is set by S input, it is said to be storing binary 1. (O/P = high). When reset by R input, it is said to be storing binary 0 (O/P = low). An R-S flip-flop constructed by cross- coupling two NAND gates as shown in fig. Fig shows the symbol of the R-S flip-flop. Both Q& Q' output goes high, when both R-S inputs are binary 0. This condition is not allowed in normal use of flip-flop, as the Q' represents the complement output of Q. The truth table for RS flip-flop is given in table.

Truth Table:-

R	S	Qn+1
0	0	Qn
0	1	1
1	0	0

1	1	Not alloowed

2. Study D Flip-Flop: -

The R –S Flip flop has two data inputs R & S. Generation of two signals to drive a flip-flop is a disadvantage in much application. Furthermore, the forbidden condition of both R and S high may occur inadvertently. This has lid to the D Flip Flop a circuit that needs only a single data input. Fig shows the simple diagram of D Flip- Flop using NOR Gate.

Truth Table:-

D	Qn+1
0	**0**
1	**1**

In this circuit the D input is just transferred to the output e.g. If D =0 then output Q is also & If D = 1 output is also 1, as shown in the truth table.

3. Study of T Flip –Flop: -

The basic digital memory circuit is known as flip flop. It two stable states which are known as the 1 state 0 state. It can be obtained by using NAND or NOR gates.Generally there are two inputs to the flip flops (R, S or J K) and two outputs Q and Q. The outputs Q and Q are always complementary. The circuit has two stable state Q=1 which is referred to as the 1 state(or set state) whereas in the other stable state Q=0 which is referred to as the 0 sate (or reset state) If the circuit is in 1 state. It continues to remain in this state and similarly if it is in 0 state, it continues to remain in this state. This property of the circuit is referred to as memory, that is it can store 1 bit of digital information. In a JK flip flop, if J=K the resulting flip flop is referred to as a T Flip Flop, as shown in fig. it has only input, referred to as T input. Its truth table is given in table 1. If T=1 it acts as a toggle witch for every clock pulse the output Q changes.

4. Study of JK Flip –Flop: -

In case of SR flip-flop S=1 & R=1 this input combination is invalid combination. To overcome this problem JK– Flip flop is used. There are two input J & K. Basically flip flop is used to store one bit data. The truth table of the JK flips
flop is as follows: -

If JK is ‘00’ then the circuit will maintain the previous value.
If JK is ‘01’ then the circuit will store the value ‘0’ (Q= ‘0’).
If JK is ‘10’ then the circuit will store the value ‘1’ (Q= ‘1’).
If JK is ‘11’ then the circuit will set in toggle mode.

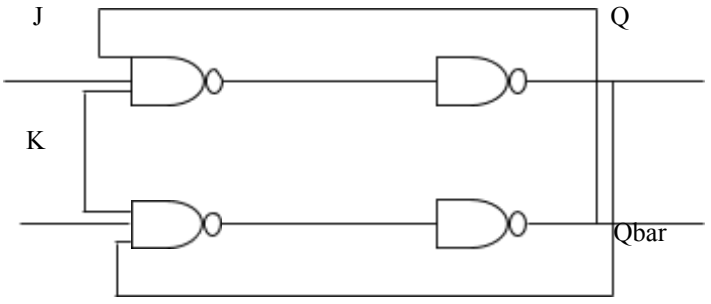

Fig: - -JK-FLIPFLOP

Truth Table

Characteristic Equation of JK-flip-flop is

J	K	Q (n+1)	Operation
0	0	Q(t)	No change
0	1	0	Reset
1	0	1	Set
1	1	Qbar(t)	Complement

PROCEDURE:-

1.Connect the Input terminal of the circuit to the Input logic.
2.Connect the Output terminal to the logic Indicator.
3.Switch ON the power supply.
4.Verify the Truth Table.

RESULT:- Thus ,we have verified the operation of SR flip-flop, JK flip-flop, T- flip-flop, D-flip-flop.

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VIVA QUESTIONS

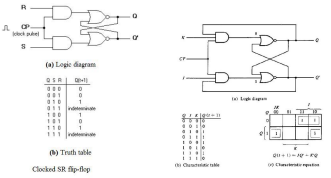
Q.1 What is a Flip flop?

flip flop is an electronic circuit with two stable states that can be used to store binary data. The stored data can be changed by applying varying inputs. Flip-flops and latches are fundamental building blocks of digital electronics systems used in computers, communications, and many other types of systems. Flip-flops and latches are used as data storage elements. It is the basic storage element in sequential logic

Q.2 What is the latch circuit?

A Latch is a special type of logical circuit. The latches have low and high two stable states. Due to these states, latches also refer to as bistable-multivibrators. A latch is a storage device that holds the data using the feedback lane. The latch stores 1 -bit until the device set to 1. The latch changes the stored data and constantly trials the inputs when the enable input set to 1. Based on the enable signal, the circuit works in two states. When the enable input is high, then both the inputs are low, and when the enable input is low, both the inputs are high.

Q.3 Draw truth table & circuit diagram of S-R, J-K, D and T?



Q.4 What are the advantages and disadvantages of S-R flip flop?]

ADVANTAGES

The obvious advantage of this clocked SR flip-flop is that the inputs R and S are considered only when the clock pulse is high. As before the condition R = S = 1 is indeterminate and should be avoided. A typical timing diagram for the clocked SR flip flop

DISADVANTAGES

In SR FF we can apply 1 to both S and R inputs. This will give unpredictable output. This is because both the output NAND gate will try to change it state and one who will win the race will remain in that state making others to compliment it. But there will be race between both NAND gates and hence it's called race condition which is avoided or marked as forbidden.

Q.5 How can you remove the problems of S-R flip flop?

In SR FF we can apply 1 to both S and R inputs. This will give unpredictable output. This is because both the output NAND gate will try to change it state and one who will win the race will remain in that state making others to compliment it. But there will be race between both NAND gates and hence it's called race condition which is avoided or marked as forbidden.

It is avoided by feedback to convert it into JK FF in which making both inputs, J and K will give one more different output that is toggle. This toggles it's last output so that if output was earlier 0 by toggling it will become 1 and vice versa.

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EXPERIMENT NO.-10

AIM: - To verify the operation of Serial in Serial out (SISO) shift register..

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APPRATUS REQUIRED: - Multisim

THEORY: A register that is used to store binary information is known as a memory register. A register capable of shifting binary information either to the right or to the left is called a shift register. The shift register permits the stored data to move from a particular location to some other location within the register. In a shift register, the flip-flops are connected in such a way that the bits of a binary number are entered into the shift register, shifted from one position to another and finally shifted out.

There are two methods of shifting the data viz.,

1. Serial Shifting
2. Parallel Shifting

The serial shifting method shifts one bit at a time for each clock pulse in a serial fashion, beginning with either MSB or the LSB.A four bit shift register requires four clock pulses to shift a bit from the input to the output.

SISO type of shift register accepts data serially, i.e. one bit at a time on a single input line.It produces the stored information on its single output also in serial form. Data may be shifted left using shifting left register or shifted right using shift right register

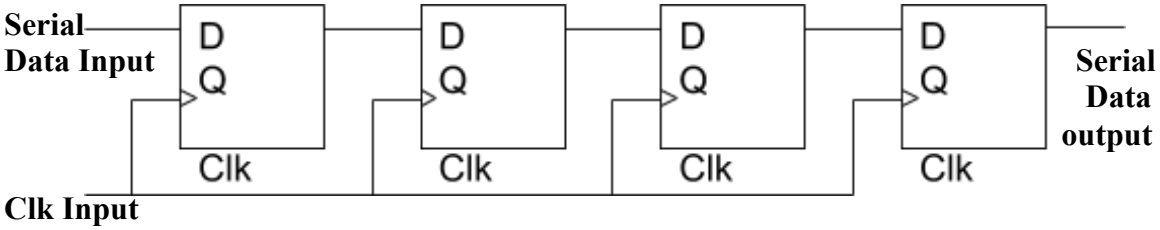

Fig: Serial In Serial Out Shift Register

PROCEDURE:-

1. Connect the Input terminal of the circuit to the Input logic.
2. Connect the Output terminal to the logic Indicator.
3. Switch ON the power supply.
4. Verify the Truth Table.

RESULT:- Thus ,we have verified the operation of Serial Input Serial Out(SISO) shift register.

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VIVA QUESTIONS

Q.1 What is a shift register?

The information stored within these registers can be transferred with the help of shift registers. Shift Register is a group of flip flops used to store multiple bits of data. The bits stored in such registers can be made to move within the registers and in/out of the registers by applying clock pulses. An n-bit shift register can be formed by connecting n flip-flops where each flip flop stores a single bit of data.

Q.2 What is serial shift register?

shift register is very similar to the SIPO above, except were before the data was read directly in a parallel form from the outputs QA to QD, this time the data is allowed to flow straight through the register and out of the other end. Since there is only one output, the DATA leaves the shift register one bit at a time in a serial pattern, hence the name Serial-in to Serial-Out Shift Register or SISO.

Q.3 What is parallel shift register?

The Parallel-in to Serial-out shift register acts in the opposite way to the serial-in to parallel-out one above. The data is loaded into the register in a parallel format in which all the data bits enter their inputs simultaneously, to the parallel input pins PA to PD of the register. The data is then read out sequentially in the normal shift-right mode from the register at Q representing the data present at PA to PD.

Q.4 Write the names of different types of shift register?

Serial-in to Parallel-out (SIPO) -
Serial-in to Serial-out (SISO) -
Parallel-in to Serial-out (PISO) -
Parallel-in to Parallel-out (PIPO) - .

Q.5 Which types of flip flop used in SISO?

The SISO shift register is one of the simplest of the four configurations as it has only three connections, the serial input (SI) which determines what enters the left hand flip-flop, the serial output (SO) which is taken from the output of the right hand flip-flop and the sequencing clock signal (Clk). The logic circuit diagram below shows a generalized serial-in serial-out shift register.

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EXPERIMENT NO.-11

AIM – To Verify different arithmetic and logical operations by using 4 bit ALU 74LS181 IC

APPRATUS REQUIRED: - Bread Board, IC – 74LS181 ALU and Connecting leads or Hookup wires.

THEORY-

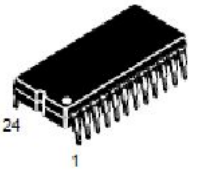
The SN54/74LS181 is a 4-bit Arithmetic Logic Unit (ALU) which can perform all the possible 16 logic, operations on two variables and a variety of arithmetic operations.

- Provides 16 Arithmetic Operations Add, Subtract, Compare, Double, Plus Twelve Other Arithmetic Operations
- Provides all 16 Logic Operations of Two Variables Exclusive — OR, Compare, AND, NAND, OR, NOR, Plus Ten other Logic Operations
- Full Lookahead for High Speed Arithmetic Operation on Long Words
- Input Clamp Diodes

4-BIT ARITHMETIC LOGIC UNIT

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 623-05

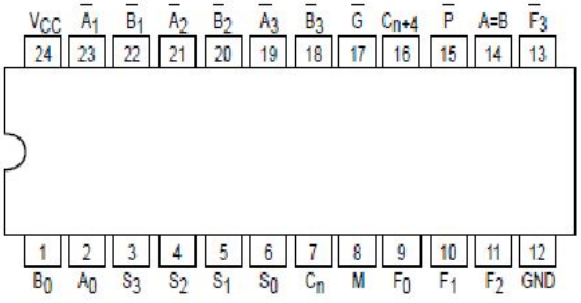


N SUFFIX
PLASTIC
CASE 649-03

ORDERING INFORMATION

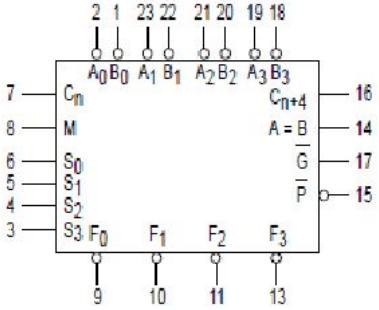
SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC SYMBOL

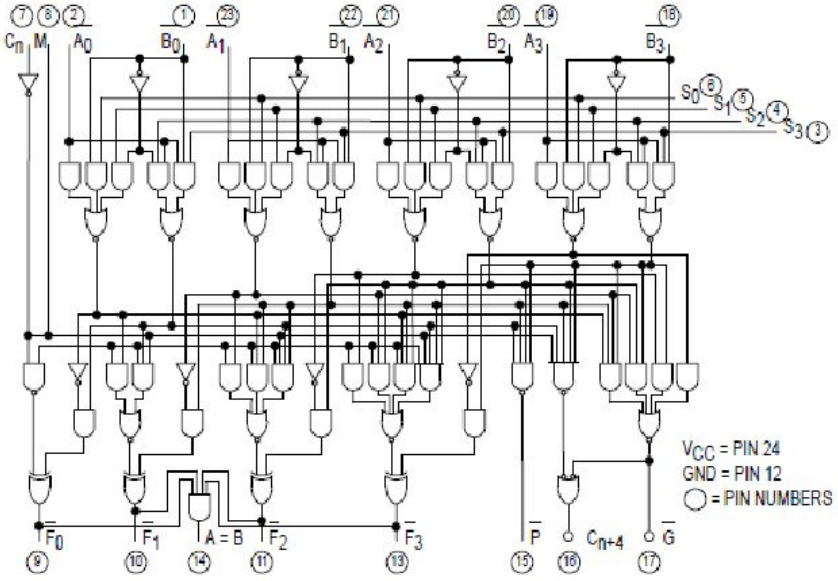


VCC = PIN 24
GND = PIN 12

PIN NAMES		LOADING (Note a)	
		HIGH	LOW
$\overline{A}_0-\overline{A}_3$, $\overline{B}_0-\overline{B}_3$	Operand (Active LOW) Inputs	1.5 U.L.	0.75 U.L.
S_0-S_3	Function — Select Inputs	2.0 U.L.	1.0 U.L.
M	Mode Control Input	0.5 U.L.	0.25 U.L.
$\overline{C}_n$	Carry Input	2.5 U.L.	1.25 U.L.
$\overline{F}_0-\overline{F}_3$	Function (Active LOW) Outputs	10 U.L.	5 (2.5) U.L.
$\overline{A=B}$	Comparator Output	Open Collector	5 (2.5) U.L.
G	Carry Generator (Active LOW) Output	10 U.L.	10 U.L.
$\overline{P}$	Carry Propagate (Active LOW) Output	10 U.L.	5 U.L.
C_{n+4}	Carry Output	10 U.L.	5 (2.5) U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION

The SN54/74LS181 is a 4-bit high speed parallel Arithmetic Logic Unit (ALU). Controlled by the four Function Select Inputs ($S_0 \ldots S_3$) and the Mode Control Input (M), it can perform all the 16 possible logic operations or 16 different arithmetic operations on active HIGH or active LOW operands. The Function Table lists these operations.

When the Mode Control Input (M) is HIGH, all internal carries are inhibited and the device performs logic operations on the individual bits as listed. When the Mode Control Input is LOW, the carries are enabled and the device performs arithmetic operations on the two 4-bit words. The device incorporates full internal carry lookahead and provides for either ripple carry between devices using the C_{n+4} output, or for carry lookahead between packages using the signals P (Carry Propagate) and G (Carry Generate). P and G are not affected by carry in. When speed requirements are not stringent, the LS181 can be used in a simple ripple carry mode by connecting the Carry Output (C_{n+4}) signal to the Carry Input (C_n) of the next unit. For high speed operation the LS181 is used in conjunction with the 9342 or 93S42 carry lookahead circuit. One carry lookahead package is required for each group of the four LS181 devices. Carry lookahead can be provided at various levels and offers high speed capability over extremely long word lengths.

The A = B output from the LS181 goes HIGH when all four $\overline{F}$ outputs are HIGH and can be used to indicate logic equivalence over four bits when the unit is in the subtract mode. The A = B output is open collector and can be wired-AND with other A = B outputs to give a comparison for more then four bits. The A = B signal can also be used with the C_{n+4} signal to indicate A>B and A<B.

The Function Table lists the arithmetic operations that are performed without a carry in. An incoming carry adds a one to each operation. Thus, select code LHHL generates A minus B minus 1 (2s complement notation) without a carry in and generates A minus B when a carry is applied. Because subtraction is actually performed by complementary addition (1s complement), a carry out means borrow; thus a carry is generated when there is no underflow and no carry is generated when there is underflow.

As indicated, the LS181 can be used with either active LOW inputs producing active LOW outputs or with active HIGH inputs producing active HIGH outputs. For either case the table lists the operations that are performed to the operands labeled inside the logic symbol.

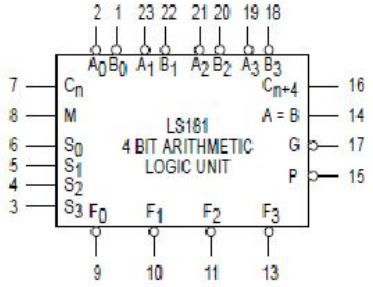
FUNCTION TABLE

MODE SELECT INPUTS				ACTIVE LOW INPUTS & OUTPUTS		ACTIVE HIGH INPUTS & OUTPUTS	
				LOGIC	ARITHMETIC**	LOGIC	ARITHMETIC**
S_3	S_2	S_1	S_0	(M = H)	(M = L) (C_n = L)	(M = H)	(M = L) (C_n = H)
L	L	L	L	$\overline{A}$	A minus 1	$\overline{A}$	A
L	L	L	H	$\overline{AB}$	AB minus 1	$\overline{A+B}$	A + B
L	L	H	L	A + B	AB minus 1	AB	A + B
L	L	H	H	Logical 1 minus 1		Logical 0 minus 1	
L	H	L	L	$\overline{A+B}$	A plus (A + B)	$\overline{AB}$	A plus AB
L	H	L	H	$\overline{B}$	AB plus (A + B)	B	(A + B) plus AB
L	H	H	L	$A \oplus \overline{B}$	A minus B minus 1	$A \oplus B$	A minus B minus 1
L	H	H	H	$\overline{A}+B$	A + B	$\overline{AB}$	AB minus 1
H	L	L	L	AB	A plus (A + B)	$\overline{A+B}$	A plus AB
H	L	L	H	$A \oplus B$	A plus B	$A \oplus \overline{B}$	A plus B
H	L	H	L	B	AB plus (A + B)	B	(A + B) plus AB
H	L	H	H	A + B	A + B	AB	AB minus 1
H	H	L	L	Logical 0	A plus A*	Logical 1	A plus A*
H	H	L	H	AB	AB plus A	A + B	(A + B) plus A
H	H	H	L	AB	AB plus A	A + B	(A + B) Plus A
H	H	H	H	A	A	A	A minus 1

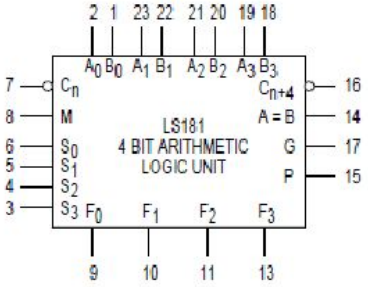
L = LOW Voltage Level
H = HIGH Voltage Level
*Each bit is shifted to the next more significant position
**Arithmetic operations expressed in 2s complement notation

LOGIC SYMBOLS

ACTIVE LOW OPERANDS



ACTIVE HIGH OPERANDS



GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA
V_{OH}	Output Voltage — High (A = B only)	54, 74			5.5	V

PROCEDURE:-

1.Connect the Input terminal of the circuit to the Input logic.
2.Connect the Output terminal to the logic Indicator.
3.Switch ON the power supply.
4.Verify the Truth Table.

RESULT- Thus ,we have verified the operation of ALU.

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VIVA QUESTIONS

Q1. Explain what is ALU.

An arithmetic logic unit(ALU) is a major component of the central processing unit of the a computer system. It does all processes related to arithmetic and logic operations that need to be done on instruction words. In some microprocessor architectures, the ALU is divided into the arithmetic unit (AU) and the logic unit (LU).

Q2. List all airthematic operations performed by 74LS181.

Provides 16 Arithmetic Operations Add, Subtract, Compare, Double,
Plus Twelve Other Arithmetic Operations

Q3.list all logical operations performed by 74LS181.

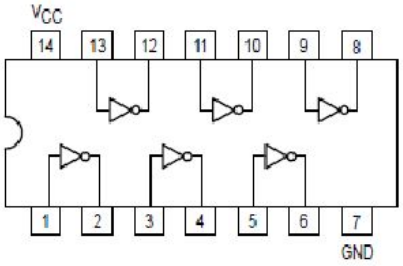
Provides all 16 Logic Operations of Two Variables Exclusive — OR,
Compare, AND, NAND, OR, NOR, Plus Ten other Logic Operations

DATA SHEET OF ALL IC USED IN MANUAL

MOTOROLA

HEX INVERTER

SN54/74LS04



HEX INVERTER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

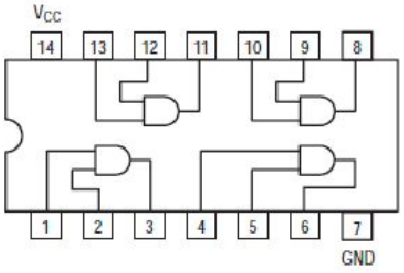
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

SN74LS08

Quad 2-Input AND Gate



ON Semiconductor
Formerly a Division of Motorola
http://onsemi.com

LOW POWER SCHOTTKY

GUARANTEED OPERATING RANGES

Symbol	Parameter	Min	Typ	Max	Unit
V_{CC}	Supply Voltage	4.75	5.0	5.25	V
T_A	Operating Ambient Temperature Range	0	25	70	°C
I_{OH}	Output Current – High			–0.4	mA
I_{OL}	Output Current – Low			8.0	mA

PLASTIC
N SUFFIX
CASE 646

SOIC
D SUFFIX
CASE 751A

ORDERING INFORMATION

Device	Package	Shipping
SN74LS08N	14 Pin DIP	2000 Units/Box
SN74LS08D	14 Pin	2500/Tape & Reel

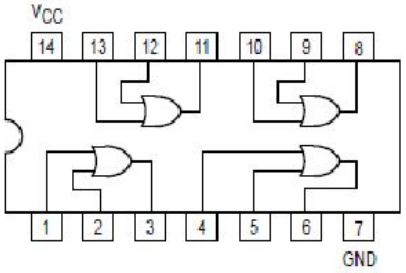
MOTOROLA

QUAD 2-INPUT OR GATE

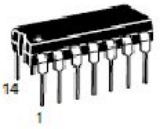
SN54/74LS32

QUAD 2-INPUT OR GATE

LOW POWER SCHOTTKY



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

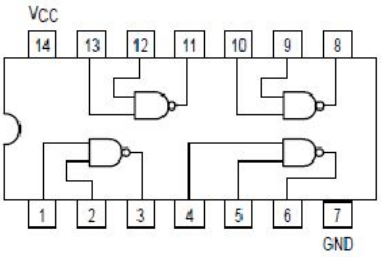
Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

MOTOROLA

QUAD 2-INPUT NAND GATE

- ESD > 3500 Volts

SN54/74LS00



QUAD 2-INPUT NAND GATE

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

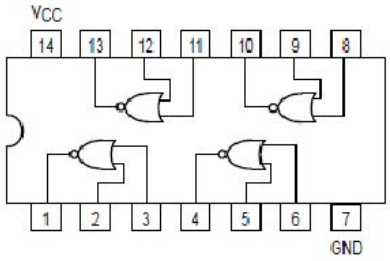
GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

MOTOROLA

QUAD 2-INPUT NOR GATE

SN54/74LS02



QUAD 2-INPUT NOR GATE

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 632-08

N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

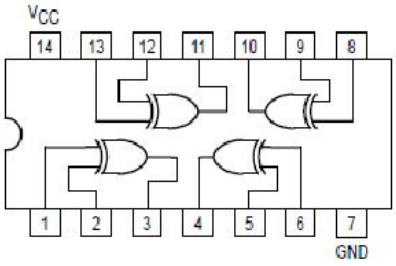
MOTOROLA

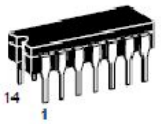
QUAD 2-INPUT EXCLUSIVE-OR GATE

SN54/74LS386

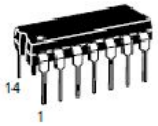
QUAD 2-INPUT EXCLUSIVE-OR GATE

LOW POWER SCHOTTKY

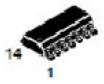




J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06



D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

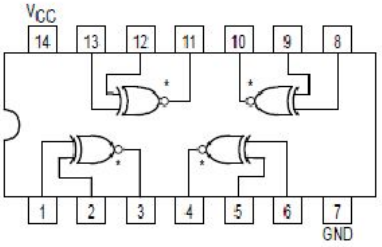
MOTOROLA

QUAD 2-INPUT EXCLUSIVE NOR GATE

SN54/74LS266

QUAD 2-INPUT EXCLUSIVE NOR GATE

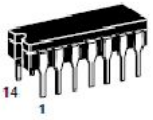
LOW POWER SCHOTTKY



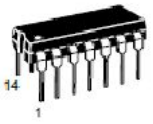
*OPEN COLLECTOR OUTPUTS

TRUTH TABLE

IN		OUT
A	B	Z
L	L	H
L	H	L
H	L	L
H	H	H



J SUFFIX
CERAMIC
CASE 632-08



N SUFFIX
PLASTIC
CASE 646-06

D SUFFIX
SOIC
CASE 751A-02

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
V_{OH}	Output Voltage — High	54, 74			5.5	V
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

MOTOROLA

SN54/74LS42

ONE-OF-TEN DECODER

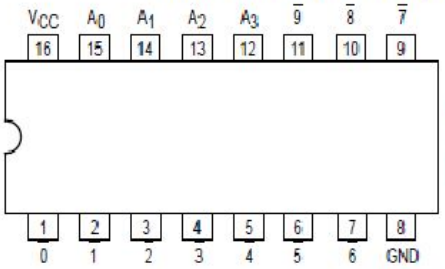
The LSTTL/MSI SN54/74LS42 is a Multipurpose Decoder designed to accept four BCD inputs and provide ten mutually exclusive outputs. The LS42 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Multifunction Capability
- Mutually Exclusive Outputs
- Demultiplexing Capability
- Input Clamp Diodes Limit High Speed Termination Effects

ONE-OF-TEN DECODER

LOW POWER SCHOTTKY

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

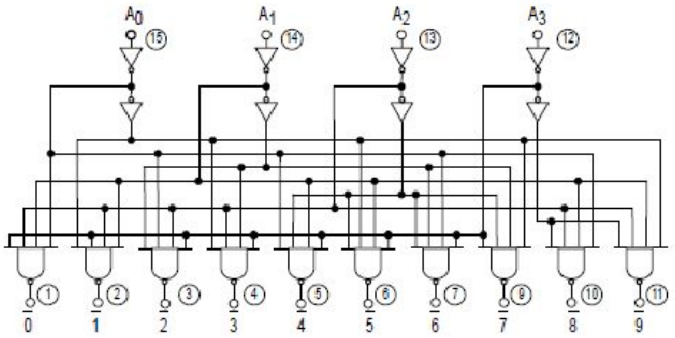
		LOADING (Note a) HIGH	LOW
$\overline{A_0}$–$\overline{A_3}$	Address Inputs	0.5 U.L.	0.25 U.L.
0 to 9	Outputs, Active LOW (Note b)	10 U.L.	5(2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

ORDERING INFORMATION

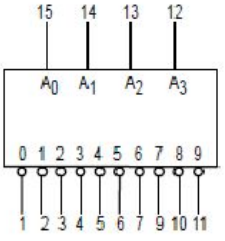
SN54LSXXJ	Ceramic
SN74LSXXN	Plastic
SN74LSXXD	SOIC

LOGIC DIAGRAM



VCC = PIN 16
GND = PIN 8
◯ = PIN NUMBERS

LOGIC SYMBOL



VCC = PIN 16
GND = PIN 8

SN54/74LS42

FUNCTIONAL DESCRIPTION

The LS42 decoder accepts four active HIGH BCD inputs and provides ten mutually exclusive active LOW outputs, as shown by logic symbol or diagram. The active LOW outputs facilitate addressing other MSI units with LOW input enables.

The logic design of the LS42 ensures that all outputs are HIGH when binary codes greater than nine are applied to the inputs.

The most significant input A_3 produces a useful inhibit function when the LS42 is used as a one-of-eight decoder. The A_3 input can also be used as the Data input in an 8-output demultiplexer application.

TRUTH TABLE

A_0	A_1	A_2	A_3	0	1	2	3	4	5	6	7	8	9
L	L	L	L	L	H	H	H	H	H	H	H	H	H
H	L	L	L	H	L	H	H	H	H	H	H	H	H
L	H	L	L	H	H	L	H	H	H	H	H	H	H
H	H	L	L	H	H	H	L	H	H	H	H	H	H
L	L	H	L	H	H	H	H	L	H	H	H	H	H
H	L	H	L	H	H	H	H	H	L	H	H	H	H
L	H	H	L	H	H	H	H	H	H	L	H	H	H
H	H	H	L	H	H	H	H	H	H	H	L	H	H
L	L	L	H	H	H	H	H	H	H	H	H	L	H
H	L	L	H	H	H	H	H	H	H	H	H	H	L
L	H	L	H	H	H	H	H	H	H	H	H	H	H
H	H	L	H	H	H	H	H	H	H	H	H	H	H
L	L	H	H	H	H	H	H	H	H	H	H	H	H
H	L	H	H	H	H	H	H	H	H	H	H	H	H
L	H	H	H	H	H	H	H	H	H	H	H	H	H
H	H	H	H	H	H	H	H	H	H	H	H	H	H

H = HIGH Voltage Level
L = LOW Voltage Level

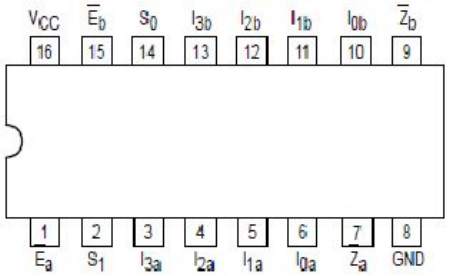
MOTOROLA

DUAL 4-INPUT MULTIPLEXER

The SN54/74LS352 is a very high-speed Dual 4-input Multiplexer with Common Select inputs and individual Enable inputs for each section. It can select two bits of data from four sources. The two buffered outputs present data in the inverted (complementary) form. The SN54/74LS352 is the functional equivalent of the SN54/74LS153 except with inverted outputs.

- Inverted Version of the SN54/74LS153
- Separate Enables for Each Multiplexer
- Input Clamp Diode Limit High Speed Termination Effects

CONNECTION DIAGRAM DIP (TOP VIEW)



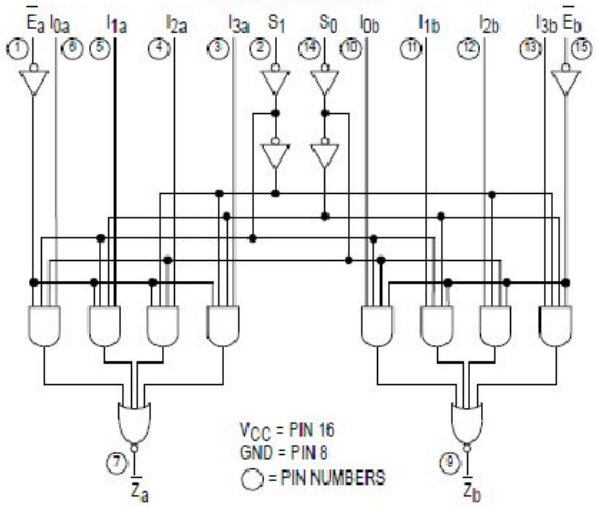
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
$\overline{S}_0$, S_1	Common Select Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$\overline{I}_0$–I_1	Multiplexer Inputs	0.5 U.L.	0.25 U.L.
$\overline{Z}$	Multiplexer Outputs (note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



SN54/74LS352

DUAL 4-INPUT MULTIPLEXER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09

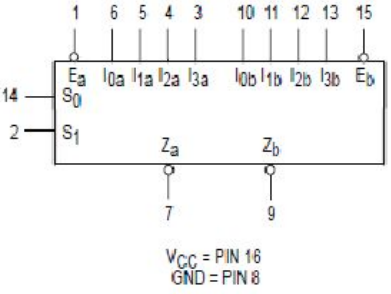
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



MOTOROLA

4-BIT BINARY FULL ADDER WITH FAST CARRY

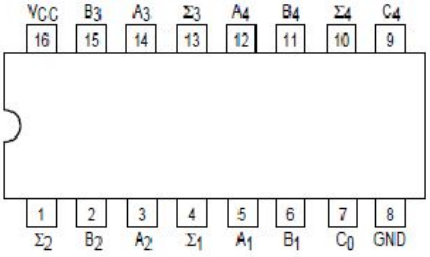
The SN54/74LS283 is a high-speed 4-Bit Binary Full Adder with internal carry lookahead. It accepts two 4-bit binary words (A_1-A_4, B_1-B_4) and a Carry Input (C_0). It generates the binary Sum outputs ($\Sigma_1-\Sigma_4$) and the Carry Output (C_4) from the most significant bit. The LS283 operates with either active HIGH or active LOW operands (positive or negative logic).

SN54/74LS283

4-BIT BINARY FULL ADDER WITH FAST CARRY

LOW POWER SCHOTTKY

CONNECTION DIAGRAM DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

PIN NAMES

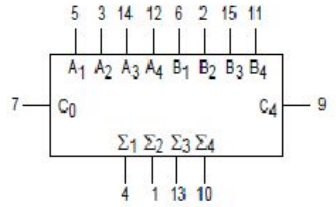
		LOADING (Note a) HIGH	LOW
A_1-A_4	Operand A Inputs	1.0 U.L.	0.5 U.L.
B_1-B_4	Operand B Inputs	1.0 U.L.	0.5 U.L.
C_0	Carry Input	0.5 U.L.	0.25 U.L.
$\Sigma_1-\Sigma_4$	Sum Outputs (Note b)	10 U.L.	5 (2.5) U.L.
C_4	Carry Output (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

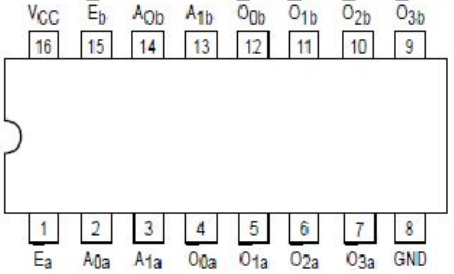
MOTOROLA

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

The LSTTL/MSI SN54/74LS139 is a high speed Dual 1-of-4 Decoder/Demultiplexer. The device has two independent decoders, each accepting two inputs and providing four mutually exclusive active LOW Outputs. Each decoder has an active LOW Enable input which can be used as a data input for a 4-output demultiplexer. Each half of the LS139 can be used as a function generator providing all four minterms of two variables. The LS139 is fabricated with the Schottky barrier diode process for high speed and is completely compatible with all Motorola TTL families.

- Schottky Process for High Speed
- Multifunction Capability
- Two Completely Independent 1-of-4 Decoders
- Active Low Mutually Exclusive Outputs
- Input Clamp Diodes Limit High Speed Termination Effects
- ESD > 3500 Volts

CONNECTION DIAGRAM DIP (TOP VIEW)



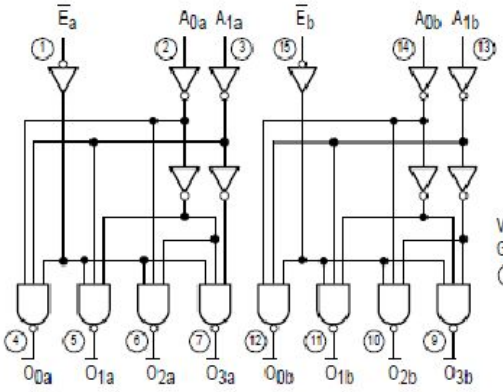
NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

PIN NAMES

		LOADING (Note a) HIGH	LOW
A_0, A_1	Address Inputs	0.5 U.L.	0.25 U.L.
$\overline{E}$	Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
$O_0 - O_3$	Active LOW Outputs (Note b)	10 U.L.	5 (2.5) U.L.

NOTES:
a) 1 TTL Unit Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 2.5 U.L. for Military (54) and 5 U.L. for Commercial (74) Temperature Ranges.

LOGIC DIAGRAM



SN54/74LS139

DUAL 1-OF-4 DECODER/ DEMULTIPLEXER

LOW POWER SCHOTTKY

J SUFFIX
CERAMIC
CASE 620-09

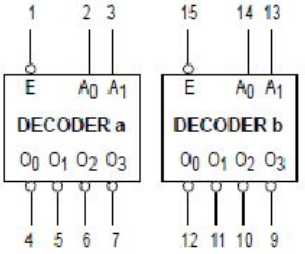
N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

LOGIC SYMBOL



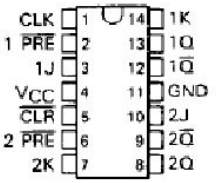
VCC = PIN 16
GND = PIN 8

SN54LS78A, SN74LS78A
DUAL J-K FLIP-FLOPS WITH PRESET, COMMON CLOCK, AND COMMON CLEAR

SDLS200 — DECEMBER 1983—REVISED MARCH 1988

- **Package Options Include Plastic "Small Outline" Packages, Flat Packages, and Plastic and Ceramic DIPs**
- **Dependable Texas Instrument Quality and Reliability**

SN54LS78A . . . J OR W PACKAGE
SN74LS78A . . . D OR N PACKAGE
(TOP VIEW)

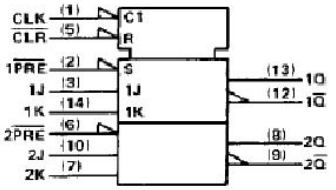


description

The 'LS78A contains two negative-edge-triggered flip-flops with individual J-K, preset inputs, and common clock and common clear inputs. The logic levels at the J and k inputs may be allowed to change while the clock pulse is high and the flip-flop will perform according to the function talbe as long as minimum setup and hold times are observed. The preset and clear are asynchronous active-low inputs. When low they override the clock and data inputs forcing the outputs to the steady-state levels as shown in the function table.

The SN54LS78A is characterized for operation over the full military temperature range of −55°C to 125°C. The SN74LS78A is characterized for operation from 0°C to 70°C.

logic symbol†



†This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

FUNCTION TABLE

INPUTS					OUTPUTS	
PRE	CLR	CLK	J	K	Q	Q̄
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H‡	H‡
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

‡This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (high) level.

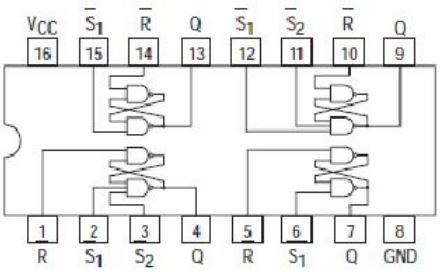
MOTOROLA

QUAD SET-RESET LATCH

SN54/74LS279

QUAD SET-RESET LATCH

LOW POWER SCHOTTKY



TRUTH TABLE

INPUT $\overline{S}_1$	INPUT $\overline{S}_2$	INPUT $\overline{R}$	OUTPUT (Q)
L	L	L	h
L	X	H	H
X	L	H	H
H	H	L	L
H	H	H	No Change

L = LOW Voltage Level
H = HIGH Voltage Level
X = Don't Care
h = The output is HIGH as long as S_1 or S_2 is LOW. If all inputs go HIGH simultaneously, the output state is indeterminate; otherwise, it follows the Truth Table

J SUFFIX
CERAMIC
CASE 620-09

N SUFFIX
PLASTIC
CASE 648-08

D SUFFIX
SOIC
CASE 751B-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXD	SOIC

GUARANTEED OPERATING RANGES

Symbol	Parameter		Min	Typ	Max	Unit
V_{CC}	Supply Voltage	54 74	4.5 4.75	5.0 5.0	5.5 5.25	V
T_A	Operating Ambient Temperature Range	54 74	−55 0	25 25	125 70	°C
I_{OH}	Output Current — High	54, 74			−0.4	mA
I_{OL}	Output Current — Low	54 74			4.0 8.0	mA

MOTOROLA

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

SN54/74LS373
SN54/74LS374

OCTAL TRANSPARENT LATCH WITH 3-STATE OUTPUTS; OCTAL D-TYPE FLIP-FLOP WITH 3-STATE OUTPUT

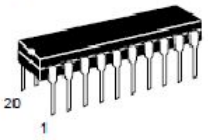
LOW POWER SCHOTTKY

The SN54/74LS373 consists of eight latches with 3-state outputs for bus organized system applications. The flip-flops appear transparent to the data (data changes asynchronously) when Latch Enable (LE) is HIGH. When LE is LOW, the data that meets the setup times is latched. Data appears on the bus when the Output Enable (OE) is LOW. When OE is HIGH the bus output is in the high impedance state.

The SN54/74LS374 is a high-speed, low-power Octal D-type Flip-Flop featuring separate D-type inputs for each flip-flop and 3-state outputs for bus oriented applications. A buffered Clock (CP) and Output Enable (OE) is common to all flip-flops. The SN54/74LS374 is manufactured using advanced Low Power Schottky technology and is compatible with all Motorola TTL families.

- Eight Latches in a Single Package
- 3-State Outputs for Bus Interfacing
- Hysteresis on Latch Enable
- Edge-Triggered D-Type Inputs
- Buffered Positive Edge-Triggered Clock
- Hysteresis on Clock Input to Improve Noise Margin
- Input Clamp Diodes Limit High Speed Termination Effects

J SUFFIX
CERAMIC
CASE 732-03



N SUFFIX
PLASTIC
CASE 738-03

DW SUFFIX
SOIC
CASE 751D-03

ORDERING INFORMATION

SN54LSXXXJ	Ceramic
SN74LSXXXN	Plastic
SN74LSXXXDW	SOIC

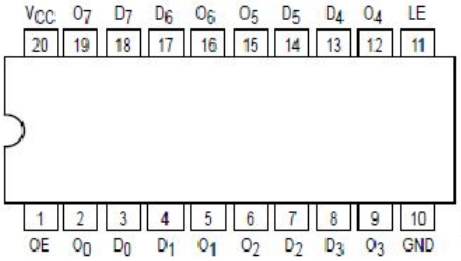
PIN NAMES

		LOADING (Note a) HIGH	LOW
D_0–D_7	Data Inputs	0.5 U.L.	0.25 U.L.
LE	Latch Enable (Active HIGH) Input	0.5 U.L.	0.25 U.L.
$\overline{CP}$	Clock (Active HIGH going edge) Input	0.5 U.L.	0.25 U.L.
$\overline{OE}$	Output Enable (Active LOW) Input	0.5 U.L.	0.25 U.L.
O_0–O_7	Outputs (Note b)	65 (25) U.L.	15 (7.5) U.L.

NOTES:
a) 1 TTL Units Load (U.L.) = 40 µA HIGH/1.6 mA LOW.
b) The Output LOW drive factor is 7.5 U.L. for Military (54) and 25 U.L. for Commercial (74) Temperature Ranges. The Output HIGH drive factor is 25 U.L. for Military (54) and 65 U.L. for Commercial (74) Temperature Ranges.

CONNECTION DIAGRAM DIP (TOP VIEW)

SN54/74LS373



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

SN54/74LS374