BL602/604

Datasheet

Version：1.4

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1 Overview

BL602/BL604 is Wi-Fi + BLE combo chipset for ultra-low-cost and low-power application.

Wireless subsystem contains 2.4G radio, Wi-Fi 802.11b/g/n and BLE 5.0 baseband/MAC designs. Microcontroller subsystem contains a low-power 32-bit RISC CPU, high-speed cache and memories. Power Management Unit controls low-power modes. Moreover, variety of security features are supported.

Peripheral interfaces include SDIO, SPI, UART, I2C, IR remote, PWM, ADC, DAC, PIR, and GPIOs.

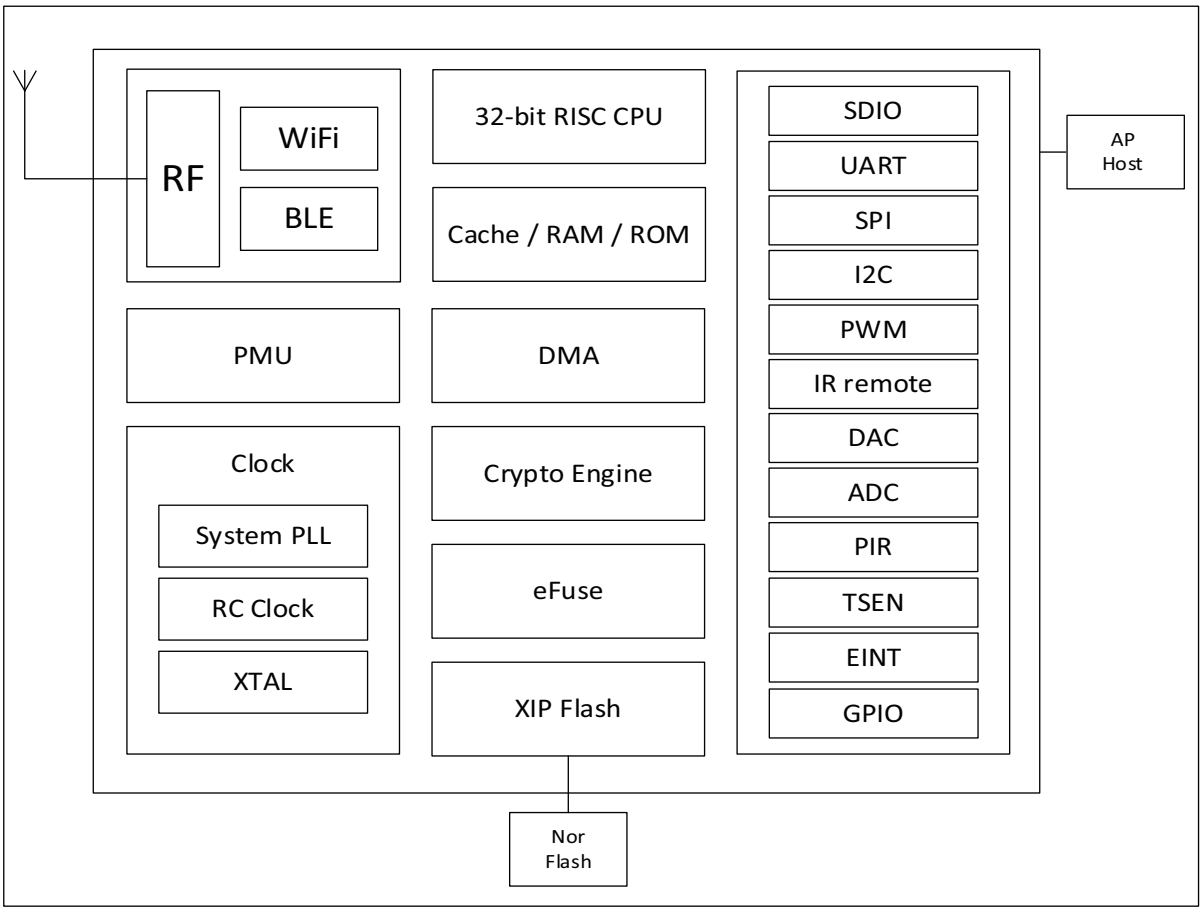

Figure 1.1: Functional Block Diagram

1.1 Wireless

- 2.4 GHz RF transceiver
- Wi-Fi 802.11b/g/n
- Bluetooth® Low Energy 5.0

  BLE 5.0 Channel Selection#2 is supported

  2M PHY / Coded PHY / ADV extension is not supported
- Wi-Fi 20MHz bandwidth
- Wi-Fi Security WPS / WEP / WPA / WPA2 Personal / WPA2 Enterprise / WPA3
- STA，SoftAP，STA+SoftAP and sniffer modes
- Multi-cloud connectivity
- Wi-Fi fast connection with BLE assistance
- Wi-Fi and BLE coexistence
- Integrated balun, PA/LNA

1.2 MCU Subsystem

- 32-bit RISC CPU with FPU (floating point unit)
- Level-1 cache
- One RTC timer update to one year
- Two 32-bit general purpose timers
- Four DMA channels
- DFS (dynamic frequency scaling) from 1MHz to 192MHz
- JTAG development support
- XIP QSPI Flash with hardware encryption support

1.3 Memory

- 276KB RAM
- 128KB ROM
- 1Kb eFuse
- Embedded Flash (Optional)

1.4 Security

- Secure boot
- Secure debug ports
- QSPI Flash On-The-Fly AES Decryption (OTFAD) - AES-128, CTR mode
- AES 128/192/256 bits
- SHA-1/224/256
- TRNG (True Random Number Generator)
- PKA (Public Key Accelerator)

1.5 Peripheral

- One SDIO 2.0 slave
- One SPI master/slave
- Two UART
- One I2C master
- Five PWM channels
- 10-bit general DAC
- 12-bit general ADC
- Two general analog comparators (ACOMP)
- PIR (Passive Infra-Red) detection
- IR remote
- 16 or 23 GPIOs

1.6 Power Management

- Off
- Hibernate (flexible modes)
- Power Down Sleep (flexible modes)
- Active

1.7 Clock

- Support XTAL 24/32/38.4/40MHz
- Internal RC 32kHz oscillator
- Internal RC 32MHz oscillator
- Internal System PLL
- XTAL 32kHz

2 Functional Description

BL602/BL604 main functions described as follows：

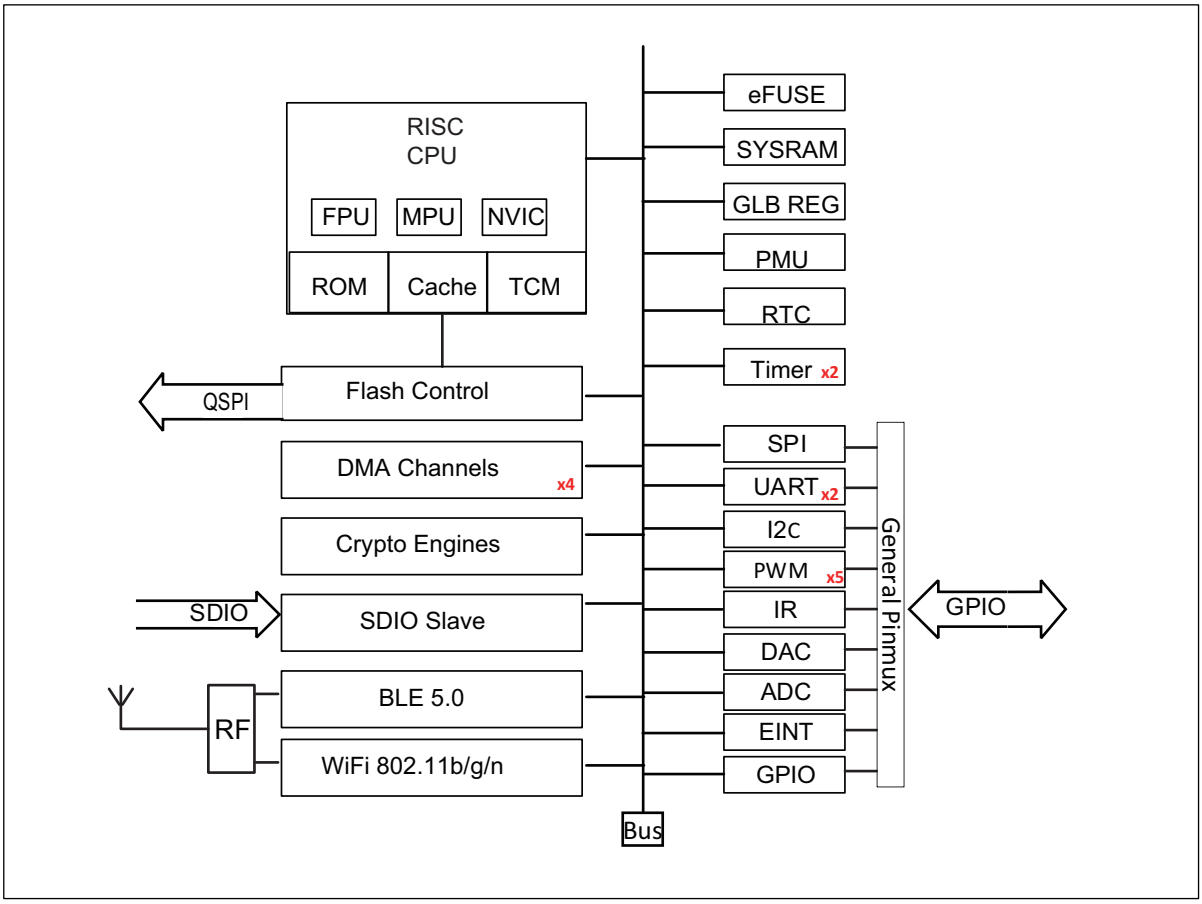

Figure 2.1: System Architecture

2.1 CPU

BL602/BL604 32-bit RISC CPU contains FPU (floating-point unit) for 32-bit single-precision arithmetic, three-stage pipelined (IF, EXE, WB), compressed 16 and 32-bit instruction set, standard JTAG debugger port including 4 hardware-

programmable breakpoints, interrupt controller including 64 interrupts and 16 interrupt levels/priorities for low latency interrupt processing. Up to 192MHz clock frequency, can be dynamically configured to change clock frequency, enter the power saving mode to achieve low power consumption.

Both WiFi/BLE stack and application run on single 32-bit RISC CPU for simple and ultra-low power applications. CPU performance ~1.46 DMIPS/MHz. ~3.1 CoreMark/MHz.

2.2 Cache

BL602/BL604 cache improves CPU performance to access external memory. Cache memories can be partially or fully configured as TCM (tightly coupled memory).

2.3 Memory

BL602/BL604 memories include: on-chip zero-delay SRAM memories, read-only memories, write-once memories, embedded flash memory (optional).

2.4 DMA

BL602/BL604 DMA (direct memory access) controller has four dedicated channels that manage data transfer between peripherals and memories to improve cpu/bus efficiency. There are three main types of transfers including memory to memory, memory to peripheral, and peripheral to memory. DMA also supports LLI (link list item) that multiple transfers are pre-defined by a series of linked lists, then hardware automatically complete all transfers according to each LLI size and address. DMA supports peripheral UART, I2C, SPI, ADC and DAC.

2.5 Bus

BL602/BL604 bus fabric connection and memory-map summarized as follows:

Table 2.1: Bus Connectiom

Slave/ Master	CPU	SDIO	DMA	Crypto Engine	Debug
SRAM	V	V	V	V	V
Peripheral	V	V	V	-	V
WiFi/BLE	V	V	V	-	V

Table 2.2: Memory Map

Module	Base Address	Size	Description
WRAM	0x42030000	112KB	Wireless SRAM memory
RETRAM	0x40010000	4KB	Deep sleep memory (Retention RAM)

Table 2.2: Memory Map

Module	Base Address	Size	Description
HBN	0x4000F000	4KB	Deep sleep control (Hibernate)
PDS	0x4000E000	4KB	Sleep control (Power Down Sleep)
SDU	0x4000D000	4KB	SDIO control
DMA	0x4000C000	4KB	DMA control
QSPI	0x4000B000	4KB	Flash control
IRR	0x4000A600	256B	IR Remote control
TIMER	0x4000A500	256B	Timer control
PWM	0x4000A400	256B	Pulse Width Modulation *5 control
I2C	0x4000A300	256B	I2C control
SPI	0x4000A200	256B	SPI master/slave control
UART1	0x4000A100	256B	UART control
UART0	0x4000A000	256B	UART control
L1C	0x40009000	4KB	Cache control
eFuse	0x40007000	4KB	eFuse memory control
TZ2	0x40006000	4KB	Trust isolation
TZ1	0x40005000	4KB	Trust isolation
SEC	0x40004000	4KB	Security engine
GPIP	0x40002000	4KB	General purpose DAC/ADC/ACOMP interface control
MIX	0x40001000	4KB	Mixed signal register
GLB	0x40000000	4KB	Global control register
RAM	0x22020000 /0x42020000	64KB	On-chip memory.If used as data memory, use address 0x42020000 for access; if used as program memory, use address 0x22020000 for access
XIP	0x23000000	16MB	XIP Flash memory
TCM1	0x22014000 /0x42014000	48KB	Cache memory.If used as data memory, use address 0x42014000 for access; if used as program memory, use address 0x22014000 for access
TCM0	0x22008000 /0x42008000	48KB	Cache memory.If used as data memory, use address 0x42008000 for access; if used as program memory, use address 0x22008000 for access
ROM	0x21000000	128KB	Read-only memory

2.6 Interrupt

BL602/BL604 supports internal RTC wake-up and external interrupts wake-up.

CPU interrupt controller supports stack/nesting, level/pulse, and high/low active.

2.7 Boot

BL602/BL604 supports multiple boot options: UART, SDIO, and Flash.

2.8 Power

PMU (power management unit) manages the power of the entire chip and is divided into active, idle, sleep, and hibernate power modes. The software can be configured to enter sleep mode and wake-up via RTC timer or EINT to achieve low-power sleep and accurate wake-up management.

Power down sleep modes are flexible for applications to configure as the lowest power consumption.

2.9 Clock

Clock control unit generates clocks to the core MCU and the peripheral SOC devices. The root clock source can be XTAL, PLL or RC oscillator. Dynamic power-saved by proper configurations such as sel, div, en, etc. PMU runs at 32kHz clock to keep system low-power in sleep mode.

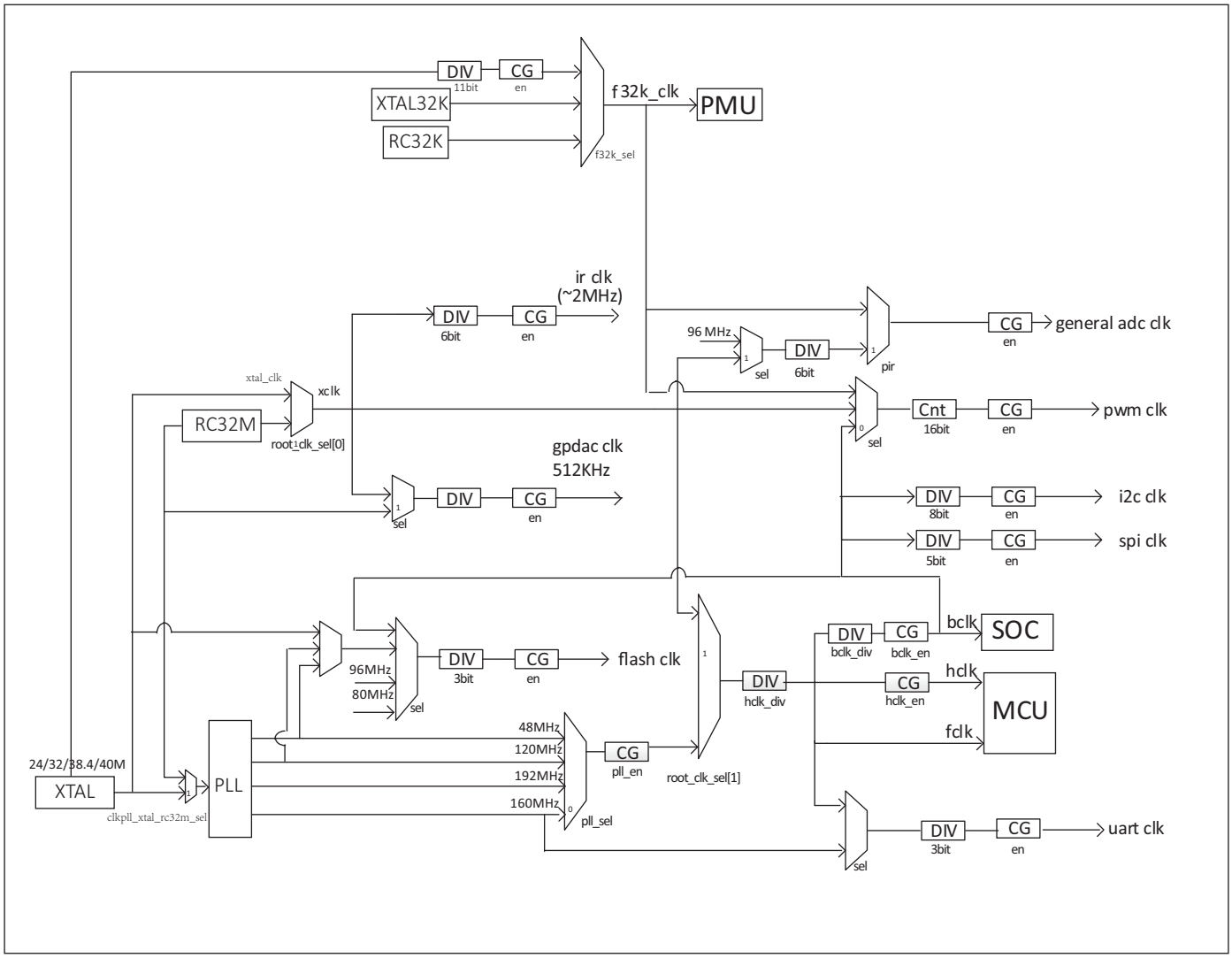

Figure 2.2: Clock Architecture

2.10 Peripherals

Peripherals include SDIO, SPI, UART, I2C, IR remote, PWM, ADC, DAC, PIR.

Each peripheral can be assigned to different groups of GPIOs through flexible configurations.

Each GPIO can be used as a general-purpose input and output function.

3 Pin Definition (QFN32)

BL602 32-pin package includes 10 power pins, 6 analog pins, and 16 flexible GPIO pins.

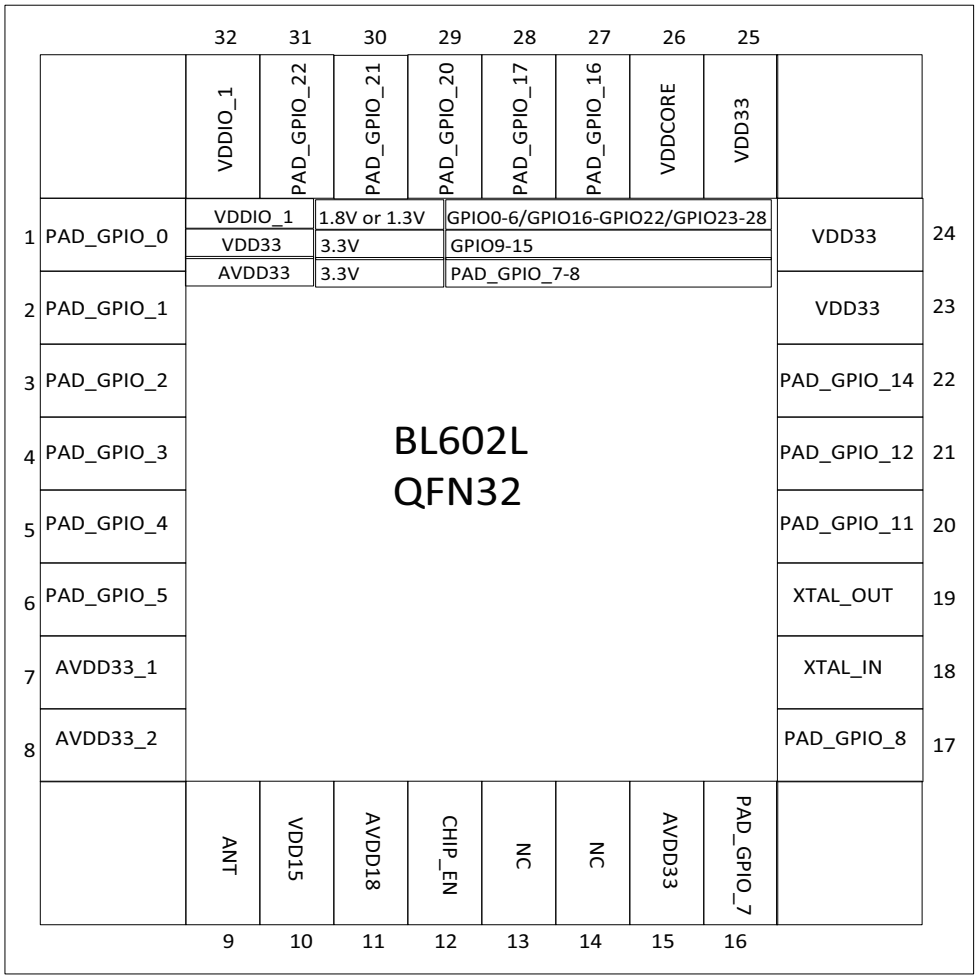

Figure 3.1: BL602L pin layout

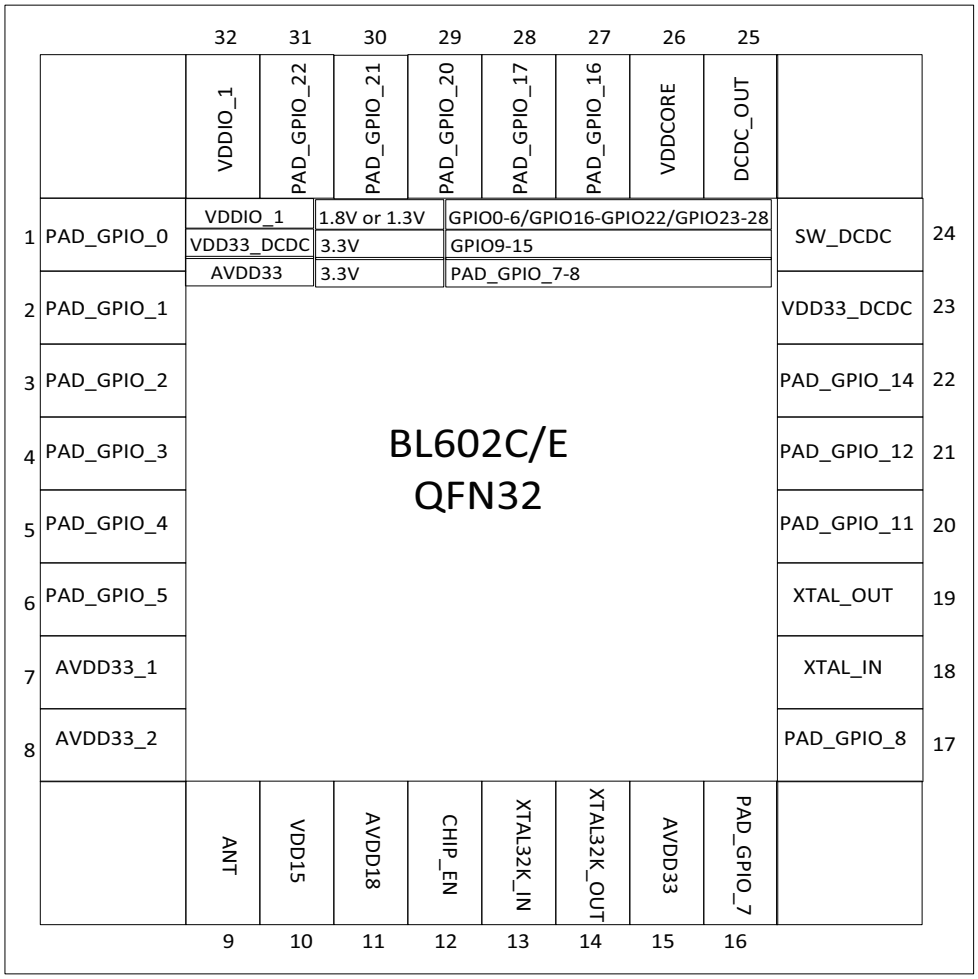

Figure 3.2: BL602C/E pin layout

Table 3.1: Pin Description (QFN32)

No.	Name	Type	Description
1	PAD_GPIO_0	Digital	SDIO_CLK, SF_D1, SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
2	PAD_GPIO_1	Digital	SDIO_CMD, SF_D2, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
3	PAD_GPIO_2	Digital	SDIO_DAT0, SF_D3, SPI_SS, I2C_SCL, UART, PWM, GPIO
4	PAD_GPIO_3	Digital	SDIO_DAT1, SPI_SCLK, I2C_SDA, UART, PWM, GPIO
5	PAD_GPIO_4	Digital	SDIO_DAT2, SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
6	PAD_GPIO_5	Digital	SDIO_DAT3, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
7	AVDD33_1	Power	Externally powered 3.3V
8	AVDD33_2	Power	Externally powered 3.3V
9	ANT	Analog	RF input and output (single pin)
10	VDD15	Power	power 1.5V
11	AVDD18	Power	power 1.8V

Table 3.1: Pin Description (QFN32)

No.	Name	Type	Description
12	CHIP_EN	Digital	Chip enable
13	NC	-	For BL602L
	XTAL32K_IN	Analog	Crystal oscillator 32.768kHz input (For BL602C/E)
14	NC	-	For BL602L
	XTAL32K_OUT	Analog	Crystal oscillator 32.768kHz output (For BL602C/E)
15	AVDD33	Power	Externally powered 3.3V
16	PAD_GPIO_7	Digital	SPI_SCLK, I2C_SDA, UART, PWM, AUXADC, GPIO
17	PAD_GPIO_8	Digital	SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, AUXADC, GPIO
18	XTAL_IN	Analog	External crystal input, support 24/32/38.4/40MHz
19	XTAL_OUT	Analog	External crystal output, support 24/32/38.4/40MHz
20	PAD_GPIO_11	Digital	SPI_SCLK, I2C_SDA, UART, PWM, AUXADC, GPIO
21	PAD_GPIO_12	Digital	SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, AUXADC, GPIO
22	PAD_GPIO_14	Digital	SPI_SS, I2C_SCL, UART, PWM, AUXADC, GPIO
23	VDD33	Power	External power supply 3.3V (For BL602L)
	VDD33_DCDC	Power	DCDC (For BL602C/E)
24	VDD33	Power	External power supply 3.3V (For BL602L)
	SW_DCDC	Power	DCDC (For BL602C/E)
25	VDD33	Power	External power supply 3.3V (For BL602L)
	DCDC_OUT	Power	DCDC (For BL602C/E)
26	VDDCORE	Power	Core Power
27	PAD_GPIO_16	Digital	SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
28	PAD_GPIO_17	Digital	SF_D3, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
29	PAD_GPIO_20	Digital	SF_D0, SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
30	PAD_GPIO_21	Digital	SF_CS, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
31	PAD_GPIO_22	Digital	SF_CLK_OUT, SPI_SS, I2C_SCL, UART, PWM, GPIO
32	DVDDIO_1	Power	Externally powered 3.3V or 1.8V

4 Pin Definition (QFN40)

BL604 40-pin package includes 10 power pins, 6 analog pins, 1 reset pin, and 23 flexible GPIO pins.

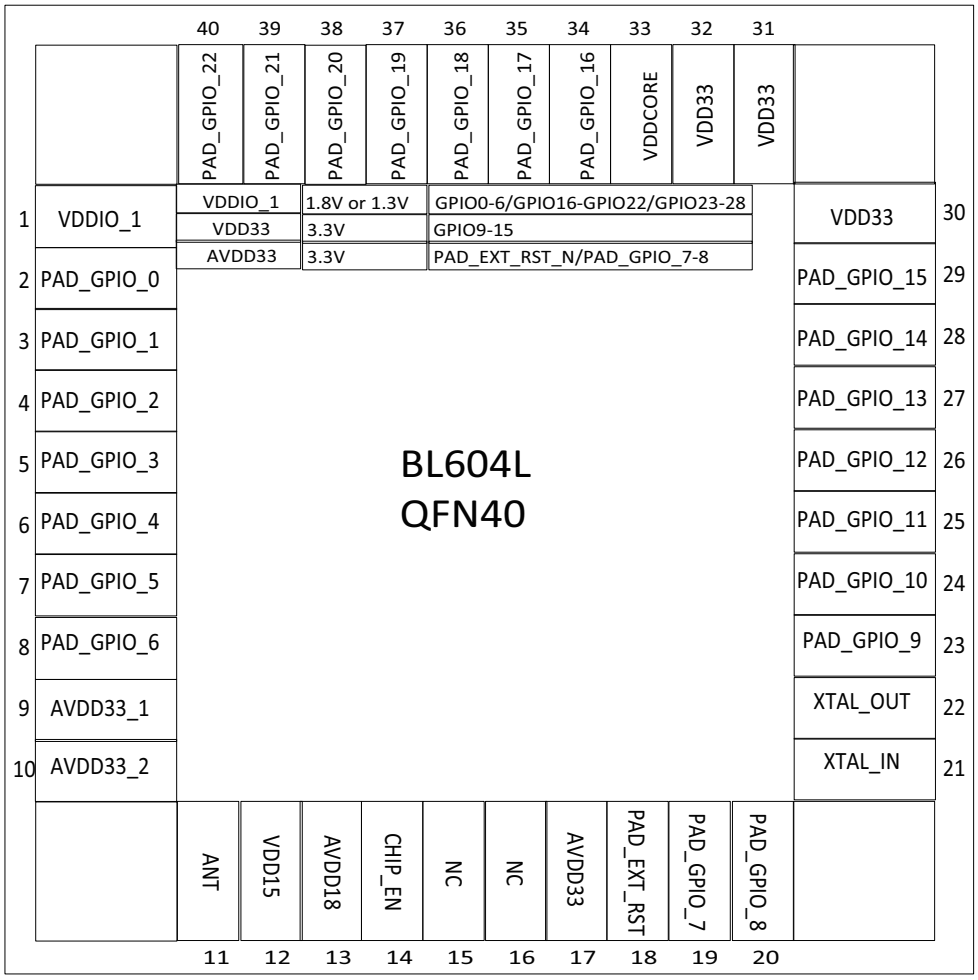

Figure 4.1: BL604L pin layout

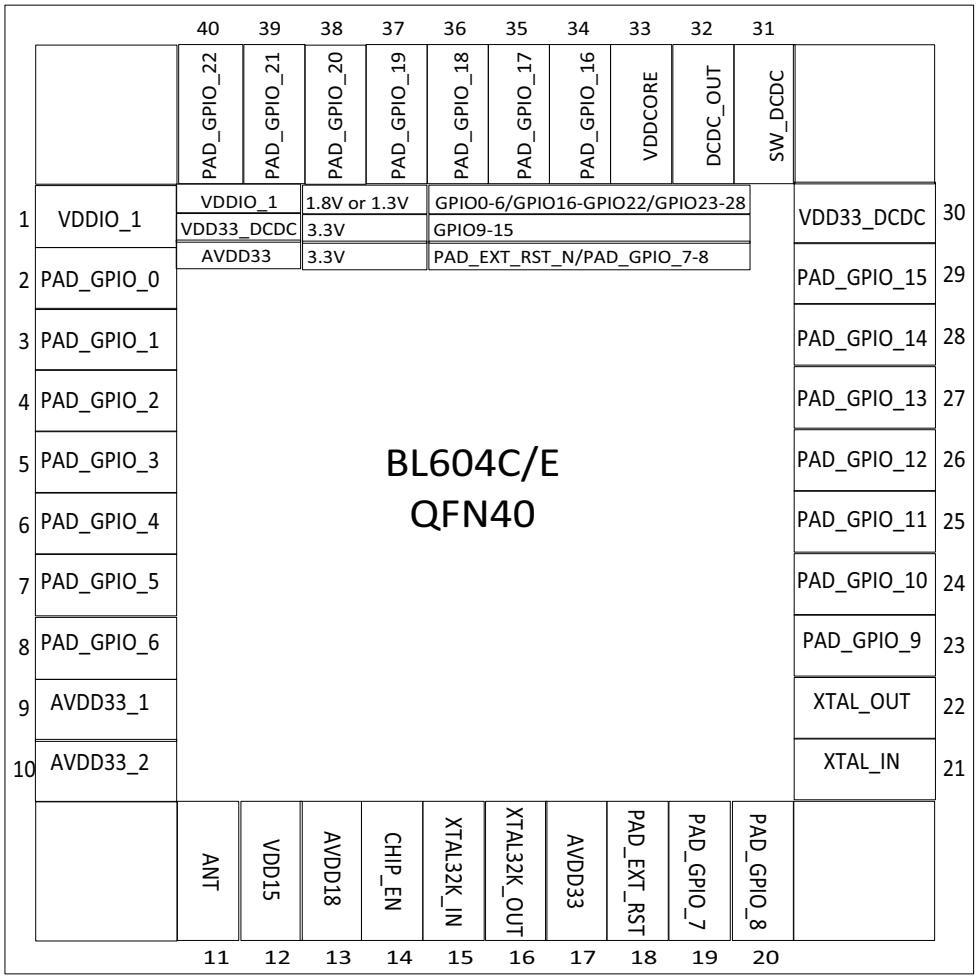

Figure 4.2: BL604C/E pin layout

Table 4.1: Pin Description (QFN40)

No.	Name	Type	Description
1	DVDDIO_1	Power	Externally powered 3.3V or 1.8V
2	PAD_GPIO_0	Digital	SDIO_CLK, SF_D1, SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
3	PAD_GPIO_1	Digital	SDIO_CMD, SF_D2, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
4	PAD_GPIO_2	Digital	SDIO_DAT0, SF_D3, SPI_SS, I2C_SCL, UART, PWM, GPIO
5	PAD_GPIO_3	Digital	SDIO_DAT1, SPI_SCLK, I2C_SDA, UART, PWM, GPIO
6	PAD_GPIO_4	Digital	SDIO_DAT2, SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
7	PAD_GPIO_5	Digital	SDIO_DAT3, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
8	PAD_GPIO_6	Digital	SPI_SS, I2C_SCL, UART, PWM, GPIO
9	AVDD33_1	Power	Externally powered 3.3V
10	AVDD33_2	Power	Externally powered 3.3V
11	ANT	Analog	RF input and output (single pin)

Table 4.1: Pin Description (QFN40)

No.	Name	Type	Description
12	VDD15	Power	power 1.5V
13	AVDD18	Power	power 1.8V
14	CHIP_EN	Digital	Chip enable
15	NC	-	For BL604L
	XTAL32K_IN	Analog	Crystal oscillator 32.768kHz input (For BL604C/E)
16	NC	-	For BL604L
	XTAL32K_OUT	Analog	Crystal oscillator 32.768kHz output (For BL604C/E)
17	AVDD33	Power	Externally powered 3.3V
18	PAD_EXT_RST	Digital	External reset
19	PAD_GPIO_7	Digital	SPI_SCLK, I2C_SDA, UART, PWM, AUXADC, GPIO
20	PAD_GPIO_8	Digital	SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, AUXADC, GPIO
21	XTAL_IN	Analog	External crystal input, support 24/32/38.4/40MHz
22	XTAL_OUT	Analog	External crystal output, support 24/32/38.4/40MHz
23	PAD_GPIO_9	Digital	SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, AUXADC, GPIO
24	PAD_GPIO_10	Digital	SPI_SS, I2C_SCL, UART, PWM, AUXADC, GPIO
25	PAD_GPIO_11	Digital	SPI_SCLK, I2C_SDA, UART, PWM, AUXADC, GPIO
26	PAD_GPIO_12	Digital	SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, AUXADC, GPIO
27	PAD_GPIO_13	Digital	SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, AUXADC, GPIO
28	PAD_GPIO_14	Digital	SPI_SS, I2C_SCL, UART, PWM, AUXADC, GPIO
29	PAD_GPIO_15	Digital	SPI_SCLK, I2C_SDA, UART, PWM, AUXADC, GPIO
30	VDD33	Power	External power supply 3.3V (For BL604L)
	VDD33_DCDC	Power	DCDC (For BL604C/E)
31	VDD33	Power	External power supply 3.3V (For BL604L)
	SW_DCDC	Power	DCDC (For BL604C/E)
32	VDD33	Power	External power supply 3.3V (For BL604L)
	DCDC_OUT	Power	DCDC (For BL604C/E)
33	VDDCORE	Power	Core Power
34	PAD_GPIO_16	Digital	SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
35	PAD_GPIO_17	Digital	SF_D3, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
36	PAD_GPIO_18	Digital	SF_D2, SPI_SS, I2C_SCL, UART, PWM, GPIO
37	PAD_GPIO_19	Digital	SF_D1, SPI_SCLK, I2C_SDA, UART, PWM, GPIO

Table 4.1: Pin Description (QFN40)

No.	Name	Type	Description
38	PAD_GPIO_20	Digital	SF_D0, SPI_MOSI/SPI_MISO, I2C_SCL, UART, PWM, GPIO
39	PAD_GPIO_21	Digital	SF_CS, SPI_MOSI/SPI_MISO, I2C_SDA, UART, PWM, GPIO
40	PAD_GPIO_22	Digital	SF_CLK_OUT, SPI_SS, I2C_SCL, UART, PWM, GPIO

5 Electrical Specifications

5.1 Absolute Maximum Rating

Table 5.1: Absolute Maximum Rating

Pin Name	Min.	Max.	Unit
AVDD33_1	-0.3	3.63	V
AVDD33_2	-0.3	3.63	V
AVDD33	-0.3	3.63	V
DVDD33_DCDC	-0.3	3.63	V
DVDDIO_1	-0.3	3.63	V
ESD Protection (HBM)		2000	V
Storage Temperature	-45	135	°C

5.2 Operating Condition

Table 5.2: Recommended Power Operating Range

Pin Name	Min.	Typ	Max.	Unit
AVDD33_1	2.1	3.3	3.63	V
AVDD33_2	2.1	3.3	3.63	V
AVDD33	2.1	3.3	3.63	V
DVDD33_DCDC	2.1	3.3	3.63	V
DVDDIO_1	2.1 / 1.62	3.3 / 1.8	3.63 / 1.98	V

Table 5.3: Recommended Temperature Operating Range

Item		Min.	Max.	Unit
Temperature	Main Die	-30	105	°C
	Multi-Die SiP	-30	85	°C

Table 5.4: General Operating Conditions

Item	Description	Min.	Typ	Max.	Unit
FCPU	CPU/TCM/Cache clock frequency	1	160	192	MHz
FSYS	System clock frequency	1	80	96	MHz

6 Reference Design (simplified)

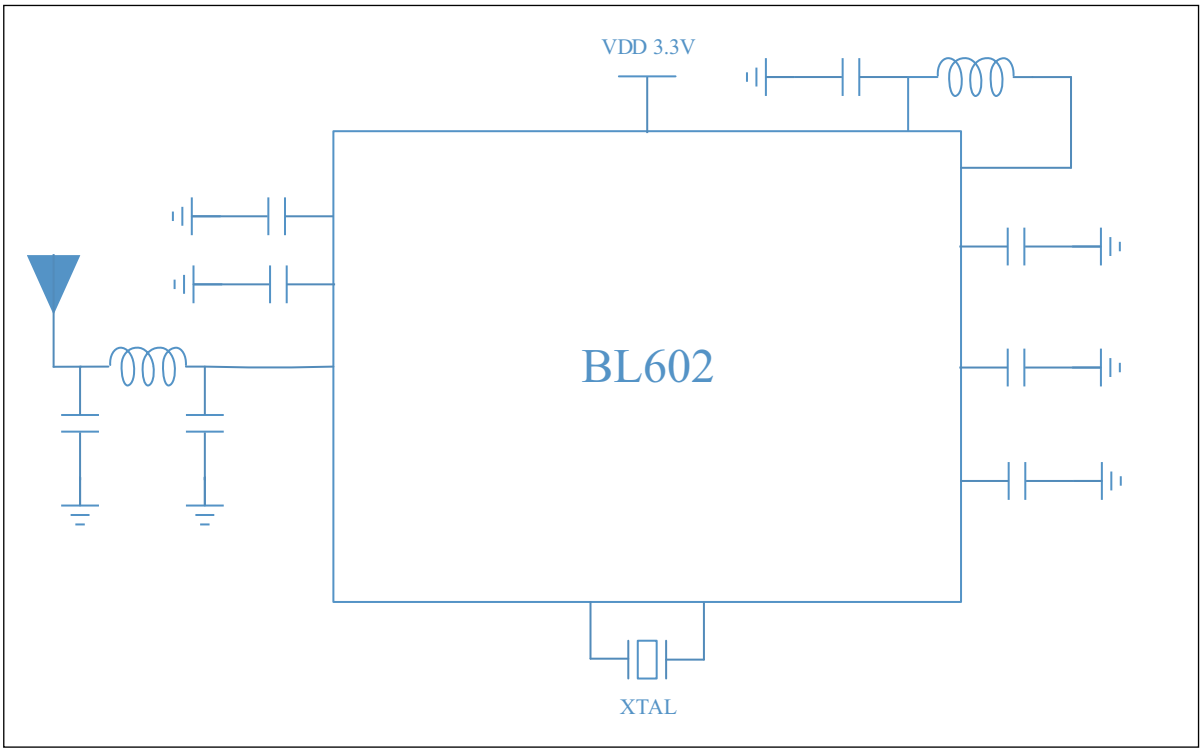

Figure 6.1: Reference Design

7 Package Information(QFN32)

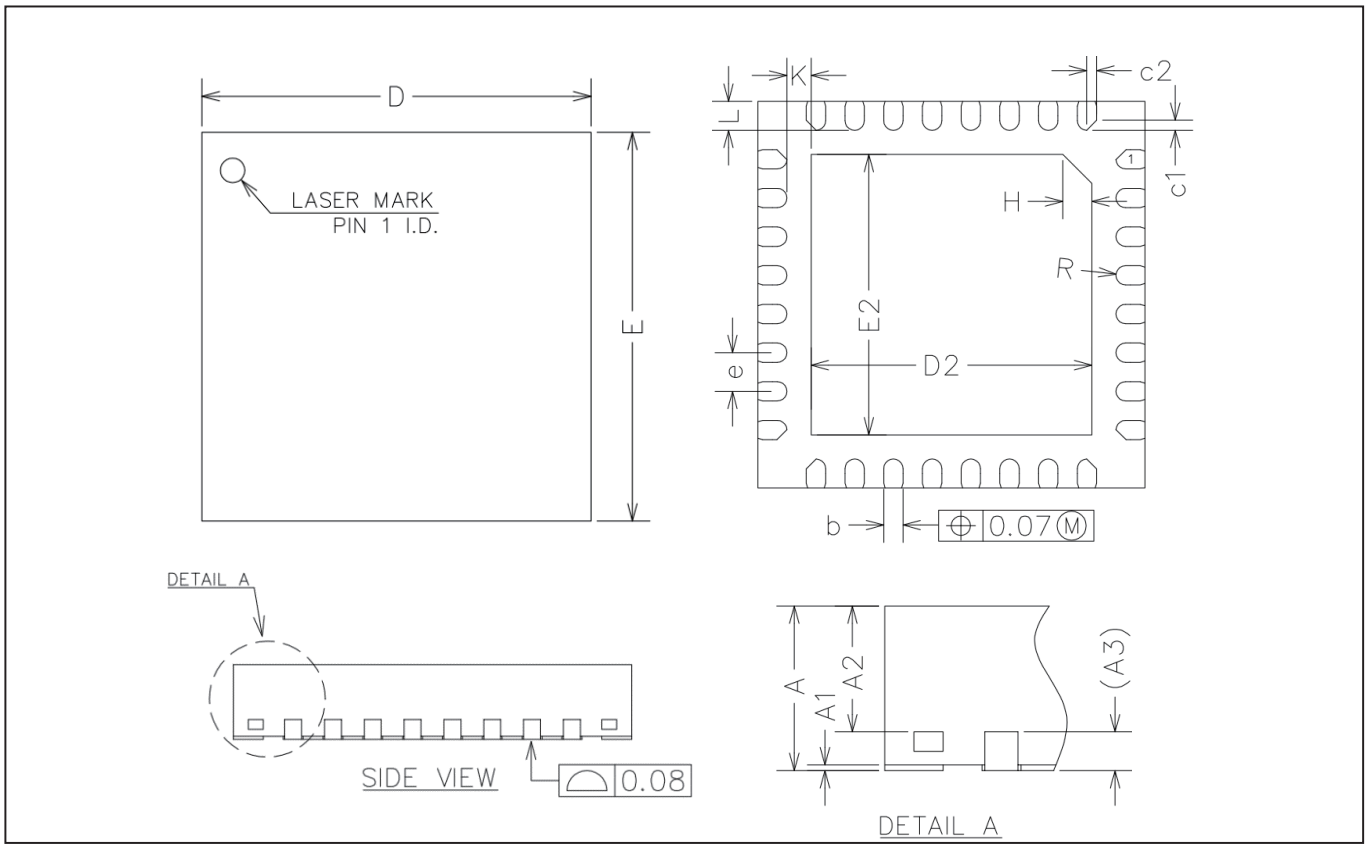

Figure 7.1: QFN32 Package drawing

Table 7.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05

Table 7.1: QFN32 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.50	0.55	0.60
A3	0.20REF		
b	0.15	0.20	0.25
D	3.90	4.00	4.10
E	3.90	4.00	4.10
D2	2.80	2.90	3.00
E2	2.80	2.90	3.00
e	0.30	0.40	0.50
H	0.30REF		
K	0.25REF		
L	0.25	0.30	0.35
R	0.09	-	-
c1	-	0.10	-
c2	-	0.10	-

8 Package Information(QFN40)

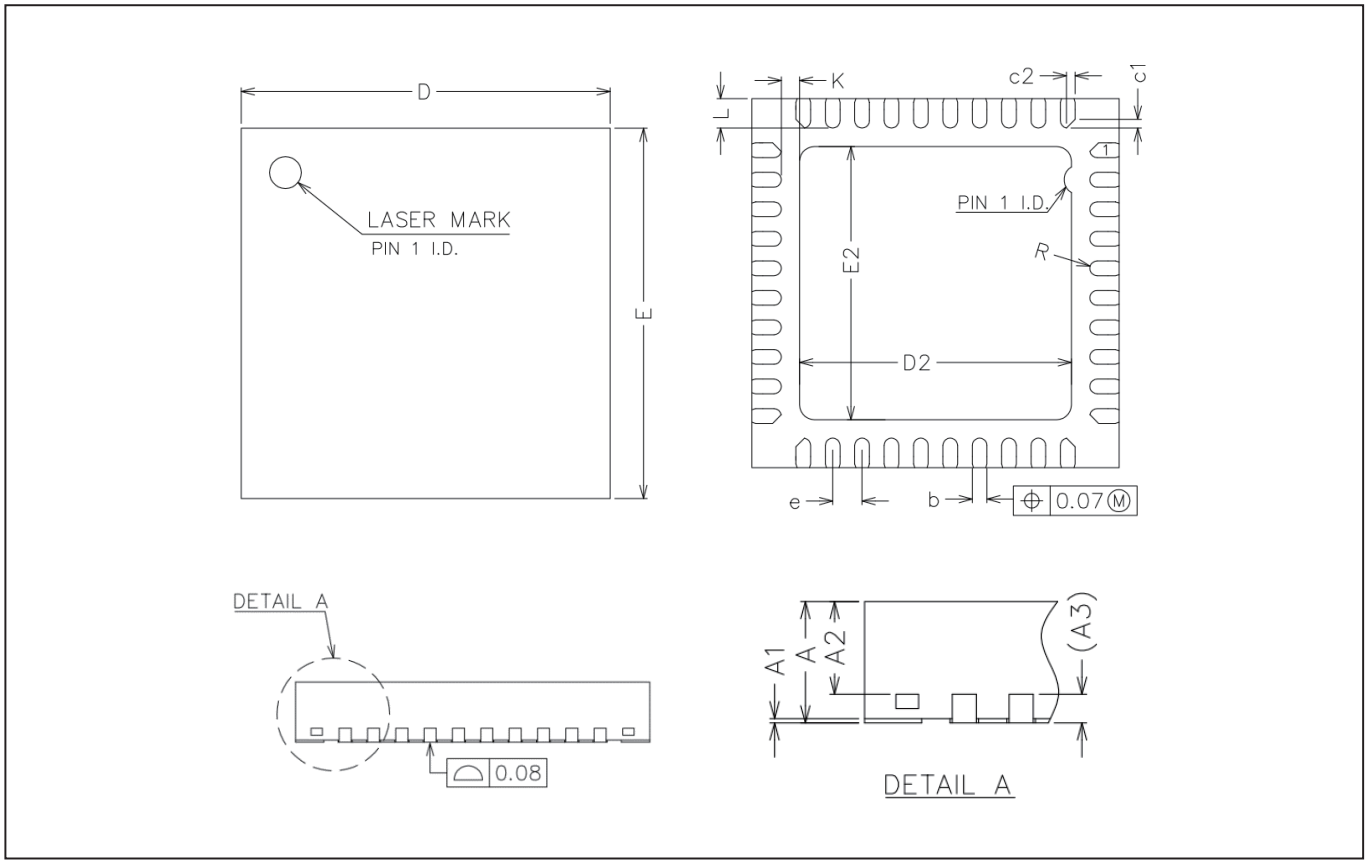

Figure 8.1: QFN40 Package drawing

Table 8.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A	0.80	0.85	0.90
A1	0	0.02	0.05

Table 8.1: QFN40 Size Description(Units Of Measure=Millimeter)

SYMBOL	MIN	NOM	MAX
A2	0.60	0.65	0.70
A3	0.20REF		
b	0.15	0.20	0.25
D	4.90	5.00	5.10
E	4.90	5.00	5.10
D2	3.60	3.70	3.80
E2	3.60	3.70	3.80
e	0.35	0.40	0.45
K	0.20	-	-
L	0.35	0.40	0.45
R	0.075	-	-
C1	-	0.12	-
C2	-	0.12	-

9 Top Marking Definition

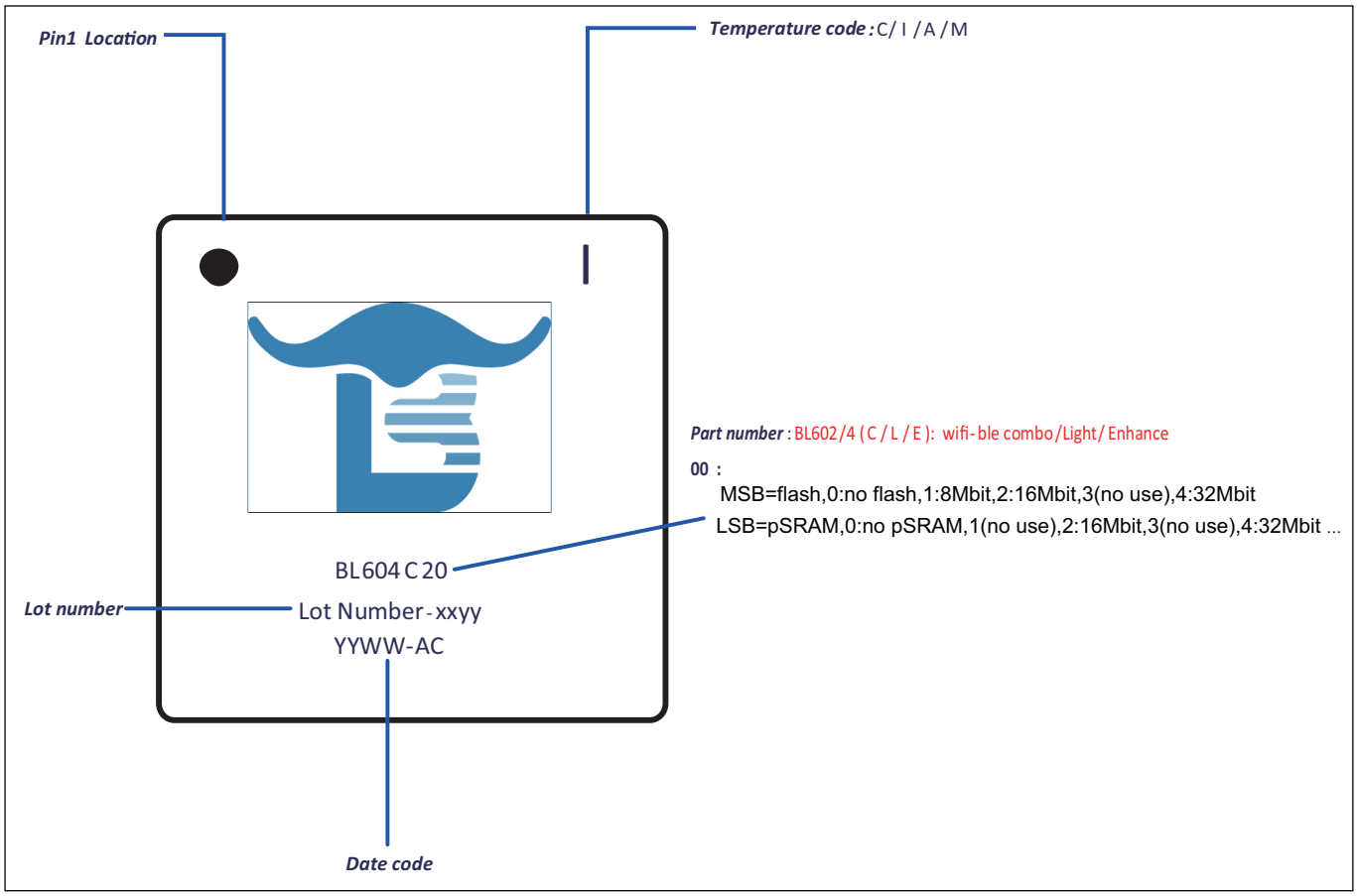

Figure 9.1: Top Marking Definition

10 Ordering Information

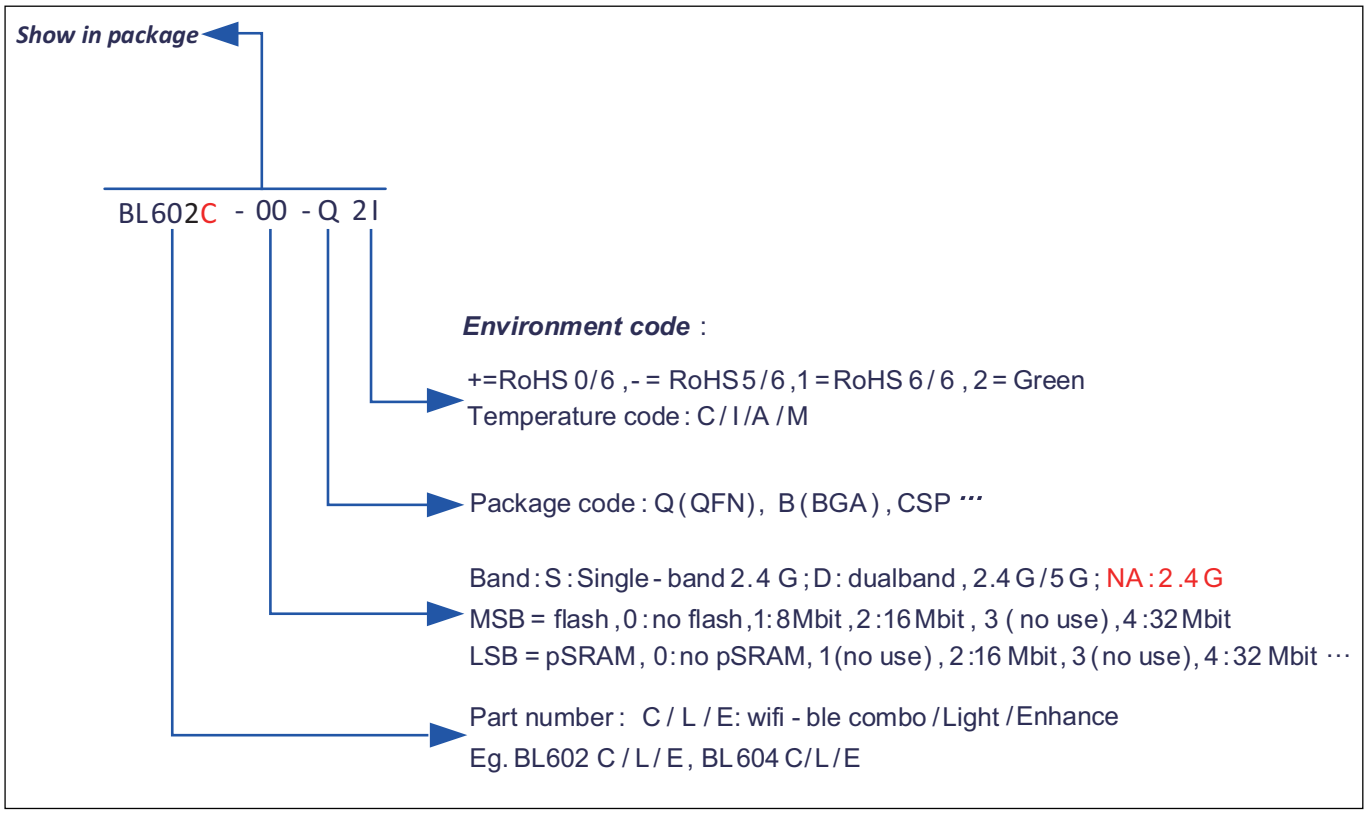

Figure 10.1: Part Number

Table 10.1: Part Order Options

Product No.	Description
BL602C-00-Q2I	WiFi/BLE Combo, QFN32
BL602C-20-Q2I	WiFi/BLE Combo, QFN32, flash 16Mb
BL604E-20-Q2I	WiFi/BLE Enhance, QFN40, flash 16Mb

Table 10.1: Part Order Options

Product No.	**Description**
BL602L-20-Q2H	Light, QFN32, flash 16Mb

11 Revision history

Table 11.1: Document revision history

Date	Revision	Changes
2020/2/13	0.9	Initial release
2020/4/20	1.0	Add Marking Definition
2020/5/28	1.1	Modify clock frequency
2020/7/28	1.2	Modify Product Number
2020/12/15	1.4	Modify peripheral characteristics