

# SERVICE MANUAL



Design and specifications are subject to change without prior notice. (Only for Reference)

<b>Description:</b> SERVICE MANUAL 7M31B
<b>Version:</b> V0.00
<b>Prepared By:</b> Hanweiwei <b>Date:</b> 2019-03-06
<b>Checked By:</b> <b>Date:</b>
<b>Approved By:</b> <b>Date:</b>

# **CONTENT**

---

---

Revision History.....	3
1. Technical Specification.....	4
2. System Block.....	6
3. List of key parts.....	7
4. IC General Description.....	10
5. Software Upgrade.....	39
6. Setting Hote Mode Menu.....	40
7. Wiring Diagram.....	41
8. PCB Silkscreen.....	42
9. Schematic Circuit Diagram.....	44
10. Key Power Check Point.....	57
11. Trouble Shooting.....	58

## Revision History

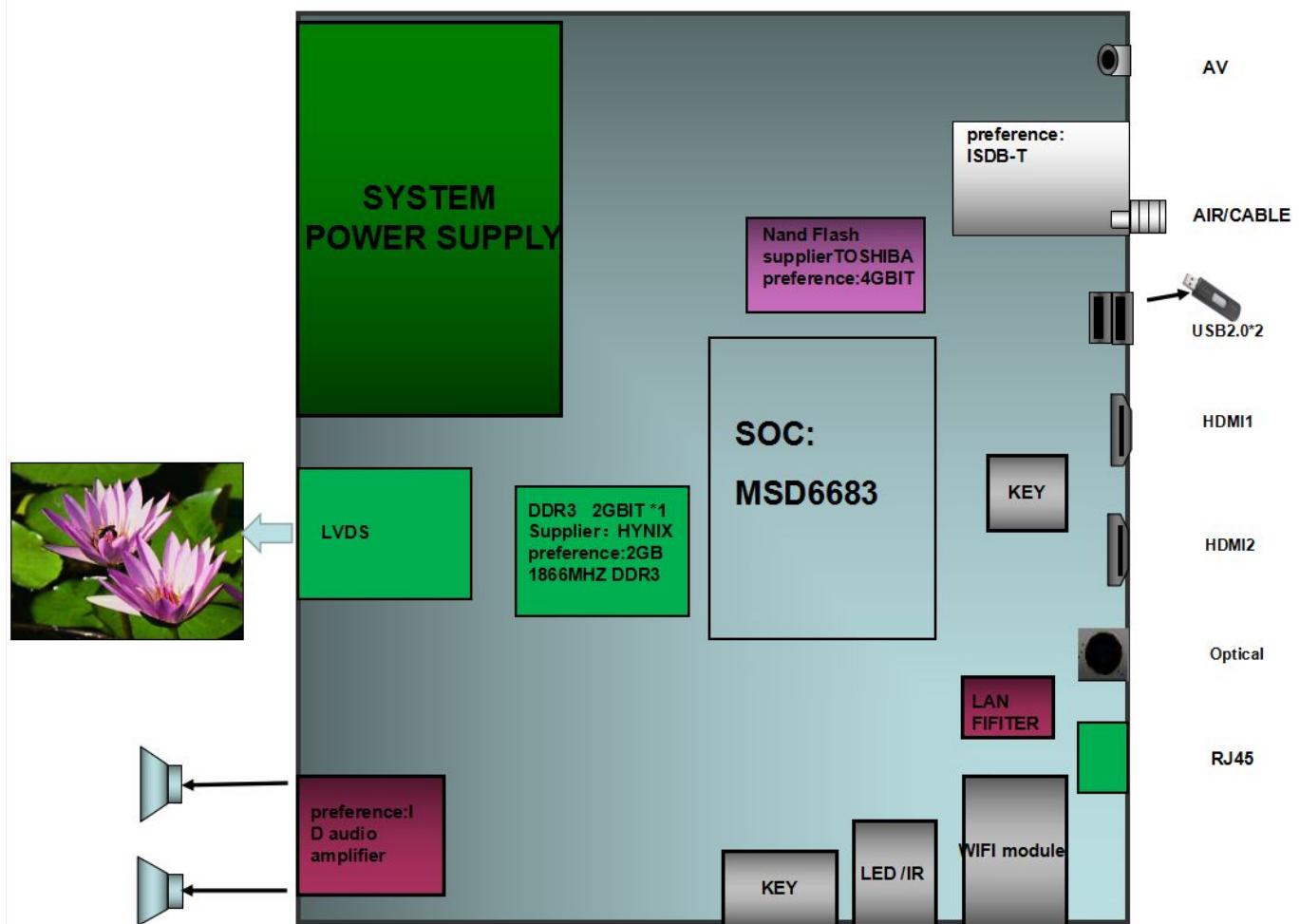
Version Number	Revision Data	Description of changes
V0.00	2018-03-06	Initial release

# 1. Technical Specification

Brief Information					
1.1	Model Name				
1.2	Solution				
1.3	Display Definition (max)				
1.4	Display Interface	LVDS/MiniLVDS/EPI/EDP/V-BY-ONE			
1.5	AC Input Range	(三合一板必须填写)			
1.6	Standby Power Consumption				
1.7	White Balance, Color Temperature	Min	TYP	Max	Unit
		6500	9877	12000	kdeg
1.8	Video Noise Limited Sensitivity(@S/N=30dB)			51	dBu
				54	dBu
1.9	Video Input Level(75 ohm)		1		Vp-p
Signal Receiving System					
2.1	ATV Receiving System	ATV Receiving System			
2.1.1		NTSC-M			
2.1.2		PAL BG/I/DK/NTSC-M			
2.1.3		PAL/SECAM BG/DK/I SECAM L/L"			
2.1.4		PAL M/N NTSC-M			
2.2	DTV Receiving System	DTV Receiving System			
2.2.1		ATSC			
2.2.2		DVB-T			
2.2.3		DVB-T with CI			
2.2.4		DVB-T2			
2.2.5		DVB-T2 with CI+			
2.2.6		ISDB-T			
2.2.7		DTMB			
2.2.8		DVB-C with CA			
2.2.9		DVB-S			
2.2.10		DVB-S2			
2.3	Antenna input	Antenna input			
2.3.1		Antenna Input port: 1 (1 for analogue)			

2.3.2		Antenna Input port: 1 (1 for both analogue and digital)	Yes
2.3.3		Antenna Input port: 2 (1 air + 1 Cable)	No
2.3.4		Type of Antenna Input Port	IEC169-24 Male
2.3.5		Receiving Frequency range (ATV)	54MHz~864MHz
2.3.6		Receiving Frequency range (DTV)	177MHz~803MHz
2.37		Receiving Frequency range (DVB-S/S2)	Nonsupport

## 2. System Block



### **3. List of key parts**

(三合一板需要加入电源部分关键器件)

#### **3.1 Part of Mainboard**

S	NAME	Part reference	DESCRIPTION	SKYWORTH P/N
	SOC	U1	SMD IC MSD6683BQHT-8-00II MSTAR (DTV PROCESSOR) BGA	475C-M66830-5770
Crystal		Y201	SMD CRYSTAL 24.000MHZ +/-20PPM 20PF HC-49/USM	4900-124052-RS00
		XOT8	SMD CRYSTAL 24.000MHZ +/-10PPM CL=9PF (3.2*2.5MM) TAPE TYPE	4900-124054-QS00
		XOT9	SMD CRYSTAL 24.000MHZ +/-10PPM CL=9PF (3.2*2.5MM) TAPE TYPE	4900-124054-QS00
DDR	UM4		SMD IC H5TQ2G63GFR-TEC HYNIX (128M*16BIT DDR3-2133MHZ) FBGA	4711-H5T2G7-0960
FLASH	U0M4		SMD IC THGBMNG5D1LBAIL TOSHIBA (4GB E-MMC MODULE) BGA	4701-T5D4G2-1530
E2PROM	U204		SMD IC FM24C32D-SO-T-G FUDANWEI (1.7V-5.5V 32K BIT EEPROM) SOP-8	472M-F24322-0080
OTHERS		U4P7	SMD IC MP1652GTF-Z MPS(2A 18V STEP DOWN CONVERTER#SOT563	476A-M16520-0060
		U4P1	SMD IC MP1653GTF-Z MPS(3A 17V STEP DOWN CONVERTER#SOT563	476A-M16530-0060
		U4P6	SMD IC MP1652GTF-Z MPS(2A 18V STEP DOWN CONVERTER#SOT563	476A-M16520-0060
		U4P2	SMD IC MSH6103A MSTAR (POWER MANAGEMENT) ESOP	475C-M61030-0080
		U0P3	SMD IC TPS562201DDCR TI(2A 4.5V-17V STEP DOWN CONVERTER) SOT-23	4722-T56220-0060
		U3P6	SMD IC JY1117EA JY(1A ADJUSTABLE LDO) SOT223	47JN-J11170-0030
Tuner		U1T4	SMD IC MXL661 MAXLINEAR (SILICON TUNER) QFN-24	471J-S21510-0240
		U1T5	SMD IC SI2151-A10 SILICON LABS (DIGITAL AND ANALOG TV TUNER) QFN-24	471J-S21510-0240
Amp	U6A01		SMD IC TPA3138D2PWPR TEXAS(10W CLASS-D AUDIO AMPLIFIER) HTSSOP	4722-T31380-0280
IR Receiver	IR1		SMD IR RECEIVER MODULES 38KHZ SSR438S-TR H-TYPE TAPE TYPE	5300-14438S-0S10
	Q1P8/Q1P9/Q1		SMD TRANSISTOR ME2345A(-30V/-4.2A P-CHANNEL MOSFET) SOT-23	4600-M23450-0S00

### 3.2 Part of Powerboard

Object / part No.	Manufacturer/ trademark	Type / model	Technical data	Standard	Mark(s) of conformity <sup>1)</sup>
AC Inlet (CN1D1)	Yueqing Hongchang Radio Co., Ltd	DB-8-Series	2,5 A, 250 V AC, standard sheet C8, 70°C	IEC/EN 60320-1	VDE (40036226)
Fuse (F0D1)	XC Electronics (Shenzhen) Corp. Ltd.	5H-Serie(s)	3.15A, 250V AC	IEC/EN 60127-3	VDE (40037020)
Thermistor (TH1D1)	Thinking Electronic Industrial Co., Ltd.	SCD-044	4Ω, 4A	EN 60539-1 EN 60730-1	TÜV (R 50351964)
Photocoupler (U0D2)	Lite-On Technology Corporation	LTV-817	Cr, Cl ≥ 6,5mm min., Dti ≥ 0,4mm, 110°C	IEC/EN 60747-5-5	VDE (40015248)
X-Capacitors (CX0D6)	Wuxi Jinlida Electronics Co. Ltd.	MKP series	Max. 0.47µF, 275VAC, 105°C, X2	IEC 60384-14 EN 60384-14	VDE (40041383)
X-Capacitors (CX0D3)	Wuxi Jinlida Electronics Co. Ltd.	MKP series	Max. 0.22µF, 275VAC, 110°C, X2	IEC 60384-14 EN 60384-14	VDE (40041383)
Y-Capacitors (CY0D3, CY0D4, CY0D7)	Yinan Don's Electronic Component Co., Ltd.	CT81	470pF/Min.400VAC, 125°C, Y1	IEC 60384-14; EN 60384-14	VDE (135256)
Y-Capacitors (CY0D8, CY0D9)	Yinan Don's Electronic Component Co., Ltd.	CT81	47pF/Min.250VAC, 125°C, Y1	IEC 60384-14; EN 60384-14	VDE (135256)
Line Filter (LF0D1)	HUIZHOU DE LI ELECTRONIC CO.,LTD	LB321-25529	N1: Φ0,13t*1.0 mm, 50Ts N2: Φ0,13t*1.0 mm, 50Ts	IEC 60065	Tested with appliance
Transformer (T0D1)	Haining Lianfeng Dongjin Electronics Co., Ltd	BCK-30-L0250 8	400uH±10%	IEC 60065	Tested with appliance

## 4. IC General Description

(选取部分对售后有帮助的 IC, 截取关键内容, 不要整份规格书粘贴, 截图要清晰, 放大后能看清楚所有文字, 三合一板需要加入电源 IC 和背光 IC 的介绍)

### 4.1 Main IC:MSD6683BQHT-8-00II



**MSD6683BQH**  
All-In-One DTV Processor  
Preliminary Data Sheet Version 0.1

Attention Please: Under the technology license agreement between MStar and Dolby/DTS/Microsoft/THAT, MStar is obliged not to provide samples that incorporate Dolby/DTS/Microsoft/THAT technology to any third party who is not a qualified licensee of Dolby/DTS/Microsoft/THAT respectively.

#### FEATURES

**MSD6683BQH a single chip iDTV solution that supports channel decoding, MPEG decoding, and media-center functionality enabled by a high performance AV CODEC and CPU.**

Key features includes,

- 1. Combo Front-End Demodulators
- 2. A Multi-Standard A/V Format Decoder
- 3. The MStarACE<sup>PRO</sup> Video Processor
- 4. Home Theater Sound Processor
- 5. Rich internet connectivity and completed digital home network solution
- 6. Dual-stream decoder for 3D contents
- 7. Multi-Purpose CPU for OS and Multimedia
- 8. Security Engine and TEE
- 9. Peripheral and Power Management
- 10. Embedded DRAM
- High Performance Micro-processor
  - ARM Coretex Advanced quad-core CPU
  - 32KB/32KB I/D cache
  - 512KB L2 cache
- Transport Stream De-multiplexer
  - Supports two parallel TS interfaces, with or without sync signal
  - Maximum TS data rate is 140Mbit/s for serial and 24MByte/s for parallel
  - 72 general purpose PID filters and 64 section filters for transport stream de-multiplexer
  - Supports time-shifting function
  - Supports 3DES/DES and AES decrypted cipher engine
- MPEG-2 Video Decoder
  - ISO/IEC 11172-2 MPEG-1 video format decoding
  - ISO/IEC 13818-2 MPEG-2 video MP@HL and HD level
  - Supports resolution up to HDTV (1080p60, 1080i, 720p) and SDTV
  - Supports dual stream decoding for 3D content
- MPEG-4 Video Decoder
  - ISO/IEC 14496-2 MPEG-4 ASP video decoding up to HD level
  - Supports resolutions up to HDTV (1080p@60fps)
  - Supports FLV version1 video format decoding
  - Supports dual stream decoding for 3D content
- AVC/H.264 Video Decoder
  - ITU-T H.264, ISO/IEC 14496-10 (main and high profile up to level 4.2) video decoding
  - Supports resolution up to 1920x1080@60fps
  - Supports bitrate up to 62.5Mbps, the upper limit of level 4.2
  - Supports resolutions for all DVB, ATSC, HDTV, DVD and VCD
  - Supports SVAF 2ES (for Dual Decode)
  - Supports MVC 3D decoding upto 1080p@30fps
- AVS/AVS+ Video Decoder Optional
  - Supports Broadcasting profile, level 6.0.1.08.60 (AVS+)
  - Supports Jizhun profile, level 6.0
  - Supports bitrate up to 50Mbps
  - Supports resolution up to 1920x1080@60fps
  - Supports dual stream decoding
- RealMedia Video Decoder Optional
  - Supports RV8, RV9, RV10 decoders
  - Supports file formats with RM and RMVB
  - Supports maximum resolution up to 1080p@30fps
  - Supports Picture Re-sampling
  - Supports in-loop de-block for B-frame

■ **AVC/H.264 Video Encoder**

- Supports H.264 encoding, Main Profile, level 4.1
- Maximum output frame-rate/resolution: 1920x1080@30fps, 1280x720@60fps
- Supports MVs: 16x16, 16x8, 8x16, 8x4, 4x8, 4x4
- Supports up to quarter-pel
- Supports up to two reference frames

■ **HEVC/H.265 Video Decoder**

- Supports HEVC/H.265 video decoding
- Supports Main/Main-10 profile & Scalable Main/Scalable Main-10 profile, level 4.1, high tier
- Supports 8-bit/10-bit color depth
- Supports resolution up to 1920x1080@60fps
- Supports max bitrate upto 50 Mbps

■ **Hardware PNG / GIF Decoder**

- Supports up to 8192 x 8192 (per channel 8 bits), or 4096 x 8192 (per channel 16 bits) pixel image
- PNG format 1bpp/2bpp/4bpp/8bpp index(palette) mode support
- PNG transparency mode support interlaced / non-interlaced GIF support
- ARGB8888, RGB565, YUV422(YUYV),YUV422(YVYU),gray, gray with alpha output format support

■ **Hardware JPEG Decoder**

- Supports upto 640x480@30fps
- Supports formats: 422/411/420/444/422T
- Supports scaling down ratios: 1/2x1/2, 1/4x1/4, 1/8x1/8
- Supports both color and grayscale pictures
- Supports sequential mode, single scan
- Supports programmable Region of Interest (ROI)
- Following the file header scan the hardware decoder fully handles the decode process

■ **VC-1 Video Decoder Optional**

- Supports SMPTE-421M (VC1 video) decoding up to AP@L3 (2048x1024p60)
- Supports dual stream decoding for 3D content
- Supports upto 1920x1080p60\*2 or 1920x1080p30\*4

■ **NTSC/PAL/SECAM Video Decoder**

- Supports NTSC-M, NTSC-J, NTSC-4.43, PAL (B, D, G, H, M, N, I, Nc), and SECAM standards
- Automatic standard detection
- Motion adaptive 3D comb filter
- Two configurable CVBS & Y/C S-video inputs
- Supports Teletext, Closed Caption (analog CC 608/ analog CC 708/digital CC 608/digital CC 708), V-chip and SCTE

■ **Multi-Standard TV Sound Processor**

- Supports BTSC/A2 demodulation
- Supports NICAM/FM/AM demodulation
- Supports MTS Mode Mono/Stereo/SAP in BTSC mode
- Supports Mono/Stereo/Dual in A2/NICAM mode
- Built-in audio sampling rate conversion (SRC)
- Audio processing for loudspeaker channel, including volume, balance, mute, tone, EQ, virtual stereo/surround and treble/bass controls
- Advanced sound processing options available, for example: Dolby<sup>1</sup>, DTS<sup>2</sup>, DBX-TV<sup>3</sup>
- Supports digital audio format decoding: MPEG-1, MPEG-2 (Layer I/II), MP3, Dolby Digital (AC-3/AC-4) Optional, AAC-LC, HE-AAC, WMA, WMA9 Pro, and Supports Optional Dolby Digital Plus, Dolby Pulse, and MS11/MS12 multistream decoder, including Dolby Digital Encoder for trans-coding streams to Dolby Digital 5.1 (DDCO), DTS M6 multistream decoder/encoder
- Supports Audio Description
- Supports MPEG audio encoding
- Supports time-shifting PVR
- Supports programmable delay for audio/video synchronization

<sup>1</sup> Trademark of Dolby Laboratories

<sup>2</sup> Trademark of DTS, Inc.

Optional Please see Ordering Guide for details.

<sup>3</sup> Trademark of DBX-TV, Inc.



- **Audio Interface**
  - Two L/R audio line-inputs
  - Two L/R outputs for main speakers and additional line-outputs
  - Supports stereo headphone driver
  - I2S digital audio output
  - S/PDIF digital audio output and input
  - Support HDMI receiver ARC function
- **VP8 Video Decoder**
  - Supports Google VP8 decoder
  - Supports resolution up to 1920x1080@60fps
  - Supports maximum bitrate upto 50Mbps
- **VP9 Video Decoder**
  - Supports Google VP9 decoder
  - Supports 4:2:0 subsampling and 8bit/10bit color depth
  - Supports max resolution and frame rate 1920x1080@60fps
  - Supports max birate upto 40Mbps
- **Analog RGB Compliant Input Ports**
  - Two analog ports support up to 1080P
  - Support PC RGB input up to SXGA@75Hz
  - Support HDTV RGB/YPbPr/YCbCr
  - Support Composite Sync and SOG (Sync-on-Green)
  - Automatic color calibration
- **Analog RGB Auto-Configuration & Detection**
  - Auto input signal format and mode detection
  - Auto-tuning function including phasing, positioning, offset, gain
  - Sync Detection for H/V Sync
- **DVI/HDCP/HDMI Compliant Input Ports**
  - Three HDMI/DVI Input ports
  - HDMI 1.4a Compliant
  - MStar iSwitch for fast HDMI switching
  - HDCP 1.4/2.2 Compliant
  - 225MHz @ 1080P 60Hz input with 12-bit Deep-color support
  - Support HDMI CEC
  - Support HDMI 1.4a 3D format input
  - Support HDMI UHD input down-scaling to FHD
  - Support HDMI ARC
  - Single link DVI 1.0 compliant
  - Robust receiver with excellent long-cable support
- **MStar High Performance Video Processor**
  - Support embedded HDCP 1.4 Key
  - Support external HDCP 2.2 key
  - Video Processing Engine
    - Supports up to FHD@60p
    - 10-/12-bit Internal Data Processing
    - Dual-Engine Architecture supporting PIP/PBP
    - Arbitrary Frame Rate Conversion
  - Video Care Technology
    - Video Line Broken Artifact Detection and Removal
  - Fully Programmable Multi-Function Scaling Engine
    - High-Tap Filters with Programmable Parameter
    - An advanced Zoom Algorithm providing Aliasing/Ringing Suppression
    - Nonlinear Video Scaling supports various modes including Panorama
    - Supports Dynamic Scaling for RM, VC-1<sup>Optional</sup>
    - Fully Programmable Zoom Ratios for Up/Down Scaling
    - Independent Horizontal and Vertical Zoom
  - Deinterlacer
    - Motion Compensated Video Deinterlacing with Motion Object Stabilizer
    - Motion Adaptive Deinterlacer
    - Edge-Oriented Deinterlacer with Edge Smoothing and Artifact Removal
    - Automatic 3:2/2:2/M:N Pull-Down Detection and Recovery
  - MStar Genuine 3D
    - Supports Mandatory 3D Format
  - Motion Frame Rate Conversion
    - Supports Frame Repeat Frame Rate Conversion
  - Backlight Technology
    - Programmable Light Spread Profile
    - Content Adaptive LCD Backlight Control

Optional Please see Ordering Guide for details.

- High-Dynamic-Range
  - Supports SMPTE ST-2084 / ST-2086
  - Supports ARIB STD-B67 ( Hybrid Log Gamma )
  - Support ITU-R BT.2100
  - MStar HDR plus Technology with Standard HDR Ready
- Response Time Compensation
  - Supports Overdrive Technology
- MStar Professional PQ Engine
  - UltraClear
    - MPEG Artifact Removal
      - ◊ Adaptive Block Noise Reduction
      - ◊ Advanced Mosquito Noise Cancellation
    - UltraClear Noise Reduction
      - ◊ 3D Motion-Estimation Temporal Filtering
    - 3D Noise Reduction
      - ◊ 3D Temporal Noise Reduction for Lousy Air/Cable Input
      - ◊ Cross-Color Suppression Technology
  - S-Powers
    - Video Enhancement Processor
      - ◊ Advanced 3D Independent Multi-Band Control Sharpness Technology
      - ◊ Advanced Video Enhancement Algorithm provides Aliasing/Ringing Suppression
      - ◊ Supports Chroma Transient Improvement
      - ◊ Content Adaptive Contrast Enhancement with Chroma Compensated
    - Super Resolution
      - ◊ Local Detail Enhancement
      - ◊ Multi-Directional Jagged Compensation Technology
  - MACE
    - MStar Advanced Color Engine
      - ◊ 3D Independent and Accurate Multi-Adaptive Color Manager
      - ◊ Color Stain Removal Technology
- Standard Color Format and Processing
  - ◊ Fully Programmable Input/Output CSC
  - ◊ BT601, BT709, BT2020 (CL/NCL)
  - ◊ xvYCC601, xvYCC709
  - ◊ AdobeRGB, AdobeYCC601
  - ◊ sRGB, sYCC601
  - ◊ Fully Programmable 12-bit RGB Gamma
- Gamut Mapping
  - ◊ Nonlinear/Linear RGB Domain Gamut Mapping
  - ◊ Supports 2D Gamut Mapping
  - ◊ The 3rd Generation 3D Gamut Mapping Engine
- Output Interface
  - Single/Dual link 10 bit LVDS output
  - Supports panel resolution up to Full HD 1920x1080@ 60Hz (LVDS 2ch)
  - Supports dithering options
  - Spread spectrum output frequency for EMI suppression
  - Supports 60Hz 3D polarized panel (line interleave)
  - Supports Cinema output mode
- CVBS Video Encoder
  - Supports all NTSC/PAL TV Standard
  - Stand-alone scaling engine
  - Programmable Hue, Contrast, Brightness
  - Supports TTX/CC/WSS output
- CVBS Video Outputs
  - Allows CVBS output from CVBS video encoder
  - Supports CVBS bypass output
- 2D Graphics Engine
  - Hardware Graphics Engine for responsive interactive applications
  - Supports point draw, line draw, rectangle draw/fill and text draw
  - Supports BitBlt, stretch BitBlt, italic BitBlt, Mirror BitBlt and rotate BitBlt
  - Supports alpha-blending operation
  - Supports source/destination color key and alpha key
  - Supports dither



MSD6683BQH

All-In-One DTV Processor  
Preliminary Data Sheet Version 0.1

- Supports color space conversion and format transformation
- Raster Operation (ROP)
- Supports DFB and Porter-Duff operation
- **3D Graphics Engine**
  - Powerful Multi-core Mali GPU
  - Supports OpenGL ES 1.1/2.0
  - Supports OpenGL VG 1.1
- **VIF Demodulator**
  - Compliant with NTSC M/N, PAL B, G/H, I, D/K, SECAM L/L' standards.
  - Support low IF architecture
  - Audio/Video internal dual-path processor
  - Locking range improvement
- **ATSC/QAM Demodulator**
  - ATSC A/53 compliant 8VSB
  - ITU-T J.83 Annex B, SCTE DVS-031 compliant 64/256QAM receiver
  - 2010 - A74 compliant
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - Impulse-Noise suppression
  - Integrated deinterleaver RAM for Level 1 J = 1 and Level 2 J = 1,2,3,4
  - Supports LIF interfaces
  - I2C repeater for tuner control from backend host controller
- **ISDB-T Demodulator**
  - Compliant with ISDB-T ARIB STD-B31
  - Compliant with ISDB-Tsb ARIB STD-B29
  - Supports all modes defined in ISDB-T spec
  - Supports all guard ratios: 1/4, 1/8, 1/16, 1/32
  - 42ms/channel, excluding AGC time and PLL sync
  - Support LIF interfaces
  - I2C repeater for tuner control from backend host controller
  - Impulse-noise suppression
  - Phase noise compensation
  - Outside-GI performance improvement
  - CNR performance improvement
- **DVB-C Demodulator**
  - Compliant with ITU J.83 Annex A/C DVB-C (EN 300 429)
  - Supports 1-7.2 M Baud symbol rate
  - Automatic blind channel scan (constellation and symbol rate)
  - Supports LIF interfaces
  - IIS performance improvement
- **DVB-T Demodulator**
  - Compliant with DVB-T (ETSI EN 300 744)
  - Nordig 2.2.2, D-book 7.0 compliant
  - Accept low IF inputs in 6, 7, 8MHz channel bandwidths
  - Supports all guard intervals (1/32 to 1/4)
  - Supports all constellations (QPSK, 16-QAM, 64-QAM)
  - Ultra fast automatic blind UHF/VHF channel scan
  - Optimized for SFN channels with pre/post-cursive echoes inside/outside the guard
  - Phase-Noise suppression
  - Impulse-Noise suppression
  - All digital demodulation and timing recovery loops for tracking frequency and clock offset
  - Automatic co-channel and adjacent channel interference suppression
  - CNR performance improvement
  - Outside-GI performance improvement
- **Connectivity**
  - Two USB 2.0 host ports & one USB 2.0 OTG port
  - USB architecture designed for efficient support of external storage devices in conjunction with off air broadcasting
  - Built-in 10/100Mbps Ethernet PHY Interface

**ELECTRICAL SPECIFICATIONS**

## Analog Interface Characteristics

Parameter	Min	Typ	Max	Unit
VIDEO ADC Resolution		10		Bits
DC ACCURACY				
Differential Nonlinearity		0.5		LSB
Integral Nonlinearity		2		LSB
VIDEO ANALOG INPUT				
Input Voltage Range				
RGB & YPbPr(without Sync)		0.7		V p-p
CVBS		1		V p-p
Input Bias Current			1	uA
SWITCHING PERFORMANCE				
Maximum Conversion Rate	170			MSPS
Minimum Conversion Rate			12	MSPS
Hsync Input Frequency	15		200	kHz
PLL Clock Rate	12		170	MHz
PLL Jitter		400		ps p-p
Sampling Phase Tempco		15		ps/°C
DIGITAL INPUTS				
Input Voltage, High ( $V_{IH}$ )	2.0			V
Input Voltage, Low ( $V_{IL}$ )			0.8	V
Input Current, High ( $I_{IH}$ )			-1.0	uA
Input Current, Low ( $I_{IL}$ )			1.0	uA
Input Capacitance		5		pF
DIGITAL OUTPUTS				
Output Voltage, High ( $V_{OH}$ )	VDDP-0.1			V
Output Voltage, Low ( $V_{OL}$ )			0.1	V
VIDEO ANALOG OUTPUT				
CVBS Output				
Output Low		0		V
Output High		1.3		V
AUDIO				
ADC Input		2.8		V p-p
DAC Output		2.8		V p-p
SIF Input Range			0.1	V p-p
Minimum				
Maximum	1.0			V p-p



**MSD6683BQH**  
All-In-One DTV Processor  
Preliminary Data Sheet Version 0.1

Parameter	Min	Typ	Max	Unit
SAR ADC Input	0		3.3	V
FB ADC Input	0		1.2	V
DEMOD ANALOG INTERFACE				
Analog Input Range		1		Vdp-p
Differential Input Impedance	50			Kohm
DEMOD AGC Output Range	0.3		3.3	Volt

Specifications subject to change without notice.

Note: Input full scale is 1.0V, but input range is 0 ~ 3.3V.  
VDDP is 3.3V supply voltages

### Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
3.3V Supply Voltages	V <sub>VDD_33</sub>	3.14	3.3	3.46	V
1.5V Supply Voltages (DDR3)	V <sub>VDD_15</sub>	1.43	1.5	1.57	V
1.22V Supply Voltages (DDR4)	V <sub>VDD_122</sub>	1.19	1.22	1.25	V
2.5V Supply Voltages (DDR4)	V <sub>VDD_25</sub>	2.38	2.5	2.62	V
Core Supply Voltages	V <sub>VDD_core</sub>	0.921	0.95	0.978	V
CPU Supply Voltages	V <sub>VDD_cdu</sub>	0.921	0.95	0.978	V
Ambient Operating Temperature	T <sub>A</sub>	0		70	°C
Junction Temperature	T <sub>J</sub>			125	°C

### Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
3.3V Supply Voltages	V <sub>VDD_33</sub>		3.63	V
1.5V Supply Voltages	V <sub>VDD_15</sub>		1.65	V
1.22V Supply Voltages (DDR4)	V <sub>VDD_122</sub>		1.5	V
2.5V Supply Voltages (DDR4)	V <sub>VDD_25</sub>		3.0	V
Core Supply Voltages	V <sub>VDD_core</sub>		1.26	V
CPU Supply Voltages	V <sub>VDD_cdu</sub>		1.26	V
Input Voltage (5V tolerant inputs)	V <sub>IN5Vtol</sub>		5.3	V
Input Voltage (non 5V tolerant inputs)	V <sub>IN</sub>		V <sub>VDD_33</sub>	V
Storage Temperature	T <sub>STG</sub>	-40	150	°C

Note: Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and does not imply functional operation of the device. Exposure to absolute maximum ratings for extended periods may affect device reliability

## 4.2 Amplifier: TPA3138D2PWPR

### 1 Features

- Wide Supply Range 3.5-V to 14.4-V
  - 2 × 10 W into 6-Ω, 1% THD+N, 12-V Supply
  - 1 × 18.5 W into 4-Ω, 10% THD+N, 12-V Supply
  - THD+N : 0.04% at 1 W, 1 kHz input, 6-Ω
- Longer Battery Life for Portable Applications:
  - 20-mA (12-V) Idle Current in 1SPW Mode
  - >90% Class-D Efficiency
- Reduced Solution Size and Cost:
  - Inductor-Free Operation
  - EN55013 and EN55022 EMC Compliant When No Inductors are Used
  - No External Heatsink Required
- Flexible Audio Solution:
  - Single-ended or Differential Analog Inputs
  - Selectable Gain: 20 dB and 26 dB
  - Pop and Click-Free Startup
- Integrated Protections and Auto Recovery:
  - Pin-to-pin, Pin-to-Ground, and Pin-to-Power Short Circuit Protection
  - Thermal Protection, Undervoltage Protection, and Overvoltage Protection
  - Power Limiter and DC Speaker Protection
- Pin-to-Pin Compatible with TPA3110D2, TPA3136D2 and TPA3136AD2

### 2 Applications

- Televisions and Monitors
- Bluetooth® Speakers and Wireless Speakers
- Audio Amplifiers in Smart Appliance
- Audio Speakers in Internet of Things
- Consumer Audio Equipment

### 3 Description

The TPA3138D2 is a 10-W/ch, high-efficiency, low-idle-current Class-D stereo audio amplifier. It can drive stereo speakers with a load as low as 3.2-Ω. In the 1SPW mode, it consumes a low idle current of only 21-mA (12-V) and can operate down to 3.5-V, allowing for longer audio play and improved thermal performance in bluetooth speakers, battery-powered appliances and other power-sensitive applications.

Advanced EMI Suppression with Spread Spectrum Control enables the use of inexpensive ferrite bead filters while meeting EMC requirements for system cost reduction.

To further simplify the design, the TPA3138D2 integrates essential protection features including undervoltage, overvoltage, power limit, short circuit, overtemperature, as well as DC speaker protection. All of these protections come with automatic recovery.

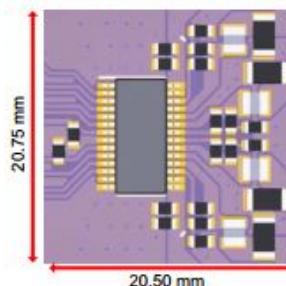
Customers can leverage every TPA3138D2 feature in existing designs as it is fully pin-to-pin compatible to TI's TPA3110D2, TPA3136D2 and TPA3136AD2.

### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPA3138D2	HTSSOP (28)	9.70 mm × 4.40 mm

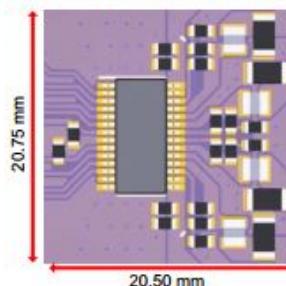
(1) For all available packages, see the orderable addendum at the end of the datasheet.

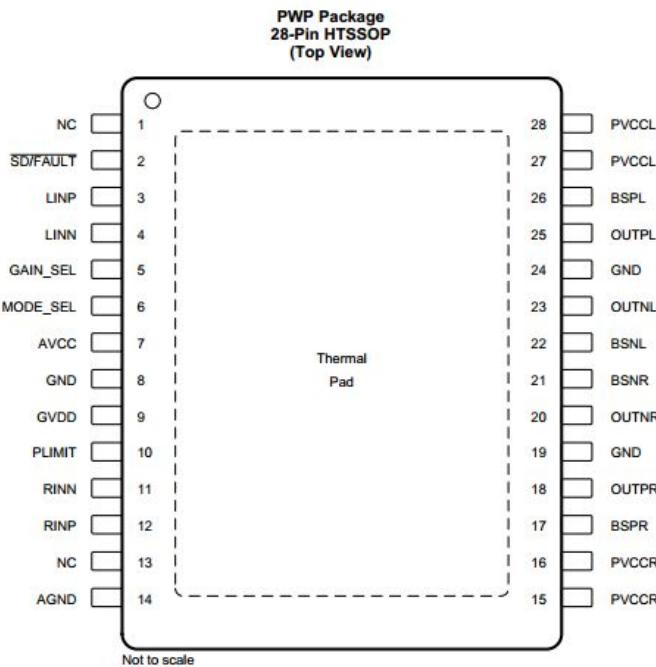
### TPA3138 Layout with Ferrite Beads



Simplified Schematic

### TPA3138 Layout with Ferrite Beads



**Pin Functions**

PIN		I/O/P <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
NC	1	-	No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
SDFAULT	2	IO	TTL logic levels with compliance to AVCC. Shutdown logic input for audio amp (LOW , outputs Hi-Z; HIGH , outputs enabled). General fault reporting including Over-Temp, Over-Current, DC Detect. SDFAULT= High, normal operation, SDFAULT= Low, fault condition Device will auto-recover once the OT/OC/DC Fault has been removed.
LINP	3	I	Positive audio input for left channel. Biased at 2.5 V. Connect to GND for PBTL mode.
LINN	4	I	Negative audio input for left channel. Biased at 2.5 V. Connect to GND for PBTL mode.
GAIN_SEL	5	I	Gain select least significant bit. TTL logic levels with compliance to AVDD. Low = 20 dB Gain, High = 26 dB Gain, Floating = 26 dB Gain.

PIN		I/O/P <sup>(1)</sup>	DESCRIPTION
NAME	NO.		
MODE_SEL	6	I	Mode select least significant bit. TTL logic levels with compliance to AVDD. Low = BD Mode/UV Threshold = 7.5 V, High = Low-Idle-Current 1SPW Mode/UV Threshold = 3.4V, Floating = Low-Idle-Current 1SPW Mode/UV threshold = 3.4V
AVCC	7	P	Analog supply.
GND	8	-	Analog signal ground.
GVDD	9	O	FET gate drive supply. Nominal voltage is 5 V.
PLIMIT	10	I	Power limiter level control. Connect a resistor divider from GVDD to GND to set power limit. Connect directly to GVDD for no power limit.
RINN	11	I	Negative audio input for right channel. Biased at 2.5 V.
RINP	12	I	Positive audio input for right channel. Biased at 2.5 V.
NC	13	-	No Connect Pin. Can be shorted to PVCC or shorted to GND or left open.
AGND	14	-	Analog signal ground. Connect to the thermal pad.
PVCCR	15, 16	P	Power supply for right channel H-bridge. Right channel and left channel power supply inputs are connected internally.
BSPR	17	P	Bootstrap supply (BST) for right channel, positive high-side FET.
OUTPR	18	O	Class-D H-bridge positive output for right channel.
GND	19	-	Power ground for the H-bridges.
OUTNR	20	O	Class-D H-bridge negative output for right channel.
BSNR	21	P	Bootstrap supply (BST) for right channel, negative high-side FET.
BSNL	22	P	Bootstrap supply (BST) for left channel, negative high-side FET.
OUTNL	23	O	Class-D H-bridge negative output for left channel.
GND	24	-	Power ground for the H-bridges.
OUTPL	25	O	Class-D H-bridge positive output for left channel.
BSPL	26	P	Bootstrap supply (BST) for left channel, positive high-side FET.
PVCL	27, 28	P	Power supply for left channel H-bridge. Right channel and left channel power supply inputs are connected internally.
Thermal Pad		-	Connect to GND for best thermal and electrical performance

## 4.3 RF controller: SI2151-A10

### Features

- Worldwide hybrid TV tuner
  - Analog TV: NTSC, PAL/SECAM
  - Digital TV: ATSC/QAM, DVB-T2/T/C2/C, ISDB-T/C, DTMB
  - 1.7 MHz, 6 MHz, 7 MHz, 8 MHz, and 10 MHz channel bandwidths
  - 42-1002 MHz frequency range
- Industry-leading margin to A/74, NorDig, DTG, ARIB, EN55020, OpenCable™, DTMB
- Lowest BOM for a hybrid TV tuner
  - No balun, SAW filters, or external inductors required
  - Increased ESD protection on 4 pins
- Best-in-class real-world reception
  - Lowest phase noise
  - High Wi-Fi and LTE immunity
- Low power consumption
  - 3.3 V and 1.8 V power supplies
  - Integrated 1.8 V LDO for 3.3 V single-supply operation
- Integrated power-on reset circuit
- Standard CMOS process
- 3x3 mm, 24-pin QFN package
- RoHS compliant



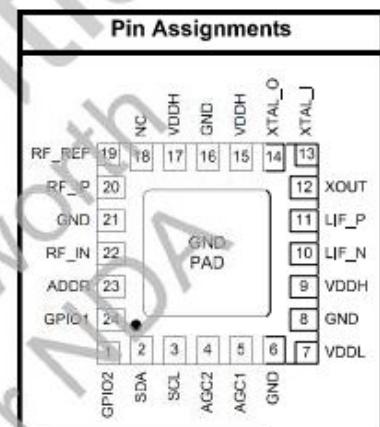
**Ordering Information:**  
See page 26.

### Applications

- Hybrid 1/2-NIM tuner module
- Hybrid PVR and BDR recorder
- IDTV (Integrated Digital TV)
- PC-TV accessories
- Hybrid terrestrial and cable STB

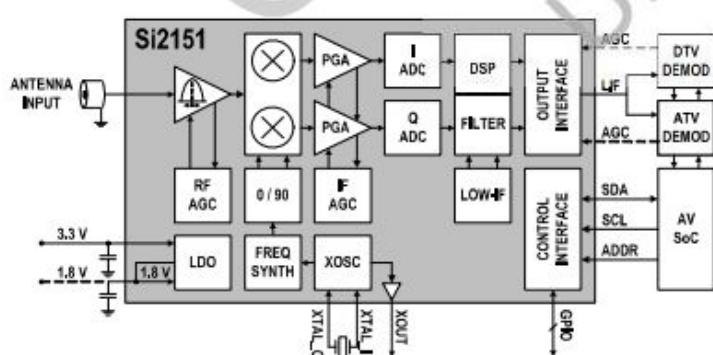
### Description

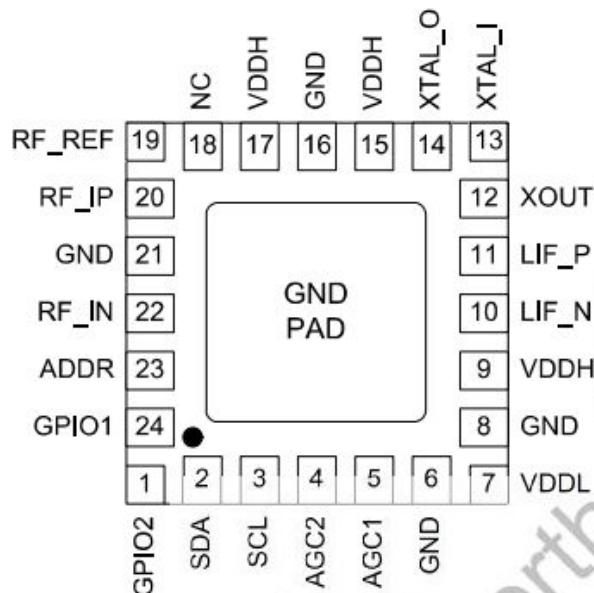
The Si2151 is Silicon Labs' sixth-generation hybrid TV tuner supporting all worldwide terrestrial and cable TV standards. Requiring no external balun, SAW filters, wirewound inductors or LNAs, the Si2151 offers the lowest-cost BOM for a hybrid TV tuner. Also included are an integrated power-on reset circuit and an option for single power supply operation. As with prior-generation Silicon Labs TV tuners, the Si2151 maintains very high linearity and low noise to deliver superior picture quality and a higher number of received stations when compared to other silicon tuners. The Si2151 offers increased immunity to WiFi and LTE interference, eliminating the need for external filtering. For the best performance with next-generation digital TV standards, such as DVB-T2/C2, the Si2151 delivers industry-leading phase noise performance.



Patents pending

### Functional Block Diagram





Pin Number(s)	Name	I/O	Description
1*	GPIO2	I/O	General purpose input/output #1
2	SDA	I/O	I <sup>2</sup> C data input/output
3	SCL	I	I <sup>2</sup> C clock input
4*	AGC2	I	LIF output amplitude control input #2
5*	AGC1	I	LIF output amplitude control input #1
6	GND	S	Ground
7	VDDL	S	Low supply voltage, 1.8 V (leave caps connected for single supply case)
8	GND	S	Ground
9	VDDH	S	High supply voltage, 3.3 V
10	LIF_N	O	Negative LIF differential output to SoC or DTV/ATV demodulator
11*	LIF_P	O	Positive LIF differential output to SoC or DTV/ATV demodulator
12	XOUT	O	Output reference clock to secondary tuner or receiver
13	XTAL_I	I	Crystal pin 1 (or RCLK input driven by XOUT of another tuner or receiver)
14	XTAL_O	O	Crystal pin 2 (leave floating if XTAL_I is driven by XOUT of another tuner or receiver)
15	VDDH	S	High supply voltage, 3.3 V
16	GND	S	Ground
17	VDDH	S	High supply voltage, 3.3 V
18*	NC	NC	No connect
19	RF_REF	O	RF reference voltage output
20	RF_IP	I	RF input (positive)
21	GND	S	Ground
22	RF_IN	I	RF input (negative)
23	ADDR	I	I <sup>2</sup> C address select
24*	GPIO1	I/O	General purpose input/output #1

\*Note: Pin should be left floating if unused.

## 4.4 Earphone AMP : NA

## 4.5 5V\_STB/3.3V\_STB : MP1652GTF-Z

### DESCRIPTION

The MP1652 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution that achieves 2A of continuous output current with excellent load and line regulation over a wide input range. The MP1652 has synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1652 requires a minimal number of readily available, standard, external components and is available in a space-saving SOT563 package.

### FEATURES

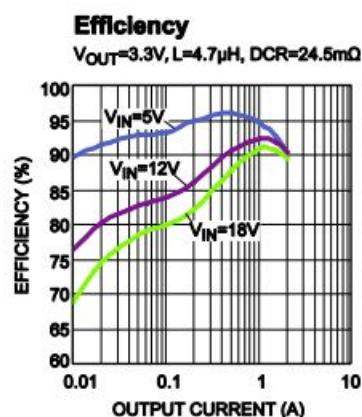
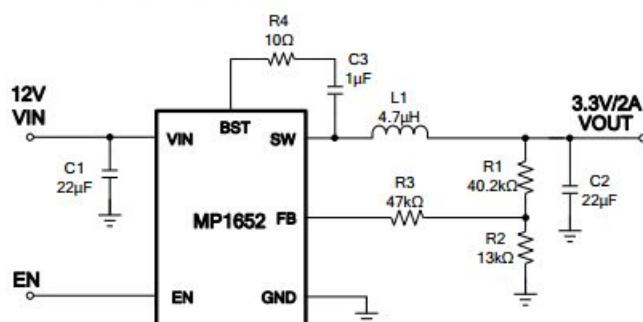
- Wide 4.2V to 18V Operating Input Range
- 130mΩ/65mΩ Low  $R_{DS(ON)}$  Internal Power MOSFETs
- 190µA Low  $I_Q$
- High-Efficiency Synchronous Mode Operation
- Power-Save Mode at Light Load
- Fast Load Transient Response
- 800kHz Switching Frequency
- Internal Soft Start
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a SOT563 Package

### APPLICATIONS

- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

### TYPICAL APPLICATION

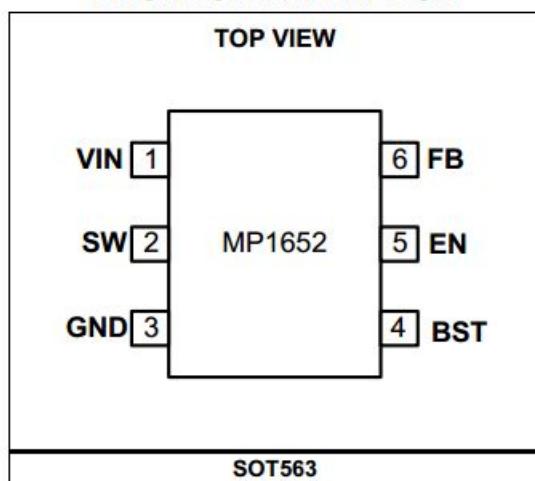


**TOP MARKING****ATUY****LLL**

ATU: Product code of MP1652GTF

Y: Year code

LLL: Lot number

**PACKAGE REFERENCE**

**ELECTRICAL CHARACTERISTICS**VIN = 12V, TJ = -40°C to +125°C<sup>(5)</sup>, typical value is tested at TJ = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I <sub>N</sub>	V <sub>EN</sub> = 0V			10	µA
Supply current (quiescent)	I <sub>Q</sub>	T <sub>J</sub> = -40°C to +125°C, V <sub>EN</sub> = 2V, V <sub>FB</sub> = 0.85V	0.15	0.19	0.3	mA
		T <sub>J</sub> = +25°C, V <sub>EN</sub> = 2V, V <sub>FB</sub> = 0.85V	0.16	0.19	0.23	
HS switch on resistance	H <sub>S</sub> RDS-ON	V <sub>BST-SW</sub> = 3.3V		130		mΩ
LS switch on resistance	L <sub>S</sub> RDS-ON			65		mΩ
Switch leakage	S <sub>W</sub> LKG	V <sub>EN</sub> = 0V, V <sub>SW</sub> = 12V			10	µA
Valley current limit	I <sub>LIMIT</sub>	V <sub>OUT</sub> = 0V	1.8	2.4	3.8	A
ZCD	I <sub>ZCD</sub>	V <sub>OUT</sub> = 3.3V, L <sub>O</sub> = 4.7µH, I <sub>OUT</sub> = 0A	-150	-20	150	mA
Oscillator frequency	f <sub>SW</sub>	V <sub>FB</sub> = 0.75V	600	800	1000	kHz
Minimum on time <sup>(6)</sup>	T <sub>ON_MIN</sub>			45		ns
Minimum off time <sup>(6)</sup>	T <sub>OFF_MIN</sub>			180		ns
Feedback voltage	V <sub>REF</sub>	T <sub>J</sub> = +25°C	795	807	819	mV
Feedback current	I <sub>FB</sub>			10	100	nA
FB UV threshold (H to L)	V <sub>UV_th</sub>	Hiccup entry		75%		V <sub>REF</sub>
Hiccup duty cycle <sup>(6)</sup>	D <sub>HICUP</sub>			25		%
EN rising threshold	V <sub>EN_RISING</sub>		1.14	1.2	1.26	V
EN hysteresis	V <sub>EN_HYS</sub>			100		mV
EN input current	I <sub>EN</sub>	V <sub>EN</sub> = 2V		2		µA
VIN under-voltage lockout threshold rising	I <sub>NUV_Vth</sub>		3.7	4.1	4.18	V
VIN under-voltage lockout threshold hysteresis	I <sub>NUV_HYS</sub>			330		mV
Soft-start period	T <sub>SS</sub>		1	1.4	2	ms
Thermal shutdown <sup>(6)</sup>	T <sub>SD</sub>			150		°C
Thermal hysteresis <sup>(6)</sup>	T <sub>SD_HYS</sub>			20		°C

## NOTES:

5) Not tested in production. Guaranteed by over-temperature correlation.

6) Guaranteed by design and engineering sample characterization.

**MPS<sup>®</sup> MP1652 – 18V, 2A, 800KHZ, SYNC, STEP-DOWN CONVERTER W/ INTERNAL MOSFETS****PIN FUNCTIONS**

Package Pin #	Name	Description
1	VIN	<b>Supply voltage.</b> The MP1652 operates from a 4.2V to 18V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	<b>Switch output.</b> Connect SW using a wide PCB trace.
3	GND	<b>System ground.</b> GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND to ground with copper traces and vias.
4	BST	<b>Bootstrap.</b> Connect a 1µF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	<b>Enable.</b> Drive EN high to enable the MP1652. For automatic start-up, connect EN to VIN with a 100kΩ pull-up resistor.
6	FB	<b>Feedback.</b> Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 600mV to prevent current limit runaway during a short-circuit fault.

## 4.6 1.0V\_VDDC : MP1653GTF-Z

### DESCRIPTION

The MP1653 is a fully integrated, high-frequency, synchronous, rectified, step-down, switch-mode converter with internal power MOSFETs. It offers a very compact solution that achieves 3A of continuous output current with excellent load and line regulation over a wide input range. The MP1653 has synchronous mode operation for higher efficiency over the output current load range.

Constant-on-time control operation provides very fast transient response, easy loop design, and very tight output regulation.

Full protection features include short-circuit protection (SCP), over-current protection (OCP), under-voltage protection (UVP), and thermal shutdown.

The MP1653 requires a minimal number of readily available, standard, external components and is available in a space-saving SOT563 (1.6mmx1.6mm) package.

### FEATURES

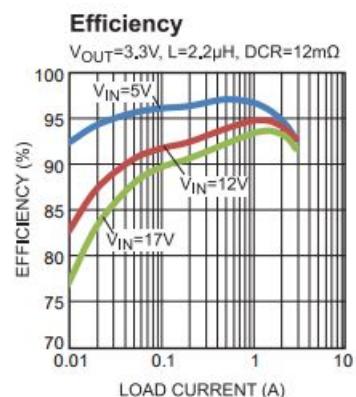
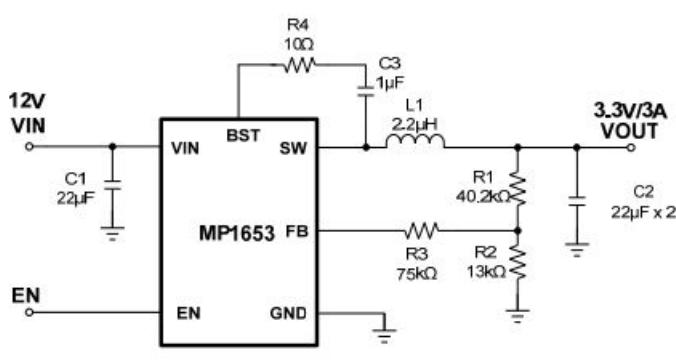
- Wide 4.2V to 17V Operating Input Range
- 70mΩ/40mΩ Low  $R_{DS(ON)}$  Internal Power MOSFETs
- 200µA Low  $I_Q$
- High-Efficiency Synchronous Mode Operation
- Power-Save Mode at Light Load
- Fast Load Transient Response
- 800kHz Switching Frequency
- Internal Soft Start
- Over-Current Protection (OCP) and Hiccup
- Thermal Shutdown
- Output Adjustable from 0.8V
- Available in a SOT563 (1.6mmx1.6mm) Package

### APPLICATIONS

- Security Cameras
- Digital Set-Top Boxes
- Flat-Panel Televisions and Monitors
- General Purposes

All MPS parts are lead-free, halogen-free, and adhere to the RoHS directive. For MPS green status, please visit the MPS website under Quality Assurance. "MPS" and "The Future of Analog IC Technology" are registered trademarks of Monolithic Power Systems, Inc.

### TYPICAL APPLICATION

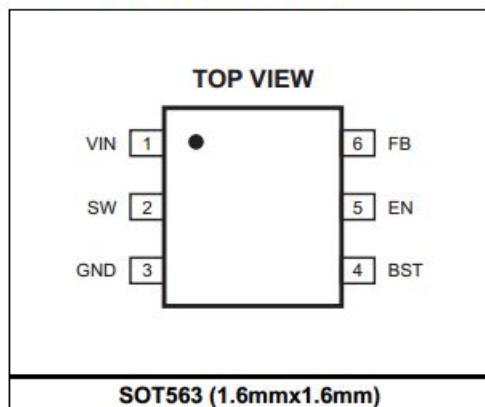


**TOP MARKING****AUCY****LLL**

AUC: Product code of MP1653GTF

Y: Year code

LLL: Lot number

**PACKAGE REFERENCE**

**ELECTRICAL CHARACTERISTICS**VIN = 12V, TJ = -40°C to +125°C<sup>(6)</sup>, typical value is tested at TJ = +25°C, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
Supply current (shutdown)	I <sub>IN</sub>	V <sub>EN</sub> = 0V			10	µA
Supply current (quiescent)	I <sub>Q</sub>	V <sub>EN</sub> = 2V, V <sub>FB</sub> = 0.85V	170	200	240	µA
HS switch-on resistance	HS <sub>RDS(ON)</sub>	V <sub>BST-SW</sub> = 3.3V		70		mΩ
LS switch-on resistance	LS <sub>RDS(ON)</sub>			40		mΩ
Switch leakage	SW <sub>LKG</sub>	V <sub>EN</sub> = 0V, V <sub>SW</sub> = 12V			10	µA
Valley current limit	I <sub>LIMIT</sub>	V <sub>OUT</sub> = 0V	2.7	4	5.8	A
ZCD	I <sub>ZCD</sub>	V <sub>OUT</sub> = 3.3V, Lo = 2.2µH, I <sub>OUT</sub> = 0A	-250	20	250	mA
Oscillator frequency	f <sub>SW</sub>	V <sub>FB</sub> = 0.75V	600	800	1000	kHz
Minimum on time <sup>(7)</sup>	T <sub>ON MIN</sub>			45		ns
Minimum off time <sup>(7)</sup>	T <sub>OFF MIN</sub>			180		ns
Feedback voltage	V <sub>REF</sub>	TJ = +25°C	790	802	814	mV
Feedback current	I <sub>FB</sub>			10	100	nA
FB UV threshold (H to L)	V <sub>UV th</sub>	Hiccup entry		75%		V <sub>REF</sub>
Hiccup duty cycle <sup>(7)</sup>	D <sub>Hiccup</sub>			25		%
EN rising threshold	V <sub>EN RISING</sub>		1.14	1.2	1.26	V
EN hysteresis	V <sub>EN HYS</sub>			100		mV
EN input current	I <sub>EN</sub>	V <sub>EN</sub> = 2V		2		µA
VIN under-voltage lockout threshold rising	INUV <sub>Vth</sub>		3.7	4	4.18	V
VIN under-voltage lockout threshold hysteresis	INUV <sub>HYS</sub>			330		mV
Soft-start period	T <sub>SS</sub>		1.6	2.5	3	ms
Thermal shutdown <sup>(7)</sup>	TSD			150		°C
Thermal hysteresis <sup>(7)</sup>	TSD <sub>HYS</sub>			20		°C

**NOTES:**

- 6) Not tested in production. Guaranteed by over-temperature correlation.  
 7) Guaranteed by design and engineering sample characterization.

**PIN FUNCTIONS**

Package Pin #	Name	Description
1	VIN	<b>Supply voltage.</b> The MP1653 operates from a 4.2V to 17V input rail. A capacitor (C1) is required to decouple the input rail. Connect VIN using a wide PCB trace.
2	SW	<b>Switch output.</b> Connect SW using a wide PCB trace.
3	GND	<b>System ground.</b> GND is the reference ground of the regulated output voltage. GND requires extra care during PCB layout. Connect GND to ground with copper traces and vias.
4	BST	<b>Bootstrap.</b> Connect a 1µF BST capacitor and a resistor between SW and BST to form a floating supply across the high-side switch driver.
5	EN	<b>Enable.</b> Drive EN high to enable the MP1653. For automatic start-up, connect EN to VIN with a 100kΩ pull-up resistor.
6	FB	<b>Feedback.</b> Connect FB to the tap of an external resistor divider from the output to GND to set the output voltage. The frequency foldback comparator lowers the oscillator frequency when the FB voltage drops below 600mV to prevent current limit runaway during a short-circuit fault.

## 4.7 1.5V\_DDR : TPS562201DDCR

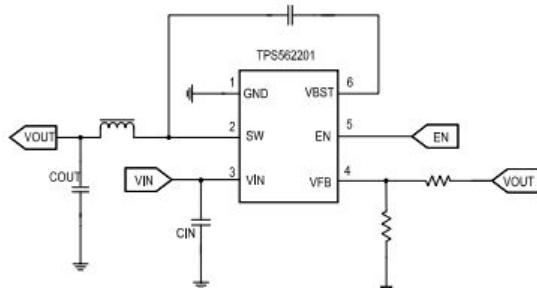
### 1 Features

- TPS562201 and TPS562208 2-A Converter Integrated 140-mΩ and 84-mΩ FETs
- D-CAP2™ Mode Control With Fast Transient Response
- Input Voltage Range: 4.5 V to 17 V
- Output Voltage Range: 0.76 V to 7 V
- Pulse-Skip Mode (TPS562201) or Continuous Current Mode (TPS562208)
- 580-kHz Switching Frequency
- Low Shutdown Current Less than 10 µA
- 2% Feedback Voltage Accuracy (25°C)
- Startup from Pre-Biased Output Voltage
- Cycle-by-Cycle Overcurrent Limit
- Hiccup-Mode Overcurrent Protection
- Non-Latch UVLP and TSD Protections
- Fixed Soft-Start: 1.0 ms

### 2 Applications

- Digital TV Power Supply
- High Definition Blu-ray™ Disc Players
- Networking Home Terminal
- Digital Set-Top Box (STB)
- Surveillance

### Simplified Schematic



### 3 Description

The TPS562201 and TPS562208 are simple, easy-to-use, 2-A synchronous step-down converters in SOT-23 package.

The devices are optimized to operate with minimum external component counts and also optimized to achieve low standby current.

These switch mode power supply (SMPS) devices employ D-CAP2 mode control providing a fast transient response and supporting both low equivalent series resistance (ESR) output capacitors such as specialty polymer and ultra-low ESR ceramic capacitors with no external compensation components.

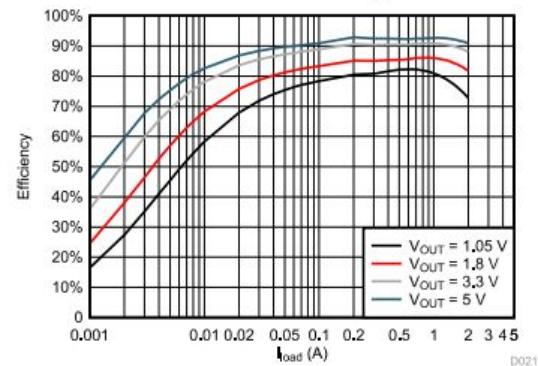
The TPS562201 operates in pulse skip mode, which maintains high efficiency during light load operation. The TPS562201 and TPS562208 are available in a 6-pin 1.6 × 2.9 (mm) SOT (DDC) package and specified from -40°C to 125°C of junction temperature.

### Device Information<sup>(1)</sup>

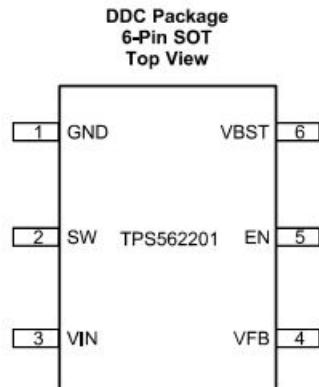
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS562201	SOT (6)	1.60 mm × 2.90 mm
TPS562208		

(1) For all available packages, see the orderable addendum at the end of the data sheet.

### TPS562201 Efficiency



## 5 Pin Configuration and Functions



**Pin Functions**

PIN		DESCRIPTION
NAME	NO.	
GND	1	Ground pin Source terminal of low-side power NFET as well as the ground terminal for controller circuit. Connect sensitive VFB to this GND at a single point.
SW	2	Switch node connection between high-side NFET and low-side NFET.
VIN	3	Input voltage supply pin. The drain terminal of high-side power NFET.
VFB	4	Converter feedback input. Connect to output voltage with feedback resistor divider.
EN	5	Enable input control. Active high and must be pulled up to enable the device.
VBST	6	Supply input for the high-side NFET gate drive circuit. Connect 0.1- $\mu$ F capacitor between VBST and SW pins.

## 6.5 Electrical Characteristics

$T_J = -40^\circ\text{C}$  to  $125^\circ\text{C}$ ,  $V = 12 \text{ V}$  (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
<b>SUPPLY CURRENT</b>					
$I_{VIN}$	Operating – non-switching supply current	$V_{IN}$ current, $EN = 5 \text{ V}$ , $V_{FB} = 0.8 \text{ V}$	TPS562201	380	520
			TPS562208	590	750
$I_{VINSNDN}$	Shutdown supply current	$V_{IN}$ current, $EN = 0 \text{ V}$		1	10
<b>LOGIC THRESHOLD</b>					
$V_{ENH}$	EN high-level input voltage	EN	1.6		V
$V_{ENL}$	EN low-level input voltage	EN		0.8	V
$R_{EN}$	EN pin resistance to GND	$V_{EN} = 12 \text{ V}$	225	400	$\text{k}\Omega$
<b>VFB VOLTAGE AND DISCHARGE RESISTANCE</b>					
$V_{FBTH}$	VFB threshold voltage	$V_O = 1.05 \text{ V}$ , $I_O = 10 \text{ mA}$ , Eco-mode™ operation	774		mV
$I_{VFB}$	VFB threshold voltage	$V_O = 1.05 \text{ V}$ , continuous mode operation	749	768	787
$I_{VFB}$	VFB input current	$V_{FB} = 0.8 \text{ V}$	0	$\pm 0.1$	$\mu\text{A}$
<b>MOSFET</b>					
$R_{DS(on)h}$	High-side switch resistance	$T_A = 25^\circ\text{C}$ , $V_{BST} - SW = 5.5 \text{ V}$	140		$\text{m}\Omega$
$R_{DS(on)l}$	Low-side switch resistance	$T_A = 25^\circ\text{C}$	84		$\text{m}\Omega$
<b>CURRENT LIMIT</b>					
$I_{ocl}$	Current limit	DC current, $V_{OUT} = 1.05 \text{ V}$ , $L_1 = 2.2 \mu\text{H}$	2.4	3.2	4.0
<b>THERMAL SHUTDOWN</b>					
$T_{SDN}$	Thermal shutdown threshold <sup>(1)</sup>	Shutdown temperature	160		$^\circ\text{C}$
		Hysteresis	25		
<b>ON-TIME TIMER CONTROL</b>					
$t_{OFF(MIN)}$	Minimum off time	$V_{FB} = 0.5 \text{ V}$	220	310	ns
<b>SOFT START</b>					
$t_{ss}$	Soft-start time	Internal soft-start time	1.0		ms
Frequency					
$F_{sw}$	Switching frequency	$V_{IN} = 12 \text{ V}$ , $V_O = 1.05 \text{ V}$ , FCCM mode	580		kHz
<b>OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION</b>					
$V_{UVP}$	Output UVP threshold	Hiccup detect ( $H > L$ )	65%		
$T_{HICCUP_WAI}$	Hiccup wait time		1.8		ms
$T_{HICCUP_RE}$	Hiccup time before restart		15		ms
<b>UVLO</b>					
UVLO	UVLO threshold	Wake up VIN voltage	4.0	4.3	V
		Shut down VIN voltage	3.3	3.6	
		Hysteresis VIN voltage	0.4		

## 4.8 EMMC : THGBMNG5D1LBAIL

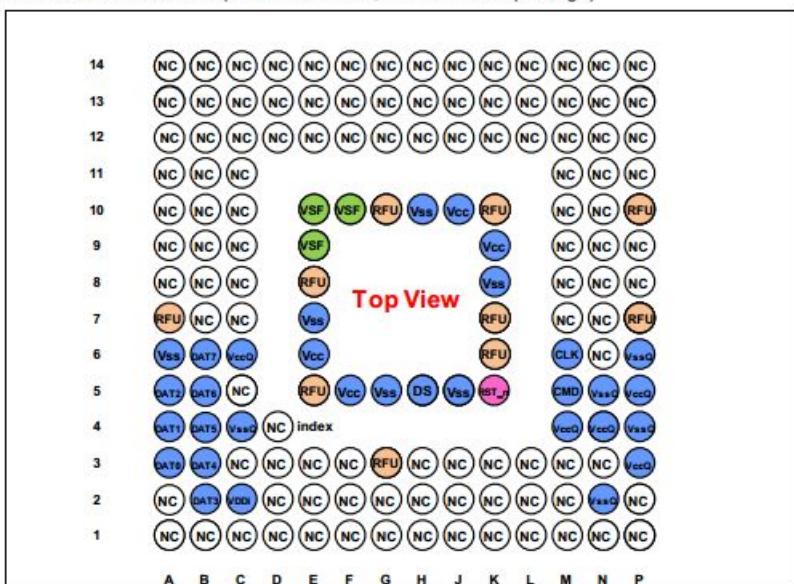
### FEATURES

#### **THGBMNG5D1LBAIL Interface**

THGBMNG5D1LBAIL has the JEDEC/MMCA Version 5.0 interface with 1-I/O, 4-I/O and 8-I/O mode.

#### **Pin Connection**

P-WFBGA153-1113-0.50 (11.5mm x 13mm, H0.8mm max. package)



Pin Number	Name	Pin Number	Name	Pin Number	Name	Pin Number	Name
A3	DAT0	C2	VDDi	J5	Vss	N4	VccQ
A4	DAT1	C4	VssQ	J10	Vcc	N5	VssQ
A5	DAT2	C6	VccQ	K5	RST_n	P3	VccQ
A6	Vss	E6	Vcc	K8	Vss	P4	VssQ
B2	DAT3	E7	Vss	K9	Vcc	P5	VccQ
B3	DAT4	F5	Vcc	M4	VccQ	P6	VssQ
B4	DAT5	G5	Vss	M5	CMD		
B5	DAT6	H5	DS	M6	CLK		
B6	DAT7	H10	Vss	N2	VssQ		

NC: No Connect, shall be connected to ground or left floating.

RFU: Reserved for Future Use, shall be left floating for future use.

VSF: Vendor Specific Function, shall be left floating.

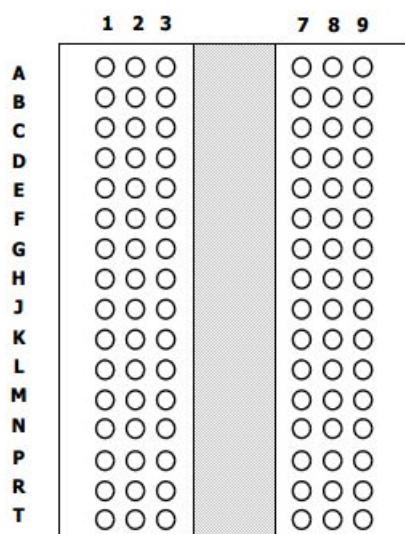
## 4.9 DDR : H5TQ2G63GFR-TEC

### FEATURES

- VDD=VDDQ=1.5V +/- 0.075V
- Fully differential clock inputs (CK,  $\overline{CK}$ ) operation
- Differential Data Strobe (DQS,  $\overline{DQS}$ )
- On chip DLL align DQ, DQS and  $\overline{DQS}$  transition with CK transition
- DM masks write data-in at the both rising and falling edges of the data strobe
- All addresses and control inputs except data, data strobes and data masks latched on the rising edges of the clock
- Programmable CAS latency 5, 6, 7, 8, 9, 10, 11, 12, 13 and 14 supported
- Programmable additive latency 0, CL-1, and CL-2 supported
- Programmable CAS Write latency (CWL) = 5, 6, 7, 8 9 and 10
- Programmable burst length 4/8 with both nibble sequential and interleave mode
- BL switch on the fly
- 8banks
- Average Refresh Cycle (Tcase 0 °C~95 °C)
  - 7.8  $\mu$ s at 0°C ~ 85 °C
  - 3.9  $\mu$ s at 85°C ~ 95 °C
- Commercial Temperature( 0°C ~ 95 °C)
- Industrial Temperature( -40°C ~ 95 °C)
- JEDEC standard 78ball FBGA(x8), 96ball FBGA(x16)
- Driver strength selected by EMRS
- Dynamic On Die Termination supported
- Asynchronous RESET pin supported
- ZQ calibration supported
- TDQS (Termination Data Strobe) supported (x8 only)
- Write Levelization supported
- 8 bit pre-fetch

**x16 Package Ball out (Top view): 96ball FBGA Package**

	1	2	3	4	5	6	7	8	9	
A	VDDQ	DQU5	DQU7				DQU4	VDDQ	VSS	A
B	VSSQ	VDD	VSS				DQSU	DQU6	VSSQ	B
C	VDDQ	DQU3	DQU1				DQSU	DQU2	VDDQ	C
D	VSSQ	VDDQ	DMU				DQU0	VSSQ	VDD	D
E	VSS	VSSQ	DQL0				DML	VSSQ	VDDQ	E
F	VDDQ	DQL2	DQSL				DQL1	DQL3	VSSQ	F
G	VSSQ	DQL6	DQSL				VDD	VSS	VSSQ	G
H	VREFDQ	VDDQ	DQL4				DQL7	DQL5	VDDQ	H
J	NC	VSS	RAS				CK	VSS	NC	J
K	ODT	VDD	CAS				CK	VDD	CKE	K
L	NC	CS	WE				A10/AP	ZQ	NC	L
M	VSS	BA0	BA2				NC	VREFCA	VSS	M
N	VDD	A3	A0				A12/BC	BA1	VDD	N
P	VSS	A5	A2				A1	A4	VSS	P
R	VDD	A7	A9				A11	A6	VDD	R
T	VSS	RESET	A13				NC	A8	VSS	T
	1	2	3	4	5	6	7	8	9	



(Top View: See the balls through the Package)

- Populated ball
- + Ball not populated

### Pin Functional Description

Symbol	Type	Function
CK, $\overline{CK}$	Input	Clock: CK and $\overline{CK}$ are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of $\overline{CK}$ .
CKE, (CKE0), (CKE1)	Input	Clock Enable: CKE HIGH activates, and CKE Low deactivates, internal clock signals and device input buffers and output drivers. Taking CKE Low provides Precharge Power-Down and Self-Refresh operation (all banks idle), or Active Power-Down (row Active in any bank). CKE is asynchronous for Self-Refresh exit. After VREFCA and VREFDQ have become stable during the power on and initialization sequence, they must be maintained during all operations (including Self-Refresh). CKE must be maintained high throughout read and write accesses. Input buffers, excluding CK, $\overline{CK}$ , ODT and CKE, are disabled during power-down. Input buffers, excluding CKE, are disabled during Self-Refresh.
$\overline{CS}$ , ( $\overline{CS0}$ ), ( $\overline{CS1}$ ), ( $\overline{CS2}$ ), ( $\overline{CS3}$ )	Input	Chip Select: All commands are masked when $\overline{CS}$ is registered HIGH. $\overline{CS}$ provides for external Rank selection on systems with multiple Ranks. $\overline{CS}$ is considered part of the command code.
ODT, (ODT0), (ODT1)	Input	On Die Termination: ODT (registered HIGH) enables termination resistance internal to the DDR3 SDRAM. When enabled, ODT is only applied to each DQ, DQS, $\overline{DQS}$ and DM/TDQS, NU/TDQS (When TDQS is enabled via Mode Register A11=1 in MR1) signal for x4/x8 configurations. For x16 configuration, ODT is applied to each DQ, DQSU, $\overline{DQSU}$ , DQSL, $\overline{DQSL}$ , DMU, and DML signal. The ODT pin will be ignored if MR1 is programmed to disable ODT.
$\overline{RAS}$ , $\overline{CAS}$ , $\overline{WE}$	Input	Command Inputs: $\overline{RAS}$ , $\overline{CAS}$ and $\overline{WE}$ (along with $\overline{CS}$ ) define the command being entered.
DM, (DMU), (DML)	Input	Input Data Mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH coincident with that input data during a Write access. DM is sampled on both edges of DQS. For x8 device, the function of DM or TDQS/ $\overline{TDQS}$ is enabled by Mode Register A11 setting in MR1.
BA0 - BA2	Input	Bank Address Inputs: BA0 - BA2 define to which bank an Active, Read, Write or Precharge command is being applied. Bank address also determines if the mode register or extended mode register is to be accessed during a MRS cycle.
A0 - A15	Input	Address Inputs: Provide the row address for Active commands and the column address for Read/Write commands to select one location out of the memory array in the respective bank. (A10/AP and A12/BC have additional functions, see below). The address inputs also provide the op-code during Mode Register Set commands.
A10 / AP	Input	Auto-precharge: A10 is sampled during Read/Write commands to determine whether Autoprecharge should be performed to the accessed bank after the Read/Write operation. (HIGH: Autoprecharge; LOW: no Autoprecharge). A10 is sampled during a Precharge command to determine whether the Precharge applies to one bank (A10 LOW) or all banks (A10 HIGH). If only one bank is to be precharged, the bank is selected by bank addresses.
A12 / $\overline{BC}$	Input	Burst Chop: A12 / $\overline{BC}$ is sampled during Read and Write commands to determine if burst chop (on-the-fly) will be performed. (HIGH, no burst chop; LOW: burst chopped). See command truth table for details.

Symbol	Type	Function
$\overline{\text{RESET}}$	Input	Active Low Asynchronous Reset: Reset is active when $\overline{\text{RESET}}$ is LOW, and inactive when $\overline{\text{RESET}}$ is HIGH. $\overline{\text{RESET}}$ must be HIGH during normal operation. $\overline{\text{RESET}}$ is a CMOS rail-to-rail signal with DC high and low at 80% and 20% of $V_{DD}$ , i.e. 1.20V for DC high and 0.30V for DC low.
DQ	Input / Output	Data Input/ Output: Bi-directional data bus.
DQU, DQL, DQS, $\overline{\text{DQS}}$ , DQSU, $\overline{\text{DQSU}}$ , DQL, $\overline{\text{DQL}}$	Input / Output	Data Strobe: output with read data, input with write data. Edge-aligned with read data, centered in write data. The data strobe DQS, DQL, and DQU are paired with differential signals $\overline{\text{DQS}}$ , $\overline{\text{DQL}}$ , and $\overline{\text{DQU}}$ , respectively, to provide differential pair signaling to the system during reads and writes. DDR3 SDRAM supports differential data strobe only and does not support single-ended.
TDQS, $\overline{\text{TDQS}}$	Output	Termination Data Strobe: TDQS/ $\overline{\text{TDQS}}$ is applicable for x8 DRAMs only. When enabled via Mode Register A11 = 1 in MR1, the DRAM will enable the same termination resistance function on TDQS/ $\overline{\text{TDQS}}$ that is applied to DQS/DQS. When disabled via mode register A11 = 0 in MR1, DM/TDQS will provide the data mask function and $\overline{\text{TDQS}}$ is not used. x4/x16 DRAMs must disable the TDQS function via mode register A11 = 0 in MR1.
NC		No Connect: No internal electrical connection is present.
NU		No Use
$V_{DDQ}$	Supply	DQ Power Supply: 1.5 V +/- 0.075 V
$V_{SSQ}$	Supply	DQ Ground
$V_{DD}$	Supply	Power Supply: 1.5 V +/- 0.075 V
$V_{SS}$	Supply	Ground
$V_{REFDQ}$	Supply	Reference voltage for DQ
$V_{REFCA}$	Supply	Reference voltage for CA
ZQ	Supply	Reference Pin for ZQ calibration

**Note:**

Input only pins (BA0-BA2, A0-A15,  $\overline{\text{RAS}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$ ,  $\overline{\text{CS}}$ , CKE, ODT, DM, and  $\overline{\text{RESET}}$ ) do not supply termination.

## 4.10 POWER IC : OZ5311GN-A2-0-TR



**PRELIMINARY  
OZ5311**

### Current-mode PWM Controller

#### FEATURES

- Line-voltage discharge when AC is removed
- Low power consumption at light load/no load
- Current-mode PWM control
- Spread-Spectrum Frequency modulation
- Soft-Start function
- Protection Features
- ✓ AC under-voltage protection
- ✓ Output overload protection
- ✓ Regulated power output
- ✓ Over-current protection at current sense
- ✓ Maximum gate-drive voltage clamp
- ✓ V<sub>DD</sub> pin over-voltage protection
- ✓ Internal over-temperature protection

The controller is built-in with a High-Voltage start-up circuit which eliminates the power losses caused by external start-up resistors. It provides a current sink circuit to discharge line voltage across X-Capacitor when AC line is removed to provide a safe operation (explained below.) Further, it implements a proprietary design to provide line compensation to regulate the output power when the input voltage varies. The controller also provides a spread-spectrum frequency modulation function which minimizes the cost of Electro-Magnetic-Interference (EMI) filter components.

The controller is equipped with a synchronous slope compensation in current-mode control which enhances the stability of the converter and avoids sub-harmonic oscillations. A soft-start function effectively reduces the in-rush current and the voltage stress of the power MOSFET during startup.

#### APPLICATIONS

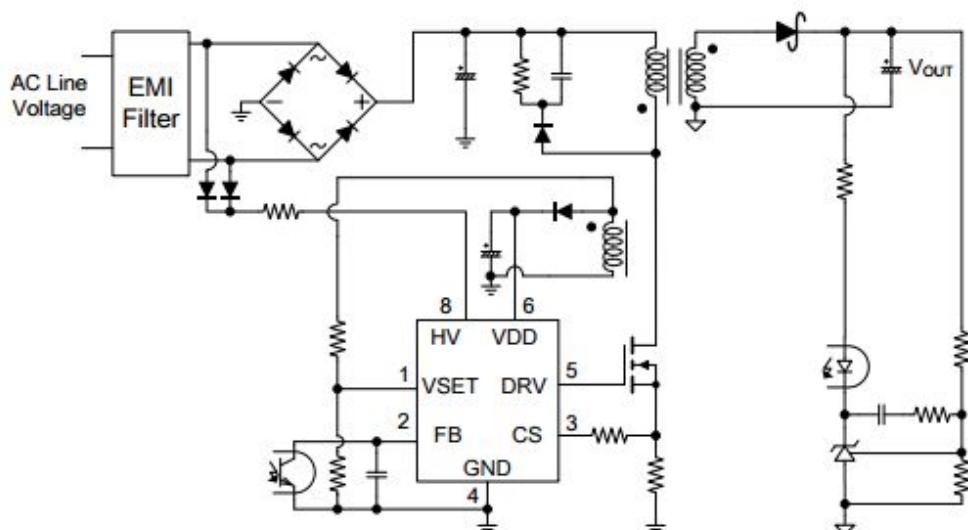
AC/DC power supply

#### GENERAL DESCRIPTION

OZ5311 is a highly integrated current-mode PWM controller for off-line Flyback converter applications.

In applications, OZ5311 provides protection functions include AC under-voltage protection, cycle-by-cycle current limiting at the current sense (CS) pin, V<sub>DD</sub> pin over-voltage protection, clamped voltage at DRV output and converter output over-load, short-circuit protections.

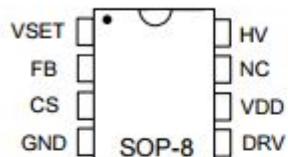
#### TYPICAL OPERATING CIRCUIT





**PRELIMINARY  
OZ5311**

### PIN DIAGRAM



### ORDERING INFORMATION

Part Number	Temp Range	Package	Frequency	VDD OVP
OZ5311GN	-20°C to +85°C Note 3, Page 4	SOP-8 Lead-Free	67KHz	Latch
OZ5311G1N	-20°C to +85°C Note 3, Page 4	SOP-8 Lead-Free	67KHz	Recovery
OZ5311G4N	-20°C to +85°C Note 3, Page 4	SOP-8 Lead-Free	132KHz	Latch
OZ5311G5N	-20°C to +85°C Note 3, Page 4	SOP-8 Lead-Free	132KHz	Recovery

OZ5311XYZ

X=G: Green package

Y=1: Package, Frequency, and OVP protection mode.

Z=N

### PIN DESCRIPTION

Name	I/O1	Pin No.	Description
VSET	I/O	1	AC-input Brown-In/Out setting and VOUT OVP detection
FB	I/O	2	Feedback pin
CS	I	3	Current sense pin
GND	Power	4	Ground
DRV	O	5	GATE Driver Output
VDD	Power	6	Power Supply
N.C.	--	7	No connection
HV	I	8	HV startup

Note<sup>(1)</sup>: I=Input, O=Output, I/O=Input and Output

## 4.11 Backlight IC :OZ560EGN-B1-0-TR



**OZ560**

## High Power LED Driver Controller

### FEATURES

- Integrates Boost converter controller and shunt voltage regulator
- Integrates MOSFETs for Boost converter and LED current switch
- PWM dimming
- PWM-to-Analog dimming
- Programmable operating frequency
- LED short circuit protection
- Over-Voltage Protection
- Over-Current protection
- Over-Temperature protection

### GENERAL DESCRIPTION

OZ560 includes LED driver control and shunt regulator. In AC/DC power converter applications, it is placed in the secondary side. When used with O2Micro's primary side AC/DC controller such as OZ531A, it provides a high performance and low cost solution for AC/DC converter and LED driver power supply modules in LCD display and general lighting applications.

The LED driver integrates two 90V<sub>DS</sub> rating N-ch MOSFETs for Boost converter and LED current switch. It supports one-string of LEDs with forward current up to 600mA.

OZ560 supports either direct-PWM or PWM-controlled analog dimming control for LED brightness adjustment. It provides a very wide dimming range for LED backlight applications.

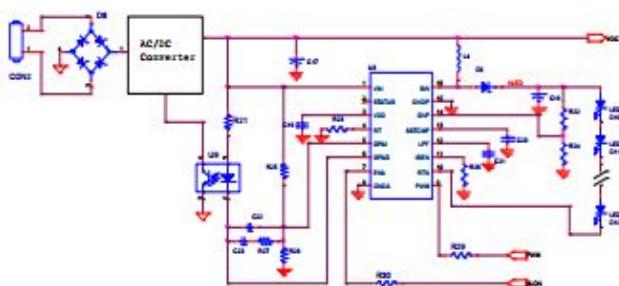
A built-in high precision shunt regulator is capable of driving an optical coupler circuit to provide a control signal for the primary side controller so that a regulated DC voltage output in secondary side is obtained.

OZ560 protection features include power MOSFET Over-Current Protection (OCP), LED short circuit protection (SCP), Over voltage protection (OVP), Open Diode protection (UVP), Over-Temperature Protection (OTP) and a STATUS pin indicator.

### ORDERING INFORMATION

Part Number	Temp Range	Package
OZ560GN	-20°C to +85°C Note 3, Page 3	16-pin SOP Lead-Free
OZ560EGN	-20°C to +85°C Note 3, Page 3	16-pin ESOP Lead-Free
OZ560DN	-20°C to +85°C Note 3, Page 3	16-pin PDIP Lead-Free

### SIMPLIFIED APPLICATION DIAGRAM



### PIN DIAGRAM

1	VIN	SW	16
2	STATUS	GNDP	15
3	VDD	OVP	14
4	RT	SSTCMP	13
5	OPAI	LPF	12
6	OPAO	ISEN	11
7	ENA	RTN	10
8	GNDA	PWM	9

**OZ560****PIN DESCRIPTION:**

Pin NO.	Name	I/O <sup>1</sup>	Description
1	VIN	---	Power supply of IC
2	STATUS	O	Fault Status output
3	VDD	I/O	Internal 6V voltage regulator output
4	RT	I/O	Resistor to set the IC Operation Frequency
5	OPAI	I	Input of Built-In Shunt Regulator
6	OPAO	I/O	Output of Built-In Shunt Regulator
7	ENA	I	ON/OFF Control of the LED driver
8	GNDA	-	Signal GND of IC
9	PWM	I	External PWM Dimming Signal Input
10	RTN	I/O	Drain of internal LED current switch
11	ISEN	I/O	Source output of LED current switch and LED current sense pin
12	LFP	I/O	Low pass filter for analog dimming and selection between analog dimming and direct PWM dimming modes
13	SSTCMP	I/O	Soft start and compensation for LED driver control loop
14	OVP	I	Over voltage protection sense input
15	GNDP	---	Power GND of IC
16	SW	O	Drain of power MOSFET for boost converter

Note<sup>1</sup>: I=Input, O=Output, I/O=Input/Output

## 5. Software Upgrade

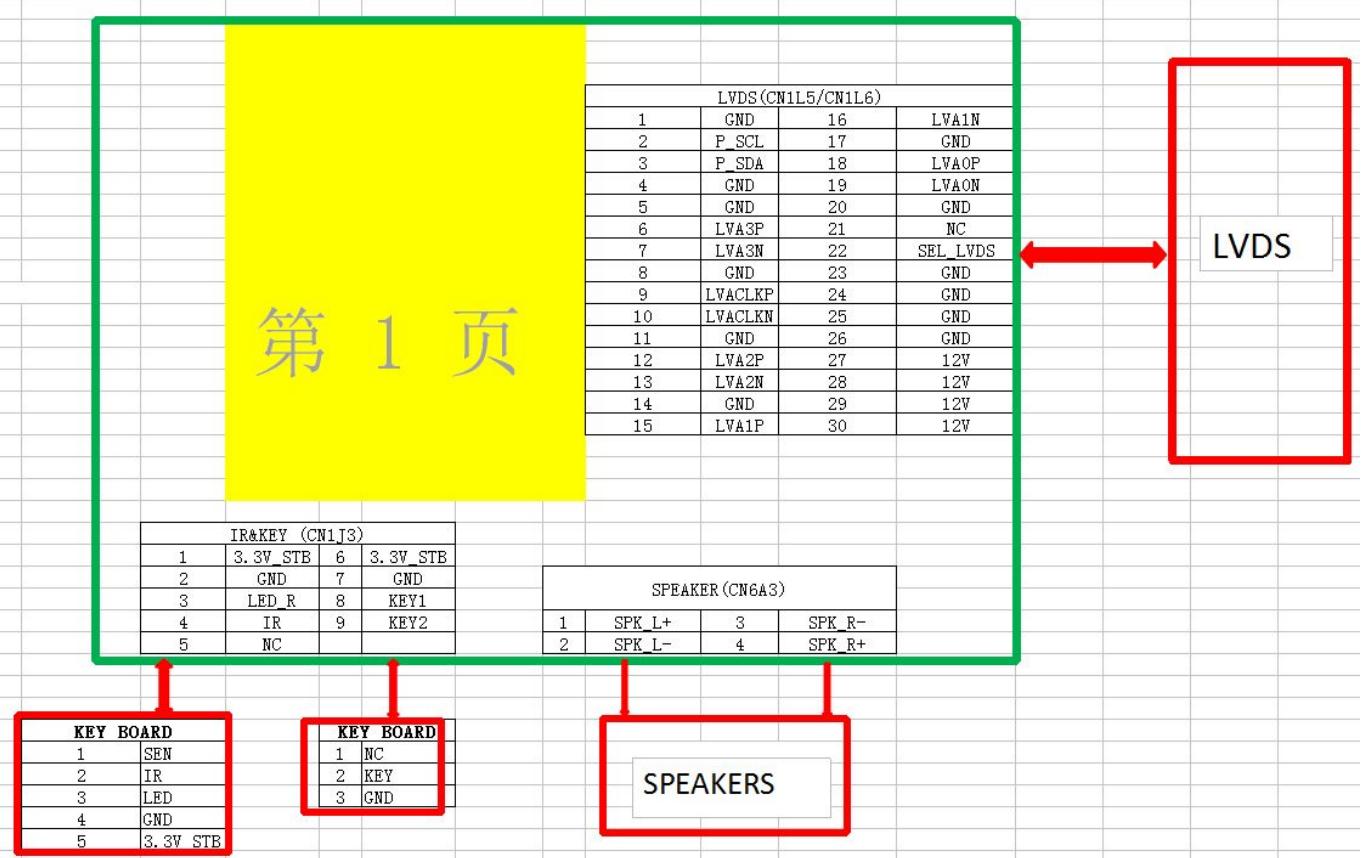
Copy the new software (named by “MstarUpgrade.bin”) to the root directory of USB drive. Plug the drive to the USB socket, enter MENU->FUNCTION->Software Update(USB), press “ENTER/OK” button to begin update. TV set will restart when finish. Note, you need to restart the TV set again by AC power.

**NOTE:** Some other settings not mentioned above are only used for software engineer, they are ready by software according to different panels and markets and usually should not be changed.

## 6. Setting Hotel Mode Menu

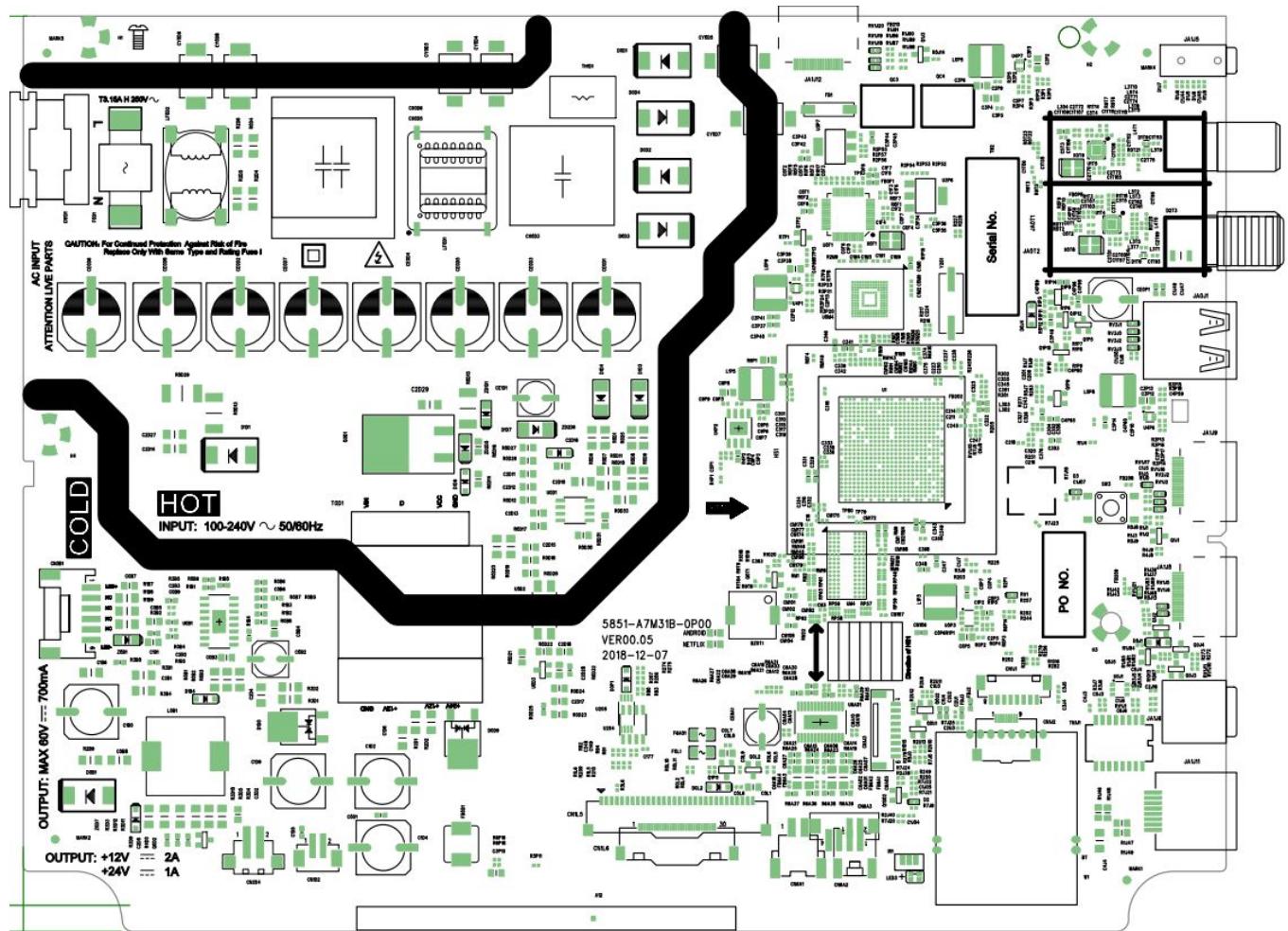
Item	option	function
Hotel Mode	ON/OFF	Enable Hotel model and allow enable all other functions of MENU
Lock Key	ON/OFF	Block all keyboard keys from TV set
Setup Menu	ON/OFF	Enable or block the Setup Menu
Max Volume	0-100	Set the max volume value you can adjust
Power On Source	AV/ATV/DVB-C/DVB-T/T2/HDMI1/HDMI2	Allow select which source TV will be set every time POWER ON
Power On Volume	0-100	Set the default volume value of every time POWER ON
Power On Mode	Direct/Memory/Secondary	Set the Power On mode when power is cut and back
Backup Database		Allow to copy all TV settings of hotel mode to be transferred to another model.
Update Database		The data copied from another TV can be input in the TV

## 7. Wiring Diagram

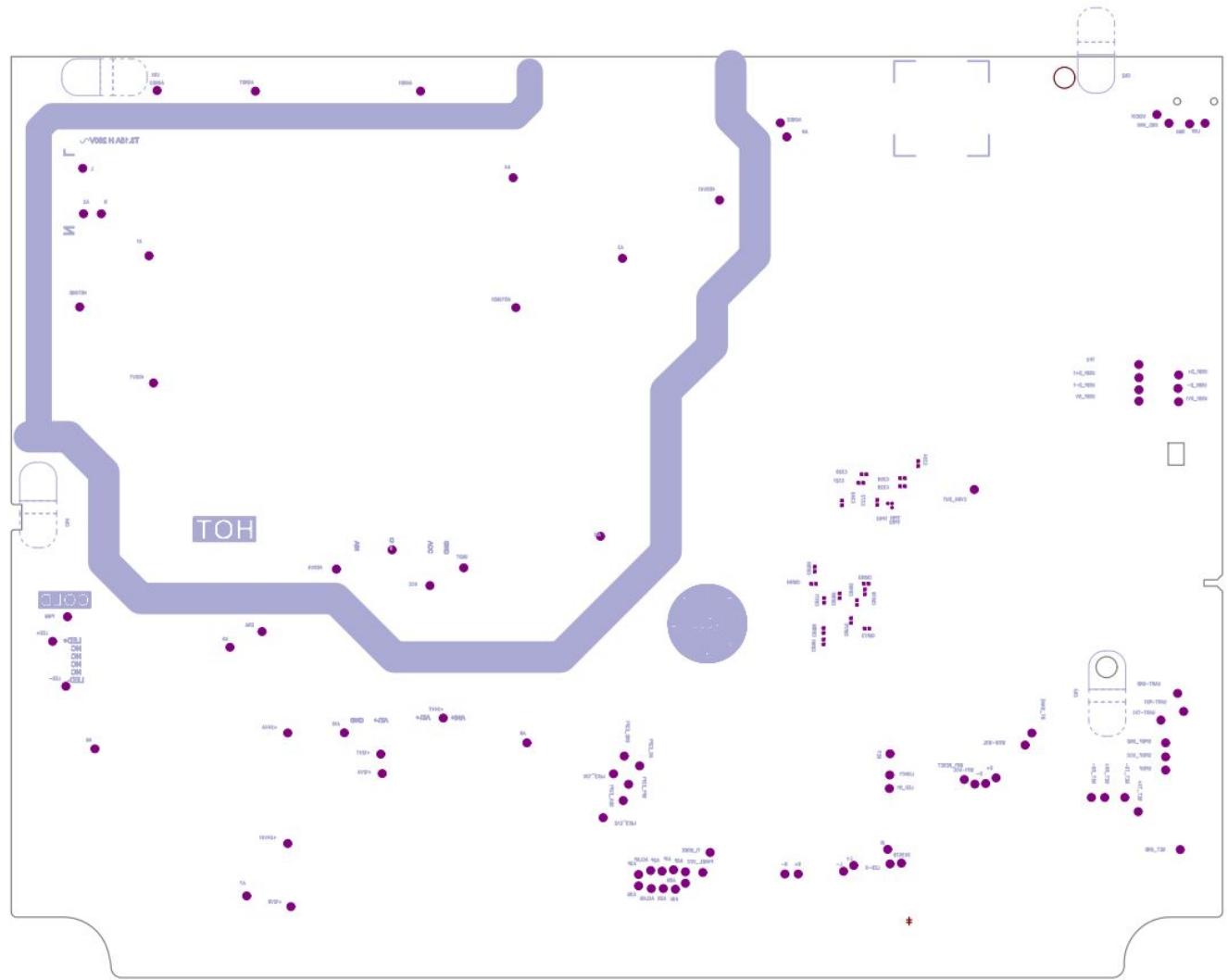


## 8. PCB Silkscreen

### 8.1 Silkscreen top

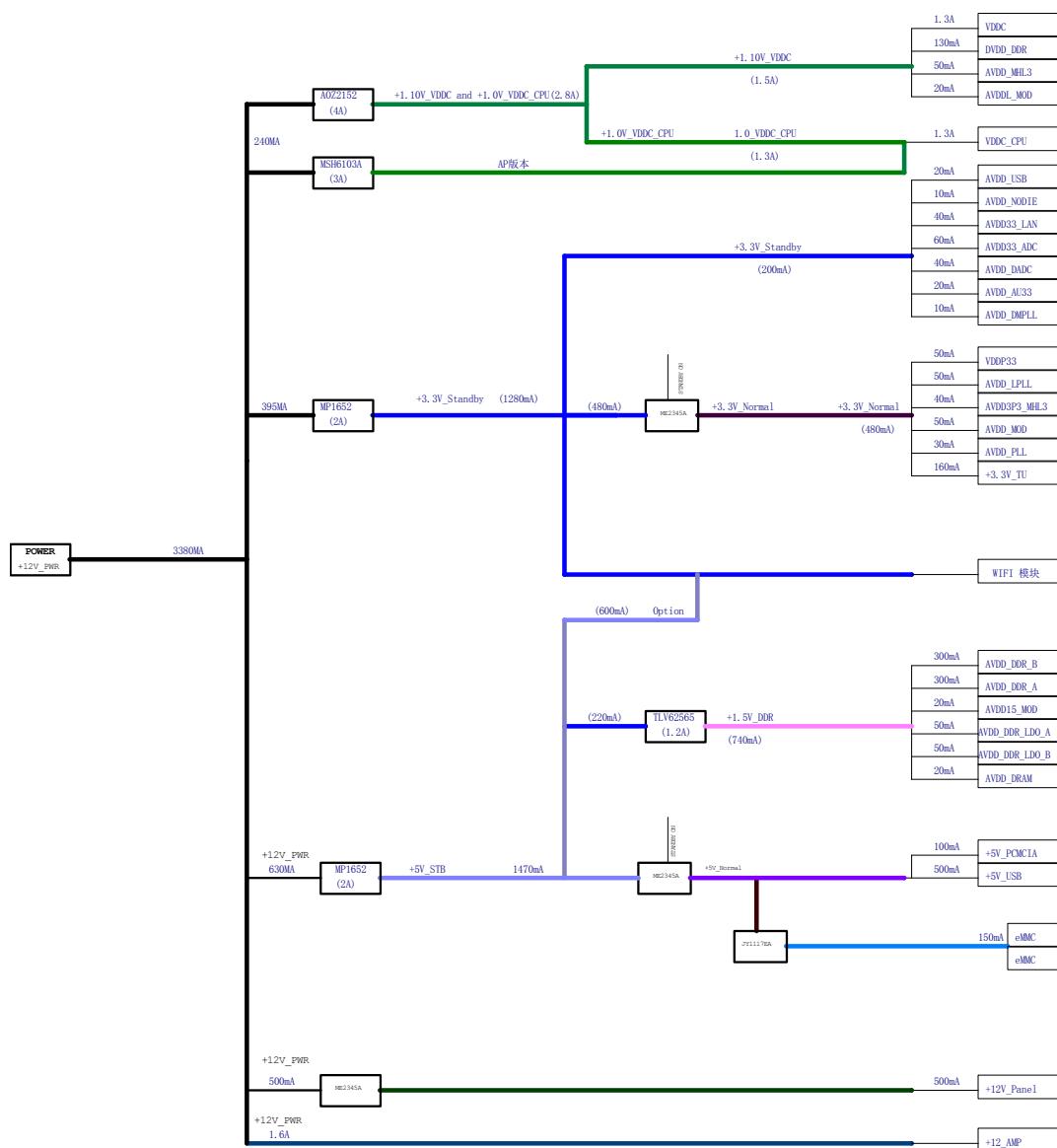


## 8.2 Silkscreen bottom

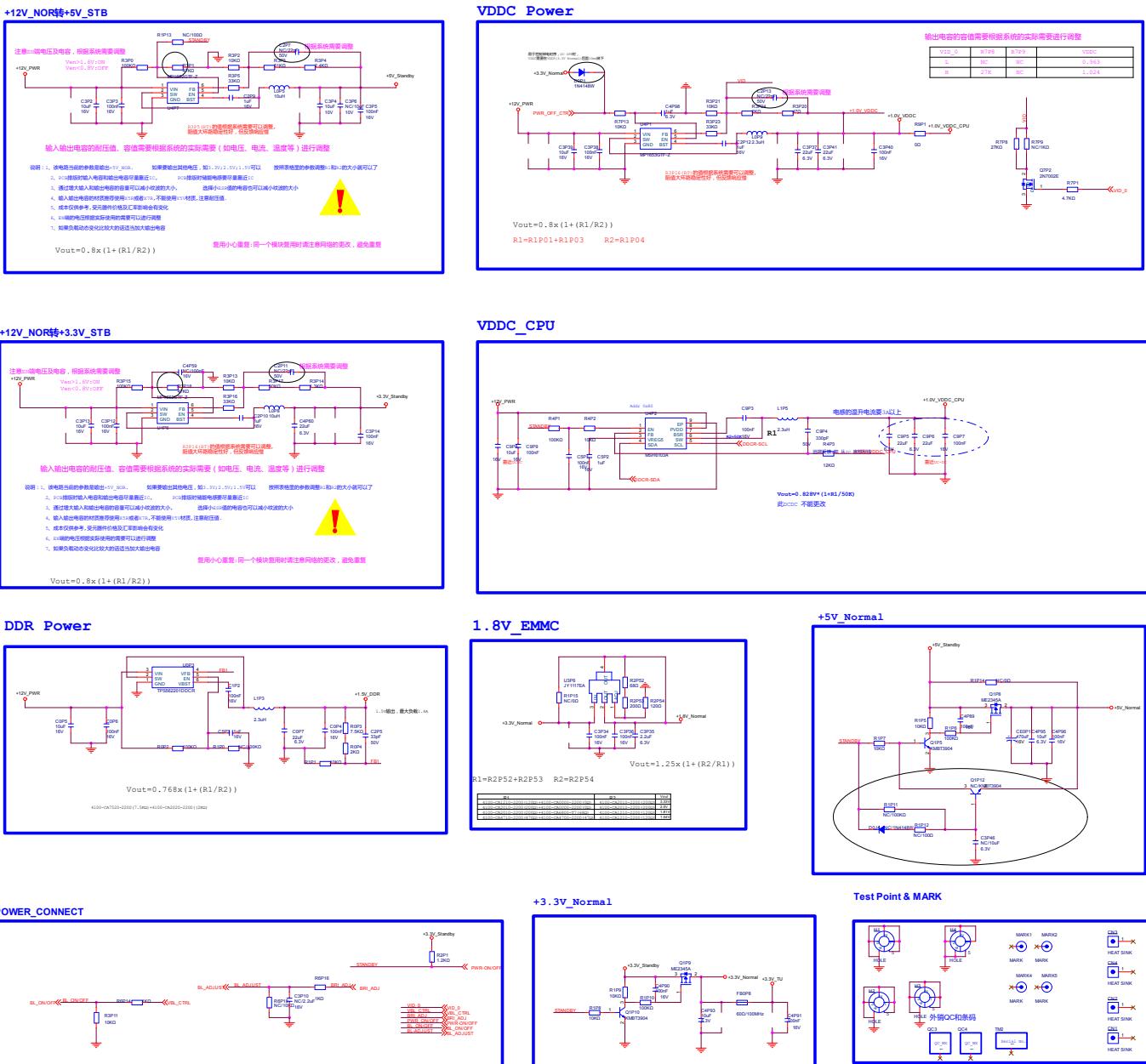


## 9. Schematic Circuit Diagram

Page0 Power Tree

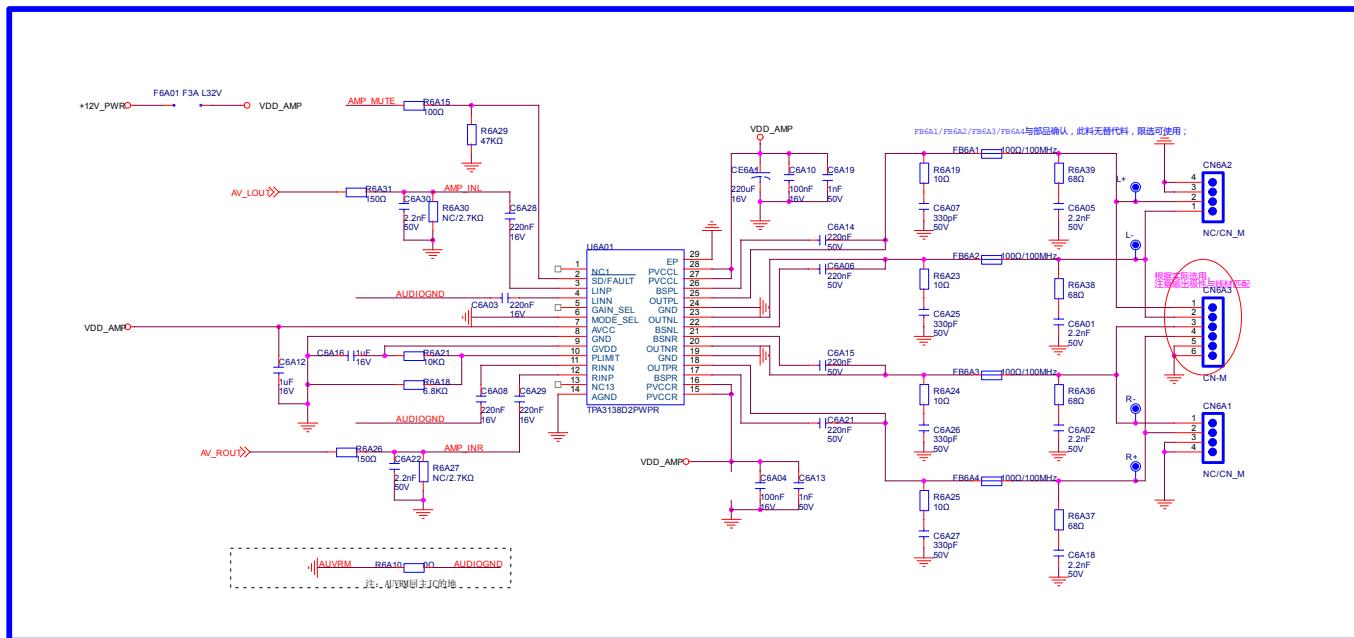


## Pag1 Power Circuit

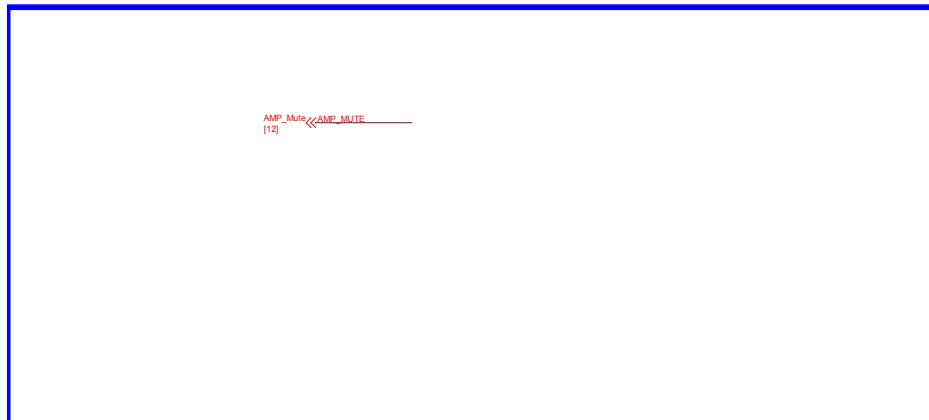


## Pag2 Amp

TPA3138

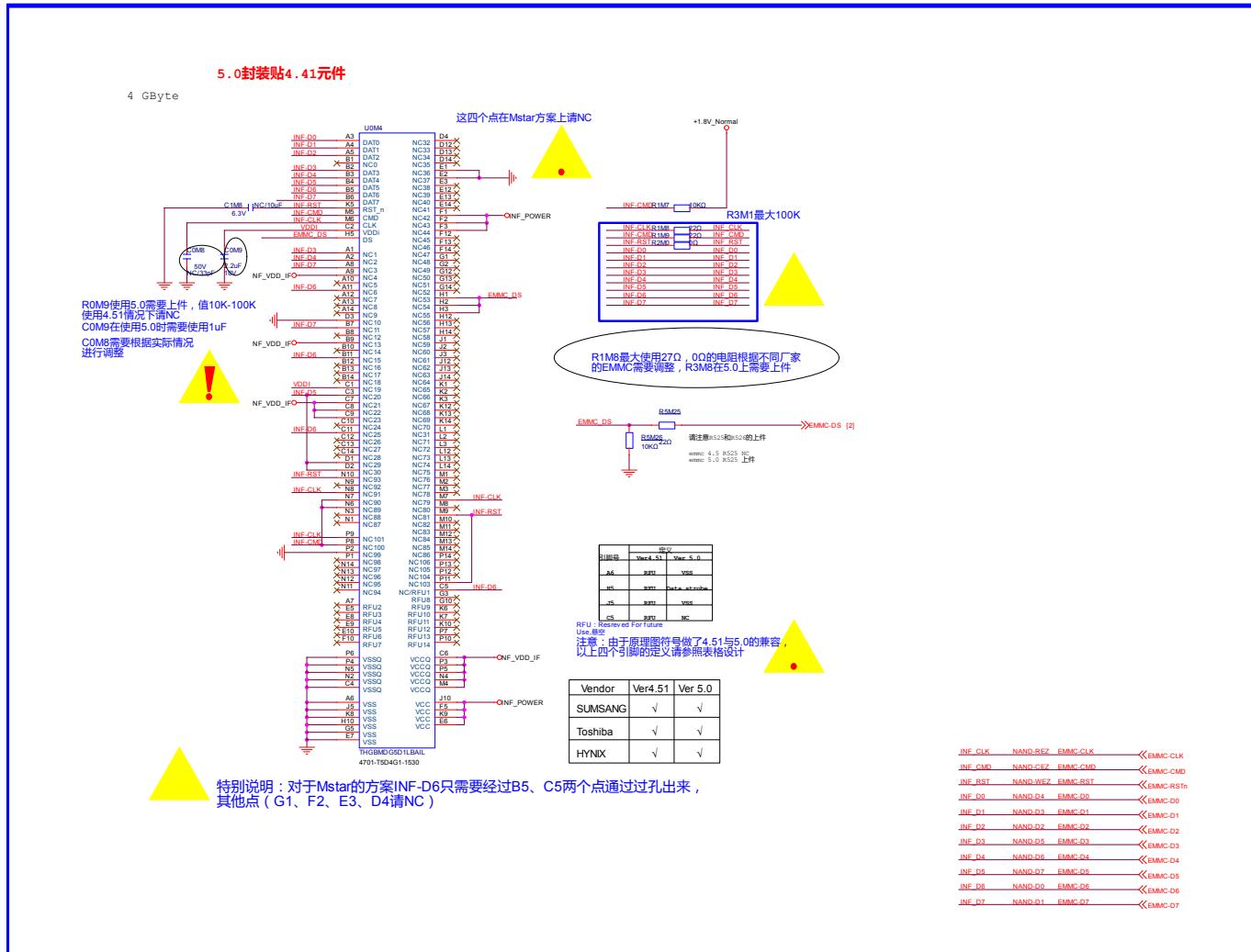


静音电路

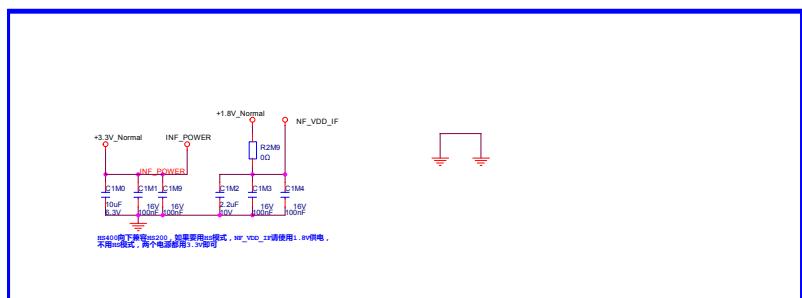


## Page3 Memory

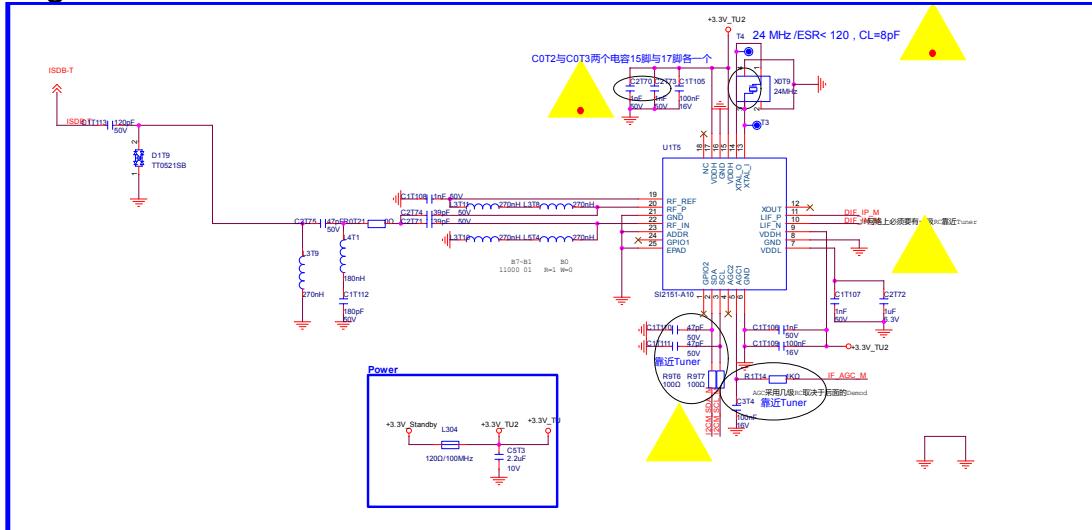
eMMC FLASH



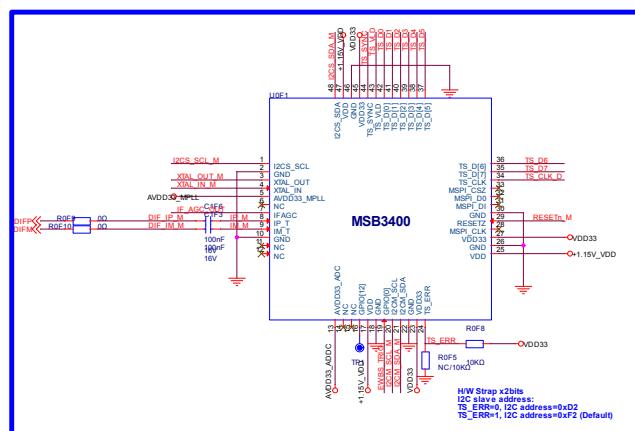
## POWER



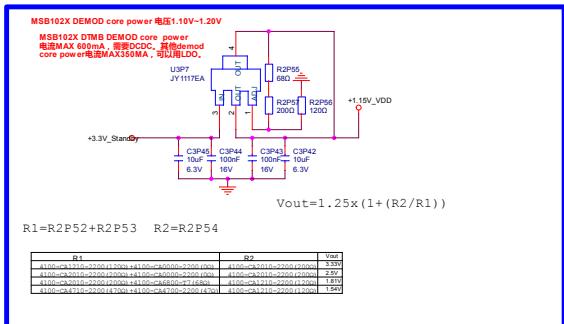
## Page4 Demodulator



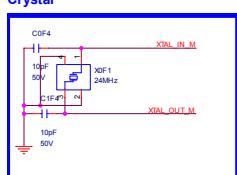
MSB3400



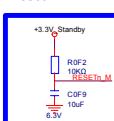
## 1.15V



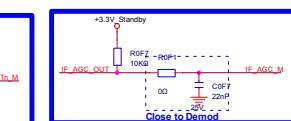
Crystal



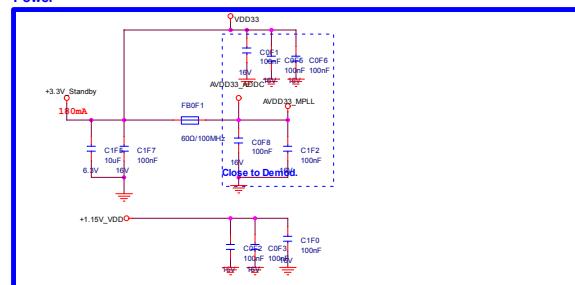
Reset



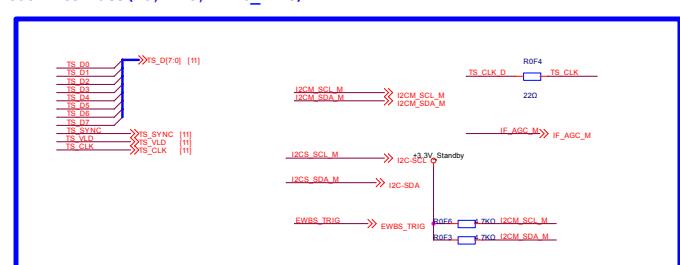
IF AGC



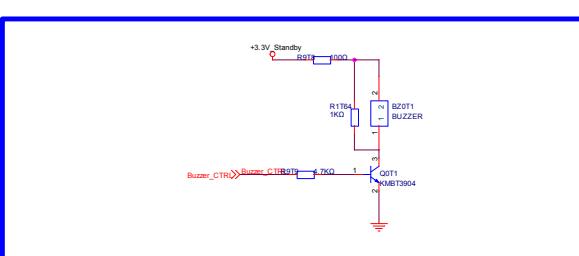
## Power



SOC Interface (TS, I2C, EWBS\_TRIGGER)

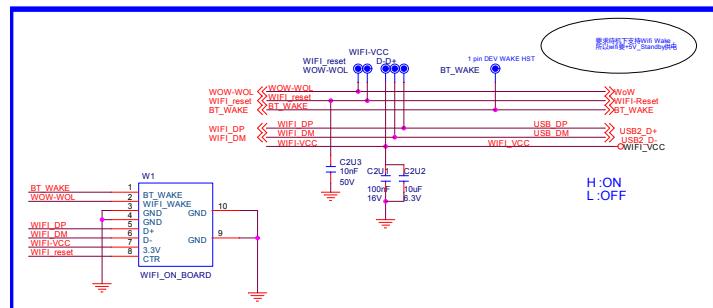


## Buzzer

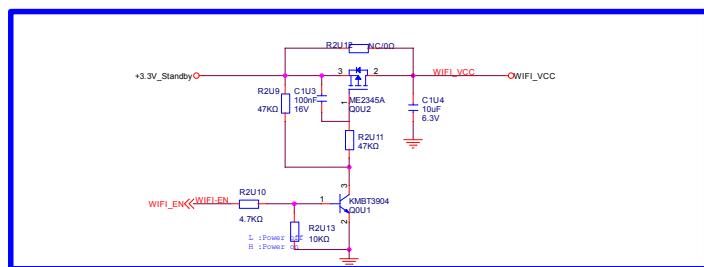


## Page5 USB HUB

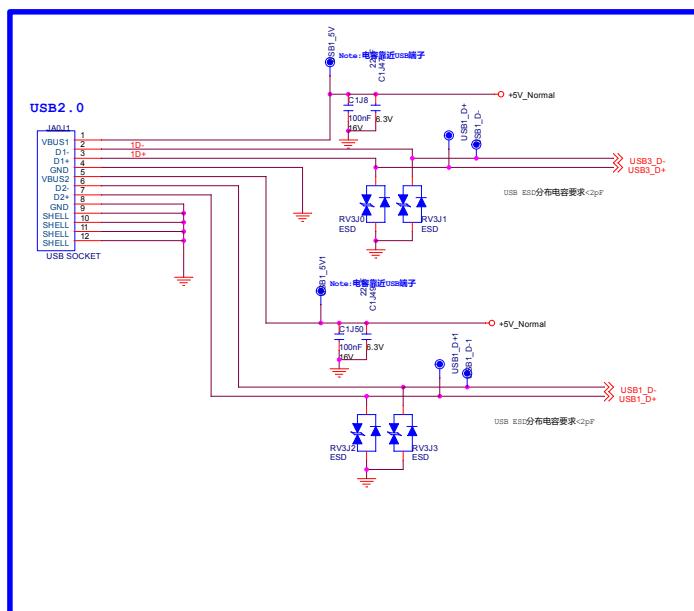
## WiFi



## WIFI POWER

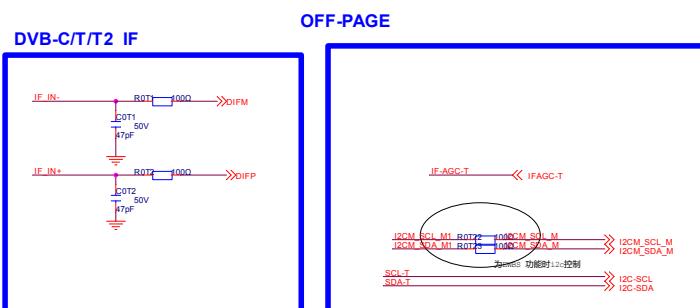
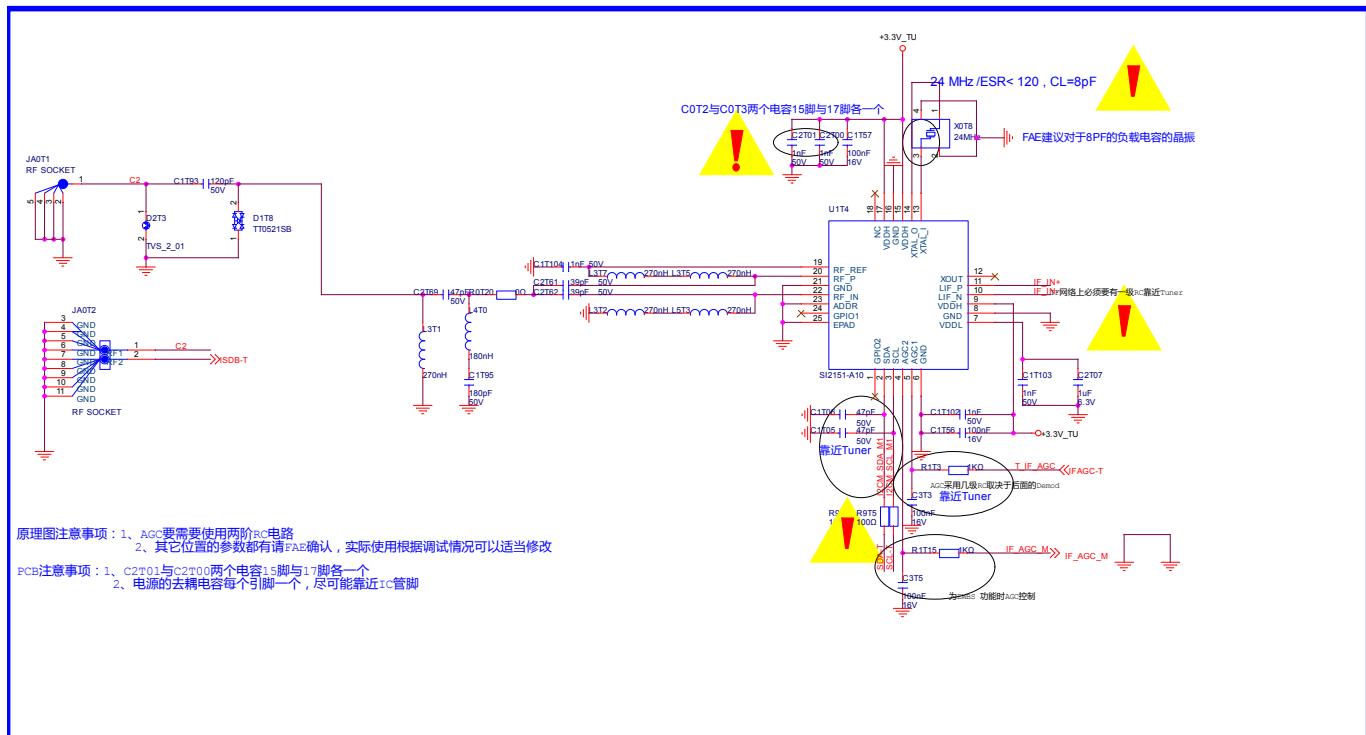


## USB2.0

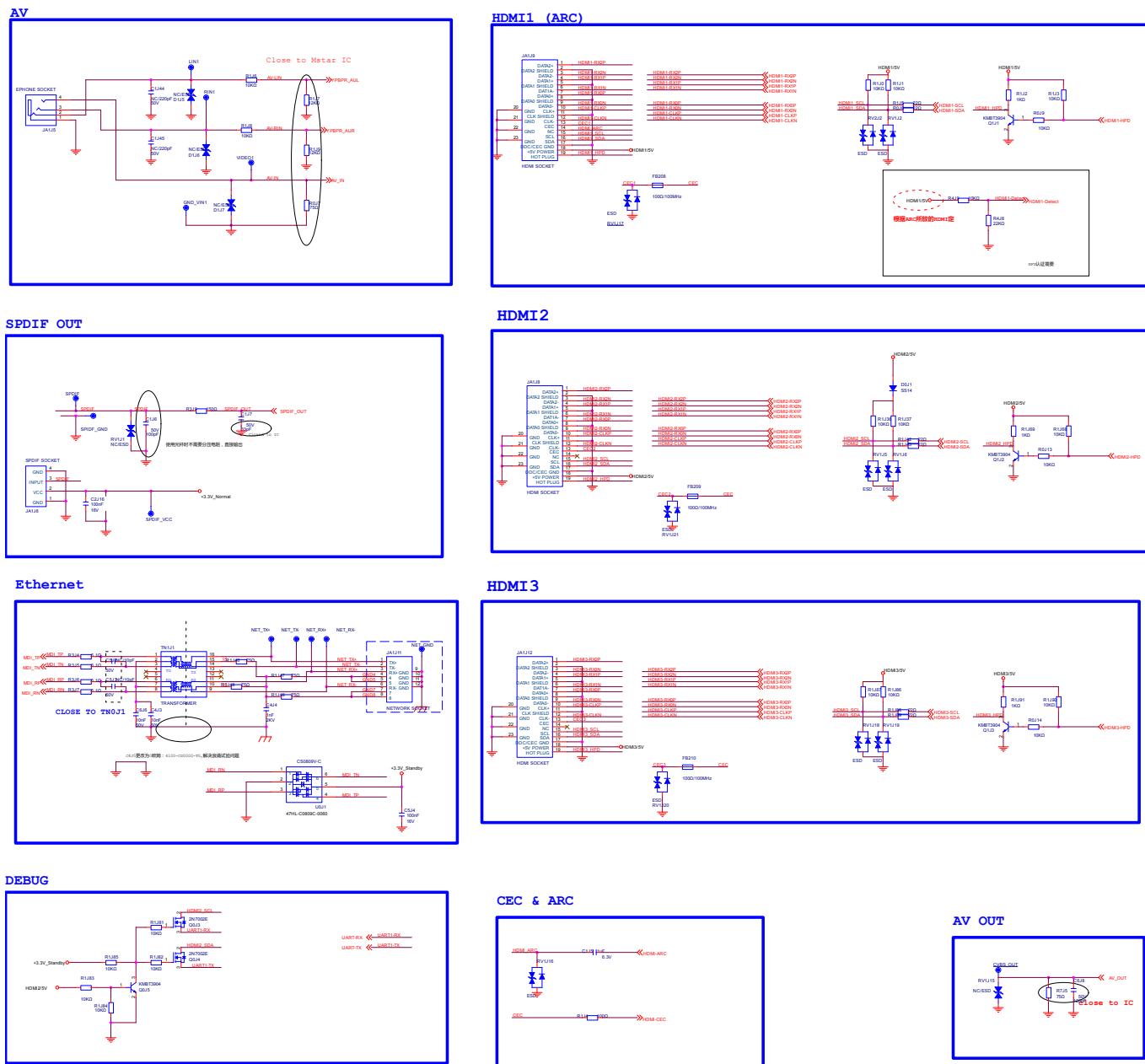


## Page6 Tuner

SI2151-----双头



## Page7 Standard port

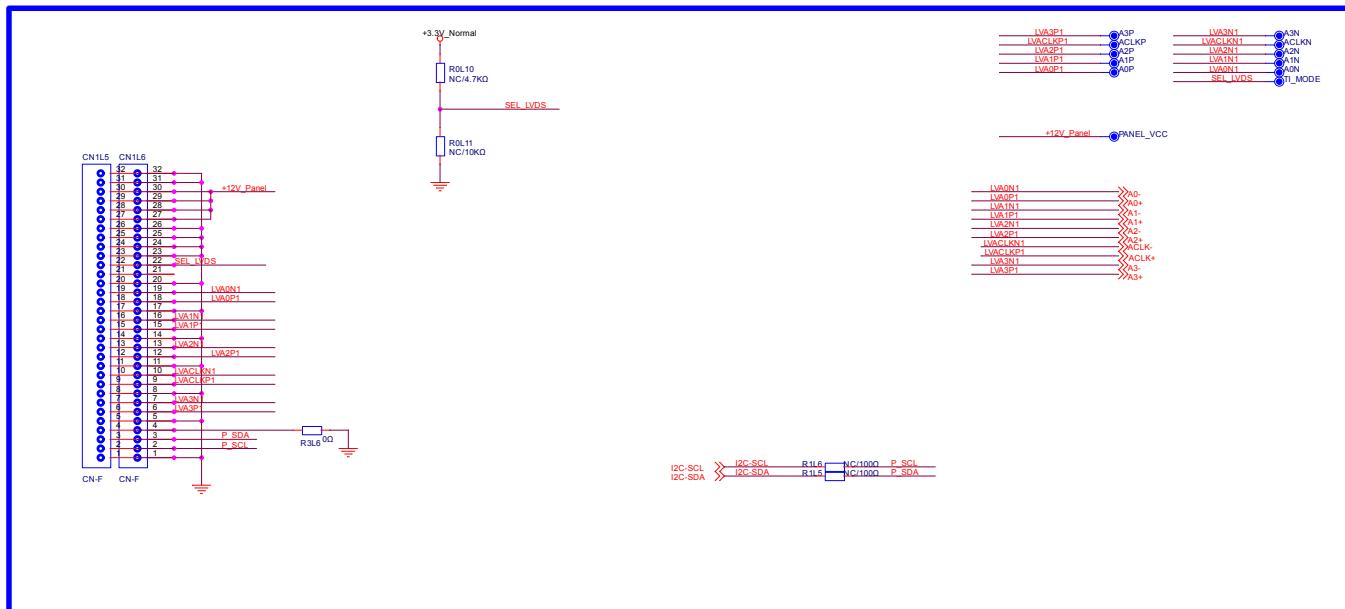


## Page8 CA Circuit

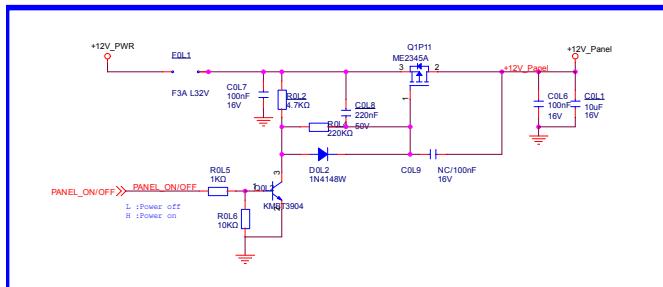
NA

## Page9 LVDS

FOR HD



## PANEL POEWR

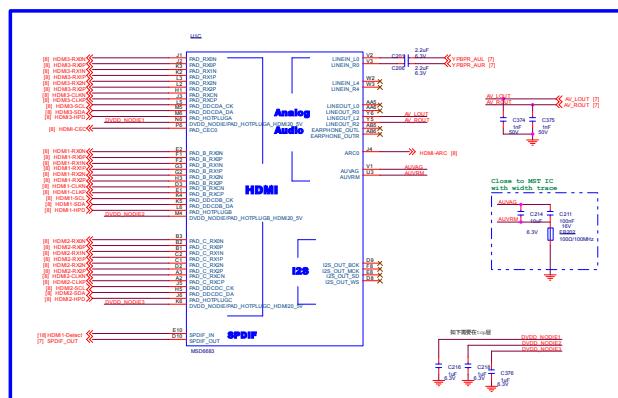


## Page10 TCON

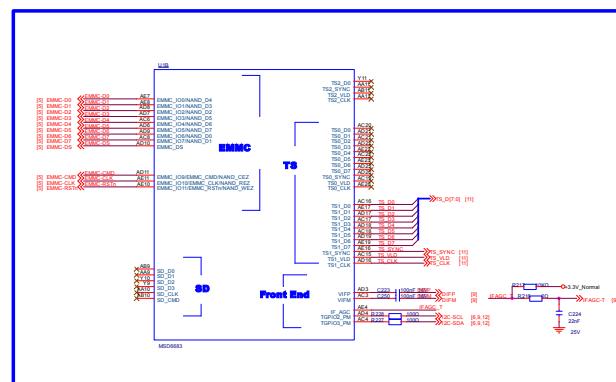
NA

## Page11 Main\_Chip

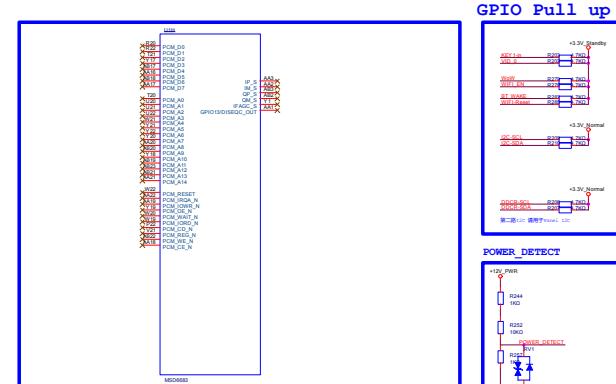
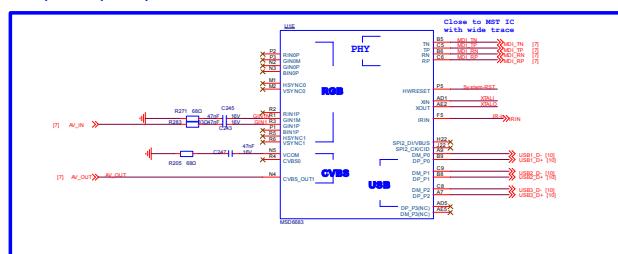
## HDMI/Audio Block



## TS/EMMC/FE



## RGB/CVBS/PHY/USB Block



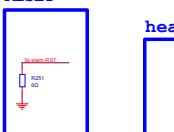
## Crystal



## Config



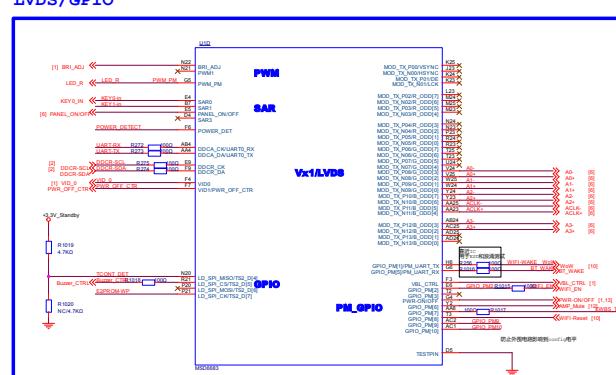
## RESET



## Symbol for Netflix&amp;Android

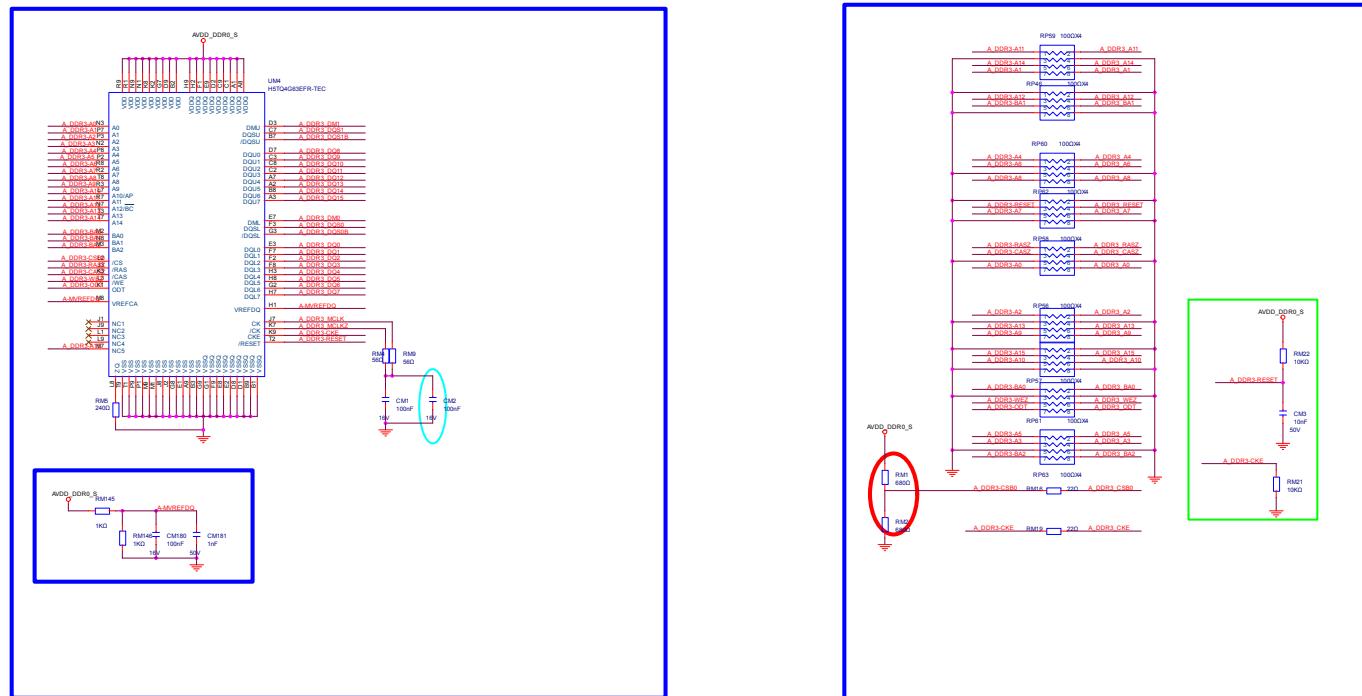


## LVDS/GPIO

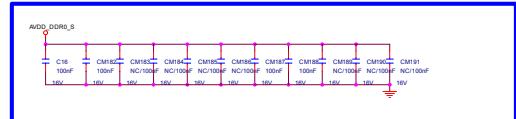


## Page12 DDR

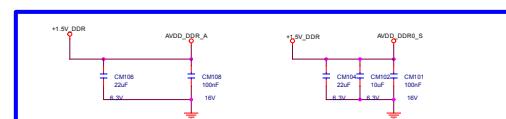
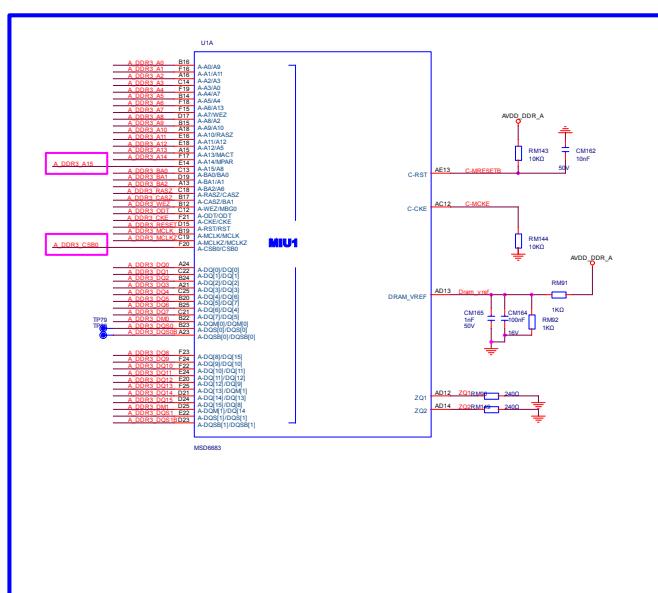
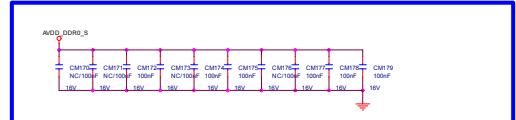
DDR3 4G bit 2133MHz



## DDR3 POWER

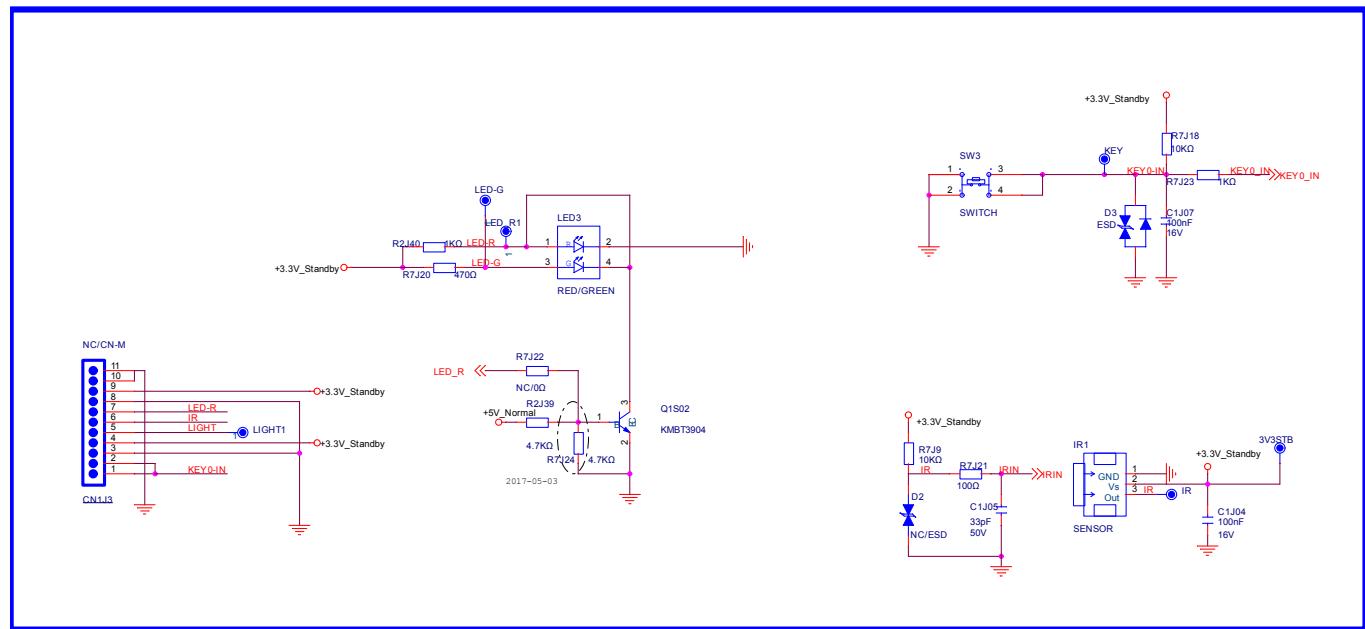


## DDR3 POWER

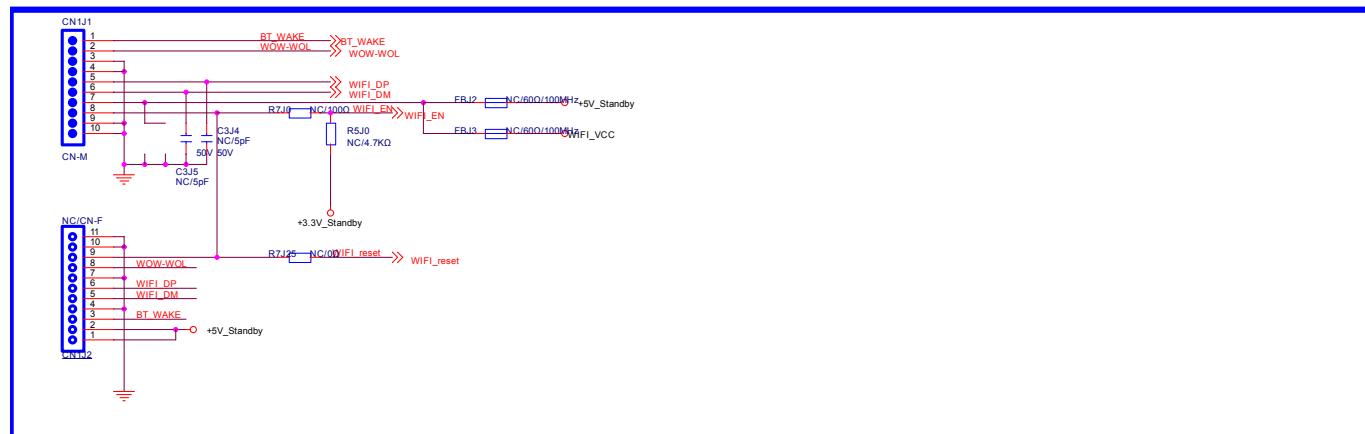


## Page13 connect

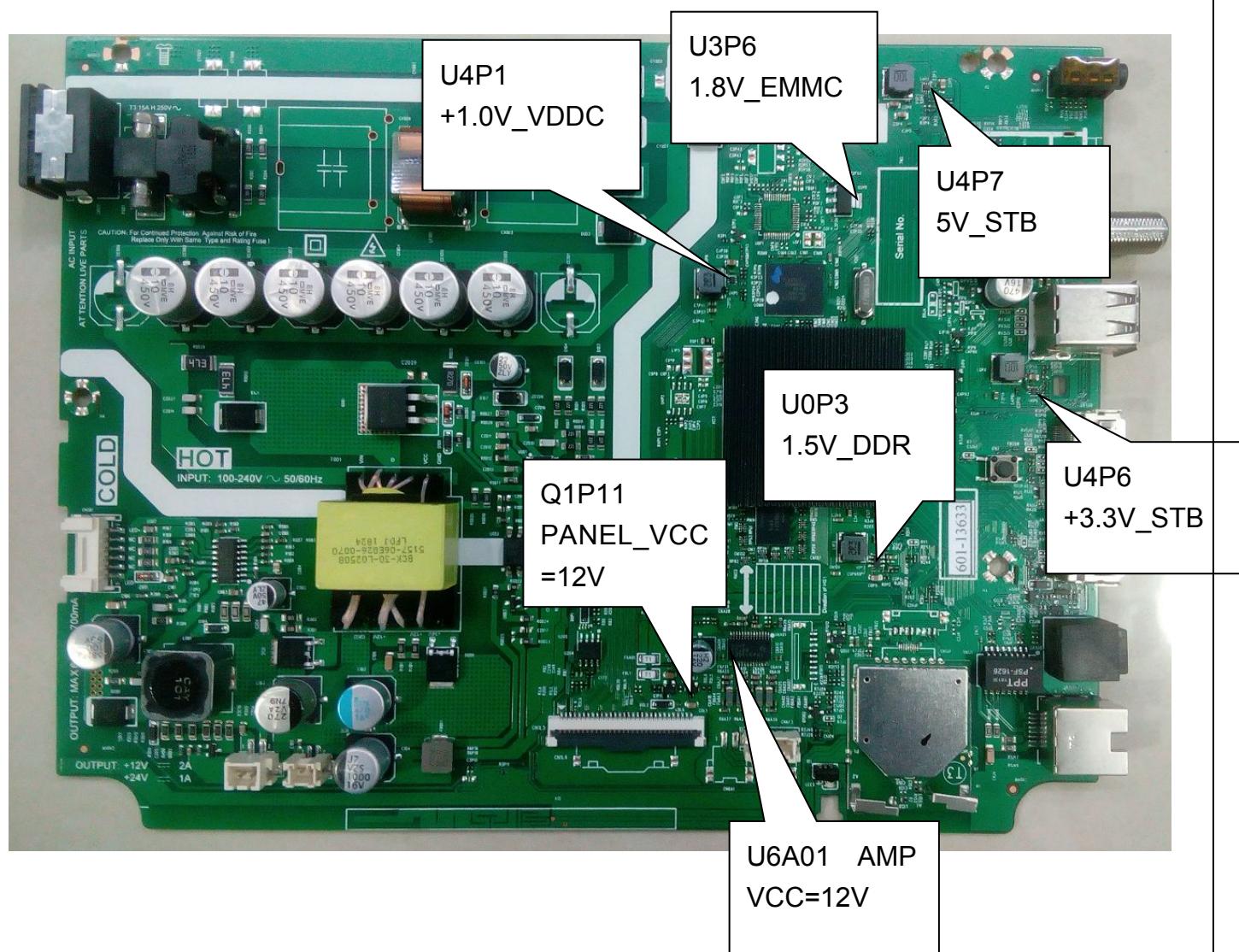
LED KEY&amp;IR



## WiFi

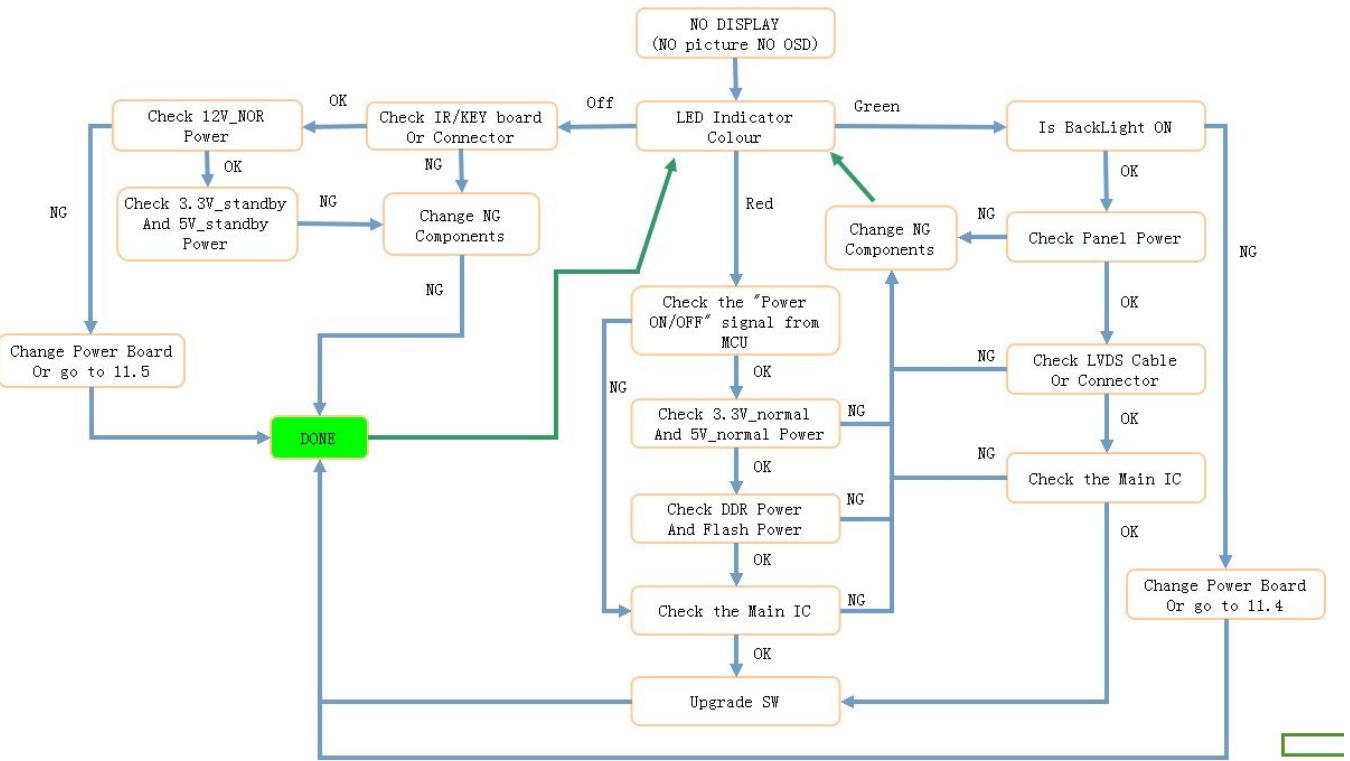


## 10.Key Power Check Point

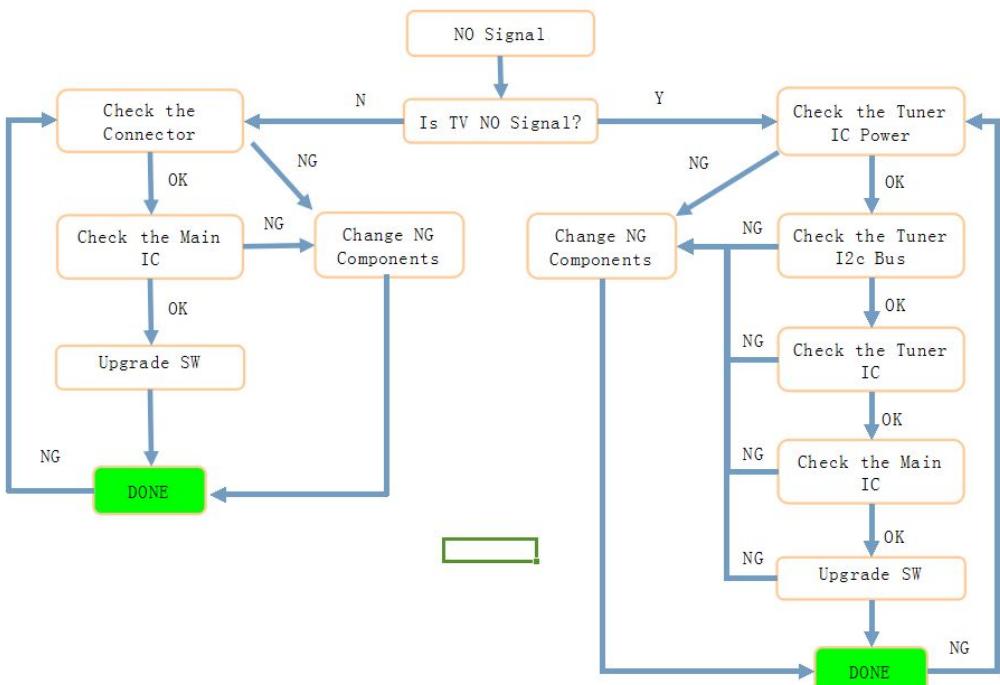


## 11.Trouble Shooting

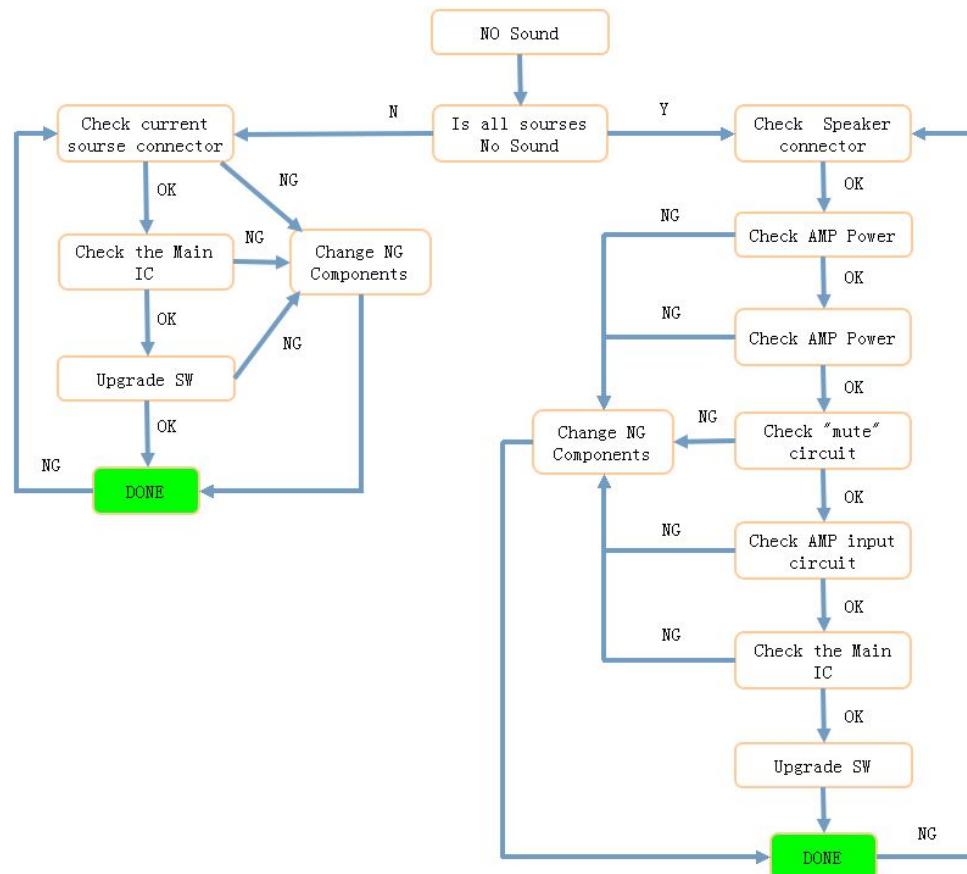
### 11.1 No Display



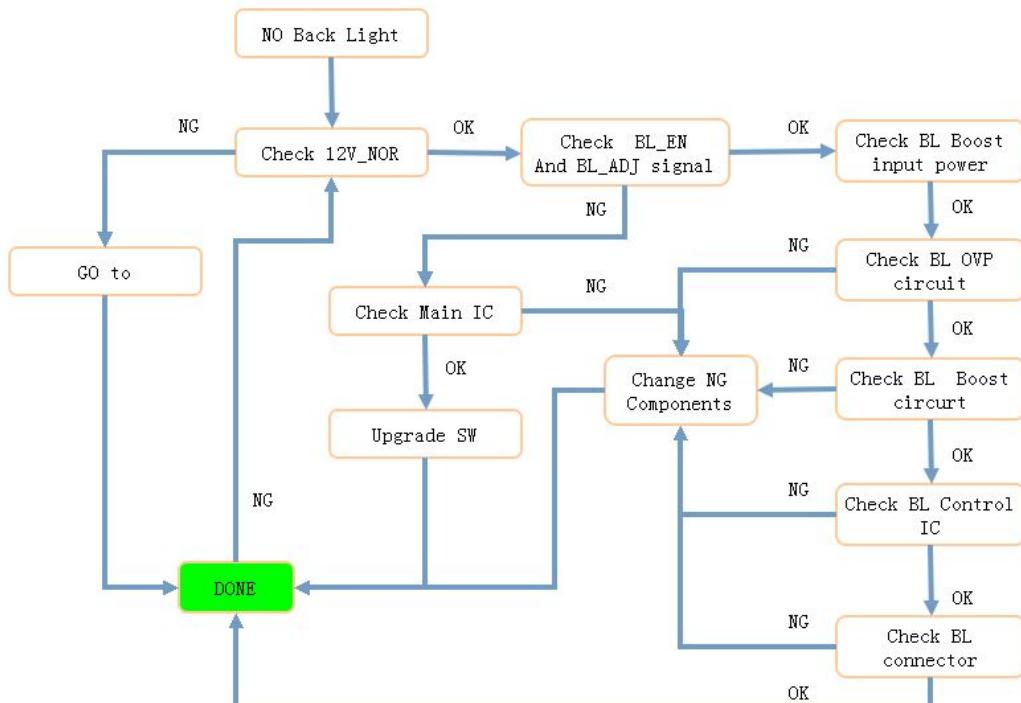
### 11.2 Has BackLight but no Image



### 11.3 Has Video but no Sound



### 11.4 Has Main power but no BackLight



## 11.5 No main power ( 12V\_NOR )

