```verilog
module fastCounter(
    input clk,
    output reg f
    );

    reg [3:0] q;

    always @(posedge clk) begin
        if (q == 3) begin
            f <= 1;
            q <= 0;
        end
        else begin
            q <= q+1;
            f <= 0;
        end
    end


endmodule
```