```
 1   module OscillatorX1 (
 2      input clk,
 3      input [7:0] x,
 4      output reg [7:0] f
 5   );
 6      reg [2:0]q = 3'b001;
 7
 8      always @(posedge clk) begin
 9         if (q == 1) begin
10            q <= 0;
11            f <= x;
12         end
13         else begin
14            q <= q + 1;
15            f <= f + 1;
16         end
17
18      end
19
20   endmodule
```