```
1   module buttonLogic(
2      input clk,
3      input subsignal,
4      input addsignal,
5      input [9:0] max,
6      output reg [7:0]k
7      );
8
9      always @(posedge clk) begin
10        if (subsignal == 1) begin
11           k <= (k - 1);
12           if (k == 0) begin
13              k <= max - 1;
14           end
15        end
16        if (addsignal == 1) begin
17           k <= (k + 1);
18           if (k > max) begin
19              k <= 0;
20           end
21        end
22     end
23
24  endmodule
```