```
1   module counter(
2      input clk,
3      input en,
4      input [1:0] s,
5      output reg f
6      );
7
8      reg [25:0] q;
9
10     always @(posedge clk) begin
11        if ((q == 50000000/((s + 1) * 8))) begin
12           f <= 1;
13           q <= 0;
14        end
15        else if (en == 1) begin
16           q <= q+1;
17           f <= 0;
18        end
19     end
20
21
22
23  endmodule
```