```
 1   module cycleColor(
 2      input clk,
 3      input changeSig,
 4      input [5:0]max,
 5      output reg [5:0]col
 6      );
 7
 8      always @(posedge clk) begin
 9         if (changeSig == 1) begin
10            col <= ((col + 1) % max);
11         end
12      end
13
14   endmodule
```