

```
1  module cycleColor4 (
2      input clk,
3      input changeSig,
4      input [3:0]max,
5      output reg [3:0]col
6  );
7
8      always @(posedge clk) begin
9          if (changeSig == 1) begin
10             col <= ((col + 1) % max);
11          end
12      end
13
14  endmodule
```