```verilog
module RunX (
    input clk,
    input [7:0] max,
    output reg [7:0] f,
    output reg next
);


    always @(posedge(clk)) begin
    if (f == max) begin
        f <= 0;
        next <= 1;
    end
    else begin
        f <= f + 1;
        next <= 0;
    end
    end
endmodule
```