Lab 1: Verilog HDL

Objective

- ✓ Review fundamental logic components.
- ✓ Introduce Verilog HDL modeling and verification.

Prerequisite

- ✓ Fundamentals of logic gates and Verilog HDL.

Experiments

1 Design and verify a binary-to-Gray-code converter for a Gray code sequence with 10 code words (input: ***abcd***, output: ***wxyz***, ***a*** and ***w*** are the MSB).
   1.1 Derive the Boolean function/logic equation.
   1.2 Draw the related logic diagram.
   1.3 Construct the Verilog RTL code for the converter and use a testbench to simulate the logic behavior for verification.

2 Design a signed 4-bit binary adder/subtractor with input ***a*** ($\mathbf{a}_3\mathbf{a}_2\mathbf{a}_1\mathbf{a}_0$), ***b*** ($\mathbf{b}_3\mathbf{b}_2\mathbf{b}_1\mathbf{b}_0$), **m** as the operator control (0 for addition and 1 for subtraction); output ***s*** ($\mathbf{s}_3\mathbf{s}_2\mathbf{s}_1\mathbf{s}_0$), **v** as overflow indicator.
   2.1 Derive the Boolean function/logic equation.
   2.2 Draw the related logic diagram.
   2.3 Construct the Verilog RTL code for the function and use a given testbench to simulate the logic behavior for verification.

3 (Bonus) For three 3-bit signed numbers ***a*** ($\mathbf{a}_2\mathbf{a}_1\mathbf{a}_0$), ***b*** ($\mathbf{b}_2\mathbf{b}_1\mathbf{b}_0$), and ***c*** ($\mathbf{c}_2\mathbf{c}_1\mathbf{c}_0$), build a logic circuit to output ***o***($o_2o_1o_0$) as the smallest number and use a given testbench for verification.

