

Supplementary 0305

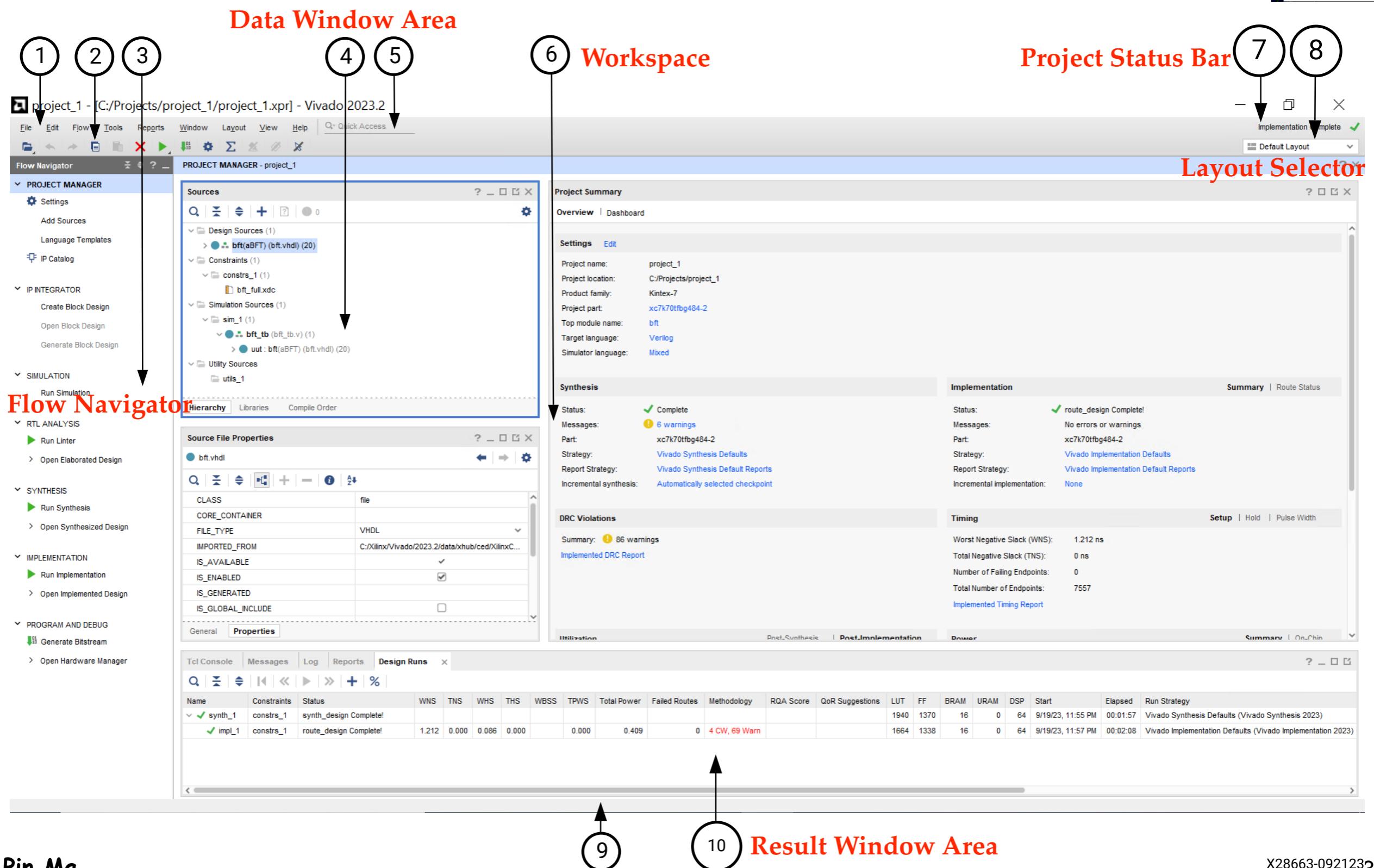
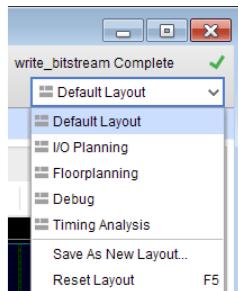
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<https://eeclass.nthu.edu.tw/course/18498>

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- Vivado Design Suite Guide - Using the Vivado IDE
 - UG893
 - <https://docs.xilinx.com/r/en-US/ug893-vivado-ide/Vivado-IDE-Viewing-Environment>

ViVado IDE View Environment



Critical Warnings

The screenshot shows the Vivado 2023.2 interface with the following details:

- Project Window:** Shows "project_1 - [C:/Projects/project_1/project_1.xpr] - Vivado 2023.2".
- Implementation Tab:** Selected, showing "IMPLEMENTED DESIGN - xc7k70tfg484-2".
- Netlist View:** Displays a tree structure of design components including "Nets (1726)", "Leaf Cells (142)", and several "arnd" components (round_1 to round_4).
- Netlist Properties View:** Shows primitive statistics: FLOP_LATCH (1338) and IIT (2038).
- Critical Messages Dialog:** A modal window titled "Critical Messages" displays one critical warning message:

! There was one critical warning message while opening this design.

Messages

[Vivado 12-4739] create_clock:No valid object(s) found for '-objects [get_ports bftClk1]'.

[C:/Projects/project_bft/project_1.srccs/constrs_1/imports/xc7k70tfg484-2/bft_full.xdc: 3]

Resolution: Check if the specified object(s) exists in the current design. If it does, ensure that the correct design hierarchy was specified for the object. If you are working with clocks, make sure create_clock was used to create the clock object before it is referenced.

Don't show this dialog again

OK Open Messages View
- Methodology View:** Shows a table of timing violations. A red box highlights the "Timing" section, specifically the "Bad Practice" and "TIMING" rows. The first two entries under "TIMING" are highlighted in yellow:

Name	Severity	Details
All Violations (73)		
Timing (73)		
Bad Practice (73)		
TIMING-6 (2)	Critical Warning	The clocks bftClk and wbClk are related (timed together) but they have no common primary clock. The design could fail in hardware. To find a timing path between these clocks, run the following command: report_timing -from [get_clocks bftClk] -to [get_clocks wbClk]
TIMING #2	Critical Warning	The clocks wbClk and bftClk are related (timed together) but they have no common primary clock. The design could fail in hardware. To find a timing path between these clocks, run the following command: report_timing -from [get_clocks wbClk] -to [get_clocks bftClk]
TIMING-7 (2)		
TIMING #1	Critical Warning	The clocks bftClk and wbClk are related (timed together) but they have no common node. The design could fail in hardware. To find a timing path between these clocks, run the following command: report_timing -from [get_clocks bftClk] -to [get_clocks wbClk]
impl_1 (73 violations) (saved)		

Project Summary

Project Summary

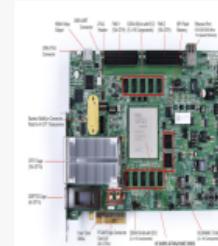
[Overview](#) | [Dashboard](#)

[Settings](#) [Edit](#)

Project name:	project_microBlaze
Project location:	c:/work/project_microBlaze
Product family:	Virtex UltraScale
Project part:	Virtex-UltraScale VCU108 Evaluation Platform (xcvu095-ffva2104-2-e)
Top module name:	base_mb_wrapper
Target language:	VHDL
Simulator language:	Mixed

Board Part

Display name:	Virtex-UltraScale VCU108 Evaluation Platform
Board part name:	xilinx.com:vcu108:part0:1.5
Connectors:	No connections
Repository path:	C:/Xilinx/2018.3/Vivado/2018.3/data/boards/board_files
URL:	www.xilinx.com/vcu108
Board overview:	Virtex-UltraScale VCU108 Evaluation Platform
Changes	



Synthesis

Status:	✓ Complete
Messages:	⚠ 832 warnings
Active run:	synth_1
Part:	xcvu095-ffva2104-2-e
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports

Implementation

Status:	✓ Complete
Messages:	⚠ 3 warnings
Active run:	impl_1
Part:	xcvu095-ffva2104-2-e
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental compile:	None

DRC Violations

Summary: ⚠ 1 warning

[Implemented DRC Report](#)

Timing

Worst Negative Slack (WNS):	5.271 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	4363

[Implemented Timing Report](#)

Utilization

[Post-Synthesis](#) | [Post-Implementation](#)

Graph | **Table**

Resource	Utilization	Available	Utilization %
LUT	1455	537600	0.27
LUTRAM	148	76800	0.19
FF	1362	1075200	0.13
BRAM	8	1728	0.46
IO	13	832	1.56
BUFG	2	960	0.21
MMC	1	16	6.25

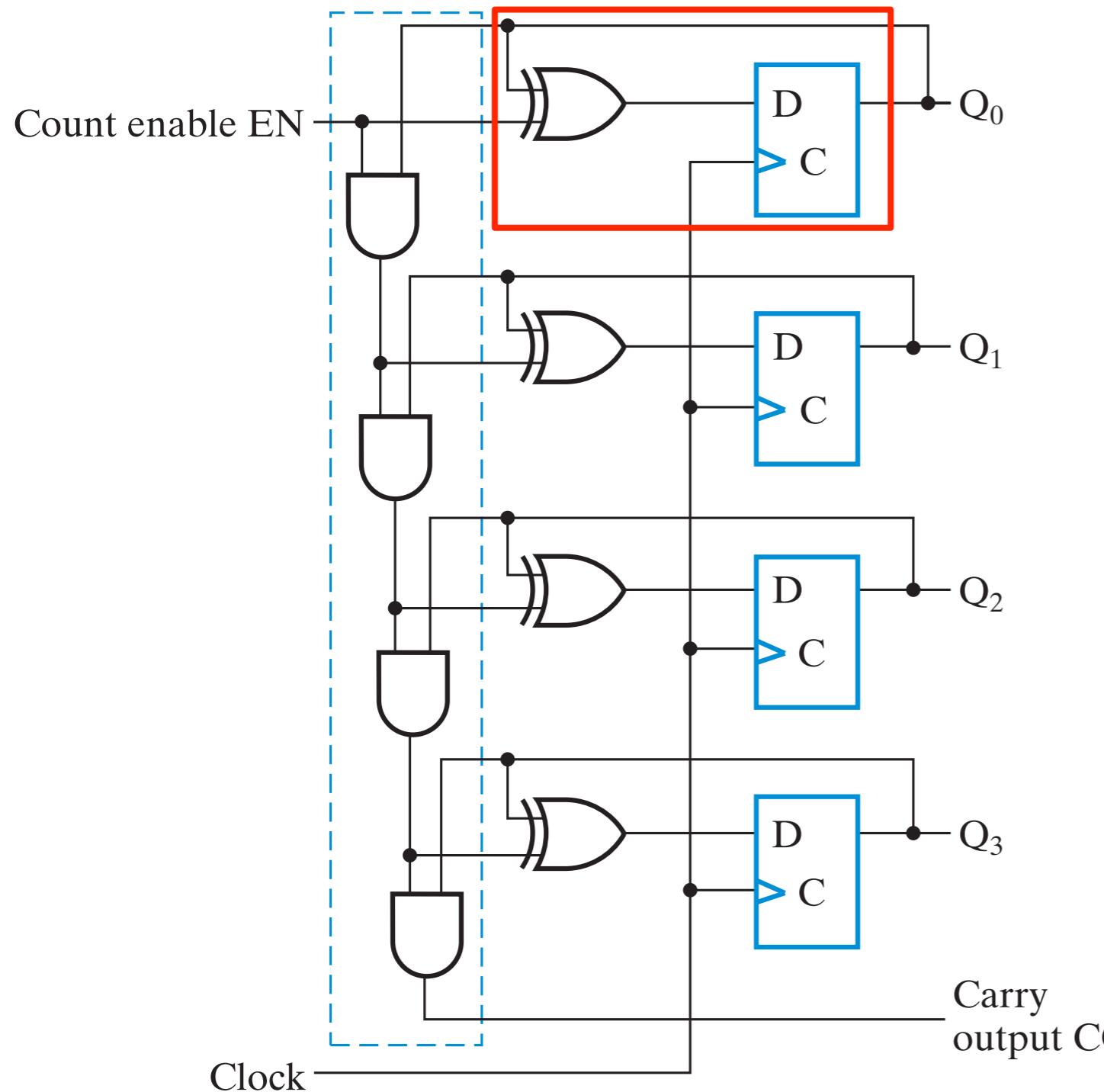
Power

[Summary](#) | [On-Chip](#)

Dynamic:	0.142 W (14%)
Clocks:	0.008 W (5%)
Signals:	0.004 W (3%)
Logic:	0.005 W (3%)
BRAM:	0.006 W (4%)
MMC:	0.114 W (80%)
I/O:	0.005 W (4%)

Static:	0.908 W (86%)
PL Static:	0.908 W (100%)

4-bit Binary Up Counter



```

module gcounter(
  q, // counter state
  clk, // clock
  rst_n, // low active reset
  en // counter enable control
);
  // I/O definition
  output [3:0] q; // counter state
  input clk; // clock
  input rst_n; // low active reset
  input en; // counter enable control
  reg [3:0] q;

  // Internal node definition
  wire [3:0] d; // input to the DFF

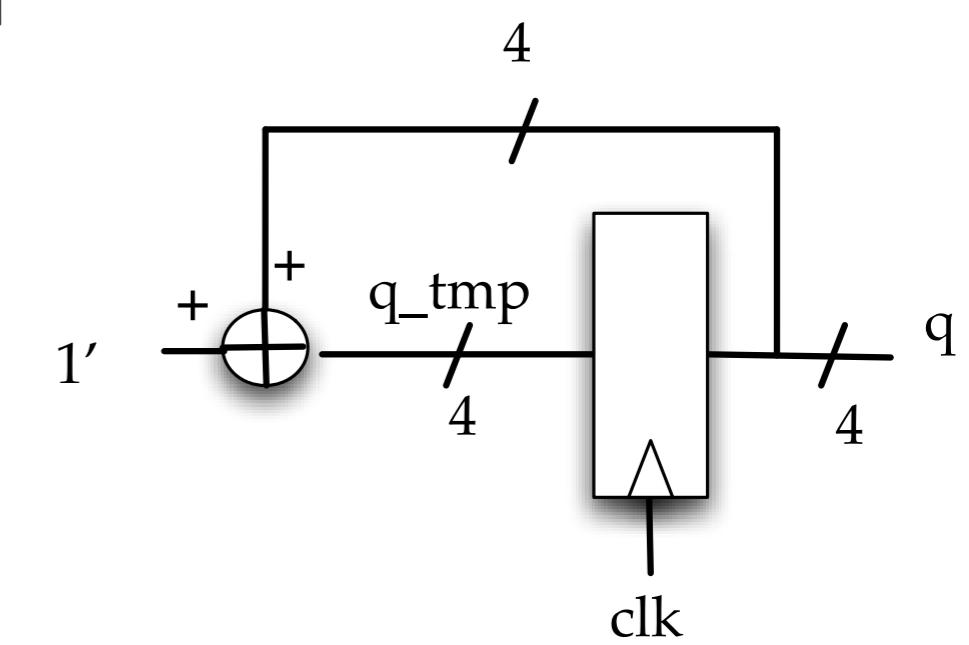
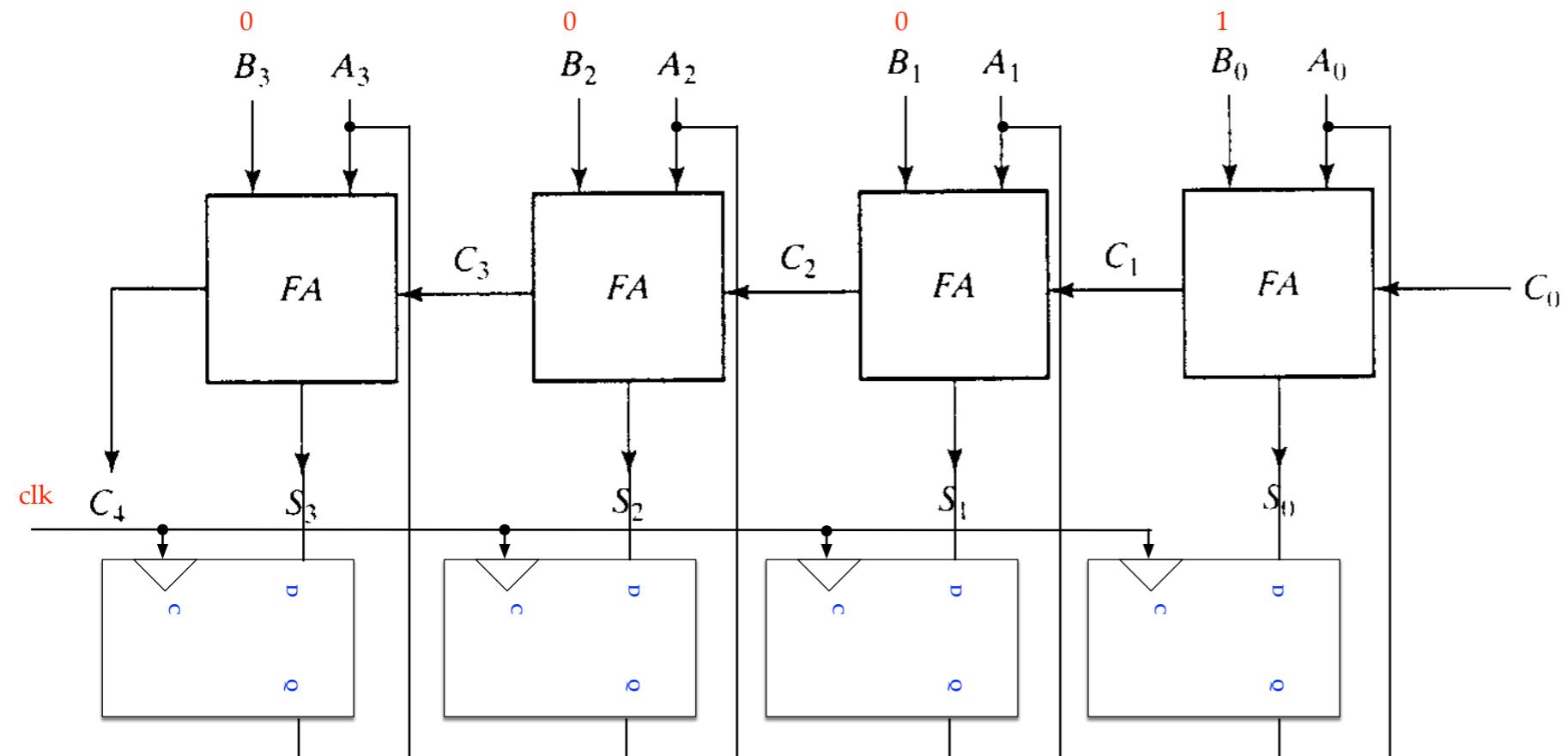
  // Combinational logics
  assign d[0] = en ^ q[0];
  assign d[1] = (en & q[0]) ^ q[1];
  assign d[2] = (en & q[0] & q[1]) ^ q[2];
  assign d[3] = (en & q[0] & q[1] & q[2]) ^ q[3];

  // Sequential logics: DFFs
  always @(posedge clk or negedge rst_n)
    if (~rst_n)
      q <= 4'd0;
    else
      q <= d;

endmodule

```

Another Design



Binary Up Counter

```

`define CNT_BIT_WIDTH 4
module bincnt(
    q, // output
    clk, // global clock
    rst_n // active low reset
);

output [`CNT_BIT_WIDTH-1:0] q; // output
input clk; // global clock
input rst_n; // active low reset

reg [`CNT_BIT_WIDTH-1:0] q; // output (in always block)
reg [`CNT_BIT_WIDTH-1:0] q_tmp; // input to dff (in always block)

// Combinational logics
always @*
    q_tmp = q + 1'b1;

// Sequential logics: Flip flops
always @(posedge clk or negedge rst_n)
    if (~rst_n) q<=`CNT_BIT_WIDTH'd0;
    else q<=q_tmp;

endmodule

```

