RICKY TRAN

Computer Engineer · Software Engineer · Electrical Engineer
1041 Regency Drive, Melbourne, FL, 32935
(+1) 561-542-6247 | rickydtran@gmail.com | www.rickytran.com

Skills

Expertise	FPGA/HDL Design and Verification, Digital System Architecture, IoT, Embedded Systems
Programming	VHDL, Perl, Python, TCL, MATLAB, C/C++, JS, Java
Implementation	Xilinx Vivado, Altera Quartus, Synopsys Synplify Pro, Microsemi Libero SoC
Simulation	Mathworks MATLAB, Cadence NCSim & Xcelium, Modelsim
Verification	Xilinx Chipscope, Real Intent Ascent Lint & Meridian, Mathworks HDL Cosimulation
Version Control	Apache Subversion, Git
Databases	MongoDB, Redis, MySQL, SQLite

Experience

L3Harris Technologies
Palm Bay, Florida

Electrial Engineer, Digital/Signal Processing
Jan. 2018 - Present

- Contributed and designed of blocks for FPGA-based Deep Learning Convolutional Neural-Net Application
- Designed, verified, and tested FPGA implementation of a Min-Max Heap/Priority Queue
- Majorly contributed to a Common Development Environment, a core group of scripts used to reduce risk and improve productivity of FPGA development
- Served as lead technical contributer for a Camera Display Bridge Application used to demonstrate capabilities of a Software Defined Radio by streaming raw image data over the air to a display
- Performed multiple formal FPGA Application Requirements Sell-Offs and Close Outs for Quality and Mission Assurance
- Designed, verified, and hardware tested COMSEC key storage interface with Single Error Correction and Double Error Detection
- Designed and architected flow control for High Data Rate Modulator capable of 2 Gbps for a Small-Satellite platform
- Designed, verified, and hardware tested baseband processing blocks for Frame Header Encoding with Unique Word insertion and Frame Payload Generation
- Digital design and integration and test experience on Aerospace Applications and Digital Payloads and Platforms
- Supported new graduate recruiting efforts by performing phone interviews and attended panels

Flow Development & Technology
Philidelphia, Pennsylvania

Independent Consultant/Software Engineer
Jan. 2019 - Present

- Architected scalable backend software architecture and connection details of hardware components for smart commercial building platform
- Developed embedded code to interface with proprietary biometric access solutions in preliminary design/prototyping
- Provided support and oversight for team building backend architecture proposed

Harris Corporation
Palm Bay, Florida

Electrial Engineer Intern
May. 2017 - Aug. 2017

- Designed multiple GUI-based tools in MATLAB to automate data collection and tool setup for anechonic chamber testing
- Exposure to theory and application of spread-spectrum techniques and chaotic signal processing
- Low Probability of Detection/Interception (LPD/LPI) Digital Communications
- Designed FPGA implementation of rate-line detector in VHDL
- Exposure to ground-up development of high-rate, real-time signal processing algorithms in hardware (FPGA)

Integrated Product and Process Design Program (IPPD@UF)
Gainesville, Florida

Computer Engineer Lead
Aug. 2016 - May 2017

- Developed Bluetooth/Wi-Fi IoT user management tracking system to improve efficency in construction industry
- Implemented backend API for client and hardware communication
- Developed code for ESP8266 microcontrollers to successfully act as sensor nodes and communicate over Wi-Fi to server via MQTT
- Integrated and interfaced HC05 bluetooth module with ESP8266 codebase and interact over a serial communication
- Worked in a multidisciplinary design team and exposure to business disciplinary skills on design projects

NSF Center for High Performance Reconfigurable Computing (CHREC)
Gainesville, Florida

Undergraduate Research Volunteer (F6 Group)
Jun. 2016 - Dec. 2016

- Exposure to implementation and testing on Texas Instruments Keystone 2 Digital Signal Processor
- Developed Single-Precison Finite Impulse Response Filter(SPFIR) with L2 cache optimzation utilizing a ping-pong DMA transfer scheme
- Learned OpenCL and OpenMP frameworks and analyzed existing code for existing filters

Education

University of Florida
Gainesville, Florida

Bachelor of Science in Computer Engineering
December 2017

- GPA: 3.29/4.00
- Coursework: Reconfigurable Computing, Computer Architecture, Operating Systems, Digital Design, Advanced System Programming, IPPD 1+2, Introduction to Software Engineering, Concurrent Programming, Microprocessor Applications, Digital Logic and Computer Systems, Data Structures and Algorithms, Introduction to Signals and Systems, Circuits 1, Applications of Discrete Structures, Programming Fundamentals 1+2