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Requirements:

1. Get simplified SOP function using k-map method. Clearly show the steps. _____
2. Model obtained SOP using **Behavioral Modelling** style of VHDL _____
3. Create a test bench to verify the design of obtained SOP. _____
4. Capture the waveforms and verify against truth table. _____

Learning Objectives:
The general learning objectives of this lab were to model the function and simulate to verify the designed model using Xilinx Vivado Design Tool. The model function is:

$$\boldsymbol{F(A,B,C,D) = \sum m(2,3,4,5,7,8,10,11,13,15)}$$

General Steps:

1. Simplify the given function using a k-map
2. Using k-map derive the Boolean equation.
3. Derive truth table
4. Model SOP function in behavioral modelling following the example given.
5. Write a testbench to verify the design.
6. Simulate and capture waveforms to verify the truth table.

Detailed Steps:
Some detailed steps to complete this lab were

1. Using a k-map to find the Boolean equation
   a. Put AB going across and CD going down
   b. Fill in the k-map
2. Start grouping the together all the possible 1's.
   a. Must be in sets divisible by 2. So groups of 1, 2 and 4

CD↓/AB→	00	01	11	10
00	0	1	0	1
01	0	1	1	0
11	1	1	1	1
10	1	0	0	1

3. Using the table, I found the Boolean equation.

$$B'C + BD + AB'D' + A'BC' = F$$

4. Afterward I got the truth table and found the outputs.
5. In Vivado using the example I change a couple pieces of code. Then I entered this in for the equation.

F <= (NOT B and C) OR (B and D) OR (A AND NOT B AND NOT D) OR (NOT A AND B AND NOT C)

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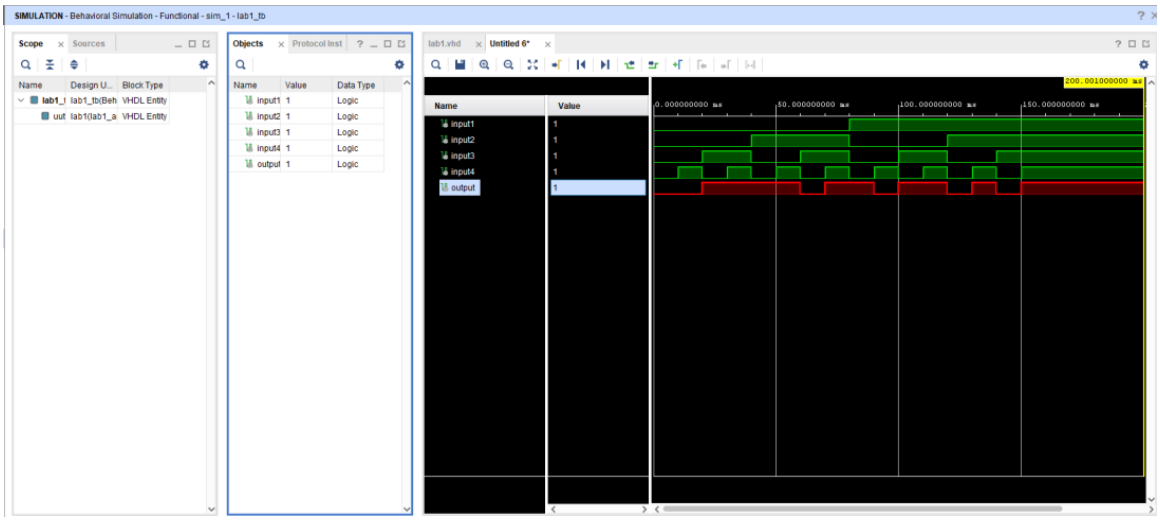
6. In the test bench file using the example lab I added in more inputs.
7. In the process section I add in all the changes manually from 0000 to 1111.
8. Then run the simulation

Observations:
One thing I noticed was that if you do not delete the part in the source code that covers "architecture behavioral" your waveform does not come out correctly. You must delete those last 3 lines of code for the waveform to form correctly.



Summary:
In this lab we learned some basic AND, OR and NOT gate combinations you can do in Vivado along with some basic VHDL code. We then coded in the Boolean equation we were looking for. Afterwards with the equation we ran a simulation that would output the waveform above. Overall, the lab was not to difficult, if anything it was a little tedious because in the test bench file, I had to manual switch inputs from 1 to 0 and vice versa, starting from 0000 all the way to 1111.