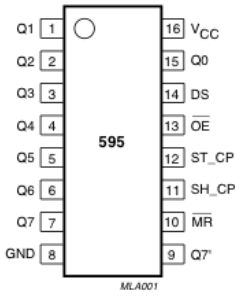
Shift Register Pins

Here is a table explaining the pin-outs adapted from the Phillip's datasheet.




| PINS 1-7, 15 | Q0 " Q7 | Output Pins |
|---|---|---|
| PIN 8 | GND | Ground, Vss |
| PIN 9 | Q7" | Serial Out |
| PIN 10 | MR | Master Reclear, active low |
| PIN 11 | SH_CP | Shift register clock pin |
| PIN 12 | ST_CP | Storage register clock pin (latch pin) |
| PIN 13 | OE | Output enable, active low |
| PIN 14 | DS | Serial data input |
| PIN 16 | Vcc | Positive supply voltage |