
# Practice 09

ECO CHAR

**Profesor:** Paz Rodríguez Héctor Manuel

**Grupo:** 3CV3

Ricardo Ruiz Maldonado
ESCUELA SUPERIOR DE CÓMPUTO | INSTITUTO POLITÉCNICO NACIONAL

# Theoretical reference

## 1 INTRODUCTION

### *USART:*

Is a piece of computer hardware that translates data between parallel and serial forms. UARTs are commonly used in conjunction with communication standards such as EIA, RS-232, RS-422 or RS-485. The universal designation indicates that the data format and transmission speeds are configurable. The electric signaling levels and methods (such as differential signaling etc.) are handled by a driver circuit external to the UART.

A UART is usually an individual (or part of an) integrated circuit used for serial communications over a computer or peripheral device serial port. UARTs are now commonly included in microcontrollers. A dual UART, or DUART, combines two UARTs into a single chip. An octal UART or OCTART combines eight UARTs into one package, an example being the NXP SCC2698. Many modern ICs now come with a UART that can also communicate synchronously; these devices are called USARTs (universal synchronous/asynchronous receiver/transmitter).

### *Data Transmiter – The USART Transmiter:*

The USART Transmitter is enabled by setting the Transmit Enable (TXEN) bit in the UCSRB Register. When the Transmitter is enabled, the normal port operation of the TxD pin is overridden by the USART and given the function as the Transmitter's serial output. The baud rate, mode of operation and frame format must be set up once before doing any transmissions. If synchronous operation is used, the clock on the XCK pin will be overridden and used as transmission clock.

### *Sending Frames with 5 to 8 Data Bits:*

A data transmission is initiated by loading the transmit buffer with the data to be transmitted. The CPU can load the transmit buffer by writing to the UDR I/O location. The buffered data in the transmit buffer will be moved to the Shift Register when the Shift Register is ready to send a new frame.

The Shift Register is loaded with new data if it is in idle state (no ongoing transmission) or immediately after the last stop bit of the previous frame is transmitted. When the Shift Register is loaded with new data, it will transfer one complete frame at the rate given by the baud register, U2X bit or by XCK depending on mode of operation.

### *Transmitter Flags and Iterrupts:*

The USART Transmitter has two flags that indicate its state: USART Data Register Empty (UDRE) and Transmit Complete (TXC). Both flags can be used for generating interrupts.

The Data Register Empty (UDRE) Flag indicates whether the transmit buffer is ready to receive new data. This bit is set when the transmit buffer is empty, and cleared when the transmit buffer contains data to be transmitted that has not yet been moved into the Shift Register. For compatibility with future devices, always write this bit to zero when writing the UCSRA Register.

When the Data Register Empty Interrupt Enable (UDRIE) bit in UCSRB is written to one, the USART Data Register Empty interrupt will be executed as long as UDRE is set (provided that global interrupts are enabled). UDRE is cleared by writing UDR. When interrupt-driven data transmission is used, the Data Register Empty interrupt routine must either write new data to UDR in order to clear UDRE or disable the Data Register Empty interrupt, otherwise a new interrupt will occur once the interrupt routine terminates.

The Transmit Complete (TXC) Flag bit is set to one when the entire frame in the transmit Shift Register has been shifted out and there are no new data currently present in the transmit buffer. The TXC Flag bit is automatically cleared when a transmit complete interrupt is executed, or it can be cleared by writing a one to its bit location. The TXC Flag is useful in half-duplex communication interfaces (like the RS-485 standard), where a transmitting application must enter receive mode and free the communication bus immediately after completing the transmission.

When the Transmit Compete Interrupt Enable (TXCIE) bit in UCSRB is set, the USART Transmit Complete Interrupt will be executed when the TXC Flag becomes set (provided that global interrupts are enabled). When the transmit complete interrupt is used, the interrupt handling routine does not have to clear the TXC Flag, this is done automatically when the interrupt is executed.

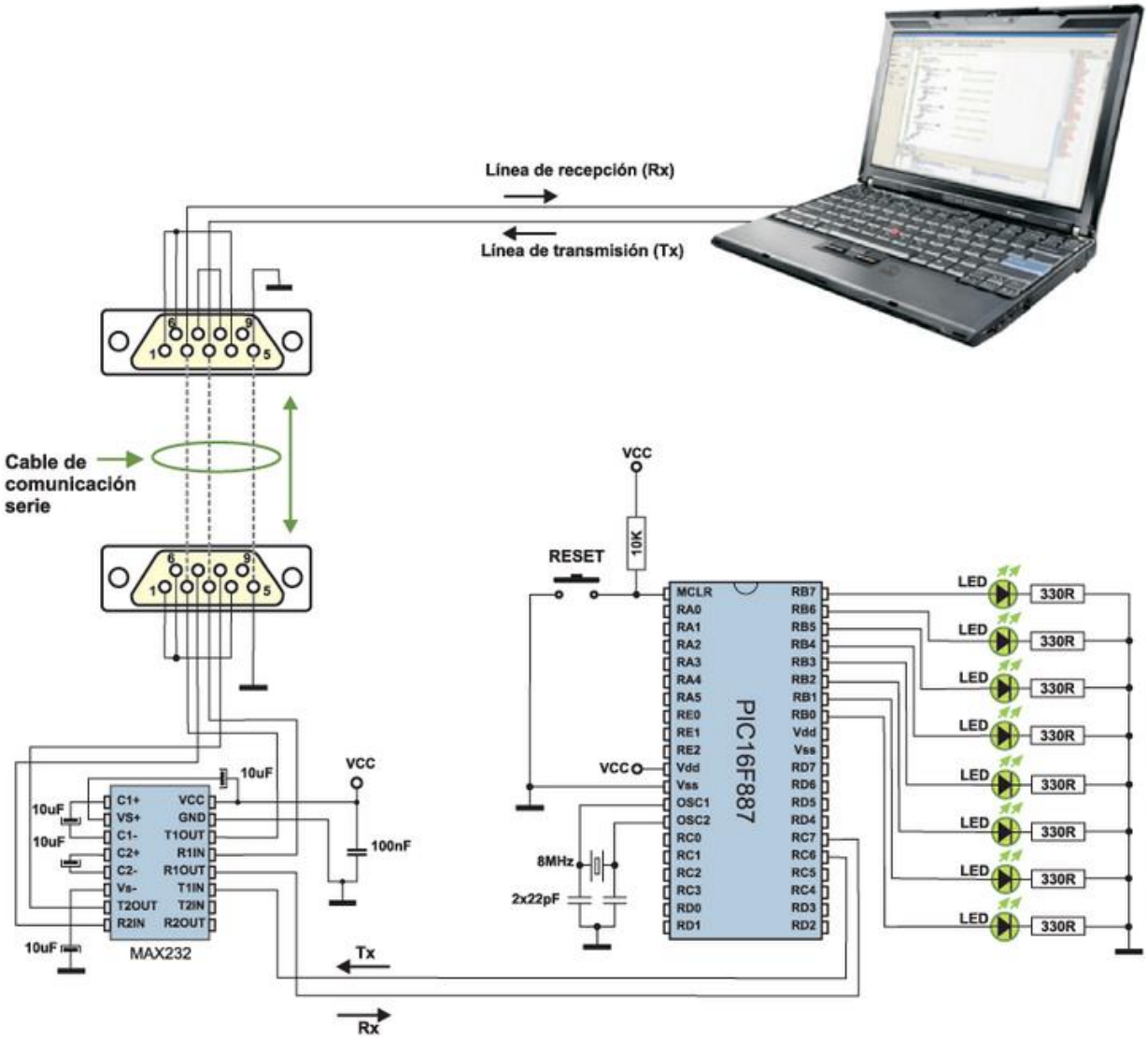
# 2 MATERIAL

- Pazuino
- Serial/usb wire

# 3 DEVELOPMENT

This example shows how to use the EUSART module microcontroller. The connection between the microcontroller and a PC is established in accordance with the standard RS-232 communication. The program works as follows. Each byte received via the serial communication is displayed when using the LEDs connected to PORTB and then automatically returns to the

transmitter. The easiest way is to check the operation of the device in practice to use a standard Windows program called Hyper Terminal.




# 4 CODE

```
; Author : Ricardo Ruiz Maldonado
; Practica 9    - Eco Caracter

        .include "m8535def.inc"
        .cseg       ;QUE TODO LO QUE SIGUE VA A LA MEMORIA DE CODIGO
        .org $0     ;DESDE DIRECCION CERO EMPIEZA
        rjmp INICIO

INICIO: LDI     R16,    LOW(RAMEND)     ;------------------------
        OUT     SPL,    R16             ;    INICIALIZAMOS EL
        LDI     R16,    HIGH(RAMEND)    ;    STACK POINTER
        OUT     SPH,    R16             ;------------------------

        LDI     R16,    79              ;SE CONFIGURA LA FRECUENCIA 9600@12MHz
        OUT     UBRRL,  R16             ;

        SBI     UCSRB,  RXEN            ;SE ENCIENDE EN MODO DE RECEPCION

        LDI     R16,    $FF             ;VALOR DE FF PARA MANDAR COMO
                                        ;   SALIDA TODO EL PUERTO
        OUT     DDRB,   R16             ;PUERTO B COMO SALIDA

DATO:   SBIS    UCSRA,  RXC             ;SE ESPERA DATO RECIBIDO
        RJMP    DATO
        IN      R16,    UDR             ;LEE DATO RECIBIDO
        OUT     PORTB,  R16             ;ESCIRBE DATO EN PUERTO B

        SBI     UCSRB, TXEN
        OUT     UDR,    R16

LOOP:   SBIS    UCSRA,  UDRE            ;SE ESPERA EL FIN DE TRANSMICION DEL CARACTER
        RJMP    LOOP

DELAY1: LDI     R22,    $14
        RJMP    DLY1
DLY1:   DEC     R20
        BRNE    DLY1
        DEC     R21
        BRNE    DLY1
        DEC     R22
        BRNE    DLY1
        RJMP    INICIO
```

# 5 CONCLUSIONES

La transmisión y recepción full dúplex es de gran utilidad pues muchas veces no solo necesitaremos enviar o recibir datos, sino que necesitaremos ambos en el mismo programa