Summary in Graph

Exam Summary (GO Classes Test Series 2024 | Digital Logic | Test 3)

Qs. Attempted:	**12** (4 + 8)	**Correct Marks:**	**15** (3 + 12)
Correct Attempts:	**9** (3 + 6)	**Penalty Marks:**	**1** (0.33 + 0.67)
Incorrect Attempts:	**3** (1 + 2)	**Resultant Marks:**	**14** (2.66 + 11.33)

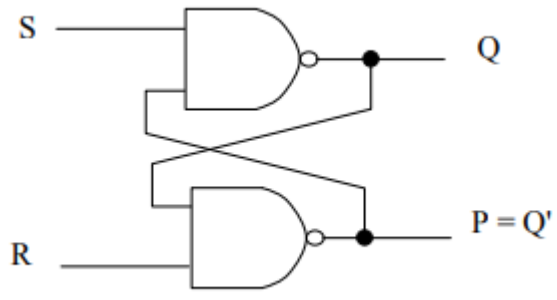
Total Questions:	**15** (5 + 10)
Total Marks:	**25** (5 + 20)
Exam Duration:	**45 Minutes**
Time Taken:	**45 Minutes**

EXAM RESPONSE | EXAM STATS | FEEDBACK

Technical

Q #1 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

A flip-flop can be constructed from two NAND gates connected as follows:



What restriction must be placed on S and R so that P always equals Q'?

A. we do not allow the $R = S = 0$ state.
B. we do not allow the $R = S = 1$ state.
C. we do not allow the $R = 0, S = 1$ state.
D. P is always equal to Q' regardless of the inputs S, P.

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #2 | Multiple Select Type | Award: 1 | Penalty: 0 | Digital Logic

Consider the following decimal numbers. Which of the following decimal numbers Do Not have an exact representation in binary notation?

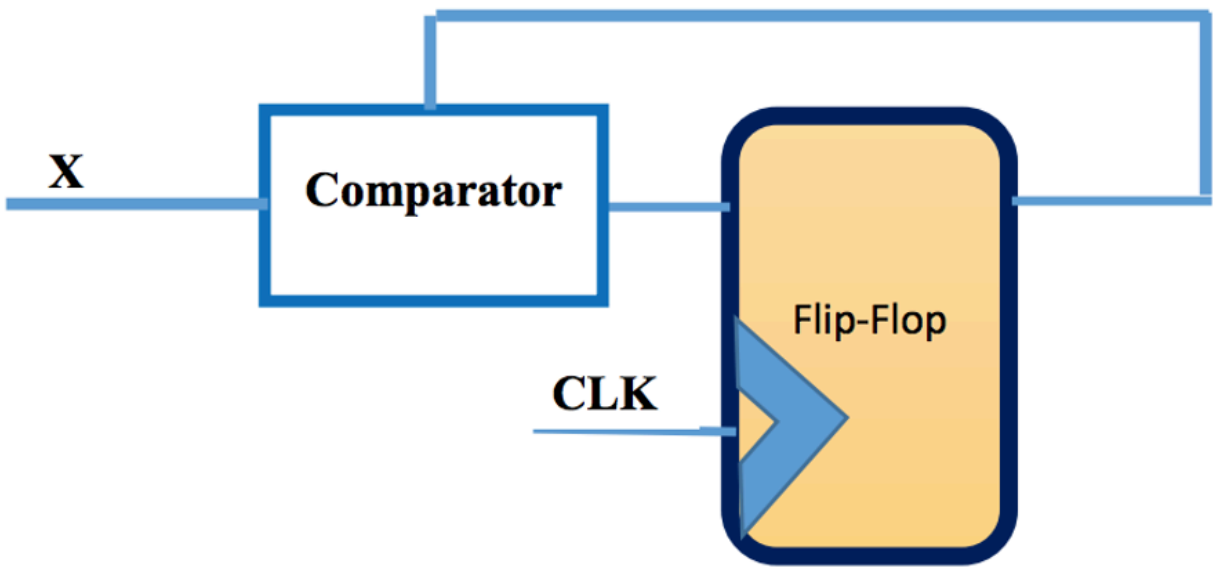
A. $U = 0.1$
B. $V = 0.3$
C. $X = 0.4$
D. $Z = 0.5$

Your Answer: A;B;C | Correct Answer: A;B;C | Correct | Discuss

Q #3 | Numerical Type | Award: 1 | Penalty: 0 | Digital Logic

A D flip-flop has a hold time of $3\ ns$, a setup time of $5\ ns$, and a propagation delay from the rising edge of the clock to the change in flip- flop output in the range of 6 to $12\ ns$. A comparator (combinational circuit) unit delay is $2\ ns$.

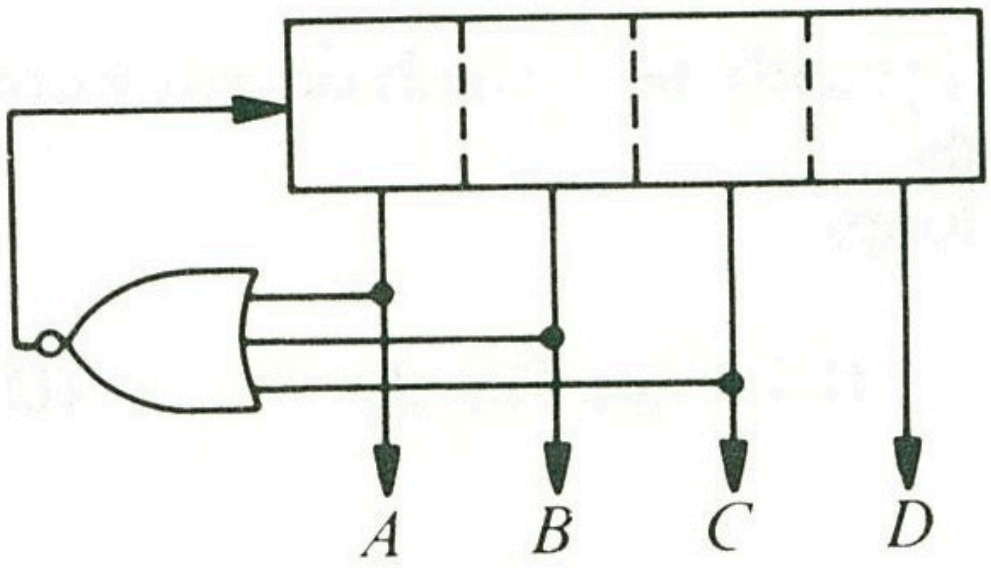
What is the shortest clock period(in ns) for proper operation of the circuit below (i.e. the circuit should not violate the timing constraints) ?



Your Answer: | Correct Answer: 19 | Not Attempted | Discuss

Q #4 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

The figure below shows a 4-bit, right shift register, and a NOR gate. If the register outputs $\{ABCD\}$ at time 0 are 0110, then their values 4 clock pulses later are :



A. 0100
B. 0110

C. 0111
D. 1000

Your Answer: A **Correct Answer: A** Correct Discuss

Q #5 Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

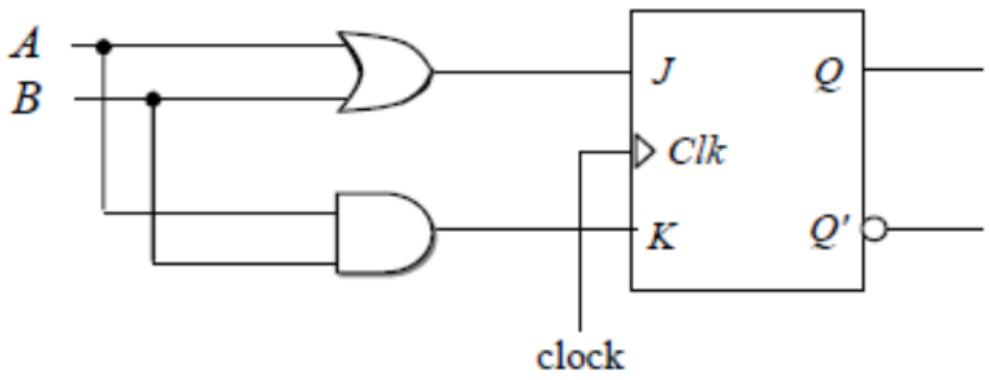
Which of the following flip flops can be made to emulate all other flip flops without any additional hardware (except probably a NOT gate)?

A. JK flipflop
B. SR flipflop
C. T flipflop
D. D flipflop

Your Answer: B **Correct Answer: A** Incorrect Discuss

Q #6 Multiple Select Type | Award: 2 | Penalty: 0 | Digital Logic

A new flip-flop, called AB flip-flop, is created as shown below. What does the flip-flop do?

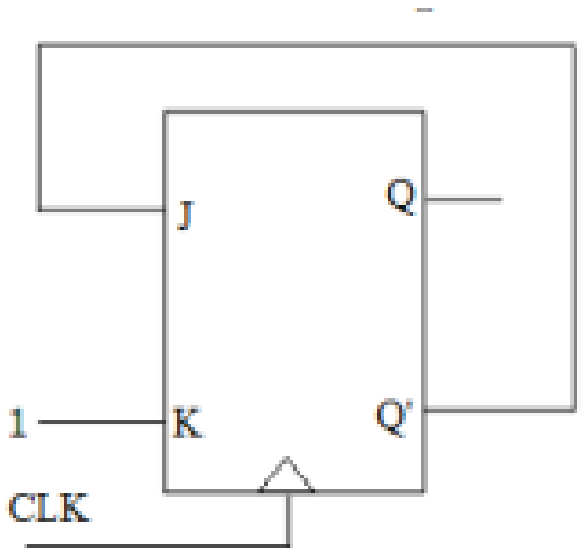


A. Set command when $A = 0, B = 0$
B. Reset command when $A = 0, B = 1$
C. Hold command when $A = 1, B = 0$
D. Toggle command when $A = 1, B = 1$

Your Answer: B;D **Correct Answer: D** Incorrect Discuss

Q #7 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

What will the output sequence of the following JK flip flop be after 7 clock pulses?



A. 0101011
B. 0110011
C. 0110110
D. 0101010

Your Answer: | Correct Answer: D | Not Attempted | Discuss

Q #8 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

An XY flip-flop operates as indicated by the following table :

Input(X)	Input(Y)	Current State	Next State
X	Y		
0	0	Q	1
0	1	Q	$\overline{Q}$
1	1	Q	0
1	0	Q	Q

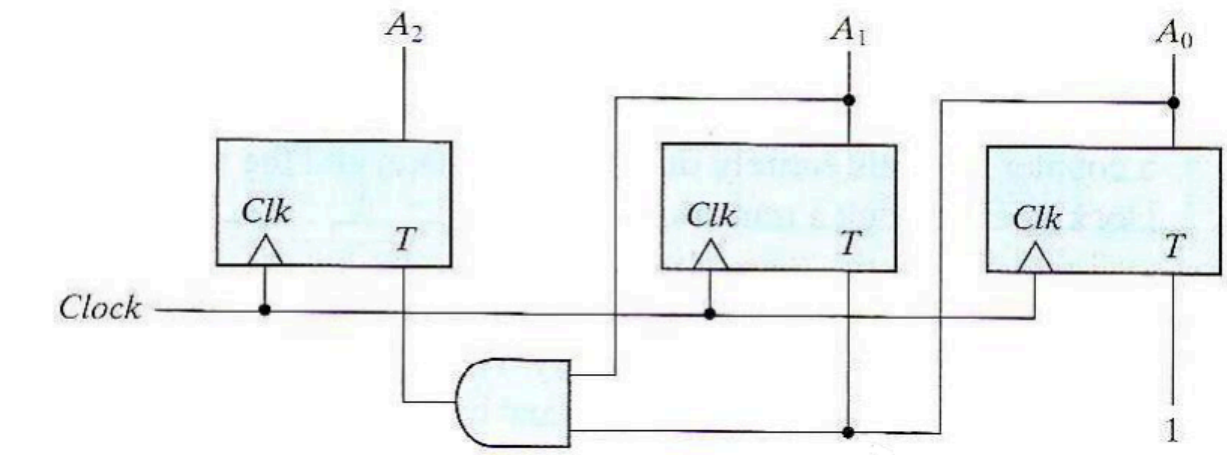
Which of the following expresses the next state in terms of the X and Y inputs and the current state Q?

A. $(\overline{X} \wedge \overline{Q}) \vee (\overline{Y} \wedge Q)$
B. $(\overline{Y} \wedge \overline{Q}) \vee (\overline{X} \wedge Q)$
C. $(X \wedge \overline{Q}) \vee (Y \wedge Q)$
D. $(\overline{Y} \wedge \overline{Q}) \vee (\overline{Q} \wedge X)$

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #9 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Consider the circuit given below with initial state $A_1 = 1, A_2 = A_0 = 0$. The state of the circuit is given by the value $4A_2 + 2A_1 + A_0$



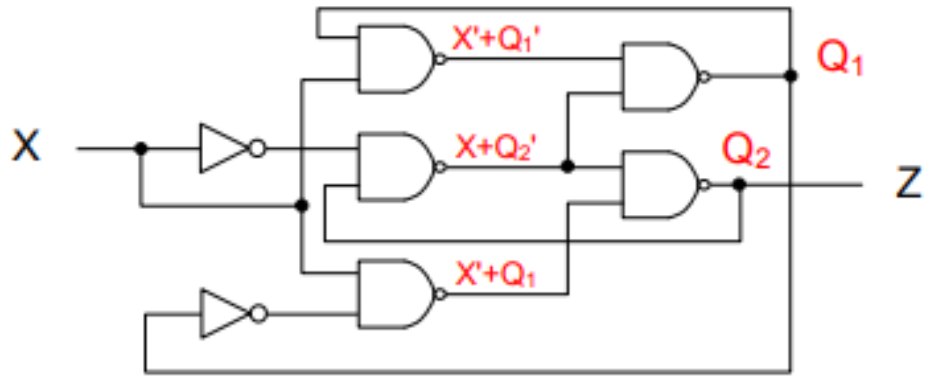
Which one of the following is the correct state sequence of the circuit?

A. $2, 1, 0, 7, 6, 5, 4, 3$
B. $2, 4, 6, 0, 2, 4, 6, 0$
C. $2, 3, 4, 5, 6, 7, 0, 1$
D. None of the above.

Your Answer: C | Correct Answer: C | Correct | Discuss

Q #10 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Analyze the following asynchronous network. Starting in the total stable state for which $X = Z = 0$, what will be the output sequences Z when the input sequence is $X = 0, 1, 0, 1, 0, 1, \ldots$



A. The output will be $Z = 0\ 1\ 1\ 0\ 0\ 1\ 1\ 0\ \ldots$
B. The output will be $Z = 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ 0\ 1\ \ldots$
C. The output will be $Z = 0\ 1\ 1\ 1\ 0\ 0\ 0\ 1\ 1\ 1\ \ldots$
D. The output will be $Z = 0\ 1\ 0\ 0\ 1\ 0\ 0\ 1\ 0\ 0\ \ldots$

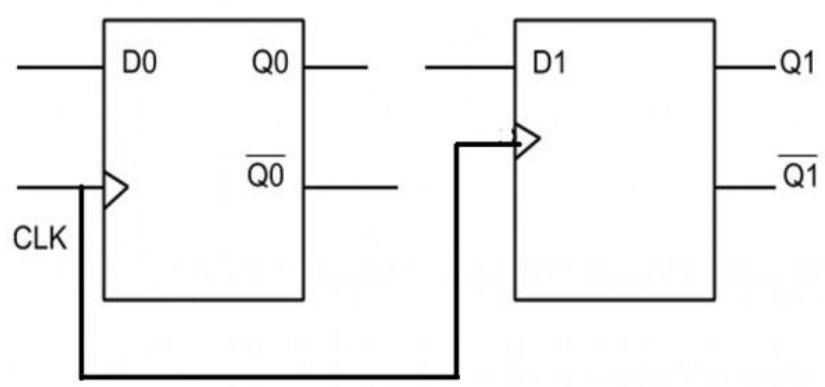
Your Answer: | Correct Answer: A | Not Attempted | Discuss

Q #11 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Two D Flip flops are connected as a synchronous counter that goes through the following sequence

$$00 \rightarrow 01 \rightarrow 11 \rightarrow 10 \rightarrow 00$$

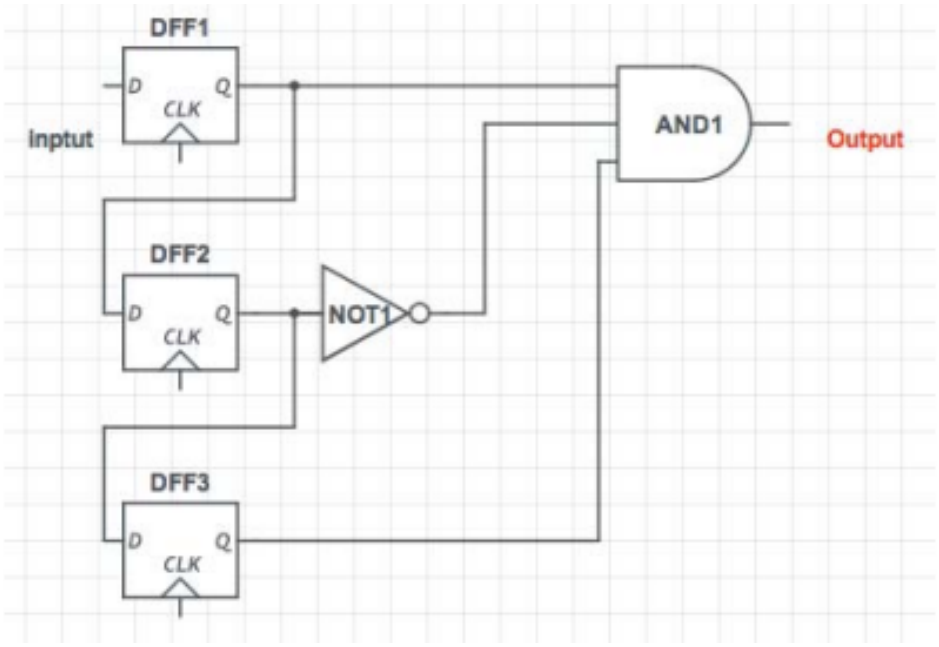
Inputs D_0 and D_1 should be connected as (Flip flop D_1 provides the MSB)



A. $\overline{Q}_1$ and Q_0
B. $\overline{Q}_0$ and Q_1
C. $\overline{Q}_1 Q_0$ and $\overline{Q}_0 Q_1$
D. $\overline{Q}_0 \overline{Q}_1$ and $Q_0 Q_1$

Your Answer: B | Correct Answer: A | Incorrect | Discuss

Q #12 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic



The pattern detected by the above circuit is?

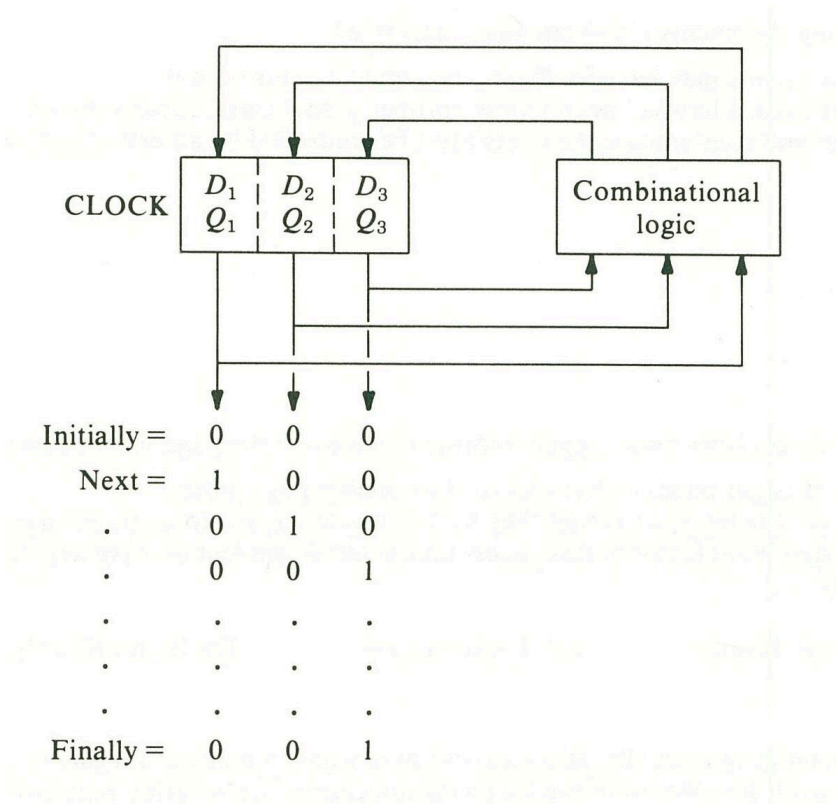
A. 100
B. 010
C. 110
D. 101

Your Answer: D | Correct Answer: D | Correct | Discuss

Q #13 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

The figure below shows a control circuit, consisting of a 3 -bit register(all the three flip flops of the register are D flip flops) and some combinational logic. This circuit is initially in the state $Q_1Q_2Q_3 = 000$. On subsequent clock pulses, the circuit is required to generate the control sequence:

$$(100) \rightarrow (010) \rightarrow (001) \rightarrow (001) \rightarrow (001) \rightarrow \ldots$$



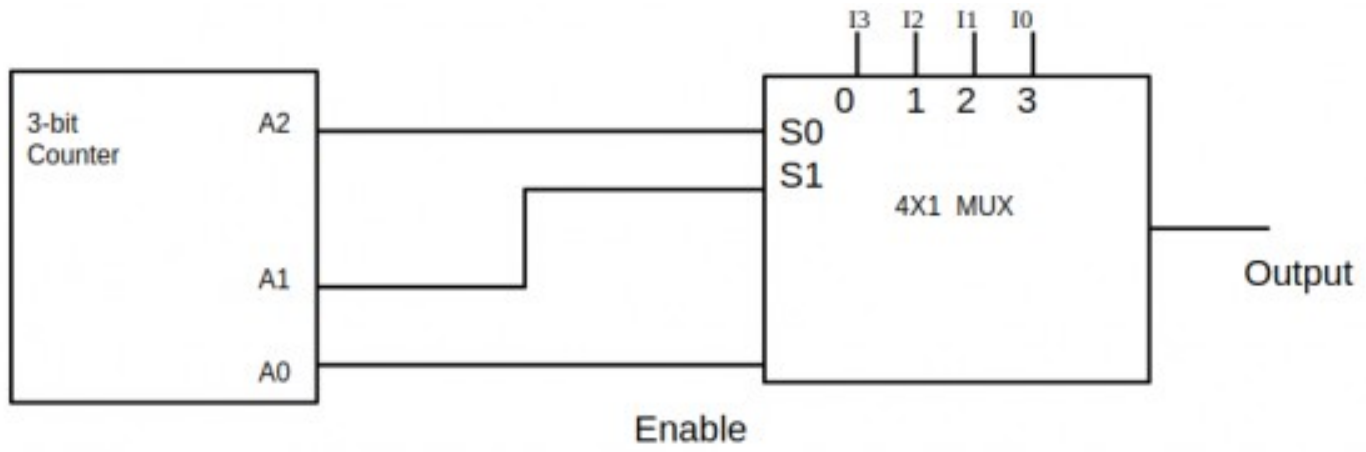
Which of the following is a correct set of equations to be implemented by the combinational logic?

A. $D_1 = \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}, D_2 = Q_1, D_3 = Q_2 \vee Q_3|$
B. $D_1 = \overline{Q_1}\ \overline{Q_2}\ \overline{Q_3}, D_2 = Q_1\overline{Q_2Q_3}, D_3 = \overline{Q_1}Q_2\overline{Q_3}$
C. $D_1 = \overline{Q_1}, D_2 = \overline{Q_2}, D_3 = \overline{Q_3}$
D. $D_1 = Q_3, D_2 = Q_1, D_3 = Q_2$

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #14 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

A 3 bit down counter is used to control the output of the multiplexer as shown in the figure. The counter is initially at $A_2A_1A_0 = 101$, the output of multiplexer will follow the sequence:(Output of mux is controlled by select lines, $S1S0$)

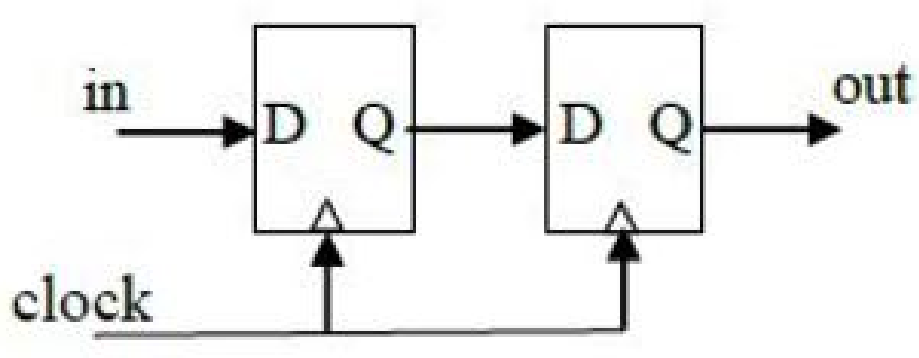


A. $I_2, 0, I_1, 0 \ldots$
B. $I_1, 0, I_2, 0 \ldots$
C. $I_1, 0, 0, I_2 \ldots$
D. $I_2, I_1, I_2, 0 \ldots$

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #15 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Consider the circuit below. If 'in' and 'out' were both 0, to begin with, and 'in' suddenly becomes 1, how many clock pulses later will out become '1' as well?



A. 1
B. 2
C. 3
D. 4

Your Answer: B | Correct Answer: B | Correct | Discuss

You're doing good, you can target above 70 percentage!

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