Summary in Graph

Exam Summary (GO Classes Test Series 2024 | CO and Architecture | Test 1)

Qs. Attempted:	**13** 5 + 8	**Correct Marks:**	**16** 4 + 12
Correct Attempts:	**10** 4 + 6	**Penalty Marks:**	**0.67** 0 + 0.67
Incorrect Attempts:	**3** 1 + 2	**Resultant Marks:**	**15.33** 4 + 11.33

Total Questions:	**15** 5 + 10
Total Marks:	**25** 5 + 20
Exam Duration:	**45 Minutes**
Time Taken:	**13 Minutes**

EXAM RESPONSE | EXAM STATS | FEEDBACK

Technical

Q #1 Numerical Type | Award: 1 | Penalty: 0 | CO and Architecture

Consider the following PC-relative addressing mode instruction of RISC instruction set architecture. $\mathrm{I1}$: 1000 : BEQ R1, R2, label $\mathrm{I2}$: 1004 : ADD R1, R2, R3 Where the label is used as an offset and 1000 is the memory location from where instruction $\mathrm{I1}$ is fetched. $\mathrm{R1}, \mathrm{R2}$, and $\mathrm{R3}$ are general purpose registers. The BEQ instruction branches the PC if the first source register's contents and the second source register's contents are equal. If $\mathrm{R1} = 0; \mathrm{R2} = 0$ and label $= 20$, what is the memory address of the next instruction to be executed?

Your Answer: 1024 | **Correct Answer: 1024** | Correct | Discuss

Q #2 Numerical Type | Award: 1 | Penalty: 0 | CO and Architecture

A digital computer has a memory unit with 32 bits per word. The instruction set consists of 110 different operations. All instructions have an operation code part (opcode) and two address fields: one for a memory address and one for a register address. This particular system includes eight general-purpose, user-addressable registers. Registers may be loaded directly from memory, and memory may be updated directly from the registers. Direct memory-to-memory data movement operations are not supported. Each instruction is stored in one word of memory. If $\mathrm{X}, \mathrm{Y}, \mathrm{Z}$ represent the number of bits that are needed for the opcode, for the register field, and bits that are left for the memory address part of the instruction, respectively, then $\mathrm{XY} + \mathrm{YZ}$ is _____

Your Answer: 87 | Correct Answer: 87 | Correct | Discuss

Q #3 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | CO and Architecture

The unsigned integer $3,505,468,161$ can be written in 32-bit binary as $11010000\ 11110001\ 00110011\ 00000001$. Putting it into four bytes of memory beginning at address 98370 in little-endian fashion would give which picture?

A.

98370	98371	98372	98373
11010000	111100001	00110011	00000001

B.

98370	98371	98072	98373
00000001	111100001	00110011	11010000

C.

98370	98371	98372	98373
00000001	00110011	11110001	11010000

D.

98370	98371	98372	98373
00110011	00000001	11010000	111100001

Your Answer: C | Correct Answer: C | Correct | Discuss

Q #4 | Multiple Select Type | Award: 1 | Penalty: 0 | CO and Architecture

When performing hardware integer arithmetic, we say that overflow has occurred when the mathematically correct result of a computation cannot be represented in the number of bits available for the type being used. Obviously, it is important to be able to detect when an overflow error has occurred.

For the following options, the bit-sequences are 16-bit 2's complement representations of (signed) integer values. For which of the following an overflow occurs when the given two integers are added?

A. $0111\ 1001\ 1011\ 1011 + 0011\ 1011\ 1110\ 1110$
B. $1111\ 0111\ 0110\ 1001 + 1000\ 0001\ 0110\ 0100$
C. $0001\ 1100\ 0110\ 1111 + 1111\ 0111\ 1110\ 1101$
D. $1100\ 1011\ 1010\ 1101 + 0111\ 1111\ 0010\ 1111$

Your Answer: A;B | Correct Answer: A;B | Correct | Discuss

Q #5 | Multiple Select Type | Award: 1 | Penalty: 0 | CO and Architecture

Consider the control unit that adopts the single address field branch control logic. Assume that the control memory is 24 bits wide. The control portion of the micro-instruction format is divided into two fields. A micro-operation field of 13 bits specifies the micro-operations to be performed. An address selection field specifies 8 conditions that will cause a micro-instruction branch.

Which of the following is/are true?

A. 8 bits are in the address selection field
B. 8 bits are in the address field
C. the size of the control memory is 768 Bytes
D. the size of the control memory is 4096 bits.

Your Answer: B | Correct Answer: B;C | Incorrect | Discuss

Q #6 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

A CPU has an arithmetic unit that adds bytes and then sets its V, C, and Z flag bits as follows. The V-bit is set if arithmetic overflow occurs (in two's complement arithmetic). The C-bit is set if a carry-out is generated from the most significant bit during an operation. The Z-bit is set if the result is zero.
What are the values of the V, C, and Z flag bits (in that order) after the 8-bit bytes $1100\ 1100$ and $1000\ 1111$ are added?

A. 000
B. 110
C. 111
D. 001

Your Answer: B | Correct Answer: B | Correct | Discuss

Q #7 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

Consider the following :

Consider the instruction Load R5, X(R7) which uses the Index addressing mode to load a word of data from memory location X + [R7] into register R5.

Execution of this instruction involves the following actions:

- $(\mathrm{I1})$ Fetch the instruction from the memory.
- $(\mathrm{I2})$ Decode the instruction to determine the operation to be performed.
- $(\mathrm{I3})$ Add the immediate value X to the contents of R7.
- $(\mathrm{I4})$ Read register R7.
- $(\mathrm{I5})$ Use the sum X + [R7] as the effective address of the source operand, and read the contents of that location in the memory.
- $(\mathrm{I6})$ Increment the program counter.
- $(\mathrm{I7})$ Load the data received from the memory into the destination register, R5.

Which of the following is the most preferred order of execution of the above instruction?

A. $\mathrm{I1} \rightarrow \mathrm{I2} \rightarrow \mathrm{I3} \rightarrow \mathrm{I4} \rightarrow \mathrm{I5} \rightarrow \mathrm{I6} \rightarrow \mathrm{I7}$
B. $\mathrm{I1} \rightarrow \mathrm{I2} \rightarrow \mathrm{I6} \rightarrow \mathrm{I3} \rightarrow \mathrm{I4} \rightarrow \mathrm{I5} \rightarrow \mathrm{I7}$
C. $\mathrm{I1} \rightarrow \mathrm{I6} \rightarrow \mathrm{I2} \rightarrow \mathrm{I4} \rightarrow \mathrm{I3} \rightarrow \mathrm{I5} \rightarrow \mathrm{I7}$
D. $\mathrm{I1} \rightarrow \mathrm{I6} \rightarrow \mathrm{I2} \rightarrow \mathrm{I5} \rightarrow \mathrm{I4} \rightarrow \mathrm{I3} \rightarrow \mathrm{I7}$

Your Answer: C | Correct Answer: C | Correct | Discuss

Q #8 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

	Micro-operations	Active Control Signals
Fetch:	t_1: MAR ← (PC)	C_2
	t_2: MBR ← Memory PC ← (PC) + 1	C_5, C_R
	t_3: IR ← (MBR)	C_4
Indirect:	t_1: MAR ← (IR(Address))	C_8
	t_2: MBR ← Memory	C_5, C_R
	t_3: IR(Address) ← (MBR(Address))	C_4
Interrupt:	t_1: MBR ← (PC)	C_1
	t_2: MAR ← Save-address PC ← Routine-address	
	t_3: Memory ← (MBR)	C_{12}, C_W

C_R = Read control signal to system bus.
C_W = Write control signal to system bus.

Let us define control signals, P and Q, that have the following interpretation

- $\mathrm{PQ} = 00$ Fetch cycle
- $\mathrm{PQ} = 01$ Indirect cycle
- $\mathrm{PQ} = 10$ Execute cycle
- $\mathrm{PQ} = 11$ Interrupt cycle

Which of the following expression boolean expression defines C_4?

A. $\mathrm{P}'t_3$
B. $Pt_3' + Q't_3$
C. $P'Q't_3 + PQ't_3$
D. $P'Q't_3 + PQt_3$

Your Answer: | **Correct Answer: A** | Not Attempted | Discuss

Q #9 Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

The 8-bit registers M, N, O and P initially have the following values.

$$\mathrm{M} = 10001111; \mathrm{N} = 01100010; \mathrm{O} = 01001001; \mathrm{P} = 01110010$$

The following assembly code is executed:

- $\mathrm{M} \leftarrow \mathrm{M} \oplus \mathrm{N}$
- $\mathrm{M} \leftarrow \mathrm{CSL\ M}$
- $\mathrm{N} \leftarrow \mathrm{M}+\mathrm{N}$
- $\mathrm{O} \leftarrow \mathrm{O} \wedge \mathrm{N}$
- $\mathrm{O} \leftarrow \mathrm{CSR\ O}$
- $\mathrm{P} \leftarrow \mathrm{P} + 1$
- $\mathrm{P} \leftarrow \mathrm{P} + \mathrm{O}$

Determine the 8-bit values in each register after the execution of the above sequence of micro-operations.
CSL : Circular shift left; CSR : Circular shift right; $\wedge$: logical AND; $+$: Arithmetic addition
$\oplus$: logical Ex-or.

A. $\mathrm{M} = 11101101; \mathrm{N} = 00111101; \mathrm{O} = 10000100; \mathrm{P} = 11110111$
B. $\mathrm{M} = 11011011; \mathrm{N} = 00111101; \mathrm{O} = 10000100; \mathrm{P} = 11110111$
C. $\mathrm{M} = 11011011; \mathrm{N} = 10111101; \mathrm{O} = 10000100; \mathrm{P} = 11110111$
D. $\mathrm{M} = 11011011; \mathrm{N} = 00111101; \mathrm{O} = 00001001; \mathrm{P} = 01110011$

Your Answer: B | Correct Answer: B | Correct | Discuss

Q #10 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

A particular parallel program computation requires 100 seconds when executed on a single processor. If 40 percent of this computation is “inherently sequential” (i.e., will not benefit from additional processors), then the theoretically best possible elapsed times for this program running with 2 and 4 processors, respectively, are

A. 20 seconds and 10 seconds
B. 50 seconds and 25 seconds
C. 70 seconds and 55 seconds
D. 80 seconds and 70 seconds

Your Answer: C | Correct Answer: C | Correct | Discuss

Q #11 | Numerical Type | Award: 2 | Penalty: 0 | CO and Architecture

A 64-bit processor has 64 registers and uses a 20-bit instruction format. It has two types of instructions : M-type and R-type. Each M-type instruction contains an opcode and a memory address. Each R-type instruction contains an opcode and two register names. Main memory is $8\mathrm{K}$ words, and it is byte addressable. If there are 10 distinct M-type opcodes, then the maximum number of distinct R-type opcodes is _____

Your Answer: 236 | Correct Answer: 96 | Incorrect | Discuss

Q #12 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

Amdahl's Law pertains to the speedup achieved when running a program on parallel processors versus using a single serial processor. In this context, the speedup is the ratio of original running time to improved running time. According to Amdahl's Law, approximately how much speedup could we expect for an unlimited number of processors if 10 percent of a program is sequential(i.e., will not benefit from additional processors) and the remaining part is ideally parallel?

A. $10\mathrm{X}$
B. $20\mathrm{X}$
C. $40\mathrm{X}$
D. Infinite

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #13 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

Following is a definition of a **widget** and a declaration of an array A that contains 10 widgets. The sizes of a byte, short, Int, and long are $1, 2, 4$ and 8 byte, respectively. Alignment is restricted so that an n-byte field must be located at an address divisible by n.
The fields in a struct are not rearranged; padding is used to ensure alignment. All widgets in A must have the same size.

```
   struct widget
       short s
       byte b
       long l
5.     int i
   end widget

   widget A[10]
```

Assuming that A is located at a memory address divisible by 8, what is the total size of A, in bytes?

A. 150
B. 160
C. 2001
D. 240

Your Answer: B **Correct Answer: D** Incorrect Discuss

Q #14 Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

Consider two different design enhancements of ALU as follows:

i. A part of a bigger task is improved twenty times than it was before. The other part of the same task constitutes 60% of the overall task time, and it remains unchanged.
ii. The designer can make changes to improve 20% of the task 100% faster, 35% of the task 4 times faster, and 10% of the task 100 times faster, but it causes the remaining part of the task to perform as bad as 50% slower than before.

Which of the following value is the best approximate difference between the two speedups achieved in those two improvements:

A. 0.3567
B. 0.2667
C. 0.4875
D. 0.4325

Your Answer: C **Correct Answer: C** Correct Discuss

Q #15 Numerical Type | Award: 2 | Penalty: 0 | CO and Architecture

Big-Endian(BE) and Little-Endian(LE) change the order in which the bytes of a word are stored in RAM. We typically show the contents of a word, especially if it's an integer, as four hexadecimal pairs of characters. For example, the hex string 0xabcdef12 contains four bytes: "ab" is the first, which have the binary value of 1010 and 1011. So the first 8 bits are 10101011. BE/LE specifies whether this byte goes into RAM as the first of the four bytes in the word or as the last. Suppose Byte 0 in RAM contains the value 0x00. Subsequent bytes contain 0x01,0x40, and 0x70. On a Big-Endian system with a 32-bit word, what's the decimal value of the word?

Your Answer: **Correct Answer: 82032** Not Attempted Discuss

You're doing good, you can target above 70 percentage!

Copyright & Stuff