Summary in Graph

Exam Summary (GO Classes Test Series 2024 | Digital Logic | Test 2)

Qs. Attempted:	**13** (5 + 8)	**Correct Marks:**	**17** (3 + 14)
Correct Attempts:	**10** (3 + 7)	**Penalty Marks:**	**0** (0 + 0)
Incorrect Attempts:	**3** (2 + 1)	**Resultant Marks:**	**17** (3 + 14)

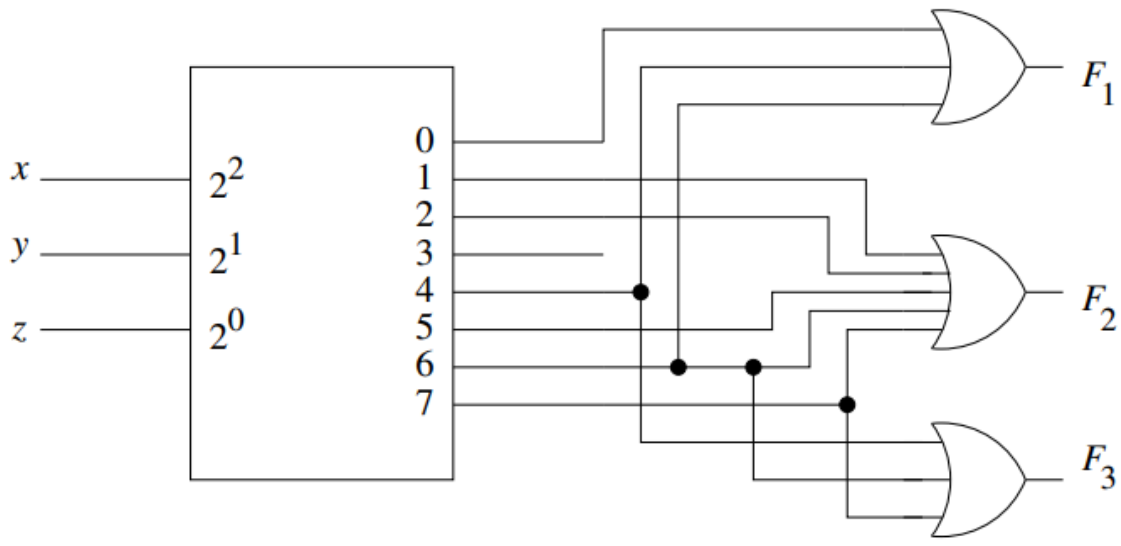
Total Questions:	**15** (5 + 10)
Total Marks:	**25** (5 + 20)
Exam Duration:	**45 Minutes**
Time Taken:	**45 Minutes**

EXAM RESPONSE | EXAM STATS | FEEDBACK

Technical

Q #1 | Numerical Type | Award: 1 | Penalty: 0 | Digital Logic

Consider the following combinational circuit using a decoder and OR gates, implementing three Boolean functions $\mathrm{F}_1, \mathrm{F}_2, \mathrm{F}_3$:



For how many input combinations (x, y, z), at least two of these boolean functions are high?

Your Answer: 4 | Correct Answer: 3 | Incorrect | Discuss

Q #2 Numerical Type | Award: 1 | Penalty: 0 | Digital Logic

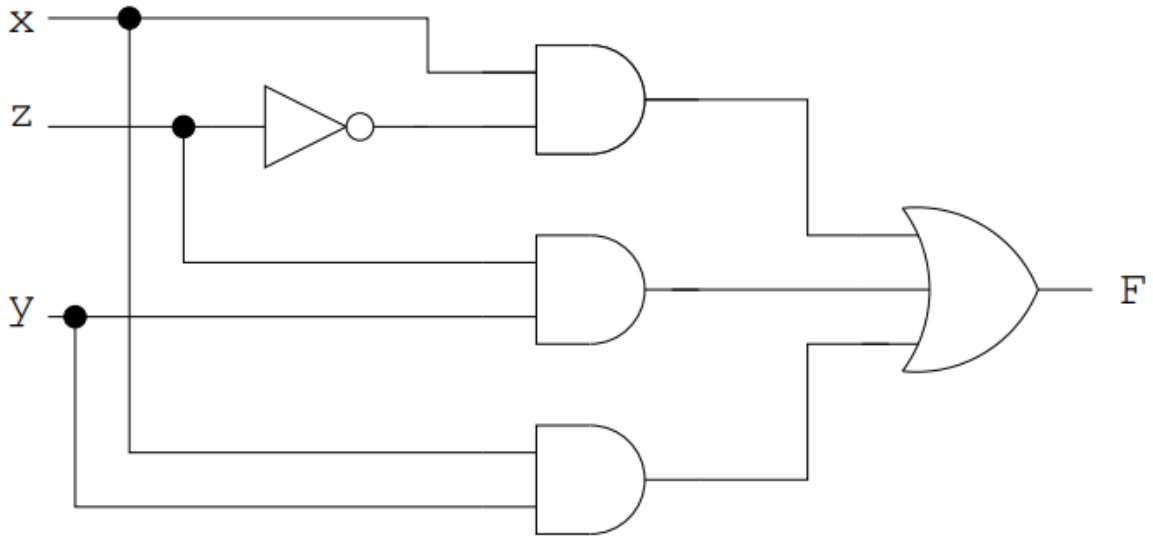
An 8×1 multiplexer has inputs A, B and C connected to the selection inputs $\mathrm{S}_2(\mathrm{MSB}), \mathrm{S}_1$, and $\mathrm{S}_0(\mathrm{LSB})$ respectively. The data inputs through I_0 through I_7 are as follows:

$$\mathrm{I}_1 = \mathrm{I}_2 = \mathrm{I}_4 = 0; \mathrm{I}_3 = \mathrm{I}_5 = 1; \mathrm{I}_0 = \mathrm{I}_7 = \mathrm{D}; \text{ and } \mathrm{I}_6 = \overline{\mathrm{D}}$$

Consider the Boolean function $\mathrm{F}(\mathrm{A}, \mathrm{B}, \mathrm{C}, \mathrm{D})$ that this multiplexer implements. How many minterms of F are there for which F is 1?

Your Answer: 6 | **Correct Answer: 7** | Incorrect | Discuss

Q #3 Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

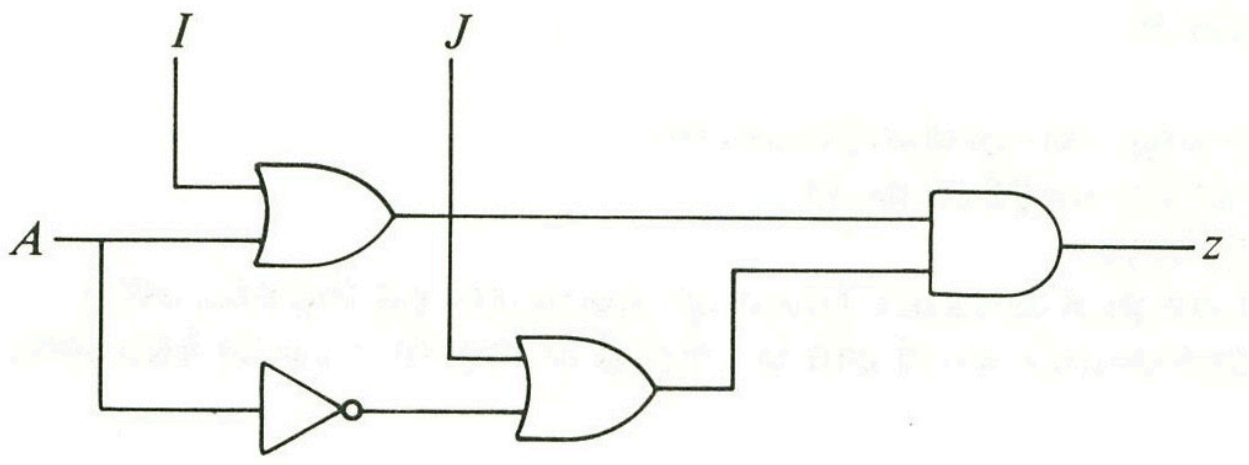


The figure above implements the Boolean function:

A. $\mathrm{F}(\mathrm{x}, \mathrm{y}, \mathrm{z}) = \Sigma(2, 3, 5, 6)$
B. $\mathrm{F}(\mathrm{x}, \mathrm{y}, \mathrm{z}) = \Sigma(3, 4, 6, 7)$
C. $\mathrm{F}(\mathrm{x}, \mathrm{y}, \mathrm{z}) = \Sigma(1, 3, 6, 7)$
D. $\mathrm{F}(\mathrm{x}, \mathrm{y}, \mathrm{z}) = \Sigma(0, 2, 4, 6)$

Your Answer: B | **Correct Answer: B** | Correct | Discuss

Q #4 Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic



The circuit above is to be used to implement the function $\mathrm{z} = \mathrm{f}(\mathrm{A}, \mathrm{B}) = \overline{\mathrm{A}} + \mathrm{B}$. Inputs I and J can be selected from the set $\{0, 1, \mathrm{B}, \overline{\mathrm{B}}\}$.

What values should be chosen for I and J?

A. $\mathrm{I} = 0, \mathrm{J} = \mathrm{B}$
B. $\mathrm{I} = 1, \mathrm{J} = \mathrm{B}$
C. $\mathrm{I} = \mathrm{B}, \mathrm{J} = 1$

D. $\mathrm{I} = \overline{\mathrm{B}}, \mathrm{J} = 0$

Your Answer: B **Correct Answer: B** Correct Discuss

Q #5 Multiple Choice Type | Award: 1 | Penalty: 0.33 | Digital Logic

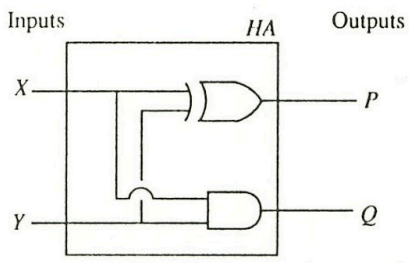
Which of the following is the correct function for Full adder where inputs ' a ' and 'b' are the numbers added, and input 'c' is the carry-in. Also, 's' and 'co' are sum and carry out, respectively.

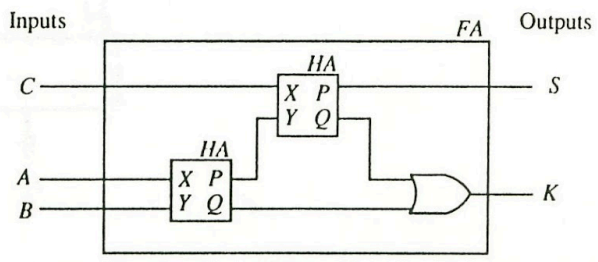
A. $co = bc + ac + ab; s = a$ xor b xor c
B. $co = b'c + a'c + ab; s = a$ xor b xor c
C. $co = bc + ac + a'b'; s = a$ xor b xor c
D. $co = bc + ac + ab; s = (ab)$ xor c

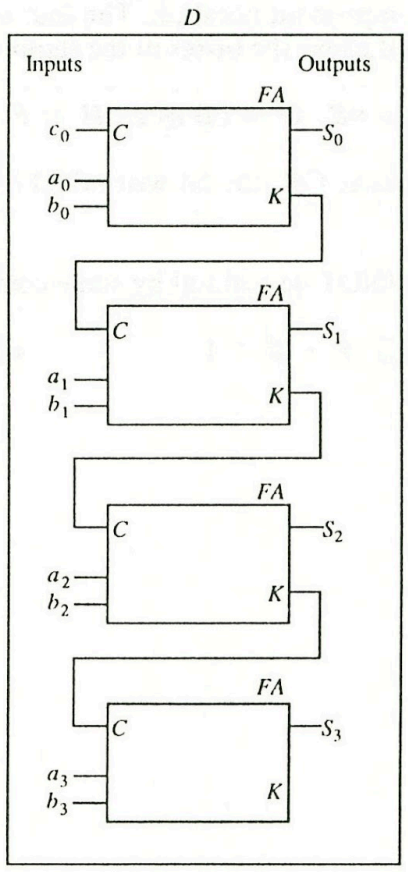
Your Answer: A **Correct Answer: A** Correct Discuss

Q #6 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

As shown in the three diagrams below, device FA makes use of Two copies of device HA, and device D makes use of four copies of device FA. Assume that all basic logic gates(AND, OR, NOT, XOR gate) have the same delay T.







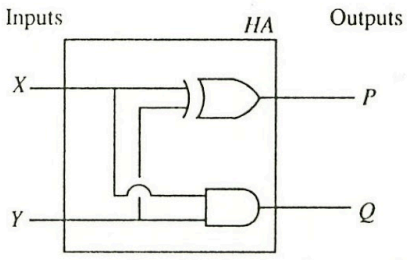
If all inputs to device D become available simultaneously, which output will be available last?

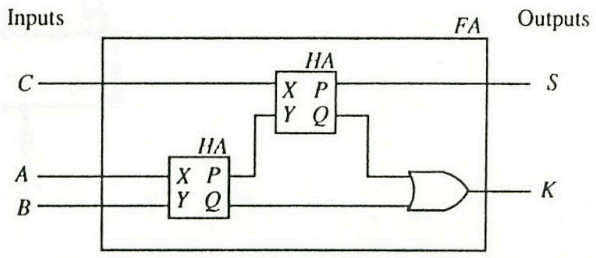
A. S_1
B. S_2
C. S_3
D. They will all be available simultaneously.

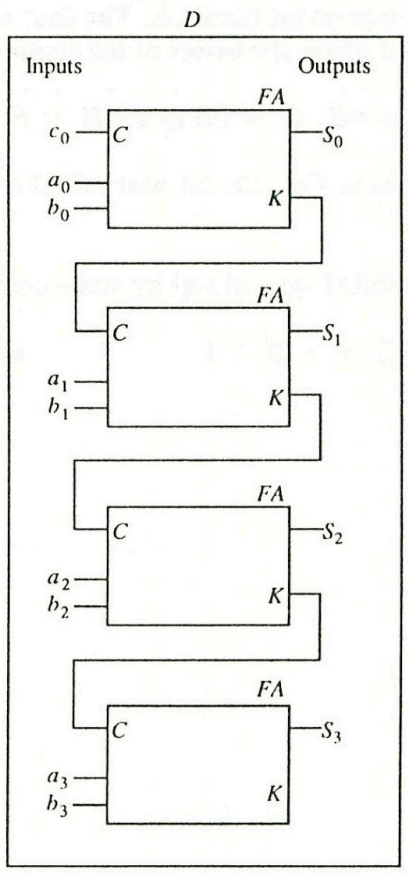
Your Answer: C **Correct Answer: C** Correct Discuss

Q #7 | Numerical Type | Award: 2 | Penalty: 0 | Digital Logic

As shown in the three diagrams below, device FA makes use of Two copies of device HA, and device D makes use of four copies of device FA. Assume that all basic logic gates(AND, OR, NOT, XOR gate) have the same delay T.



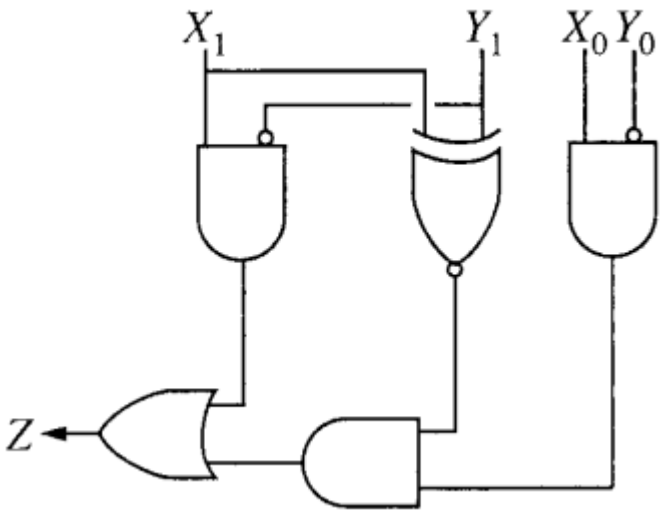




If all inputs to device D become available simultaneously, the delay before S_2 must be valid is kT, then what is k?

Your Answer: 8 | Correct Answer: 6 | Incorrect | Discuss

Q #8 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic



The logic circuit above is used to compare two unsigned 2-bit numbers,

$\mathrm{X_1X_0} = \mathrm{X}$ and $\mathrm{Y_1Y_0} = \mathrm{Y}$, where $\mathrm{X_0}$ and $\mathrm{Y_0}$ are the least significant bits. (A small circle on any line in a logic diagram indicates logical NOT.)

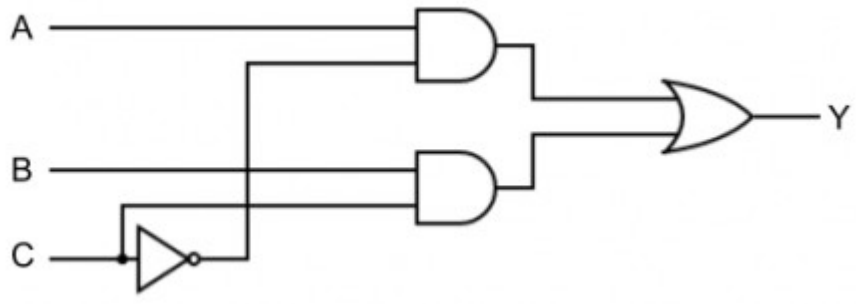
Which of the following always makes the output Z have the value 1?

A. $\mathrm{X} > \mathrm{Y}$
B. $\mathrm{X} < \mathrm{Y}$

C. $\mathrm{X} \neq \mathrm{Y}$
D. $\mathrm{X} \geq \mathrm{Y}$

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #9 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic



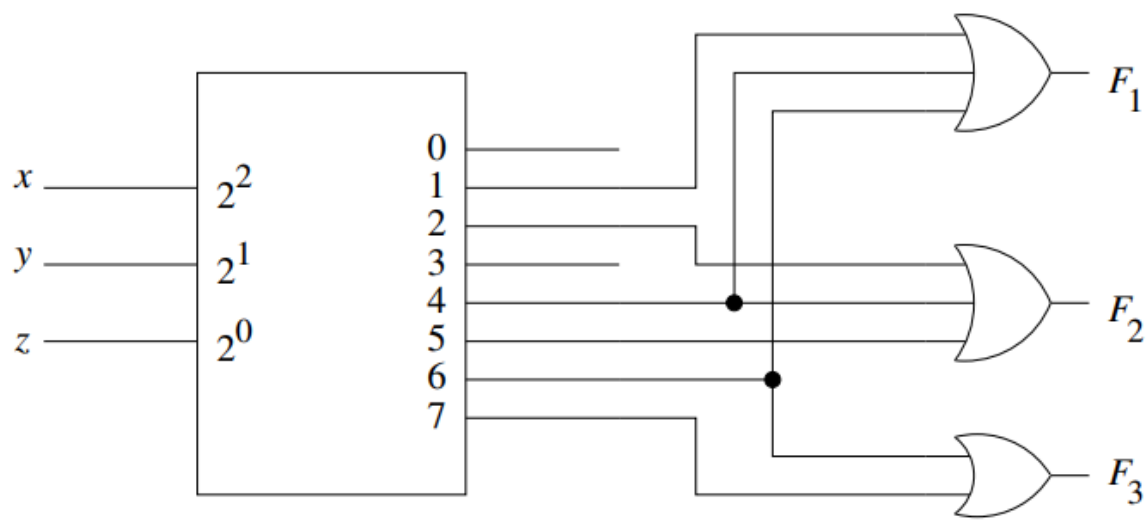
Above circuit represents

A. 2×1 MUX with A, B as input lines and C as a select line
B. 4×1 MUX with A, B as input lines and C as a select line
C. 2×1 MUX with A, C as input lines and B as a select line
D. $4 \times 1 \mathrm{MUX}$ with A, C as input lines and B as a select line

Your Answer: A | Correct Answer: A | Correct | Discuss

Q #10 | Multiple Select Type | Award: 2 | Penalty: 0 | Digital Logic

Consider the following combinational circuit using a decoder and OR gates, implementing three Boolean functions $\mathrm{F}_1, \mathrm{F}_2, \mathrm{F}_3$:



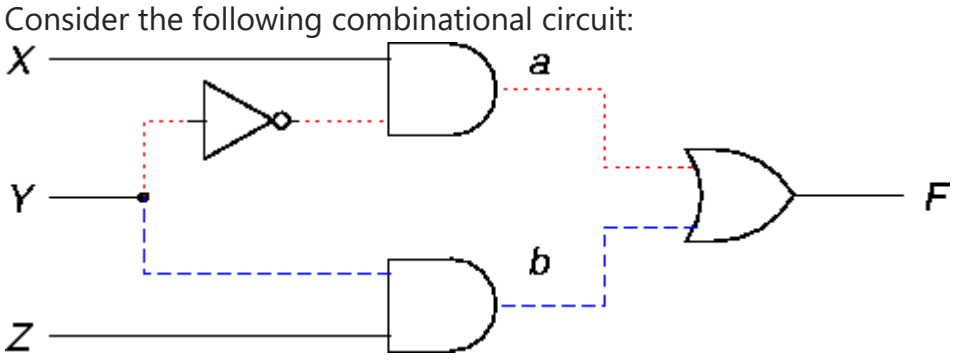
Which of the following is/are correct boolean expressions for these boolean functions?

A. $\mathrm{F}_1 = \mathrm{x}'\mathrm{y}'\mathrm{z} + \mathrm{xz}'$
B. $\mathrm{F}_2 = \mathrm{x}'\mathrm{yz}' + \mathrm{xy}$ '
C. $\mathrm{F}_3 = \mathrm{xyz}' + \mathrm{xz}$
D. $\mathrm{F}_3 = \mathrm{x}'yz + \mathrm{x}y$

Your Answer: A;B | Correct Answer: A;B | Correct | Discuss

Q #11 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

Consider the following combinational circuit:



By adding which term to this circuit, it will be free from "Static-1 Hazard"?

A. XZ
B. XZ'
C. $XY'Z + XYZ$
D. XYZ

Your Answer: | **Correct Answer: A** | Not Attempted | Discuss

Q #12 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

We design a comparator circuit that takes two 4-bit words $a_3a_2a_1a_0$ and $b_3b_2b_1b_0$ as inputs, and generates one output f which is 1 iff the two words are identical, i.e. $a_i = b_{i,\text{ for all four bits}}$ $(i = 0, 1, 2, 3)$. Then which of the following is NOT a correct expression for f?

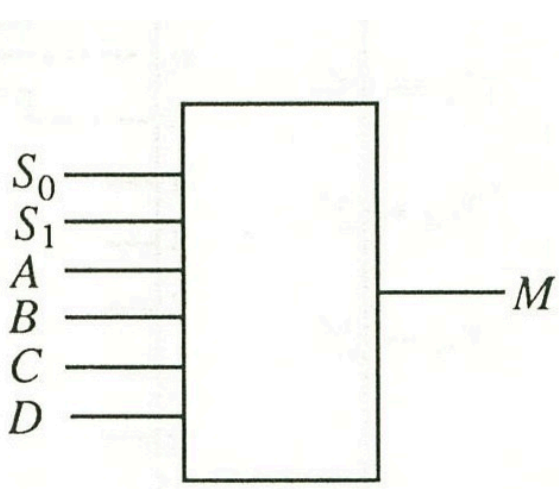
A. $\overline{(a_3 \oplus b_3) + (a_2 \oplus b_2) + (a_1 \oplus b_1) + (a_0 \oplus b_0)}$
B. $(a_3 \odot b_3)\,(a_2 \odot b_2)\,(a_1 \odot b_1)\,(a_0 \odot b_0)$
C. $(a_3 \odot b_3) + (a_2 \odot b_2) + (a_1 \odot b_1) + (a_0 \odot b_0)$
D. $(\overline{a_3} \oplus b_3)\,(\overline{a_2} \oplus b_2)\,(\overline{a_1} \oplus b_1)\,(\overline{a_0} \oplus b_0)$

Your Answer: C | **Correct Answer: C** | Correct | Discuss

Q #13 Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic

A multiplexer, shown below on the right, has 6 inputs, S_0, S_1, A, B, C, and D. The truth table on the left describes its function.

S_0S_1	
00	A
01	B
10	C
11	D

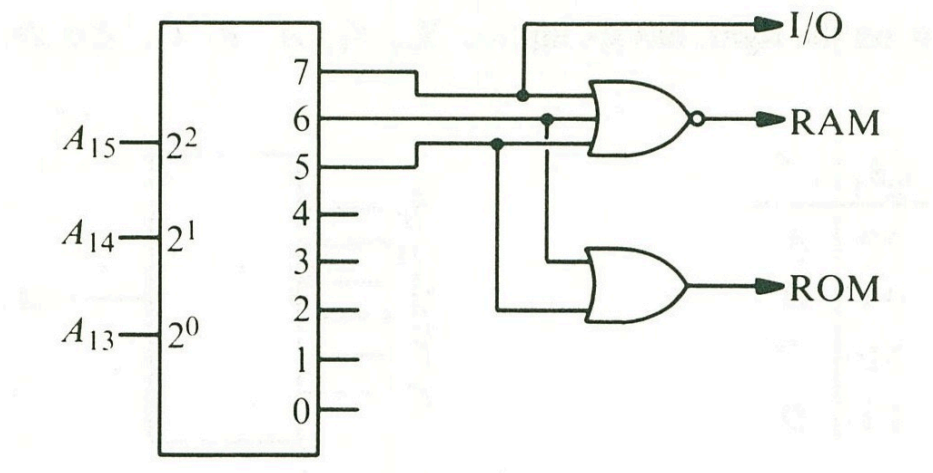


It is desired to implement the function $F = (X \oplus Y) \oplus Z$ using the multiplexer. If X is applied to S_0, and Y is applied to S_1, what inputs should be applied to A, B, C and D to realize the function F?

A. $A = B = C = D = Z$
B. $A = X \oplus Y, B = X \oplus Z, C = Y \oplus Z, D = Z$
C. $\mathrm{A = D = Z; B = C = }\overline{Z}$
D. the function F can not be realized with any of the inputs shown above.

Your Answer: C | **Correct Answer: C** | Correct | Discuss

Q #14 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic



The $64K$ address space of a certain microcomputer is accessed by address signals $A_0. A_1, \ldots, A_{14}, A_{15}$ (Where A_0 is the least significant bit and A_{15} is the most significant bit) and is divided equally among read-only memory(ROM), read-write memory(RAM), and input-output registers (I/O) by means of the decoder and gates as shown above.

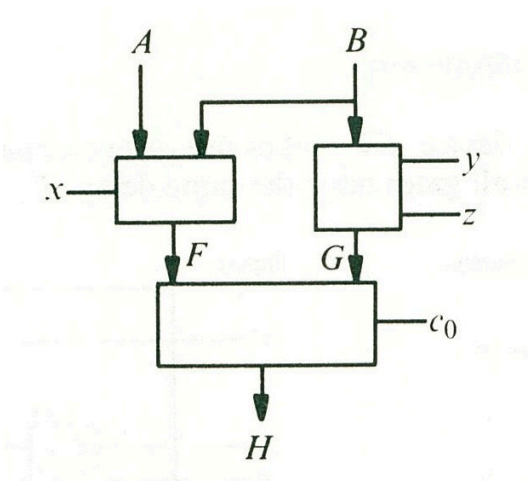
Note that only the three high order outputs of the decoder are used. Output $i(0 \leq i \leq 7)$ of the decoder is 1 if and only if the binary value of the inputs $A_{15}A_{14}A_{13}$ is i.

Which of the following correctly indicates the beginning and ending hexadecimal addresses of the three portions of the address space?

A. ROM (0000 - 3FFF), RAM (4000 - DFFF), I/O (E000 - FFFF)
B. ROM (0000 - 9FFF), RAM (A000 - DFFF), I/O (E000 - FFFF)
C. ROM (A000 - DFFF), RAM (0000 - 9FFF), I/O (E000 - FFFF)
D. ROM (4000 - 4FFF), RAM (6000 - FFFF), I/O (0000 - 3FFF)

Your Answer: C | Correct Answer: C | Correct | Discuss

Q #15 | Multiple Choice Type | Award: 2 | Penalty: 0.67 | Digital Logic



The figure above shows part of a CPU with parallel data paths A, B, F, G and H. The information on these paths is interpreted as integers in two's complement number notation. The four control signals $x, y, z,$ and (the low-order carry-in) c_0, come from a control unit and cause the boxes in the figure to implement the following functions:

$$F = \overline{x}A \vee xB; G = yB \oplus z; H = F + G + c_0$$

Where V is bitwise OR, $\oplus$ is bitwise exclusive OR, the bitwise AND is denoted by juxtaposition, and $+$ is arithmetic plus.

Which of the following values of H CANNOT be realized by some combination of the control signals and c_0?

A. A
B. $A + B + 1$
C. $A - B$
D. $A - B + 1$

Your Answer: **Correct Answer: D** Not Attempted Discuss

You're doing good, you can target above 70 percentage!