Summary in Graph

## Exam Summary (GO Classes Test Series 2024 | CO and Architecture | Test 3)

Qs. Attempted:	<b>10</b> 3 + 7	Correct Marks:	<b>15</b> 3 + 12
Correct Attempts:	<b>9</b> 3 + 6	Penalty Marks:	0
Incorrect Attempts:	1	Resultant Marks:	<b>15</b>

Total Questions:

25
5 + 20

Exam Duration:
45 Minutes

Time Taken:
45 Minutes

## **Technical**

**EXAM STATS** 

FEEDBACK

**EXAM RESPONSE** 

Q #1 Numerical Type Award: 1 Penalty: 0 CO and Architecture

If an 8-way set-associative cache is made up of 32 bit words, 4 words per line and 4096 sets, how big is the cache in Kilo bytes (1 kilo = 1024)?

Your Answer: 512 Correct Answer: 512 Correct Discuss

Q #2 Numerical Type Award: 1 Penalty: 0 CO and Architecture

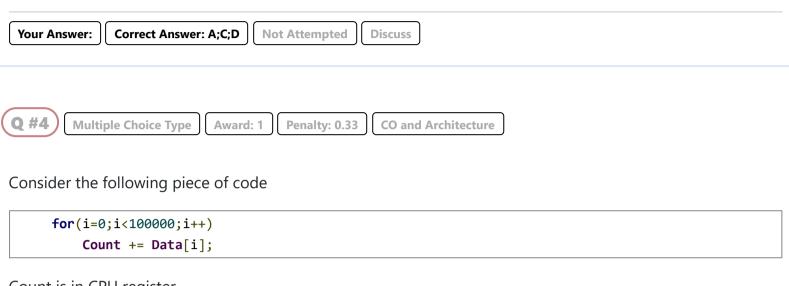
Assume that a read request takes 50 nsec on a cache miss and 5 nsec on a cache hit. While running a program, it is observed that 80 of the processor's read requests result in a cache hit. The average read access time is \_\_\_\_\_ nsec.

Your Answer: 14 Correct Answer: 14 Correct Discuss

Q #3 Multiple Select Type Award: 1 Penalty: 0 CO and Architecture

Which of the following statements about caches is (are) true?

- A. A direct-mapped cache can have a lower miss rate than an associative cache of the same size (number of blocks).
- B. Programs with high spatial locality have a low cache miss rate primarily because the exact same addresses are re-referenced.
- C. Programs with high temporal locality have a low cache miss rate primarily because the exact same addresses are re-referenced.
- D. In direct mapped cache, there is no need of page replacement algorithm.



Count is in CPU register.

What kind of locality is exhibited by access to "Data"?

- A. Temporal
- B. Spatial
- C. Both
- D. Neither



A  $64~\mathrm{KB}$ , direct mapped cache has  $16~\mathrm{byte}$  blocks. If addresses are  $32~\mathrm{bits}$ , how many bits are used the tag, index, and offset in this cache, respectively?

- A. 16, 20, 4
- B. 16, 4, 12
- C. 16, 12, 4
- D. 12, 16, 4





The designers of a cache system need to reduce the number of cache misses that occur in a certain group of programs. Which of the following statements is/are true?

- A. If compulsory misses are most common, then the designers should consider increasing the cache line size to take better advantage of locality.
- B. If capacity misses are most common, then the designers should consider increasing the total cache size so it can contain more lines.
- C. If conflict misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs.
- D. If capacity misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs.

Your Answer: Correct Answer: A;B;C Not Attempted Discuss



A simple rule of thumb is that doubling the cache size reduces the miss rate by roughly 30%. Consider the following three systems :

- System 1: In system 1, we have main memory whose access time is 60 ns and there is no cache.
- System 2 : You implement a small, direct-mapped cache of 32K bytes with an access time of 30 ns. However, the hit rate is only about 50%.
- System 3 : We doubled the cache size of System 2 to 64K bytes.

Which of the following is/are true about the (approx)expected percentage improvement in the effective memory access time?

- A. 0 improvement using system 2 over system 1.
- B. 0 improvement using system 3 over system 1.
- C. 15 improvement using system 3 over system 1.
- D. 15 improvement using system 3 over system 2.

Your Answer: Correct Answer: A;C;D Not Attempted Discuss



A computer has a 32 bit address and a 64 bit data bus with address resolution to the byte level. The computer is using a direct mapped cache with  $4~\mathrm{K}$  cache lines. The size of each cache line is 64 bytes. How many memory cycles are required to fill up a cache line?

Your Answer: Correct Answer: 8 Not Attempted Discuss



A computer has a 32-bit address bus with a direct mapped cache, using 4 bits for block offset, 16 tag bits, and 12 index bits.

Which of the following address pairs can be placed in the cache simultaneously?

- A. 3AC6 F456 and 26 A35456
- B. 3 F08C304 and 3 F08C371
- C. 5E3C7680 and 8 F3C768 A
- D. 22334455 and 2233445C

Your Answer: A;B Correct Answer: A;B;D Discuss

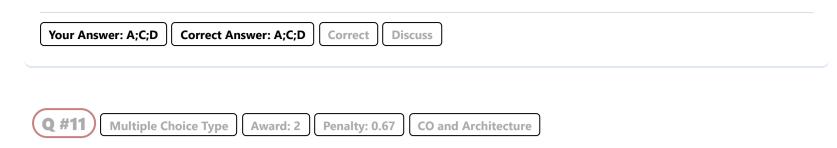


Calculate the size of the tag and the size of the cache index and total number of bits is cache given that: Cache is direct mapped; Cache size  $= 8~\mathrm{KB}$ ; Block size  $= 4~\mathrm{bytes}$ ; Memory address size  $= 32~\mathrm{bits}$ .

Which of the following is true?

- A. Tag bits =19
- B. Cache Index bits =19
- C. Cache Index bits = 11

D. A total of  $2^{19}$  main memory blocks map to each cache line.



Consider a Direct Mapped Cache with 8 Entries(lines). The contents of the TAG entries are given below.

- Entry 0 0x080101
- Entry 1 0x234234
- Entry 2 0x132342
- Entry 3 0x143456
- Entry 4 0x002233
- Entry 5 0x423553
- Entry 6 0x000235
- Entry 7 0x100002

Each block stores 32 Bytes, for a 32 bits address.

If there is a reference to address " $0 \times 10020200$ " (a byte reference), which entry in the cache will be accessed, is there a cache hit?

- A. Entry 1, Hit
- B. Entry 0, Hit
- C. Entry 1, Miss
- D. Entry 0, Miss



Assume a computer has 32 bit addresses. Each block stores 16 words. A direct-mapped cache has 256 blocks. In which line(decimal value) of the cache would we look for each of the following addresses? Addresses are given in hexadecimal for convenience.

- A. Address 1A2BC012 will be found in line 1.
- B. Address 1A2BC012 will be found in line 192.
- C. Address FFFF00FF will be found in line 15.
- D. Address FFFF00FF will be found in line 0.





Assume a program consists of 8 pages and a computer has 16 frames of memory. A page consists of 4096 words and memory is word addressable. Currently, page 0 is in frame 2, page 4 is in frame 15, page 6 is in frame 5 and page 7 is in frame 9. No other pages are in memory. Translate the following virtual memory addresses into physical memory addresses below.

- A. 111000011110000 becomes 1001000011110000
- B. 111000011110000 becomes 1011000011110000
- D. 0000000000000000 becomes 0000000000000010



Correct

Discuss

Assume you have a 2-way set associative cache.

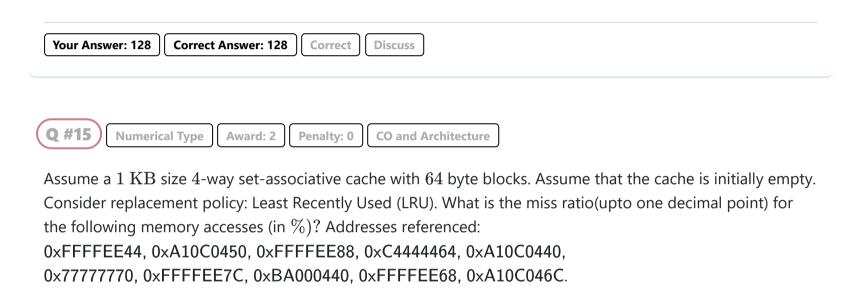
Correct Answer: A;C

• Words are 4 bytes

Your Answer: A;C

- Addresses are to the byte
- Each block holds 512 bytes
- There are 1024 blocks in the cache

If you reference a 32-bit physical address - and the cache is initially empty - how many data words are brought into the cache with this reference?





## You're doing good, you can target above 70 percentage!

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