Summary in Graph

Exam Summary (GO Classes Test Series 2024 | CO and Architecture | Test 2)

Qs. Attempted:	**14** (5 + 9)	**Correct Marks:**	**11** (3 + 8)
Correct Attempts:	**7** (3 + 4)	**Penalty Marks:**	**1.67** (0.33 + 1.33)
Incorrect Attempts:	**7** (2 + 5)	**Resultant Marks:**	**9.33** (2.66 + 6.66)

Total Questions:	**15** (5 + 10)
Total Marks:	**25** (5 + 20)
Exam Duration:	**45 Minutes**
Time Taken:	**45 Minutes**

EXAM RESPONSE | EXAM STATS | FEEDBACK

Technical

Q #1 | Numerical Type | Award: 1 | Penalty: 0 | CO and Architecture

Instruction frequencies for a load/store machine :

Instruction Type	Frequency	Cycles
Load	25%	2
Store	15%	2
Branch	20%	2
ALU	40%	1

What is the average CPI of this machine?

Your Answer: 1.6 | **Correct Answer: 1.6** | Correct | Discuss

Q #2 | Multiple Choice Type | Award: 1 | Penalty: 0.33 | CO and Architecture

Individual stages of the processor have the following latencies:

IF	ID	EX	MEM	WB
$210ps$	$90ps$	$110ps$	$240ps$	$50ps$

If the processor is pipelined, each pipeline latch adds a latency of $20ps$ to the stage that precedes it this is a so-called setup latency, where the signals need to be stable at the input of the latch for some amount of time before they can be latched correctly at the end of the cycle.

If this processor is to be implemented with a 6-stage pipeline, but the design effort and time-to-market are such that there is only enough time to split one of the five existing stages into two new stages, which stage would you chose to split so that we can improve cycle time?

A. IF stage
B. ID stage
C. Ex stage
D. Mem stage

Your Answer: D **Correct Answer: D** Correct Discuss

Q #3 Multiple Choice Type Award: 1 Penalty: 0.33 CO and Architecture

In a pipelined RISC computer where all arithmetic instructions have the same CPI (cycles per instruction), which of the following actions would improve the execution time of a typical program?

I. Increasing the clock cycle rate
II. Disallowing any forwarding in the pipeline
III. Doubling the sizes of the instruction cache and the data cache without changing the clock cycle time

A. I only
B. II only
C. III only
D. I and III

Your Answer: D **Correct Answer: D** Correct Discuss

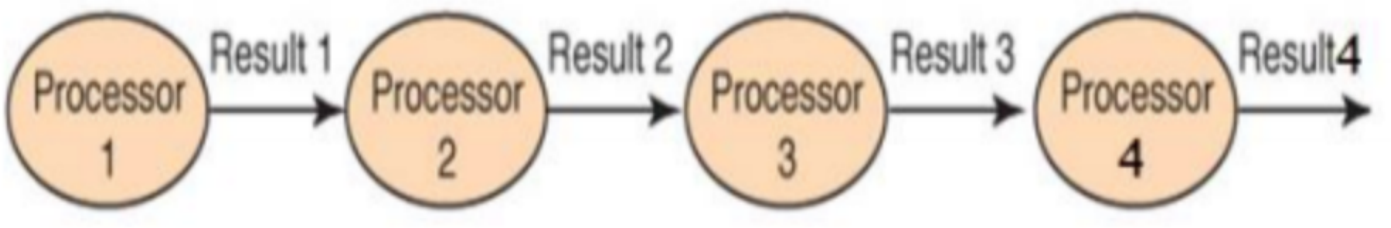
Q #4 Multiple Choice Type Award: 1 Penalty: 0.33 CO and Architecture

In typical RISC ISA, delayed branch executes which instruction irrespective of whether the branch condition is true or false?

A. Instruction immediately following the branch condition
B. Instruction immediately preceding the branch condition
C. Instruction that belongs to a different sub-routine
D. It waits till the branch condition is evaluated

Your Answer: C **Correct Answer: A** Incorrect Discuss

Q #5 Multiple Select Type Award: 1 Penalty: 0 CO and Architecture



A computer pipeline has 4 processors, as shown above. Each processor takes 15 ms to execute, and each instruction must go sequentially through all 4 processors. Which of the following is/are true?

A. 1 single instruction execution time on a Non-pipelined system is 60 ms.
B. 10 instructions execution time on Non-pipelined system is 600 ms.
C. 10 instructions execution time on a pipelined system is 195 ms.
D. 1 single instruction execution time on a pipelined system is 15 ms.

Your Answer: A;B;C;D **Correct Answer: A;B;C** Incorrect Discuss

Q #6 Multiple Select Type Award: 2 Penalty: 0 CO and Architecture

A compiler designer is trying to decide between two code sequences for a particular computer. The hardware designers have supplied the following facts :

Instruction class	CPI for this instruction class
A	1
B	2
C	3

For a particular high-level-language statement, the compiler writer is considering two code sequences that require the following instruction counts:

Code sequence	IC for Instruction class		
	A	B	C
1	2	1	2
2	4	1	1

A. Sequence 1 executes fewer instructions than sequence 2.
B. Sequence 2 executes faster than sequence 1.
C. Sequence 1 executes faster than sequence 2.
D. CPI for sequence 2 is 1.5.

Your Answer: A;C;D **Correct Answer: A;B;D** Incorrect Discuss

Q #7 Multiple Select Type Award: 2 Penalty: 0 CO and Architecture

A compiler designer is trying to decide between two code segments for a particular machine. The hardware designers have provided the following data below about the CPI for each class, and the instruction counts being considered for each code sequence.

Class	CPI for this instruction class
A	2
B	3

	Instruction Counts for Instruction Classes	
Code sequence	A	B
1	3	5
2	7	2

Which of the following is true?

A. Sequence 1 executes fewer instructions than sequence 2.
B. Sequence 2 executes faster than sequence 1.
C. Sequence 1 executes faster than sequence 2.
D. CPI for sequence 1 is 2.

Your Answer: A;B **Correct Answer: A;B** Correct Discuss

Q #8 Numerical Type Award: 2 Penalty: 0 CO and Architecture

A pipelined processor uses a stage instruction pipeline with the following stages: Instruction fetch (IF), Instruction decode (ID), Execute (EX) and Writeback (WB). The arithmetic operations as well as the load and store operations are carried out in the EX stage.
Consider the following sequence of instructions:

1. lw $\$s2, 0(\$s1)$; $\mathrm{s2} \leftarrow \mathrm{M}[0 + \mathrm{s1}]$
2. lw $\$s1, 40(\$s6)$; $s1 \leftarrow M[40 + s6]$
3. sub $\$s6, \$s1, \$s2$; $s6 \leftarrow s1 + s2$
4. add $\$s6, \$s2, \$s2$; $s6 \leftarrow s2 + s2$
5. or $\$s3, \$s6, \$\mathrm{zero}$; $s3 \leftarrow s6\ v\ 0$
6. sw $\$\ \mathrm{s6}, 50(\$\mathrm{s1})$; $\mathrm{M}[50 + \mathrm{s1}] \leftarrow \mathrm{s6}$

The number of Read-After-Write (RAW) dependencies in the sequence of instructions are _____

Your Answer: 7 **Correct Answer: 6** Incorrect Discuss

Q #9 Numerical Type Award: 2 Penalty: 0 CO and Architecture

Assume the 5-stage MIPS pipeline(IF, ID, EX, MEM, and WB) with no forwarding, and each stage takes 1 cycle. Instead of inserting nops, you let the processor stall on hazards.
The functionality of the five stages of this pipeline is as follows :

1. Instruction fetch (IF) – get instruction from memory, increment PC
2. Instruction Decode (ID) – translate opcode into control signals and read registers
3. Execute (EX) – perform ALU operation, compute jump/branch targets
4. Memory (MEM) – access memory if needed
5. Writeback (WB) – update register file (write back to register file)

The pipeline does not have other bypassing/forwarding hardware.
All Instructions, including loads and stores, spend only one cycle in each stage. The register file can be written and then read in the same cycle.
Consider the following sequence of instructions executed on this pipeline:

1. lw $\$s2, 0(\$s1)$; $\mathrm{s2} \leftarrow \mathrm{M}[0 + \mathrm{s1}]$
2. lw $\$s1, 40(\$s6)$; $s1 \leftarrow M[40 + s6]$
3. sub $\$s6, \$s1, \$s2$; $s6 \leftarrow s1 + s2$
4. add $\$s6, \$s2, \$s2$; $s6 \leftarrow s2 + s2$
5. or $\$s3, \$s6, \$\mathrm{zero}$; $s3 \leftarrow s6\ v\ 0$
6. sw $\$\ \mathrm{s6}, 50(\$\mathrm{s1})$; $\mathrm{M}[50 + \mathrm{s1}] \leftarrow \mathrm{s6}$

What is the execution time (in cycles) for the whole program?

Your Answer: **Correct Answer: 14** Not Attempted Discuss

Q #10 Numerical Type | Award: 2 | Penalty: 0 | CO and Architecture

Consider a processor with an in-order five-stage pipeline (IF, ID, EX, MEM, and WB) with clock cycle time 10 ns. This processor is executing a program in which 30% of the instructions are conditional branch instructions, 10% of the instructions are unconditional branch instructions. 40% of the conditional branches are taken. Branch target is available at the end of 2nd stage for unconditional branches and at the end of 3rd stage for conditional branches. Assume that the instruction following the branch is always started and ignored if the branch is taken. What is the throughput (In million instructions per second) of the system?

Your Answer: 74.63 | **Correct Answer: 74.60:74.65** | Correct | Discuss

Q #11 Multiple Choice Type | Award: 2 | Penalty: 0.67 | CO and Architecture

The 5 stages of two processors a,b have the following latencies:

Type	IF	ID	EX	MM	WB
a	300	400	350	550	100
b	200	150	100	190	140

Assume that when pipelining, each pipeline stage costs $20ps$ extra for the registers between pipeline stages. Which of the following pairs of tuples represents the cycle time, the latency of one instruction, and the throughput for a pipelined processor for both the types a and b mentioned above?

A. $(570, 570, 1/570)(220, 220, 1/220)$
B. $(570, 1700, 1/1700), (220, 220, 1/780)$
C. $(570, 570, 1/1700), (220, 780, 1/780)$
D. $(570, 2850, 1/570), (220, 1100, 1/220)$

Your Answer: A | **Correct Answer: D** | Incorrect | Discuss

Q #12 Numerical Type | Award: 2 | Penalty: 0 | CO and Architecture

The ideal CPI that we can expect in a pipelined implementation is only 1. If we want to further reduce CPI, we need to explore the option of issuing and completing multiple instructions every clock cycle. For example, if we issue and complete two instructions every clock cycle, ideally we should get a CPI of 0.5. Such processors are called multiple issue processors. So, *in multiple issue processors, we Fetch (and execute) more than one instructions at one time (expand every pipeline stage to accommodate multiple instructions).*

A single issue processor is basically “one instruction each clock cycle” processor.

A computer can parallelize the program execution by using multiple issue processor.

Assume that a program execution takes 100 nsec when executed on a single issue processor and it takes 40 nsec when it is executed on a 4-issue processor(i.e. Four instructions each clock cycle). Assuming that some part of the execution is non-parallelizable(i.e. will not benefit from multiple issue processing) then what percentage of execution is non parallelizable ? (Rounded off to nearest integer)

Your Answer: 80 | **Correct Answer: 20** | Incorrect | Discuss

Q #13 Numerical Type | Award: 2 | Penalty: 0 | CO and Architecture

Consider the following instruction sequence in a single-issue in-order 5-stage pipeline (IF, ID, EX, MEM, and WB).

Opcode	Destination	Source1	Source2	
ADD	R1	R2	R3	(First instruction to enter the pipeline)
SUB	R2	R3	R1	
MUL	R1	R2	R3	(Last instruction to enter the pipeline)

How many data hazards does the ID stage need to detect for this instruction sequence?

Your Answer: 2 **Correct Answer: 2** Correct Discuss

Q #14 Numerical Type Award: 2 Penalty: 0 CO and Architecture

Consider an unpipelined processor. Assume that it has 1-ns clock cycle and that it uses 4 cycles for ALU operations and 5 cycles for branches and 4 cycles for memory operations. Assume that the relative frequencies of these operations are $50\%, 35\%$ and 15% respectively. Suppose that due to clock skew and set up, pipelining the processor adds 0.15 ns of overhead to the clock. Ignoring any latency impact, how much speed up in the instruction execution rate will we gain from a pipeline?

Your Answer: 3.78 **Correct Answer: 3.78** Correct Discuss

Q #15 Multiple Choice Type Award: 2 Penalty: 0.67 CO and Architecture

Two processors, M-5 and M-7, implement the same instruction set. Processor M-5 uses a 5-stage pipeline and a clock cycle of 10 nanoseconds. Processor M-7 uses a 7-stage pipeline and a clock cycle of 7.5 nanoseconds. Which of the following is (are) true?

I. M-7's pipeline has better maximum throughput than M-5's pipeline.
II. The latency of a single instruction is shorter on M-7's pipeline than on M-5's pipeline.
III. Programs executing on M-7 will always run faster than programs executing on M-5.

A. I only
B. II only
C. I and III only
D. II and III only

Your Answer: D **Correct Answer: A** Incorrect Discuss

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