Summary in Graph

Exam Summary (GO Classes Test Series 2024 | CO and Architecture | Test 3)

Qs. Attempted:	**10** (3 + 7)	**Correct Marks:**	**15** (3 + 12)
Correct Attempts:	**9** (3 + 6)	**Penalty Marks:**	**0** (0 + 0)
Incorrect Attempts:	**1** (0 + 1)	**Resultant Marks:**	**15** (3 + 12)

Total Questions:	**15** (5 + 10)
Total Marks:	**25** (5 + 20)
Exam Duration:	**45 Minutes**
Time Taken:	**45 Minutes**

EXAM RESPONSE | EXAM STATS | FEEDBACK

Technical

Q #1 | Numerical Type | Award: 1 | Penalty: 0 | CO and Architecture

If an 8-way set-associative cache is made up of 32 bit words, 4 words per line and 4096 sets, how big is the cache in Kilo bytes $(1\ \text{kilo} = 1024)$?

Your Answer: 512 | Correct Answer: 512 | Correct | Discuss

Q #2 | Numerical Type | Award: 1 | Penalty: 0 | CO and Architecture

Assume that a read request takes 50 nsec on a cache miss and 5 nsec on a cache hit. While running a program, it is observed that 80 of the processor's read requests result in a cache hit. The average read access time is _____ nsec.

Your Answer: 14 | Correct Answer: 14 | Correct | Discuss

Q #3 | Multiple Select Type | Award: 1 | Penalty: 0 | CO and Architecture

Which of the following statements about caches is (are) true?

A. A direct-mapped cache can have a lower miss rate than an associative cache of the same size (number of blocks).
B. Programs with high spatial locality have a low cache miss rate primarily because the exact same addresses are re-referenced.
C. Programs with high temporal locality have a low cache miss rate primarily because the exact same addresses are re-referenced.
D. In direct mapped cache, there is no need of page replacement algorithm.

Your Answer: | **Correct Answer: A;C;D** | Not Attempted | Discuss

Q #4 Multiple Choice Type | Award: 1 | Penalty: 0.33 | CO and Architecture

Consider the following piece of code

```
for(i=0;i<100000;i++)
    Count += Data[i];
```

Count is in CPU register.

What kind of locality is exhibited by access to "Data"?

A. Temporal
B. Spatial
C. Both
D. Neither

Your Answer: | **Correct Answer: B** | Not Attempted | Discuss

Q #5 Multiple Choice Type | Award: 1 | Penalty: 0.33 | CO and Architecture

A 64 KB, direct mapped cache has 16 byte blocks. If addresses are 32 bits, how many bits are used the tag, index, and offset in this cache, respectively?

A. $16, 20, 4$
B. $16, 4, 12$
C. $16, 12, 4$
D. $12, 16, 4$

Your Answer: C | **Correct Answer: C** | Correct | Discuss

Q #6 Multiple Select Type | Award: 2 | Penalty: 0 | CO and Architecture

The designers of a cache system need to reduce the number of cache misses that occur in a certain group of programs. Which of the following statements is/are true?

A. If compulsory misses are most common, then the designers should consider increasing the cache line size to take better advantage of locality.
B. If capacity misses are most common, then the designers should consider increasing the total cache size so it can contain more lines.
C. If conflict misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs.
D. If capacity misses are most common, then the designers should consider increasing the cache's associativity, in order to provide more flexibility when a collision occurs.

Your Answer: | Correct Answer: A;B;C | Not Attempted | Discuss

Q #7 | Multiple Select Type | Award: 2 | Penalty: 0 | CO and Architecture

A simple rule of thumb is that doubling the cache size reduces the miss rate by roughly 30%.
Consider the following three systems :

- System 1 : In system 1, we have main memory whose access time is 60 ns and there is no cache.
- System 2 : You implement a small, direct-mapped cache of 32K bytes with an access time of 30 ns. However, the hit rate is only about 50%.
- System 3 : We doubled the cache size of System 2 to 64K bytes.

Which of the following is/are true about the (approx)expected percentage improvement in the effective memory access time?

A. 0 improvement using system 2 over system 1.
B. 0 improvement using system 3 over system 1.
C. 15 improvement using system 3 over system 1.
D. 15 improvement using system 3 over system 2.

Your Answer: | Correct Answer: A;C;D | Not Attempted | Discuss

Q #8 | Numerical Type | Award: 2 | Penalty: 0 | CO and Architecture

A computer has a 32 bit address and a 64 bit data bus with address resolution to the byte level. The computer is using a direct mapped cache with 4 K cache lines. The size of each cache line is 64 bytes. How many memory cycles are required to fill up a cache line?

Your Answer: | Correct Answer: 8 | Not Attempted | Discuss

Q #9 | Multiple Select Type | Award: 2 | Penalty: 0 | CO and Architecture

A computer has a 32-bit address bus with a direct mapped cache, using 4 bits for block offset, 16 tag bits, and 12 index bits.
Which of the following address pairs can be placed in the cache simultaneously?

A. 3AC6 F456 and $26\ \text{A35456}$
B. $3\ \text{F08C304}$ and $3\ \text{F08C371}$
C. 5E3C7680 and $8\ \text{F3C768 A}$
D. 22334455 and 2233445C

Your Answer: A;B | Correct Answer: A;B;D | Incorrect | Discuss

Q #10 | Multiple Select Type | Award: 2 | Penalty: 0 | CO and Architecture

Calculate the size of the tag and the size of the cache index and total number of bits is cache given that: Cache is direct mapped; Cache size $= 8\ \text{KB}$; Block size $= 4$ bytes ; Memory address size $= 32$ bits.

Which of the following is true?

A. Tag bits $= 19$
B. Cache Index bits $= 19$
C. Cache Index bits $= 11$

D. A total of 2^{19} main memory blocks map to each cache line.

Your Answer: A;C;D **Correct Answer: A;C;D** Correct Discuss

Q #11 Multiple Choice Type Award: 2 Penalty: 0.67 CO and Architecture

Consider a Direct Mapped Cache with 8 Entries(lines). The contents of the TAG entries are given below.

- Entry 0 0x080101
- Entry 1 0x234234
- Entry 2 0x132342
- Entry 3 0x143456
- Entry 4 0x002233
- Entry 5 0x423553
- Entry 6 0x000235
- Entry 7 0x100002

Each block stores 32 Bytes, for a 32 bits address.

If there is a reference to address "0x10020200" (a byte reference), which entry in the cache will be accessed, is there a cache hit?

A. Entry 1, Hit
B. Entry 0, Hit
C. Entry 1, Miss
D. Entry 0, Miss

Your Answer: D **Correct Answer: D** Correct Discuss

Q #12 Multiple Select Type Award: 2 Penalty: 0 CO and Architecture

Assume a computer has 32 bit addresses. Each block stores 16 words. A direct-mapped cache has 256 blocks. In which line(decimal value) of the cache would we look for each of the following addresses? Addresses are given in hexadecimal for convenience.

A. Address 1A2BC012 will be found in line 1.
B. Address 1A2BC012 will be found in line 192.
C. Address FFFF00FF will be found in line 15.
D. Address FFFF00FF will be found in line 0.

Your Answer: A;C **Correct Answer: A;C** Correct Discuss

Q #13 Multiple Select Type Award: 2 Penalty: 0 CO and Architecture

Assume a program consists of 8 pages and a computer has 16 frames of memory. A page consists of 4096 words and memory is word addressable. Currently, page 0 is in frame 2, page 4 is in frame 15, page 6 is in frame 5 and page 7 is in frame 9. No other pages are in memory. Translate the following virtual memory addresses into physical memory addresses below.

A. 111000011110000 becomes 1001000011110000
B. 111000011110000 becomes 1011000011110000
C. 000000000000000 becomes 0010000000000000
D. 000000000000000 becomes 0000000000000010

Your Answer: A;C **Correct Answer: A;C** Correct Discuss

Q #14 Numerical Type Award: 2 Penalty: 0 CO and Architecture

Assume you have a 2-way set associative cache.

- Words are 4 bytes
- Addresses are to the byte
- Each block holds 512 bytes
- There are 1024 blocks in the cache

If you reference a 32-bit physical address - and the cache is initially empty - how many data words are brought into the cache with this reference?

Your Answer: 128 **Correct Answer: 128** Correct Discuss

Q #15 Numerical Type Award: 2 Penalty: 0 CO and Architecture

Assume a 1 KB size 4-way set-associative cache with 64 byte blocks. Assume that the cache is initially empty. Consider replacement policy: Least Recently Used (LRU). What is the miss ratio(upto one decimal point) for the following memory accesses (in $\%$)? Addresses referenced:
0xFFFFEE44, 0xA10C0450, 0xFFFFEE88, 0xC4444464, 0xA10C0440,
0x77777770, 0xFFFFEE7C, 0xBA000440, 0xFFFFEE68, 0xA10C046C.

Your Answer: 60 **Correct Answer: 60** Correct Discuss

You're doing good, you can target above 70 percentage!