Power Supply

Lesson 1

1. Always search for development kit, evaluation board, starter kit, any existing board which will have schematic available. They may have BoM or other useful information.
2. All pins need to be place with 100mils grid.
3. Use 10 mils when drawing symbols.
4. Use 50V rated capacitor (no difference in price).
5. Capacitor for switching power supply output is important; always consider ESR.
6. Choosing the proper inductor for power supply is very tricky and important. Value of inductor depends on output voltage and current.

Lesson 2

1. Schematic should be done in 100mils grid.
2. X and Y mirror parts.
3. Make sure to use Wire (CTRL+W) when making connection and not line when laying out schematic.
4. DNP in schematics means “Do Not Place”.
5. Optional Resistors: Resistors placed just in case user wants to utilize other chip function.
6. When you create a power symbol, NEVER WRITE IT AGAIN, ALWAYS COPY PASTE IT. Same with NET names.
7. Power Lines always have a filtering cap.
8. Always optimize BoM: check pricing for similar value components and if higher rating is cheaper, use it for all instead.
9. O Ohm resistors are to create variant of the board (see note 4).
10. NF: “Not Fitted”: components you don’t want to fit by default.
11. How are enable lines receive logic high or low? Look at evaluation board (if there is). Use pull up or pull down resistors.
12. Use Directives NO ERC on unused pins (to prevent issues during error checking). Place-Directives-Generic No ERC.
13. Datasheet, Datasheet, Datasheet.
14. Annotation: Replacing “?” with numbering.

Tools-Annotation-Annotate Schematic-Update Changes List-Accept-Validate Changes-Execute Changes

1. Always name important traces in schematic for the PCB layout.
2. Always validate/compile Schematic once it’s done.
3. Every change in the library should be updated in schematic by right clicking edited component and updating schematic.

Lesson 3

1. Always add markings on polarized components (ie diodes, caps, etc).
2. Always validate/compile project before schematic capture.

Lesson 4

1. Make sure Cross Select Mode is Active under tools tab.
2. “L” is to place components on the underside.
3. Disable virtual connection while laying out: View-Connections-Hide All.
4. “J” to manually input x and y location of component while on hold.
5. Create layer set in View Configuration tab: Top, Bottom and Top & Bottom.
6. Check PCB manufacturer and Set Rules: [PCB WAY](https://www.pcbway.com/?ngaw=32&campaignid=169427011&adgroupid=8586088891&feeditemid=&targetid=kwd-296088856449&loc_physical_ms=9032007&matchtype=b&network=g&device=c&devicemodel=&creative=345537941013&keyword=print%20pcb%20online&placement=&target=&adposition=&gclid=CjwKCAiAwKyNBhBfEiwA_mrUMloV8Zy0ejKlaAqpXxw1ZaFRcxr6U05c17Uvop7VHBtnpFyUxOKuoRoCPO0QAvD_BwE)
7. Design-Layer Stack Manager to add more layers.
8. Signal Layers you draw the tracks; Plane layers you draw spaces between the objects. Everything drawn on plane layer is removing the copper (opposite of tracks). Plane layer=negative layer. So Signal layer is empty and every drawn track is adding copper; Plane layer is copper and every drawn track is removing the copper.
9. Planes are used for Gnd and Power nets. Double click plane to assign net to a plane.
10. Always name layer L1, L2, L3….
11. Shift+S to isolate selected/active layer.
12. Assign colors to help during layout.
13. To highlight, hold ctrl and select a pad; [ and ] change intensity of the highlight.
14. Main goal is to connect pins as quickly as possible. Improvements will be done later.
15. Tented via mean the color of the pcb will be over the vias as well.
16. TOP and BOTTOM layer set is the best view while doing layout.
17. Shift+R to change mode.
18. Place via on exposed pad to take heat away from the chip.

Lesson 5

1. To improve pcb, read datasheet’s PC Board Layout Guidelines.
2. To easily change track width in a layer, select a segment and press tab and change the width. To change all tracks and all layers, press tab twice.
3. For parts of the tracks that need to be enlarged that are in crowded area (mostly near the leads), make it as short as possible.
4. For high current connection, consider adding polygons.
5. Priority is quality of connection>making it look nice.
6. Why use thermal relief on Gnd Pads? so that when soldering, gnd planes don’t cool down the soldering iron.

Lesson 6

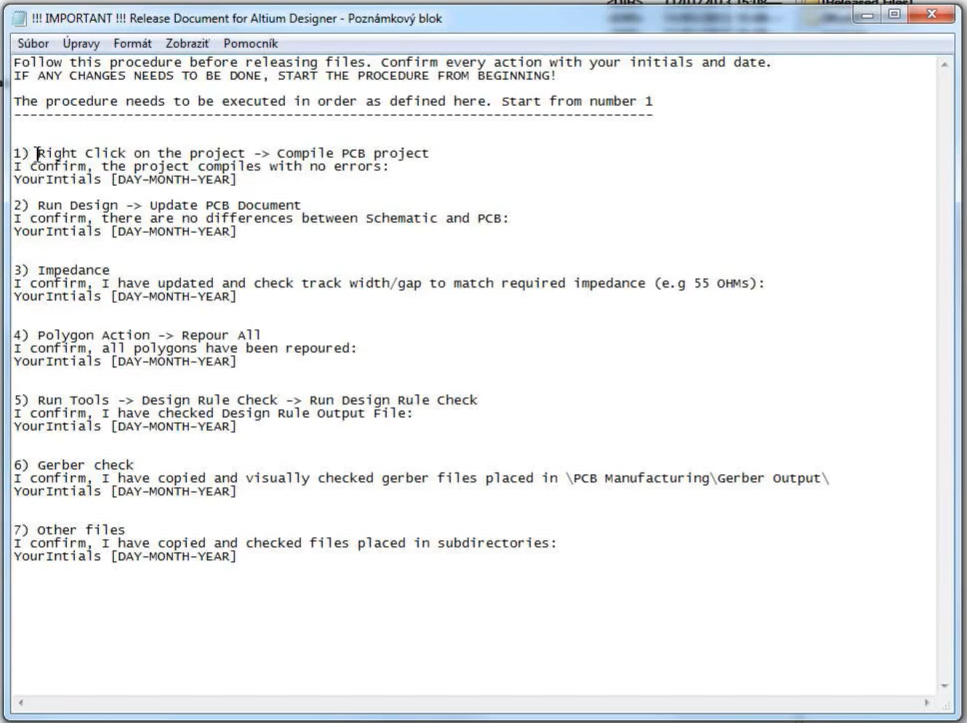
1. Enable reference designator for small projects; might look like a clutter on larger projects.
2. Don’t place reference designator too close to other top overlay components.
3. Right click-PCB editor-DRC violation Display.
4. Use descriptive designators as necessary (gnd, power).
5. On Chips, itll be nice to mark where pin 1 is.
6. Steps to generate files for manufacturing:
   1. Projects-right click project name-Output Job file
   2. Right click and save in project directory.
   3. In-house: Create Assembly Output
      1. Left add new assembly-assembly drawings-pcb document
      2. Hover curser assembly drawing-configure-set the scale mode scaled print-set scale to 1-color set to mono
      3. Hover cursor to assembly drawings again-configure-select want you want to print.
   4. Manufacturer: Create Fabrication Output
      1. Left click add new fabrication output-Gerber File-PCB document
      2. Right click gerber file-configure-general-mm-4x4-layers
      3. Layers tab-top overlay-top paste-top solder-all layers-bottom solder, paste, overlay-board outline
      4. Left click add new fabrication output-NC Drill File-PCB document
      5. Configure-general tab-mm-4:4
      6. Output container for both Gerber and NC drill files then generate content
      7. Don’t use the generated files in the free generated output files\*
      8. Only use files in original output directory\*
      9. Generate contents again
   5. Files in project output (not free document) Gerber files and NC drills are the files to be sent to manufacturer.

Advance Hardware Design

Support.spectrumdigital.com

Lesson1 Starting Project

1. Beginning: Specification provided by client (or by you) of the scope of project, which will change multiple times along the way.
2. Do market research to see what other similar products that have been done; don’t reinvent the wheel. Learn from the market and do better (not worse).
3. Always look for development boards, evaluation kit and/or reference design/schematic. Make sure it is close to the board you want to achieve.
   1. Ask manufacturer for .DSN files if they only show pdf files.
4. Along with hardware aspect, look at software aspect as well.
5. Select product/component with better support
6. Have an easily to follow directory folder. Have a folder for released files.
7. Save schematics as PDF.
8. Record the changes you need to do on your design files.
9. Have a checklist before releasing a document.



1. Have a backup directory; use cloud.
2. Signal Integrity  
   Crosstalk: 2 signals parallel may affect each other. (ie clock signal next to interrupt lines. There are online crosstalk calculators. Multiple layer>2 layer PCB for high speed to reduce substrate height which reduces coupled voltage. Crosstalk accumulates through the parallel line but once it achieves maximum, it stays constant.

[www.eeweb.com/toolbox/microstrip-crosstalk/](http://www.eeweb.com/toolbox/microstrip-crosstalk/)

www.skottanselektronik.com

1. If the driver and the load are adapted to the trace impedance, the crosstalk can be further reduced. In other words, it is good practice to match impedance between driver and load.

Lesson2 Drawing Schematic

1. Use page number on schdoc file names [01], [02]
2. Use short and clear names, capitalized
3. Use versions
4. Create hierarchy: Place- Sheet Symbol
5. Use Cover Page. Ise the company’s format; look at other previous deliverables.
6. DRAFT: Very Early stage of schematic, ignore details.  
   PRELIMINARY: Close to final schematic.  
   CHECKED: There hould not be any mistakes.

RELEASED: A board with this schematic has been sent to the manufacturer.

1. Create Block Diagrams.
2. Add titles on pages.
3. Label components
4. Include a revision history page at the end.
5. Use wide tracks for power rails; add “+” sign and the level voltage so it is easy to see since it will be on top of the net names list.
6. Net Class=group of nets. Use classes for different type of nets: SPI, Ethernet, Cameras, Audios, etc.
7. Use page reference on signals: Reports-port cross reference-add to projects to add page numbers.
8. Always put test points on the bottom of the board (Bed of Nails set up); power rails and control signals.
9. Use optional resistors. For example, for the power supply design, add the different config using the resistor dividers and just leave it unfilled. Gives you option to tweak the design without adding wires which look unprofessional.
10. Never use junctions on schematics!
11. Put everything into schematic; just omit if needed.
12. Name nets to help you identify important net during layout.
13. Add mechanical components into schematic: Fiducials, mounting holes, dip sockets, PCB itself (for BoM generation), even firmware file names in some cases.

Lesson 3 Components and Libraries

1. Go to a distributor/supplier instead of the manufacturer: Digikey, Arrow, Mouser
   1. Datasheet, min order, specs, compare table
2. Don’t copy paste components; make each unique one in the library; it will help with the BoM.
3. It’s a good test have your PCB for ESD testing. Use handheld EMI-EMC instrumentation to test PCB before sending for official ESD test (since it is very expensive).
   1. http://www.elmac.co.uk/ESD\_considerations.pdf
4. Should you create or find your component? It is faster to create one.
5. Use exact part number on names of important components.
6. Import libraries (footprint and schematic) from reference docs to save time.
7. Place the component in schematic near where they should be.
8. Place it in group: one side output, one side input, analog, digital, busses, etc.
9. Should you do common gnd for analog and digital? Depends on the PCB design. Do some research!

Lesson 4 Footprints

1. Footprint origins are used by pick and place for SMD components so always put it on the middle.
2. Use footprint wizard and choose the right or closest pattern.
3. Read datasheet to check dimension.
4. Always check pin numbering in datasheet.
5. Most 3D models are available. Use it to check for clearance for chassis design. Models also help check footprint dimension.
6. Outlines are better when estimated higher to make sure clearances are good.
7. Always create Assembly Drawing by creating another mechanical layer.

Lesson 5 BoM

1. Always specify the exact part number and component parameters during footprint and symbol library generation to help BoM creation at the end.
2. Double check BoM before ordering components especially in BoM.
3. Fill information right once and reuse it for future use and save time.
4. Environmental chamber testing: find weak points on your board. Make sure board is working functionally for few days. Check if board turns off and on properly.
   1. Few memory and oscillator components fail at some certain temps.
5. Use Variant Manager to manage different pcb configuration. Use new value or NF functions on Altium
6. Some parts you need in schematic but not in BoM (ie Mounting Holes) and vice versa (BoM), right click component and change the component type as necessary.
7. ODT: One-die termination – termination resistors for impedance matching are placed on the chip itself on the data lines and other signals (instead of pcb).

Lesson 6 Checking

1. Before starting checking schematic/board, make sure it is complete and there are no more changes.
2. Order the components to check fitting in board and footprints.
3. Check lead time of components.
4. Check each component: PN, source, lead time. Add a property and use your initialize if components is already checked. Create custom BoM to see checked components.
5. Make sure each component only has 1 footprint.
6. Check Pin #, Pin names are correct and if all pins are considered (both in footprint and component schematic symbol.
7. Make sure anode and cathode pins are labeled.
8. Compare component symbol and its footprint (Ctrl+M to measure) with datasheet.
9. \*Serial ports are use to debug booting.
10. If time permits, create 1:1 printed board and check fittings.
11. Common mistakes: TX to TX, RX to RX; + connected to – and vice versa; swapping net names.
12. Check reference document for functionality.
13. Copy-Paste net names (don’t re-type to avoid typos.
14. Check timing sequence.
15. Always compile schematic before starting PCB layout (make sure there is not any error/warning). Again, make sure schematic is done first and symbols are correct (see note 6).
16. Brose schematic: Use navigator tab to check pin to pin connection of all nets.
17. Try to imagine how current will flow through you board starting from the power lines.

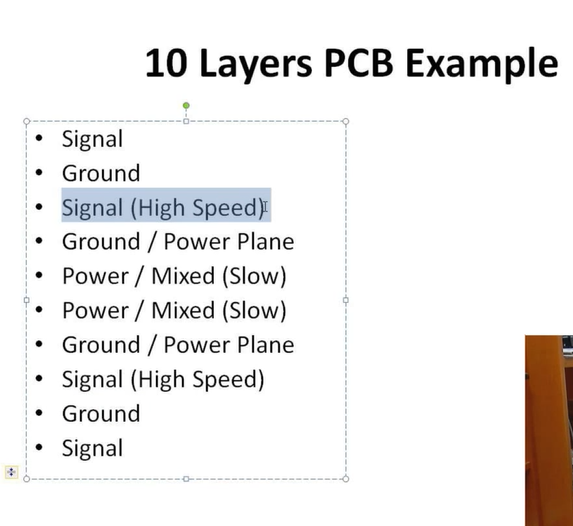
Lesson 7

1. Always set up your rules first before starting layout.
2. Don’t Draw silkscreen on pads.
3. Set up layer set first. Look at other example files for templates.
4. What are you placing first? Mechanical parts
   1. Mounting holes
   2. Connectors
      1. Think about how the mating connectors’ clearances.
5. Next? Processor, then memory. Then big chips.
   1. Memories are mirrored so place them on top of each other.
6. Leave space for length matching. Think ahead.
7. Avoid using through hole vias as much as possible. They take a lot of space.
8. Place power components (regulators etc) where they can be routed to the power layer easily.
9. Place LEDs where easily visible. (not hiding from other bigger components).
10. Think about the heat distribution.
11. Don’t start layout until you are sure about your placement.
12. Always put ESD protection near the connectors.
13. It is easier to remove a via in the later design than moving/adding a via at towards the end.
    1. Always add a via for all vias.
14. Set up default settings before starting layout.
    1. Track:
       1. Holes size 0,2mm
       2. Diameter 0.45mm
       3. Always mask all vias
    2. Clearance: 0.1mm (at the beginning but it really depends on
    3. Width: 0.1mm
    4. Through hole
       1. Size
          1. Min 0.1
          2. Max 0.25mm
          3. Preferred 0.2mm
       2. Diameter
          1. Min 0.2mm
          2. Max 0.5mm
          3. Preferred 0.45m
15. Set up stack up.
    1. Try to start with 4 layers but if needed more, start with more.
16. Do all the fanouts first.
17. Read the design guide.

Lesson 8

1. Decoupling capacitors and crystals should be close to its pin.
2. Then reference resistors, pull ups and pull downs.
3. Start in the middle of BGA chip.
4. Then busses. But make sure vias are placed already.
5. Do layout by group: bus, topology, power lines, memory group.
6. Just draw track in the beginning somehow. How it looks in the beginning doesn’t matter.
7. Set up rule for differential pairs before routing them. Also add differential directive to the differential signal in the schematic.
8. When cleaning up, work systematically to fix the errors. Work on the most complicated error first.
9. Match impedance. TX, RX impedance should be matched. Read the design guide.
   1. Use given calculators online.
   2. Manufacturers also suggest numbers for track width and PCB stackups.

Lesson9

1. 
2. Set up classes/group; create rules for these classes/groups
3. Typical tolerance for diff pairs is 20mils.
4. Occupy length at first for length matched tracks. Eyeball it at first. It will be cleaned later.
5. To put page numbers for hierarchical structure; reports, cross reference.
6. Shift+R to change mode when routing.
7. Always put small mark on pin 1 with “1” and a small circle during footprint.
8. Change grid when things are not snapping into place.
9. Once length matching and differential tracks are done; start doing polygons.
10. Current carrying capacity to know the trace width for certain currents.
11. Spread tracks when you have extra space.
12. Make sure tracks are not close to edge or mounting holes.
13. Fix all silkscreen; don’t change in footprint because it will change it for every project; right clock silkscreen and change primitive.

Lesson 10

1. Put as much information as you can to reduce back and forth question with PCB manufacturing.
2. See Fedevel’s template information: Stack up info, Company, version, panelization, etc.
3. Be descriptive about labels on silkscreen if space allowed.
4. Most important output is Gerber files and drilling files.
5. Limit power supply when testing board.

\*Download and organize all files

Advanced PCB Layout

Lesson 1

**Placement**

1. If placement is not right, your board may not work.
2. If placement is right, layout will be much easier.
3. What component would you place first? Microprocessors, then memories (since they are connected with the most important interface.
4. Shift+Ctrl+X Cross Select Mode.
5. In high density layout, place the big components first to their most and closes connections.
6. When placing power supplies, always look at PC Board Layout Guidelines (good chip will always have this available.
7. When routing, make sure to have a good stack up.
8. Panel-PCB to show netlist.
9. Right Click-Preference-PCB Editor-DRC Violation Display-Check component clearance to highlight clearance issue with green.
10. Always think about the routing of power line.
11. Once you place the important components and mounting holes, lock them down.
12. Always put mounting holes.
13. Make outline for footprints a little bit bigger to help with clearance during placement.
14. Do not place components touching the edge. Especially high speed components to avoid emc (electromagnetic compatibility) issues.
15. Place components the heat up on one side and on the top layer so heat escapes (heat goes up); or connect a heatsink (plan ahead since it is bulky and heavy, make sure there is enough support especially when board goes into high vib).
16. Place smaller components on bottom and big components on top. Think about the enclosure it goes into.
17. ALWAYS SEE DESIGN GUIDE FOR CHIPS/ICs USED (for decoupling capacitor, placement etc)!
18. In placement stage, you guys want to see how much space you have. So it is okay to commit clearance issues.
19. Components that needs to be placed near power pin: decoupling capacitor (very close), zero ohm resistors, beads, ferrites, (everything use to power local power planes.
20. Use short tracks for precise resistors, calibration resistors and capacitors; place closest to the pin where they are used.
21. Series resistors, capacitors, place them close to the output.
22. Crystal put close to its pins.
23. Pull ups if used as termination resistors, place them ideally at the end of the line; if use for configuration, it’s useful to place near close to processor.
24. How do you know when to put component top or bottom: path of lease resistance, straight connection avoid placing vias…plan ahead. And try to make it look nice and symmetric. It’s art.
25. Avoid using vias for high speed tracks.
26. Do placement of all components first before starting layout.
27. Always think about how your board will be mounted.
28. ESD discharge through the lowest impedance; the enclosure. Sure some connector have a good contact with the panel/enclosure.
29. Place all analog and digital on their own side/layer.
30. Also know the environment your board will got to so you know if you need to put mounting holes on specific spots.
31. Always try to use a through hole connector; never use smd connectors (it’s got less plug in plug out cycle for obvious reason.
32. Add info about height clearance.
33. Silkscreen is for you, user, and the manufacturer. Make it easier for everyone.
34. Use descriptive names for silkscreens for components.
35. Put test points on bottom. Why? Because you can do pogo pins (Bed of Nails).
    1. Add descriptive labels on test points.
36. Always visualize how high current will be distributed through the board.
    1. USB, PCI express cards, etc
    2. Place it as close as possible
    3. Always remember, current produces magnetic field
37. Where should you place ESD protection circuit? Close connector or deep into the board? Close to the connector because that’s where most user touch occurs.
38. Filters should be placed near comm connectors.
39. Don’t place components near or at through holes to avoid short circuit and less expensive.
40. Ctrl and click track to highlight it; ctrl+shift clock to select multiple. Will be helpfule for checking and visualizing paths for comm interface (high speed tracks).
41. One of the rules for high-speed interface, there should not be any stopped; should be continuous.
42. For resistors that needs to be change, place in accessible areas.
43. Put big capacitors near the outputs; some capacitors can be placed under the power pins where the big current will flow.
44. You can place decoupling capacitors around memory.
45. Group components that need in a certain position (mounting holes and its components for example): select, right click, and create union.
46. Basic rules in the beginning of layout: Tools-Design rule check-change stop when xxx violation found to high for continuous work time; uncheck un-routed net in rules to check.
47. PCBlayout-Design-rules
    1. Silk to solder mask clearance = 0.1mm
    2. Min solder mask silver = 0.1mm
48. PCB Rules and Violation tab to easily browse through errors.
49. Print footprints and compare with actual components; do a paper layout.
    1. Plug in mating connectors, add sd cards; check clearance. Make sure there is no conflict.
       1. Or save as stp file and check in solidworks.
    2. Check if components are solderable.
    3. Improve footprints; improve placements.
    4. Always update update files when doing changes: right click and update docs
50. Altium have template designs. You can import parts and save time.
51. Assignment: Place big components and place its passive components close to it for easy routing.

Lesson 2

**Starting: Basic Stack-up rules, Fanout, connection**

**Stackup**

1. Layer vs Plane: Plane is pure copper connected to one net; Layer is standard layer you draw nets and polygons.
2. Add as much as you think you need at first; omit and add more as necessary.
3. Name L1, L2 Ln…….
4. Pullback is how much copper is from the PCB edge. 01mm for typical number
5. If the power plane edge is retracted 20H of the ground plane edge, 70% of the energy radiation can be repressed (use 1mm).
6. 2 Basic rules for every PCB:
   1. Minimum clearance: space between two tracks. (0.1mm…at first)
   2. Minimum track width (0.1mm…at first)
7. Always ask PCB house for minimum values or check their website.
8. Minimum track width for power tracks (wider than signal): 0.2mm (twice as the signal).
9. Via:
   1. Diameter 0.24mm min and 4max (preferred 0.45mm)
   2. Hole Size: 0.09 mm min and 4mm max (preferred 0.2)
10. Put + sign on all power net names.
11. Use 0.1 grid when doing fanout.
12. Use tab when you want to change setting while routing.
13. In the beginning, it always look like it will not fit. Just keep trying to improve placement and track routing.

**Fanout**

1. Start fanout on pwr and gnd nets.
2. Take advantage of dedicated planes/layers for power and ground nets. Use fanouts.
3. Play it like sudoku: Start with something you are most sure then expand from there. Adjust as necessary.
4. Always try to place 1 through hole via per power pin.
5. Always try to make as short connection as possible
6. Memory chips are design so that fanouts for power and gnd can share vias (since pinouts are basically mirrored.
7. Fanout pins on the first layer away from the BGA; same on all side (facing out of the BGA chip to avoid busy area).
8. Micro vias: 0.1mm size and 0.27mm diameter, and make sure it’s masked. Make sure you specify starting layer to end layer.
9. Through hole size: max PCB thickness = (min through via hole size) X10; for micro via it is 1:1 (see video and diagram)
10. Read reference sheet for tracking rules for chips.
11. Min distance of via holes for fanning out should be enough to route a track in between.
    1. Also think about the polygon shape for the power planes. You don’t want a very thin paths for the polygons.
12. Just route tracks somehow and worry about length matching later.
13. Where should you start fanning out? Middle of processor.
14. How to decide to use micro or full vias?
    1. Use micro vias with the group with the greatest number of signals.
15. Keep fanout connection short.
16. Don’t close vias too close (See rules).
17. Remember rules about board thickness and via hole size.
18. Don’t place micro vias under pads.
19. Don’t route the track 0.2mm from holes.
20. Always read design guide before start routing.

**DDR 3 routing Length Matching**

1. Rules are different for different processors so make sure you read datasheet.
2. Why route in groups? To make routing easier.
3. To create group (Net Classes):
   1. Place-directive-blanket-select nets to group
   2. Place-directive-net class-select the blanketed group
   3. Design-update PCB
   4. Assign color for visual help
4. All signal in the same group should be routed the same way.

**Differential Pair rules**

1. 0.1mm for everything as default
   1. Then route to occupy space needed
   2. Change the rules later and adjust as necessary.
2. Use differential routing for differential signals.
3. Leave big gap between other signals from differential pairs (same with clock signal).
4. Why do we do length matching? To have the signal pairs to arrive at destination at the same time.
5. Do preliminary length matching at first. Make it longer than necessary to have a better idea of space.

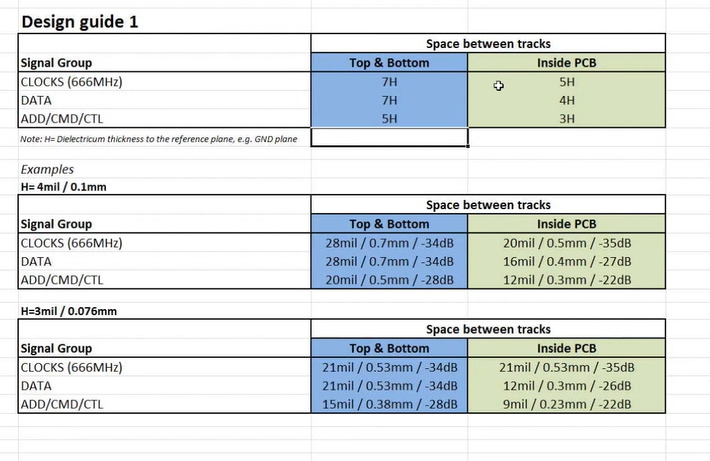
**Routing**

1. Dedicate layer(s) for group of signals.
2. Don’t fully connect two points right away. Do routing by group/sections and visualize spacing.
3. Byte swap as necessary to make routing after fanout easier. Goal is to reduce crossovers.

**Lesson 3**

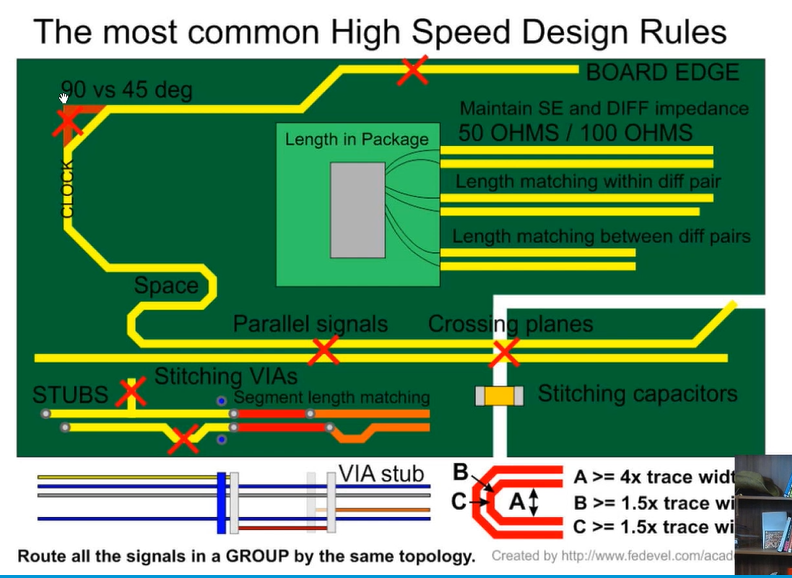
1. Try to avoid interface crossing.
2. Route most signals to just one layer but think ahead for the rest.
3. Ideally start with pads that runs on high frequency.
4. Make sure to fanout all the pins of BGA.
5. Place vias early.
6. Place wires in the same direction, then add the vias.
7. Start with high speed first.
8. If possible, route vias so that the current flows through the via, to the to capacitor to power pad. For gnd pads, place vias as close as possible.
9. Short and wide track for power and gnd lines.
10. Ideally, one power via per power pin; same with gnd pins.
11. [PCB via tool](:%20https:/saturnpcb.com/saturn-pcb-toolkit/) to calculate current max through vias.
12. Smaller the via size, the lower the current rating.
13. Make custom grid: Measure pitch of pins/pad – snap – grid – modify – apply.
14. Hole sizes to set up in PCB rules as macro
    1. Through hole via: Size: 0.45mm, Hole Size: 0.2mm
       1. Start layer L1 and Stop Layer is L12
    2. uVia: Size: Size: 0.27mm, Hole Size: 0.1mm
       1. Start layer L1 and Stop Layer is Lx
    3. Buried via: same as Through hole, just change the layers.
       1. Start layer Lx and Stop Layer is Ly
15. “+” key to change layer when routing (need to have layer to active).
16. Masked vias to make it safer.
17. Double check component placement and mounting hole position.

**High Speed**

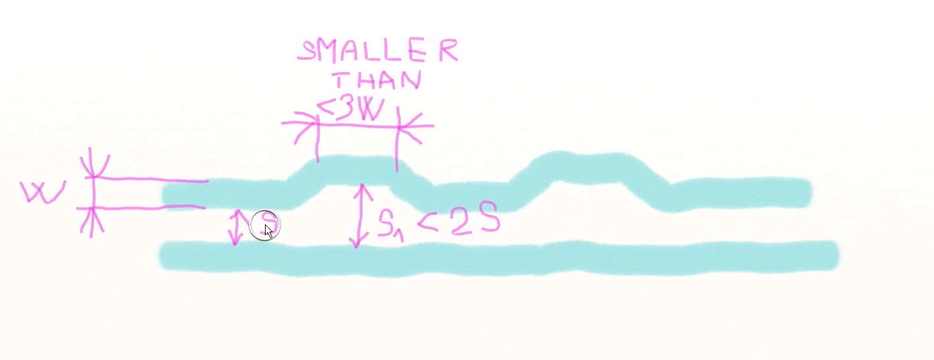
1. Cross talk (noise)
2. Use crosstalk calculator from Saturn PCB design (see 11).
3. High layer PCB can significantly reduce crosstalk.
   1. Crosstalk depends on conductor height.
   2. Don’t use 2-layer PCB if you can.
4. Crosstalk does not depend on frequency but on rise (or falling) time.
   1. This mean not just high freq component can generate crosstalk.
5. 
6. Crosstalk is different from top and bottom layer and mid layers.
7. -35dB crosstalk coefficient and lower is better
8. If you match impedance can lower crosstalk coefficient. This will be seen in design guide.
   1. Every output, input and track have its own impedance, and if you match these all 3 together, the signal quality will be the best.
9. How can you match impedance?
   1. Check design guide (impedance signal recommendations.
   2. Contact PCB manufacturer for the impedance number given your PCB stackup.
   3. Use Saturn PCB design software and use conductor impedance.
10. You need reference plane on your stack up.
    1. GND is the best reference plane.

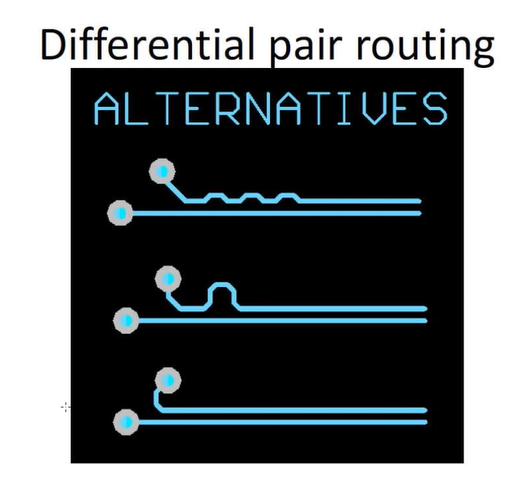
**Lesson 4**

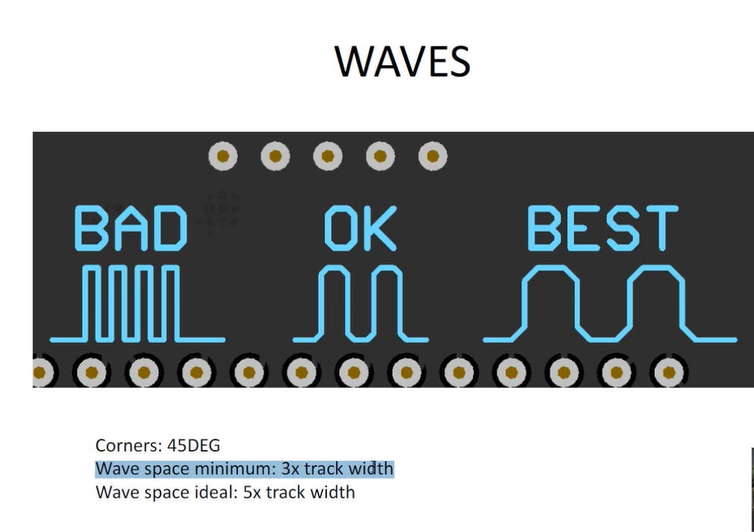
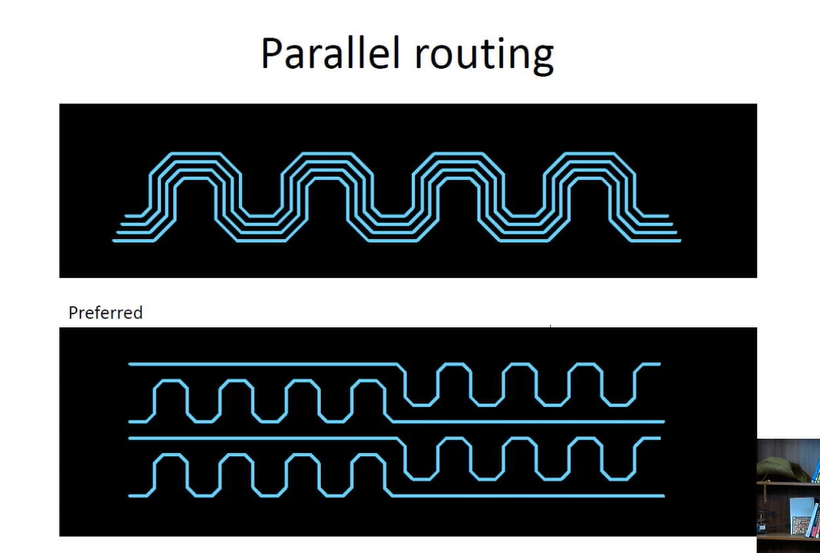
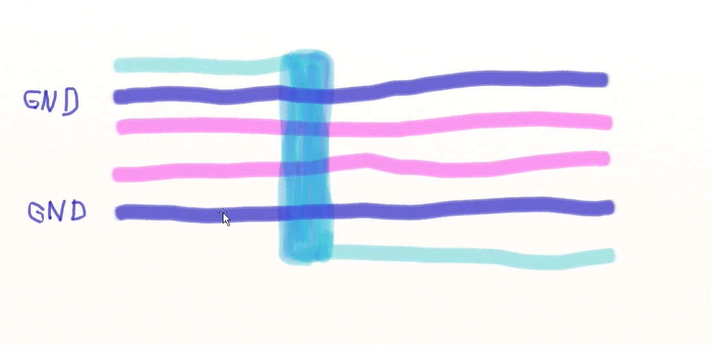
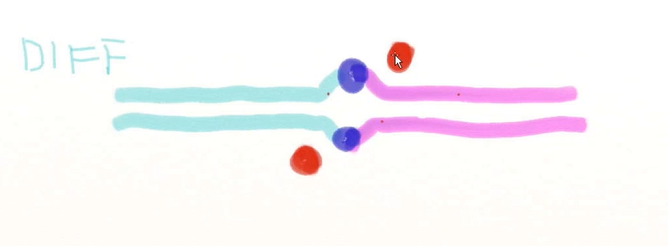
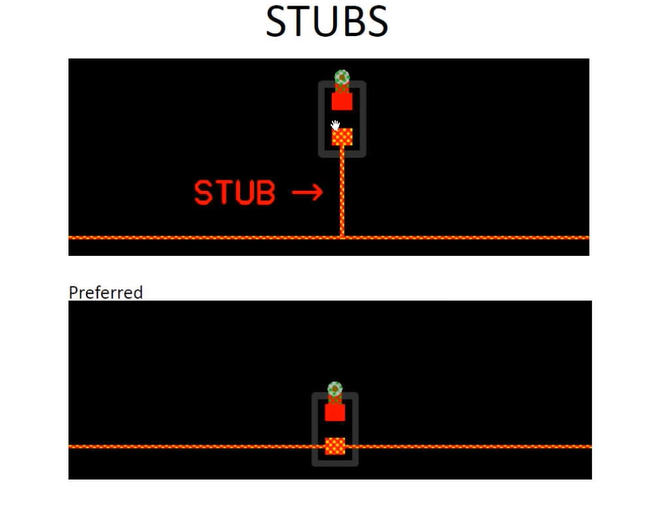
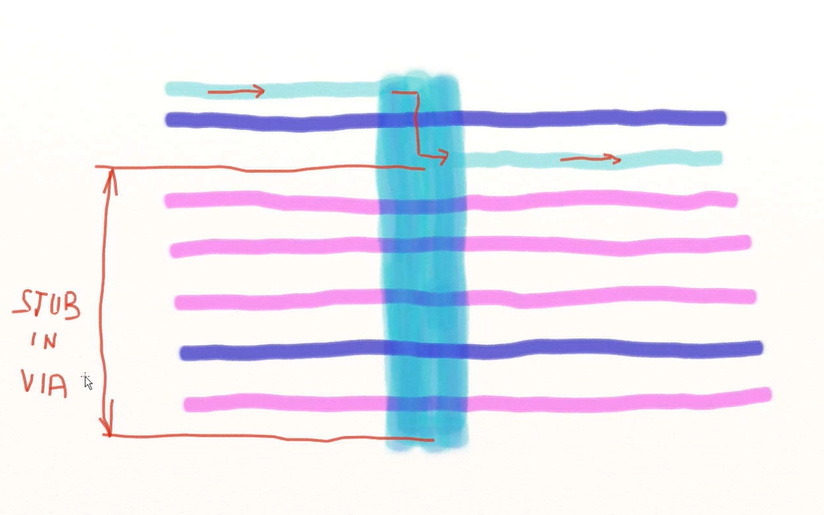
**11 Most Common High Speed Design Rules**

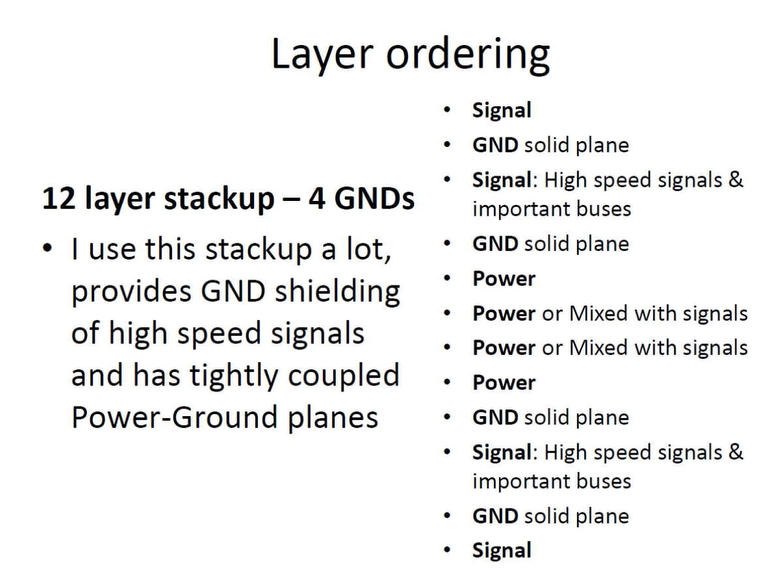


1. Maintain Single Ended and Differential pair impedance.
   1. Look at design guide impedance signal recommendation and use your impedance calculator to calculate your numbers (or sometimes there is a table available).
   2. When not possible to follow design guide closely, try to deviate just a little bit but make sure to simulate/test/double check if changes are acceptable.
   3. Set up Altium for high speed to save time
      1. There is a button for differential pair. Labeled differential named net with xxx\_N and xxx\_P – Place tab – Directives – Differential Pair – select differential pair net lines. Add a class name for visual help you see impedance; this way can be grouped into differential group.
      2. All Differential pairs is grouped in PCB panel
      3. Differential Pair Class: Design – Classes – Differential Pair Class – Right Click - Add Class – Place all differential pair signal in one group.
      4. Rule Wizard: Tolerance 5mil; put number for your stackup from your calculator;
2. Length match differential pair signals within pair.
   1. Length match within layer (not total length).
   2. Add extra length to a pair as necessary.
   3. Add waves to length match. Ideally…

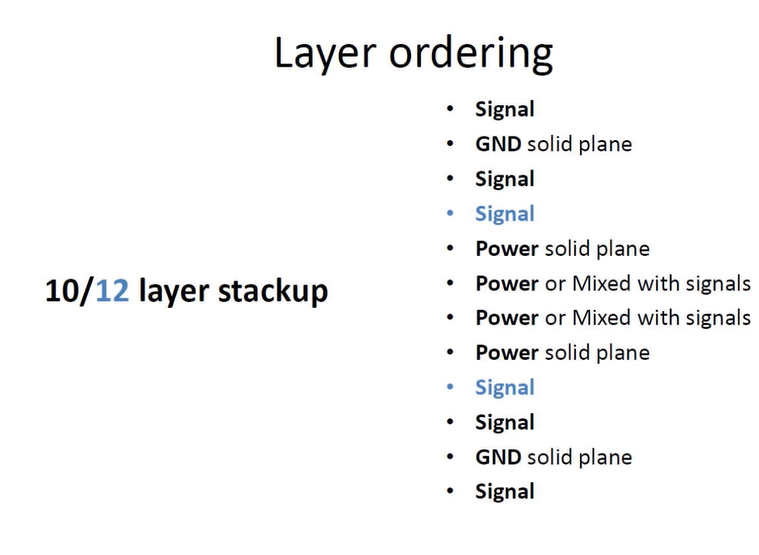


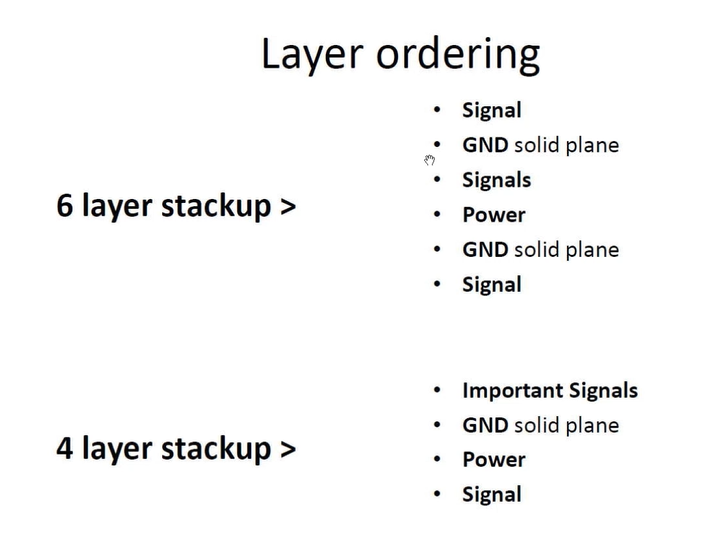
* 1. 
  2. Do not do right angles.
  3. 

1. Keep space between “waves”.
   1. 
   2. Initially, occupy space with large waves.
2. Length match busses and differential pairs.
   1. See design guide for numbers.
   2. Ignore termination resistors (or series resistors, or other passive components) in length calculations.
      1. Make sure termination resistors are as close as possible to the outputs.
   3. Again, max difference between differential pairs is 5mm.
   4. Use spreadsheet as necessary to help with calculation.
   5. Manually check on tracks if no segment overlaps in a track because Altium will calculate those segments in total length calculation.
   6. 
   7. Signal on top vs bottom move at different rate. Therefore, try to do the via layer switch at around the same spot.
3. Route signal groups by same topology.
   1. Start on same layer, continue on same layer…..and end in same layer.
   2. Help you a lot with length calculation.
4. Be aware of tracks running in parallel.
   1. Clock especially
      1. Place via around clock as a protection
   2. Between 2 differential pairs.
   3. Reset signals are routed away from high speed and clock signal.
   4. Crosstalk can also happen between 2 tracks in parallel in two different layers.
      1. Try to route them perpendicular (vs parallel.
   5. Route tracks in as much as you can in the beginning. Optimize at the end.
   6. Keep tracks and clearance with bigger min values at first then change it during optimization.
5. Use stitching VIAs when reference plane changes. This help keep a good return path for signals. See design guide for suggested numbers.
   1. 
   2. 
6. Do not use 90 degrees angles.
7. Do not do stubs.
   1. 
   2. Stub in via: 
   3. Minimize via anyways for high speed. Try to keep straight connection in same layer.
8. Do no route close to the board/plane edge or a hole.
   1. External signal may influence signal near edge.
   2. Keep clearance of 3H or 15mils.
9. Do not cross planes.
   1. Add stitching capacitor (since caps are short ckt for high speed signals).
   2. When designing stack up, place solid gnd plane closer to the signal layer than the power plane with a lot of polygons.

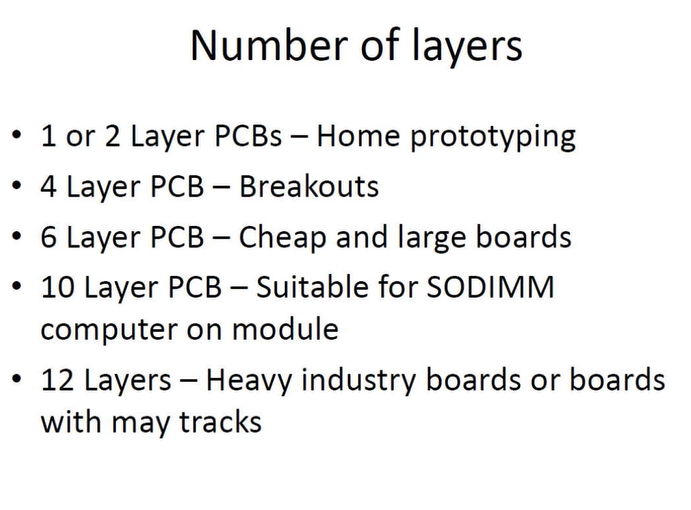
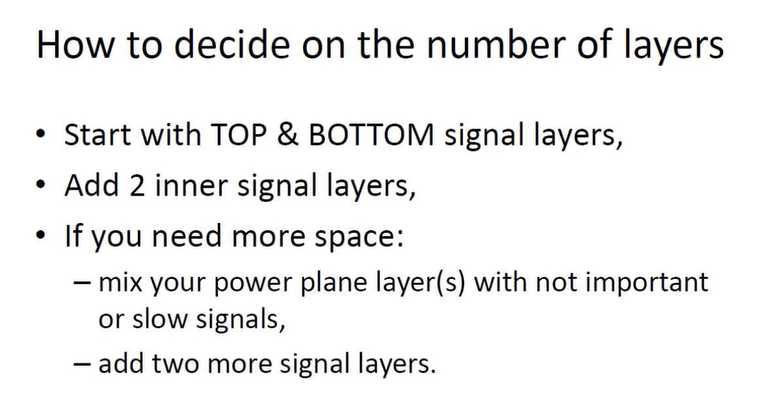
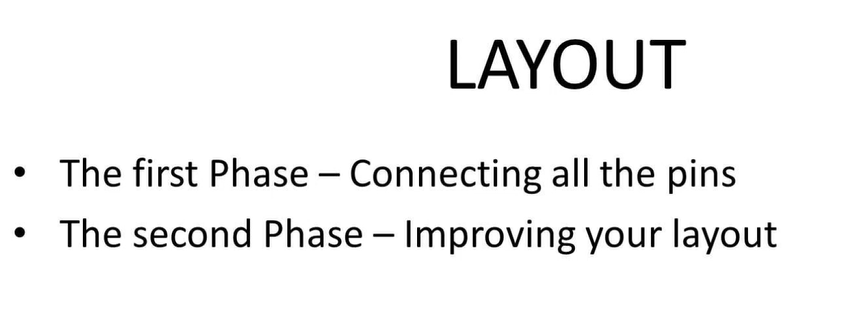


Layering ordering for solid plane gnds





**Lesson 5 Layout**

1. 
2. 
3. 
4. Layout: Phase 1 – Connecting all the pins
   1. Set up basic rules
      1. See the manufacturers for your board’s numbers; may have to go back and forth few times.
   2. Set up a basic stack up.
      1. If you do know the stack up, set it up; if not, just set a basic one to get started
   3. Do fanout under CPU
   4. Do preliminary memory layout
   5. Do fanout under other BGAs.
   6. Do CPU fanout for big and wide buses, do fanout in the way of these and route them.
   7. Do CPU fanout of differential pairs, do fanout in the way of these, route them
   8. Do rest of CPU fanout
   9. Do fanout for all components
   10. Connect long buses
   11. Do local connections (ie audio, power supply….)
   12. Connect power nets (or between steps 3-5)
   13. Connect all the pins and run DRC
5. Layout: Phase 2 – Improving your layout
   1. Set the real stackup
   2. Set the real differential pair rules; redraw all differential pairs
   3. Do preliminary memory length matching
   4. Do preliminary diff pair length matching
   5. Do preliminary length matching of other signals
   6. Improve & spread all the tracks
   7. Clear all electrical DRC
   8. Create power planes and polygons, check high current tracks
   9. Check all the nets one-by-one
      1. PCB panel
      2. Nets – all Net
   10. Add stitching VIAs
   11. Do final length matching (except memory)
   12. Do memory final length matching
   13. Lock down important tracks
   14. Clear rest of DRCs
   15. Add compony name, copyright, year, board name &version
   16. Add manufacturing information
   17. Adjust track width to achieve 50 ohm impedance
6. Time period for this kind of projects: 3 months
7. Shift+R to change rules to follow when improving layout.
8. Having tracks in all vertically/horizontally in same layers or spaces.
9. Hide as any tracks inside 2 ground planes.
10. Name signals (especially the important ones).
11. When routing diff pairs, make sure you have enough space so consume as much space.
    1. When needed to swap position of diff pairs, swap it during layer change.
12. Feedback signal tracks need to be short and wide.
13. Always read the datasheet of chips to see recommended track width etc.
14. Keep pad gaps as it is in original footprint.
15. Don’t put track near the track of crystal and oscillator. Put gnd track around it instead.
    1. Also keep as short as possible.
16. Keep clocks away from other signals.
17. Be mindful where to put vias near metallic connector housing.
18. Never mount under mounting holes.
19. Generally, connect all mounting holes to gnd.
20. For some specific spots, especially BGAs, make special case rules.
    1. Check min clearance (get your numbers).
    2. Rules
    3. Create new rules
    4. Add in query, and input your new numbers.
21. Useful tips to delete tracks
    1. Select last segment and hit backspace
    2. Redraw and double clock
22. To navigate easily, use navigator
    1. You have to compile first always
    2. Right clock on net and zoom in/mask
    3. (you can also use prober)
    4. Double screen will help a lot
    5. Set layer set
       1. Shift-S to change single layer
    6. Use filters when working with either tracks vs vias
23. Snap points for cltr c and ctrl v. Where you select when you ctrl+c is your reference point when you ctrl+v.
24. How route analog tracks?
    1. Read design guide and reference documents
    2. Place analog components in one side of the pcb
    3. Route on only one layer as much as you can
    4. Place gnd planes near analog layers
25. It is okay to connect analog and digital gnd planes.
    1. (there might be some special cases so always check reference guide.
26. Always put design note for max Current and required current on power supply schematic document.
27. Place through vias on polygons to help take heat away.
    1. Don’t place vias very close to each other to avoid cutting the polygons in pieces
    2. PCB can also lose firmness if through hole vias are placed very close to each other (itll make unintended perforated line).
28. Make polygons as wide as possible to distribute the heat.
29. Do polygons last.
30. Place power and gnd planes in middle of your board.

**Lesson 6**

**Making Length Matching easier**

1. Set up a special rule
   1. Design-rules-high speed- matched net lengthts-new rule-check if all the signal in “bank” is in tolerance in 10 mils (of course you have to make all the data banks first).
   2. PCB panel will highlight if signals in the group is not within tolerance.
   3. Tools-interactive length tuning (for Altium to automatically add signal length needed to be to match).
   4. Press tab while tuning to adjust the waves; gaps should be 5x track width.
   5. “1” and “2” changes the angle of curves.
   6. Right click-union-explode length tuning to manually adjust it.
2. Segmented tracks connected through vias cannot be calculated automatically in Altium yet. You’d have to use “measure selected object” and do the math to match manually
   1. Holding ctrl key while laying track can turn off auto snap on grid.
3. If you don’t have enough space for the waves, add them to other segments.
4. Check design guide first to check length requirement but as rule-of-thumb, just use 10mils tolerance.
5. Connect everything first to know how much space you have. Do fine tuning towards the end.
6. Leave enough space for clocks. They need a lot of space to match.
7. T-branch vs Flyby:



1. Once done with all the tracks, check if tracks can be further spread out on each layers.

**Polygons and planes**

1. Before starting polygons, make sure you set up the pullbacks of the power (gnd and high) layers correctly: 0.1mm.
   1. Pullback is the distance between the copper and the edge.
   2. To assign net on layers, double click on layer and a drop down menu will pop out and select your power assignment.
      1. To assign more different power on the same layer, just add a section using lines and double click repeat 9.a.
   3. Instead of b.i, draw polygons instead.
      1. “Pour Over all same Net objects”
      2. Check remove dead copper
      3. Check is poured
   4. Polygon Manager can setup priority on polygons
2. Be creative where to place the edge of polygons.
3. Lockdown parts, tracks, pieces, vias, if you’re sure about their positions.

**Lesson 7**

1. Do a layout checklist (see template online).
2. Double check every single net on every single layer.
3. Make sure to fine tune diff pair to length match the best you can.
   1. Lock down as you go (even its corresponding vias).
4. Use filters to make condition statement to check power lines: “For all Gnd, track and is width < xx.xx.
5. Some rules that are set cant be followed all the time. Try your best to avoid all violation and clear the rules once no more choice is available.
6. For silkscreen error, right click overlaps or gap violation and right click and change primitive and adjust manually. If done in PCB footprint, itll change for all projects that used it.
7. Disable silk to board clearance when using it to check clearance for mating connector.
8. If given enough time and space, improve the aesthetic of the board. But always remember functionality and quality >> look.
9. Add board name, version, copyright, designer, company.
10. To add logo/picture: Word-black and white picture, ctrl+c – go to slelected layer ctrlv- resize – place.
11. When space permits, be descriptive on component labels: +5V power, Reset switch, on/off switch, etc.
12. Know how to use the filter to easily clean up board.
13. Use parameters for version/revision to automatically change all document:   
    Project Option – parameter
14. Panelization: Create copy of layout - Place tab – embedded board- panelize.
15. Check for double segments: go to a layer – select a track – Go to a different layer (to see segment properly) check each segment.
16. Check board with o-scope, environmental chamber (to see edge cases temperature wise).
17. Change the track width to achieve ideal impedance (use filter to change all of them all at once).
18. Generate gerber files.
19. ViewMate is a free gerber viewer to double check your gerber files.
20. Check spellings.

Arduino

1. Top Overlay – Silkscreen; footprints; white tracks on around the components on PCB.

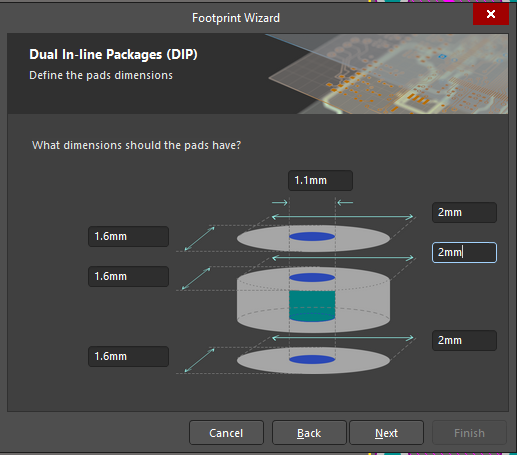
Top Layer – Copper; Pads where components sit and will be soldered.

Top Solder – Solder/Masked layer; Area with no green/blue color on PCB.

Top Paste – Layer with Tin; use stencil to place the Tin.

\*Same with Bottom Overlay, Layer, Solder, Paste

1. For PCB library, always use Top side; just place components on bottom during layout.
2. When creating PCB Lib for components, always put the reference point in the middle of the component for the pick and place machine: Edit>Set Reference>Center.
3. Top overlay drawing lines 0.2mm.
4. Mils=0.001 inch=0.0254mm
5. “q” to change grid from mils to mm
6. During PCB Lib creation, make footprints (top overlay) big as big (or a little bigger) than components.
7. Get 3D model higher up using standoff height in properties; 3.2mm for DIP packages.
8. Shift-S for Single layer mode: you only see active/selected layer.
9. X, Y to flip a group of pins about axis
10. 2.54mm pitch through hole headers TYP, but holder diameter (first dimension) is different, check datasheet.



1. Always check datasheet to check footprint drawing.
2. Shift+Ctrl+G for snap grid.
3. Cut tape is the easiest packaging for prototyping.
4. Reflow vs Wave soldering:
5. Always choose the higher tolerance for fittings to make sure it always fits.
6. Check schematic for manufacturers hardware design guide for noise filtering power supplies.
7. When choosing capacitors, keep in mind that the higher the capacitance, the more expensive it is for higher rated voltages. Low capacitance caps almost have the same price for a range of voltages.
8. Footprint for same type of components is the same ie 0805 caps; JUST ALWAYS CHECK FOR THE HEIGHT IN DATASHEET AND ALWAYS USE THE HIGHER END (SEE NOTE 16).
9. Place decoupling or noise filtering capacitor directly/close to uController’s VCC and GND.
10. Always check current rating when choosing Ferrite Beads.
11. CT = Cut Tape
12. Resistors tolerance for PCBs are mostly 1%-5% (same price).
13. It’s a good practice to place 22 or 33 series termination resistors on clock signal.
14. For diodes: pin 1 cathode, pin 2 anode
15. CTRL+M to measure; SHIFT+C to clear
16. Sometimes, datasheet suggest top paste dimension.
17. Always mark the cathode side of diodes in footprint.
18. Series resistor is to limit current. To calculate:
    1. Forward Current - max current that can flow through current
    2. Forward Voltage – min voltage to turn the voltage)
    3. Min Value of Resistor (meaning max current, not recommended)

= (Vsupply – Forward Voltage) / Forward Current

* 1. Go higher to “limit” current. Just remember, the higher the value, the dimmer the LED.

1. Check Datasheet for pads that are for multilayer etc when creating footprints (usually for interface connectors ie USBs).
2. For through holes pads, one parameter in properties is important: Plated. Plated/Platting means there is a copper connecting bottom and top layer.
3. Always include info on footprint of connectors (ie USB) about the max width of the mating connector. Why? If you need to place more connector on the same edge, you can easily eyeball the minimum distance between connector placements.
4. Varistor: Voltage Dependent Resistor. Component used to protect from ESD.
5. CLC circuit (see USB connector) is to filter power (peaks and dropouts) coming from the PC to UCB micro connector to the board. Output power is just as important as input power so filter both sides.
6. Some resistors are used to limit current to protect on different logic levels.
7. **Fiducials: Fiducials are small pads that are placed on a PCB to aid Pick & Place machines during component placement. They are also frequently added to the rails of a PCB array. To achieve better assembly results, we recommend that you always add fiducials to your PCB design. (No paste in the fiducial: paste mask expansion is -40mil).**
8. Add standard screw head size on top overlay of mounting holes to help prevent placing components around it.
9. Annotation: Replacing “?” with numbering.

Tools-Annotation-Annotate Schematic-Update Changes List-Accept-Validate Changes-Execute Changes

1. Validate/Compile and check for error messages.
2. Best way to check schematic is through the navigator panel.
   1. Right click on Net name and use graph for better visualization.
3. Always annotate and add labels.
4. Add title block info as parameters: Project – Project Option – Parameters
5. Even if there is no error after compiling, there can still be difference between schematic and PCB. Design – Update Schematic Document
6. PCB Placmente Tip: View-Connection-Hide All to hide connection; Use PCB filter to hide Connection (IsDesignator). 0.1mm snap grid for general size components placement.
7. Once placement of component(s) is good, select then lock.
8. Best way to do placement is to put schematic next to pcb layout. Select tools-Cross Select Mode
9. Always place decoupling capacitors near power.
10. Right Click-cross probe to highlight net connections in pcb layout to know the best placement for components.
11. Tools – Component Placement-reposition selected components to pick up components by clicking schematics.
12. Put Crystals as close as possible to the pin.
13. ESD protection components should be place close to its connection; straight connection, no via holes or change layer.
14. Always place coupling capacitors near power pins, especially for voltage regulators (read datasheet for recommendation).
15. Hold Ctrl and click pad to see what’s connected in pcb layout.
16. Tools-design rule check to change error rules.
17. Ask PCB manufacturer: Ask minimum clearance, min track width, min routing via.
18. Layer Stack: Design-Layer Stack Manager
19. Layers are usually named L1, L2, etc
20. 2 Layer PCB is usually 1.6mm
21. Set color on Nets: typical GND is blue, Power is Red
22. To switch components from top to bottom (or vice versa) press “L”.
23. For 2 layer pcb, try to route most signals in one layer.
24. Ctrl+Shif+Scroll to change layers (and add via) while routing.
25. Shift+S to single out a layer for better view.

Side Notes

1. Electrolytic capacitors need to be kept cool (because of the liquid inside); but never too cool because ESR will shoot to the roof. Never placed near heatsink.