

- [Interview](#)
- [Online Test](#)

Placement Papers :: Wipro

@ : [Home](#) > [Placement Papers](#) > [Wipro](#) > View Paper

WIPRO Placement Paper (Aptitude and Technical) January 2010

Rated : +34 , -7

1. If the time quantum is too large, Round Robin scheduling degenerates to

- (a) Shortest Job First Scheduling
- (b) Multilevel Queue Scheduling
- (c) FCFS
- (d) None of the above

Ans. (c)

2. Transponders are used for which of the following purposes

- (a) Uplinking
- (b) Downlinking
- (c) Both (a) and (b)
- (d) None of the above

Ans. (c)

3. The format specifier "%d" is used for which purpose in C

- (a) Left justifying a string
- (b) Right justifying a string
- (c) Removing a string from the console
- (d) Used for the scope specification of a char[] variable

Ans. (a)

4. A sorting algorithm which can prove to be a best time algorithm in one case and a worst time algorithm in worst case is

- (a) Quick Sort
- (b) Heap Sort

Companies

- [3i Infotech](#)
- [AAI](#)
- [ABACUS](#)
- [ABB](#)
- [Accel Frontline](#)
- [Accenture](#)
- [Aditi](#)
- [Adobe](#)
- [ADP](#)
- [Agreeya](#)
- [Akamai](#)

- [Alcatel Lucent](#) (c) Merge Sort
- [Allfon](#) (d) Insert Sort
- [Alumnus](#)
- [Amazon](#) Ans. (a)
- [Amdocs](#)
- [AMI](#) 5. What details should never be found in the top level of a top-down design?
- [Andhra Bank](#) (a) Details
- [AppLabs](#) (b) Coding
- [Apps](#) (c) Decisions
- [Associates](#) (d) None of the above
- [Aricent](#)
- [Ashok Leyland](#) Ans. (c)
- [Aspire](#)
- [Atos Origin](#) 6. In an absolute loading scheme, which loader function is accomplished by assembler
- [Axes](#)
- [Bajaj](#) (a) Reallocation
- [Bank of](#) (b) Allocation
- [Maharashtra](#) (c) Linking
- [BEL](#) (d) Both (a) and (b)
- [BEML](#)
- [BHEL](#) Ans. (d)
- [BirlaSoft](#)
- [Blue Dart](#) 7. Banker's algorithm for resource allocation deals with
- [Blue Star](#)
- [BOB](#) (a) Deadlock prevention
- [BPCL](#) (b) Deadlock avoidance
- [BPL](#) (c) Deadlock recovery
- [Brakes](#) (d) None of these
- [BSNL](#)
- [C-DOT](#) Ans. (b)
- [Cadence](#)
- [Calsoft](#) 8. Thrashing can be avoided if
- [Canara Bank](#) (a) The pages, belonging to the working set of the programs, are in main memory
- [Canarys](#) (b) The speed of CPU is increased
- [Capgemini](#) (c) The speed of I/O processor are increased
- [Caritor](#) (d) All of the above
- [Caterpillar](#)
- [CDAC](#) Ans. (a)
- [CGI](#)
- [Changepond](#) 9. Which of the following communications lines is best suited to interactive processing applications?

AdChoices [► Question Paper](#)[► Placement Papers](#)[► Wipro Interview](#)



- [Ciena](#)
- [Cisco](#)
- [Citicorp](#)
- [CMC](#)
- [Consagous](#)
- [Convergys](#)
- [CORDYS](#)
- [Crompton](#)
- [CSC](#)
- [CTS](#)
- [Cummins](#)
- [Dell](#)
- [Deloitte](#)
- [Delphi-TVS](#)
- [DeShaw](#)
- [Deutsche](#)
- [Dotcom](#)
- [DRDO](#)
- [EDS](#)
- [EIL](#)
- [ELGI](#)
- [ELICO](#)
- [ERICSSON](#)
- [Essar](#)
- [Fidelity](#)
- [Flextronics](#)
- [Freescale](#)
- [FXLabs](#)
- [GAIL](#)
- [GE](#)
- [Genpact](#)
- [Geodesic](#)
- [Geometric](#)
- [Globaledge](#)
- [GlobalLogic](#)
- [Godrej](#)
- [Google](#)
- [Grapecity](#)
- [HAL](#)
- [HCL](#)

- (a) Narrowband channels
- (b) Simplex channels
- (c) Full-duplex channels
- (d) Mixed band channels

Ans. (b)

10. A feasibility document should contain all of the following except

- (a) Project name
- (b) Problem descriptions
- (c) Feasible alternative
- (d) Data flow diagrams

Ans. (d)

11. What is the main function of a data link content monitor?

- (a) To detect problems in protocols
- (b) To determine the type of transmission used in a data link
- (c) To determine the type of switching used in a data link
- (d) To determine the flow of data

Ans. (a)

12. Which of the following is a broadband communications channel?

- (a) Coaxial cable
- (b) Fiber optic cable
- (c) Microwave circuits
- (d) All of the above

Ans. (d)

13. Which of the following memories has the shortest access time?

- (a) Cache memory
- (b) Magnetic bubble memory
- (c) Magnetic core memory
- (d) RAM

Ans. (a)

- [Hexaware](#)
- [Honeywell](#)
- [HP](#)
- [HPCL](#)
- [HSBC](#)
- [Huawei](#)
- [Hughes](#)
- [IBM](#)
- [IBS](#)
- [ICICI](#)
- [iGate](#)
- [Impetus](#)
- [iNautix](#)
- [Indian Airforce](#)
- [Indian Airlines](#)
- [Infosys](#)
- [Infotech](#)
- [Intec](#)
- [Integra](#)
- [Intergraph](#)
- [IOCL](#)
- [iSOFT](#)
- [ISRO](#)
- [Ittiam](#)
- [JSW](#)
- [Keane](#)
- [Kenexa](#)
- [L & T](#)
- [L & T Infotech](#)
- [LG Soft](#)
- [Lifetree](#)
- [LionBridge](#)
- [Mahindra Satyam](#)
- [Mastek](#)
- [Maveric](#)
- [McAfee](#)
- [MECON](#)
- [Microsoft](#)

14. A shift register can be used for

- (a) Parallel to serial conversion
- (b) Serial to parallel conversion
- (c) Digital delay line
- (d) All the above

Ans. (d)

15. In which of the following page replacement policies, Balady's anomaly occurs?

- (a) FIFO
- (b) LRU
- (c) LFU
- (d) NRU

Ans. (a)

16. Subschema can be used to

- (a) Create very different, personalised views of the same data
- (b) Present information in different formats
- (c) Hide sensitive information by omitting fields from the sub-schema's description
- (d) All of the above

Ans. (d)

17. A 12 address lines maps to the memory of

- a. 1k bytes b. 0.5k bytes c. 2k bytes d. none

Ans: b

18. In a processor these are 120 instructions . Bits needed to implement this instructions

- [a] 6 [b] 7 [c] 10 [d] none

Ans: b

19. In a compiler there is 36 bit for a word and to store a character 8bits are needed. IN this to store a character two words are appended .Then for storing a K characters string, How many words are needed.

- [a] $2k/9$ [b] $(2k+8/9)$ [c] $(k+8/9)$ [d] $2*(k+8/9)$ [e] none



- [MindTree](#)
- [Miraclesoft](#)
- [Mistral](#)
- [Motorola](#)
- [Mphasis](#)
- [MTNL](#)
- [NIC](#)
- [Nokia Siemens](#)
- [Novell](#)
- [NTPC](#)
- [Nucleus](#)
- [ORACLE](#)
- [Patni](#)
- [Perot](#)
- [Polaris](#)
- [Ramco](#)
- [Robert Bosch](#)
- [Samsung](#)
- [SAP](#)
- [Sapient](#)
- [Sasken](#)
- [SBI](#)
- [Sierra Atlantic](#)
- [Sonata](#)
- [Sony India](#)
- [Sutherland](#)
- [Syntel](#)
- [TCS](#)
- [Tech Mahindra](#)
- [VeriFone](#)
- [Virtusa](#)
- [Wipro](#)
- [Zensar](#)

Ans: a

20. Virtual memory size depends on

[a] address lines [b] data bus

[c] disc space [d] a & c [e] none

Ans : a

Like this? +34 👍 -7 👎



Read more: