Question 1 (20 points): The access time to the main memory that serves data and instructions to a processor is 70 ns. For a given program, 20% of the instructions are loads or stores. The design team is considering two versions for the processor:

- **Design A**, with an 8 KB unified L1 cache that has a miss rate of 4.0%.
- **Design B**, with a 16 KB L1 unified cache that has a hit time of 1.07 ns.

In both designs, the hit time of the L1 cache determines the clock cycle of the processor. Both designs are equiped with a 4 MB L2 cache that has a miss rate of 75% and a hit time of 12 ns.

1. (**7 points**) The Average Memory Acccess Time (AMAT) for design **A** was measured to be 3.5 ns. What is the clock cycle for this design?

2. (**7 points**) The AMAT for design **B** was measured to be 3.0 ns. What is the miss rate, expressed as a percentage, for the L1 cache in this design?

3. (**6 points**) A new member of the design team says that she can change the L1 of design **A** to reduce the clock cycle without affecting miss rate. As a manager, you are skeptical about her claim because you calculated how much faster the clock cycle would have to be to match design **B**. What should be the percent reduction in the hit time of L1 of design **A** for that design to have the same AMAT as design **B** for this program?