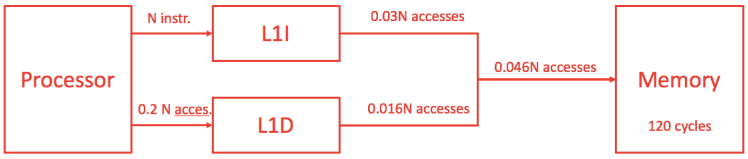
Question 3 (20 points): You have received a placement for your Science Internship Program with Redstoke Mobile Computer Solutions. They are evaluating a new hardware that they intend to use with a new app, called Wine4U, that is able to learn your taste on wine over time and make recommendations when you are at a store or restaurant. The processor in this hardware runs at a frequency of 2 GHz. The system has a level 1 instruction cache (L1I) and a level 1 data cache (L1D). The data access to L1D occurs in parallel with an instruction fetch from L1I. Both of them can complete a hit access in one cycle and for both of them an access is not started to the lower level until the access in the higher level is completed. While running Wine4U, the L1I has a hit rate of 97% and L1D has a hit rate of 92%. An access to main memory takes 60 nanoseconds. You have determined that 20% of the instructions executed by Wine4U are load/store instructions.

1. (**7 points**) What is the Average Memory Access Time (AMAT) for this system?



The combined number of accesses that leave L1I and L1D is: $0.03N + 0.08 \times 0.2N = 0.046N$
The L1D access happens at the memory stage of the pipeline and it occurs in parallel with an instruction fetch to the L1I. Therefore the time needed to access L1I should not be included when computing AMAT.

$$\begin{aligned}
\text{Clock Cycle} &= \frac{1}{\text{Frequency}} = \frac{1}{2 \times 10^9 \text{Hz}} = 0.5\ ns \\
\text{Memory Access} &= \frac{60\ ns}{0.5\ ns} = 120 \text{ cycles} \\
\text{AMAT} &= \frac{N + 0.046N \times 120}{N + 0.2N} \\
&= \frac{1.0 + 0.046 \times 120}{1.2} = \frac{6.52}{1.2} = 5.43 \frac{\text{cycles}}{\text{access}} \\
&= 5.43 \frac{\text{cycles}}{\text{access}} \times 0.5 \frac{ns}{\text{cycle}} = 2.72 \frac{ns}{\text{access}}
\end{aligned}$$

2. (**8 points**) After Redstoke raised concerns about the AMAT, the hardware supplier offered a new version of the system that added an L2 unified cache to the memory hierarchy. Redstoke determined through extensive testing that, while running Wine4U, this new hardware has an Average Memory Access Time (AMAT) of 2.75 cycles per access. The access time to this L2 is 20 cycles and there is no overlap between the access to the L2 and the access to memory, in other words, an access to the main memory is only started after the access to the L2 (hit or miss) is completed. What is the local hit rate of this L2?

$$\text{AMAT} = \frac{N + 0.046N \times 20 + X \times 0.046N \times 120}{N + 0.2N}$$

$$
\begin{aligned}
2.75 &= \frac{N + 0.046N \times 20 + X \times 5.52N}{1.2N} \\
2.75 &= \frac{1.0 + 0.92 + 5.52X}{1.2} \\
X &= \frac{2.75 \times 1.2 - 1.92}{5.52} = \frac{1.38}{5.52} = 0.25 \Rightarrow 25\% \text{ local miss rate} \\
\text{hit rate} &= 75\%
\end{aligned}
$$

3. (**5 points**) Assume that in a typical execution Wine4U runs 10000 instructions and that the CPI with a perfect cache is 1.0 clock cycle per instruction. How much faster is the improved hardware with L2 in comparison with the first hardware evaluated that did not have an L2?

   Without memory stalls Wine4U execute in 10000 cycles

$$
\begin{aligned}
\text{stalls}_{\text{no L2}} &= 0.046 \times 10000 \times 120 = 55200 \text{ cycles} \\
\text{Wine4U cycles}_{\text{no L2}} &= 10000 + 55200 = 65200 \text{ cycles} \\
\text{stalls}_{\text{L2}} &= 0.046 \times 10000 \times 20 + 0.046 \times 0.25 \times 10000 \times 120 \\
&= 9200 + 13800 = 23000 \\
\text{Wine4U cycles}_{\text{L2}} &= 10000 + 23000 = 33000 \text{ cycles} \\
\frac{\text{Wine4U cycles}_{\text{no L2}}}{\text{Wine4U cycles}_{\text{L2}}} &= \frac{65200}{33000} = 1.98
\end{aligned}
$$

   The version with L2 is 1.98 times **faster** than the version without L2.

   Given that the basic CPI and the number of accesses is the same, a simpler way to arrive at the same answer is to compute the rate between the AMATs:

$$
\frac{\text{AMAT}_{noL2}}{\text{AMAT}_{L2}} = \frac{5.43}{2.75} = 1.98
$$