Processor Frequency	5 GHz
L1 Instruction Cache access time	1 cycle
L1 Data Cache access time	1 cycle
L2 access time	??
Memory Access Time	175 cycles

Table 1: Execution and Memory Hierarchy Characteristics

Instructions executed	10^6 instructions
Instructions that access data (load or store)	200,000 instructions
Instructions that hit in the L1 Instruction cache	984,000 instructions
Instructions that hit in the L1 Data cache	184,000 instructions
Accesses that hit in the L2 cache	19,200 instructions

Table 2: Hardware-counter measurements for an application

Question 3 (20 points):

Table 1 has information about the CPU execution and the memory hierarchy for a given processor. In this data, the penalty of L2 assumes that the access to L2 is not overlapped with the access to L1. In other words, an access to L2 is only started after one cycle has been spent to determine that it was a miss in L1. Similarly, the time to access main memory will be specified as the time necessary to access main memory after L2 has been accessed to establish that the access is a miss in L2. Table 2 has information obtained from hardware counters while running an important application in this processor.

a. (**10 points**) For the application whose measurements appear in Table 2 running in the processor whose characteristics are in Table 1, assuming that the L2 access time is 25 cycles, what is the Average Memory Access Time (AMAT) expressed in *nano* seconds?

b. (**10 points**) If the Average Memory Access Time (AMAT) for the application whose measurements appear in Table 2, while running in the processor whose characteristics are in Table 1, is 0.64 *nano* seconds, how long does it take to complete an access to the L2 (expressed in *nano* seconds)?