Question 3 (20 points): Consider a two-way set associative cache for a 16-bit address space. The cache has 4 word blocks and 16 entries.

a) **(4 points)** How many bits are used for each of the tag, index and offset?

b) **(4 points)** What is the data capacity of the cache in bits?

c) **(4 points)** How many total bits are required to represent the cache, including tags and data, as well as a Valid bit and a Dirty bit for each cache block and a LRU bit for each cache entry?

d) **(8 points)** In the table below indicate the state of the cache after the following sequence of memory references:

reference type	address
load	0x0730
load	0xA43C
load	0x40B4
load	0x073C
store	0x40B4
load	0x0F3C
load	0x04B0
store	0x04BC

Assume that, prior to the references above, all entries in the cache are invalid, i.e. all the valid bits (V) in the cache are 0, and all the least-recently-used (LRU) bits are equal to 0.

You must indicate the value of the valid bit and the LRU bits for all entries in the cache. For entries that have a valid bit V=1 you must also list the value of the dirty bit (D) and the value of the Tag.

Index	**V**	**D**	**Tag**	**Data**	**LRU**	**V**	**D**	**Tag**	**Data**
0									
1									
2									
3									
4									
5									
6									
7									
8									
9									
10									
11									
12									
13									
14									
15									