CMPUT 229 - Quiz # 2 - Fall 2010

Name: Solution

Question 1 (100 points): The figure below displays the slide used in class to explain the format of a branch-not-equal instruction. The table below lists two branch instructions that were fetched by a processor. It shows the memory address from which the instruction was fetched and the hexadecimal representation of the fetched instruction. For each instruction, indicate the address of the next instruction executed in case of a branch-taken and in case of a branch-not-taken outcome.

Fetching Address	Fetched Instruction	Address of Next Instruction Executed	
		Branch Not Taken	Branch Taken
0x1000 1000	0x1410 01FB	0x1000 1004	0x1000 17F0
0x1000 4FCC	0x16F9 FFFE	0x1000 4FD0	0x1000 4FC8

address	=	0x01FB
after shift	=	0x07EC
after sign extension	=	0x0000 07EC
Original PC	=	0x1000 1000
	+	4
	+	0x0000 07EC
Target Address	=	0x1000 17F0

address	=	0xFFFE
after shift	=	0xFFF8
after sign extension	=	0xFFFF FFF8
Original PC	=	0x1000 4FCC
	+	4
	+	0xFFFF FFF8
Target Address	=	0x1000 4FC8