Question 1 (10 points): The Average Memory Access Time (AMAT) for a program P executing in a given processor is 2.0 clock cycles per access. 25% of the instructions are loads or stores. The access time for both L1 data and L1 instruction caches is 1 clock cycle and these two accesses occur in parallel in case of an instruction that accesses memory. The miss rate for the L1 instruction cache is 1%, the miss rate for the L1 data cache is 5%. The miss penalty for both L1 caches is the same. What is the average penalty, **expressed in number of cycles** for an access that misses in either L1 data or L1 instruction cache?