Question 1 (30 points): During the design of the MIPS architecture, several options were under consideration for the implementation of branch instruction. The discussion was around the issue of how to interpret the 16 bits in the address field of the branch instruction. In all the options considered, the address field contains an amount that is added to the value of PC + 4 to obtain the address of the instruction that is the target of the branch. The following three options were considered:

- **Option 1:** The 16 bit address field is interpreted as a sign-magnitude representation where the bit 15 represents the sign and the bits 0-14 represent the magnitude of the number. Thus, when bit 15 is 1, the processor has to obtain the two-complement negative representation of the magnitude in 32 bits to add to the PC+4
- **Option 2:** The 16 bit address field contains a two-complement number, which is sign-extended to 32 bits before it is added to PC + 4.
- **Option 3:** The 16-bit address field is a two-complement representation that is first shifted left by two and then sign-extended to 32 bits before it is added to PC + 4
 - 1. (15 points) Fill the table below with the address, expressed in hexadecimal, of the instruction that is the target of each branch (the branches are represented by their hexadecimal representation) for each of the options above. Assume that the branch instruction is at address 0x 8000 0000.

Branch instruction	Address of the target of the branch			
	Option 1	Option 2	Option 3	
0x 1674 0008				
0x 1509 8004				

2. (15 points) Recall that all instructions must be at word-aligned addresses (the address of an instruction must be a multiple of 4). Again, assume that the address of a given branch instruction is 0x 8000 0000. In the table below, indicate the lowest and highest possible address for the target of this branch with each of the design options described above. Express the address in hexadecimal notation.

Branch target	Memory Address			
	Option 1	Option 2	Option 3	
Lowest				
Highest				