Question 1 (30 points): For each of the following statements you have three options: (i) leave it blank; (ii) Mark it with **T** to indicate that the statement is true; (iii) Mark it with `F` to indicate that the statement is false. **You lose 3 points for each incorrect answer.** You win 6 points for each correct answer. You don't win or lose any points if you leave the statement blank. Regardless of how many statements you mark wrong, your score in this question cannot be below zero.

a. ( ) In an embedded processor whose design was derived from the MIPS architecture, the address field for a branch instruction is 12 bits. The execution procedure for a branch is the same as in MIPS:

```
bne  $s3, $s4, 8:      PC <-- PC + 4
                       if($1 != $2) then PC <-- PC + (address << 2)
```

The largest distance that a branch can jump backward in this architecture is 2047 instructions.

b. ( ) Assume two cache designs C_A and C_B have the same block size. C_A is a 32 KB 2-way set associative cache and C_B is an 16 KB direct-mapped cache. The length of the tag, measured in the number of bits, is the same in C_A and in C_B.

c. ( ) The following code correctly executes an atomic swap between the value stored in the address specified by `$s1` and the content of register `$s4`:

```
try:          add   $t0, $zero, $s4
              ll    $t1, 0($s1)
              sc    $t1, 0($s1)
              beq   $t0, $zero, try
              add   $s4, $zero, $t1
```

d. ( ) The *sticky bit* is used in floating-point arithmetic to improve the performance of floating-point addition.

e. ( ) Figure 1 depicts the architecture of a 5-stage pipelined implementation of the data path for the MIPS architecture. This drawing is incorrect because the instruction fetched at time T_i will write to the register specified by the instruction fetched at time T_{i+3}.

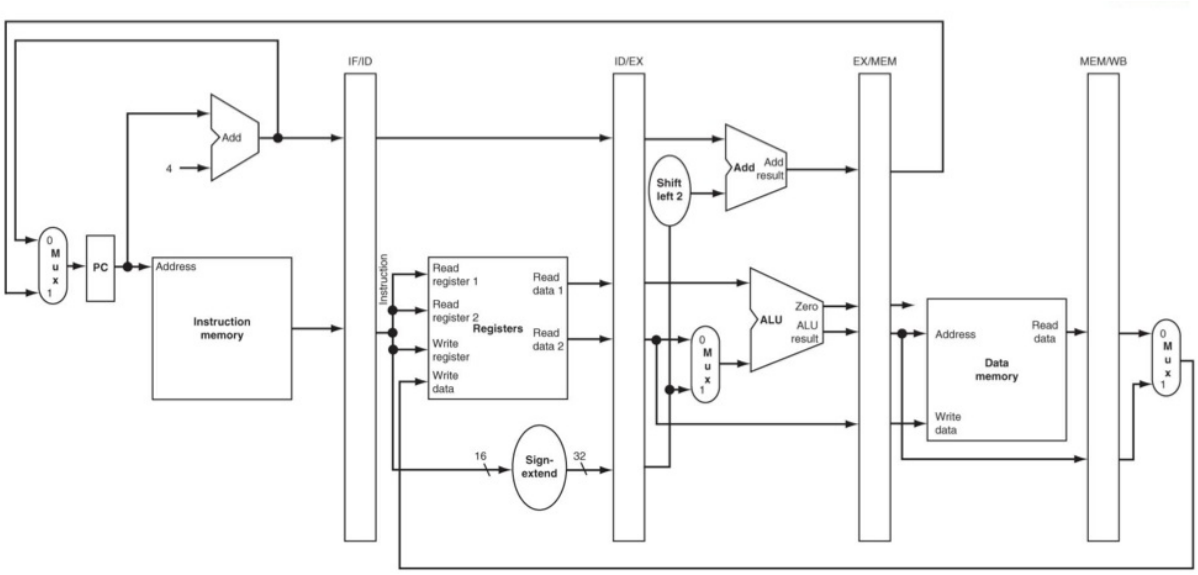

Figure 1: A design for a MIPS pipeline.