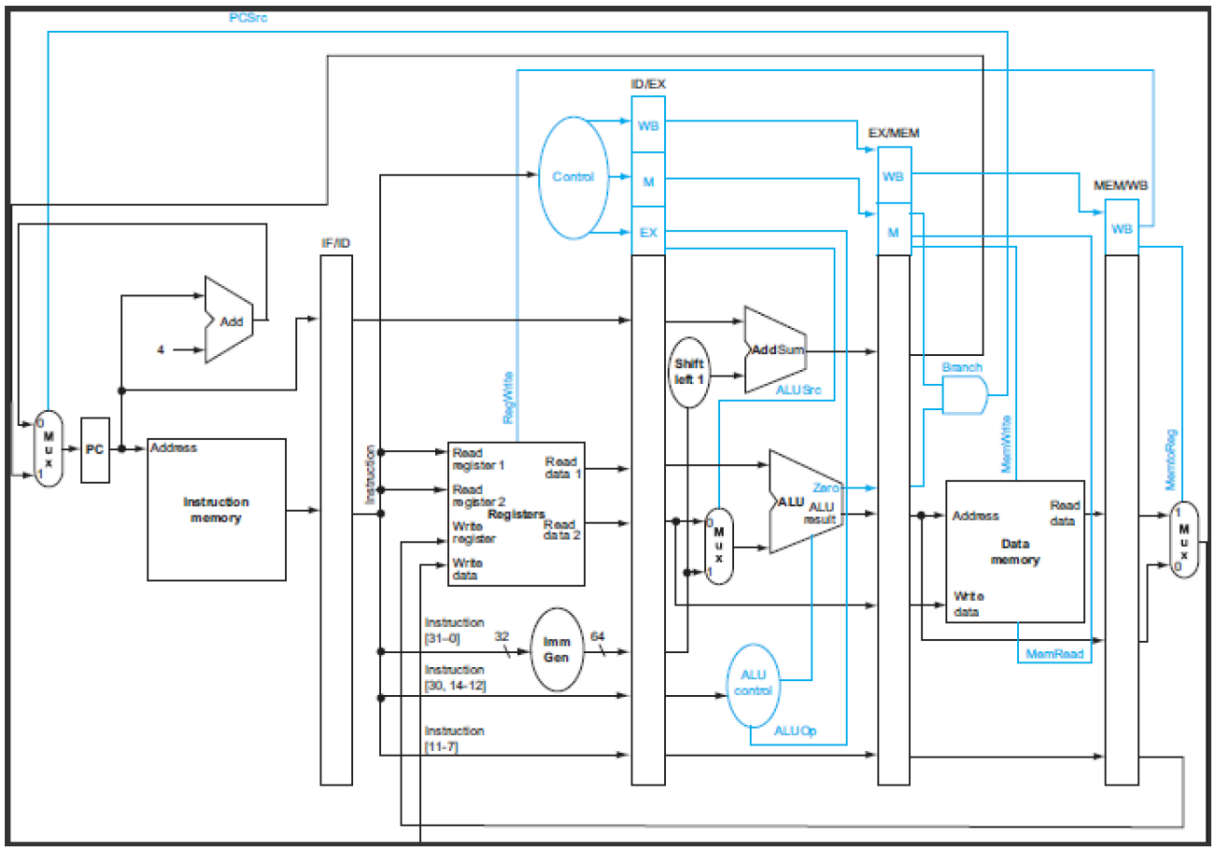

Figure 1: A diagram for a pipelined datapath.

Question 3 (15 points): Figure **??** contains a block diagram for a possible implementation of a five-stage pipeline similar to the one that we studied in class.

Assume that the following sequence of instructions execute in this pipeline:

```
0x000F 4000   lw     t0, 0(s1)
0x000F 4004   add    t1, t2, t3
0x000F 4008   sub    t4, t0, t1
0x000F 400C   sll    t5, t4, 4
0x000F 4010   sw     t0, 0(s5)
0x000F 4014   sra    t5, t5, 5
0x000F 4018   bne    t5, zero, loop
```

1. (**4 points**) During the execution of the sequence of instructions above, is there a need to insert any delay ("bubble") in the pipeline for the correct execution of the instructions? Explain

2. (**4 points**) Consider the clock cycle in which the `lw` instruction is in the write-back stage. Is there any forward that is needed in that clock cycle? If yes, state which forwarding is needed.

3. (**4 points**) Assume that during the execution of this sequence of instructions, the value in `s5` is 0x8000 0007. Would the execution of this sequence generate any exceptions in the pipeline? Explain your answer. If any exception is generated, explain how the exception would be handled in the pipeline. Make sure to specify in which stage of the pipeline exceptions are generated and what will happen with each of the instructions in the sequence.

4. (**3 points**) The `Mux` on the far left side of the Figure **??** has two inputs. The output of that `Mux` is sent to the `PC`. Explain what is the role of these two inputs, There is a third value that may be sent to the `PC`, but this value is not shown in this diagram. When is this third input used?