Question 2 (20 points): A processor with 32-bit addresses uses a 32KB 2-way set associative cache with 16-byte blocks.

a. (**10 points**) In the table below indicate how many bits are used for offset, index, and tag

Field	**Number of bits**
Offset	
Index	
Tag	

b. (**10 points**) Below is a sequence of accesses by the processor to the cache specified above. Assume that all entries in the cache are invalid when the first access occurs. For each access indicate whether it is a hit or a miss.

Address	**Outcome (hit or miss)**
`0x1000 8E38`	
`0x1000 8E3C`	
`0x3CB4 CE30`	
`0x1000 8E30`	
`0x2844 4E34`	
`0x3CB4 CE30`	
`0x1000 8E3C`	