Question 3 (10 points):

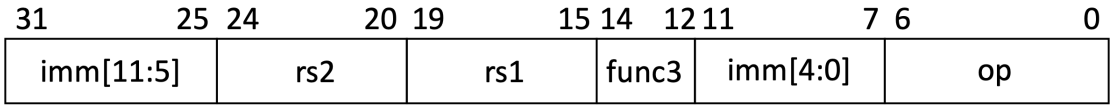

Figure 1: S-Type format. Used for store instructions in RISC-V.

This question explores the binary format of RISC-V instructions. This question will focus on the S-Type format used for the `sw` and for the `sb` instructions. Figure **??** shows the S-Type format. The opcode for both an `sw` and an `sb` instruction is `0100011`. The func3 code for `sb` is 000, while the func3 code for `sw` is `010`. In assembly the `sw` and `sb` instruction is expressed as follows — `(31:0)` indicates that the 32 bits of the register are used and `(7:0)` indicates that the eight least significant bits are used:

```
sw  rs2, imm(rs1)   # Mem[Reg[rs1]+imm](31:0) <- Reg[rs2](31:0)
sb  rs2, imm(rs1)   # Mem[Reg[rs1]+imm](7:0) <- Reg[rs2](7:0)
```

a. (**5 points)** The binary encoding of an instruction fetched from memory is `0xFF142623`. What is the assembly code for this RISC-V instruction?

b. (**5 points)** What is the binary representation, expressed in hexadecimal, for the following assembly instruction?

```
sb t5, 2047(s10)
```