Question 2 (20 points): A processor with 32-bit addresses uses a 32KB 2-way set associative cache with 16-byte blocks.

a. (**10 points**) In the table below indicate how many bits are used for offset, index, and tag

Field	Number of bits
Offset	4
Index	10
Tag	18

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\begin{aligned}
\text{Offset} &= \log_2(16) = 4 \\
\frac{\text{bytes}}{\text{entry}} &= \text{associativity} \times \text{block size} \\
&= 2 \times 16 = 32 \text{ bytes} \qquad (1) \\
\frac{\text{entries}}{\text{cache}} &= \frac{\text{cachesize}}{\frac{\text{bytes}}{\text{entry}}} \\
&= \frac{32KB}{32} = 1KB = 2^{10} \text{ entries} \Rightarrow \text{index} = 10 \text{ bits} \\
\text{tag} &= 32 - \text{index} - \text{Offset} \\
&= 32 - 10 - 4 = 18 \text{ bits}
\end{aligned}
$$

b. (**10 points**) Below is a sequence of accesses by the processor to the cache specified above. Assume that all entries in the cache are invalid when the first access occurs. For each access indicate whether it is a hit or a miss.

Address	Outcome (hit or miss)	Tag	Index	Offset
0x1000 8E38	miss	0x1000_10	00 1110 0011	1000
0x1000 8E3C	hit	0x1000_10	00 1110 0011	1100
0x3CB4 CE30	miss	0x3CB4_11	00 1110 0011	0000
0x1000 8E30	hit	0x1000_10	00 1110 0011	0000
0x2844 4E34	miss	0x2844_01	00 1110 0011	0100
0x3CB4 CE30	miss	0x3CB4_11	00 1110 0011	0000
0x1000 8E3C	miss	0x1000_10	00 1110 0011	1100