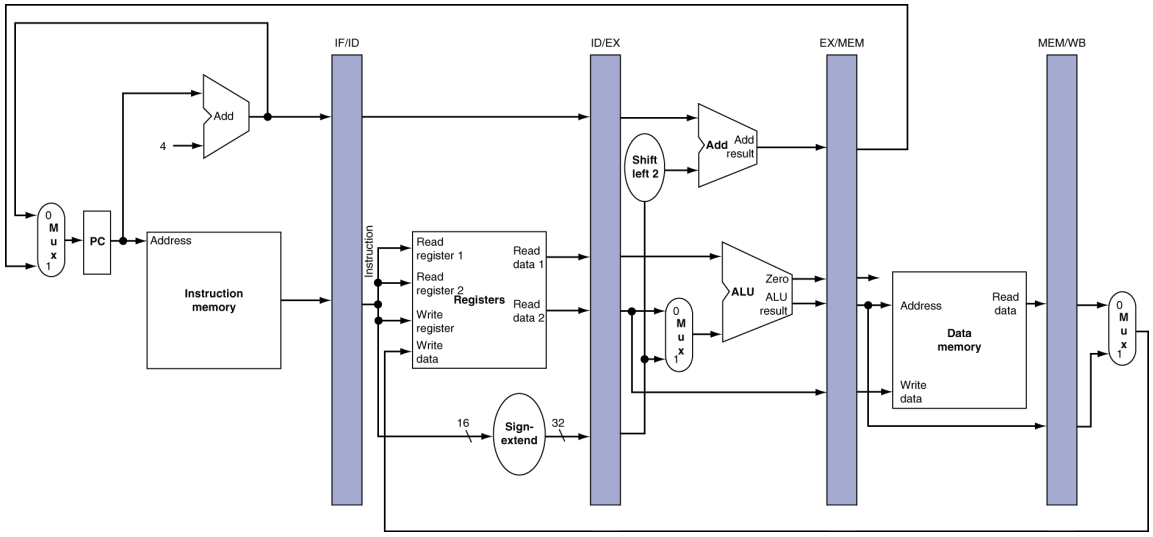


Figure 1: Schematic diagram for a pipelined datapath.

**Question 3 (20 points):**

1. (**7 points)** Figure **??** is a representation of the architecture of a pipelined datapath for a MIPS processor. However, if we were to implement this pipeline as represented in this schematic diagram, the operation of the processor would be incorrect. Explain why it is incorrect and the required change(s) to the datapath schematics to make its operation correct (this question is about the data flow in the datapath, we assume that the control logic, not shown in the schematic, is correctly implemented).

2. (**7 points)** We are writing a MIPS assembly program and we need to load a value from memory and put this value in `$t0`. Then we need to shift this value to the left by 16 bits. Explain why it is a bad idea to place the shift instruction immediately after the load instruction in the assembly program.

3. (**6 points)** What is the role of dirty bits in a memory hierarchy? Which write policy requires a dirty bit?