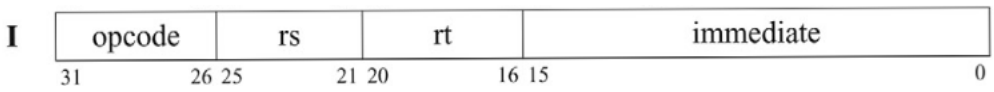
Question 3 (12 points): During the design of the MIPS architecture, several options were under consideration for the implementation of a branch instruction. The discussion was around the issue of how to interpret the 16 bits in the immediate field of the branch instruction. In all the options considered, the immediate field contains an amount that is added to the value of $PC + 4$ to obtain the address of the instruction that is the target of the branch. In all three options listed below the same I-Format is used for the branch instruction:



Option A: The 16-bit immediate field is interpreted as a sign-magnitude representation where the bit 15 represents the sign and the bits 0-14 represent the magnitude of the number (this 15-bit magnitude must be treated as an unsigned int). Thus, when bit 15 is 1, the processor has to obtain the negative representation of the magnitude in 32 bits to add to the $PC + 4$

Option B: The 16-bit immediate field contains a two-complement number, which is sign-extended to 32 bits before it is added to $PC + 4$.

Option C: The 16-bit immediate field is a two-complement representation that is first shifted left by two and then sign-extended to 32 bits before it is added to $PC + 4$

Fill the table below with the address, expressed in hexadecimal, of the instruction that is the target of each branch (the branch instructions are represented by their binary encoding converted to hexadecimal) for each of the options above. Assume that the branch instruction is at address 0x C000 0000.

Branch instruction	**Address of the target of the branch**		
	Option A	**Option B**	**Option C**
`0x 1674 001C`			
`0x 1509 8008`			