

CMPUT 229 - Quiz # 2 - Fall 2010

Name:

Question 1 (100 points): The figure below displays the slide used in class to explain the format of a branch-not-equal instruction. The table below lists two branch instructions that were fetched by a processor. It shows the memory address from which the instruction was fetched and the hexadecimal representation of the fetched instruction. For each instruction, indicate the address of the next instruction executed in case of a branch-taken and in case of a branch-not-taken outcome.

Fetching Address	Fetched Instruction	Address of Next Instruction Executed	
		Branch Not Taken	Branch Taken
0x1000 1000	0x1410 01FB		
0x1000 4FCC	0x16F9 FFFE		

MIPS assembly:

```

0x1000 0000      bne    $s3, $s4, Else    # if i ≠ j goto Else
0x1000 0004      add    $s0, $s1, $s2    # f ← g + h
0x1000 0008      j      Exit              # goto Exit
0x1000 000C      Else:  sub    $s0, $s1, $s2    # f ← g - h
0x1000 0010      Exit:  ...
  
```

R19 = \$s3, R20=\$s4

bne \$s3, \$s4, 8 ⇔ PC ← PC + 4
 if(\$1 ≠ \$2) PC ← PC + 8

OpCode				rs	rt	address			
5				19	20	2			
31	26	25	21	20	16	15	0		
000101				10011		10100		0000 0000 0000 0010	

In memory we would see: 0x16740002

I-Type Instruction Format

Address is sign-extended to 32 bits to allow backward branches.

Internally the processor shifts this constant left by 2 to obtain the distance of 8 bytes required.

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