Question 1 (20 points): Consider a processor with a 2 GHz clock frequency, and separate instruction and data L1 caches. The base CPI with no memory stalls is 1. The instruction cache has a miss rate of 1% and the data cache has a miss rate of 4%. In the program running on this machine, approximately 25% of the instructions are loads and 15% are stores. On a cache miss, the processor must stall for 100 *ns* to complete a memory access.

1. (**6 marks**) What percentage of the total time spent by the program is memory stalls?

2. (**6 marks**) What is the average memory access time (in nanoseconds) for this machine?

3. (**8 marks**) To improve performance, your machine is being redesigned to include an L2 unified cache. The L2 cache has an access time of 10 *ns*, but will reduce the number of accesses to memory to 1% of all L1 accesses. How many times faster is this machine than the one in Part (b)?