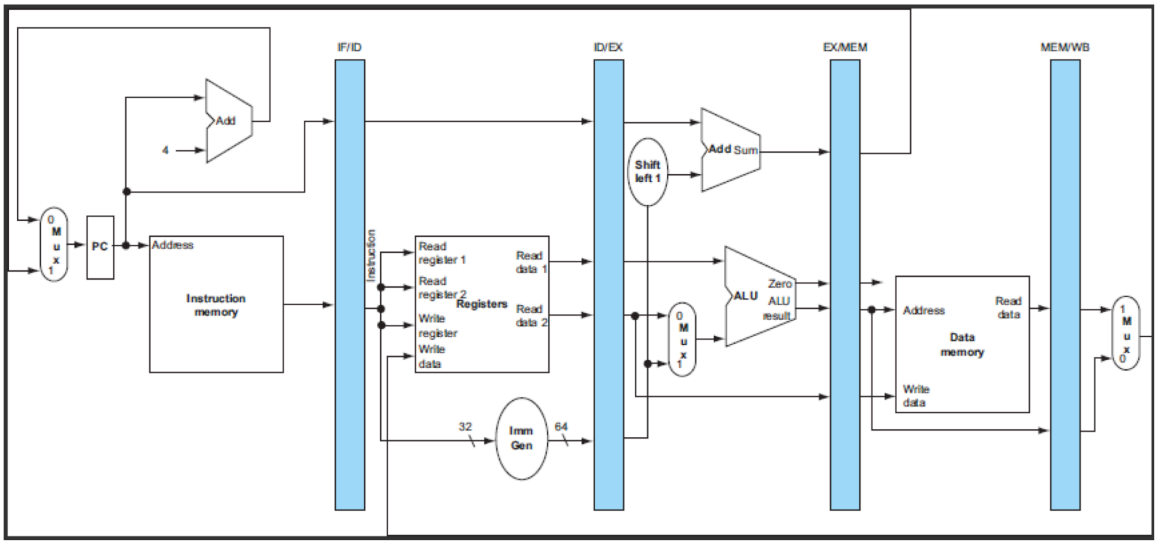

Figure 1: A diagram for a pipelined datapath.

Question 4 (10 points): Figure 1 contains a block diagram for a possible implementation of a five-stage pipeline similar to the one that we studied in class.

1. (**5 points**)As drawn, this datapath would produce incorrect results. Explain what is wrong and what change is required in order for this pipeline to produce correct results?

   The specification of the register to write is coming from the wrong instruction. Must carry the five bits specifying the register to write along the pipeline with the instruction. Thus, the "write register" bits must come from the MEM/WB inter-stage register.

2. (**5 points**) Forwarding is a technique used to prevent delays in the execution in the pipeline. Explain which paths must be added to the datapath shown in Figure 1 to enable forwarding. Will any new muxes or changes to existing muxes be necessary?

   A path from the EX/MEM register to both inputs of the ALU and a path from MEM/WB to both inputs of the ALU. A new mux is needed on the top entry of the ALU and the mux on the bottom entry of the ALU needs to be expanded.