

Question 1: (20 points)

The main competitor of *TinyProc Inc.* is *Sneak Inc.* The latter is trying to increase their market share by offering their latest processor **S75**. Despite using the same Instruction Set Architecture, **S75** is an improvement over **TP500** from *TinyProc Inc.* The most important application in this market is **ControLux**, an application that controls the dashboard of a luxury car. After getting access to **S75**, *TinyProc Inc.* was able to design *TinyComp*, a compiler that generates code that runs on both **TP500** and **S75**. Trying to preserve their market share, *Sneak Inc.* developed their own compiler *SneakComp*, which also generates code that runs on both processors. An independent performance comparison between **TP500** and **S75** reveals that **S75** is twice as fast as **TP500** when running **ControLux**. The *TinyProc Inc.* management is panicking and has asked you, as an Industrial Internship Program (IIP) student with a placement at *TinyProc Inc.*, to investigate what *Sneak Inc.* has done to deliver this performance gain. Here is the information that you have to work with:

- **ControLux** compiled with *SneakComp* runs twice as fast in **S75** compared with **ControLux** compiled with *TinyComp* running on **TP500**.
 - **S75** runs at 750 MHz, while **TP500** runs at 500 MHz.
 - The instructions in the ISA of **TP500** can be divided into three classes according to the number of cycles that each instruction needs to execute: ALU instructions, load/store instructions and branch instructions. When **ControLux** is compiled with *TinyComp*, its instruction mix is 40% ALU, 25% load/stores, and 35% branches.
 - In **TP500**, an ALU instruction requires 1 cycle to execute, a load/store instruction requires 5 cycles, and a branch requires 3 cycles.
 - In **S75**, you were able to measure the number of cycles per instruction for ALU and branch instructions, but not for load/store instructions. On average, it takes 1 cycle to execute an ALU instruction and 3 cycles to execute a branch. To measure the number of cycles per load/store instruction, you ran the **ControLux** code generated by *TinyComp* on the **S75**. You found out that **S75** is 2.025 times faster than **TP500** when executing this code.
- a. (5 points) What is the CPI of **ControLux**, compiled with *TinyComp*, when it runs on **TP500**?
 - b. (5 points) What is the CPI of **ControLux**, compiled with *TinyComp*, when it runs on **S75**?
 - c. (5 points) What is the average number of cycles required to execute load/store instructions when executing the **ControLux** code generated with *TinyComp* on the **S75**?
 - d. (5 points) *TinyProc Inc.* managed to obtain an executable for **ControLux** that was generated by *SneakComp*. Using hardware event counters, you managed to determine that, in the *SneakComp* code, the number of branch instructions and the number of load/store instructions is 20% less than in that generated with *TinyComp*. What is the percentage change in the number of ALU instructions executed

by the *SneakComp* version of **ControLux** in comparison with the code generated with *TinyComp*?