Question 1 (20 points): You've been hired to create instruction formats for MIPS-48, a new version of MIPS that has 48 32-bit registers instead of 32 registers. These registers will be numbered 0 to 47, instead of 0 to 31. Assume that 0-31 are the original MIPS registers and 32-47 are the new registers. Other than the number of registers, MIPS-48 is just like MIPS.

Part A (2 points): How many bits are required to represent a register in a MIPS-48 instruction?

Part B (8 points): MIPS-48 has 32-bit instructions. Assume that the opcode field remains the same, and that for I-type instructions, extra bits needed for the register fields come from the immediate field. What is the highest possible address of the next instruction if the current instruction is `beq` and is at address `0x4000 0000`?

Part C (6 points): Give the hexadecimal representation of the MIPS-48 instruction `beq $s0, $s1, foo`, if that instruction is at `0x4000 0000` and the label `foo` refers to an instruction at address `0x4000 00A8`.

Part D (2 points): How many more registers could be added to MIPS-48 without changing the opcode field or affecting the range of a branch instruction?

Part E (2 points): What would the format for a J-type instruction be in MIPS-48?