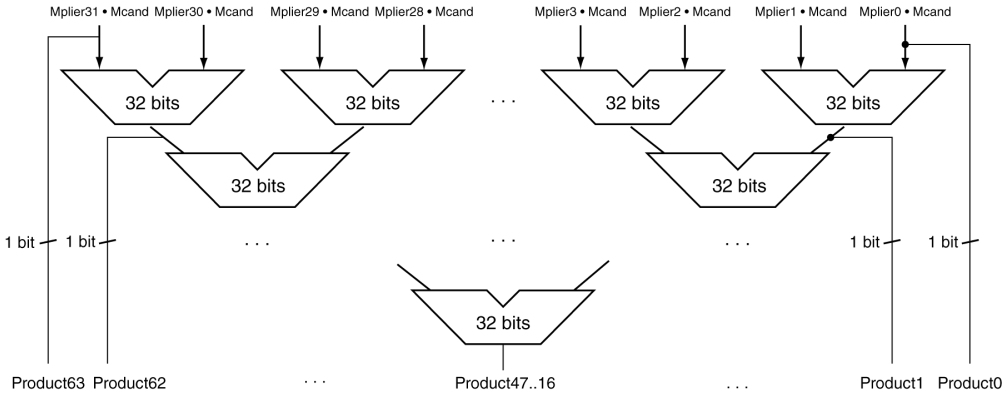

Figure 1: Fast Multiplication Hardware.

►Solution◄

Question 1: (15 points)

Figure 1 shows the design of a fast multiplication hardware that is able to do the multiplication in parallel. Assume that:

- The multiplication of a single bit of the multiplier by the multiplicand to produce the input for one of the adders on the top of the figure takes one clock cycle, but all the 32 single-bit multiplications can be done in parallel.
- Each addition takes one clock cycle to complete.
- All the additions on the same level of the adder tree can be executed in parallel.

Answer the following questions about this circuit:

a. (5 points) The latency of an operation is measured as the number of clock cycles that elapses between the start of the operation and its completion. What is the latency, measured in clock cycles, to complete a 32-bit multiplication (producing a 64-bit result) operation with this circuit?

Solution: latency $= 1 + log_2 32 = 6$ clock cycles

b. (5 points) What is the minimum interval, measured in number of clock cycles, between the completion of two consecutive multiplication operations in this circuit? In other words, how often can you complete a multiplication with this multiplier?

Solution: One cycle.

c. (5 points) How many adders are necessary to implement this circuit?

Solution: # of adders $= 16 + 8 + 4 + 2 + 1 = 31$ adders