►Solution◄

Question 1: (5 points)

Consider that a processor architecture *ToyProc*, which was initially designed as big-endian, is changed to use little-endian byte ordering. Assuming the subset of the MIPS ISA that you are familiar with, and assuming a memory with a word-level interface, give examples of instructions whose operations will be affected by such a change in endianness.

Solution:

The word-size load and store instructions will not be affected by this change, because the memory has a word-level interface. However, the halfword- and byte-sized load and store instructions will be affected. Examples of such instructions are `LH`, `LHU`, `SH`, `LB`, `LBU`, and `SB`.