Question 1 (20 points): A processor operates at a frequency of 4 GHz. It has separate L1 instruction and L1 data caches. It has an unified L2 cache. Both the 64Kb L1 instruction cache and the 32Kb L1 data cache are 2-way set associative and have 64-byte blocks. The 512Kb L2 cache is 4-way set associative and has 256-byte blocks. Both instruction and data L1 cache accesses can be completed in one clock cycle in the case of a hit. An access to the L2 cache requires an additional 10 cycles in case of a hit in the L2. If it results is a miss in the L2, then the access requires an additional 140 cycles for the data to be retrieved from the main memory. In a given program 20% of the instructions are load or store, the hit ratio in the L1 instruction cache is 98.4% and the hit ratio in the L1 data cache is 92%. Moreover, 40% of all the accesses that reach L2 result in misses that must access main memory.

1. (**10 points**) What is the Average Memory Access Time (AMAT), expressed in terms of *nano seconds* (*ns*), for this program in this memory hierarchy?

2. (**10 points**) A design change that may reduce the AMAT is to increase the size of the L2 cache. An engineer claims that she can reduce the AMAT by 25% by changing the size of L2. What is the new local miss ratio of L2?