Question 1 (30 points): You are working in the design team for a computer that has a memory hierarchy with the following characteristics: It has a base average number of clocks per instruction (CPI) of 1.0 (the base CPI is computed assuming that all the memory accesses hit in the first level of cache). This computer operates at the clock frequency of 4.0 GHz (1 GHz = 10^9 Hertz), and has an L1 instruction cache with an access time of 1 cycle and with a hit rate of 99%. It also has an L1 data cache with a hit rate of 92% and an access time of 1 cycle. The design team has determined that in the most important workload for this machine, 25% of the instructions executed are load or store. An access to the main memory requires 25 *nano*seconds (1 $ns = 10^{-9}$ seconds).

a. (**10 points**) What is the effective CPI when the miss rate and the memory access penalty for L1 and D1 are taken into account?

b. (**10 points**) How much faster the machine becomes when an unified L2 cache is added to the design? This L2 cache has a 75% local hit rate, and it has an access time of 5 cycles. The access to the L2 **does not** occur simultaneously to the access to the lower levels of the memory.

c. (**10 points**) The head of the design team wants the CPI to be reduced to 1.5 $\frac{\text{clocks}}{\text{instruction}}$ in order to beat a competing machine that is expected to hit the market at the same time as this design. The design team decides to attempt to achieve this goal by adding an L3 cache to the design — the L2 from part (b) remains in the hierarchy. A preliminary study indicates that the L3 cache will have an access time of 20 cycles and that the access to L3 access **cannot proceed** in parallel with the memory access. What is the minimum L3 hit rate that the team has to achieve in order to reach the CPI goal?