Question 2 (20 points): A new processor, designed to be used in the toy industry, works with a 12-bit address. You need to determine the configuration of a cache after a certain number of memory references by this processor.

The cache that you are studying is a two-way set associative cache with 16-byte blocks and a capacity to store 256 bytes.

a. (**10 points**) How many bits will be used for tag, index, and offset for this cache design?

b. (**10 points**) In the table below indicate the state of the cache after the following sequence of memory references:

```
operation      address
load            0x060
load            0x064
load            0x068
load            0x0A4
store           0x064
load            0x120
```

Assume that before the references above all entries are invalid, *i.e.* all the valid bits (**V**) in the cache are 0. And all the least-recently-used (**LRU**) bits are equal 0.

You must indicate the value of the valid bit and the LRU bits for all entries in the cache. For entries that have a valid bit V=1 you must also list the value of the dirty bit (**D**) and the value of the Tag.

Index	**V**	**D**	**Tag**	**Data**	**LRU**	**V**	**D**	**Tag**	**Data**
0									
1									
2									
3									
4									
5									
6									
7									