Question 1 (15 points): A processor operates with 16-bit addresses. The L1 data cache is two-way set associative with 16-byte blocks. The entire cache is depicted in the table below.

1. (**5 points**) What is the data capacity of this cache expressed in bytes?

```
1  QuickSum:
2      lw      t1, 0(a0)
3      add     t2, t1, a1
4      mv      t4, zero
5  nexItem:
6      lw      t3, 0(t1)
7      add     t4, t4, t3
8      addi    t1, t1, 4
9      ble     t1, t2, nextItem
10     sw      t4, 256(a0)
11     jalr    zero, ra, 0
```

Figure 1: Assembly code for QuickSum.

2. (**5 points**) Assume that before the execution of the function `QuickSum`, shown in Figure **??**:

   - all valid bits are zero and all LRU bits are zero
   - `a0 = 0x0000A850`
   - `a1 = 0x00000020`
   - The word `0x0000B3B0` is at the memory address `0xA850`

   List the memory address of all the accesses, executed by `QuickSum`, that go into the data cache. State if each access results in a hit or a miss in the data cache.

3. (**5 points**) In the table below, indicate the value of the valid, dirty, and Tag fields after the function `QuickSum` is executed. You can leave the Data fields blank. You can also leave the dirty bit and the Tag field blank if nothing is written in these fields for a given block during the execution of this function. You must indicate the value of the valid bit for every block and the value of the LRU bit for every set in the cache.

Index	**V**	**D**	**Tag**	**Data**	**LRU**	**V**	**D**	**Tag**	**Data**
0									
1									
2									
3									
4									
5									
6									
7									