**Question 1 (20 points):** In this question you will demonstrate that you understand how the data stored in caches is organized. Assume that each cache operates in a machine with a 32-bit virtual address.

- (**10 points**) For each of the cache configurations below, indicate how many bits are used for byte offset, for cache index, and for tag.

| Cache capacity | Associativity | Size of Cache Block | Tag Size | Index Size | Byte offset size |
|---|---|---|---|---|---|
| 64 KB | Direct mapped | 128 bytes | | | |
| 32 KB | 2-way | 64 bytes | | | |
| 32 MB | 8-way | 512 bytes | | | |

- **10 points** The table below contains the same cache organizations listed in the table above. Using binary notation, provide the value of the tag and the value of the cache index for a memory reference to the address 0xABCD EF78. Also indicate which word within the block is being accessed. The word at offset 0 is word #0, the word at offset 4 is word #1, etc.

| Cache capacity | Associativity | Cache Block | Tag | Index | word accessed |
|---|---|---|---|---|---|
| 64 KB | Dir. map. | 128 bytes | | | |
| 32 KB | 2-way | 64 bytes | | | |
| 32 MB | 8-way | 512 bytes | | | |