Question 1 (30 points):

1. (**10 points**) Let `i` be an integer value stored in memory at the address given by `$sp+8`. `P` is a vector of 32-bit integers, and `C` is a vector of characters. Assume that the address of `P` is in `$a0` and the address of `C` is in `$a1`. Write the segment of MIPS assembly instructions to execute the following C-language statement:
   ```
   C[P[i]+3] = C[P[i+1]];
   ```
   Use the minimum number of instructions (a solution that uses nine instructions is known).

2. (**5 points**) Assume that `p` is in the memory position given by `$fp-4` and `q` is in the memory position whose address is `$fp-8`. Assume that in this machine addresses have 32 bits, and that `short` is a 16-bit integer. Write MIPS assembly code for the statement in the following segment of C-language code:

   ```
   short *p;
   short *q;
   *p = *(q+1);
   ```

   Use the minimum number of instructions (a solution that uses four instructions is known).

3. (**5 points**) Assume that the jump instruction at address 0xCFFF FFFC has the following binary representation: `0x0800 0CC0`. Which is the address of the target of this instruction?

4. (**10 points**) The Intel Itanium processor is an IA64 architecture processor. When running in this architecture the Microsoft Windows operating system uses a page size of 8KB. The L1 instruction cache can store 16 KB of data, is 4-way set associative and each cache block contains 32 bytes. The Itanium operates with a 64-bit address bus. Assume that a given machine constructed with the Itanium implements 64GB of physical RAM memory. Given an instruction fetch to a specific address in this machine, specify how many bits are used for each of the following elements of the memory hierarchy:

   (a) Virtual Page Number:

   (b) Physical Page Number:

   (c) Virtual Page Offset:

   (d) Physical Page Offset:

   (e) L1 Icache offset:

   (f) L1 Icache index:

   (g) L1 Icache tag: