54162/74162 Fully synchronous Decade Conuter

	Schottky TTL					High-SSpeed TTL					Low-Power Schottky TTL					Standard TTL					Low-Power TTL				
	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF	Device Type	Package C	P	M	CF
T. I.	SN54S162	J①			W①						SN54LS162	J①			W①	SN54162	J①			W①					
	SN74S152	J①	N①								SN74LS162	J①	N①			SN74162	J①	N①							
FAIRCHILD											FM54LS162／FM9LS162	D①			F①	FM93162	D①								
											FC74LS162／FC9LS162	D①	P①		F①	FC74162／FC93162	D①	P①		F①					
MOTOROLA																									
											SN74LS162		P①			MC74162		P①							
N. S. C.											DM54LS162		①			DM54162A									
											DM74LS162		①			DM74162A									
PHILIPS																									
																N74162		①							
SIGNETICS																S54162	F①	B①		W①					
											N74LS162		A①			N74162	F①	B①							
SIEMENS																									
																FLJ421		①							
FUJITSU																									
											74LS162		M①			74162		H①							
HITACHI																									
											HD74LS162		P①			HD74162	①	P①							
MITSUBISHI																									
											M74LS162		P①			M53362		P①							
NEC																									
AMD											Am54LS162														
											Am74LS162														

Electrical Characteristica SN54LS162/SN74LS162

absolute maximum ratings over operating free-air temperature range

Supply voltage, V_{CC}	7 V	Operamng free-air temperature range	SN54LS	−55°C to 125°C
Input voltage	7V		SN74LS	0°C to 70°C
		Storage temperature range		−65°C to 150°C

recommended operating conditi ons

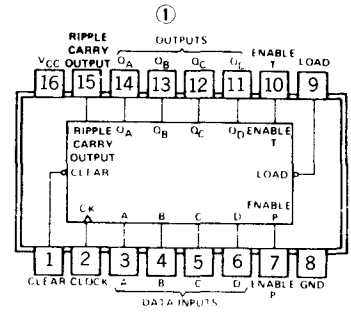
		SN54LS162 MIN	NOM	MAX	SN74LS162 MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				400			400	μA
Low-level output current, I_{OL}				4			8	mA
Input clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{W\ (clock)}$		25			25			n s
Width of clear pulse, $t_{W\ (clear)}$		20			20			n s
Setup time, t_{setup}	Data inputs A, B, C, D	20			20			n s
	Enable P or T	20			20			
	Load	20			20			
	Clear	20			20			
Hold time at any input, t_{hold}		0			0			n s
Operating free-air temperature, T_A		55		125	0		70	°C

electrical characterisics over recommended operating free-air temperature range

PARAMETER*			TESTCONDITIONS†		MIN	TYR‡	MAX	UNIT
V_{IH}	High-level input voltage				2			V
V_{IL}	Low-level input voltage						0.8	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −12mA				−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8V, I_{OH} = −400μA		2.7	3.4		V
V_{OL}	Low-level output votage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8V, I_{OL} = 8mA			0.35	0.5	V
I_I	Input current at maximum input voltage	Load, clock or enable T	V_{CC} MAX, V_I 7V				0.2	mA
		Other input					0.1	
I_{IH}	High-level load input current	Clock or enable T	V_{CC} = MAX, V_I = 2.7V				40	μA
		Other inputs					20	
I_{IL}	Low-level load input current	Clock or enable T	V_{CC} = MAX, V_I = 0.4V				0.8	mA
		Other inputs					0.4	
I_{OS}	Short-circuit output current◆		V_{CC} = MAX		−20		100	mA
I_{CCH}	Supply current, all outputs high		V_{CC} = MAX, See Note 2	SN54LS		18	31	mA
				SN74LS		18	31	
I_{CCL}	Supply current, all outputs low		V_{CC} = MAX, See Note 3	SN54LS		19	32	mA
				SN74LS		19	32	
f_{max}	Maximum Clock frequency				25	32		MHz
t_{PLH}	from Clock to output Ripple carry		V_{CC} = 5V, T_A = 25°C, C_L = 15pF, R_L = 2kΩ, See Note 4			20	35	n s
t_{PHL}						18	35	
t_{PLH}	from Clock (load input high) to output Any Q					13	24	n s
t_{PHL}						18	27	
t_{PLH}	from Clock (load input low) to output Any Q					13	24	n s
t_{PHL}						18	27	
t_{PLH}	from Enable T to output Ripple carry					9	14	n s
t_{PHL}						9	14	
t_{PHL}	from Clear to output Any Q					20	28	n s

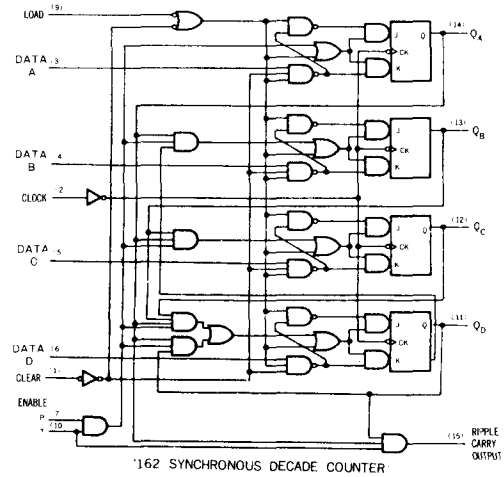
† For conditons shown as MIN or MAX, use the appropriate value specified under recommednd operating conditions.
‡ All typical values are at V_{CC} = 5 V, TA = 25°C
◆ Not more than onne output should be shorted at a time.
* t_{PLH} = propagation delay time, low-to-high-level output
t_{PHL} = propagation delay time, high-to-low-level output

Pin Assignment (Top View)



positive logic:

Funcfional Block Diagram



'162 SYNCHRONOUS DECADE COUNTER

NOTES: 1. This is the voltage between two emitters of a multiple-emitter transistor. For these circuits, this rating applies between the countenable inputs P and T.
2. I_{CCH} is measured with the load int hen agen again with the load input low, with all other inputs high and all outputs open.
3. I_{CCL} is measured with the clock input high, then again with the clock input low, with all othenr inputs low and all outputs open.
4. Propagation delay for clearing is measured fron the clock input transition for the 162.

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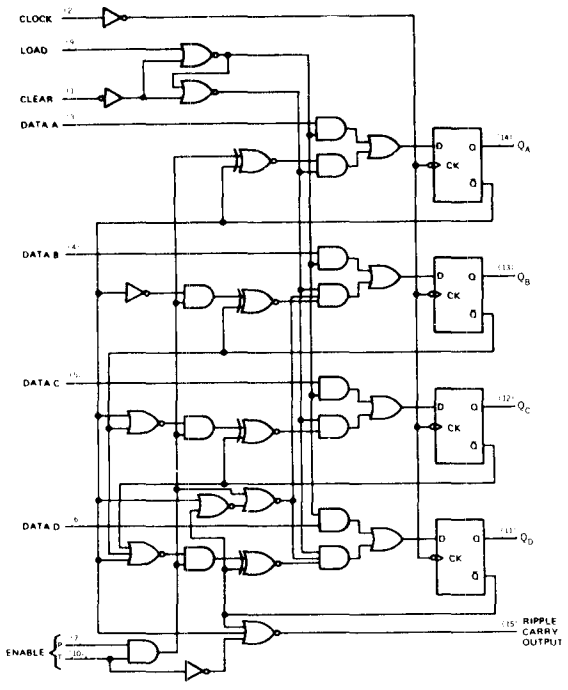
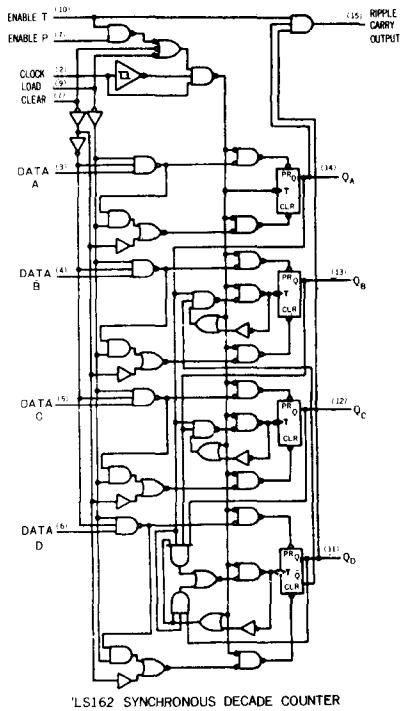
54162/74162(CONTINUED)

Functional Block Diagrams



'S162 SYNCHRONOUS DECADE COUNTER



'LS162 SYNCHRONOUS DECADE COUNTER

typical clear, preset, count, and inhibit sequences

Illustrated below is the following sequence:

1. Clear outputs to zero
2. *Preset to BCD seven*
3. Count to eight, nine, zero, one, two, and three
4. Inhibit