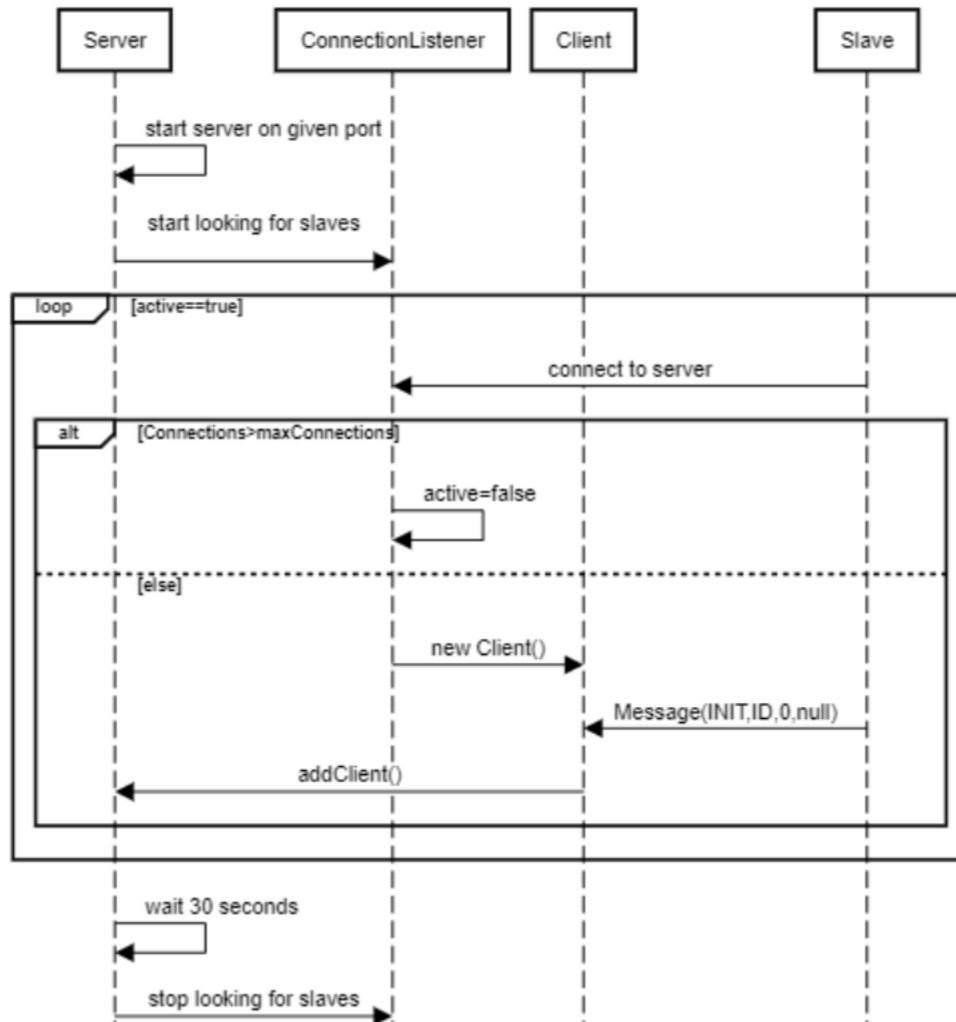


## Master/Slave Init Phase



## Master/Slave Execute/Result Phase

