CECS 225: 8X8 REGISTER FILE

OBJECTIVE: Create an 8x8 Register file.

PROCEDURE: The following files will be needed:

- **flop.v**
- **mux2to1.v**
- **reg8.v**

Create an 8to1 mux in a file named **mux8to1.v** according to the following verilog module definition:

```
module mux8to1(input [7:0] d0,d1,d2,d3,d4,d5,d6,d7,
               input [2:0] s,
               output reg [7:0] y);
  always @(*)
    case(s)
      3'b000:   y = d0;
      3'b001:   y = d1;
      3'b010:   y = d2;
      3'b011:   y = d3;
      3'b100:   y = d4;
      3'b101:   y = d5;
      3'b110:   y = d6;
      3'b111:   y = d7;
      default:  y = 8'bx;
    endcase
endmodule
```

Create a 3to8 decoder in a file named **decoder3to8.v** according to the following Verilog module definition:

```
module decoder3to8(input [2:0] a,
                   output reg [7:0] d);
  always @(*)
    case(a)
      3'b000: d = 8'b0000_0001;
      3'b001: d = 8'b0000_0010;
      3'b010: d = 8'b0000_0100;
      3'b011: d = 8'b0000_1000;
      3'b100: d = 8'b0001_0000;
      3'b101: d = 8'b0010_0000;
      3'b110: d = 8'b0100_0000;
      3'b111: d = 8'b1000_0000;
      default: d = 8'bx;
    endcase
endmodule
```

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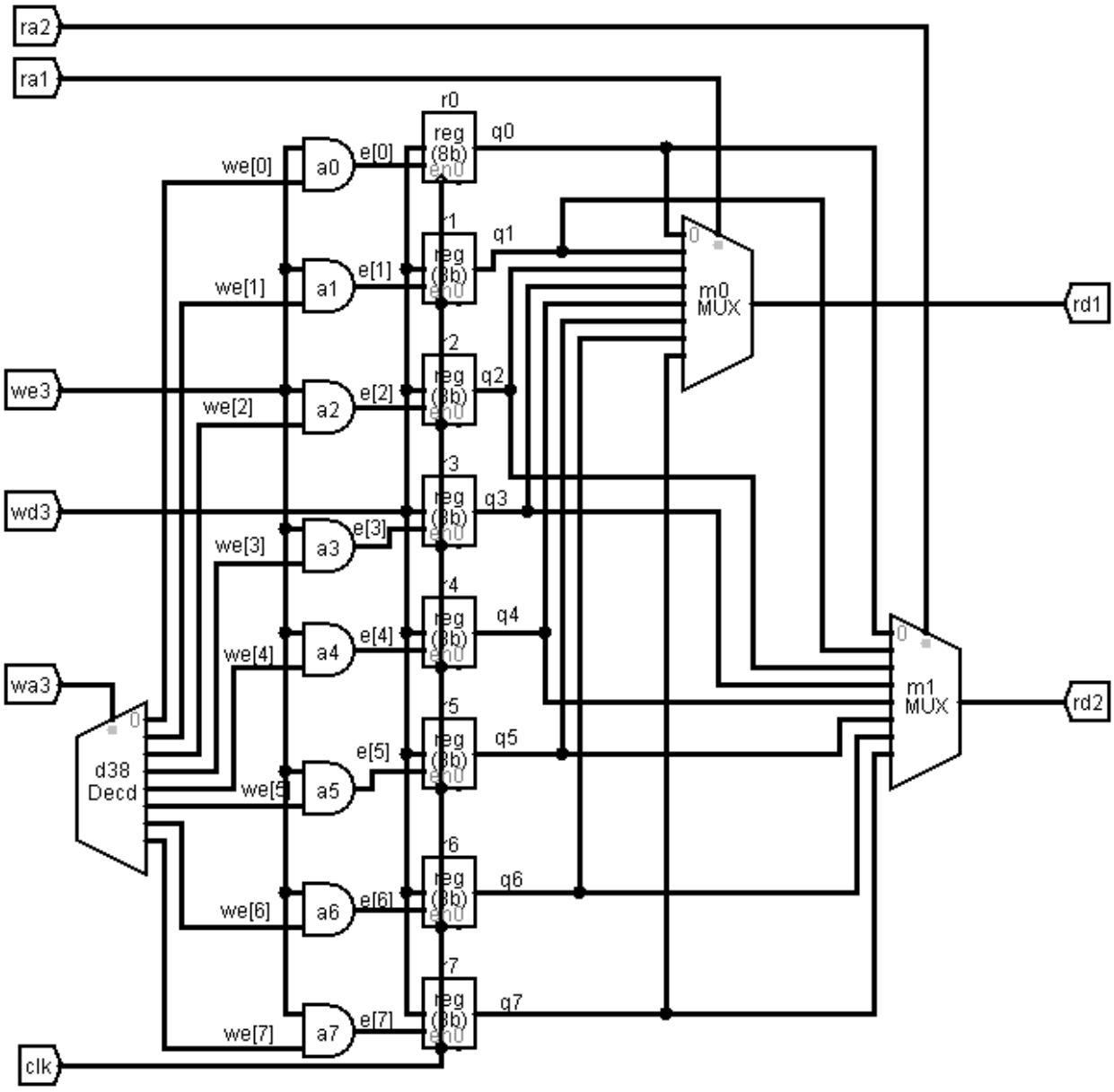
Create the 8x8 Register File according to the following block diagram:



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Use the skeleton code below to get started. Create a file named regfile8x8.v

```
`include "mux8to1.v"
`include "decoder3to8.v"
`include "reg8.v"
module regfile8x8(input clk,
                  input we3,
                  input [2:0] ra1, ra2, wa3,
                  input [7:0] wd3,
                  output [7:0] rd1, rd2);
  wire [7:0] we,e;  //write enable internal wires
  wire [7:0] q0, q1, q2, q3, q4, q5, q6, q7;

  decoder3to8
  d38(wa3,we);

  and
  a0(    , we[0], we3),
  a1(    ,      , we3),
  a2(    ,      , we3),
  a3(    ,      , we3),
  a4(    ,      , we3),
  a5(    ,      ,    ),
  a6(    ,      ,    ),
  a7(e[7],      ,    );

  reg8
  r0(clk, e[0], wd3, q0),
  r1(                ),
  r2(                ),
  r3(                ),
  r4(                ),
  r5(                ),
  r6(                ),
  r7(                );

  mux8to1
  m0(                          ),
  m1(                          );

endmodule
```

Leave the **design.sv** file empty as we will not be using it in this project.

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Source code for testbench.sv is provided below:

```
`include "regfile8x8.v"
module regfiletester;
  reg clk, we3;  reg [2:0] ra1, ra2, wa3;
  reg [7:0] wd3;  wire[7:0] rd1, rd2;
  integer i;
  regfile8x8 uut(clk,we3,ra1,ra2,wa3,wd3,rd1,rd2);
  always #5 clk = ~clk; //clock pulse generation
  initial begin
    clk = 1'b1; we3 = 1'b0;
    $display("Initial register contents");
    register_dump;  we3 = 1'b1;
    for(i = 0; i < 9; i = i + 1)
      begin
        @(negedge clk) wd3 = 16*i; wa3 = i; ra1 = i;
        $display("register %d gets 0x%h",wa3,wd3);
      end
    we3 = 1'b0;
    $display("\nFinal register contents");
    register_dump;
    $finish;
  end
  task register_dump;
    for(i = 0; i < 8; i = i + 2)
      begin
        @(negedge clk)
        ra1 = i; ra2 = i+1;
        @(posedge clk) #1
        $display("register %d contains the value 0x%h",ra1,rd1);
        $display("register %d contains the value 0x%h",ra2,rd2);
      end
  endtask
endmodule
```

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Test results for a properly functioning 8-bit register is shown below:

```
Initial register contents
register 0 contains the value 0xxx
register 1 contains the value 0xxx
register 2 contains the value 0xxx
register 3 contains the value 0xxx
register 4 contains the value 0xxx
register 5 contains the value 0xxx
register 6 contains the value 0xxx
register 7 contains the value 0xxx
register 0 gets 0x00
register 1 gets 0x10
register 2 gets 0x20
register 3 gets 0x30
register 4 gets 0x40
register 5 gets 0x50
register 6 gets 0x60
register 7 gets 0x70
register 0 gets 0x80

Final register contents
register 0 contains the value 0x00
register 1 contains the value 0x10
register 2 contains the value 0x20
register 3 contains the value 0x30
register 4 contains the value 0x40
register 5 contains the value 0x50
register 6 contains the value 0x60
register 7 contains the value 0x70
Done
```

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If your module did not work correctly get assistance from the instructor or a reputable student to troubleshoot your design.

WHAT TO TURN IN: Once the modules in this lab are working correctly:

- Copy the contents of your **regfile8x8.v** module to a file named **regfile8x8.txt**
- upload **regfile8x8.txt** to the beachboard dropbox for **regfile8x8**

NOTE:

Keep the source files from this lab as they will be used in future Labs!