CECS 341 – LAB 3

MIPS Control Unit

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I certify that this submission is my original work

Lab Report: Lab Assignment 3 – MIPS Control Unit

1. Goal: The goal of the MIPS Control Unit Lab Assignment is to use Structural Verilog to stimulate a control unit with the implementation of the main decoder, ALU decoder and the controller.

2. Steps:
    a. Go to edaplayground.com and log in to your account.
    b. Create a new file for ALU decoder and main decoder.
    c. Fill in the skeleton code given into the testbench, decoders, and design.
    d. Identify the ports that are needed to be filled.
    e. Check for errors
    f. Run the code for test cases.

3. Results: In this lab assignment we tested the R-type instructions. The output displays the keywords lw and calls the showsignals() method. After displaying sw, it proceeds to call the method again. The first five lines of output represents the elements from the iterations of the funct_codes. The simulation ends once it has run through all the iterations of the code.

4. Conclusion: In conclusion of this lab, I learned to create a control unit. I learned about the functions of the main decoder and the ALU decoder. I have a better understanding of how the main decoder and the ALU decoder work together to make a MIPS control unit. One of the challenges I faced during this lab was filling in the ports of the design.sv file correctly as the order matters in this case.

5. Notes: The R-Type instruction lw is for load word. The sw instruction is known as store word. The beq R-Type instruction represents branch if equal and the bne stands for branch if not equal.

6. Lab Screenshots:

```
design.sv:5: warning: timescale for controller inherited from another file.
./maindec.v:1: ...: The inherited timescale is here.
Testing R-Type instructions
0000110010
0000110110
0000110000
0000110001
0000110111
lw
1001010010
sw
0101000010
beq (branch taken)
0010000110
beq (branch NOT taken)
0000000110
addi
0001010010
j
0000001010
end simulation
Done
```