Project Report

Project: Displaying Characters using Seven Segment Display

Course Title: CSE 231- Digital Logic Design

Submitted To: Tanjila Farah (TNF)
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Group: 1
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Acknowledgement

First of all, we would like to thank our honorable faculty Tanjila Farah for giving us the opportunity to work on the project titled “Displaying Characters using Seven Segment Display” and encouraging to complete this project properly. On the other hand our lab instructor Shagorika Mukherjee also helped us a lot to do this project.She guided us about implementing circuits and other learning objects.

Our main incentive is to prepare this project according to her guidelines in accordance with her instructions. We have tried our best to frame our work as per her instructions and we believe that we have done an adequate job considering our level of experience and expertise and are able to relate the fundamental things with realistic applications.

We are extremely grateful for the opportunities that she gave us to express our innovative ability.

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Overview:

In this project we print a series of characters in a seven segment display in a certain sequence. Each of the character is displayed one at a time and in interval of 2 seconds. The series of the characters combine the string "**CO-537d**". There is also a control switch and when it is pressed the sequence is displayed skipping the very next character of the currently displayed character. This project has two parts, combinational part and sequential part, and the combinational part selects the segments of the seven segment display to light up for every part of the sequence while the sequential part produce the sequence.

Combinational Part:

Circuit Design:

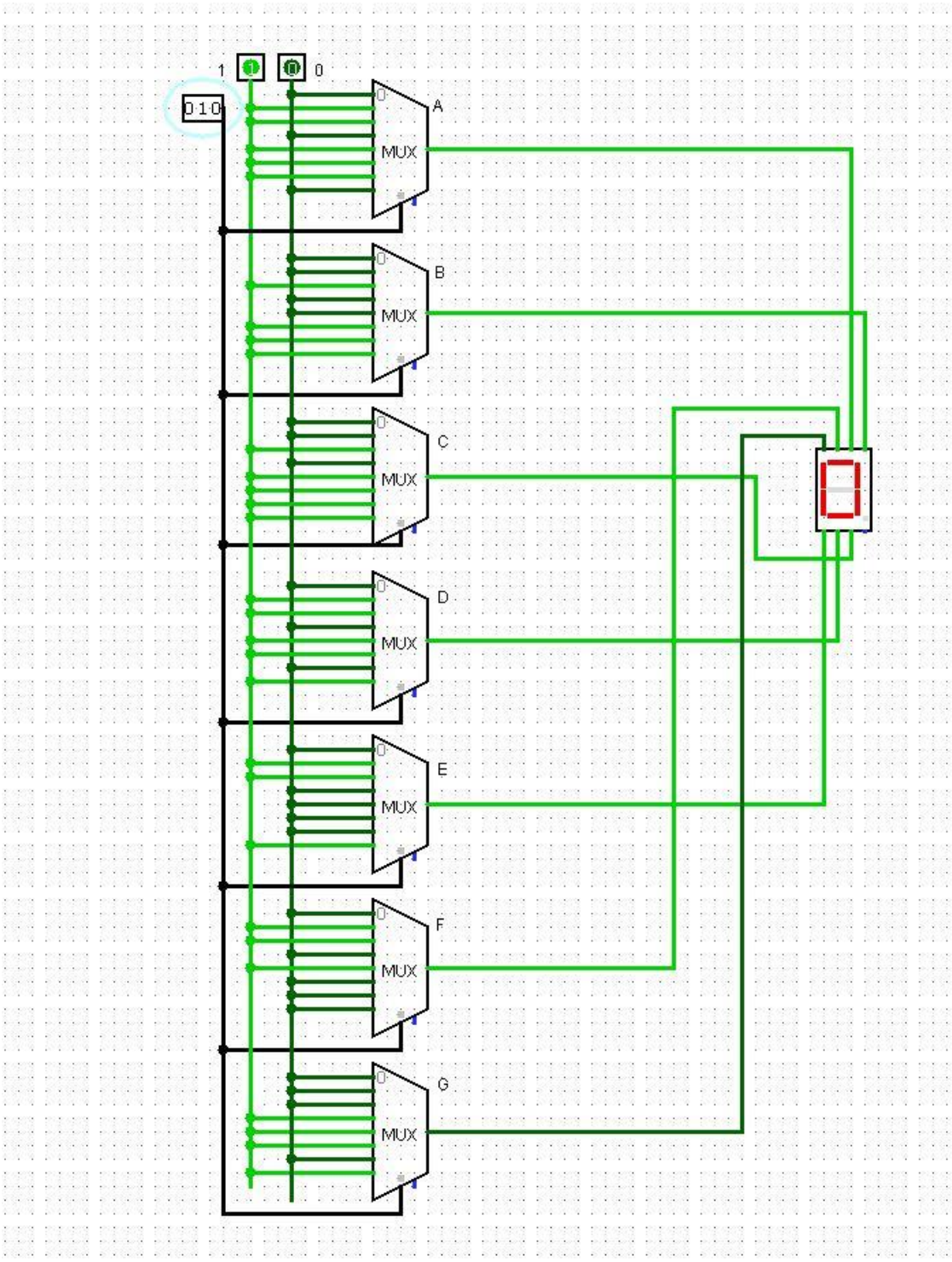
The combinational part of the project determines which segments of the seven segment display will light up for every stage of the sequence. For this part, we first built a truth table with 4 bits input as we had 15 characters to identify the outputs for the each of the segments and dot of the seven segment display. Then we designed the logic circuits from table for the combinational part.

Before implementation we designed four different circuits for this combinational part. We decided not to implement the circuit design with basic gates, universal gate or decoder as implementing with the basic gates and universal gates requires many gates for each of the segment of the display and the decoder requires to use multiple gates with the output from the decoder for each segment and it becomes complex for us to implement. So, we decided to go with the design using multiplexer as it requires only one multiplexer and no basic gates for each segment of the display. From the truth table we identified each of the input for the multiplexers for the out outputs for the seven segment display.

Truth Table for Combinational Part:

INDEX	Character	Inputs			Seven Segment Outputs						
		X	Y	Z	a	b	c	d	e	f	g
0		0	0	0	X	X	X	X	X	X	X
1	C	0	0	1	1	0	0	1	1	1	0
2	[]	0	1	0	1	1	1	1	1	1	0
3	-	0	1	1	0	0	0	0	0	0	1
4	5	1	0	0	1	0	1	1	0	1	1
5	3	1	0	1	1	1	1	1	0	0	1
6	7	1	1	0	1	1	1	0	0	0	0
7	d	1	1	1	0	1	1	1	1	0	1

Figure: Combinational Circuit Diagram:



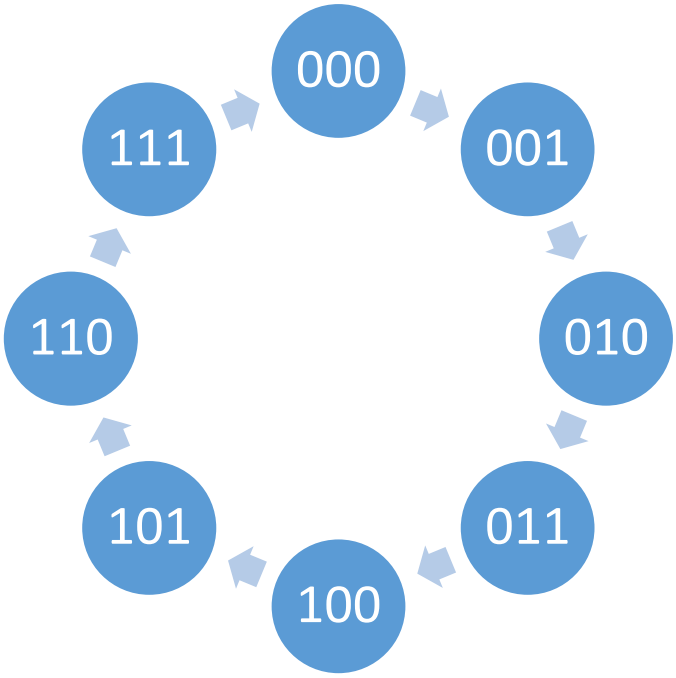
Sequential Part:

Circuit Design:

After we had successfully completed our journey with the combinational part of our project circuit, we worked on the sequential part of our project circuit, to make it so accessible that it is able to work simply on the basis of a clock pulse and a simple input. We first developed our own state table as well as our state diagram so that we could base our project from it.

Being done with the more difficult part of our project, we just hard to decide on using either of the three sorts of flip-flop(T-flipflop, JK-flipflop, D-flipflop) available in the market. We found that using either a T-flipflip or a D-flipflop was an easier alternative than using a JK-flipflop that requires two inputs, and finally all of us had decided to base our project on D-flipflops. We also had to use a clock to make a full-fledged working digital sequential circuit.

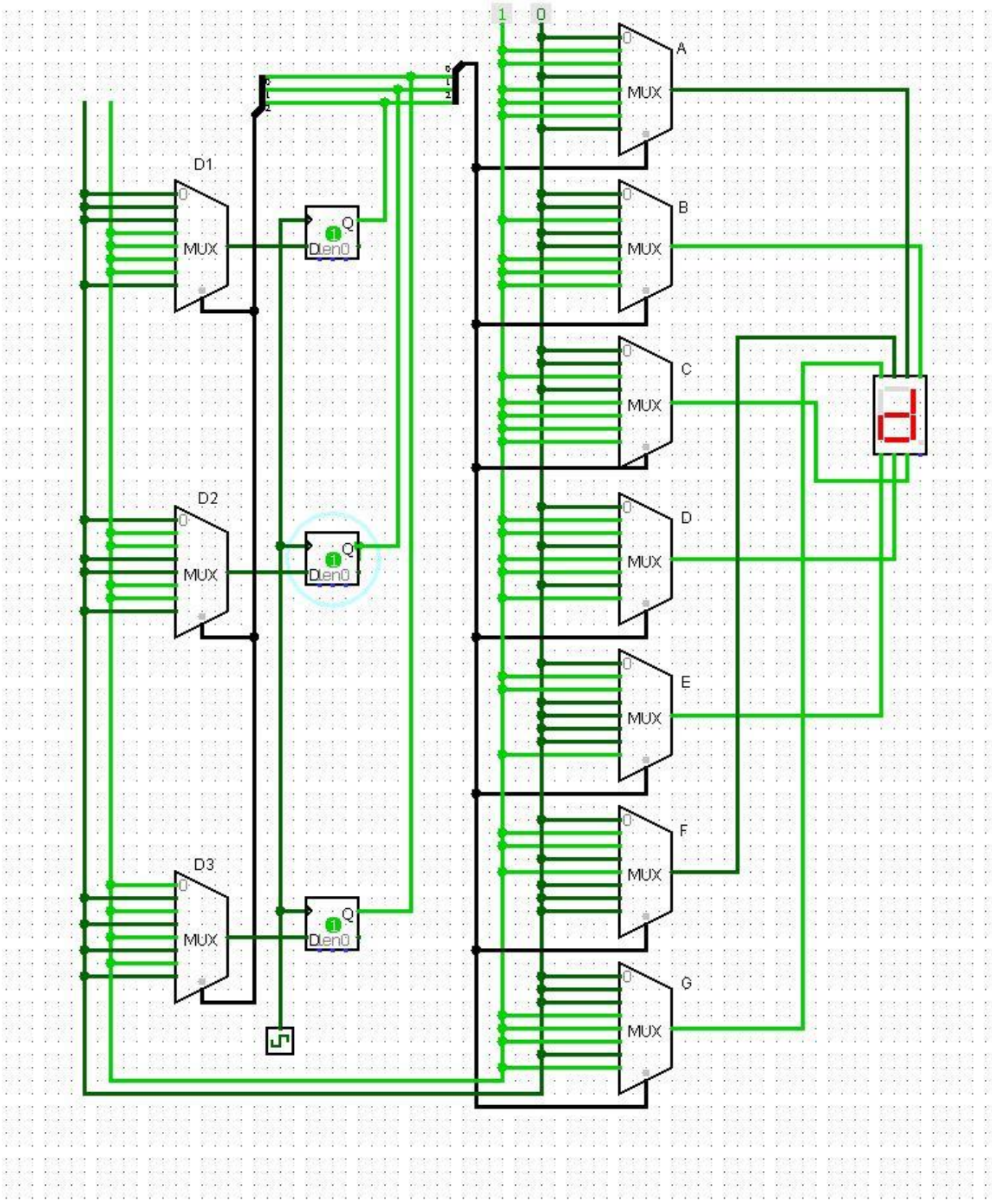
State Diagram:



State Table (Sequential Part):

Present State			Next State			Flip Flops		
x_t	y_t	z_t	x_{t+1}	y_{t+1}	z_{t+1}	D_x	D_y	D_z
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	0
0	1	0	0	1	1	0	1	1
0	1	1	1	0	0	1	0	0
1	0	0	1	0	1	1	0	1
1	0	1	1	1	0	1	1	0
1	1	0	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

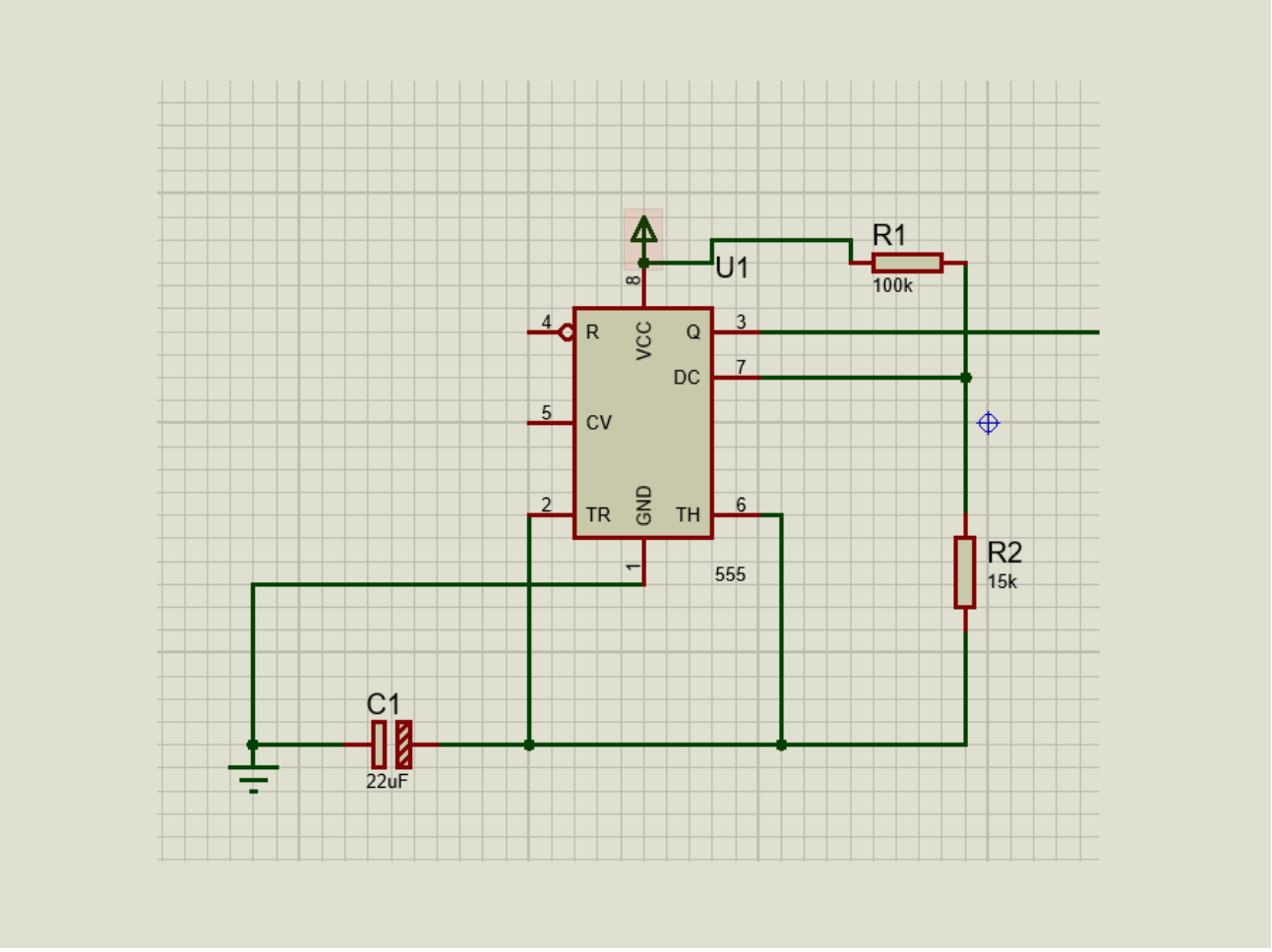
Figure: Sequential Circuit Diagram:



Implementation:

Our implementation of the given project was a very simple one. As stated before, preliminarily our project was implemented on a few multiplexers, three switches for input, as well as resistors. In this second part of our project, our implementation was on constricting the entire work of this project based solely on flip-flops. Simply stated, the only further implementation that took place was on using the D-flipflops to shorten the input. We build a timer clock to auto generate the clock which generates pulse after every 2 seconds.

Diagram of Timer Clock:



Apparatus and Cost:

Apparatus	Quantity	Cost(BDT)
74151 IC 8:1 Multiplexer	11	220
7474 IC Dual D flip flop	2	036
555 IC Timer	1	010
Capacitor	1	002
Resistor	3	003
Seven Segment Display	1	020
Breadboard	3	240
Wires		040
	Total	571

Conclusion:

We have utilized what we have learned from both the course lecturer as well as the lab instructor to equip ourselves with both theoretical knowledge as well as practical knowledge to build forth our circuit. In doing the project, our members stood as a well knit team to bring the project under a successful conclusion, we had taken the help of the internet, as well as many course related books to have a sharp and defined knowledge of what we were going to accomplish. In our search we had found many ways that could help us to both shorten our circuit and our time, not to mention our monetary situation. Thus, in conclusion, the lecturer, the instructor as well as the books have helped us to shape our knowledge of the processes of digital logic enough to implement it in our project.