TCA9539 Low Voltage 16-Bit I²C and SMBus Low-Power I/O Expander with Interrupt Output, Reset pin, and Configuration Registers

1 Features

- I²C to Parallel Port Expander
- Low Standby-Current Consumption of 3 µA Max
- Open-Drain Active-Low Interrupt Output
- Active-Low Reset Input
- 5-V Tolerant I/O Ports
- Compatible With Most Microcontrollers
- 400-kHz Fast I²C Bus
- Input/Output Configuration Register
- Polarity Inversion Register
- Internal Power-on Reset
- No Glitch on Power Up
- Noise Filter on SCL/SDA Inputs
- Address by Two Hardware Address Pins for Use of up to Four Devices
- Latched Outputs With High-Current Drive Capability for Directly Driving LEDs
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 1000-V Charged-Device Model (C101)

2 Applications

- Servers
- Routers (Telecom Switching Equipment)
- Personal Computers, smartphones
- Industrial Automation
- Automotive infotainment, Advanced Driver Assistance Systems (ADAS)
- I²C GPIO Expansion

3 Description

The TCA9539 is a 24-pin device that provides 16 bits of general purpose parallel input/output (I/O) expansion for the two-line bidirectional I²C bus (or SMBus protocol). The device can operate with a power supply voltage (V_{CC}) range from 1.65 V to 5.5 V. The device supports 100-kHz (I²C Standard mode) and 400-kHz (I²C Fast mode) clock frequencies. I/O expanders such as the TCA9539 provide a simple solution when additional I/Os are needed for switches, sensors, push-buttons, LEDs, fans, and other similar devices.

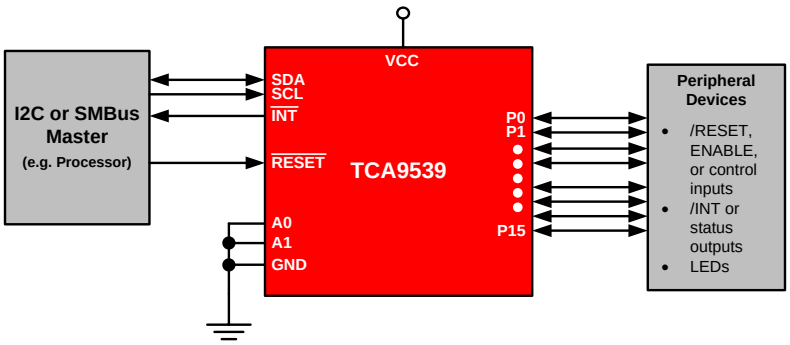
The features of the TCA9539 include an interrupt that is generated on the $\overline{INT}$ pin whenever an input port changes state. The A0 and A1 hardware selectable address pins allow up to four TCA9539 devices on the same I²C bus. The device can be reset to its default state by cycling the power supply and causing a power-on-reset. Also, the TCA9539 has a hardware $\overline{RESET}$ pin that can be used to reset the device to its default state.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TCA9539	TSSOP (24)	7.80 mm × 4.40 mm
	WQFN (24)	4.00 mm × 4.00 mm
	VQFN (24)	4.00 mm × 4.00 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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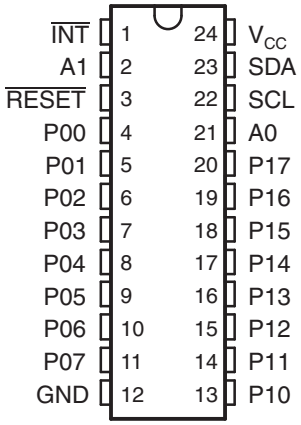
4 Revision History

Changes from Revision A (September 2009) to Revision B **Page**

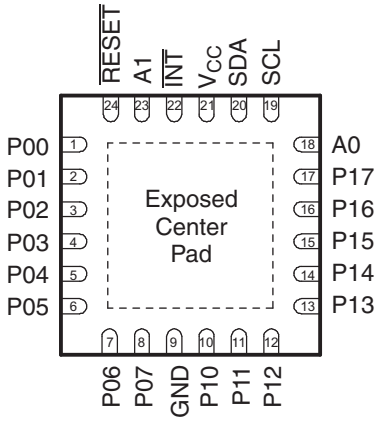
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1
- Added RGE package. ... 1
- Added Thermal Information table ... 5
- Added "Time to reset; VCC = 1.65 - 2.3 V" parameter to RESET Timing Requirements table. ... 7
- Added "Output data valid; VCC = 1.65 - 2.3 V" to Switching Characteristics table. ... 7

5 Pin Configuration and Functions

PW Package
24-Pins TSSOP
Top View



RTW, RGE Package
24-Pins WQFN, VQFN
Top View



Pin Functions

NAME	NO.		I/O	DESCRIPTION
	TSSOP (PW)	QFN (RTW, RGE)		
$\overline{INT}$	1	22	O	Interrupt open-drain output. Connect to V_{CC} through a pullup resistor.
A1	2	23	I	Address input. Connect directly to V_{CC} or ground.
$\overline{RESET}$	3	24	I	Active-low reset input. Connect to V_{CC} through a pullup resistor if no active connection is used.
P00	4	1	I/O	P-port input/output. Push-pull design structure. At power on, P00 is configured as an input.
P01	5	2	I/O	P-port input/output. Push-pull design structure. At power on, P01 is configured as an input.
P02	6	3	I/O	P-port input/output. Push-pull design structure. At power on, P02 is configured as an input.
P03	7	4	I/O	P-port input/output. Push-pull design structure. At power on, P03 is configured as an input.
P04	8	5	I/O	P-port input/output. Push-pull design structure. At power on, P04 is configured as an input.
P05	9	6	I/O	P-port input/output. Push-pull design structure. At power on, P05 is configured as an input.
P06	10	7	I/O	P-port input/output. Push-pull design structure. At power on, P06 is configured as an input.
P07	11	8	I/O	P-port input/output. Push-pull design structure. At power on, P07 is configured as an input.
GND	12	9	—	Ground
P10	13	10	I/O	P-port input/output. Push-pull design structure. At power on, P10 is configured as an input.
P11	14	11	I/O	P-port input/output. Push-pull design structure. At power on, P11 is configured as an input.
P12	15	12	I/O	P-port input/output. Push-pull design structure. At power on, P12 is configured as an input.
P13	16	13	I/O	P-port input/output. Push-pull design structure. At power on, P13 is configured as an input.
P14	17	14	I/O	P-port input/output. Push-pull design structure. At power on, P14 is configured as an input.

Pin Functions (continued)

NAME	NO.		I/O	DESCRIPTION
	TSSOP (PW)	QFN (RTW, RGE)		
P15	18	15	I/O	P-port input/output. Push-pull design structure. At power on, P15 is configured as an input.
P16	19	16	I/O	P-port input/output. Push-pull design structure. At power on, P16 is configured as an input.
P17	20	17	I/O	P-port input/output. Push-pull design structure. At power on, P17 is configured as an input.
A0	21	18	I	Address input. Connect directly to V_{CC} or ground.
SCL	22	19	I	Serial clock bus. Connect to V_{CC} through a pullup resistor.
SDA	23	20	I/O	Serial data bus. Connect to V_{CC} through a pullup resistor.
V_{CC}	24	21	—	Supply voltage

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		–0.5	6	V
V_I	Input voltage range (2)		–0.5	6	V
V_O	Output voltage range (2)		–0.5	6	V
I_{IK}	Input clamp current	$V_I < 0$		–20	mA
I_{OK}	Output clamp current	$V_O < 0$		–20	mA
I_{IOK}	Input/output clamp current	$V_O < 0$ or $V_O > V_{CC}$		±20	mA
I_{OL}	Continuous output low current	$V_O = 0$ to V_{CC}		50	mA
I_{OH}	Continuous output high current	$V_O = 0$ to V_{CC}		–50	mA
I_{CC}	Continuous current through GND			–250	mA
	Continuous current through V_{CC}			160	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions.

6.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		1.65	5.5	V
V_{IH}	High-level input voltage	SCL, SDA	0.7 × V_{CC}	V_{CC} (1)	V
		A0, A1, $\overline{RESET}$, P07–P00, P10–P17	0.7 × V_{CC}	5.5	
V_{IL}	Low-level input voltage	SCL, SDA	–0.5	0.3 × V_{CC}	V
		A0, A1, $\overline{RESET}$, P07–P00, P10–P17	–0.5	0.3 × V_{CC}	
I_{OH}	High-level output current	P07–P00, P17–P10		–10	mA
I_{OL}	Low-level output current	P07–P00, P17–P10		25	mA
T_A	Operating free-air temperature		–40	85	°C

(1) The SCL and SDA pins shall not be at a higher potential than the supply voltage V_{CC} in the application, or an increase in supply current, I_{CC}, will result

6.4 Thermal Information

THERMAL METRIC (1)		TCA9539			UNIT
		PW (TSSOP)	RTW (WQFN)	RGE (VQFN)	
		24 PINS	24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	108.8	43.6	48.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	54.0	46.2	58.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	62.8	22.1	27.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.1	1.5	3.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.3	22.2	27.2	°C/W
$R_{\theta JC(bottom)}$	Junction-to-case (bottom) thermal resistance	—	10.7	15.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP (1)	MAX	UNIT
V_{IK}	Input diode clamp voltage	I_I = –18 mA	1.65 V to 5.5V	–1.2			V
V_{PORR}	Power-on reset voltage, VCC rising	V_I = V_{CC} or GND, I_O = 0	1.65 V to 5.5 V		1.2	1.5	V
V_{PORF}	Power-on reset voltage, VCC falling		1.65 V to 5.5 V	0.75	1		
V_{OH}	P-port high-level output voltage (2)	I_{OH} = –8 mA	1.65 V	1.2			V
			2.3 V	1.8			
			3 V	2.6			
			4.75 V	4.1			
		I_{OH} = –10 mA	1.65 V	1.0			
			2.3 V	1.7			
			3 V	2.5			
			4.75 V	4			
I_{OL}	SDA	V_{OL} = 0.4 V	1.65 V to 5.5 V	3			mA
	P port (3)	V_{OL} = 0.5 V	1.65 V	8	10		
			2.3 V	8	13		
			3 V	8	15		
			4.5 V	8	17		
		V_{OL} = 0.7 V	1.65 V	10	14		
			2.3 V	10	17		
			3 V	10	20		
			4.5 V	10	24		
	$\overline{INT}$	V_{OL} = 0.4 V		3			
I_I	SCL, SDA	V_I = V_{CC} or GND	1.65 V to 5.5 V			±1	µA
	A0, A1, $\overline{RESET}$					±1	
I_{IH}	P port	V_I = V_{CC}	1.65 V to 5.5 V			1	µA
I_{IL}	P port	V_I = GND	1.65 V to 5.5 V			–1	µA
I_{CC}	Operating mode	V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{SCL} = 400 kHz, No load	5.5 V		100	200	µA
			3.6 V		30	75	
			2.7 V		20	50	
			1.95 V		10	45	
	Standby mode	V_I = V_{CC} or GND, I_O = 0, I/O = inputs, f_{SCL} = 0 kHz, No load	5.5 V		1.9	3.5	
			3.6 V		1.1	1.8	
			2.7 V		1.0	1.6	
			1.95 V		0.4	1.0	
ΔI_{CC}	Additional current in standby mode	One input at V_{CC} – 0.6 V, Other inputs at V_{CC} or GND	1.65 V to 5.5 V			70	µA
C_i	SCL	V_I = V_{CC} or GND	1.65 V to 5.5 V		3	8	pF
C_{io}	SDA	V_{IO} = V_{CC} or GND	1.65 V to 5.5 V		3	7	pF
	P port				3.7	9.5	

(1) All typical values are at nominal supply voltage (1.8-V, 2.5-V, 3.3-V, or 5-V V_{CC}) and T_A = 25°C.
(2) Each I/O must be externally limited to a maximum of 25 mA, and each octal (P07–P00 and P17–P10) must be limited to a maximum current of 100 mA, for a device total of 200 mA.
(3) The total current sourced by all I/Os must be limited to 160 mA (80 mA for P07–P00 and 80 mA for P17–P10).

6.6 I²C Interface Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 18)

			STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
			MIN	MAX	MIN	MAX	
f_{scl}	I²C clock frequency		0	100	0	400	kHz
t_{sch}	I²C clock high time		4		0.6		µs
t_{scl}	I²C clock low time		4.7		1.3		µs
t_{sp}	I²C spike time			50		50	ns
t_{sds}	I²C serial-data setup time		250		100		ns
t_{sdh}	I²C serial-data hold time		0		0		ns
t_{icr}	I²C input rise time			1000	20	300	ns
t_{icf}	I²C input fall time			300	20 × (V_{DD} / 5.5 V)	300	ns
t_{ocf}	I²C output fall time	10-pF to 400-pF bus		300	20 × (V_{DD} / 5.5 V)	300	ns
t_{buf}	I²C bus free time between Stop and Start		4.7		1.3		µs
t_{sts}	I²C Start or repeated Start condition setup		4.7		0.6		µs
t_{sth}	I²C Start or repeated Start condition hold		4		0.6		µs
t_{sps}	I²C Stop condition setup		4		0.6		µs
$t_{vd(data)}$	Valid data time	SCL low to SDA output valid		3.45		0.9	µs
$t_{vd(ack)}$	Valid data time of ACK condition	ACK signal from SCL low to SDA (out) low		3.45		0.9	µs
C_b	I²C bus capacitive load			400		400	pF

6.7 $\overline{\text{RESET}}$ Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 21)

		MIN	MAX	UNIT
t_W	Reset pulse duration	6		ns
t_{REC}	Reset recovery time	0		ns
t_{RESET}	Time to reset; For V_{CC} = 2.3 - 5.5 V	400		ns
	Time to reset; For V_{CC} = 1.65 - 2.3 V	550		ns

6.8 Switching Characteristics

over recommended operating free-air temperature range, C_L ≤ 100 pF (unless otherwise noted) (see Figure 19 and Figure 20)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{iv}	Interrupt valid time	P port	$\overline{\text{INT}}$		4	µs
t_{ir}	Interrupt reset delay time	SCL	$\overline{\text{INT}}$		4	µs
t_{pv}	Output data valid; For V_{CC} = 2.3 - 5.5 V	SCL	P port		200	ns
	Output data valid; For V_{CC} = 1.65 - 2.3 V				300	ns
t_{ps}	Input data setup time	P port	SCL	150		ns
t_{ph}	Input data hold time	P port	SCL	1		µs

6.9 Typical Characteristics

T_A = 25°C (unless otherwise noted)

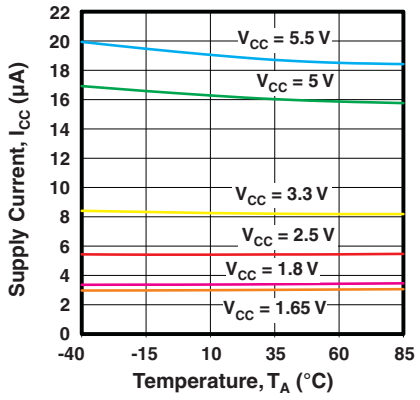


Figure 1. Supply Current vs Temperature

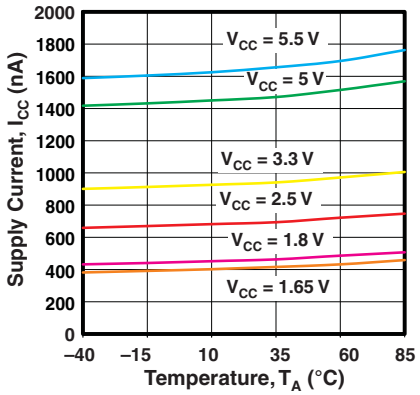


Figure 2. Standby Supply Current vs Temperature

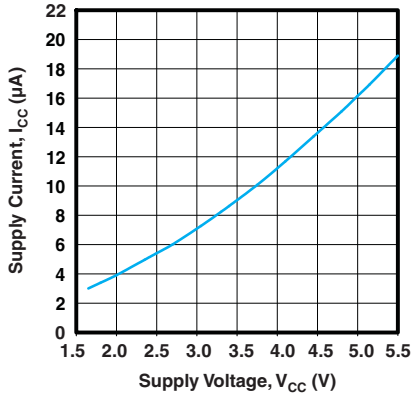


Figure 3. Supply Current vs Supply Voltage

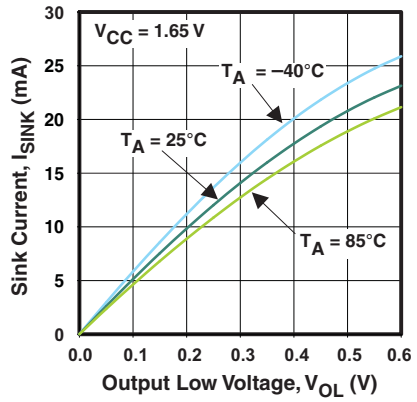


Figure 4. I/O Sink Current vs Output Low Voltage

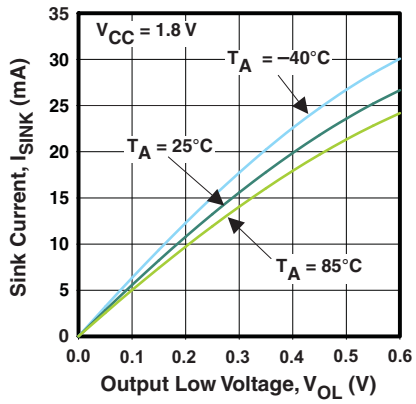


Figure 5. I/O Sink Current vs Output Low Voltage

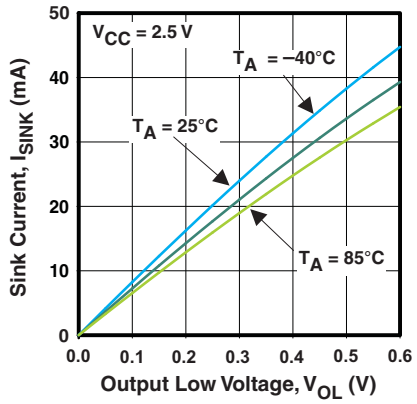


Figure 6. I/O Sink Current vs Output Low Voltage

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

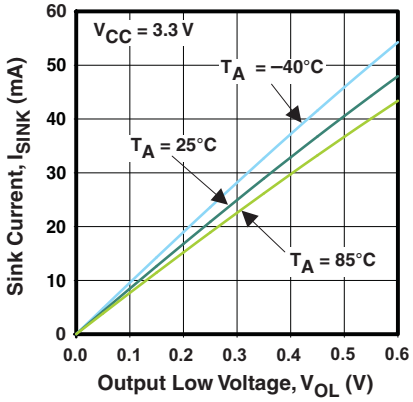


Figure 7. I/O Sink Current vs Output Low Voltage

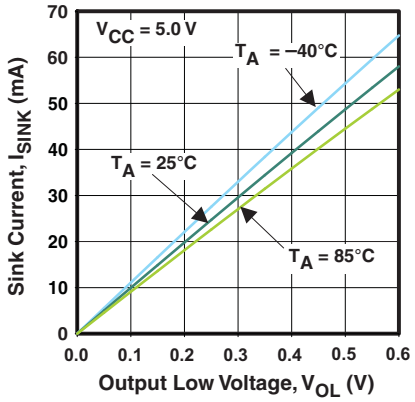


Figure 8. I/O Sink Current vs Output Low Voltage

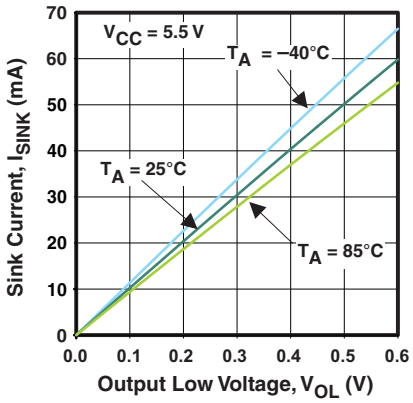


Figure 9. I/O Sink Current vs Output Low Voltage

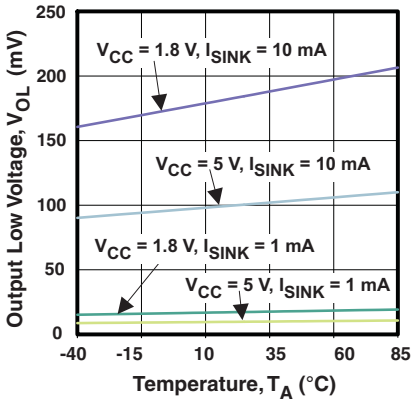


Figure 10. I/O Low Voltage vs Temperature

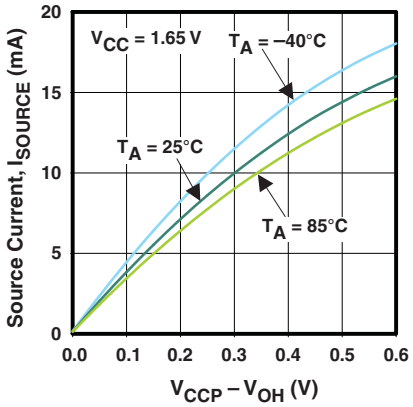


Figure 11. I/O Source Current vs Output High Voltage

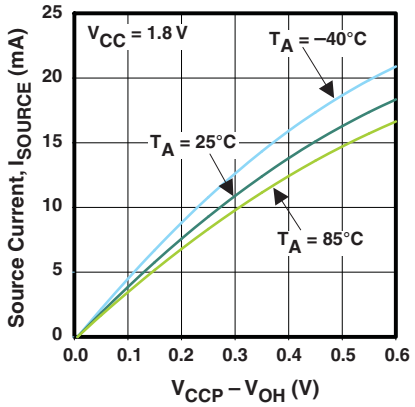


Figure 12. I/O Source Current vs Output High Voltage

Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

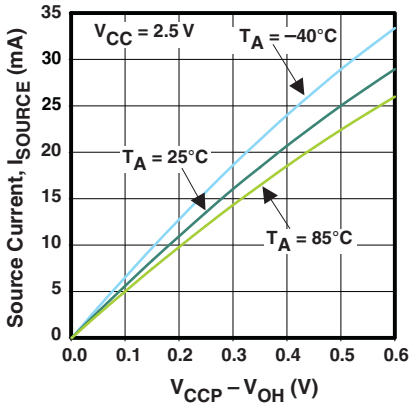


Figure 13. I/O Source Current vs Output High Voltage

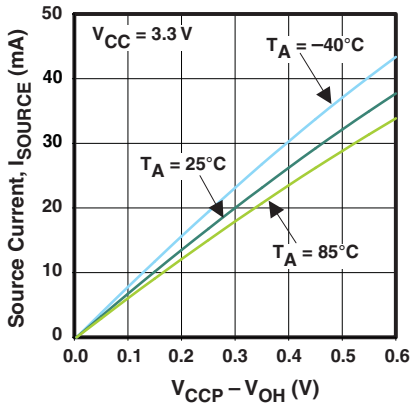


Figure 14. I/O Source Current vs Output High Voltage

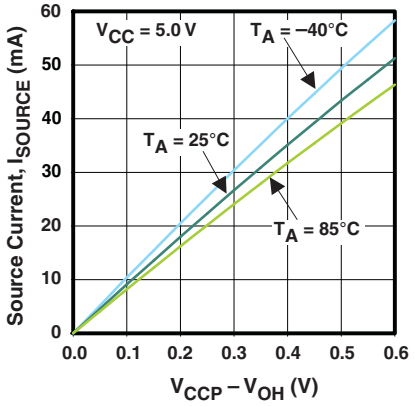


Figure 15. I/O Source Current vs Output High Voltage

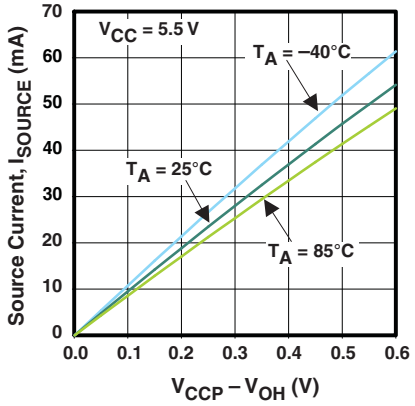


Figure 16. I/O Source Current vs Output High Voltage

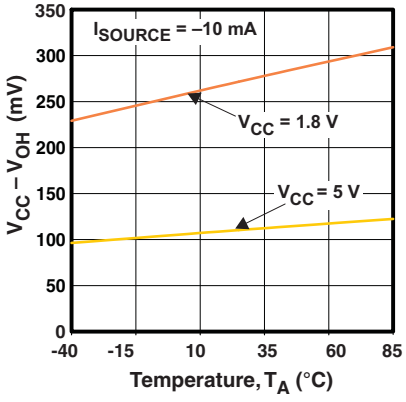
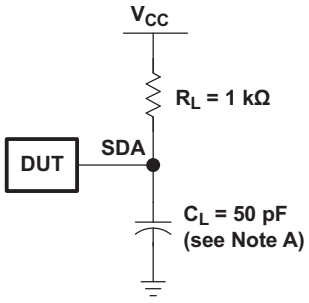
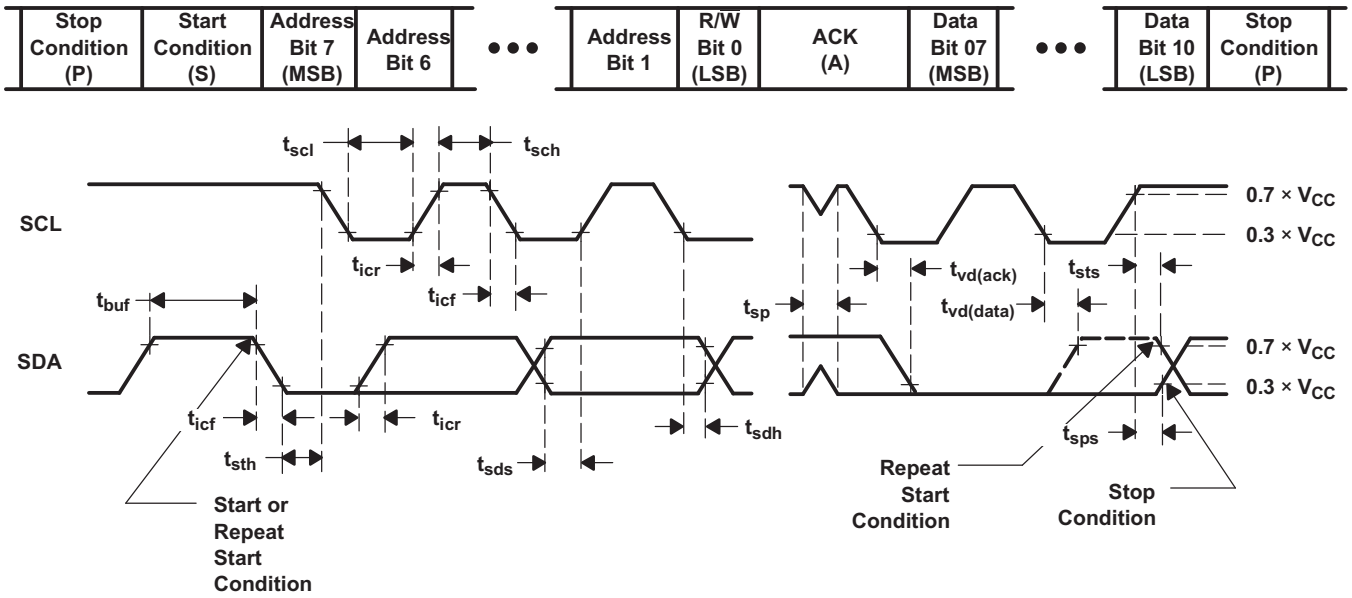


Figure 17. I/O High Voltage vs Temperature

7 Parameter Measurement Information



SDA LOAD CONFIGURATION



VOLTAGE WAVEFORMS

BYTE	DESCRIPTION
1	I^2C address
2, 3	P-port data

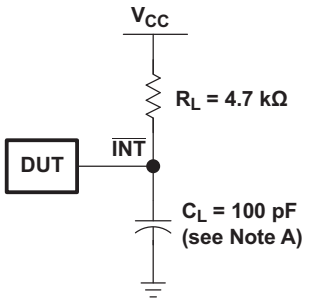
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

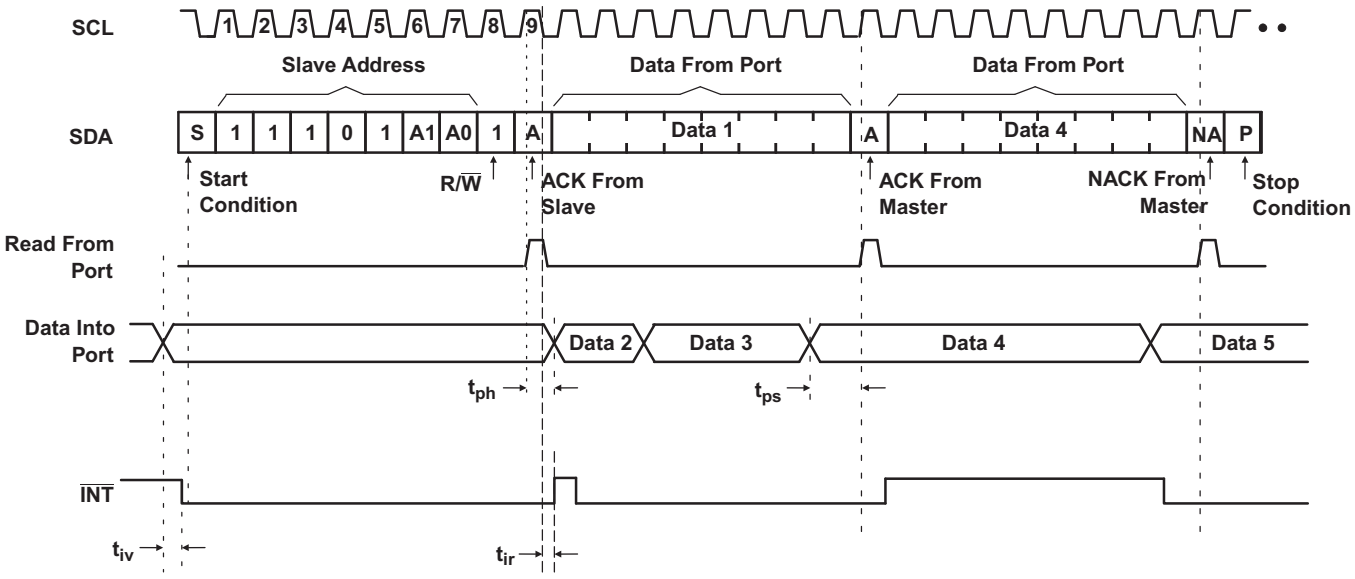
C. All parameters and waveforms are not applicable to all devices.

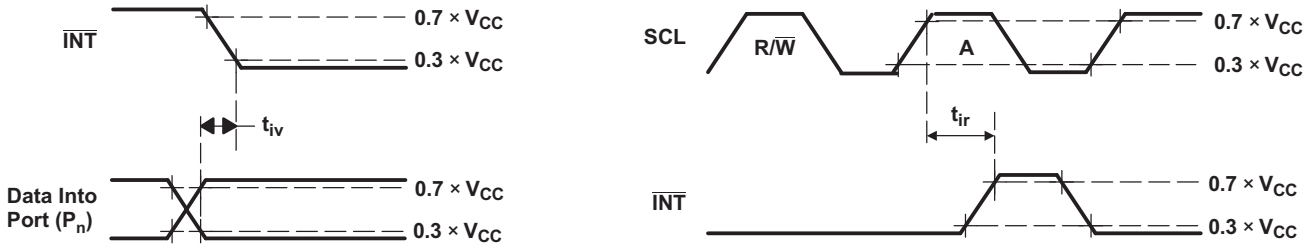
Figure 18. I^2C Interface Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)



INTERRUPT LOAD CONFIGURATION





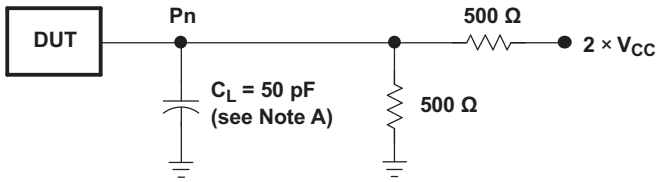
A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

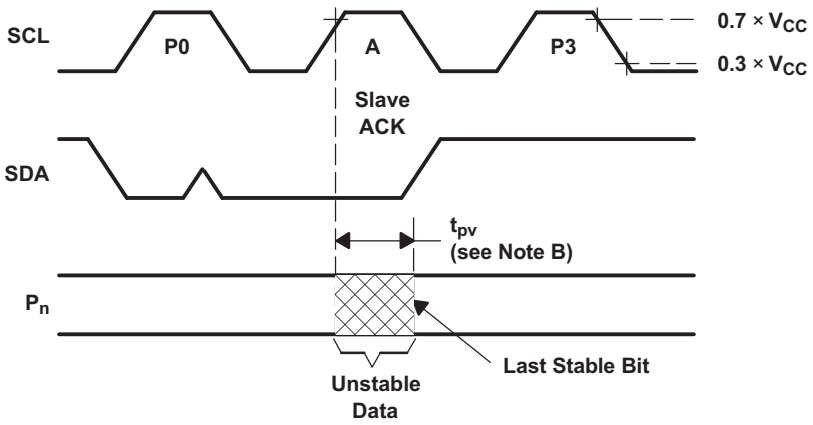
C. All parameters and waveforms are not applicable to all devices.

Figure 19. Interrupt Load Circuit And Voltage Waveforms

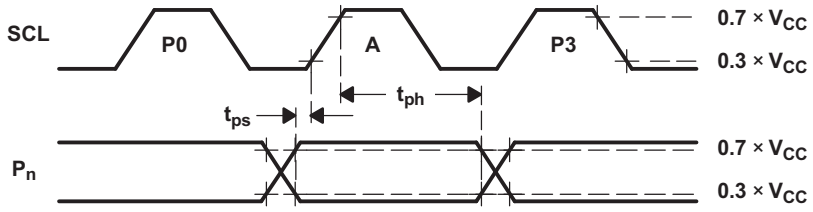
Parameter Measurement Information (continued)



P-PORT LOAD CONFIGURATION



WRITE MODE (R/$\overline{W}$ = 0)



READ MODE (R/$\overline{W}$ = 1)

A. C_L includes probe and jig capacitance.

B. t_{pv} is measured from 0.7 × V_{CC} on SCL to 50% I/O (Pn) output.

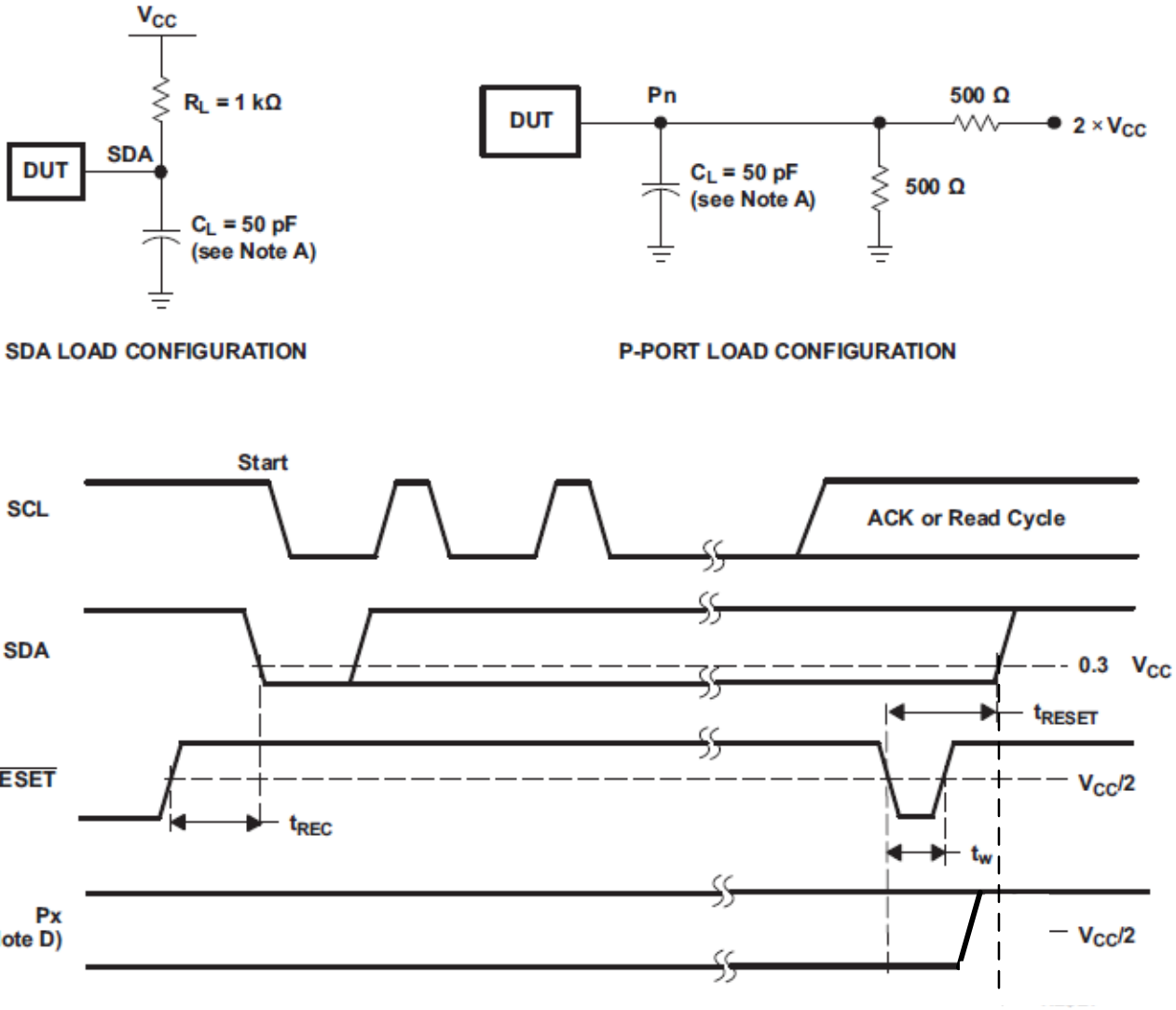
C. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

D. The outputs are measured one at a time, with one transition per measurement.

E. All parameters and waveforms are not applicable to all devices.

Figure 20. P-Port Load Circuit And Voltage Waveforms

Parameter Measurement Information (continued)



A. C_L includes probe and jig capacitance.

B. All inputs are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r/t_f ≤ 30 ns.

C. The outputs are measured one at a time, with one transition per measurement.

D. I/Os are configured as inputs.

E. All parameters and waveforms are not applicable to all devices.

Figure 21. Reset Load Circuits And Voltage Waveforms

8 Detailed Description

8.1 Overview

The TCA9539 is a 16-bit I/O expander for the two-line bidirectional bus (I^2C) designed for 1.65-V to 5.5-V V_{CC} operation. It provides general-purpose remote I/O expansion for most microcontroller families via the I^2C interface [serial clock (SCL), serial data (SDA)].

The TCA9539 consists of two 8-bit Configuration (input or output selection), Input Port, Output Port, and Polarity Inversion (active-high or active-low operation) registers. At power-on, the I/Os are configured as inputs. The system master can enable the I/Os as either inputs or outputs by writing to the I/O configuration register bits. The data for each input or output is kept in the corresponding Input or output register. The polarity of the Input Port register can be inverted with the Polarity Inversion register. All registers can be read by the system master.

The system master can reset the TCA9539 in the event of a time-out or other improper operation by asserting a low in the $\overline{\text{RESET}}$ input. The power-on reset puts the registers in their default state and initializes the I^2C/SMBus state machine. Asserting $\overline{\text{RESET}}$ causes the same reset/initialization to occur without depowering the part.

The TCA9539 open-drain interrupt ($\overline{\text{INT}}$) output is activated when any input state differs from its corresponding Input Port register state and is used to indicate to the system master that an input state has changed.

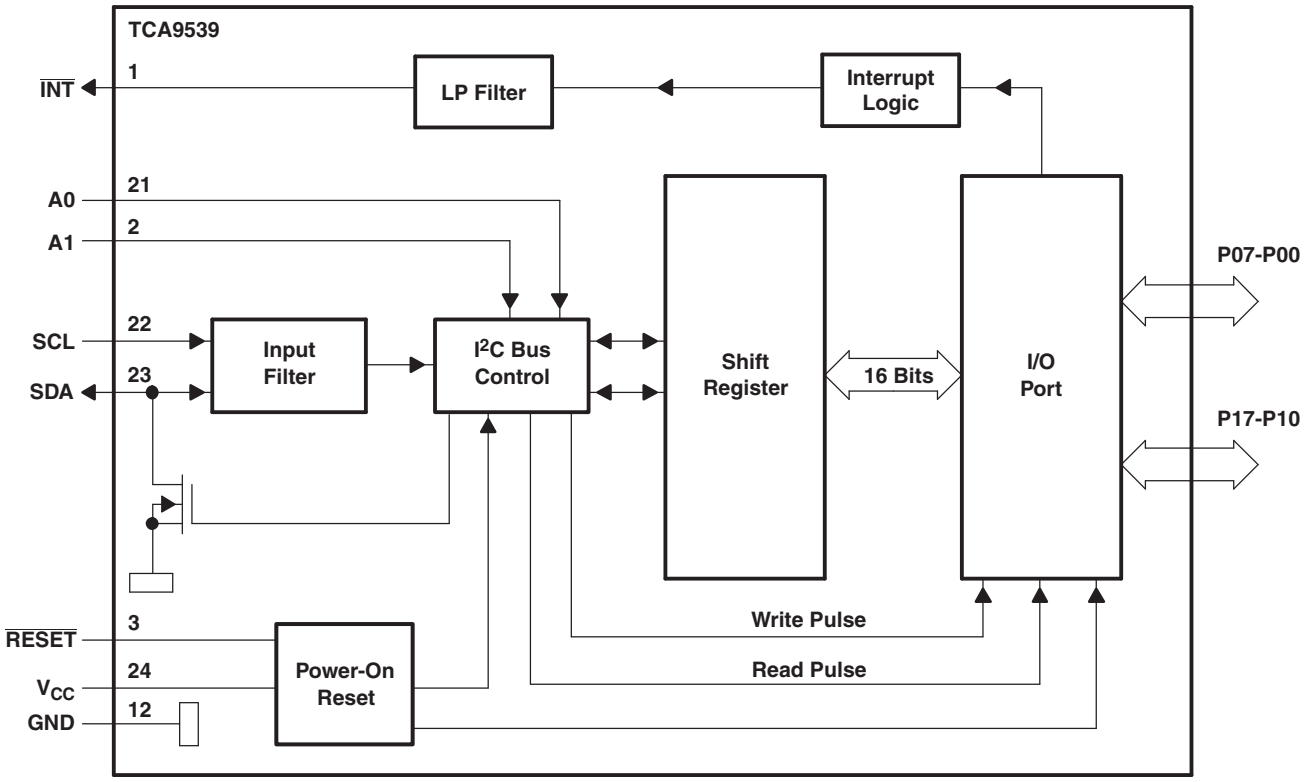
$\overline{\text{INT}}$ can be connected to the interrupt input of a microcontroller. By sending an interrupt signal on this line, the remote I/O can inform the microcontroller if there is incoming data on its ports without having to communicate via the I^2C bus. Thus, the TCA9539 can remain a simple slave device.

The device outputs (latched) have high-current drive capability for directly driving LEDs. The device has low current consumption.

The TCA9539 is identical to the PCA9555, except for the removal of the internal I/O pullup resistor, which greatly reduces power consumption when the I/Os are held low, replacement of A2 with $\overline{\text{RESET}}$, and a different address range. The TCA9539 is similar to the PCA9539 with lower voltage support (down to V_{CC} = 1.65 V), and also improved power-on-reset circuitry for different application scenarios.

Two hardware pins (A0 and A1) are used to program and vary the fixed I^2C address and allow up to four devices to share the same I^2C bus or SMBus.

8.2 Functional Block Diagram

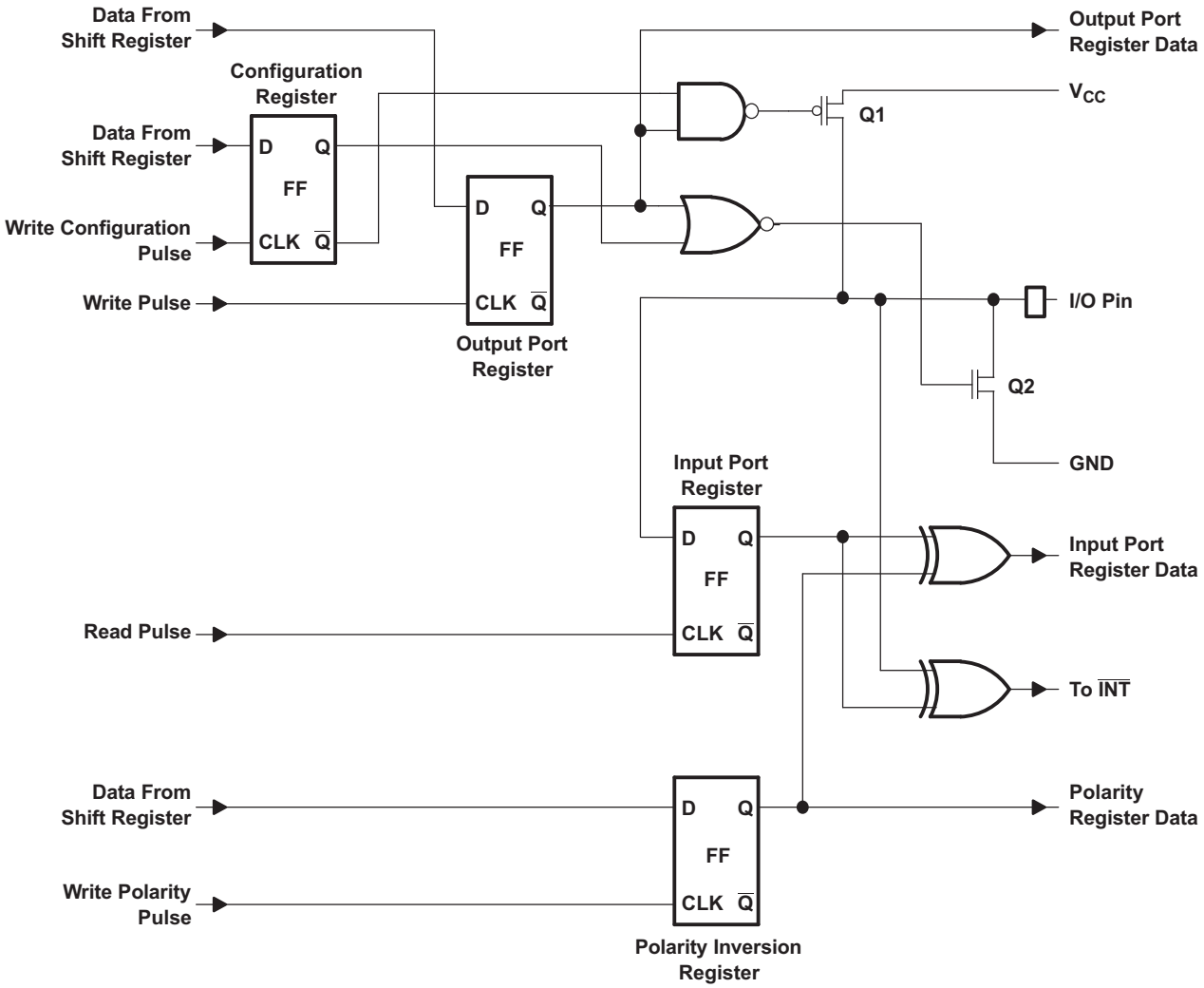


A. Pin numbers shown are for PW package.

B. All I/Os are set to inputs at reset.

Figure 22. Logic Diagram (Positive Logic)

Functional Block Diagram (continued)



(1) At power-on reset, all registers return to default values.

Figure 23. Simplified Schematic of P-Port I/Os

8.3 Feature Description

8.3.1 I/O Port

When an I/O is configured as an input, FETs Q1 and Q2 are off, which creates a high-impedance input. The input voltage may be raised above V_{CC} to a maximum of 5.5 V.

If the I/O is configured as an output, Q1 or Q2 is enabled, depending on the state of the Output Port register. In this case, there are low-impedance paths between the I/O pin and either V_{CC} or GND. The external voltage applied to this I/O pin should not exceed the recommended levels for proper operation.

8.3.2 $\overline{\text{RESET}}$ Input

A reset can be accomplished by holding the $\overline{\text{RESET}}$ pin low for a minimum of t_W. The TCA9539 registers and I^2C/SMBus state machine are held in their default states until $\overline{\text{RESET}}$ is once again high. This input requires a pullup resistor to V_{CC}, if no active connection is used.

Feature Description (continued)

8.3.3 Interrupt ($\overline{INT}$) Output

An interrupt is generated by any rising or falling edge of the port inputs in the input mode. After time, t_{iv}, the signal $\overline{INT}$ is valid. Resetting the interrupt circuit is achieved when data on the port is changed to the original setting or data is read from the port that generated the interrupt. Resetting occurs in the read mode at the acknowledge (ACK) bit or not acknowledge (NACK) bit after the falling edge of the SCL signal. Interrupts that occur during the ACK or NACK clock pulse can be lost (or be very short) due to the resetting of the interrupt during this pulse. Each change of the I/Os after resetting is detected and is transmitted as $\overline{INT}$.

Reading from or writing to another device does not affect the interrupt circuit, and a pin configured as an output cannot cause an interrupt. Changing an I/O from an output to an input may cause a false interrupt to occur if the state of the pin does not match the contents of the Input Port register. Because each 8-bit port is read independently, the interrupt caused by port 0 is not cleared by a read of port 1, or vice versa.

$\overline{INT}$ has an open-drain structure and requires a pullup resistor to V_{CC}.

8.4 Device Functional Modes

8.4.1 Power-On Reset

When power (from 0 V) is applied to VCC, an internal power-on reset holds the TCA9539 in a reset condition until V_{CC} has reached V_{POR_R}. At that point, the reset condition is released and the TCA9539 registers and I^2C/SMBus state machine initialize to their default states. After that, V_{CC} must be lowered to below V_{PORF} and then back up to the operating voltage for a power-reset cycle.

8.5 Programming

8.5.1 I^2C Interface

The TCA9539 has a standard bidirectional I^2C interface that is controlled by a master device in order to be configured or read the status of this device. Each slave on the I^2C bus has a specific device address to differentiate between other slave devices that are on the same I^2C bus. Many slave devices will require configuration upon startup to set the behavior of the device. This is typically done when the master accesses internal register maps of the slave, which have unique register addresses. A device can have one or multiple registers where data is stored, written, or read. For more information see *Understanding the I^2C Bus*, (SLVA704).

The physical I^2C interface consists of the serial clock (SCL) and serial data (SDA) lines. Both SDA and SCL lines must be connected to V_{CC} through a pull-up resistor. The size of the pull-up resistor is determined by the amount of capacitance on the I^2C lines. For further details, refer to *I^2C Pull-up Resistor Calculation* (SLVA689). Data transfer may be initiated only when the bus is idle. A bus is considered idle if both SDA and SCL lines are high after a STOP condition.

The following is the general procedure for a master to access a slave device:

1. If a master wants to send data to a slave:
   - Master-transmitter sends a START condition and addresses the slave-receiver.
   - Master-transmitter sends data to slave-receiver.
   - Master-transmitter terminates the transfer with a STOP condition.
2. If a master wants to receive or read data from a slave:
   - Master-receiver sends a START condition and addresses the slave-transmitter.
   - Master-receiver sends the requested register to read to slave-transmitter.
   - Master-receiver receives data from the slave-transmitter.

Programming (continued)

– Master-receiver terminates the transfer with a STOP condition.

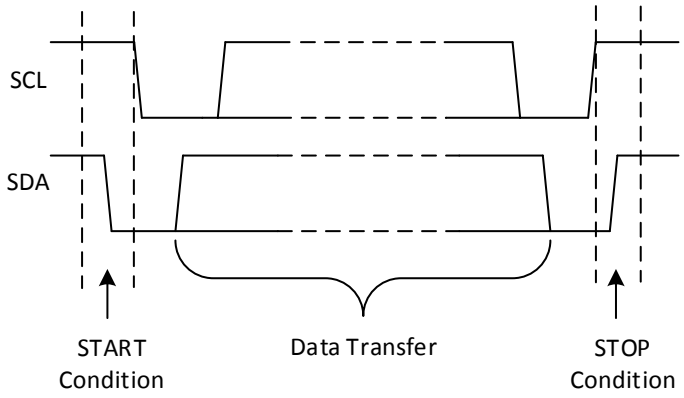


Figure 24. Definition of Start and Stop Conditions

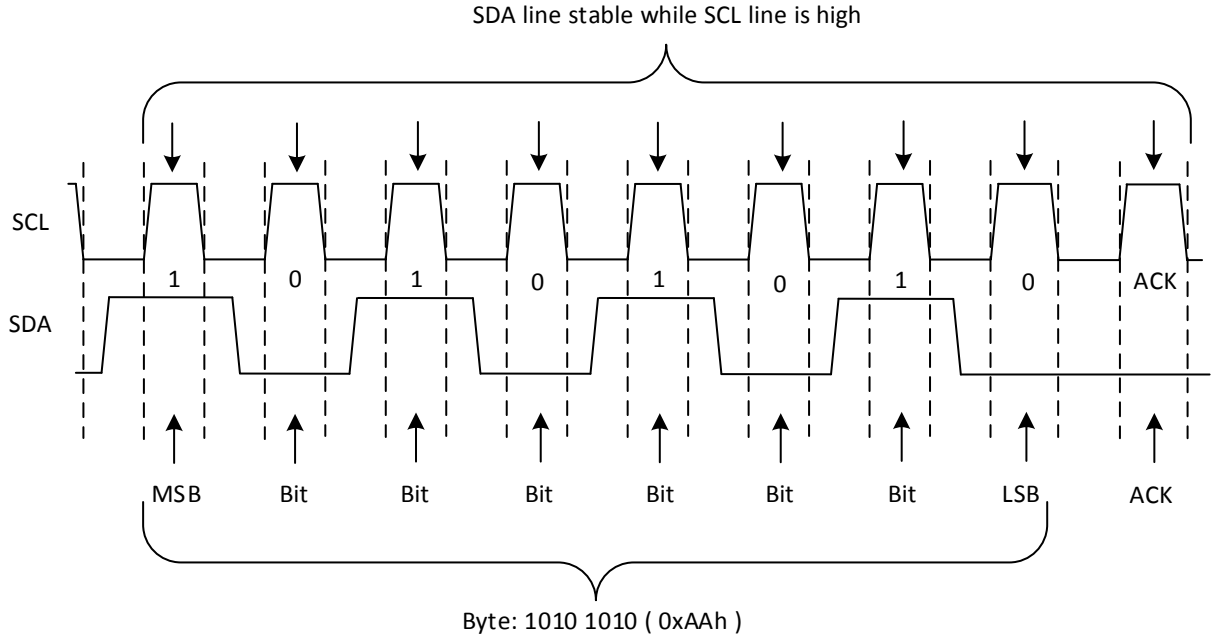


Figure 25. Bit Transfer

Table 1. Interface Definition

BYTE	BIT							
	7 (MSB)	6	5	4	3	2	1	0 (LSB)
I^2C slave address	H	H	H	L	H	A1	A0	R/$\overline{W}$
P0x I/O data bus	P07	P06	P05	P04	P03	P02	P01	P00
P1x I/O data bus	P17	P16	P15	P14	P13	P12	P11	P10

8.6 Register Maps

8.6.1 Device Address

Figure 26 shows the address byte of the TCA9539.

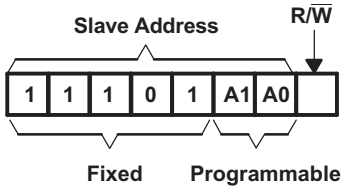


Figure 26. TCA9539 Address

Table 2. Address Reference

INPUTS		I^2C BUS SLAVE ADDRESS
A1	A0	
L	L	116 (decimal), 74 (hexadecimal)
L	H	117 (decimal), 75 (hexadecimal)
H	L	118 (decimal), 76 (hexadecimal)
H	H	119 (decimal), 77 (hexadecimal)

The last bit of the slave address defines the operation (read or write) to be performed. A high (1) selects a read operation, while a low (0) selects a write operation.

8.6.2 Control Register and Command Byte

Following the successful acknowledgment of the address byte, the bus master sends a command byte that is stored in the control register in the TCA9539. Three bits of this data byte state the operation (read or write) and the internal register (input, output, Polarity Inversion or Configuration) that will be affected. This register can be written or read through the I^2C bus. The command byte is sent only during a write transmission.

Once a command byte has been sent, the register pair that was addressed continues to be accessed by reads until a new command byte has been sent.

0	0	0	0	0	B2	B1	B0

Figure 27. Control Register Bits

Table 3. Command Byte

CONTROL REGISTER BITS			COMMAND BYTE (HEX)	REGISTER	PROTOCOL	POWER-UP DEFAULT
B2	B1	B0				
0	0	0	0x00	Input Port 0	Read byte	xxxx xxxx
0	0	1	0x01	Input Port 1	Read byte	xxxx xxxx
0	1	0	0x02	Output Port 0	Read/write byte	1111 1111
0	1	1	0x03	Output Port 1	Read/write byte	1111 1111
1	0	0	0x04	Polarity Inversion Port 0	Read/write byte	0000 0000
1	0	1	0x05	Polarity Inversion Port 1	Read/write byte	0000 0000
1	1	0	0x06	Configuration Port 0	Read/write byte	1111 1111
1	1	1	0x07	Configuration Port 1	Read/write byte	1111 1111

8.6.3 Register Descriptions

The Input Port registers (registers 0 and 1) reflect the incoming logic levels of the pins, regardless of whether the pin is defined as an input or an output by the Configuration register. It only acts on read operation. Writes to these registers have no effect. The default value, X, is determined by the externally applied logic level.

Before a read operation, a write transmission is sent with the command byte to indicate to the I^2C device that the Input Port register will be accessed next.

Table 4. Registers 0 And 1 (Input Port Registers)

Bit	I0.7	I0.6	I0.5	I0.4	I0.3	I0.2	I0.1	I0.0
Default	X	X	X	X	X	X	X	X
Bit	I1.7	I1.6	I1.5	I1.4	I1.3	I1.2	I1.1	I1.0
Default	X	X	X	X	X	X	X	X

The Output Port registers (registers 2 and 3) show the outgoing logic levels of the pins defined as outputs by the Configuration register. Bit values in this register have no effect on pins defined as inputs. In turn, reads from this register reflect the value that is in the flip-flop controlling the output selection, not the actual pin value.

Table 5. Registers 2 And 3 (Output Port Registers)

Bit	O0.7	O0.6	O0.5	O0.4	O0.3	O0.2	O0.1	O0.0
Default	1	1	1	1	1	1	1	1
Bit	O1.7	O1.6	O1.5	O1.4	O1.3	O1.2	O1.1	O1.0
Default	1	1	1	1	1	1	1	1

The Polarity Inversion registers (registers 4 and 5) allow Polarity Inversion of pins defined as inputs by the Configuration register. If a bit in this register is set (written with 1), the corresponding port pin's polarity is inverted. If a bit in this register is cleared (written with a 0), the corresponding port pin's original polarity is retained.

Table 6. Registers 4 And 5 (Polarity Inversion Registers)

Bit	N0.7	N0.6	N0.5	N0.4	N0.3	N0.2	N0.1	N0.0
Default	0	0	0	0	0	0	0	0
Bit	N1.7	N1.6	N1.5	N1.4	N1.3	N1.2	N1.1	N1.0
Default	0	0	0	0	0	0	0	0

The Configuration registers (registers 6 and 7) configure the directions of the I/O pins. If a bit in this register is set to 1, the corresponding port pin is enabled as an input with a high-impedance output driver. If a bit in this register is cleared to 0, the corresponding port pin is enabled as an output.

Table 7. Registers 6 And 7 (Configuration Registers)

Bit	C0.7	C0.6	C0.5	C0.4	C0.3	C0.2	C0.1	C0.0
Default	1	1	1	1	1	1	1	1
Bit	C1.7	C1.6	C1.5	C1.4	C1.3	C1.2	C1.1	C1.0
Default	1	1	1	1	1	1	1	1

8.6.3.1 Bus Transactions

Data is exchanged between the master and the TCA9539 through write and read commands, and this is accomplished by reading from or writing to registers in the slave device.

Registers are locations in the memory of the slave which contain information, whether it be the configuration information or some sampled data to send back to the master. The master must write information to these registers in order to instruct the slave device to perform a task.

8.6.3.1.1 Writes

To write on the I^2C bus, the master will send a START condition on the bus with the address of the slave, as well as the last bit (the R/$\overline{W}$ bit) set to 0, which signifies a write. After the slave sends the acknowledge bit, the master will then send the register address of the register to which it wishes to write. The slave will acknowledge again, letting the master know it is ready. After this, the master will start sending the register data to the slave until the master has sent all the data necessary (which is sometimes only a single byte), and the master will terminate the transmission with a STOP condition.

See *Register Descriptions* section to see list of the TCA9539's internal registers and a description of each one.

Figure 28 shows an example of writing a single byte to a slave register.

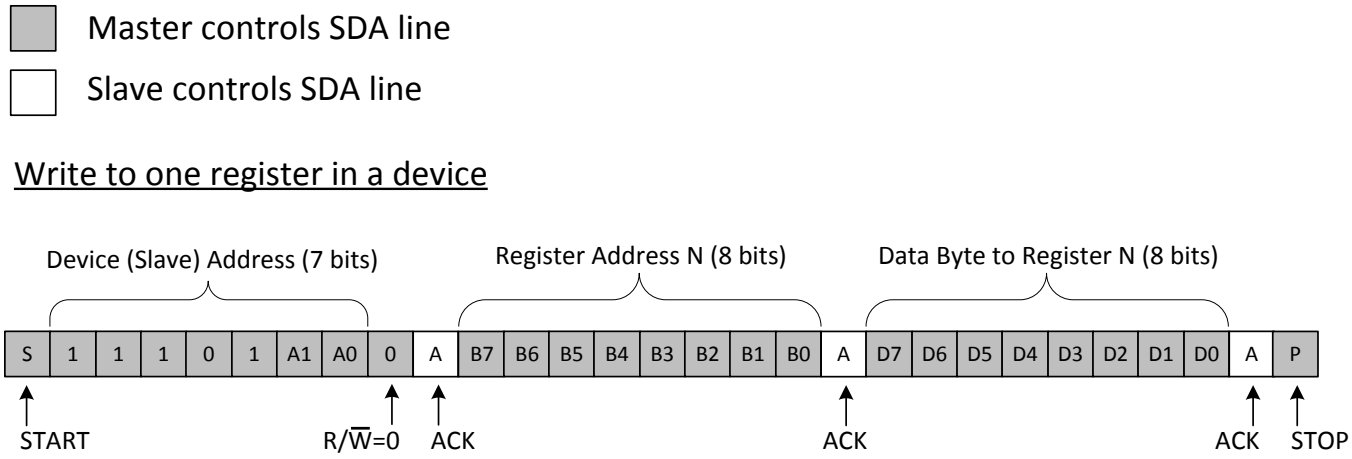


Figure 28. Write to Register

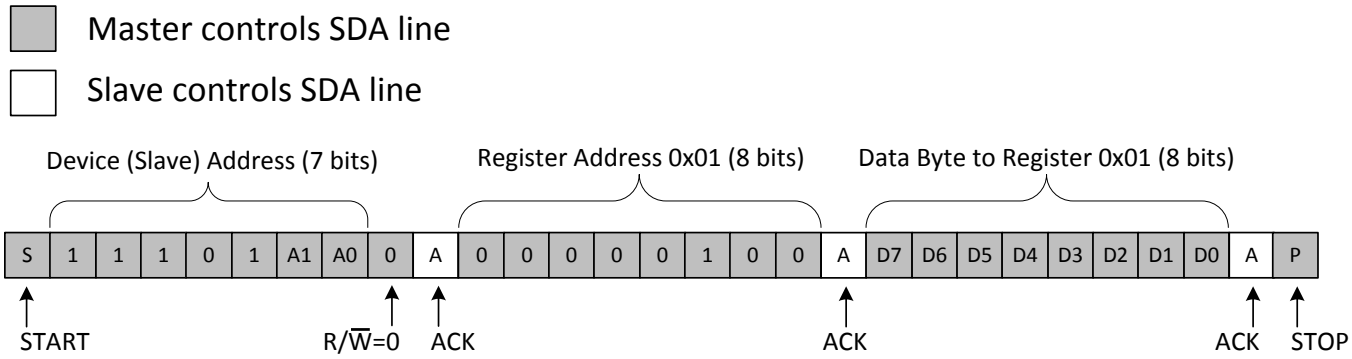


Figure 29. Write to the Polarity Inversion Register

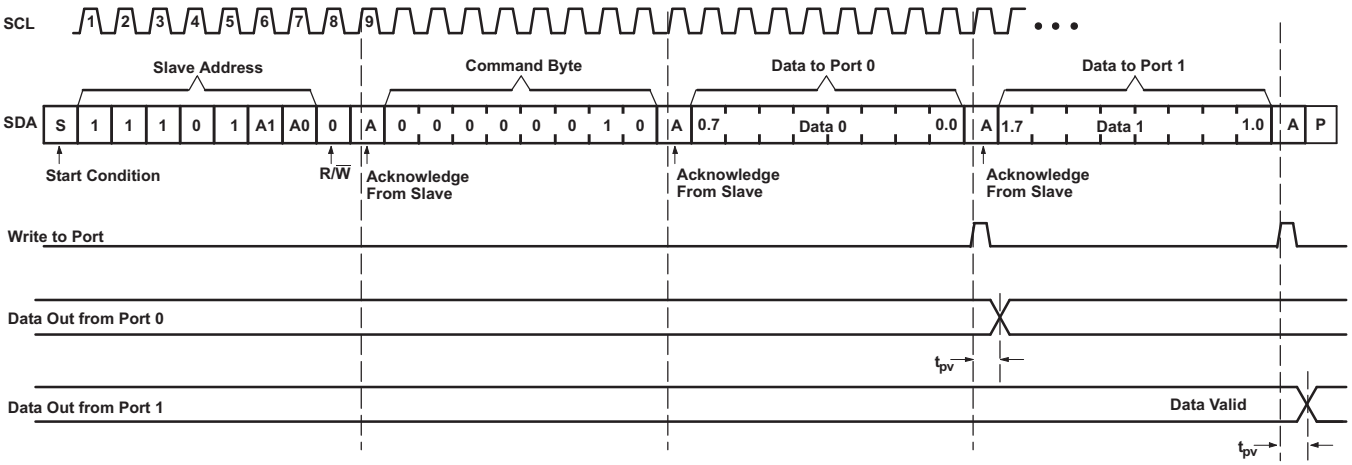


Figure 30. Write to Output Port Registers

8.6.3.1.2 Reads

Reading from a slave is very similar to writing, but requires some additional steps. In order to read from a slave, the master must first instruct the slave which register it wishes to read from. This is done by the master starting off the transmission in a similar fashion as the write, by sending the address with the R/$\overline{W}$ bit equal to 0 (signifying a write), followed by the register address it wishes to read from. Once the slave acknowledges this register address, the master will send a START condition again, followed by the slave address with the R/$\overline{W}$ bit set to 1 (signifying a read). This time, the slave will acknowledge the read request, and the master will release the SDA bus but will continue supplying the clock to the slave. During this part of the transaction, the master will become the master-receiver, and the slave will become the slave-transmitter.

The master will continue to send out the clock pulses, but will release the SDA line so that the slave can transmit data. At the end of every byte of data, the master will send an ACK to the slave, letting the slave know that it is ready for more data. Once the master has received the number of bytes it is expecting, it will send a NACK, signaling to the slave to halt communications and release the bus. The master will follow this up with a STOP condition.

See *Register Descriptions* section to see list of the TCA9539's internal registers and a description of each one.

Figure 31 shows an example of reading a single byte from a slave register.

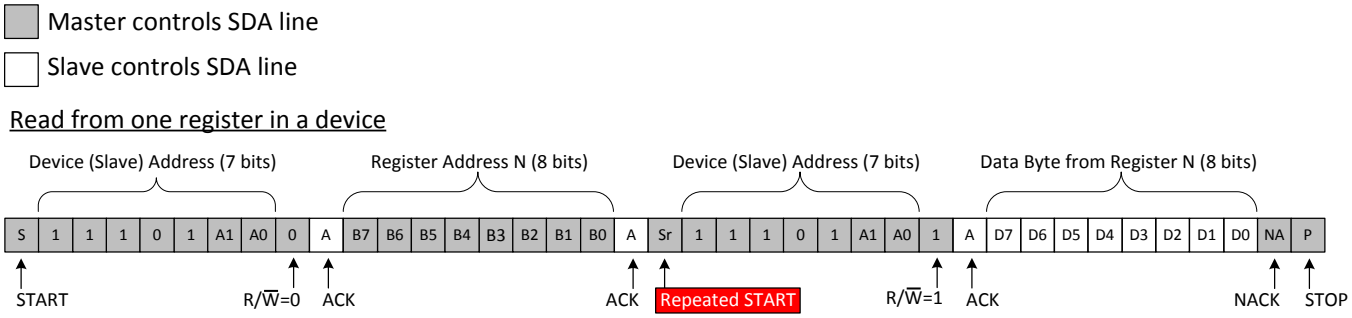
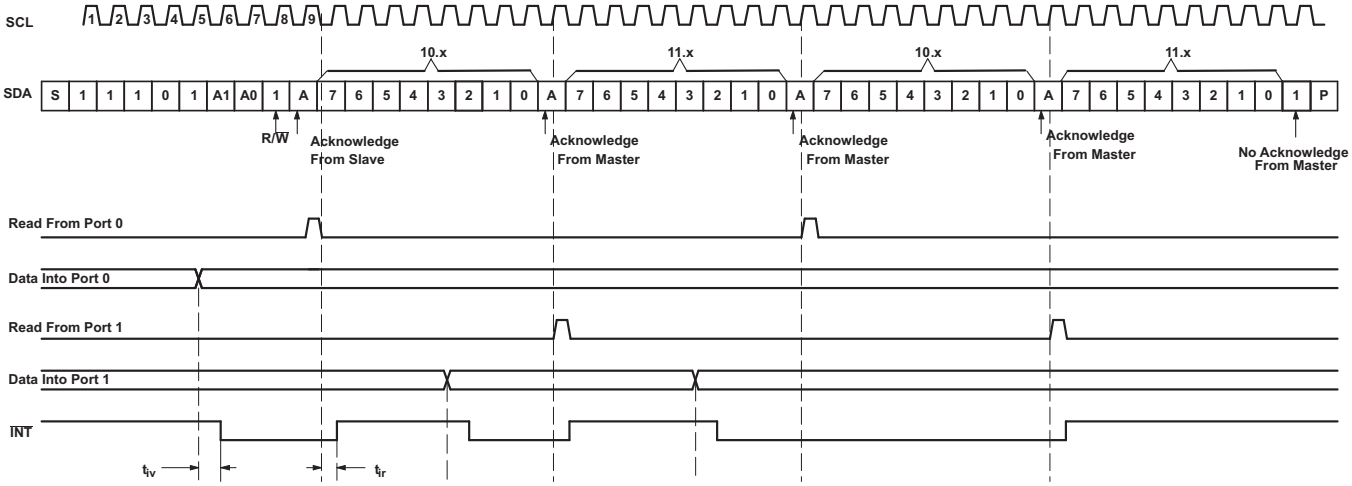


Figure 31. Read from Register

After a restart, the value of the register defined by the command byte matches the register being accessed when the restart occurred. For example, if the command byte references Input Port 1 before the restart, and the restart occurs when Input Port 0 is being read, the stored command byte changes to reference Input Port 0. The original command byte is forgotten. If a subsequent restart occurs, Input Port 0 is read first. Data is clocked into the register on the rising edge of the ACK clock pulse. After the first byte is read, additional bytes may be read, but the data now reflect the information in the other register in the pair. For example, if Input Port 1 is read, the next byte read is Input Port 0.

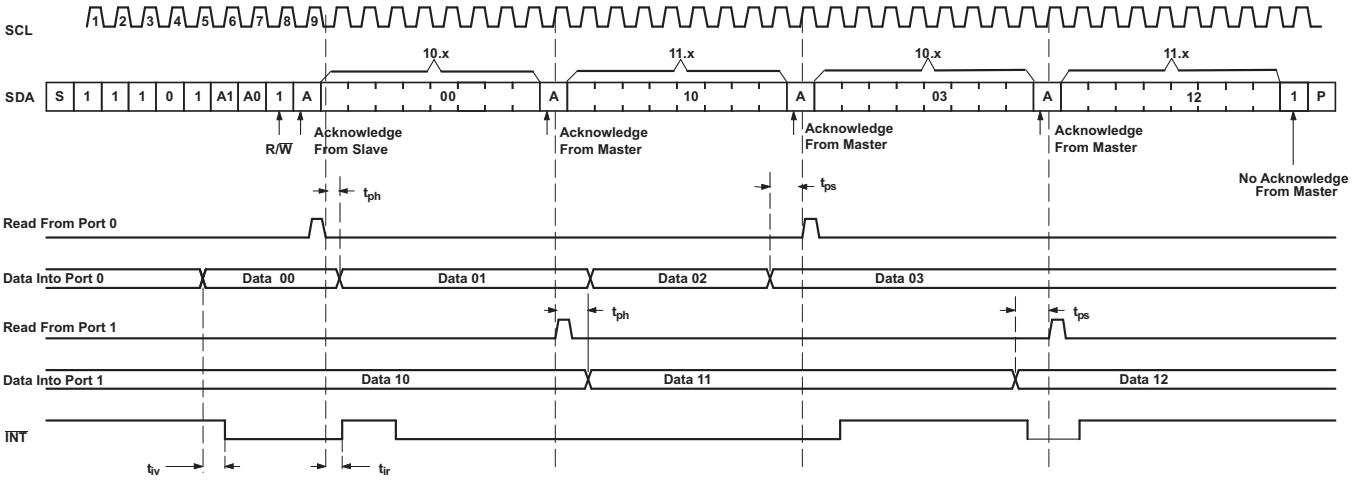
Data is clocked into the register on the rising edge of the ACK clock pulse. There is no limitation on the number of data bytes received in one read transmission, but when the final byte is received, the bus master must not acknowledge the data.



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 31 for these details).

Figure 32. Read Input Port Register, Scenario 1



A. Transfer of data can be stopped at any time by a Stop condition. When this occurs, data present at the latest acknowledge phase is valid (output mode). It is assumed that the command byte previously has been set to 00 (Read Input Port register).

B. This figure eliminates the command byte transfer, a restart, and slave address call between the initial slave address call and actual data transfer from the P port (see Figure 31 for these details).

Figure 33. Read Input Port Register, Scenario 2

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

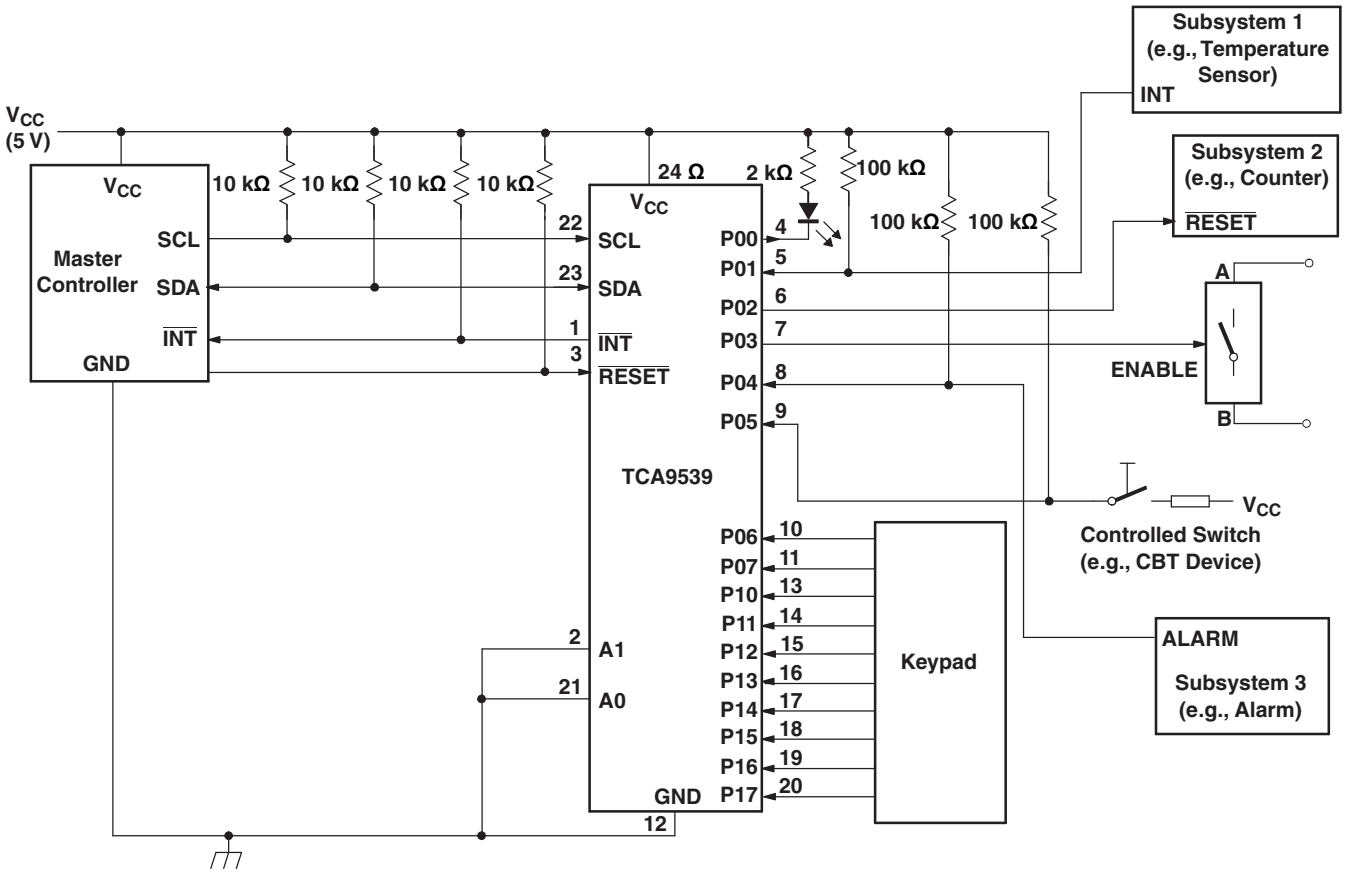
9.1 Application Information

Applications of the TCA9539 will have this device connected as a slave to an I^2C master (processor), and the I^2C bus may contain any number of other slave devices. The TCA9539 will typically be in a remote location from the master, placed close to the GPIOs to which the master needs to monitor or control.

IO Expanders such as the TCA9539 are typically used for controlling LEDs (for feedback or status lights), controlling enable or reset signals of other devices, and even reading the outputs of other devices or buttons.

9.2 Typical Application

Figure 34 shows an application in which the TCA9539 can be used.



A. Device address is configured as 1110100 for this example.

B. P00, P02, and P03 are configured as outputs.

C. P01 and P04 to P17 are configured as inputs.

D. Pin numbers shown are for the PW package.

Figure 34. Application Schematic

Typical Application (continued)

9.2.1 Design Requirements

9.2.1.1 Minimizing I_{CC} When I/Os Control LEDs

When an I/O is used to control an LED, normally it is connected to V_{CC} through a resistor (see Figure 34). Because the LED acts as a diode, when the LED is off, the I/O V_{IN} is about 1.2 V less than V_{CC}. The ΔI_{CC} parameter in *Electrical Characteristics* shows how I_{CC} increases as V_{IN} becomes lower than V_{CC}. For battery-powered applications, it is essential that the voltage of I/O pins is greater than or equal to V_{CC}, when the LED is off, to minimize current consumption.

Figure 35 shows a high-value resistor in parallel with the LED. Figure 36 shows V_{CC} less than the LED supply voltage by at least 1.2 V. Both of these methods maintain the I/O V_{CC} at or above V_{CC} and prevent additional supply-current consumption when the LED is off.

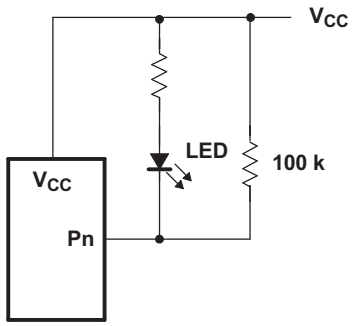


Figure 35. High-Value Resistor In Parallel With Led

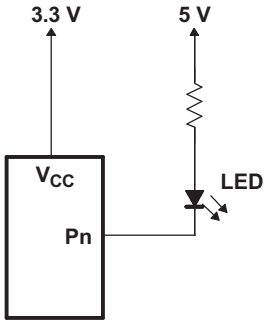


Figure 36. Device Supplied By Lower Voltage

Typical Application (continued)

9.2.2 Detailed Design Procedure

The pull-up resistors, R_P, for the SCL and SDA lines need to be selected appropriately and take into consideration the total capacitance of all slaves on the I^2C bus. The minimum pull-up resistance is a function of V_{CC}, $V_{OL,(max)}$, and I_{OL}:

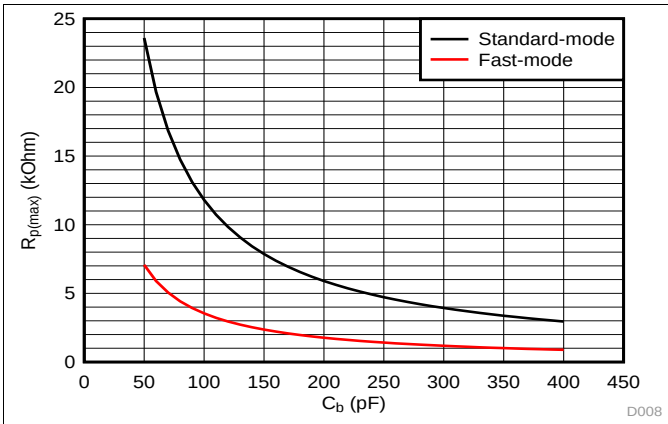
$$R_{p(min)} = \frac{V_{CC} - V_{OL(max)}}{I_{OL}} \quad (1)$$

The maximum pull-up resistance is a function of the maximum rise time, t_r (300 ns for fast-mode operation, f_{SCL} = 400 kHz) and bus capacitance, C_b:

$$R_{p(max)} = \frac{t_r}{0.8473 \times C_b} \quad (2)$$

The maximum bus capacitance for an I^2C bus must not exceed 400 pF for standard-mode or fast-mode operation. The bus capacitance can be approximated by adding the capacitance of the TCA9554A, C_i for SCL or C_{io} for SDA, the capacitance of wires/connections/traces, and the capacitance of additional slaves on the bus.

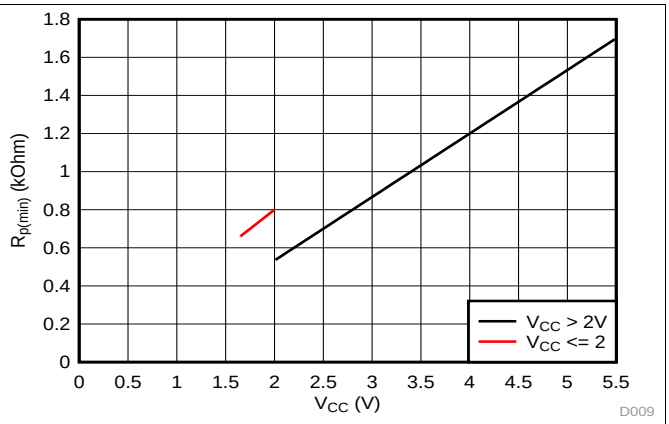
9.2.3 Application Curves



Standard-mode (f_{SCL}= 100 kHz, t_r = 1 µs)

Fast-mode (f_{SCL}= 400 kHz, t_r= 300 ns)

Figure 37. Maximum Pull-Up resistance ($R_{p(max)}$) vs Bus Capacitance (C_b)



V_{OL} = 0.2*V_{CC}, I_{OL} = 2 mA when V_{CC} ≤ 2 V

V_{OL} = 0.4 V, I_{OL} = 3 mA when V_{CC} > 2 V

Figure 38. Minimum Pull-Up Resistance ($R_{p(min)}$) vs Pull-Up Reference Voltage (V_{CC})

10 Power Supply Recommendations

10.1 Power-On Reset Requirements

In the event of a glitch or data corruption, TCA9539 can be reset to its default conditions by using the power-on reset feature. Power-on reset requires that the device go through a power cycle to be completely reset. This reset also happens when the device is powered on for the first time in an application.

The voltage waveform for a power-on reset is shown in Figure 39.

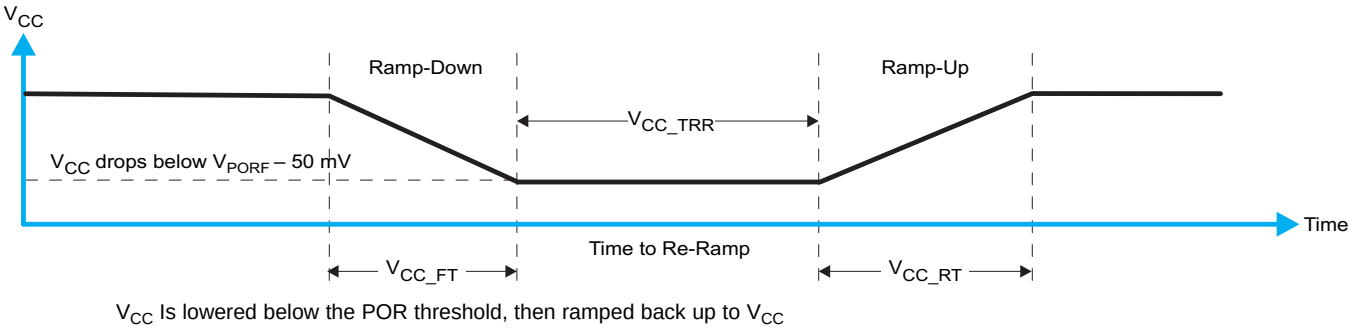


Figure 39. Voltage Waveform for Power-On Reset

Table 8 specifies the performance of the power-on reset feature for TCA9539.

Table 8. Recommended Supply Sequencing and Ramp Rates (1)

PARAMETER			MIN	TYP	MAX	UNIT
V_{CC_FT}	Fall rate	See Figure 39	0.22			ms
V_{CC_RT}	Rise rate	See Figure 39	0.15			ms
V_{CC_TRR}	Time to re-ramp (when V_{CC} drops to V_{POR_MIN} – 50 mV or when V_{CC} drops to GND)	See Figure 39	1			µs
V_{CC_GH}	Level that V_{CC} can glitch down to, but not cause a functional disruption when V_{CC_GW} = 1 µs	See Figure 40			1.2	V
V_{CC_GW}	Glitch width that will not cause a functional disruption when V_{CC_GH} = 0.5 × V_{CC} (For V_{CC} > 3.0 V)	See Figure 40			10	µs

(1) T_A = –40°C to 85°C (unless otherwise noted)

Glitches in the power supply can also affect the power-on reset performance of this device. The glitch width (V_{CC_GW}) and height (V_{CC_GH}) are dependent on each other. The bypass capacitance, source impedance, and device impedance are factors that affect power-on reset performance. Figure 40 and Table 8 provide more information on how to measure these specifications.

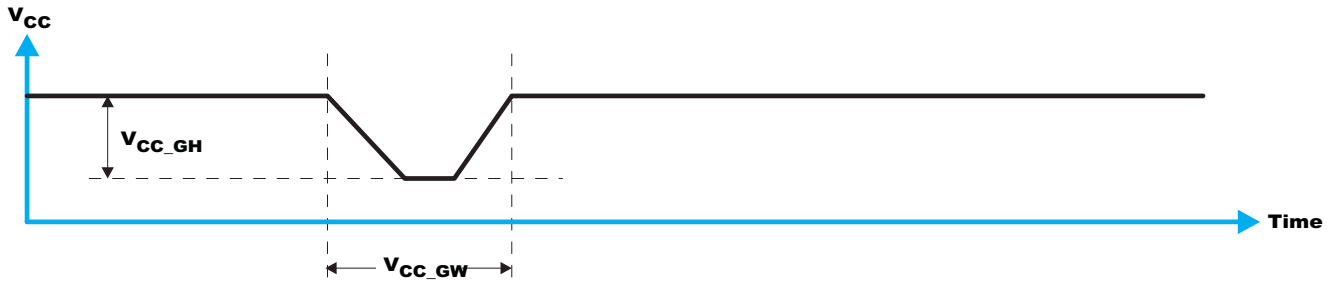


Figure 40. Glitch Width and Glitch Height

V_{POR} is critical to the power-on reset. V_{PORR} is the voltage level at which the reset condition is released and all the registers and the I^2C/SMBus state machine are initialized to their default states. The value of V_{POR} differs based on the V_{CC} being lowered to or from 0. Figure 41 and Table 8 provide more details on this specification.

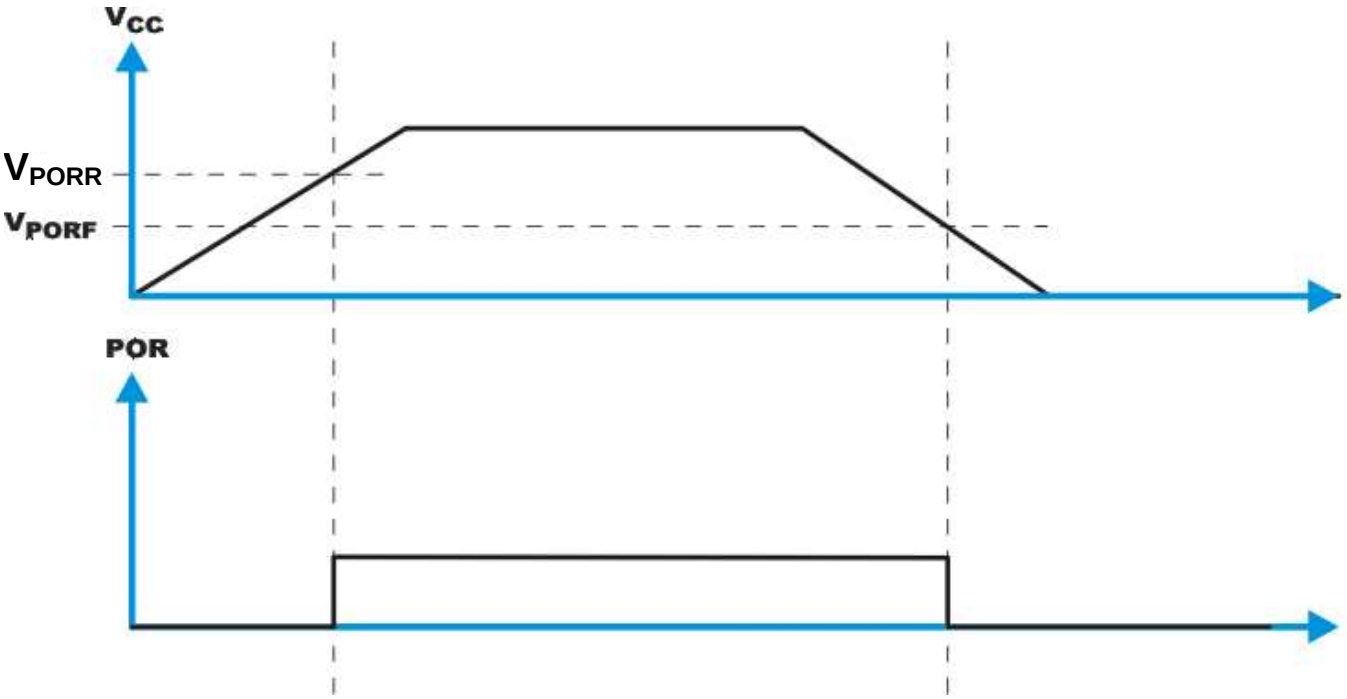


Figure 41. V_{POR}

11 Layout

11.1 Layout Guidelines

For printed circuit board (PCB) layout of the TCA9554A, common PCB layout practices should be followed but additional concerns related to high-speed data transfer such as matched impedances and differential pairs are not a concern for I^2C signal speeds.

In all PCB layouts, it is a best practice to avoid right angles in signal traces, to fan out signal traces away from each other upon leaving the vicinity of an integrated circuit (IC), and to use thicker trace widths to carry higher amounts of current that commonly pass through power and ground traces. By-pass and de-coupling capacitors are commonly used to control the voltage on the VCC pin, using a larger capacitor to provide additional power in the event of a short power supply glitch and a smaller capacitor to filter out high-frequency ripple. These capacitors should be placed as close to the TCA9554A as possible. These best practices are shown in Figure 42.

For the layout example provided in Figure 42, it would be possible to fabricate a PCB with only 2 layers by using the top layer for signal routing and the bottom layer as a split plane for power (V_{CC}) and ground (GND). However, a 4 layer board is preferable for boards with higher density signal routing. On a 4 layer PCB, it is common to route signals on the top and bottom layer, dedicate one internal layer to a ground plane, and dedicate the other internal layer to a power plane. In a board layout using planes or split planes for power and ground, vias are placed directly next to the surface mount component pad which needs to attach to V_{CC} or GND and the via is connected electrically to the internal layer or the other side of the board. Vias are also used when a signal trace needs to be routed to the opposite side of the board, but this technique is not demonstrated in Figure 42.

11.2 Layout Example

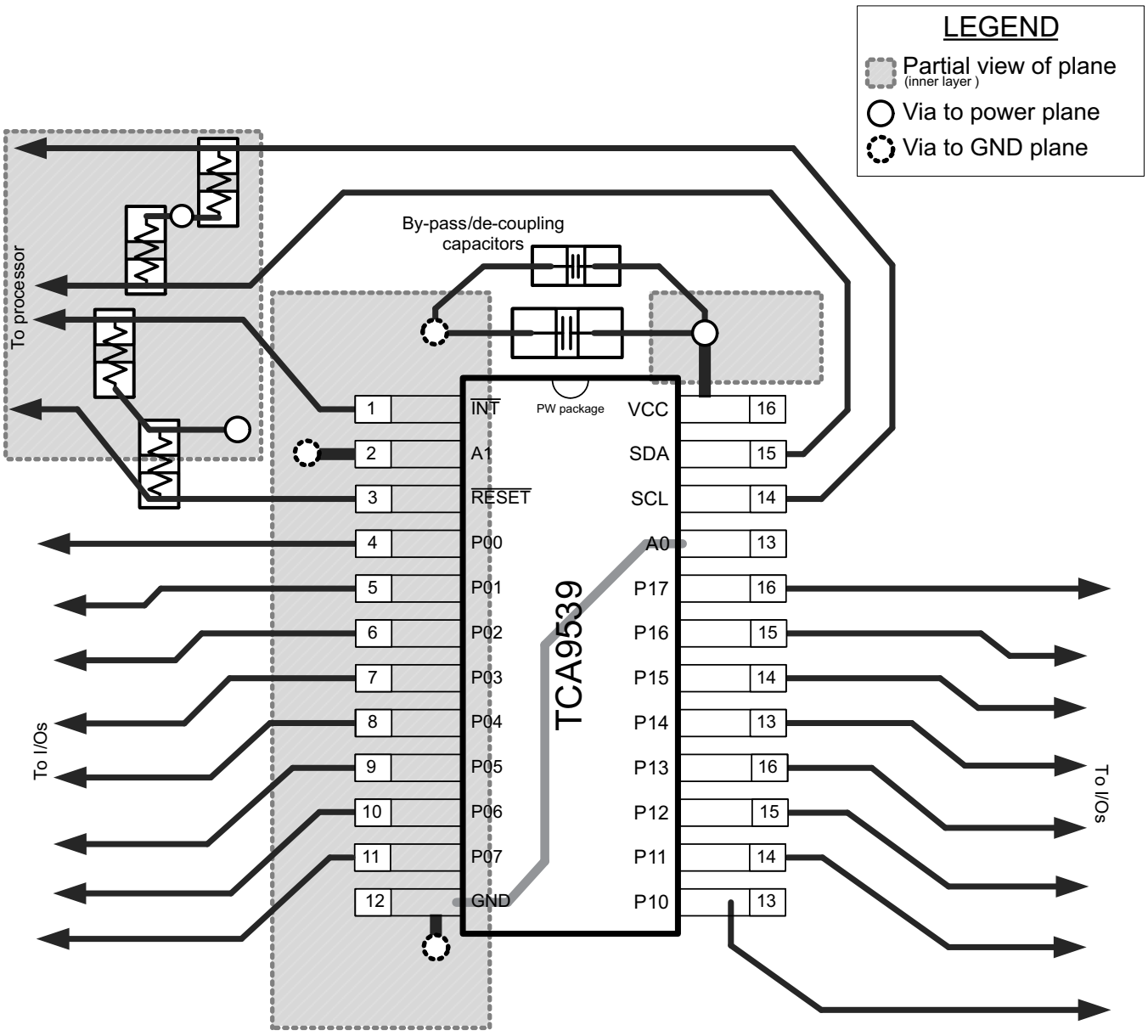


Figure 42. TCA9539 Layout

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TCA9539PWR	ACTIVE	TSSOP	PW	24	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW539	Samples
TCA9539RTWR	ACTIVE	WQFN	RTW	24	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	PW539	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TCA9539 :

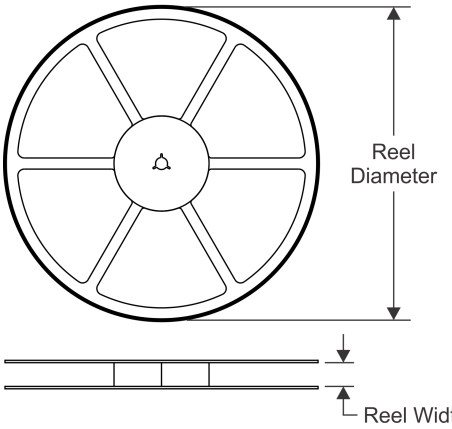
- Automotive: TCA9539-Q1

NOTE: Qualified Version Definitions:

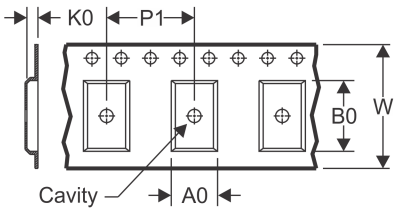
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

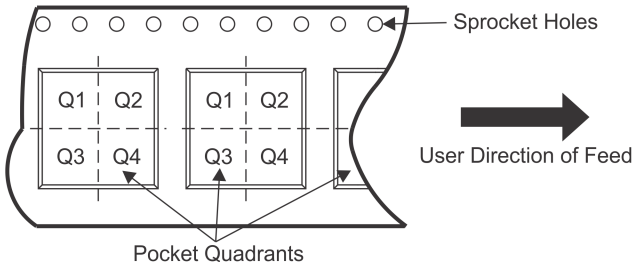


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

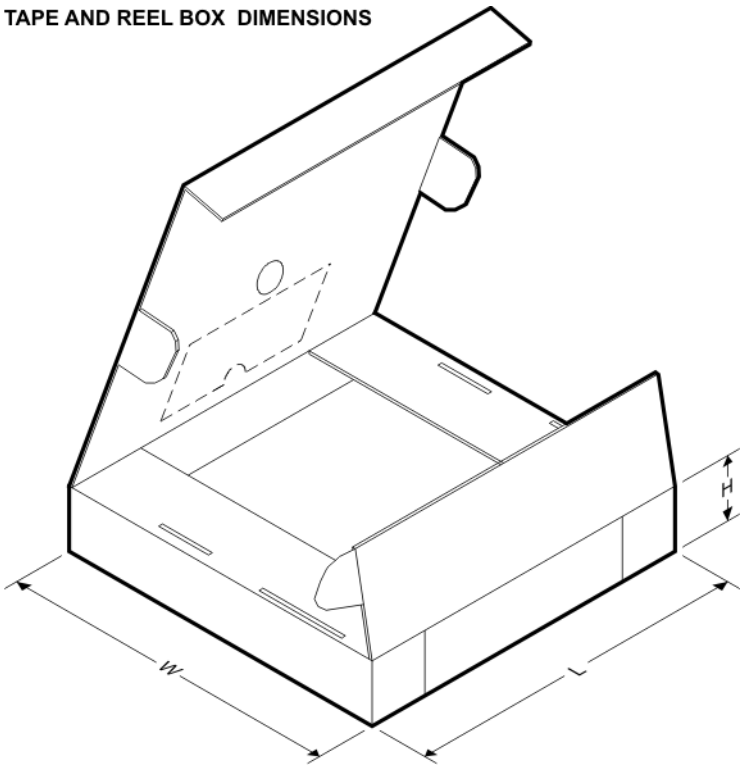
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TCA9539PWR	TSSOP	PW	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
TCA9539RTWR	WQFN	RTW	24	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

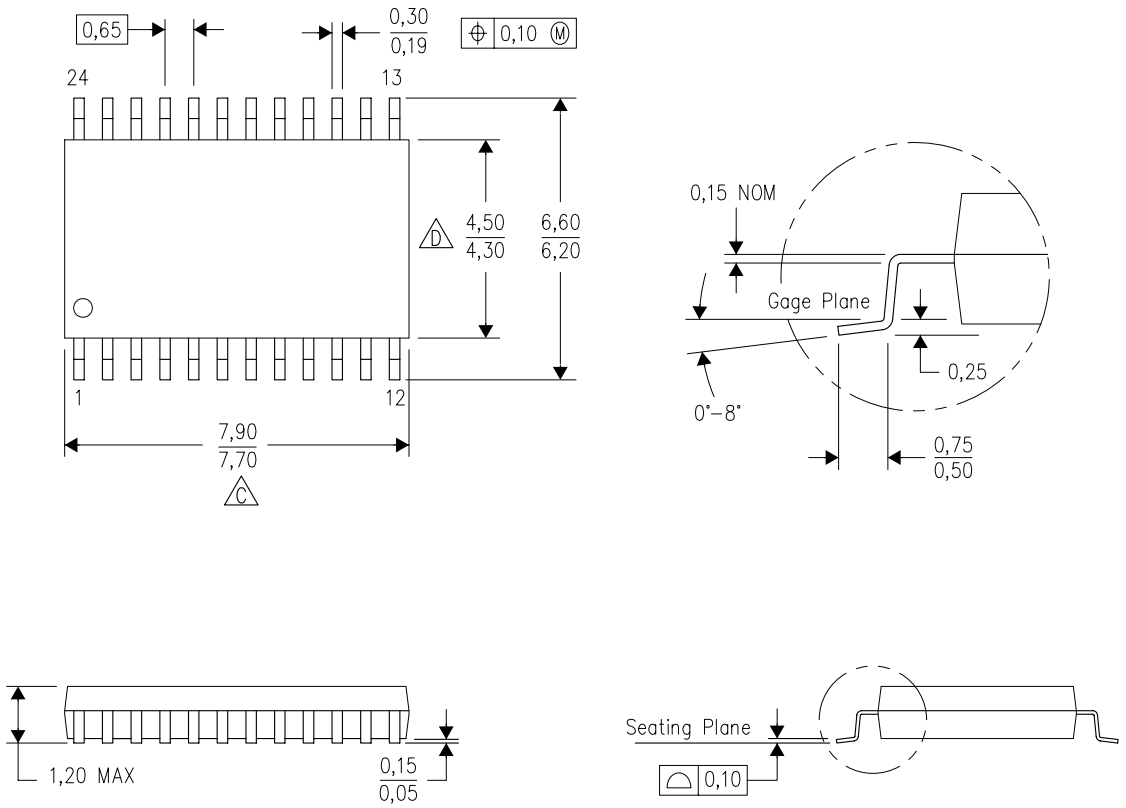
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TCA9539PWR	TSSOP	PW	24	2000	367.0	367.0	38.0
TCA9539RTWR	WQFN	RTW	24	3000	367.0	367.0	35.0

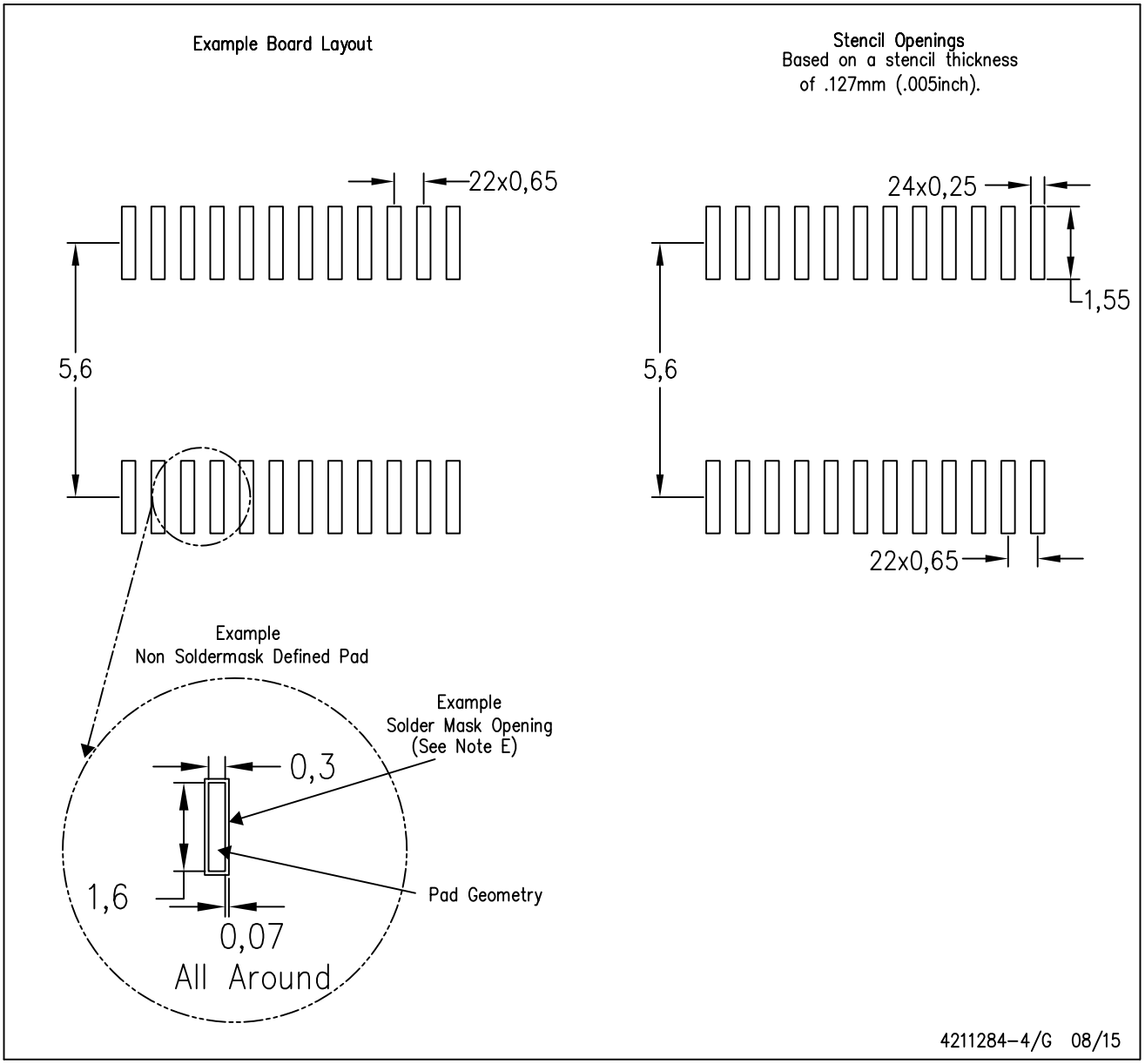
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



4040064–6/G 02/11

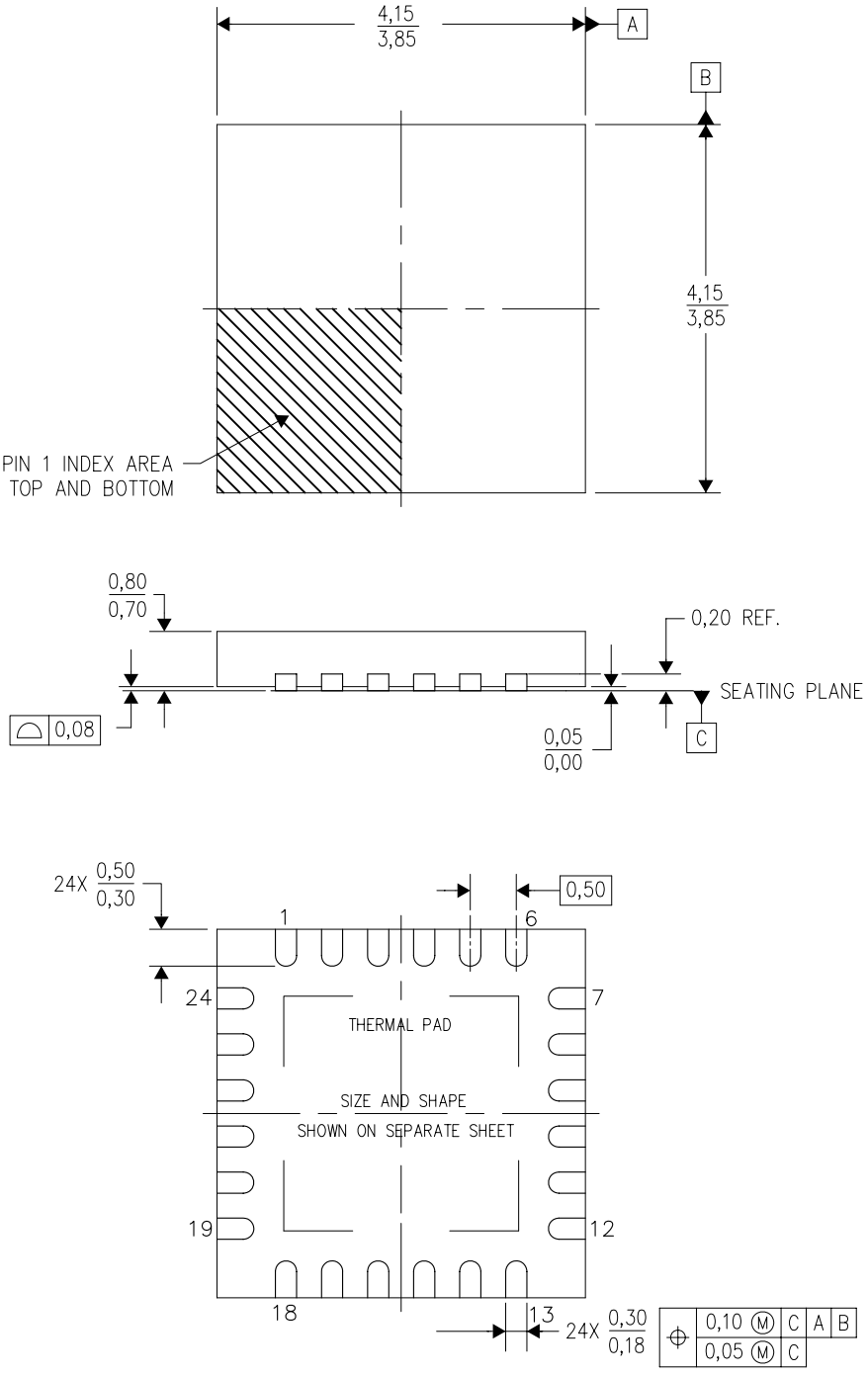
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–Leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Falls within JEDEC MO–220.

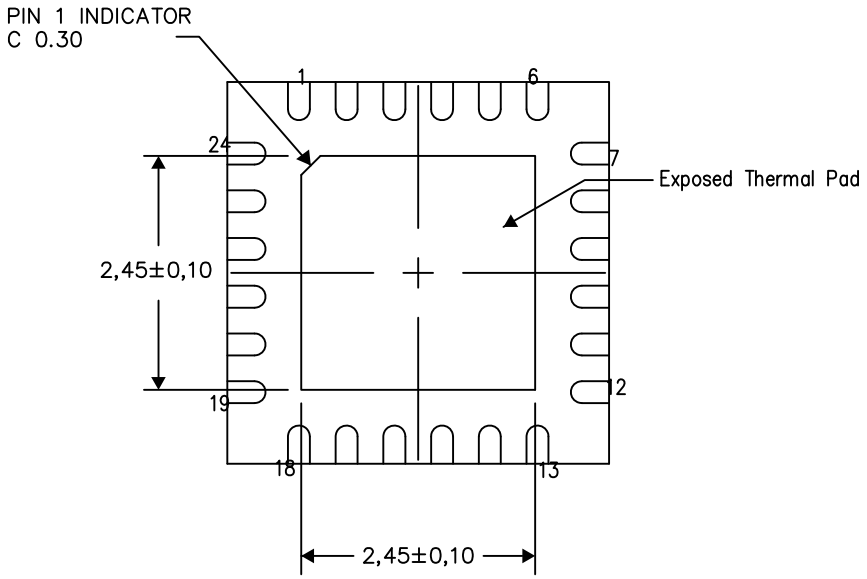
RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



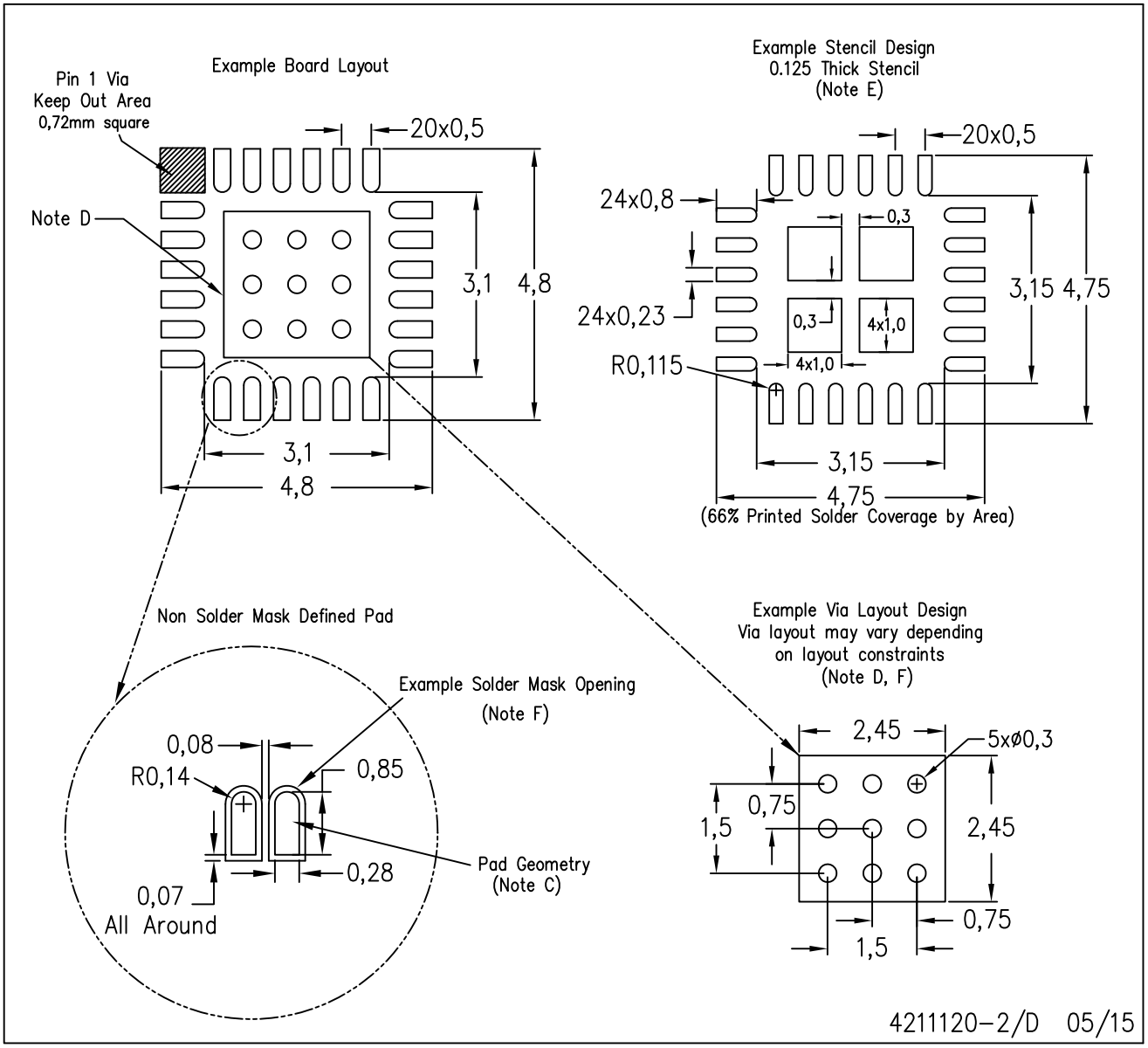
Bottom View

Exposed Thermal Pad Dimensions

4206249–3/P 05/15

NOTES: A. All linear dimensions are in millimeters

RTW (S–PWQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for recommended solder mask tolerances and via tenting recommendations for vias placed in the thermal pad.

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TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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Data Converters	dataconverter.ti.com	Computers and Peripherals	www.ti.com/computers
DLP® Products	www.dlp.com	Consumer Electronics	www.ti.com/consumer-apps
DSP	dsp.ti.com	Energy and Lighting	www.ti.com/energy
Clocks and Timers	www.ti.com/clocks	Industrial	www.ti.com/industrial
Interface	interface.ti.com	Medical	www.ti.com/medical
Logic	logic.ti.com	Security	www.ti.com/security
Power Mgmt	power.ti.com	Space, Avionics and Defense	www.ti.com/space-avionics-defense
Microcontrollers	microcontroller.ti.com	Video and Imaging	www.ti.com/video
RFID	www.ti-rfid.com		
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