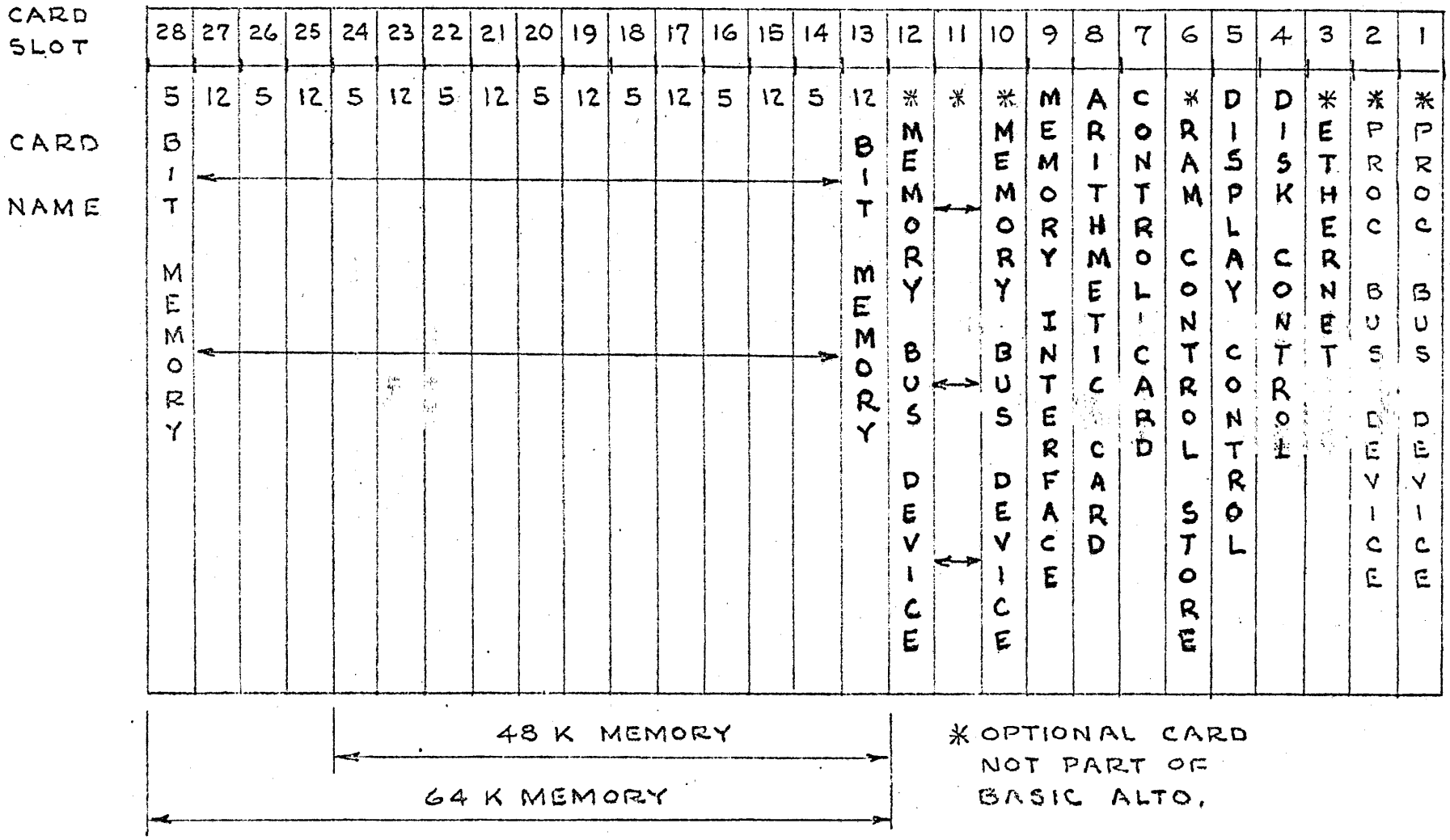
P.C. ALTO CARD ARRANGEMENT



XEROX, P.A.R.C.
1-31-72 L

* FILE CREATED 1-FEB-77 11:45:39
* ALTOBPNL MAIN WIRELIST

$$ +:								0	$
+15V:	1*7	2*7	3*7					0	1
-15V:	1*8	2*8	3*8					0	2
-5ACT:	7*102							0	3
-6ACT:	7*101							0	4
ALUF0:	7*40	8*40						0	5
ALUF1:	7*41	8*41						0	6
ALUF2:	7*42	8*42						0	7
ALUF3:	7*43	8*43						0	8
ALU[00]:	6*100	8*100	9*100					0	9
ALU[01]:	6*101	8*101	9*101					0	10
ALU[02]:	6*102	8*102	9*102					0	11
ALU[03]:	6*103	8*103	9*103					0	12
ALU[04]:	6*104	8*104	9*104					0	13
ALU[05]:	6*105	8*105	9*105					0	14
ALU[06]:	6*106	8*106	9*106					0	15
ALU[07]:	6*107	8*107	9*107					0	16
ALU[08]:	6*108	8*108	9*108					0	17
ALU[09]:	6*109	8*109	9*109					0	18
ALU[10]:	6*110	8*110	9*110					0	19
ALU[11]:	6*111	8*111	9*111					0	20
ALU[12]:	6*112	8*112	9*112					0	21
ALU[13]:	6*113	8*113	9*113					0	22
ALU[14]:	6*114	8*114	9*114					0	23
ALU[15]:	6*115	8*115	9*115					0	24
AUSYSCLK:	3*72	5*72	8*72					0	25
-AUSYSCLK:	3*12	4*75	5*8	7*70	8*8			0	26
-BLOCK:	4*110	5*110	7*110					0	27
BS0:	7*120	9*120						0	28
BS1:	7*121	9*121						0	29
BS2:	7*122	9*122						0	30
BSZ0:	7*44	8*44						0	31
BUS[00]:	1*80	2*80	3*80	4*80	5*80	6*80	7*80		
		8*80	9*80					0	32
BUS[01]:	1*81	2*81	3*81	4*81	5*81	6*81	7*81		
		8*81	9*81					0	33
BUS[02]:	1*82	2*82	3*82	4*82	5*82	6*82	7*82		
		8*82	9*82					0	34

BUS[03]:	1*83	2*83	3*83	4*83	5*83	6*83	7*83	0	35
		8*83	9*83						
BUS[04]:	1*84	2*84	3*84	4*84	5*84	6*84	7*84	0	36
		8*84	9*84						
BUS[05]:	1*85	2*85	3*85	4*85	5*85	6*85	7*85	0	37
		8*85	9*85						
BUS[06]:	1*86	2*86	3*86	4*86	5*86	6*86	7*86	0	38
		8*86	9*86						
BUS[07]:	1*87	2*87	3*87	4*87	5*87	6*87	7*87	0	39
		8*87	9*87						
BUS[08]:	1*88	2*88	3*88	4*88	5*88	6*88	7*88	0	40
		8*88	9*88						
BUS[09]:	1*89	2*89	3*89	4*89	5*89	6*89	7*89	0	41
		8*89	9*89						
BUS[10]:	1*90	2*90	3*90	4*90	5*90	6*90	7*90	0	42
		8*90	9*90						
BUS[11]:	1*91	2*91	3*91	4*91	5*91	6*91	7*91	0	43
		8*91	9*91						
BUS[12]:	1*92	2*92	3*92	4*92	5*92	6*92	7*92	0	44
		8*92	9*92						
BUS[13]:	1*93	2*93	3*93	4*93	5*93	6*93	7*93	0	45
		8*93	9*93						
BUS[14]:	1*94	2*94	3*94	4*94	5*94	6*94	7*94	0	46
		8*94	9*94						
BUS[15]:	1*95	2*95	3*95	4*95	5*95	6*95	7*95	0	47
		8*95	9*95						
CARRY:	8*73							0	48
-CE:	9*14	13*75	14*75	15*75	16*75	17*75	18*75		
		19*75	20*75	21*75	22*75	23*75	24*75		
		25*75	26*75	27*75	28*75			0	49
-CONST←:	6*97	7*97	9*97					0	50
-CS0:	9*15	13*76	14*76	15*76	16*76			0	51
-CS1:	9*75	17*76	18*76	19*76	20*76			0	52
-CS2:	9*76	21*76	22*76	23*76	24*76			0	53
-CS3:	9*77	25*76	26*76	27*76	28*76			0	54
CSYSCLK:	5*70							0	55
-CURTAC:	5*114	7*114						0	56
DBARC:	1*63	2*63	3*63	5*63	6*63	7*63		0	57
DBSYSCLK:	5*62	6*62	7*62					0	58
DCLK:	5*10							0	59
DDR←:	5*6	7*6						0	60
-DHTAC:	5*23	7*23						0	61
DNS:	7*75	8*75						0	62
-DS0:	9*19	13*79	14*79	17*79	18*79	21*79	22*79		
		25*79	26*79					0	63
-DS1:	9*18	15*79	16*79	19*79	20*79	23*79	24*79		
		27*79	28*79					0	64
-DVTAC:	5*22	7*22						0	65

170 NS
1.2 µS

-DWTAC:	5*24	7*24						0	66
EMACT:	3*99	6*99	7*99	8*99				0	67
-ETAC:	3*100	7*100						0	68
F1[0]:	1*30	2*30	3*30	4*30	7*30			0	69
F1[1]:	1*31	2*31	3*31	4*31	7*31			0	70
F1[2]:	1*32	2*32	3*32	4*32	7*32			0	71
F1[3]:	1*33	2*33	3*33	4*33	7*33			0	72
-F2EQ10:	5*51	7*51						0	73
-F2EQ11:	5*116	7*116	8*116					0	74
F2[0]:	1*36	2*36	3*36	4*36	7*36	8*36		0	75
F2[1]:	1*37	2*37	3*37	4*37	7*37	8*37		0	76
F2[2]:	1*38	2*38	3*38	4*38	7*38	8*38		0	77
F2[3]:	1*39	2*39	3*39	4*39	7*39			0	78
IBUSY:	3*113							0	79
-IR[00]:	7*10	8*10						0	80
-IR[01]:	7*11	7*12	8*11	8*12				0	81
-IR[03]:	7*13	8*13						0	82
-IR[04]:	7*14	8*14						0	83
-IR[05]:	7*15	8*15						0	84
-IR[06]:	7*16	8*16						0	85
-IR[07]:	7*78	8*78						0	86
-IR[08]:	7*18	8*18						0	87
-IR[09]:	7*19	8*19						0	88
-IR[10]:	8*20							0	89
-IR[11]:	8*21							0	90
-IR[12]:	8*22	8*23						0	91
-IR[14]:	8*24							0	92
-IR[15]:	8*25							0	93
IR←:	7*71	8*71						0	94
-KSTAC:	4*28	7*28						0	95
KSYSCLK:	4*7	5*7						0	96
-KWDTAC:	4*25	7*25						0	97
LALUC0:	7*49	8*49						0	98
-LCY8:	7*48	8*48						0	99
LOADL:	7*7	8*7						0	100
LOADR:	7*68	8*68						0	101
-LOADT:	7*69	8*69						0	102
-LSH1:	7*46	8*46						0	103
MAR[05]:	9*40	13*101	14*101	15*101	16*101	17*101	18*101		
		19*101	20*101	21*101	22*101	23*101	24*101		
		25*101	26*101	27*101	28*101			0	104

```
MAR[06]:    9*39    13*100  14*100  15*100  16*100  17*100  18*100
                    19*100  20*100  21*100  22*100  23*100  24*100
                    25*100  26*100  27*100  28*100                  0     105

MAR[07]:    9*41    10*41   11*41   12*41   13*102  14*102  15*102
                    16*102  17*102  18*102  19*102  20*102  21*102
                    22*102  23*102  24*102  25*102  26*102  27*102
                    28*102                                   0     106

MAR[08]:    9*42    10*42   11*42   12*42   13*103  14*103  15*103
                    16*103  17*103  18*103  19*103  20*103  21*103
                    22*103  23*103  24*103  25*103  26*103  27*103
                    28*103                                   0     107

MAR[09]:    9*50    10*50   11*50   12*50   13*111  14*111  15*111
                    16*111  17*111  18*111  19*111  20*111  21*111
                    22*111  23*111  24*111  25*111  26*111  27*111
                    28*111                                   0     108

MAR[10]:    9*52    10*52   11*52   12*52   13*113  14*113  15*113
                    16*113  17*113  18*113  19*113  20*113  21*113
                    22*113  23*113  24*113  25*113  26*113  27*113
                    28*113                                   0     109

MAR[11]:    9*44    10*44   11*44   12*44   13*105  14*105  15*105
                    16*105  17*105  18*105  19*105  20*105  21*105
                    22*105  23*105  24*105  25*105  26*105  27*105
                    28*105                                   0     110

MAR[12]:    9*51    10*51   11*51   12*51   13*112  14*112  15*112
                    16*112  17*112  18*112  19*112  20*112  21*112
                    22*112  23*112  24*112  25*112  26*112  27*112
                    28*112                                   0     111

MAR[13]:    9*46    10*46   11*46   12*46   13*106  14*106  15*106
                    16*106  17*106  18*106  19*106  20*106  21*106
                    22*106  23*106  24*106  25*106  26*106  27*106
                    28*106                                   0     112

MAR[14]:    9*43    10*43   11*43   12*43   13*104  14*104  15*104
                    16*104  17*104  18*104  19*104  20*104  21*104
                    22*104  23*104  24*104  25*104  26*104  27*104
                    28*104                                   0     113

MAR←:       7*72    9*72                                     0     114

-MD[00]:    9*20    10*20   11*20   12*20   13*81   13*85   15*81
                    15*85   17*81   17*85   19*81   19*85   21*81
                    21*85   23*81   23*85   25*81   25*85   27*81
                    27*85                                    0     115

-MD[01]:    9*21    10*21   11*21   12*21   13*82   13*84   15*82
                    15*84   17*82   17*84   19*82   19*84   21*82
                    21*84   23*82   23*84   25*82   25*84   27*82
                    27*84                                    0     116

-MD[02]:    9*22    10*22   11*22   12*22   13*80   13*86   15*80
                    15*86   17*80   17*86   19*80   19*86   21*80
                    21*86   23*80   23*86   25*80   25*86   27*80
                    27*86                                    0     117

-MD[03]:    9*23    10*23   11*23   12*23   13*83   13*87   15*83
                    15*87   17*83   17*87   19*83   19*87   21*83
                    21*87   23*83   23*87   25*83   25*87   27*83
                    27*87                                    0     118

-MD[04]:    9*24    10*24   11*24   12*24   13*88   13*90   15*88
                    15*90   17*88   17*90   19*88   19*90   21*88
                    21*90   23*88   23*90   25*88   25*90   27*88
                    27*90                                    0     119

-MD[05]:    9*25    10*25   11*25   12*25   13*89   13*91   15*89
                    15*91   17*89   17*91   19*89   19*91   21*89
                    21*91   23*89   23*91   25*89   25*91   27*89
                    27*91                                    0     120
```

-MD[06]:	9*26	10*26	11*26	12*26	13*93	13*94	15*93		
		15*94	17*93	17*94	19*93	19*94	21*93		
		21*94	23*93	23*94	25*93	25*94	27*93		
		27*94						0	121
-MD[07]:	9*28	10*28	11*28	12*28	13*92	13*95	15*92		
		15*95	17*92	17*95	19*92	19*95	21*92		
		21*95	23*92	23*95	25*92	25*95	27*92		
		27*95						0	122
-MD[08]:	9*29	10*29	11*29	12*29	13*96	13*107	15*96		
		15*107	17*96	17*107	19*96	19*107	21*96		
		21*107	23*96	23*107	25*96	25*107	27*96		
		27*107						0	123
-MD[09]:	9*30	10*30	11*30	12*30	13*97	13*108	15*97		
		15*108	17*97	17*108	19*97	19*108	21*97		
		21*108	23*97	23*108	25*97	25*108	27*97		
		27*108						0	124
-MD[10]:	9*31	10*31	11*31	12*31	13*98	13*109	15*98		
		15*109	17*98	17*109	19*98	19*109	21*98		
		21*109	23*98	23*109	25*98	25*109	27*98		
		27*109						0	125
-MD[11]:	9*32	10*32	11*32	12*32	13*99	13*110	15*99		
		15*110	17*99	17*110	19*99	19*110	21*99		
		21*110	23*99	23*110	25*99	25*110	27*99		
		27*110						0	126
-MD[12]:	9*33	10*33	11*33	12*33	14*92	14*95	16*92		
		16*95	18*92	18*95	20*92	20*95	22*92		
		22*95	24*92	24*95	26*92	26*95	28*92		
		28*95						0	127
-MD[13]:	9*34	10*34	11*34	12*34	14*96	14*107	16*96		
		16*107	18*96	18*107	20*96	20*107	22*96		
		22*107	24*96	24*107	26*96	26*107	28*96		
		28*107						0	128
-MD[14]:	9*36	10*36	11*36	12*36	14*97	14*108	16*97		
		16*108	18*97	18*108	20*97	20*108	22*97		
		22*108	24*97	24*108	26*97	26*108	28*97		
		28*108						0	129
-MD[15]:	9*37	10*37	11*37	12*37	14*98	14*109	16*98		
		16*109	18*98	18*109	20*98	20*109	22*98		
		22*109	24*98	24*109	26*98	26*109	28*98		
		28*109						0	130
MIARC:	5*71	9*71	10*71	11*71	12*71			0	131
MISYSCLK:	5*69	9*69	10*69	11*69	12*69			0	132
-NEXT[05]:	1*105	2*105	4*105	7*105				0	133
-NEXT[06]:	1*106	2*106	3*106	4*106	7*106			0	134
-NEXT[07]:	1*107	2*107	3*107	4*107	7*107			0	135
-NEXT[08]:	1*108	2*108	4*108	7*108				0	136
-NEXT[09]:	1*109	2*109	4*109	5*109	7*109			0	137
OBUSY:	3*114							0	138
OKTORUN:	1*1	2*1	3*1	4*1	6*1			0	139
-PARTAC:	7*61	9*61						0	140
-PC:	9*13	13*74	14*74	15*74	16*74	17*74	18*74		
		19*74	20*74	21*74	22*74	23*74	24*74		
		25*74	26*74	27*74	28*74			0	141
-READMOUS:	7*117	9*117						0	142
READPAR:	9*38	14*99	16*99	18*99	20*99	22*99	24*99		
		26*99	28*99					0	143

RESET:	1*2	2*2	3*2	4*2	6*2	7*2	9*2	0	144
RS0:	9*16	13*77	14*77	15*77	16*77	17*77	18*77		
		19*77	20*77	21*77	22*77	23*77	24*77		
		25*77	26*77	27*77	28*77			0	145
RS1:	9*12	13*73	14*73	15*73	16*73	17*73	18*73		
		19*73	20*73	21*73	22*73	23*73	24*73		
		25*73	26*73	27*73	28*73			0	146
RS2:	9*10	13*71	14*71	15*71	16*71	17*71	18*71		
		19*71	20*71	21*71	22*71	23*71	24*71		
		25*71	26*71	27*71	28*71			0	147
RS3:	9*70	13*70	14*70	15*70	16*70	17*70	18*70		
		19*70	20*70	21*70	22*70	23*70	24*70		
		25*70	26*70	27*70	28*70			0	148
RS4:	9*8	13*69	14*69	15*69	16*69	17*69	18*69		
		19*69	20*69	21*69	22*69	23*69	24*69		
		25*69	26*69	27*69	28*69			0	149
RS5:	9*11	13*72	14*72	15*72	16*72	17*72	18*72		
		19*72	20*72	21*72	22*72	23*72	24*72		
		25*72	26*72	27*72	28*72			0	150
RS6:	9*7	13*68	14*68	15*68	16*68	17*68	18*68		
		19*68	20*68	21*68	22*68	23*68	24*68		
		25*68	26*68	27*68	28*68			0	151
RS7:	9*6	13*67	14*67	15*67	16*67	17*67	18*67		
		19*67	20*67	21*67	22*67	23*67	24*67		
		25*67	26*67	27*67	28*67			0	152
RSEL0:	7*54	8*54	9*54					0	153
RSEL1:	7*55	8*55	9*55					0	154
RSEL2:	7*56	8*56	9*56					0	155
RSEL3:	7*57	8*57	9*57					0	156
RSEL4:	7*59	8*59	9*59					0	157
-RSH1:	7*47	8*47						0	158
-RSN:	3*42							0	159
SELR37:	7*74	9*74						0	160
SHZERO:	7*26	8*26						0	161
SH[00]:	7*50	8*50						0	162
-SIO:	3*41							0	163
SKIP:	8*74							0	164
SN[00]:	3*18							0	165
SN[01]:	3*19							0	166
SN[02]:	3*20							0	167
SN[03]:	3*21							0	168
SN[04]:	3*22							0	169
SN[05]:	3*23							0	170
SN[06]:	3*24							0	171
SN[07]:	3*25							0	172
-SRESET:	1*62	2*62	3*62	4*62	7*1	9*62		0	173
-STOP:	5*1	9*1						0	174
STOPCLK:	5*20	7*20						0	175

-STORE:	7*73	9*73						0	176
-SWAKMRT:	3*68	5*68	9*68					0	177
-W0:	9*79	13*78	14*78	17*78	18*78	21*78	22*78		
		25*78	26*78					0	178
-W1:	9*78	15*78	16*78	19*78	20*78	23*78	24*78		
		27*78	28*78					0	179
-WAKE5:	7*60							0	180
-WAKE6:	7*104							0	181
WAKECURT:	5*115	7*115						0	182
-WAKEDHT:	5*77	7*77						0	183
-WAKEDVT:	5*76	7*76						0	184
-WAKEDWT:	5*21	7*21						0	185
-WAKEET:	3*103	7*103						0	186
-WAKEKST:	4*8	7*8						0	187
-WAKEKWDT:	4*79	7*79						0	188
-WAKEMRT:	7*67	9*67						0	189
-WAKEPART:	7*118	9*118						0	190
WRITEPAR:	9*49	14*110	16*110	18*110	20*110	22*110	24*110		
		26*110	28*110					0	191
XIOREF:	9*48	10*48	11*48	12*48				0	192
XMAR[15]:	9*47	10*47	11*47	12*47				0	193
XMT2:	9*98	10*98	11*98	12*98				0	194
-ZEROBUS:	7*34	8*34						0	195
←DISP:	7*98	8*98						0	196
-←KDATA:	3*111	4*111	7*111					0	197
-←KSTAT:	4*112	7*112						0	198
-←MD:	7*96	9*96						0	199

* This card uses 1058 wires
↑L

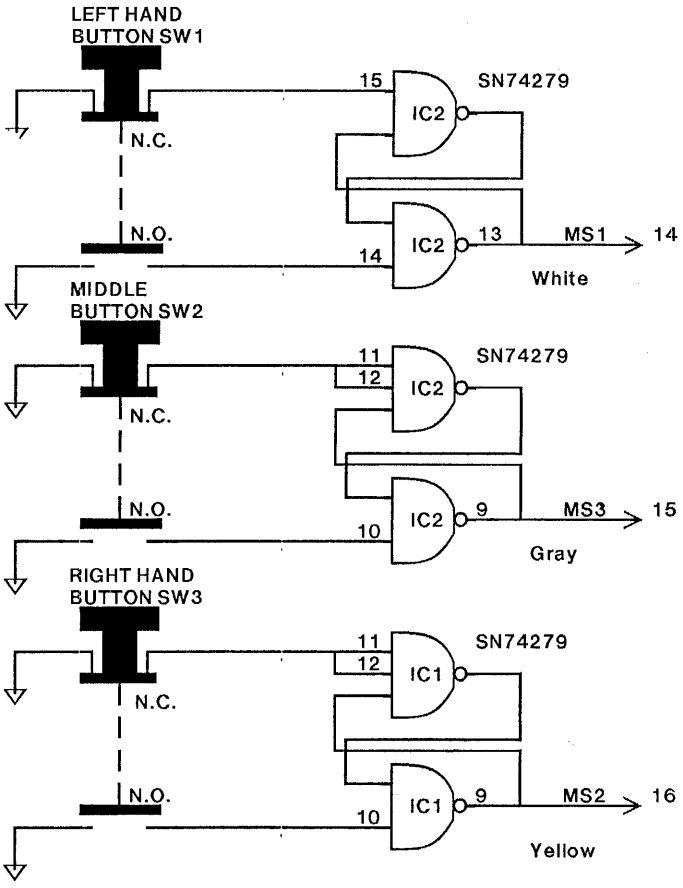
1*1	OKTORUN	1*2	RESET	1*7	+15V	1*8	-15V
1*30	F1[0]	1*31	F1[1]	1*32	F1[2]	1*33	F1[3]
1*36	F2[0]	1*37	F2[1]	1*38	F2[2]	1*39	F2[3]
1*62	-SRESET	1*63	DBARC	1*80	BUS[00]	1*81	BUS[01]
1*82	BUS[02]	1*83	BUS[03]	1*84	BUS[04]	1*85	BUS[05]
1*86	BUS[06]	1*87	BUS[07]	1*88	BUS[08]	1*89	BUS[09]
1*90	BUS[10]	1*91	BUS[11]	1*92	BUS[12]	1*93	BUS[13]
1*94	BUS[14]	1*95	BUS[15]	1*105	-NEXT[05]	1*106	-NEXT[06]
1*107	-NEXT[07]	1*108	-NEXT[08]	1*109	-NEXT[09]	2*1	OKTORUN
2*2	RESET	2*7	+15V	2*8	-15V	2*30	F1[0]
2*31	F1[1]	2*32	F1[2]	2*33	F1[3]	2*36	F2[0]
2*37	F2[1]	2*38	F2[2]	2*39	F2[3]	2*62	-SRESET
2*63	DBARC	2*80	BUS[00]	2*81	BUS[01]	2*82	BUS[02]
2*83	BUS[03]	2*84	BUS[04]	2*85	BUS[05]	2*86	BUS[06]
2*87	BUS[07]	2*88	BUS[08]	2*89	BUS[09]	2*90	BUS[10]
2*91	BUS[11]	2*92	BUS[12]	2*93	BUS[13]	2*94	BUS[14]
2*95	BUS[15]	2*105	-NEXT[05]	2*106	-NEXT[06]	2*107	-NEXT[07]
2*108	-NEXT[08]	2*109	-NEXT[09]	3*1	OKTORUN	3*2	RESET
3*7	+15V	3*8	-15V	3*12	-AUSYSCLK	3*18	SN[00]
3*19	SN[01]	3*20	SN[02]	3*21	SN[03]	3*22	SN[04]
3*23	SN[05]	3*24	SN[06]	3*25	SN[07]	3*30	F1[0]
3*31	F1[1]	3*32	F1[2]	3*33	F1[3]	3*36	F2[0]
3*37	F2[1]	3*38	F2[2]	3*39	F2[3]	3*41	-SIO
3*42	-RSN	3*62	-SRESET	3*63	DBARC	3*68	-SWAKMRT
3*72	AUSYSCLK	3*80	BUS[00]	3*81	BUS[01]	3*82	BUS[02]
3*83	BUS[03]	3*84	BUS[04]	3*85	BUS[05]	3*86	BUS[06]
3*87	BUS[07]	3*88	BUS[08]	3*89	BUS[09]	3*90	BUS[10]
3*91	BUS[11]	3*92	BUS[12]	3*93	BUS[13]	3*94	BUS[14]
3*95	BUS[15]	3*99	EMACT	3*100	-ETAC	3*103	-WAKEET
3*106	-NEXT[06]	3*107	-NEXT[07]	3*111	-←KDATA	3*113	IBUSY
3*114	OBUSY	4*1	OKTORUN	4*2	RESET	4*7	KSYSCLK
4*8	-WAKEKST	4*25	-KWDTAC	4*28	-KSTAC	4*30	F1[0]
4*31	F1[1]	4*32	F1[2]	4*33	F1[3]	4*36	F2[0]
4*37	F2[1]	4*38	F2[2]	4*39	F2[3]	4*62	-SRESET
4*75	-AUSYSCLK	4*79	-WAKEKWDT	4*80	BUS[00]	4*81	BUS[01]
4*82	BUS[02]	4*83	BUS[03]	4*84	BUS[04]	4*85	BUS[05]
4*86	BUS[06]	4*87	BUS[07]	4*88	BUS[08]	4*89	BUS[09]
4*90	BUS[10]	4*91	BUS[11]	4*92	BUS[12]	4*93	BUS[13]
4*94	BUS[14]	4*95	BUS[15]	4*105	-NEXT[05]	4*106	-NEXT[06]
4*107	-NEXT[07]	4*108	-NEXT[08]	4*109	-NEXT[09]	4*110	-BLOCK
4*111	-←KDATA	4*112	-←KSTAT	5*1	-STOP	5*6	DDR←
5*7	KSYSCLK	5*8	-AUSYSCLK	5*10	DCLK	5*20	STOPCLK
5*21	-WAKEDWT	5*22	-DVTAC	5*23	-DHTAC	5*24	-DWTAC
5*51	-F2EQ10	5*62	DBSYSCLK	5*63	DBARC	5*68	-SWAKMRT
5*69	MISYSCLK	5*70	CSYSCLK	5*71	MIARC	5*72	AUSYSCLK
5*76	-WAKEDVT	5*77	-WAKEDHT	5*80	BUS[00]	5*81	BUS[01]
5*82	BUS[02]	5*83	BUS[03]	5*84	BUS[04]	5*85	BUS[05]
5*86	BUS[06]	5*87	BUS[07]	5*88	BUS[08]	5*89	BUS[09]
5*90	BUS[10]	5*91	BUS[11]	5*92	BUS[12]	5*93	BUS[13]
5*94	BUS[14]	5*95	BUS[15]	5*109	-NEXT[09]	5*110	-BLOCK
5*114	-CURTAC	5*115	WAKECURT	5*116	-F2EQ11	6*1	OKTORUN
6*2	RESET	6*62	DBSYSCLK	6*63	DBARC	6*80	BUS[00]
6*81	BUS[01]	6*82	BUS[02]	6*83	BUS[03]	6*84	BUS[04]
6*85	BUS[05]	6*86	BUS[06]	6*87	BUS[07]	6*88	BUS[08]
6*89	BUS[09]	6*90	BUS[10]	6*91	BUS[11]	6*92	BUS[12]
6*93	BUS[13]	6*94	BUS[14]	6*95	BUS[15]	6*97	-CONST←
6*99	EMACT	6*100	ALU[00]	6*101	ALU[01]	6*102	ALU[02]
6*103	ALU[03]	6*104	ALU[04]	6*105	ALU[05]	6*106	ALU[06]
6*107	ALU[07]	6*108	ALU[08]	6*109	ALU[09]	6*110	ALU[10]
6*111	ALU[11]	6*112	ALU[12]	6*113	ALU[13]	6*114	ALU[14]
6*115	ALU[15]	7*1	-SRESET	7*2	RESET	7*6	DDR←
7*7	LOADL	7*8	-WAKEKST	7*10	-IR[00]	7*11	-IR[01]
7*12	-IR[01]	7*13	-IR[03]	7*14	-IR[04]	7*15	-IR[05]
7*16	-IR[06]	7*18	-IR[08]	7*19	-IR[09]	7*20	STOPCLK
7*21	-WAKEDWT	7*22	-DVTAC	7*23	-DHTAC	7*24	-DWTAC
7*25	-KWDTAC	7*26	SHZERO	7*28	-KSTAC	7*30	F1[0]
7*31	F1[1]	7*32	F1[2]	7*33	F1[3]	7*34	-ZEROBUS
7*36	F2[0]	7*37	F2[1]	7*38	F2[2]	7*39	F2[3]
7*40	ALUF0	7*41	ALUF1	7*42	ALUF2	7*43	ALUF3
7*44	BSZ0	7*46	-LSH1	7*47	-RSH1	7*48	-LCY8
7*49	LALUC0	7*50	SH[00]	7*51	-F2EQ10	7*54	RSEL0
7*55	RSEL1	7*56	RSEL2	7*57	RSEL3	7*59	RSEL4
7*60	-WAKE5	7*61	-PARTAC	7*62	DBSYSCLK	7*63	DBARC
7*67	-WAKEMRT	7*68	LOADR	7*69	-LOADT	7*70	-AUSYSCLK
7*71	IR←	7*72	MAR←	7*73	-STORE	7*74	SELR37
7*75	DNS	7*76	-WAKEDVT	7*77	-WAKEDHT	7*78	-IR[07]
7*79	-WAKEKWDT	7*80	BUS[00]	7*81	BUS[01]	7*82	BUS[02]
7*83	BUS[03]	7*84	BUS[04]	7*85	BUS[05]	7*86	BUS[06]
7*87	BUS[07]	7*88	BUS[08]	7*89	BUS[09]	7*90	BUS[10]

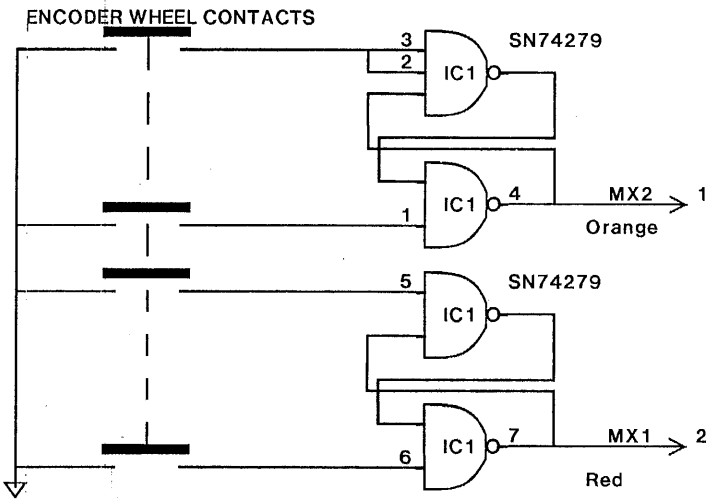
7*91	BUS[11]	7*92	BUS[12]	7*93	BUS[13]	7*94	BUS[14]
7*95	BUS[15]	7*96	-←MD	7*97	-CONST←	7*98	←DISP
7*99	EMACT	7*100	-ETAC	7*101	-6ACT	7*102	-5ACT
7*103	-WAKEET	7*104	-WAKE6	7*105	-NEXT[05]	7*106	-NEXT[06]
7*107	-NEXT[07]	7*108	-NEXT[08]	7*109	-NEXT[09]	7*110	-BLOCK
7*111	-←KDATA	7*112	-←KSTAT	7*114	-CURTAC	7*115	WAKECURT
7*116	-F2EQ11	7*117	-READMOUS	7*118	-WAKEPART	7*120	BS0
7*121	BS1	7*122	BS2	8*7	LOADL	8*8	-AUSYSCLK
8*10	-IR[00]	8*11	-IR[01]	8*12	-IR[01]	8*13	-IR[03]
8*14	-IR[04]	8*15	-IR[05]	8*16	-IR[06]	8*18	-IR[08]
8*19	-IR[09]	8*20	-IR[10]	8*21	-IR[11]	8*22	-IR[12]
8*23	-IR[12]	8*24	-IR[14]	8*25	-IR[15]	8*26	SHZERO
8*34	-ZEROBUS	8*36	F2[0]	8*37	F2[1]	8*38	F2[2]
8*40	ALUF0	8*41	ALUF1	8*42	ALUF2	8*43	ALUF3
8*44	BSZ0	8*46	-LSH1	8*47	-RSH1	8*48	-LCY8
8*49	LALUC0	8*50	SH[00]	8*54	RSEL0	8*55	RSEL1
8*56	RSEL2	8*57	RSEL3	8*59	RSEL4	8*68	LOADR
8*69	-LOADT	8*71	IR←	8*72	AUSYSCLK	8*73	CARRY
8*74	SKIP	8*75	DNS	8*78	-IR[07]	8*80	BUS[00]
8*81	BUS[01]	8*82	BUS[02]	8*83	BUS[03]	8*84	BUS[04]
8*85	BUS[05]	8*86	BUS[06]	8*87	BUS[07]	8*88	BUS[08]
8*89	BUS[09]	8*90	BUS[10]	8*91	BUS[11]	8*92	BUS[12]
8*93	BUS[13]	8*94	BUS[14]	8*95	BUS[15]	8*98	←DISP
8*99	EMACT	8*100	ALU[00]	8*101	ALU[01]	8*102	ALU[02]
8*103	ALU[03]	8*104	ALU[04]	8*105	ALU[05]	8*106	ALU[06]
8*107	ALU[07]	8*108	ALU[08]	8*109	ALU[09]	8*110	ALU[10]
8*111	ALU[11]	8*112	ALU[12]	8*113	ALU[13]	8*114	ALU[14]
8*115	ALU[15]	8*116	-F2EQ11	9*1	-STOP	9*2	RESET
9*6	RS7	9*7	RS6	9*8	RS4	9*10	RS2
9*11	RS5	9*12	RS1	9*13	-PC	9*14	-CE
9*15	-CS0	9*16	RS0	9*18	-DS1	9*19	-DS0
9*20	-MD[00]	9*21	-MD[01]	9*22	-MD[02]	9*23	-MD[03]
9*24	-MD[04]	9*25	-MD[05]	9*26	-MD[06]	9*28	-MD[07]
9*29	-MD[08]	9*30	-MD[09]	9*31	-MD[10]	9*32	-MD[11]
9*33	-MD[12]	9*34	-MD[13]	9*36	-MD[14]	9*37	-MD[15]
9*38	READPAR	9*39	MAR[06]	9*40	MAR[05]	9*41	MAR[07]
9*42	MAR[08]	9*43	MAR[14]	9*44	MAR[11]	9*46	MAR[13]
9*47	XMAR[15]	9*48	XIOREF	9*49	WRITEPAR	9*50	MAR[09]
9*51	MAR[12]	9*52	MAR[10]	9*54	RSEL0	9*55	RSEL1
9*56	RSEL2	9*57	RSEL3	9*59	RSEL4	9*61	-PARTAC
9*62	-SRESET	9*67	-WAKEMRT	9*68	-SWAKMRT	9*69	MISYSCLK
9*70	RS3	9*71	MIARC	9*72	MAR←	9*73	-STORE
9*74	SELR37	9*75	-CS1	9*76	-CS2	9*77	-CS3
9*78	-W1	9*79	-W0	9*80	BUS[00]	9*81	BUS[01]
9*82	BUS[02]	9*83	BUS[03]	9*84	BUS[04]	9*85	BUS[05]
9*86	BUS[06]	9*87	BUS[07]	9*88	BUS[08]	9*89	BUS[09]
9*90	BUS[10]	9*91	BUS[11]	9*92	BUS[12]	9*93	BUS[13]
9*94	BUS[14]	9*95	BUS[15]	9*96	-←MD	9*97	-CONST←
9*98	XMT2	9*100	ALU[00]	9*101	ALU[01]	9*102	ALU[02]
9*103	ALU[03]	9*104	ALU[04]	9*105	ALU[05]	9*106	ALU[06]
9*107	ALU[07]	9*108	ALU[08]	9*109	ALU[09]	9*110	ALU[10]
9*111	ALU[11]	9*112	ALU[12]	9*113	ALU[13]	9*114	ALU[14]
9*115	ALU[15]	9*117	-READMOUS	9*118	-WAKEPART	9*120	BS0
9*121	BS1	9*122	BS2	10*20	-MD[00]	10*21	-MD[01]
10*22	-MD[02]	10*23	-MD[03]	10*24	-MD[04]	10*25	-MD[05]
10*26	-MD[06]	10*28	-MD[07]	10*29	-MD[08]	10*30	-MD[09]
10*31	-MD[10]	10*32	-MD[11]	10*33	-MD[12]	10*34	-MD[13]
10*36	-MD[14]	10*37	-MD[15]	10*41	MAR[07]	10*42	MAR[08]
10*43	MAR[14]	10*44	MAR[11]	10*46	MAR[13]	10*47	XMAR[15]
10*48	XIOREF	10*50	MAR[09]	10*51	MAR[12]	10*52	MAR[10]
10*69	MISYSCLK	10*71	MIARC	10*98	XMT2	11*20	-MD[00]
11*21	-MD[01]	11*22	-MD[02]	11*23	-MD[03]	11*24	-MD[04]
11*25	-MD[05]	11*26	-MD[06]	11*28	-MD[07]	11*29	-MD[08]
11*30	-MD[09]	11*31	-MD[10]	11*32	-MD[11]	11*33	-MD[12]
11*34	-MD[13]	11*36	-MD[14]	11*37	-MD[15]	11*41	MAR[07]
11*42	MAR[08]	11*43	MAR[14]	11*44	MAR[11]	11*46	MAR[13]
11*47	XMAR[15]	11*48	XIOREF	11*50	MAR[09]	11*51	MAR[12]
11*52	MAR[10]	11*69	MISYSCLK	11*71	MIARC	11*98	XMT2
12*20	-MD[00]	12*21	-MD[01]	12*22	-MD[02]	12*23	-MD[03]
12*24	-MD[04]	12*25	-MD[05]	12*26	-MD[06]	12*28	-MD[07]
12*29	-MD[08]	12*30	-MD[09]	12*31	-MD[10]	12*32	-MD[11]
12*33	-MD[12]	12*34	-MD[13]	12*36	-MD[14]	12*37	-MD[15]
12*41	MAR[07]	12*42	MAR[08]	12*43	MAR[14]	12*44	MAR[11]
12*46	MAR[13]	12*47	XMAR[15]	12*48	XIOREF	12*50	MAR[09]
12*51	MAR[12]	12*52	MAR[10]	12*69	MISYSCLK	12*71	MIARC
12*98	XMT2	13*67	RS7	13*68	RS6	13*69	RS4
13*70	RS3	13*71	RS2	13*72	RS5	13*73	RS1
13*74	-PC	13*75	-CE	13*76	-CS0	13*77	RS0
13*78	-W0	13*79	-DS0	13*80	-MD[02]	13*81	-MD[00]

13*82	-MD[01]	13*83	-MD[03]	13*84	-MD[01]	13*85	-MD[00]
13*86	-MD[02]	13*87	-MD[03]	13*88	-MD[04]	13*89	-MD[05]
13*90	-MD[04]	13*91	-MD[05]	13*92	-MD[07]	13*93	-MD[06]
13*94	-MD[06]	13*95	-MD[07]	13*96	-MD[08]	13*97	-MD[09]
13*98	-MD[10]	13*99	-MD[11]	13*100	MAR[06]	13*101	MAR[05]
13*102	MAR[07]	13*103	MAR[08]	13*104	MAR[14]	13*105	MAR[11]
13*106	MAR[13]	13*107	-MD[08]	13*108	-MD[09]	13*109	-MD[10]
13*110	-MD[11]	13*111	MAR[09]	13*112	MAR[12]	13*113	MAR[10]
14*67	RS7	14*68	RS6	14*69	RS4	14*70	RS3
14*71	RS2	14*72	RS5	14*73	RS1	14*74	-PC
14*75	-CE	14*76	-CS0	14*77	RS0	14*78	-W0
14*79	-DS0	14*92	-MD[12]	14*95	-MD[12]	14*96	-MD[13]
14*97	-MD[14]	14*98	-MD[15]	14*99	READPAR	14*100	MAR[06]
14*101	MAR[05]	14*102	MAR[07]	14*103	MAR[08]	14*104	MAR[14]
14*105	MAR[11]	14*106	MAR[13]	14*107	-MD[13]	14*108	-MD[14]
14*109	-MD[15]	14*110	WRITEPAR	14*111	MAR[09]	14*112	MAR[12]
14*113	MAR[10]	15*67	RS7	15*68	RS6	15*69	RS4
15*70	RS3	15*71	RS2	15*72	RS5	15*73	RS1
15*74	-PC	15*75	-CE	15*76	-CS0	15*77	RS0
15*78	-W1	15*79	-DS1	15*80	-MD[02]	15*81	-MD[00]
15*82	-MD[01]	15*83	-MD[03]	15*84	-MD[01]	15*85	-MD[00]
15*86	-MD[02]	15*87	-MD[03]	15*88	-MD[04]	15*89	-MD[05]
15*90	-MD[04]	15*91	-MD[05]	15*92	-MD[07]	15*93	-MD[06]
15*94	-MD[06]	15*95	-MD[07]	15*96	-MD[08]	15*97	-MD[09]
15*98	-MD[10]	15*99	-MD[11]	15*100	MAR[06]	15*101	MAR[05]
15*102	MAR[07]	15*103	MAR[08]	15*104	MAR[14]	15*105	MAR[11]
15*106	MAR[13]	15*107	-MD[08]	15*108	-MD[09]	15*109	-MD[10]
15*110	-MD[11]	15*111	MAR[09]	15*112	MAR[12]	15*113	MAR[10]
16*67	RS7	16*68	RS6	16*69	RS4	16*70	RS3
16*71	RS2	16*72	RS5	16*73	RS1	16*74	-PC
16*75	-CE	16*76	-CS0	16*77	RS0	16*78	-W1
16*79	-DS1	16*92	-MD[12]	16*95	-MD[12]	16*96	-MD[13]
16*97	-MD[14]	16*98	-MD[15]	16*99	READPAR	16*100	MAR[06]
16*101	MAR[05]	16*102	MAR[07]	16*103	MAR[08]	16*104	MAR[14]
16*105	MAR[11]	16*106	MAR[13]	16*107	-MD[13]	16*108	-MD[14]
16*109	-MD[15]	16*110	WRITEPAR	16*111	MAR[09]	16*112	MAR[12]
16*113	MAR[10]	17*67	RS7	17*68	RS6	17*69	RS4
17*70	RS3	17*71	RS2	17*72	RS5	17*73	RS1
17*74	-PC	17*75	-CE	17*76	-CS1	17*77	RS0
17*78	-W0	17*79	-DS0	17*80	-MD[02]	17*81	-MD[00]
17*82	-MD[01]	17*83	-MD[03]	17*84	-MD[01]	17*85	-MD[00]
17*86	-MD[02]	17*87	-MD[03]	17*88	-MD[04]	17*89	-MD[05]
17*90	-MD[04]	17*91	-MD[05]	17*92	-MD[07]	17*93	-MD[06]
17*94	-MD[06]	17*95	-MD[07]	17*96	-MD[08]	17*97	-MD[09]
17*98	-MD[10]	17*99	-MD[11]	17*100	MAR[06]	17*101	MAR[05]
17*102	MAR[07]	17*103	MAR[08]	17*104	MAR[14]	17*105	MAR[11]
17*106	MAR[13]	17*107	-MD[08]	17*108	-MD[09]	17*109	-MD[10]
17*110	-MD[11]	17*111	MAR[09]	17*112	MAR[12]	17*113	MAR[10]
18*67	RS7	18*68	RS6	18*69	RS4	18*70	RS3
18*71	RS2	18*72	RS5	18*73	RS1	18*74	-PC
18*75	-CE	18*76	-CS1	18*77	RS0	18*78	-W0
18*79	-DS0	18*92	-MD[12]	18*95	-MD[12]	18*96	-MD[13]
18*97	-MD[14]	18*98	-MD[15]	18*99	READPAR	18*100	MAR[06]
18*101	MAR[05]	18*102	MAR[07]	18*103	MAR[08]	18*104	MAR[14]
18*105	MAR[11]	18*106	MAR[13]	18*107	-MD[13]	18*108	-MD[14]
18*109	-MD[15]	18*110	WRITEPAR	18*111	MAR[09]	18*112	MAR[12]
18*113	MAR[10]	19*67	RS7	19*68	RS6	19*69	RS4
19*70	RS3	19*71	RS2	19*72	RS5	19*73	RS1
19*74	-PC	19*75	-CE	19*76	-CS1	19*77	RS0
19*78	-W1	19*79	-DS1	19*80	-MD[02]	19*81	-MD[00]
19*82	-MD[01]	19*83	-MD[03]	19*84	-MD[01]	19*85	-MD[00]
19*86	-MD[02]	19*87	-MD[03]	19*88	-MD[04]	19*89	-MD[05]
19*90	-MD[04]	19*91	-MD[05]	19*92	-MD[07]	19*93	-MD[06]
19*94	-MD[06]	19*95	-MD[07]	19*96	-MD[08]	19*97	-MD[09]
19*98	-MD[10]	19*99	-MD[11]	19*100	MAR[06]	19*101	MAR[05]
19*102	MAR[07]	19*103	MAR[08]	19*104	MAR[14]	19*105	MAR[11]
19*106	MAR[13]	19*107	-MD[08]	19*108	-MD[09]	19*109	-MD[10]
19*110	-MD[11]	19*111	MAR[09]	19*112	MAR[12]	19*113	MAR[10]
20*67	RS7	20*68	RS6	20*69	RS4	20*70	RS3
20*71	RS2	20*72	RS5	20*73	RS1	20*74	-PC
20*75	-CE	20*76	-CS1	20*77	RS0	20*78	-W1
20*79	-DS1	20*92	-MD[12]	20*95	-MD[12]	20*96	-MD[13]
20*97	-MD[14]	20*98	-MD[15]	20*99	READPAR	20*100	MAR[06]
20*101	MAR[05]	20*102	MAR[07]	20*103	MAR[08]	20*104	MAR[14]
20*105	MAR[11]	20*106	MAR[13]	20*107	-MD[13]	20*108	-MD[14]
20*109	-MD[15]	20*110	WRITEPAR	20*111	MAR[09]	20*112	MAR[12]
20*113	MAR[10]	21*67	RS7	21*68	RS6	21*69	RS4
21*70	RS3	21*71	RS2	21*72	RS5	21*73	RS1
21*74	-PC	21*75	-CE	21*76	-CS2	21*77	RS0

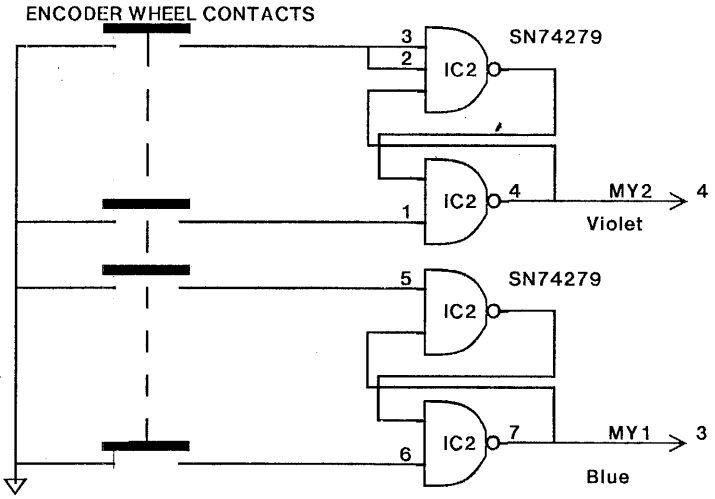
21*78 -W0	21*79 -DS0	21*80 -MD[02]	21*81 -MD[00]
21*82 -MD[01]	21*83 -MD[03]	21*84 -MD[01]	21*85 -MD[00]
21*86 -MD[02]	21*87 -MD[03]	21*88 -MD[04]	21*89 -MD[05]
21*90 -MD[04]	21*91 -MD[05]	21*92 -MD[07]	21*93 -MD[06]
21*94 -MD[06]	21*95 -MD[07]	21*96 -MD[08]	21*97 -MD[09]
21*98 -MD[10]	21*99 -MD[11]	21*100 MAR[06]	21*101 MAR[05]
21*102 MAR[07]	21*103 MAR[08]	21*104 MAR[14]	21*105 MAR[11]
21*106 MAR[13]	21*107 -MD[08]	21*108 -MD[09]	21*109 -MD[10]
21*110 -MD[11]	21*111 MAR[09]	21*112 MAR[12]	21*113 MAR[10]
22*67 RS7	22*68 RS6	22*69 RS4	22*70 RS3
22*71 RS2	22*72 RS5	22*73 RS1	22*74 -PC
22*75 -CE	22*76 -CS2	22*77 RS0	22*78 -W0
22*79 -DS0	22*92 -MD[12]	22*95 -MD[12]	22*96 -MD[13]
22*97 -MD[14]	22*98 -MD[15]	22*99 READPAR	22*100 MAR[06]
22*101 MAR[05]	22*102 MAR[07]	22*103 MAR[08]	22*104 MAR[14]
22*105 MAR[11]	22*106 MAR[13]	22*107 -MD[13]	22*108 -MD[14]
22*109 -MD[15]	22*110 WRITEPAR	22*111 MAR[09]	22*112 MAR[12]
22*113 MAR[10]	23*67 RS7	23*68 RS6	23*69 RS4
23*70 RS3	23*71 RS2	23*72 RS5	23*73 RS1
23*74 -PC	23*75 -CE	23*76 -CS2	23*77 RS0
23*78 -W1	23*79 -DS1	23*80 -MD[02]	23*81 -MD[00]
23*82 -MD[01]	23*83 -MD[03]	23*84 -MD[01]	23*85 -MD[00]
23*86 -MD[02]	23*87 -MD[03]	23*88 -MD[04]	23*89 -MD[05]
23*90 -MD[04]	23*91 -MD[05]	23*92 -MD[07]	23*93 -MD[06]
23*94 -MD[06]	23*95 -MD[07]	23*96 -MD[08]	23*97 -MD[09]
23*98 -MD[10]	23*99 -MD[11]	23*100 MAR[06]	23*101 MAR[05]
23*102 MAR[07]	23*103 MAR[08]	23*104 MAR[14]	23*105 MAR[11]
23*106 MAR[13]	23*107 -MD[08]	23*108 -MD[09]	23*109 -MD[10]
23*110 -MD[11]	23*111 MAR[09]	23*112 MAR[12]	23*113 MAR[10]
24*67 RS7	24*68 RS6	24*69 RS4	24*70 RS3
24*71 RS2	24*72 RS5	24*73 RS1	24*74 -PC
24*75 -CE	24*76 -CS2	24*77 RS0	24*78 -W1
24*79 -DS1	24*92 -MD[12]	24*95 -MD[12]	24*96 -MD[13]
24*97 -MD[14]	24*98 -MD[15]	24*99 READPAR	24*100 MAR[06]
24*101 MAR[05]	24*102 MAR[07]	24*103 MAR[08]	24*104 MAR[14]
24*105 MAR[11]	24*106 MAR[13]	24*107 -MD[13]	24*108 -MD[14]
24*109 -MD[15]	24*110 WRITEPAR	24*111 MAR[09]	24*112 MAR[12]
24*113 MAR[10]	25*67 RS7	25*68 RS6	25*69 RS4
25*70 RS3	25*71 RS2	25*72 RS5	25*73 RS1
25*74 -PC	25*75 -CE	25*76 -CS3	25*77 RS0
25*78 -W0	25*79 -DS0	25*80 -MD[02]	25*81 -MD[00]
25*82 -MD[01]	25*83 -MD[03]	25*84 -MD[01]	25*85 -MD[00]
25*86 -MD[02]	25*87 -MD[03]	25*88 -MD[04]	25*89 -MD[05]
25*90 -MD[04]	25*91 -MD[05]	25*92 -MD[07]	25*93 -MD[06]
25*94 -MD[06]	25*95 -MD[07]	25*96 -MD[08]	25*97 -MD[09]
25*98 -MD[10]	25*99 -MD[11]	25*100 MAR[06]	25*101 MAR[05]
25*102 MAR[07]	25*103 MAR[08]	25*104 MAR[14]	25*105 MAR[11]
25*106 MAR[13]	25*107 -MD[08]	25*108 -MD[09]	25*109 -MD[10]
25*110 -MD[11]	25*111 MAR[09]	25*112 MAR[12]	25*113 MAR[10]
26*67 RS7	26*68 RS6	26*69 RS4	26*70 RS3
26*71 RS2	26*72 RS5	26*73 RS1	26*74 -PC
26*75 -CE	26*76 -CS3	26*77 RS0	26*78 -W0
26*79 -DS0	26*92 -MD[12]	26*95 -MD[12]	26*96 -MD[13]
26*97 -MD[14]	26*98 -MD[15]	26*99 READPAR	26*100 MAR[06]
26*101 MAR[05]	26*102 MAR[07]	26*103 MAR[08]	26*104 MAR[14]
26*105 MAR[11]	26*106 MAR[13]	26*107 -MD[13]	26*108 -MD[14]
26*109 -MD[15]	26*110 WRITEPAR	26*111 MAR[09]	26*112 MAR[12]
26*113 MAR[10]	27*67 RS7	27*68 RS6	27*69 RS4
27*70 RS3	27*71 RS2	27*72 RS5	27*73 RS1
27*74 -PC	27*75 -CE	27*76 -CS3	27*77 RS0
27*78 -W1	27*79 -DS1	27*80 -MD[02]	27*81 -MD[00]
27*82 -MD[01]	27*83 -MD[03]	27*84 -MD[01]	27*85 -MD[00]
27*86 -MD[02]	27*87 -MD[03]	27*88 -MD[04]	27*89 -MD[05]
27*90 -MD[04]	27*91 -MD[05]	27*92 -MD[07]	27*93 -MD[06]
27*94 -MD[06]	27*95 -MD[07]	27*96 -MD[08]	27*97 -MD[09]
27*98 -MD[10]	27*99 -MD[11]	27*100 MAR[06]	27*101 MAR[05]
27*102 MAR[07]	27*103 MAR[08]	27*104 MAR[14]	27*105 MAR[11]
27*106 MAR[13]	27*107 -MD[08]	27*108 -MD[09]	27*109 -MD[10]
27*110 -MD[11]	27*111 MAR[09]	27*112 MAR[12]	27*113 MAR[10]
28*67 RS7	28*68 RS6	28*69 RS4	28*70 RS3
28*71 RS2	28*72 RS5	28*73 RS1	28*74 -PC
28*75 -CE	28*76 -CS3	28*77 RS0	28*78 -W1
28*79 -DS1	28*92 -MD[12]	28*95 -MD[12]	28*96 -MD[13]
28*97 -MD[14]	28*98 -MD[15]	28*99 READPAR	28*100 MAR[06]
28*101 MAR[05]	28*102 MAR[07]	28*103 MAR[08]	28*104 MAR[14]
28*105 MAR[11]	28*106 MAR[13]	28*107 -MD[13]	28*108 -MD[14]
28*109 -MD[15]	28*110 WRITEPAR	28*111 MAR[09]	28*112 MAR[12]
28*113 MAR[10]↑L			

Alto Mouse Circuitry

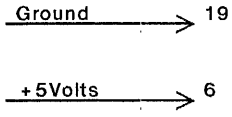




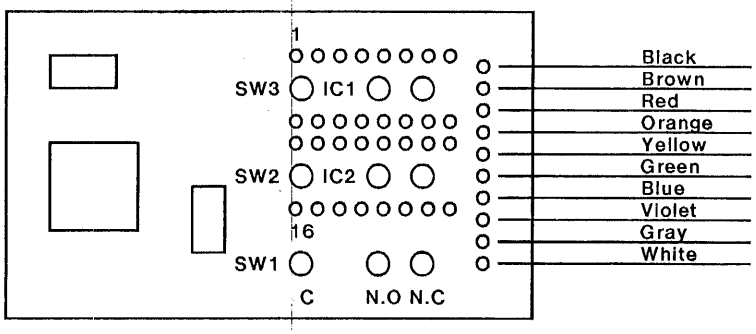
'Y' Encoder



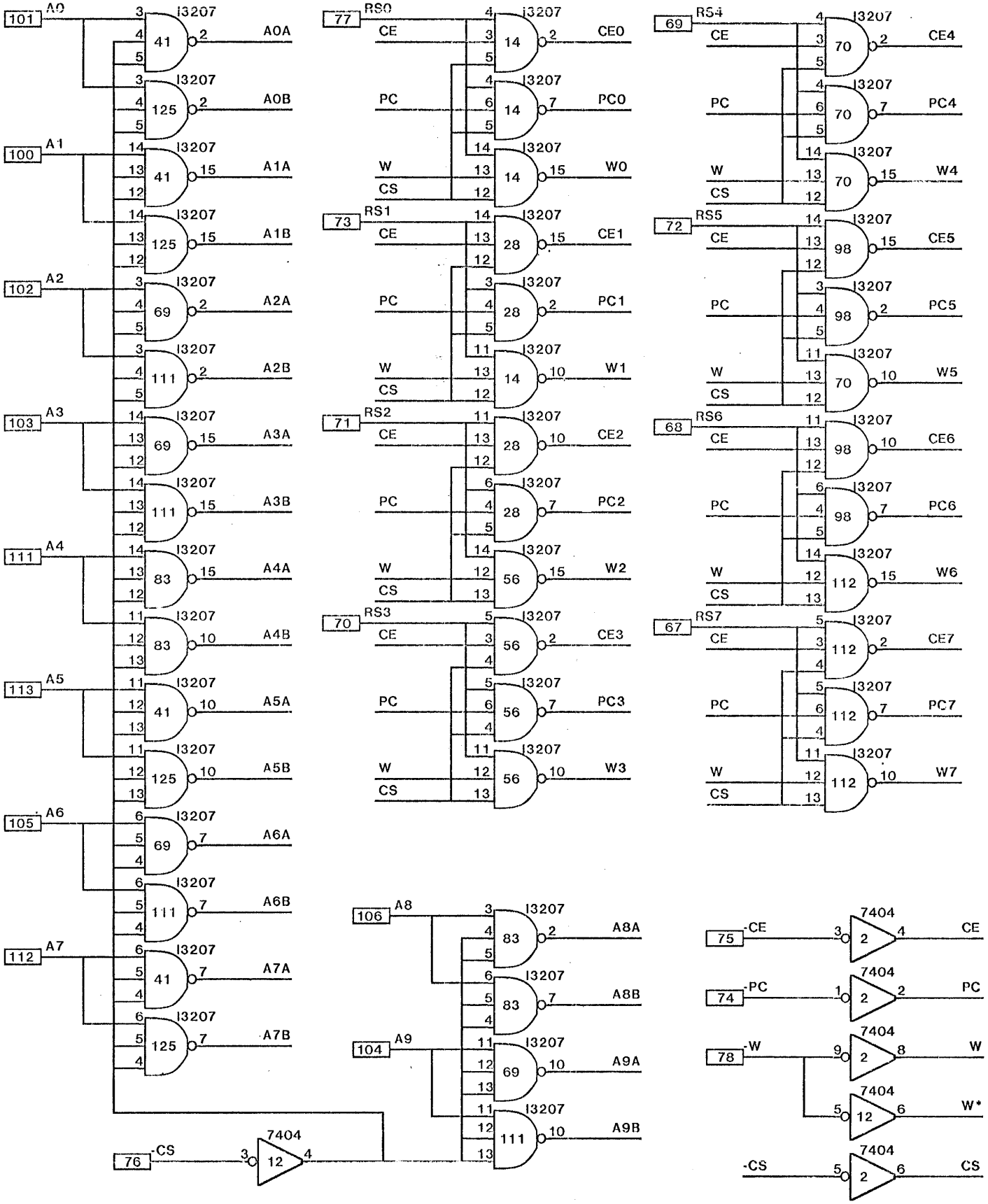
'X' Encoder

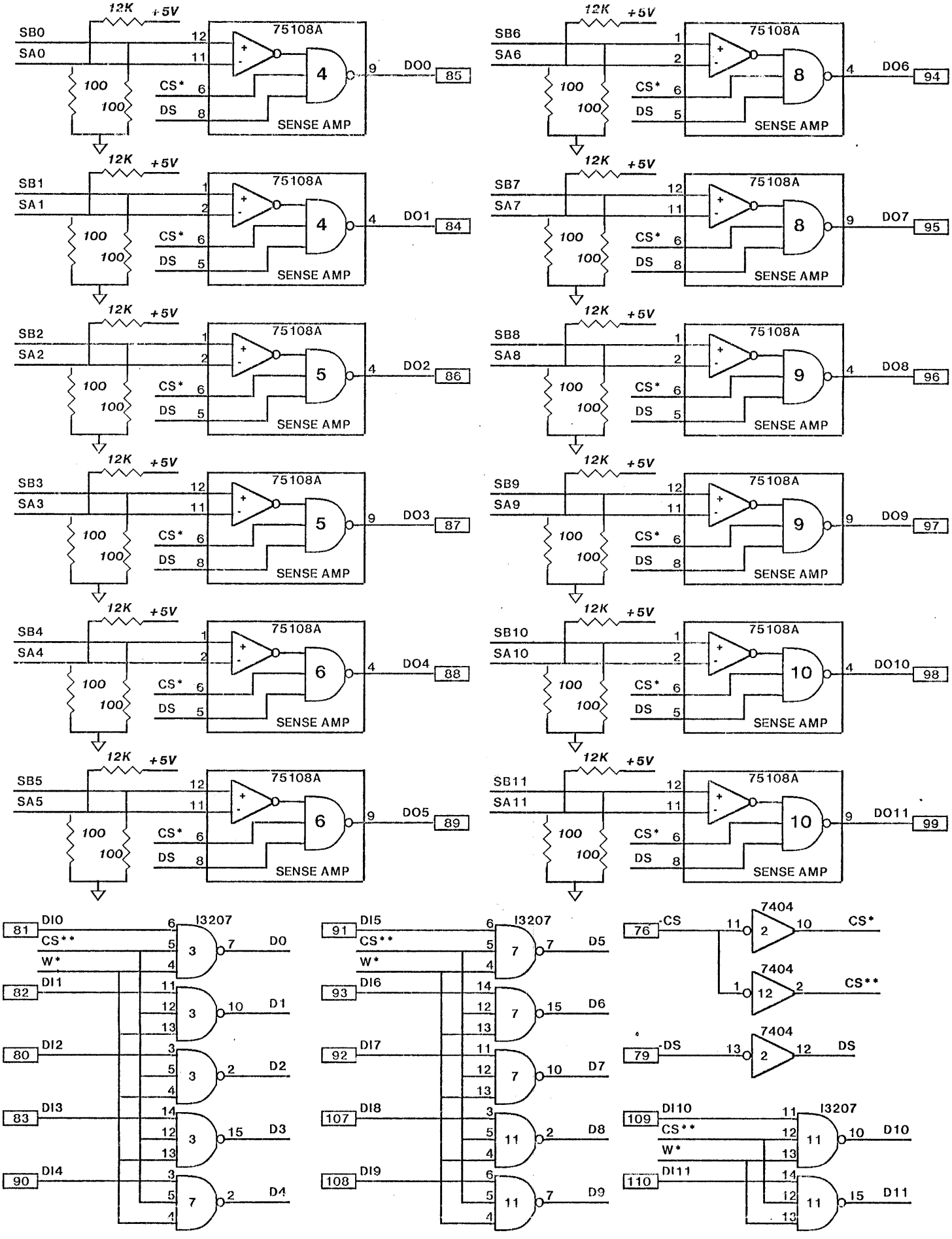


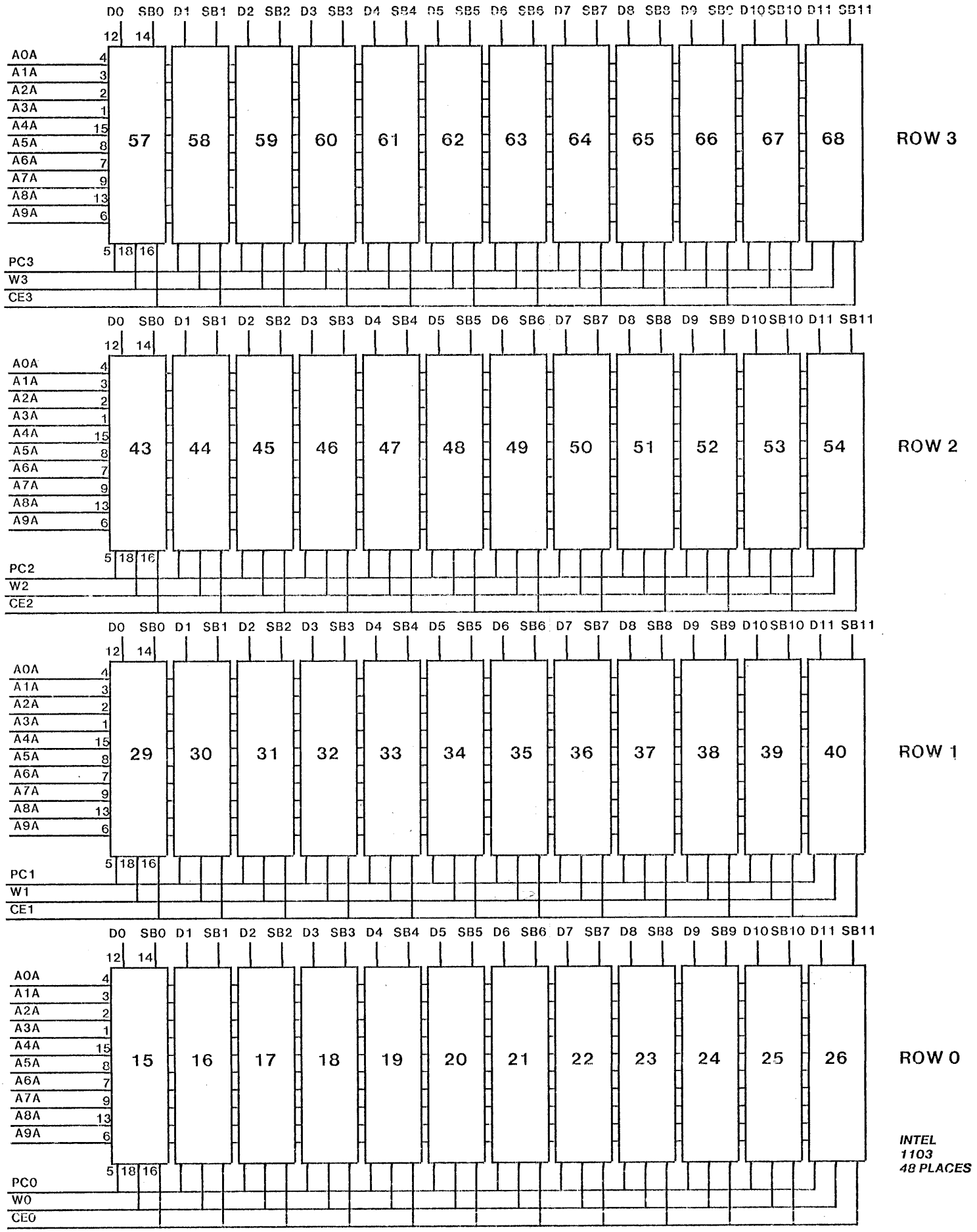
THESE REPRESENT
MOUSE CONNECTOR
PIN NUMBERS

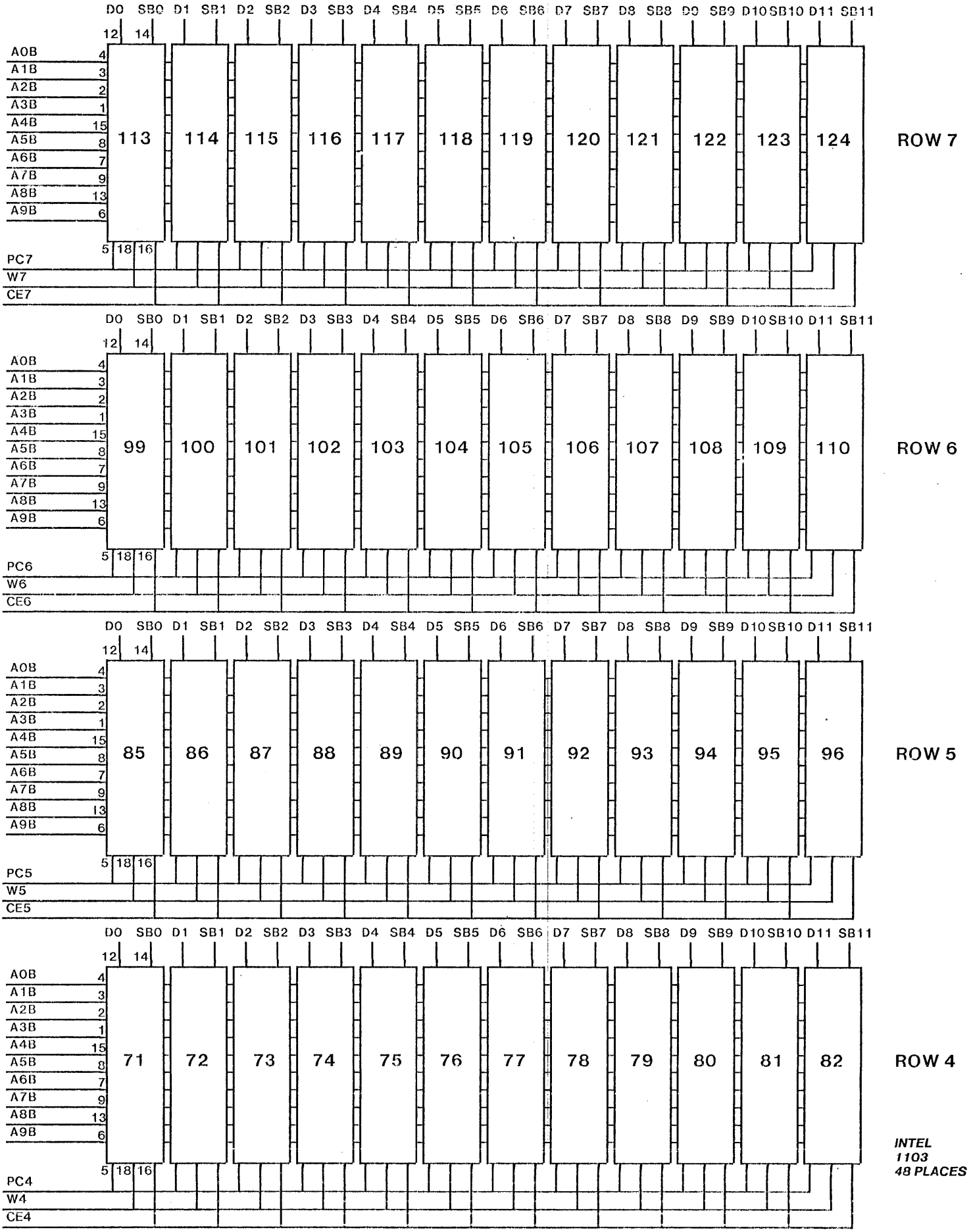


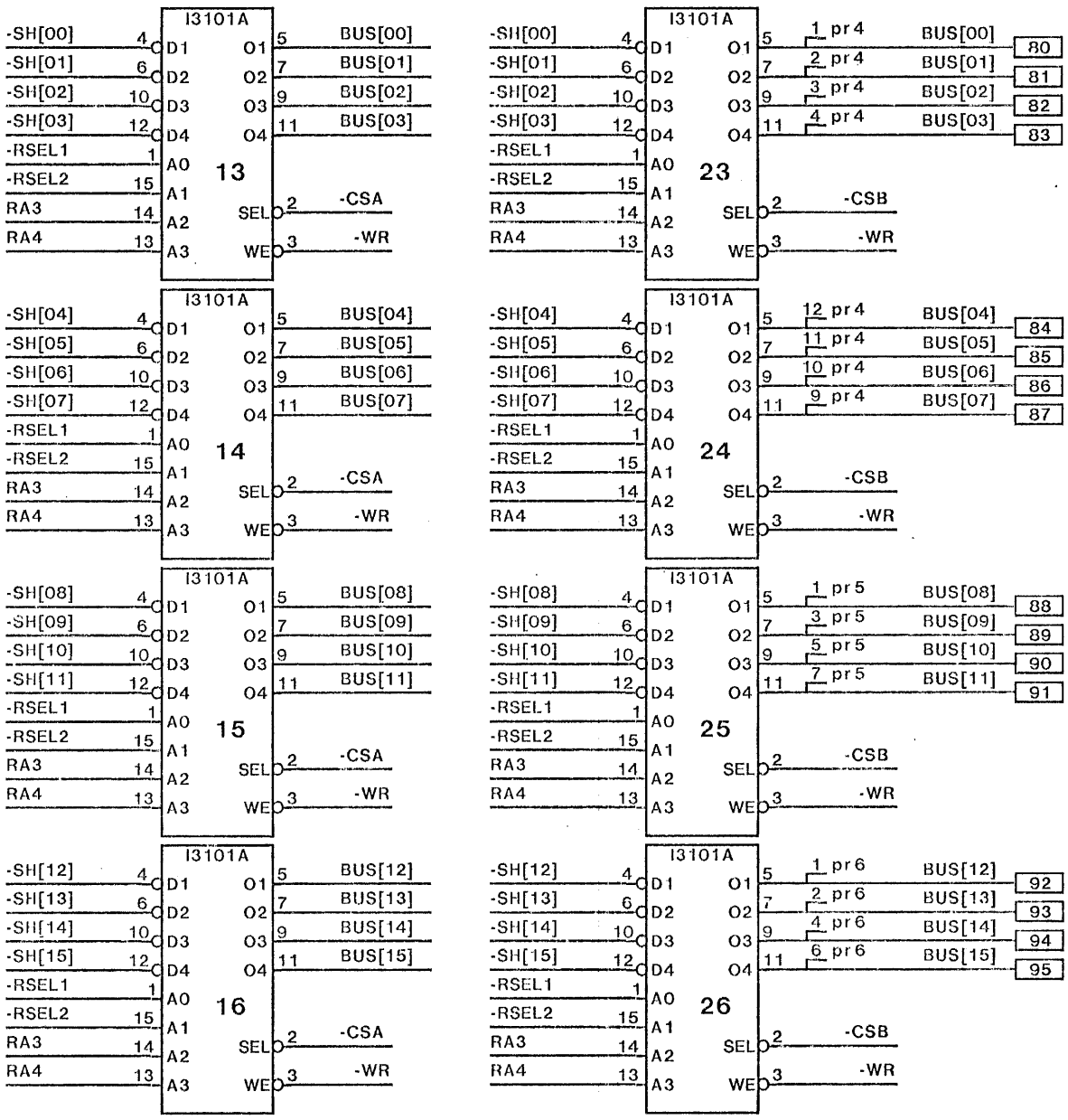
Mouse P.C.B.

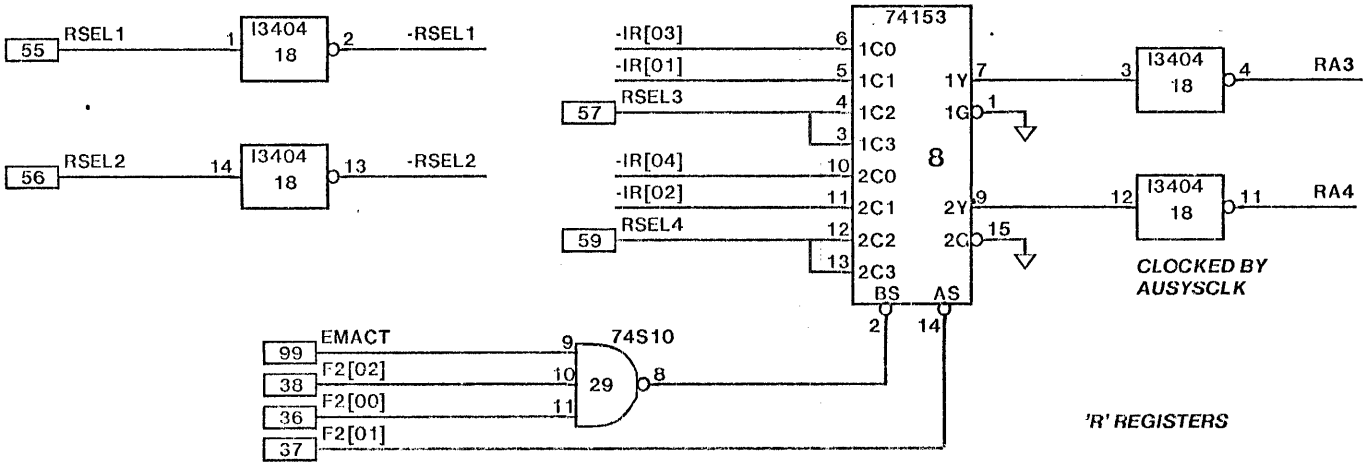

101 A0
100 A1
102 A2
103 A3
111 A4
113 A5
105 A6
112 A7
106 A8
104 A9
76 -CS
7404
77 RS0
73 RS1
71 RS2
70 RS3
CE
PC
W
CS
CE0
PC0
W0
CE1
PC1
W1
CE2
PC2
W2
CE3
PC3
W3
69 RS4
72 RS5
68 RS6
67 RS7
CE4
PC4
W4
CE5
PC5
W5
CE6
PC6
W6
CE7
PC7
W7
A0A
A0B
A1A
A1B
A2A
A2B
A3A
A3B
A4A
A4B
A5A
A5B
A6A
A6B
A7A
A7B
A8A
A8B
A9A
A9B
75 -CE
74 -PC
78 -W
CE
PC
W
W*
-CS
CS

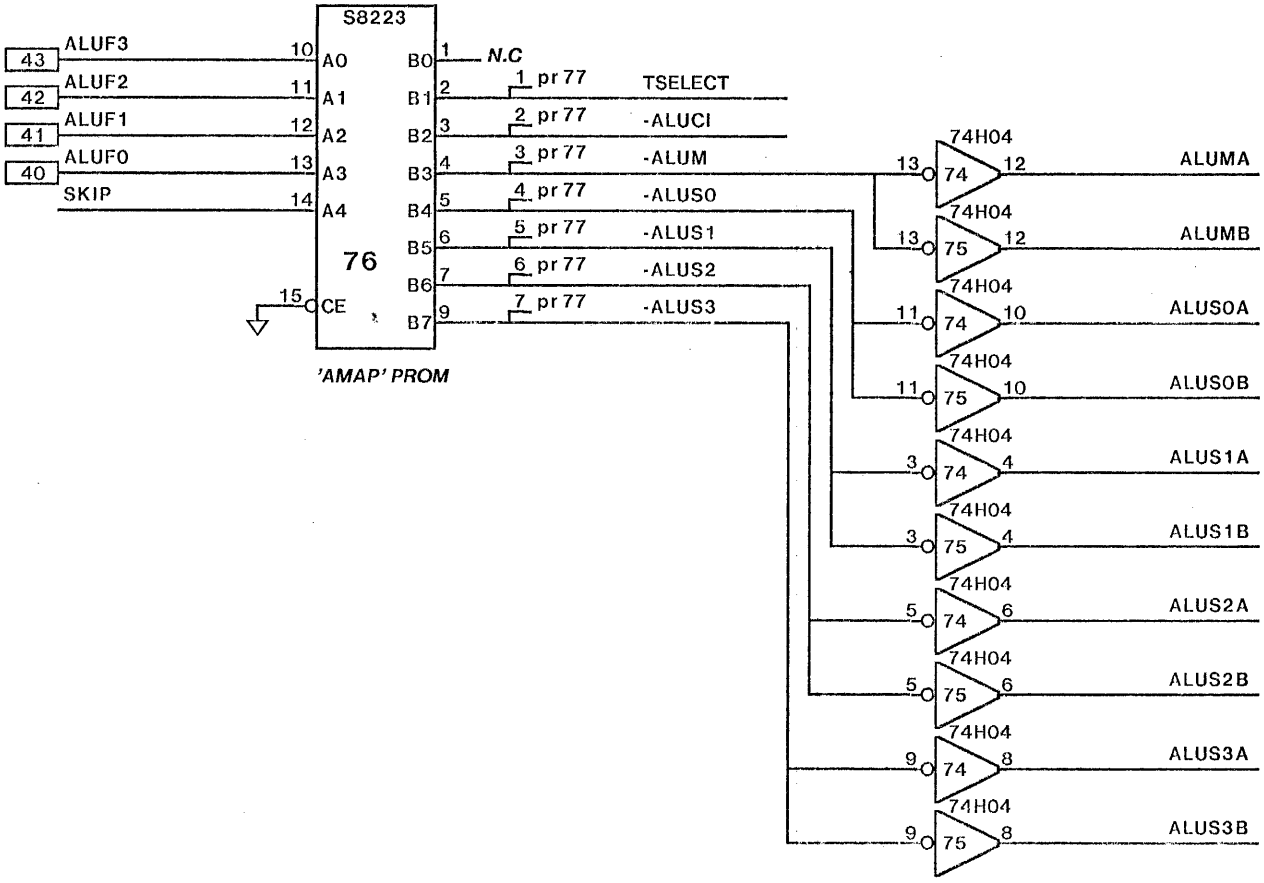

12K +5V
SB0
SA0
100
100
CS* 6
DS 8
75108A
SENSE AMP
4
DO0 85
SB1
SA1
DS 5
DO1 84
SB2
SA2
5
DO2 86
SB3
SA3
DO3 87
SB4
SA4
6
DO4 88
SB5
SA5
DO5 89
SB6
SA6
8
DO6 94
SB7
SA7
DO7 95
SB8
SA8
9
DO8 96
SB9
SA9
DO9 97
SB10
SA10
10
DO10 98
SB11
SA11
DO11 99
DI0 81
CS** 5
W* 4
DI1 82
DI2 80
DI3 83
DI4 90
I3207
D0
D1
D2
D3
D4
DI5 91
DI6 93
DI7 92
DI8 107
DI9 108
D5
D6
D7
D8
D9
CS 76
7404
CS*
CS**
DS 79
DS
DI10 109
DI11 110
D10
D11

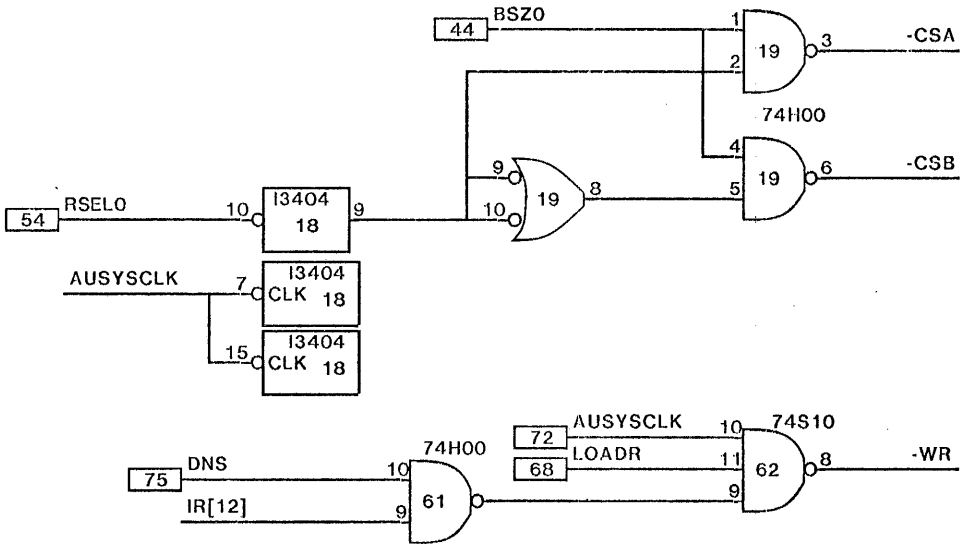

D0 SB0 D1 SB1 D2 SB2 D3 SB3 D4 SB4 D5 SB5 D6 SB6 D7 SB7 D8 SB8 D9 SB9 D10 SB10 D11 SB11
12 14
A0A 4
A1A 3
A2A 2
A3A 1
A4A 15
A5A 8
A6A 7
A7A 9
A8A 13
A9A 6
57 58 59 60 61 62 63 64 65 66 67 68
ROW 3
5 18 16
PC3
W3
CE3
43 44 45 46 47 48 49 50 51 52 53 54
ROW 2
PC2
W2
CE2
29 30 31 32 33 34 35 36 37 38 39 40
ROW 1
PC1
W1
CE1
15 16 17 18 19 20 21 22 23 24 25 26
ROW 0
PC0
W0
CE0
INTEL
1103
48 PLACES
COLUMNS 11 10 9 8 7 6 5 4 3 2 1 0


D0 SB0 D1 SB1 D2 SB2 D3 SB3 D4 SB4 D5 SB5 D6 SB6 D7 SB7 D8 SB8 D9 SB9 D10 SB10 D11 SB11
12 14
A0B 4
A1B 3
A2B 2
A3B 1
A4B 15
A5B 8
A6B 7
A7B 9
A8B 13
A9B 6
113 114 115 116 117 118 119 120 121 122 123 124
ROW 7
5 18 16
PC7
W7
CE7
99 100 101 102 103 104 105 106 107 108 109 110
ROW 6
PC6
W6
CE6
85 86 87 88 89 90 91 92 93 94 95 96
ROW 5
PC5
W5
CE5
71 72 73 74 75 76 77 78 79 80 81 82
ROW 4
PC4
W4
CE4
INTEL
1103
48 PLACES
COLUMNS 11 10 9 8 7 6 5 4 3 2 1 0

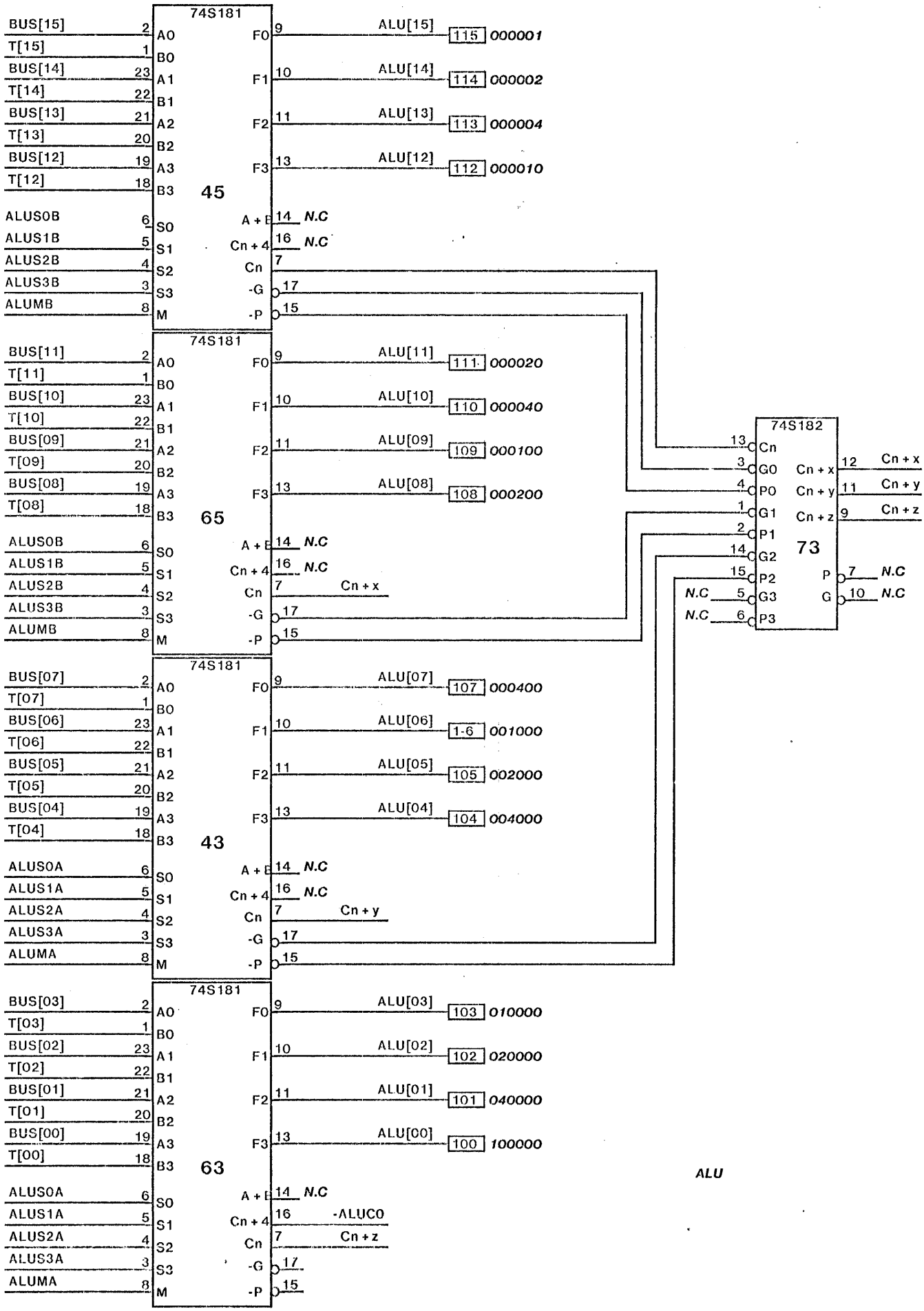

I3101A
13
-SH[00]
-SH[01]
-SH[02]
-SH[03]
-RSEL1
-RSEL2
RA3
RA4
BUS[00]
BUS[01]
BUS[02]
BUS[03]
-CSA
-WR
I3101A
23
-CSB
-WR
BUS[00]
BUS[01]
BUS[02]
BUS[03]
80
81
82
83
I3101A
14
-SH[04]
-SH[05]
-SH[06]
-SH[07]
BUS[04]
BUS[05]
BUS[06]
BUS[07]
-CSA
-WR
I3101A
24
-CSB
-WR
BUS[04]
BUS[05]
BUS[06]
BUS[07]
84
85
86
87
I3101A
15
-SH[08]
-SH[09]
-SH[10]
-SH[11]
BUS[08]
BUS[09]
BUS[10]
BUS[11]
-CSA
-WR
I3101A
25
-CSB
-WR
BUS[08]
BUS[09]
BUS[10]
BUS[11]
88
89
90
91
I3101A
16
-SH[12]
-SH[13]
-SH[14]
-SH[15]
BUS[12]
BUS[13]
BUS[14]
BUS[15]
-CSA
-WR
I3101A
26
-CSB
-WR
BUS[12]
BUS[13]
BUS[14]
BUS[15]
92
93
94
95


55
RSEL1
I3404
18
-RSEL1
56
RSEL2
-RSEL2
74153
8
-IR[03]
-IR[01]
RSEL3
57
-IR[04]
-IR[02]
RSEL4
59
BS
AS
I3404
18
RA3
RA4
CLOCKED BY
AUSYSCLK
EMACT
99
F2[02]
38
F2[00]
36
F2[01]
37
74S10
29
'R' REGISTERS

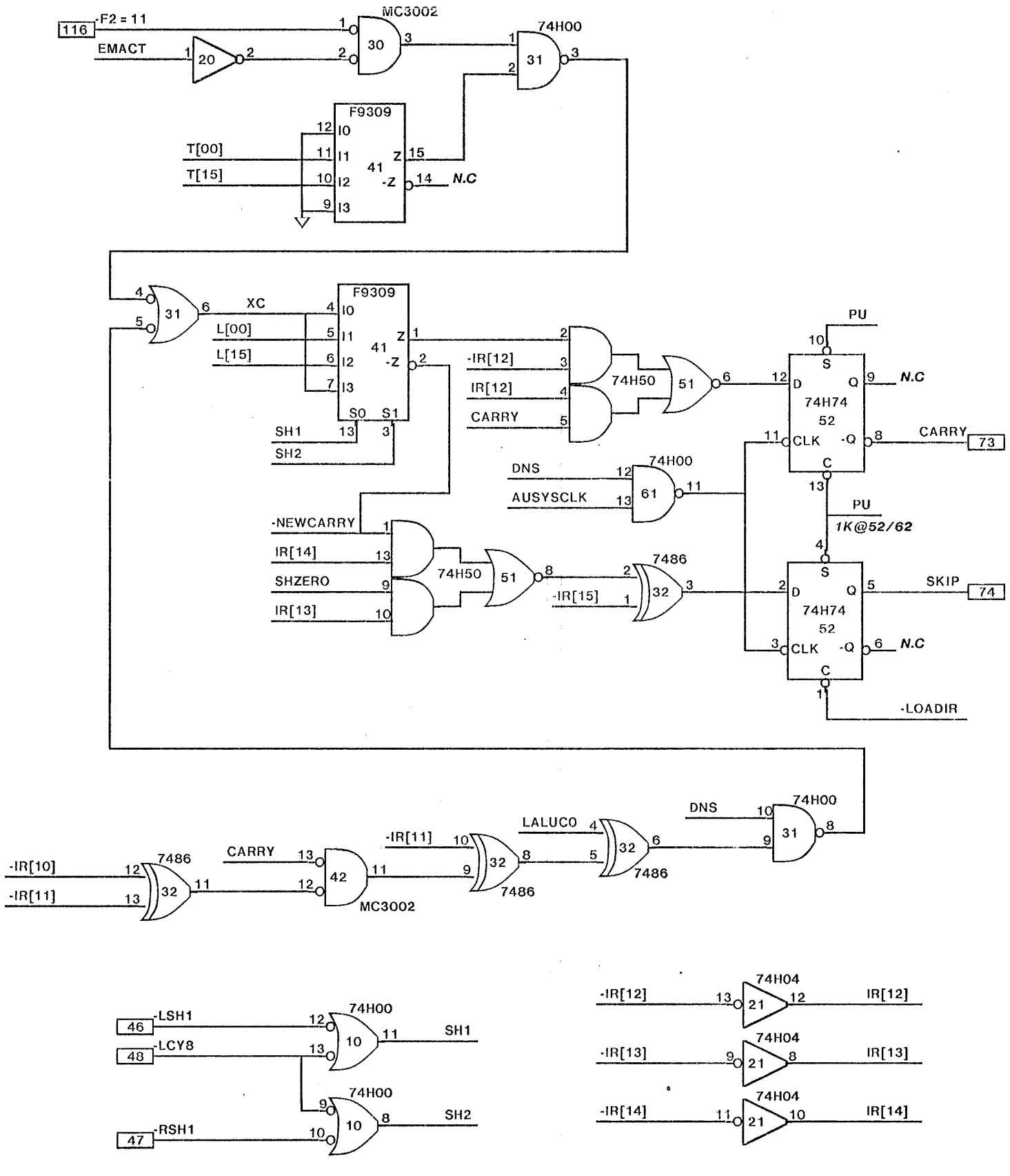

S8223
ALUF3
ALUF2
ALUF1
ALUF0
SKIP
A0
A1
A2
A3
A4
B0
B1
B2
B3
B4
B5
B6
B7
CE
76
N.C
TSELECT
-ALUCI
-ALUM
-ALUS0
-ALUS1
-ALUS2
-ALUS3
'AMAP' PROM
74H04
ALUMA
ALUMB
ALUS0A
ALUS0B
ALUS1A
ALUS1B
ALUS2A
ALUS2B
ALUS3A
ALUS3B


BSZ0
RSELO
AUSYSCLK
I3404
CLK
-CSA
-CSB
74H00
74S10
DNS
IR[12]
LOADR
-WR

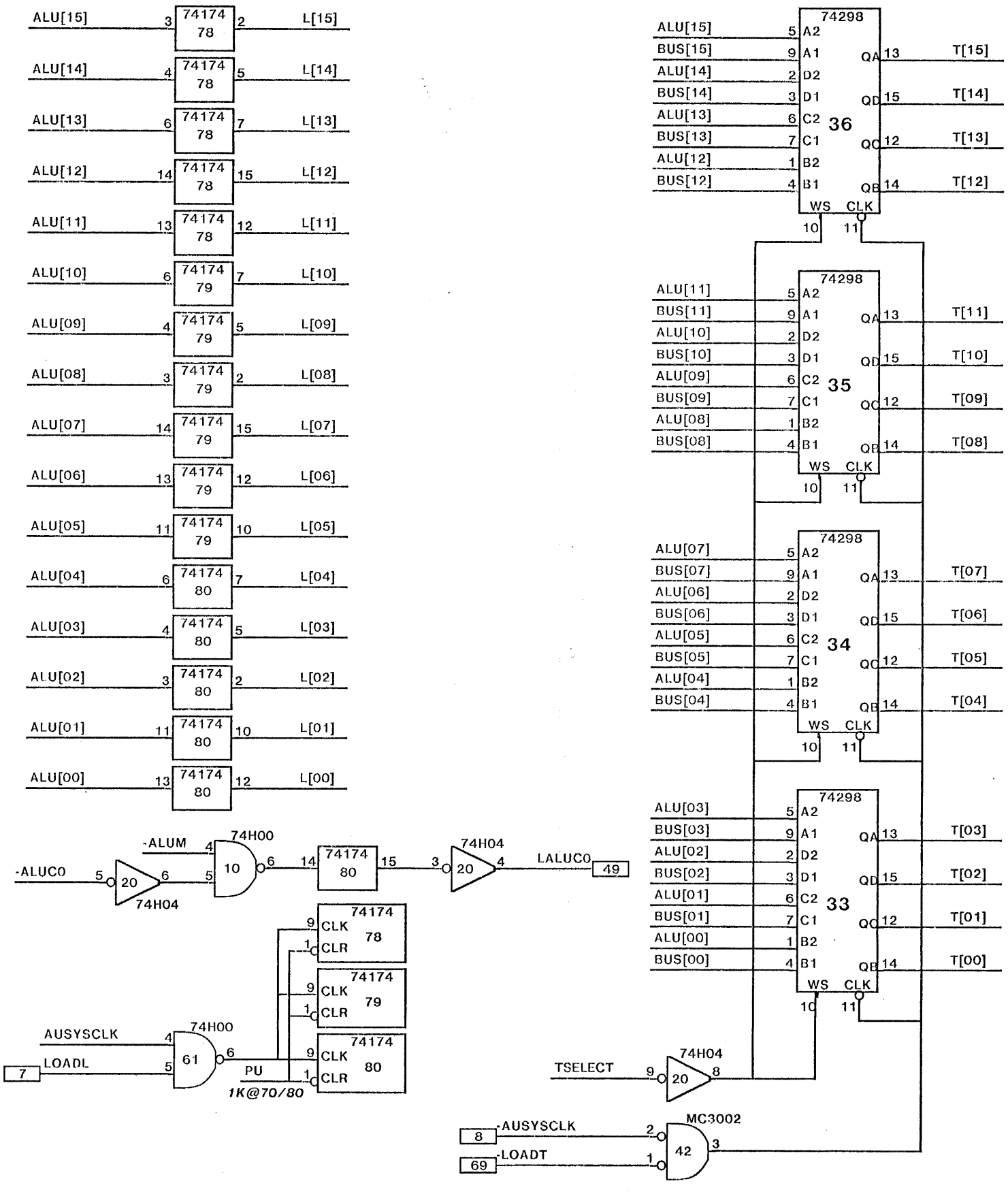
ALU CONTROL

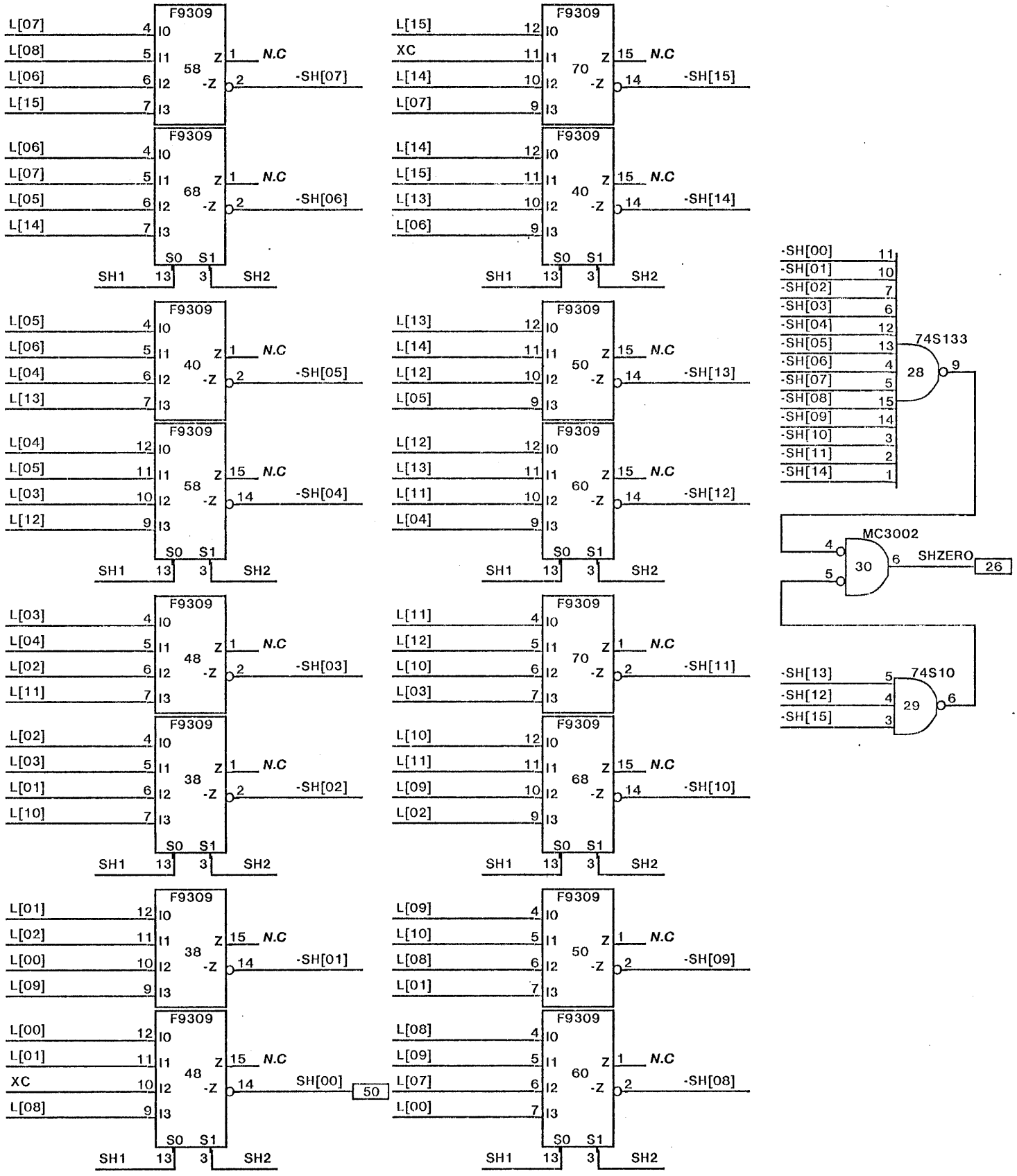

74S181
45
BUS[15] 2
T[15] 1
BUS[14] 23
T[14] 22
BUS[13] 21
T[13] 20
BUS[12] 19
T[12] 18
ALUS0B 6
ALUS1B 5
ALUS2B 4
ALUS3B 3
ALUMB 8
A0
B0
A1
B1
A2
B2
A3
B3
S0
S1
S2
S3
M
F0 9 ALU[15] 115 000001
F1 10 ALU[14] 114 000002
F2 11 ALU[13] 113 000004
F3 13 ALU[12] 112 000010
A + B 14 N.C
Cn + 4 16 N.C
Cn 7
-G 17
-P 15
74S181
65
BUS[11] 2
T[11] 1
BUS[10] 23
T[10] 22
BUS[09] 21
T[09] 20
BUS[08] 19
T[08] 18
ALUS0B 6
ALUS1B 5
ALUS2B 4
ALUS3B 3
ALUMB 8
F0 9 ALU[11] 111 000020
F1 10 ALU[10] 110 000040
F2 11 ALU[09] 109 000100
F3 13 ALU[08] 108 000200
A + B 14 N.C
Cn + 4 16 N.C
Cn 7 Cn + x
-G 17
-P 15
74S181
43
BUS[07] 2
T[07] 1
BUS[06] 23
T[06] 22
BUS[05] 21
T[05] 20
BUS[04] 19
T[04] 18
ALUS0A 6
ALUS1A 5
ALUS2A 4
ALUS3A 3
ALUMA 8
F0 9 ALU[07] 107 000400
F1 10 ALU[06] 106 001000
F2 11 ALU[05] 105 002000
F3 13 ALU[04] 104 004000
A + B 14 N.C
Cn + 4 16 N.C
Cn 7 Cn + y
-G 17
-P 15
74S181
63
BUS[03] 2
T[03] 1
BUS[02] 23
T[02] 22
BUS[01] 21
T[01] 20
BUS[00] 19
T[00] 18
ALUS0A 6
ALUS1A 5
ALUS2A 4
ALUS3A 3
ALUMA 8
F0 9 ALU[03] 103 010000
F1 10 ALU[02] 102 020000
F2 11 ALU[01] 101 040000
F3 13 ALU[00] 100 100000
A + B 14 N.C
Cn + 4 16 -ALUC0
Cn 7 Cn + z
-G 17
-P 15
74S182
73
13 Cn
3 G0
4 P0
1 G1
2 P1
14 G2
15 P2
N.C 5 G3
N.C 6 P3
Cn + x 12 Cn + x
Cn + y 11 Cn + y
Cn + z 9 Cn + z
P 7 N.C
G 10 N.C

ALU

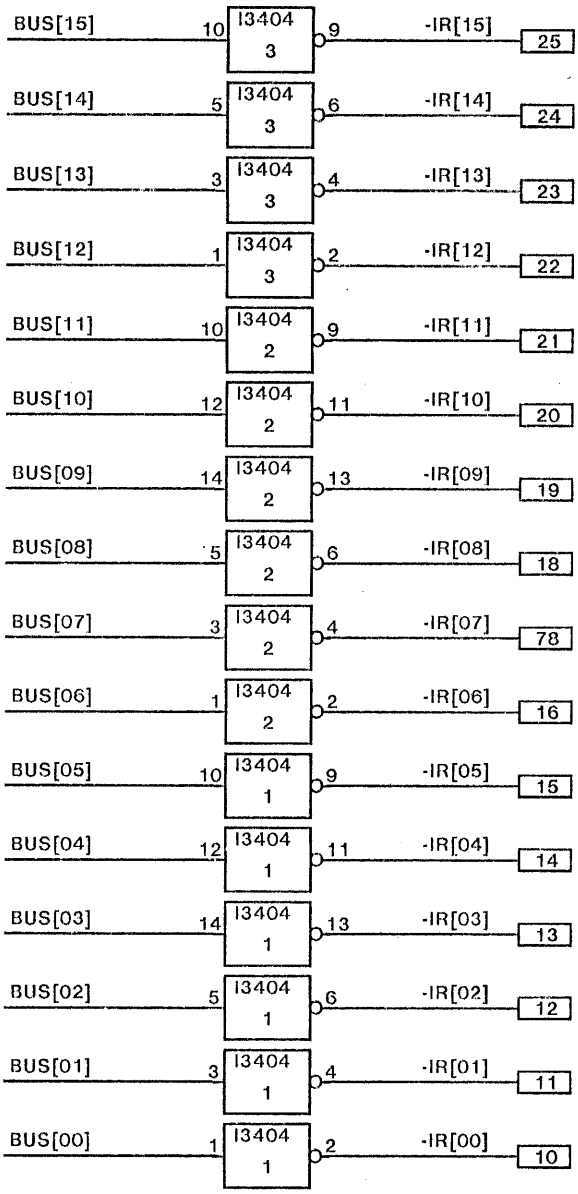

116
-F2 = 11
EMACT
MC3002
30
20
74H00
31
F9309
T[00]
T[15]
41
N.C
XC
L[00]
L[15]
SH1
SH2
-IR[12]
IR[12]
CARRY
74H50
51
PU
74H74
52
N.C
CARRY
73
DNS
AUSYSCLK
61
1K@52/62
-NEWCARRY
IR[14]
SHZERO
IR[13]
7486
32
-IR[15]
SKIP
74
-LOADIR
-IR[10]
-IR[11]
42
LALUCO
-LSH1
46
-LCY8
48
-RSH1
47
10
SH1
SH2
-IR[12]
-IR[13]
-IR[14]
74H04
21
IR[12]
IR[13]
IR[14]

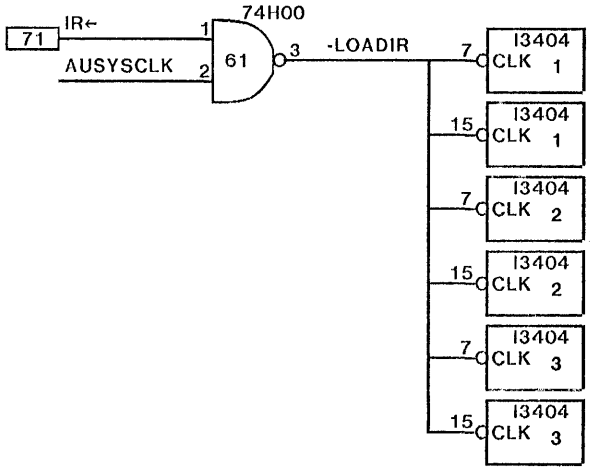
SKIP/CARRY

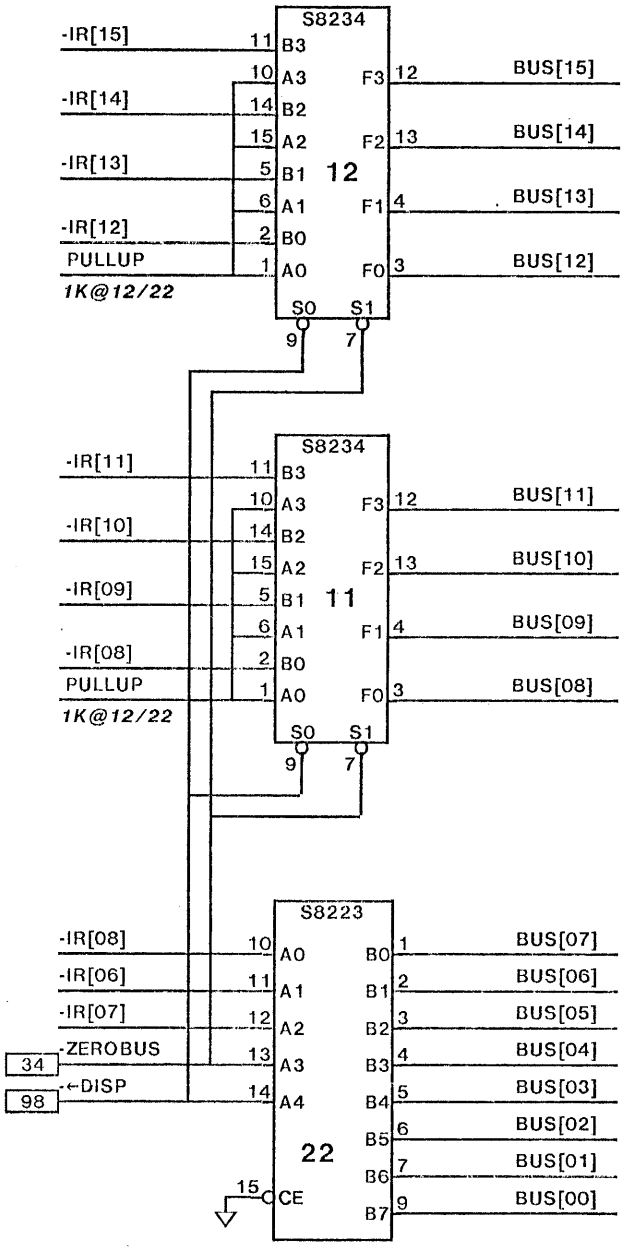

ALU[15] 3 74174 78 2 L[15]
ALU[14] 4 74174 78 5 L[14]
ALU[13] 6 74174 78 7 L[13]
ALU[12] 14 74174 78 15 L[12]
ALU[11] 13 74174 78 12 L[11]
ALU[10] 6 74174 79 7 L[10]
ALU[09] 4 74174 79 5 L[09]
ALU[08] 3 74174 79 2 L[08]
ALU[07] 14 74174 79 15 L[07]
ALU[06] 13 74174 79 12 L[06]
ALU[05] 11 74174 79 10 L[05]
ALU[04] 6 74174 80 7 L[04]
ALU[03] 4 74174 80 5 L[03]
ALU[02] 3 74174 80 2 L[02]
ALU[01] 11 74174 80 10 L[01]
ALU[00] 13 74174 80 12 L[00]
-ALUM
74H00
-ALUC0
20
74H04
74174 80
74H04
LALUC0 49
74174 78
74174 79
74174 80
AUSYSCLK
LOADL
7
74H00
61
PU
1K@70/80
'L' REGISTER
74298
ALU[15] BUS[15] ALU[14] BUS[14] ALU[13] BUS[13] ALU[12] BUS[12]
A2 A1 D2 D1 C2 C1 B2 B1
QA QB QC QD
T[15] T[14] T[13] T[12]
36
WS CLK
ALU[11] BUS[11] ALU[10] BUS[10] ALU[09] BUS[09] ALU[08] BUS[08]
T[11] T[10] T[09] T[08]
35
ALU[07] BUS[07] ALU[06] BUS[06] ALU[05] BUS[05] ALU[04] BUS[04]
T[07] T[06] T[05] T[04]
34
ALU[03] BUS[03] ALU[02] BUS[02] ALU[01] BUS[01] ALU[00] BUS[00]
T[03] T[02] T[01] T[00]
33
TSELECT
74H04
MC3002
8 -AUSYSCLK
69 -LOADT
42
'T' REGISTER



ARITHMETIC SHIFTER

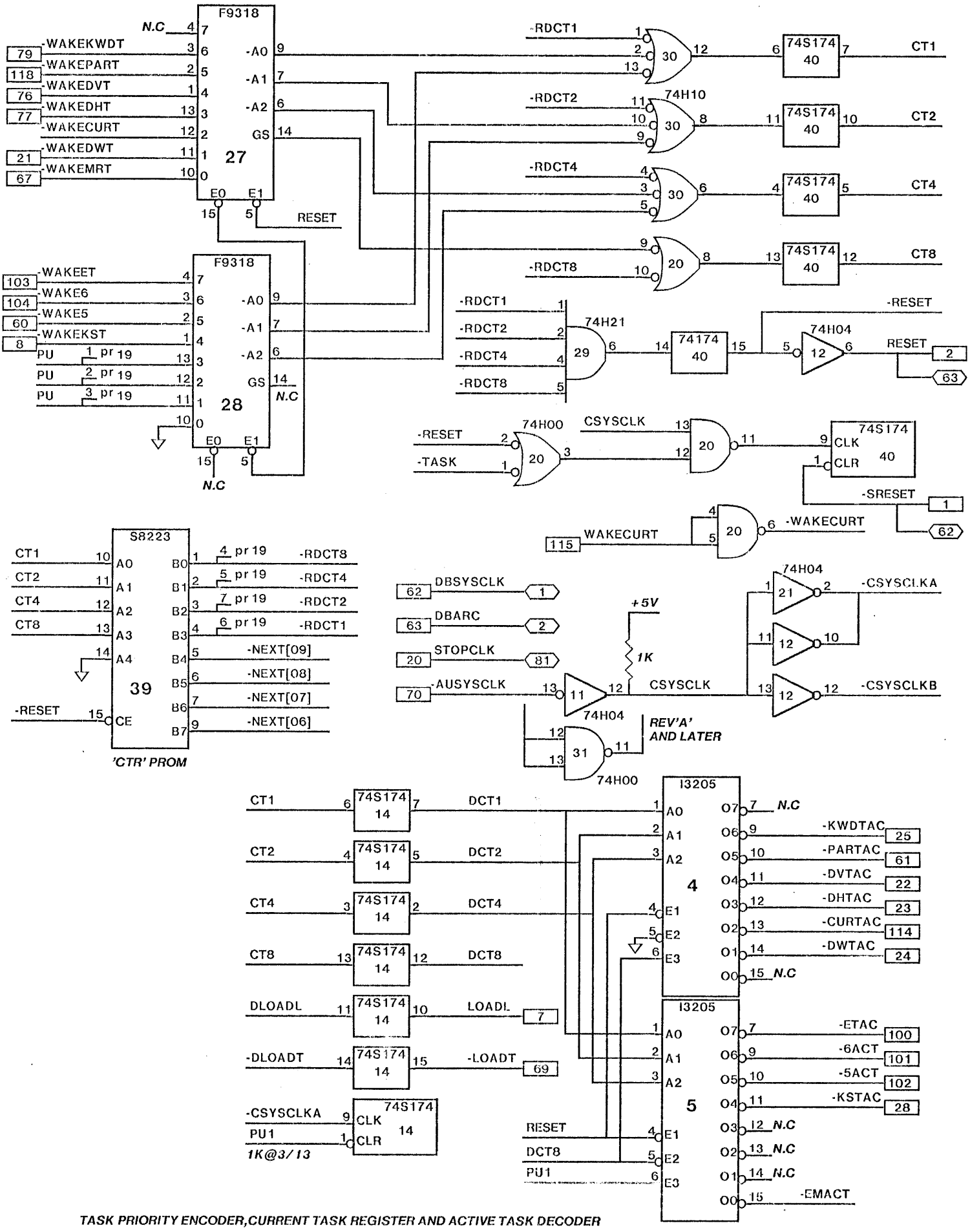




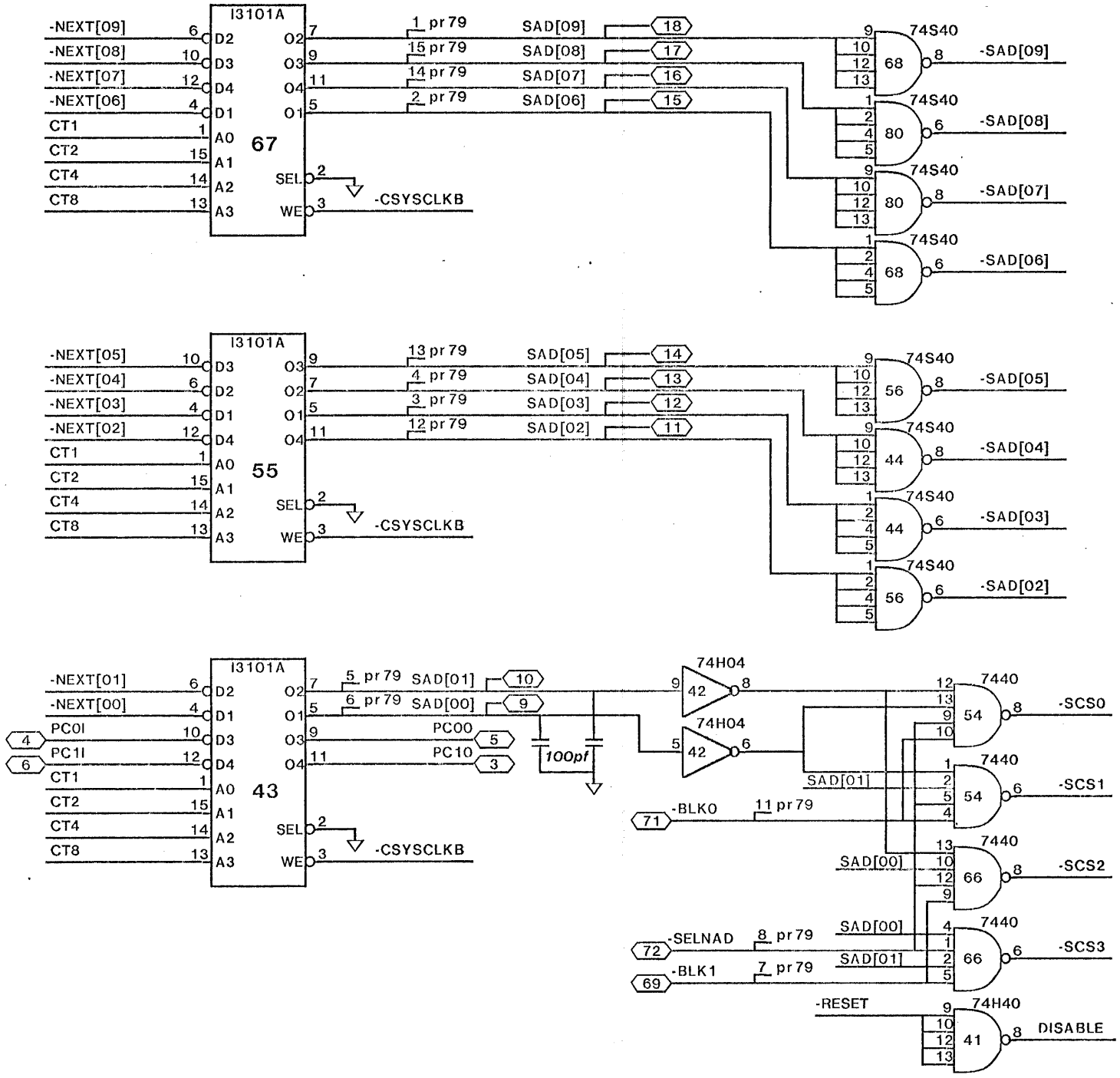


'DISPLAY' PROM

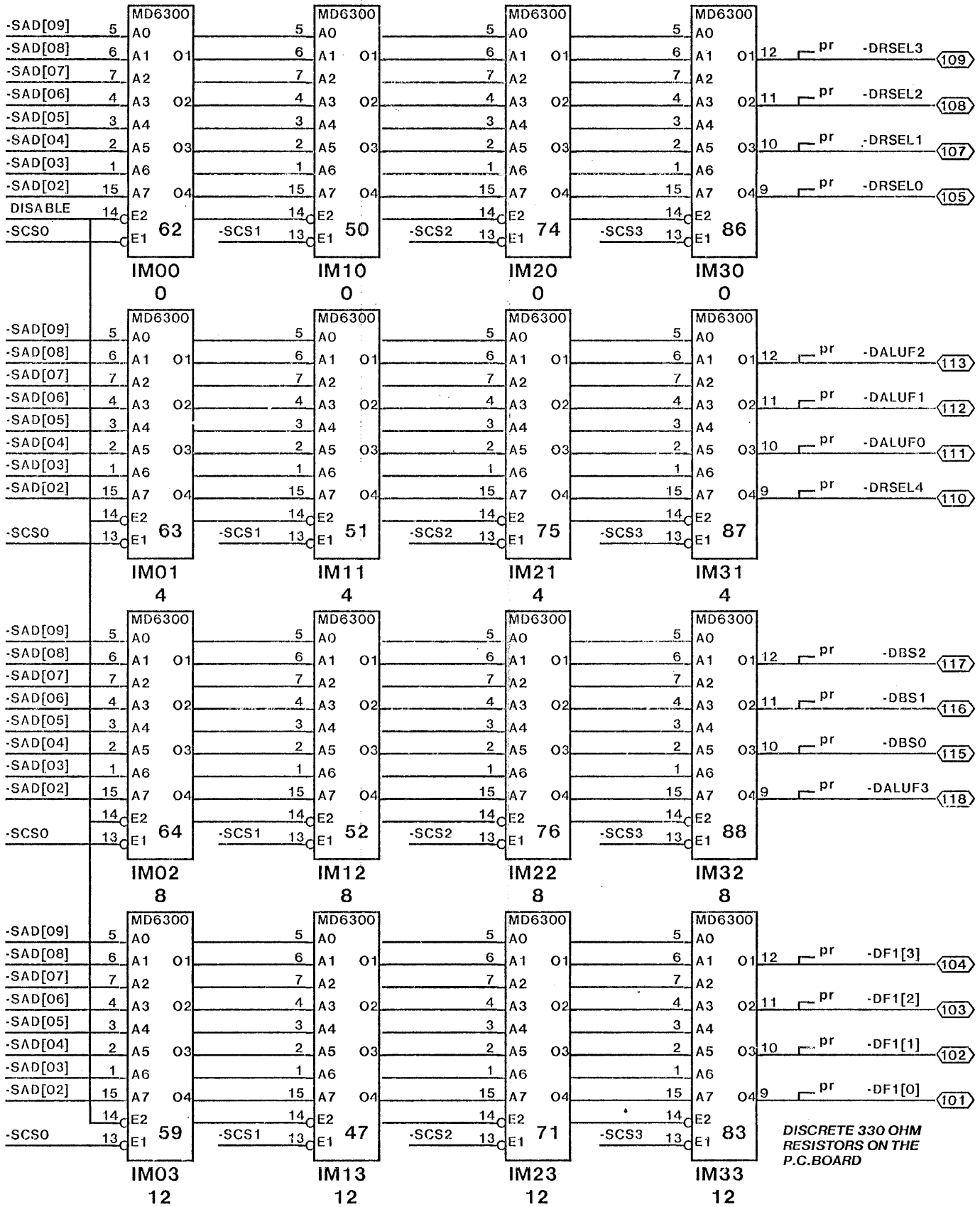
INSTRUCTION REGISTER



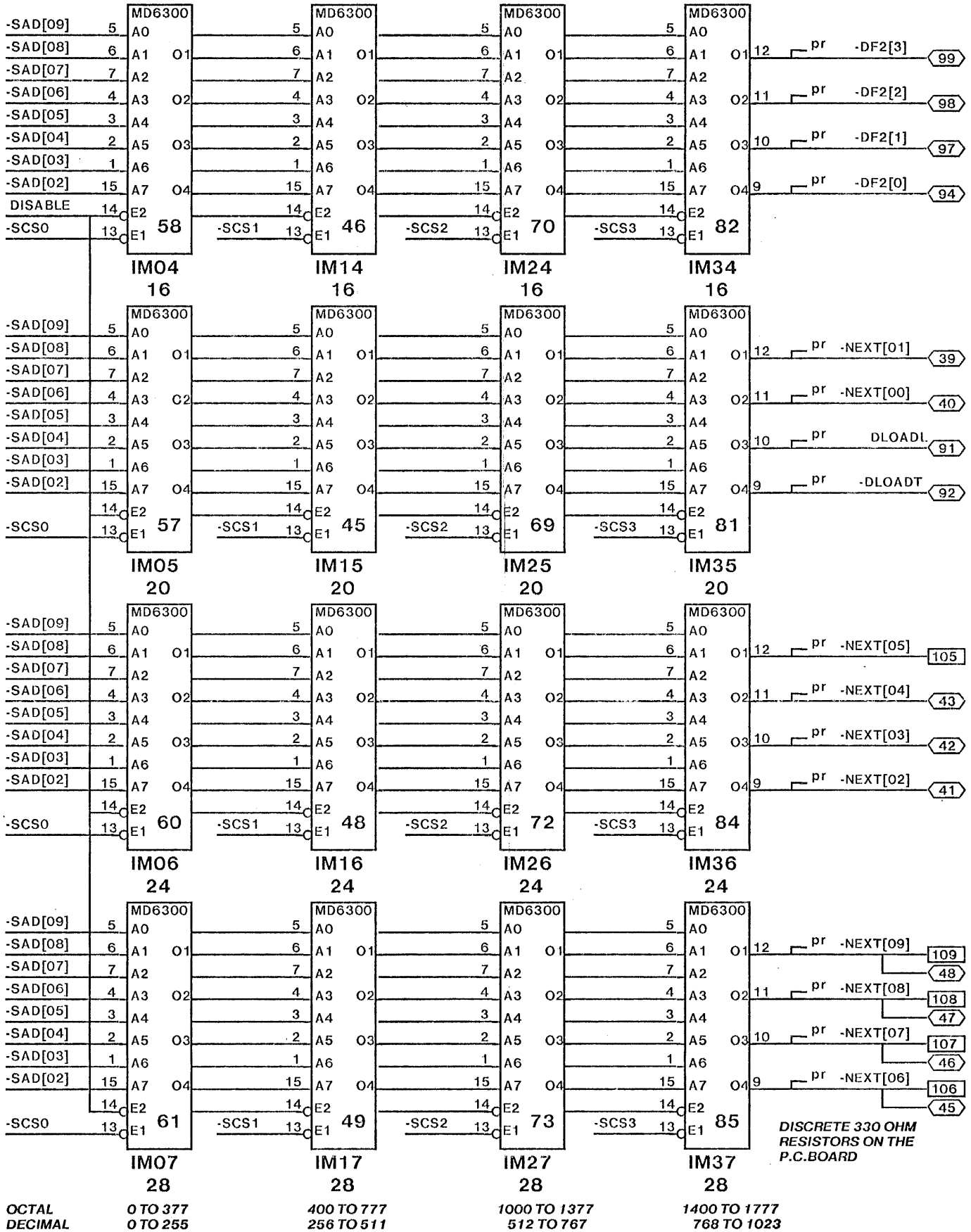
TASK PRIORITY ENCODER,CURRENT TASK REGISTER AND ACTIVE TASK DECODER


I3101A
67
-NEXT[09]
-NEXT[08]
-NEXT[07]
-NEXT[06]
CT1
CT2
CT4
CT8
D2
D3
D4
D1
A0
A1
A2
A3
O2
O3
O4
O1
SEL
WE
-CSYSCLKB
1 pr79
15 pr79
14 pr79
2 pr79
SAD[09]
SAD[08]
SAD[07]
SAD[06]
74S40
68
80
80
68
-SAD[09]
-SAD[08]
-SAD[07]
-SAD[06]
I3101A
55
-NEXT[05]
-NEXT[04]
-NEXT[03]
-NEXT[02]
13 pr79
4 pr79
3 pr79
12 pr79
SAD[05]
SAD[04]
SAD[03]
SAD[02]
56
44
44
56
-SAD[05]
-SAD[04]
-SAD[03]
-SAD[02]
I3101A
43
-NEXT[01]
-NEXT[00]
PC0I
PC1I
CT1
CT2
CT4
CT8
5 pr79
6 pr79
SAD[01]
SAD[00]
PC00
PC10
100pf
74H04
42
42
7440
54
54
66
66
-SCS0
-SCS1
-SCS2
-SCS3
-BLK0
11 pr79
-SELNAD
8 pr79
-BLK1
7 pr79
-RESET
74H40
41
DISABLE

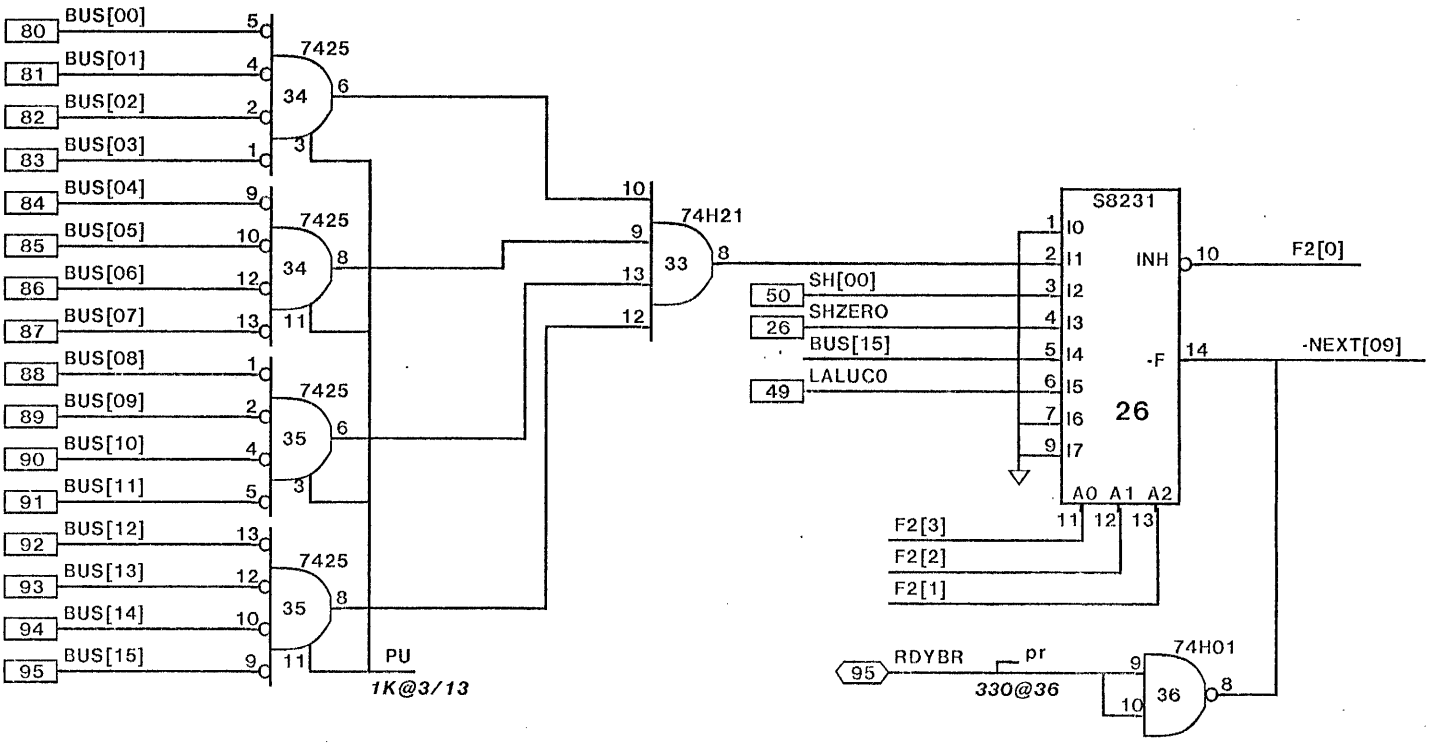
PC RAM

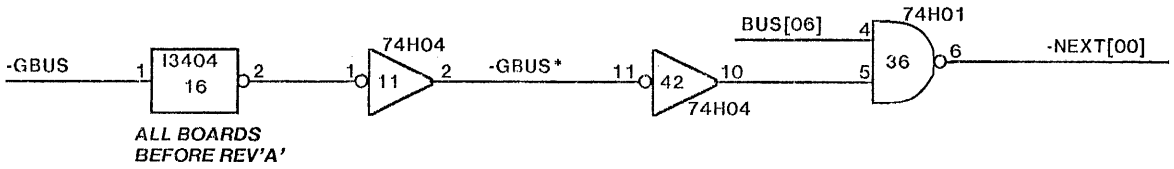

MD6300
-SAD[09]
-SAD[08]
-SAD[07]
-SAD[06]
-SAD[05]
-SAD[04]
-SAD[03]
-SAD[02]
DISABLE
-SCS0
-SCS1
-SCS2
-SCS3
A0
A1
A2
A3
A4
A5
A6
A7
E2
E1
O1
O2
O3
O4
62
50
74
86
63
51
75
87
64
52
76
88
59
47
71
83
IM00
IM10
IM20
IM30
IM01
IM11
IM21
IM31
IM02
IM12
IM22
IM32
IM03
IM13
IM23
IM33
0
4
8
12
pr
-DRSEL3
-DRSEL2
-DRSEL1
-DRSEL0
-DALUF2
-DALUF1
-DALUF0
-DRSEL4
-DBS2
-DBS1
-DBS0
-DALUF3
-DF1[3]
-DF1[2]
-DF1[1]
-DF1[0]
109
108
107
105
113
112
111
110
117
116
115
118
104
103
102
101
DISCRETE 330 OHM RESISTORS ON THE P.C.BOARD
OCTAL
DECIMAL
0 TO 377
0 TO 255
400 TO 777
256 TO 511
1000 TO 1377
512 TO 767
1400 TO 1777
766 TO 1023

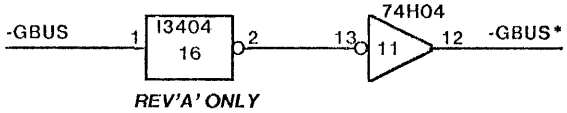
PROM ARRAY

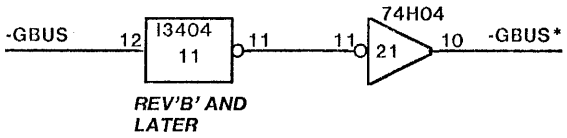

MD6300
-SAD[09]
-SAD[08]
-SAD[07]
-SAD[06]
-SAD[05]
-SAD[04]
-SAD[03]
-SAD[02]
DISABLE
-SCS0
-SCS1
-SCS2
-SCS3
A0
A1
A2
A3
A4
A5
A6
A7
E2
E1
O1
O2
O3
O4
58
46
70
82
IM04 16
IM14 16
IM24 16
IM34 16
pr -DF2[3] 99
pr -DF2[2] 98
pr -DF2[1] 97
pr -DF2[0] 94
57
45
69
81
IM05 20
IM15 20
IM25 20
IM35 20
pr -NEXT[01] 39
pr -NEXT[00] 40
pr DLOADL 91
pr -DLOADT 92
60
48
72
84
IM06 24
IM16 24
IM26 24
IM36 24
pr -NEXT[05] 105
pr -NEXT[04] 43
pr -NEXT[03] 42
pr -NEXT[02] 41
61
49
73
85
IM07 28
IM17 28
IM27 28
IM37 28
pr -NEXT[09] 109 48
pr -NEXT[08] 108 47
pr -NEXT[07] 107 46
pr -NEXT[06] 106 45
DISCRETE 330 OHM RESISTORS ON THE P.C.BOARD
OCTAL
DECIMAL
0 TO 377
0 TO 255
400 TO 777
256 TO 511
1000 TO 1377
512 TO 767
1400 TO 1777
768 TO 1023

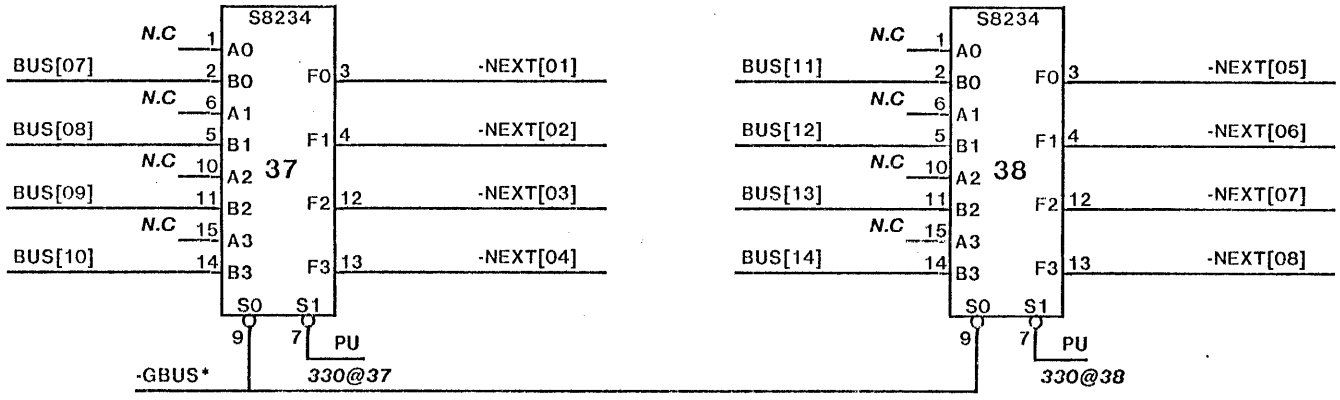
PROM ARRAY



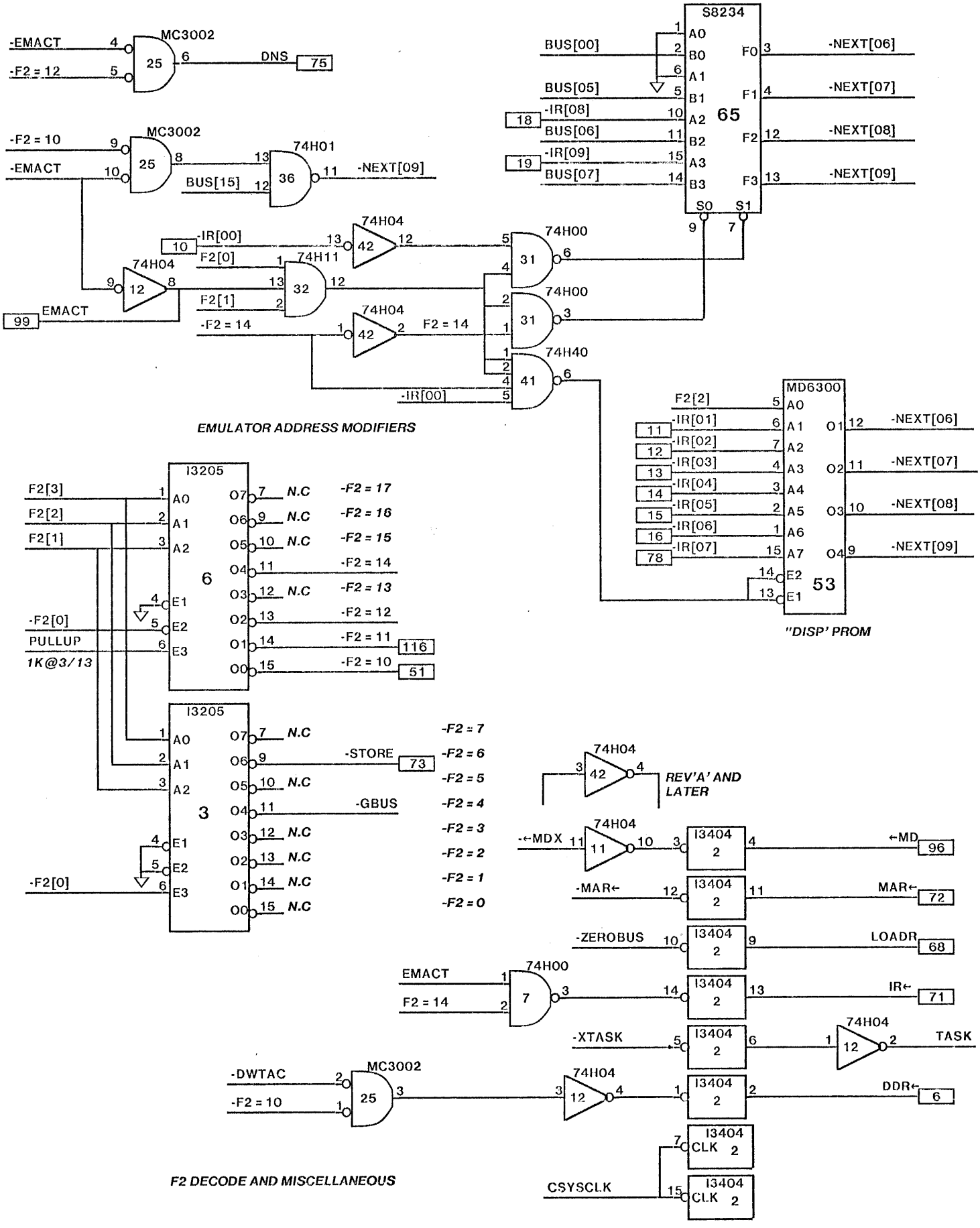


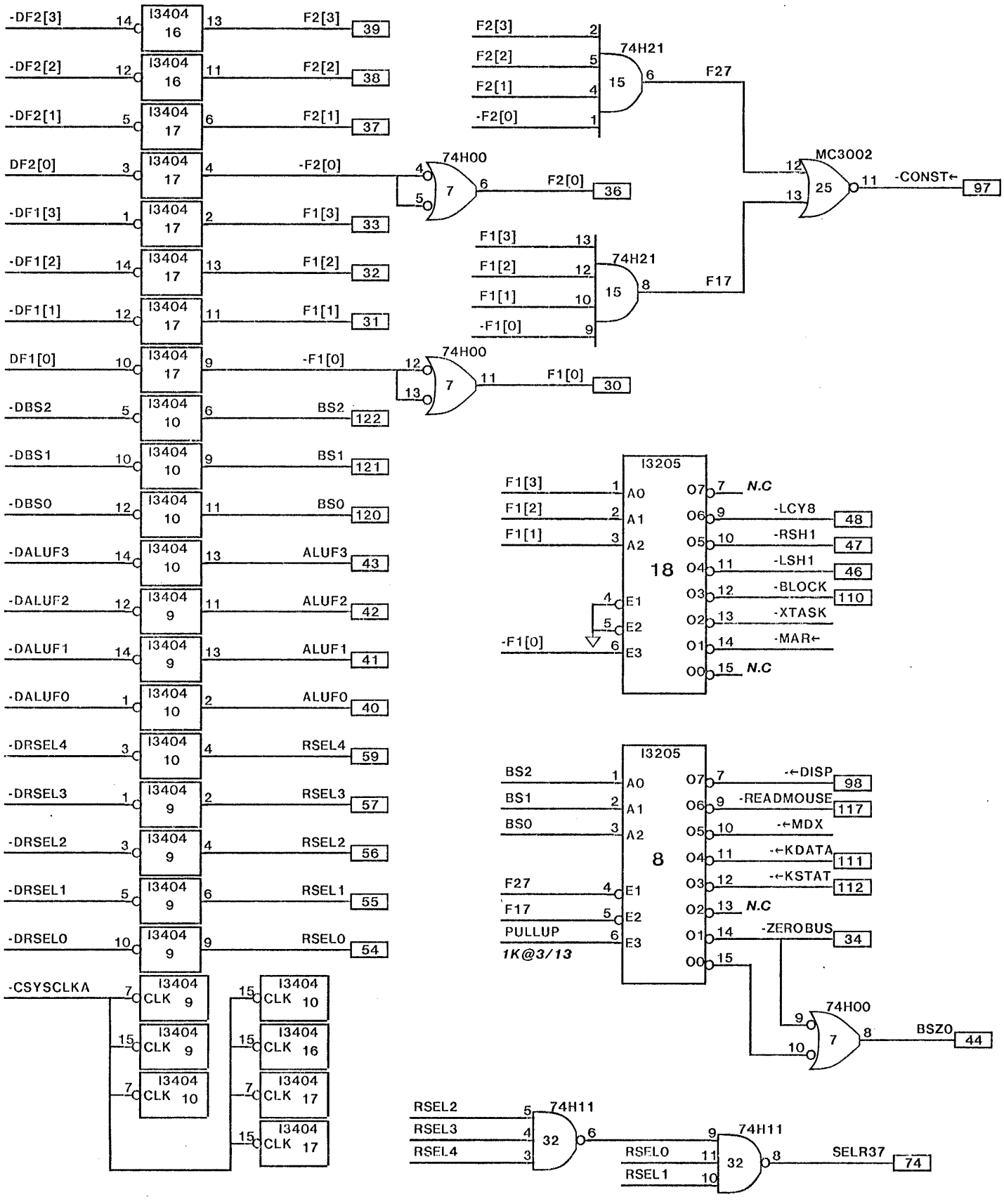




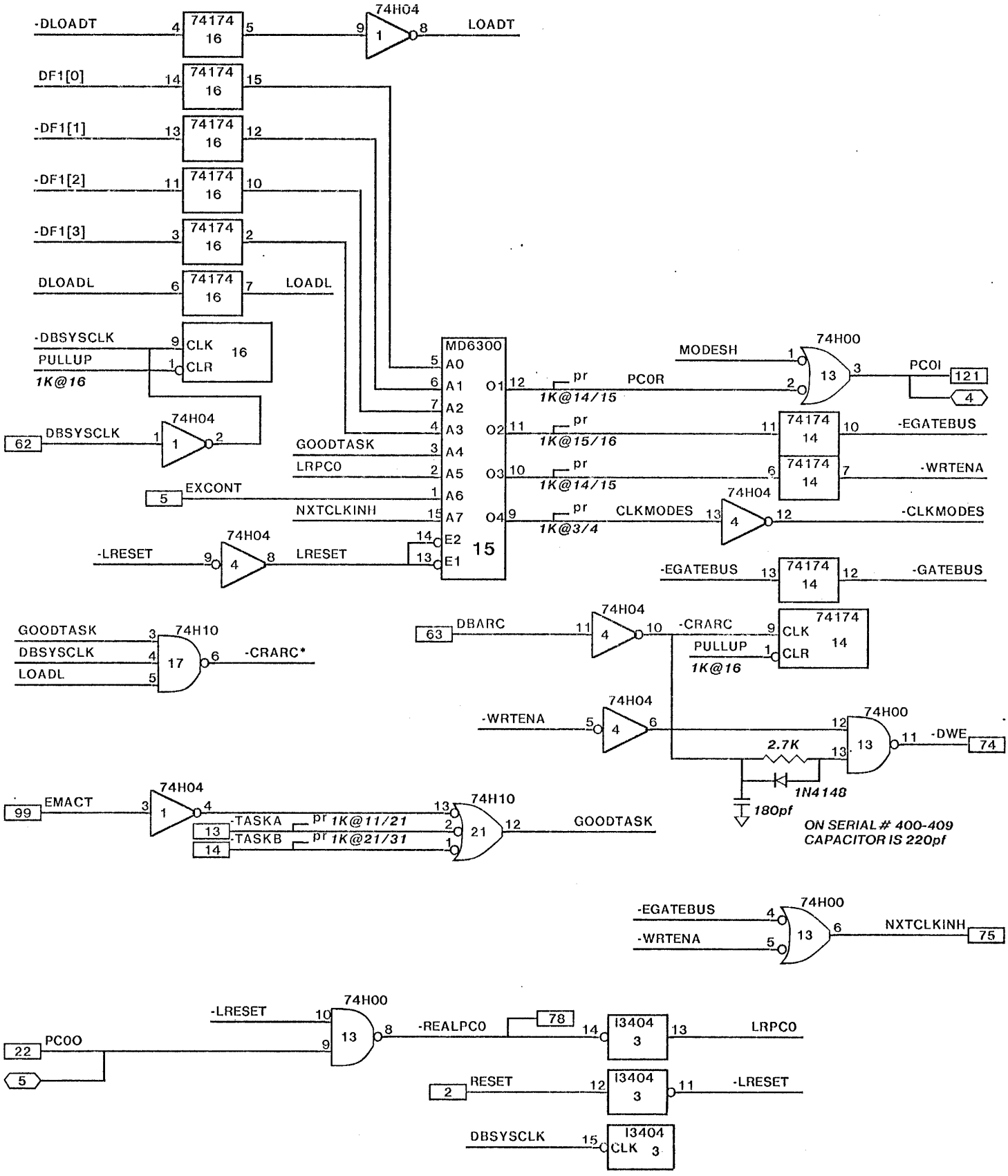


ADDRESS MODIFIERS

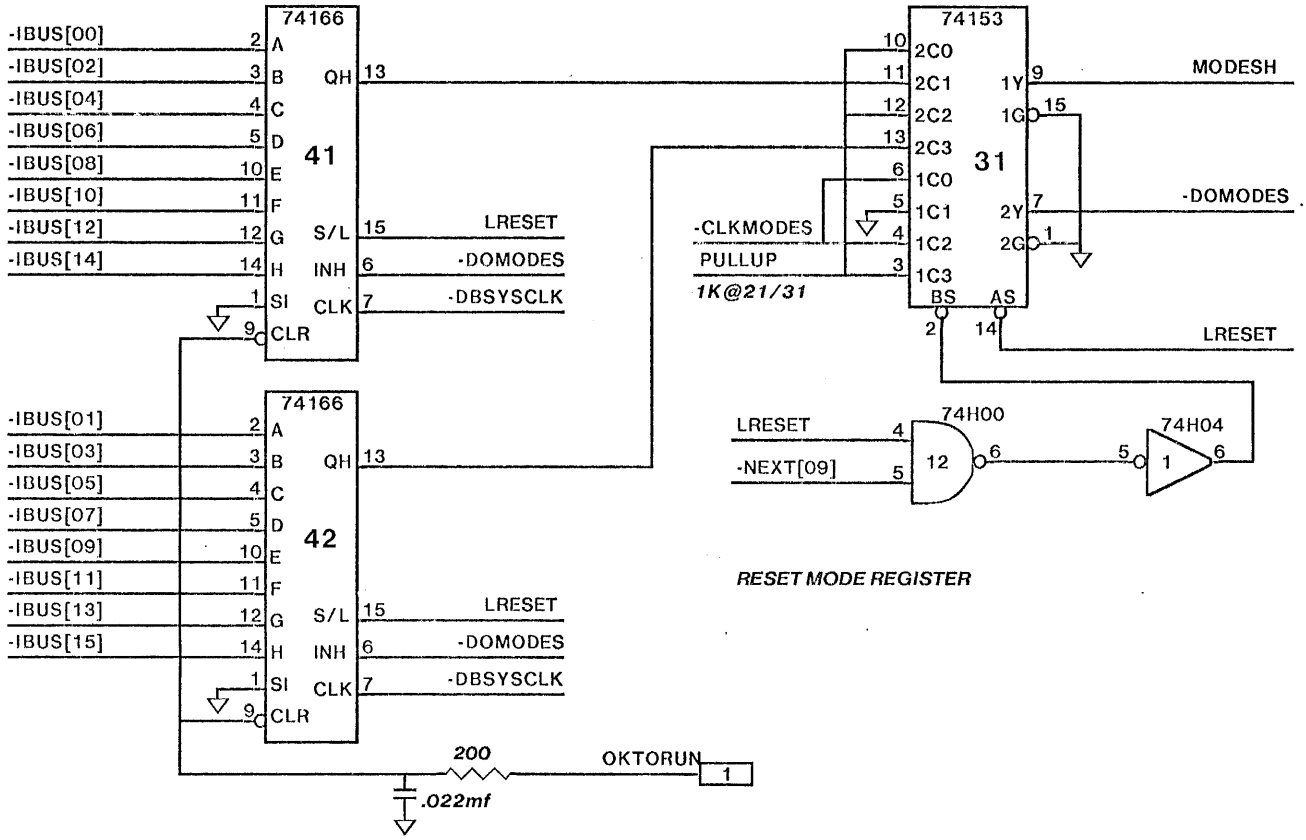

-EMACT
-F2 = 12
MC3002
25
DNS
75
-F2 = 10
-EMACT
MC3002
25
74H01
36
BUS[15]
-NEXT[09]
S8234
65
BUS[00]
BUS[05]
18
-IR[08]
BUS[06]
19
-IR[09]
BUS[07]
-NEXT[06]
-NEXT[07]
-NEXT[08]
-NEXT[09]
S0
S1
74H04
12
74H04
42
10
-IR[00]
74H11
32
F2[0]
F2[1]
74H04
42
-F2 = 14
F2 = 14
74H00
31
74H00
31
74H40
41
-IR[00]
99
EMACT
EMULATOR ADDRESS MODIFIERS
MD6300
53
F2[2]
-IR[01]
-IR[02]
-IR[03]
-IR[04]
-IR[05]
-IR[06]
-IR[07]
-NEXT[06]
-NEXT[07]
-NEXT[08]
-NEXT[09]
"DISP' PROM
I3205
6
F2[3]
F2[2]
F2[1]
-F2[0]
PULLUP
1K@3/13
N.C
-F2 = 17
-F2 = 16
-F2 = 15
-F2 = 14
-F2 = 13
-F2 = 12
-F2 = 11
-F2 = 10
116
51
I3205
3
-STORE
73
-GBUS
-F2 = 7
-F2 = 6
-F2 = 5
-F2 = 4
-F2 = 3
-F2 = 2
-F2 = 1
-F2 = 0
74H04
42
REV'A' AND LATER
74H04
11
-←MDX
I3404
2
←MD
96
-MAR←
MAR←
72
-ZEROBUS
LOADR
68
EMACT
F2 = 14
74H00
7
IR←
71
-XTASK
74H04
12
TASK
-DWTAC
-F2 = 10
MC3002
25
74H04
12
DDR←
6
I3404
CLK 2
CSYSCLK
F2 DECODE AND MISCELLANEOUS

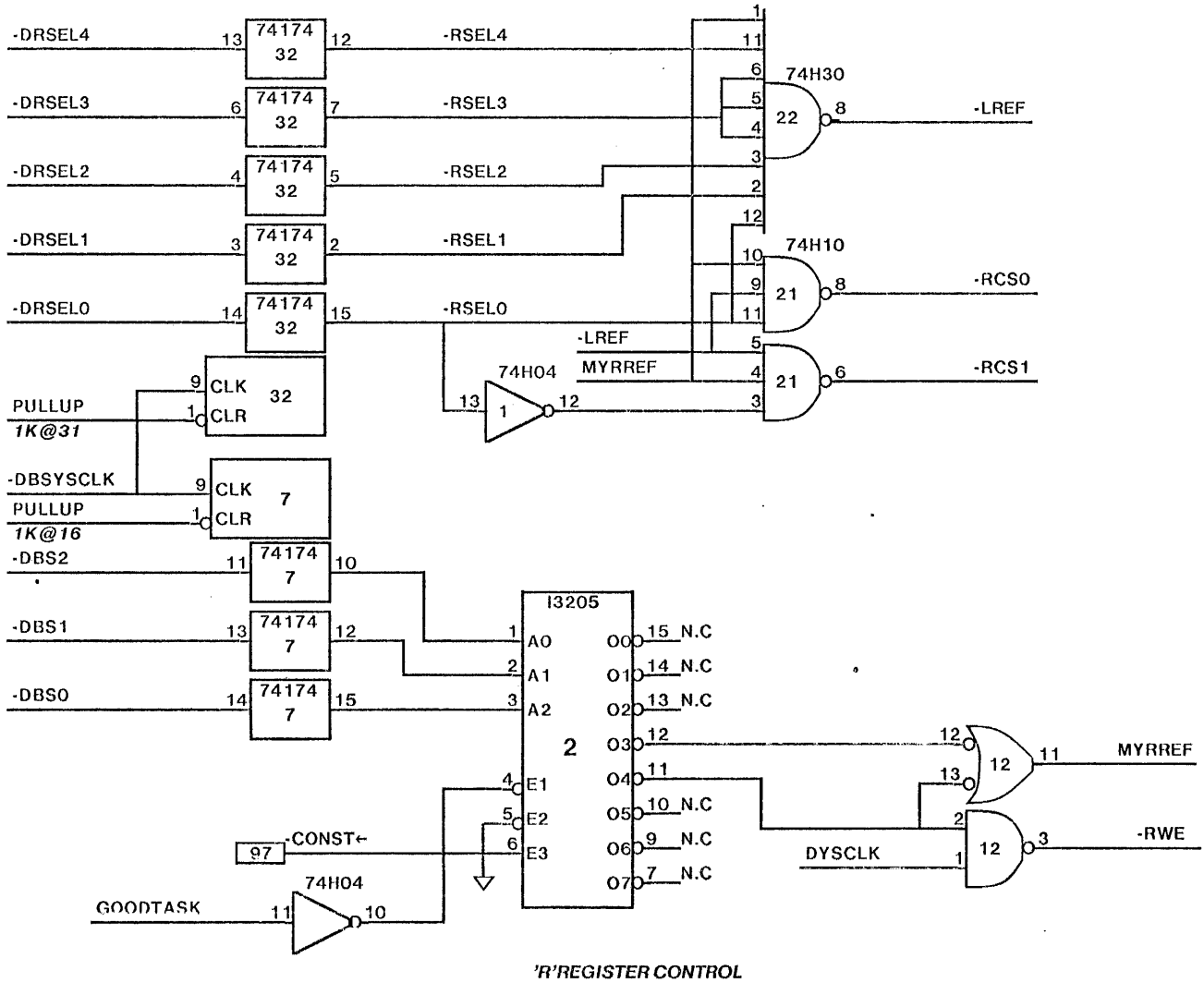


MIR, F1 AND DECODE

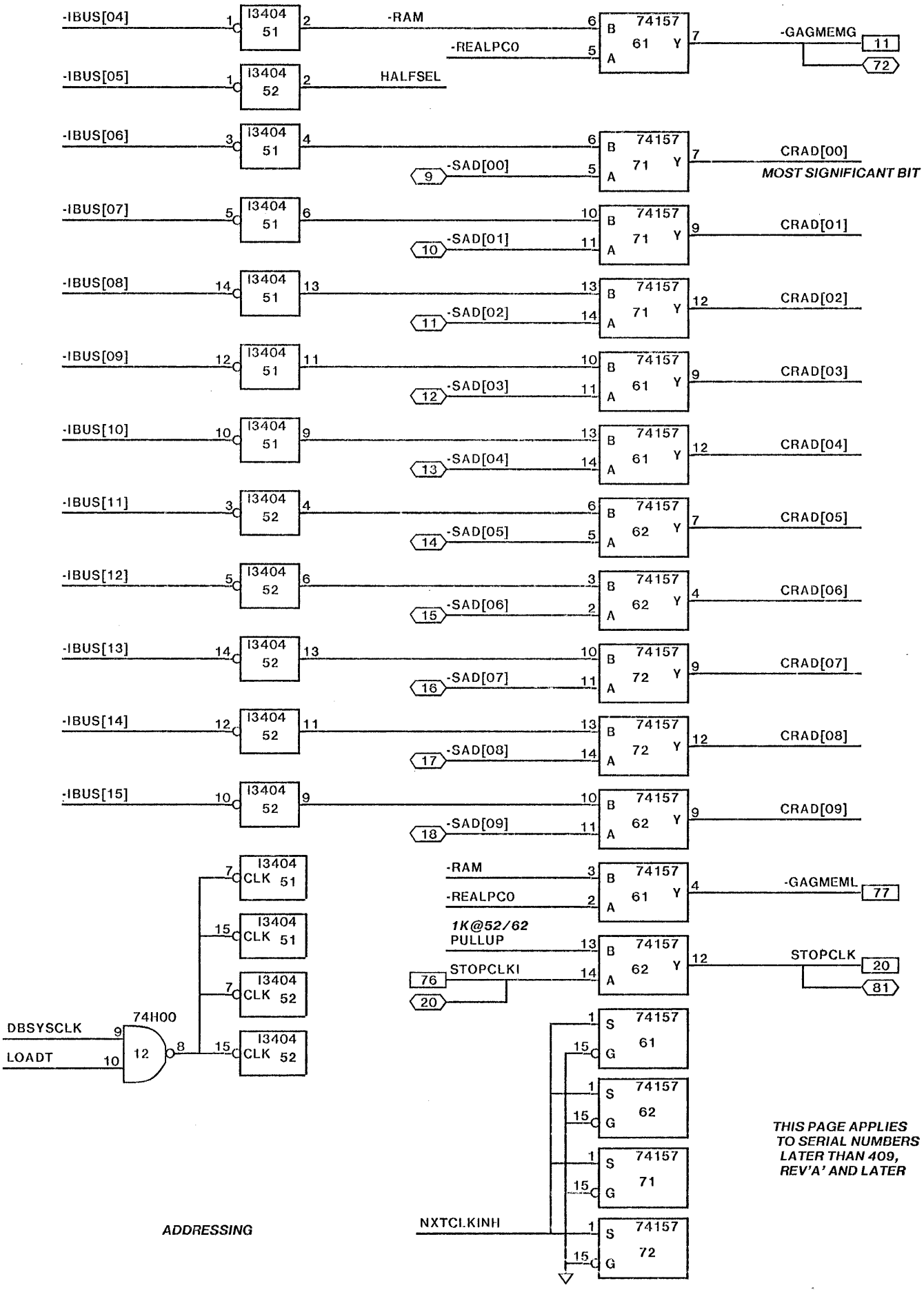


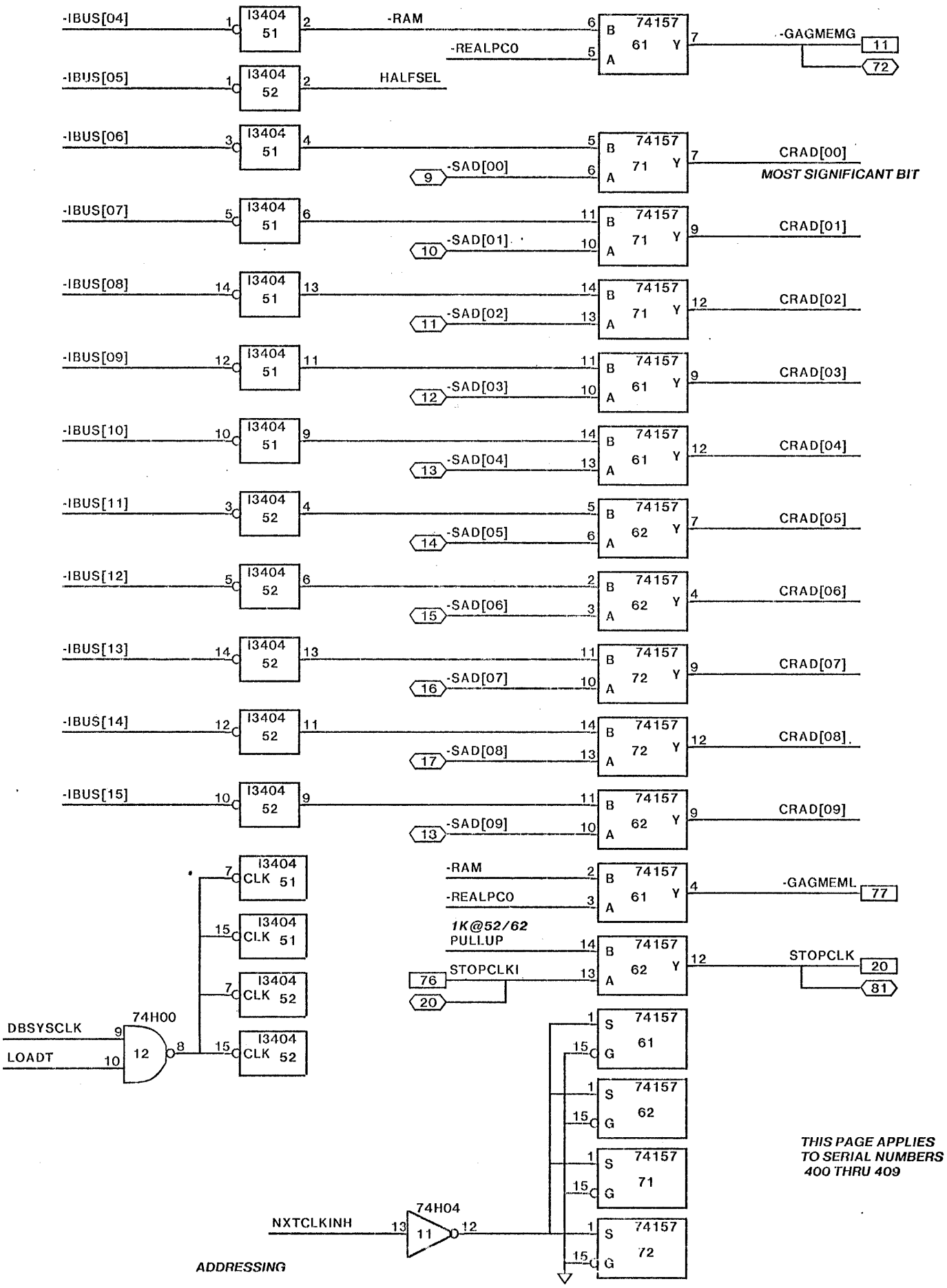
CONTROL SIGNALS

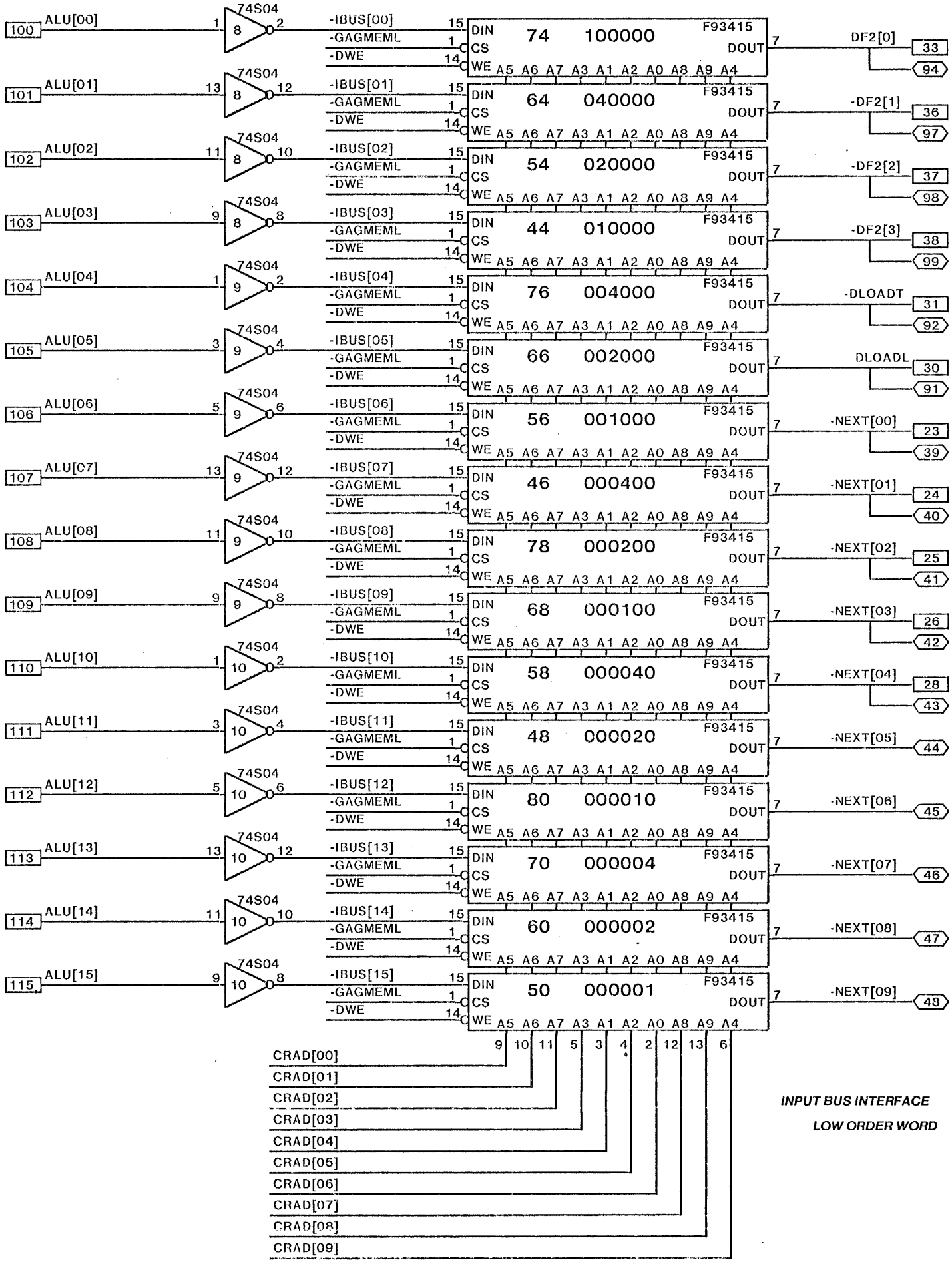


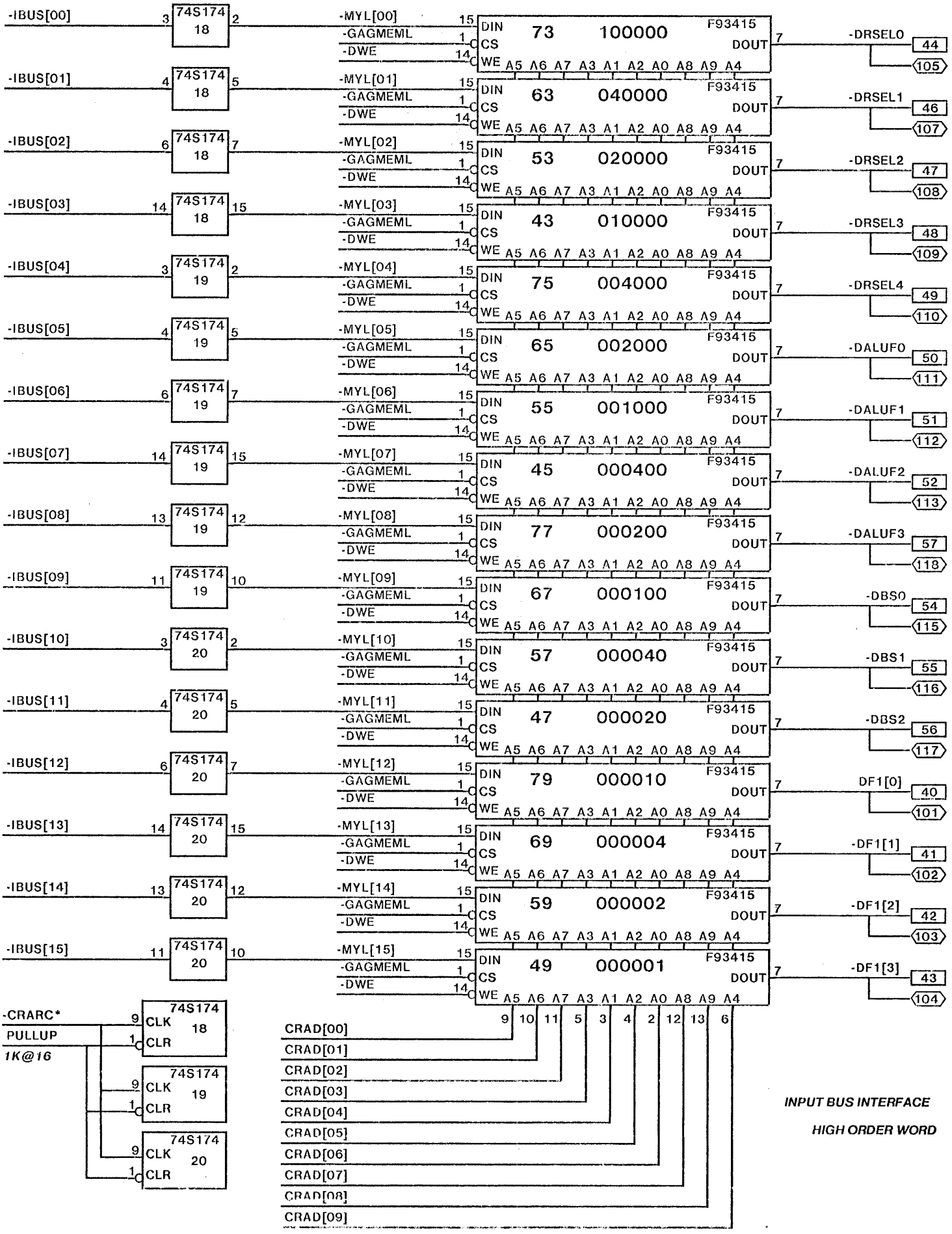


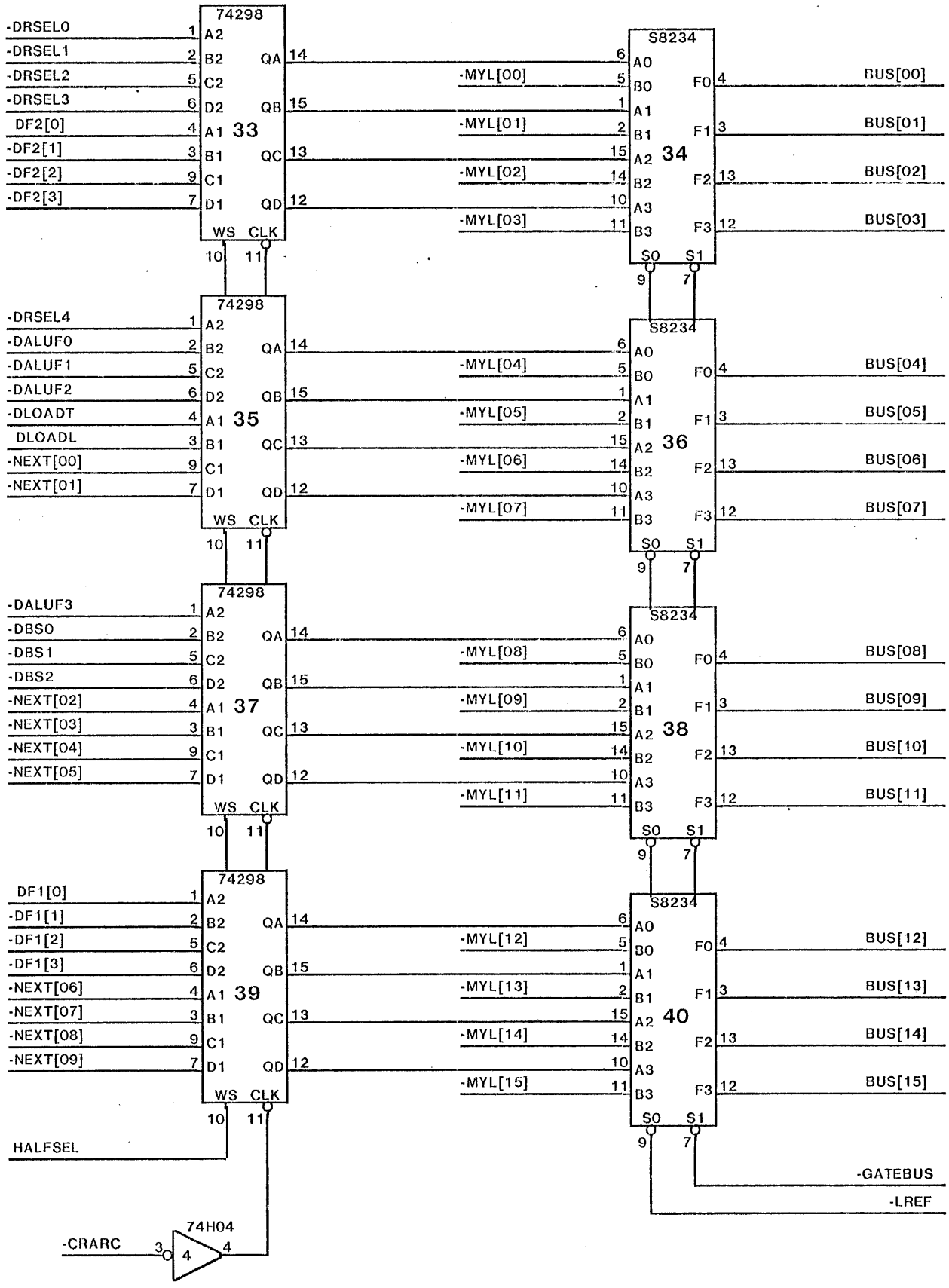
'R' REGISTER CONTROL


-IBUS[04]
-IBUS[05]
-IBUS[06]
-IBUS[07]
-IBUS[08]
-IBUS[09]
-IBUS[10]
-IBUS[11]
-IBUS[12]
-IBUS[13]
-IBUS[14]
-IBUS[15]
I3404 51
I3404 52
-RAM
HALFSEL
-REALPCO
74157 61
74157 71
74157 72
74157 62
-GAGMEMG
-GAGMEML
CRAD[00]
MOST SIGNIFICANT BIT
CRAD[01]
CRAD[02]
CRAD[03]
CRAD[04]
CRAD[05]
CRAD[06]
CRAD[07]
CRAD[08]
CRAD[09]
-SAD[00]
-SAD[01]
-SAD[02]
-SAD[03]
-SAD[04]
-SAD[05]
-SAD[06]
-SAD[07]
-SAD[08]
-SAD[09]
1K@52/62
PULLUP
STOPCLKI
STOPCLK
I3404 CLK 51
I3404 CLK 52
74H00
DBSYSCLK
LOADT
NXTCLKINH
ADDRESSING
THIS PAGE APPLIES TO SERIAL NUMBERS LATER THAN 409, REV'A' AND LATER

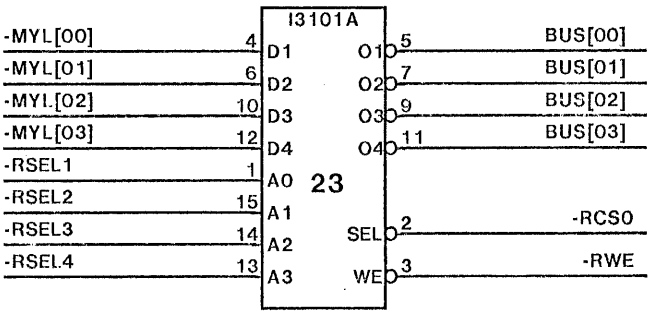

-IBUS[04]
-IBUS[05]
-IBUS[06]
-IBUS[07]
-IBUS[08]
-IBUS[09]
-IBUS[10]
-IBUS[11]
-IBUS[12]
-IBUS[13]
-IBUS[14]
-IBUS[15]
I3404 51
I3404 52
-RAM
HALFSEL
-REALPCO
-SAD[00]
-SAD[01]
-SAD[02]
-SAD[03]
-SAD[04]
-SAD[05]
-SAD[06]
-SAD[07]
-SAD[08]
-SAD[09]
74157 61
74157 71
74157 62
74157 72
-GAGMEMG
CRAD[00]
MOST SIGNIFICANT BIT
CRAD[01]
CRAD[02]
CRAD[03]
CRAD[04]
CRAD[05]
CRAD[06]
CRAD[07]
CRAD[08]
CRAD[09]
-GAGMEML
STOPCLK
STOPCLKI
1K@52/62 PULLUP
I3404 CLK 51
I3404 CLK 52
74H00
DBSYSCLK
LOADT
74H04
NXTCLKINH
ADDRESSING
THIS PAGE APPLIES TO SERIAL NUMBERS 400 THRU 409

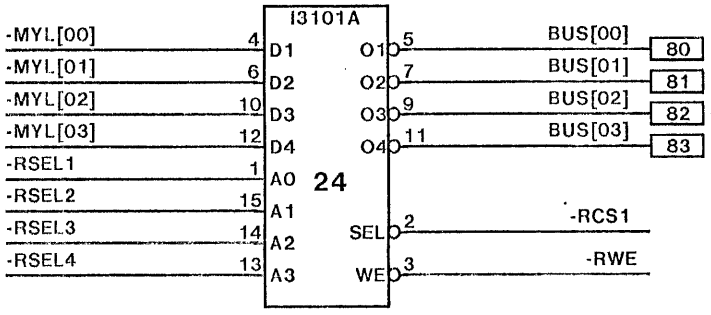

100 ALU[00] 74S04 8 -IBUS[00] -GAGMEML -DWE
101 ALU[01] 74S04 8 -IBUS[01] -GAGMEML -DWE
102 ALU[02] 74S04 8 -IBUS[02] -GAGMEML -DWE
103 ALU[03] 74S04 8 -IBUS[03] -GAGMEML -DWE
104 ALU[04] 74S04 9 -IBUS[04] -GAGMEML -DWE
105 ALU[05] 74S04 9 -IBUS[05] -GAGMEML -DWE
106 ALU[06] 74S04 9 -IBUS[06] -GAGMEML -DWE
107 ALU[07] 74S04 9 -IBUS[07] -GAGMEML -DWE
108 ALU[08] 74S04 9 -IBUS[08] -GAGMEML -DWE
109 ALU[09] 74S04 9 -IBUS[09] -GAGMEML -DWE
110 ALU[10] 74S04 10 -IBUS[10] -GAGMEML -DWE
111 ALU[11] 74S04 10 -IBUS[11] -GAGMEML -DWE
112 ALU[12] 74S04 10 -IBUS[12] -GAGMEML -DWE
113 ALU[13] 74S04 10 -IBUS[13] -GAGMEML -DWE
114 ALU[14] 74S04 10 -IBUS[14] -GAGMEML -DWE
115 ALU[15] 74S04 10 -IBUS[15] -GAGMEML -DWE
DIN CS WE F93415 DOUT
74 100000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
64 040000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
54 020000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
44 010000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
76 004000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
66 002000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
56 001000 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
46 000400 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
78 000200 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
68 000100 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
58 000040 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
48 000020 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
80 000010 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
70 000004 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
60 000002 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
50 000001 A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
DF2[0] 33 94
-DF2[1] 36 97
-DF2[2] 37 98
-DF2[3] 38 99
-DLOADT 31 92
DLOADL 30 91
-NEXT[00] 23 39
-NEXT[01] 24 40
-NEXT[02] 25 41
-NEXT[03] 26 42
-NEXT[04] 28 43
-NEXT[05] 44
-NEXT[06] 45
-NEXT[07] 46
-NEXT[08] 47
-NEXT[09] 48
9 10 11 5 3 4 2 12 13 6
CRAD[00]
CRAD[01]
CRAD[02]
CRAD[03]
CRAD[04]
CRAD[05]
CRAD[06]
CRAD[07]
CRAD[08]
CRAD[09]
INPUT BUS INTERFACE
LOW ORDER WORD

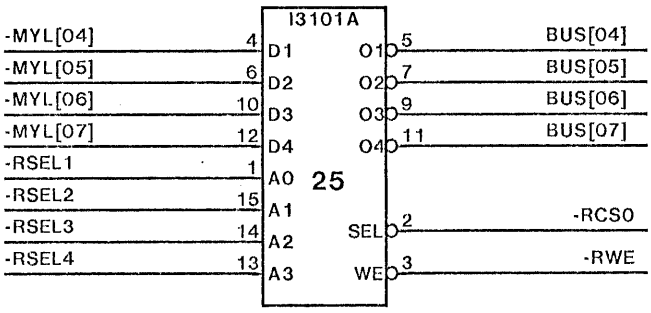

-IBUS[00]
-IBUS[01]
-IBUS[02]
-IBUS[03]
-IBUS[04]
-IBUS[05]
-IBUS[06]
-IBUS[07]
-IBUS[08]
-IBUS[09]
-IBUS[10]
-IBUS[11]
-IBUS[12]
-IBUS[13]
-IBUS[14]
-IBUS[15]
74S174 18
74S174 19
74S174 20
-MYL[00]
-MYL[01]
-MYL[02]
-MYL[03]
-MYL[04]
-MYL[05]
-MYL[06]
-MYL[07]
-MYL[08]
-MYL[09]
-MYL[10]
-MYL[11]
-MYL[12]
-MYL[13]
-MYL[14]
-MYL[15]
-GAGMEML
-DWE
DIN
CS
WE
DOUT
F93415
73 100000
63 040000
53 020000
43 010000
75 004000
65 002000
55 001000
45 000400
77 000200
67 000100
57 000040
47 000020
79 000010
69 000004
59 000002
49 000001
A5 A6 A7 A3 A1 A2 A0 A8 A9 A4
-DRSEL0
-DRSEL1
-DRSEL2
-DRSEL3
-DRSEL4
-DALUF0
-DALUF1
-DALUF2
-DALUF3
-DBS0
-DBS1
-DBS2
DF1[0]
-DF1[1]
-DF1[2]
-DF1[3]
-CRARC*
PULLUP
1K@16
CLK
CLR
CRAD[00]
CRAD[01]
CRAD[02]
CRAD[03]
CRAD[04]
CRAD[05]
CRAD[06]
CRAD[07]
CRAD[08]
CRAD[09]
INPUT BUS INTERFACE
HIGH ORDER WORD

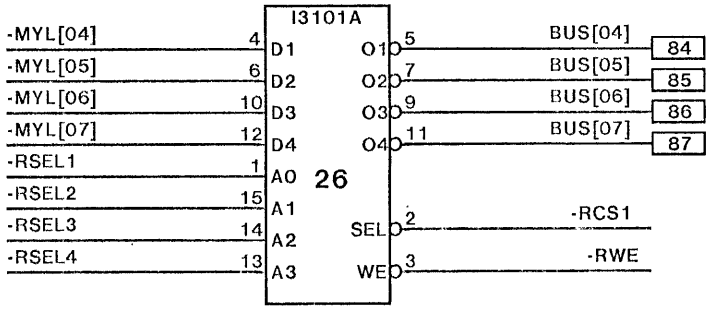


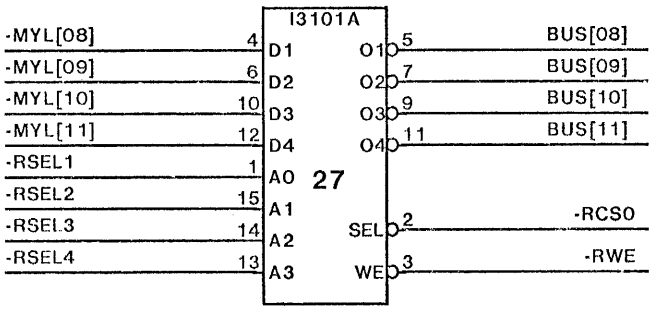
OUTPUT BUS INTERFACE

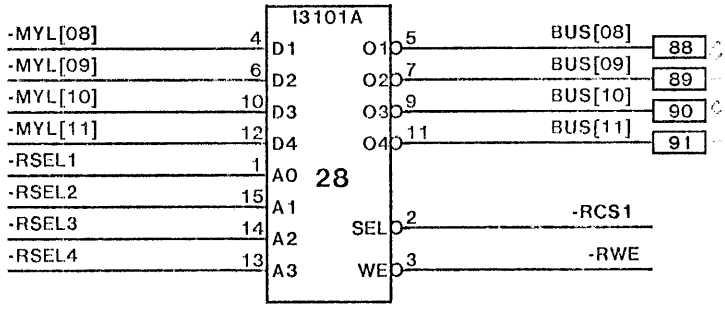

I3101A
23
-MYL[00] 4
-MYL[01] 6
-MYL[02] 10
-MYL[03] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[00]
BUS[01]
BUS[02]
BUS[03]
-RCS0
-RWE

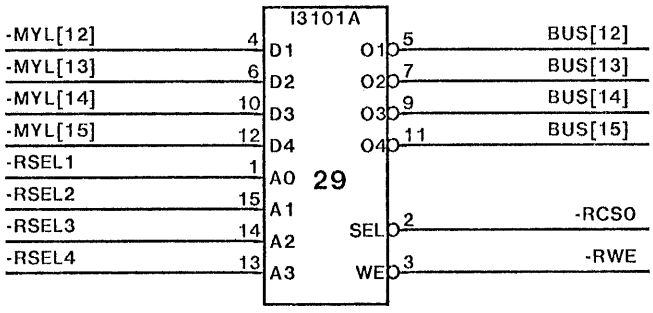

I3101A
24
-MYL[00] 4
-MYL[01] 6
-MYL[02] 10
-MYL[03] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[00] 80
BUS[01] 81
BUS[02] 82
BUS[03] 83
-RCS1
-RWE


I3101A
25
-MYL[04] 4
-MYL[05] 6
-MYL[06] 10
-MYL[07] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[04]
BUS[05]
BUS[06]
BUS[07]
-RCS0
-RWE

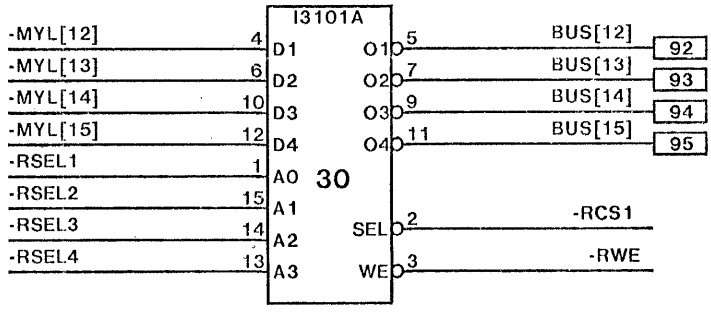

I3101A
26
-MYL[04] 4
-MYL[05] 6
-MYL[06] 10
-MYL[07] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[04] 84
BUS[05] 85
BUS[06] 86
BUS[07] 87
-RCS1
-RWE


I3101A
27
-MYL[08] 4
-MYL[09] 6
-MYL[10] 10
-MYL[11] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[08]
BUS[09]
BUS[10]
BUS[11]
-RCS0
-RWE

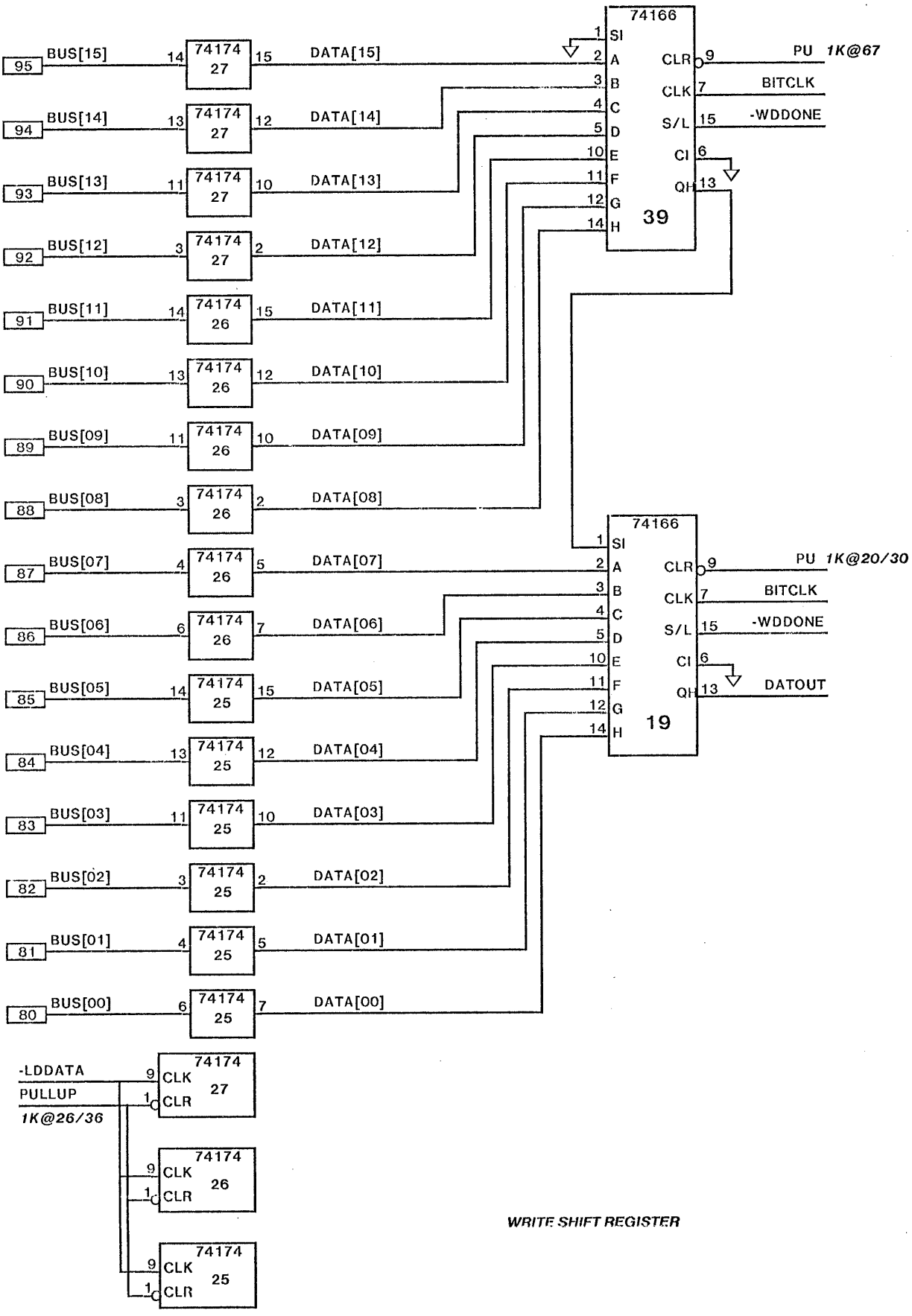

I3101A
28
-MYL[08] 4
-MYL[09] 6
-MYL[10] 10
-MYL[11] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[08] 88
BUS[09] 89
BUS[10] 90
BUS[11] 91
-RCS1
-RWE


I3101A
29
-MYL[12] 4
-MYL[13] 6
-MYL[14] 10
-MYL[15] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[12]
BUS[13]
BUS[14]
BUS[15]
-RCS0
-RWE

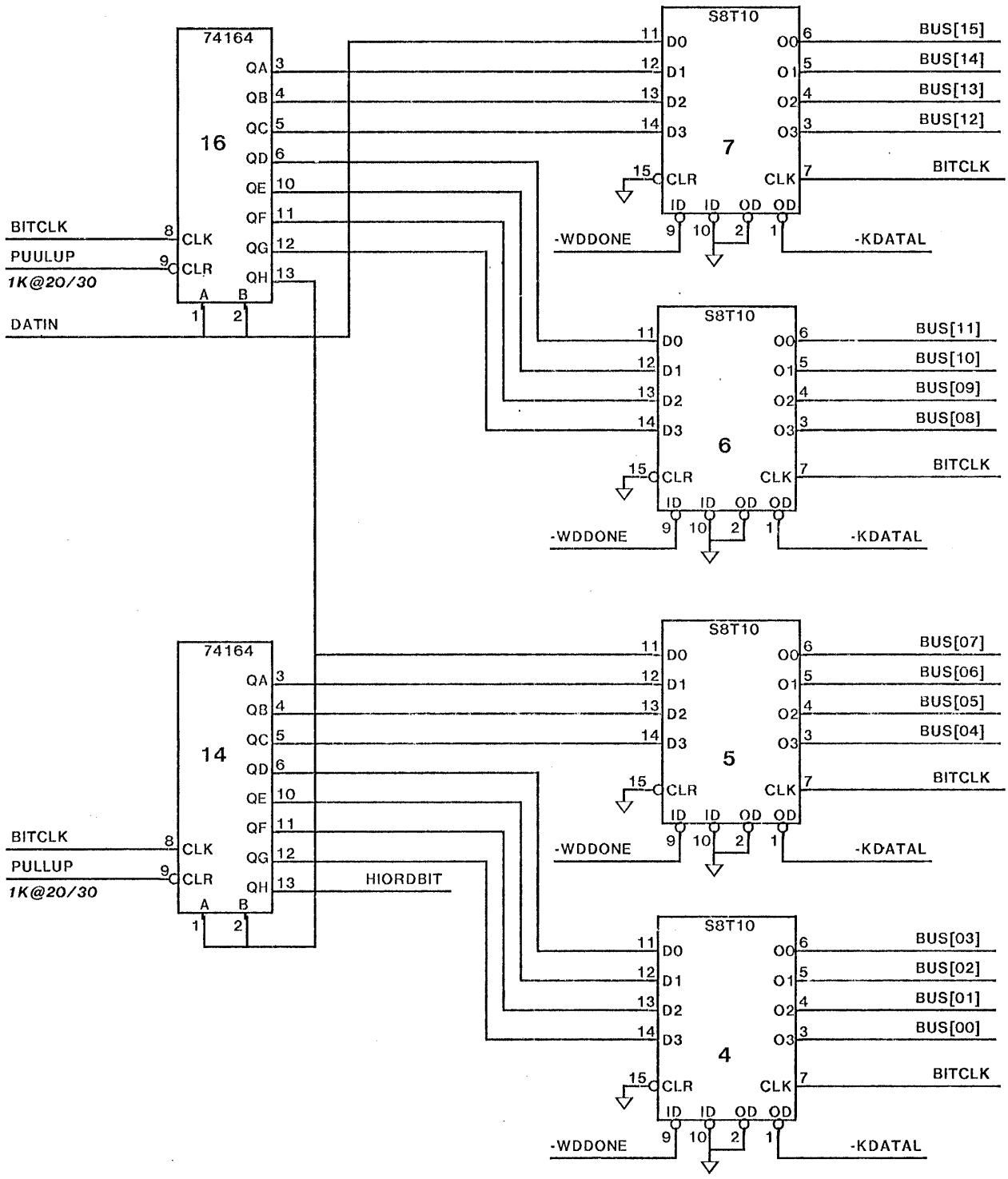
(41-57)


I3101A
30
-MYL[12] 4
-MYL[13] 6
-MYL[14] 10
-MYL[15] 12
-RSEL1 1
-RSEL2 15
-RSEL3 14
-RSEL4 13
D1 D2 D3 D4 A0 A1 A2 A3
O1 O2 O3 O4 SEL WE
5 7 9 11 2 3
BUS[12] 92
BUS[13] 93
BUS[14] 94
BUS[15] 95
-RCS1
-RWE

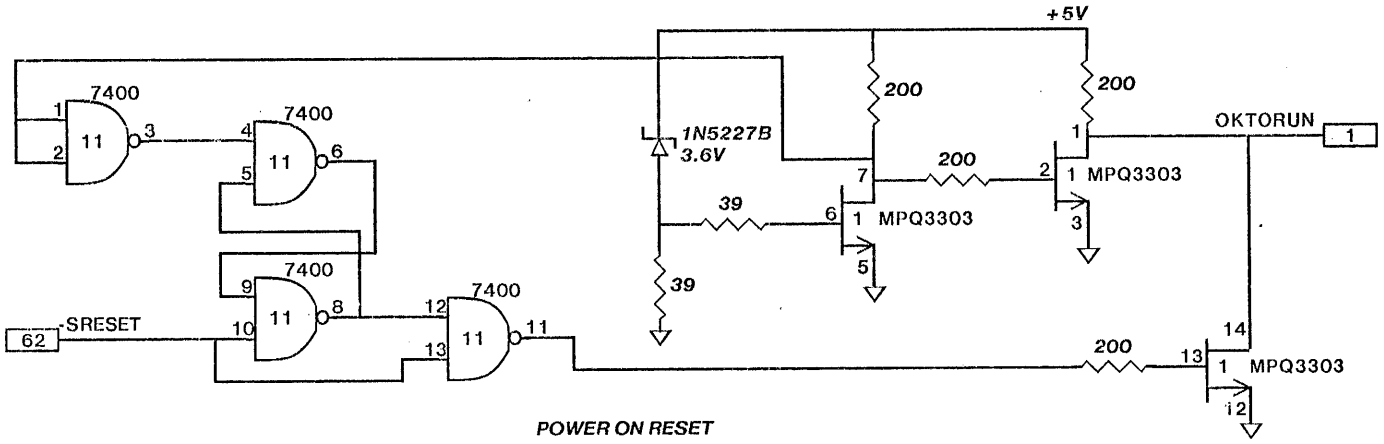
(60-77)



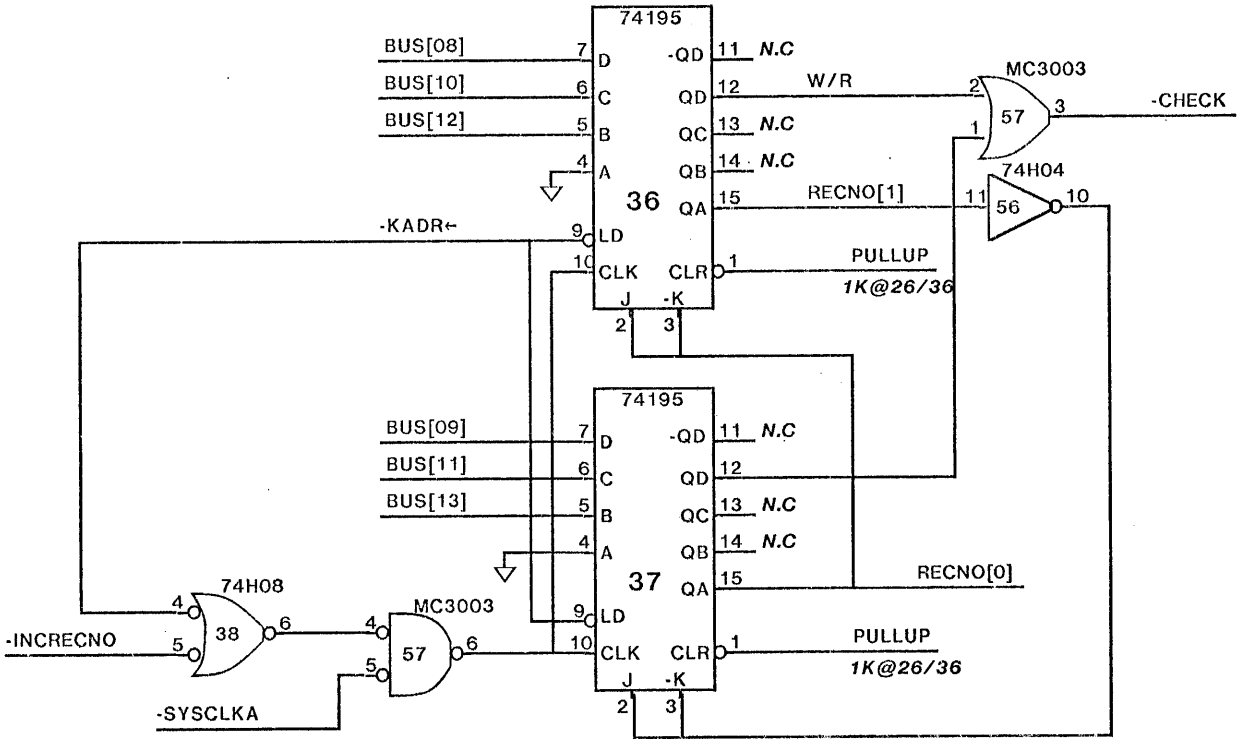
WRITE SHIFT REGISTER

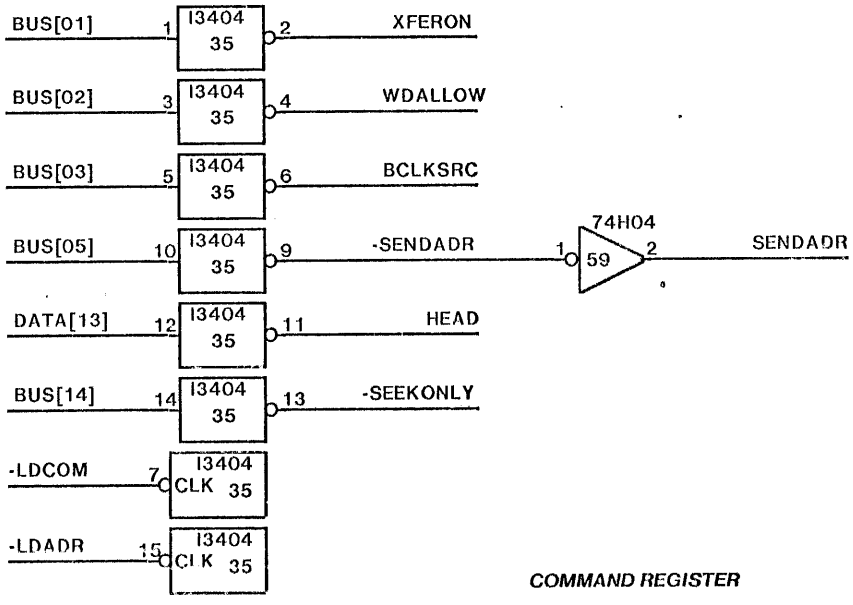


READ SHIFT REGISTER

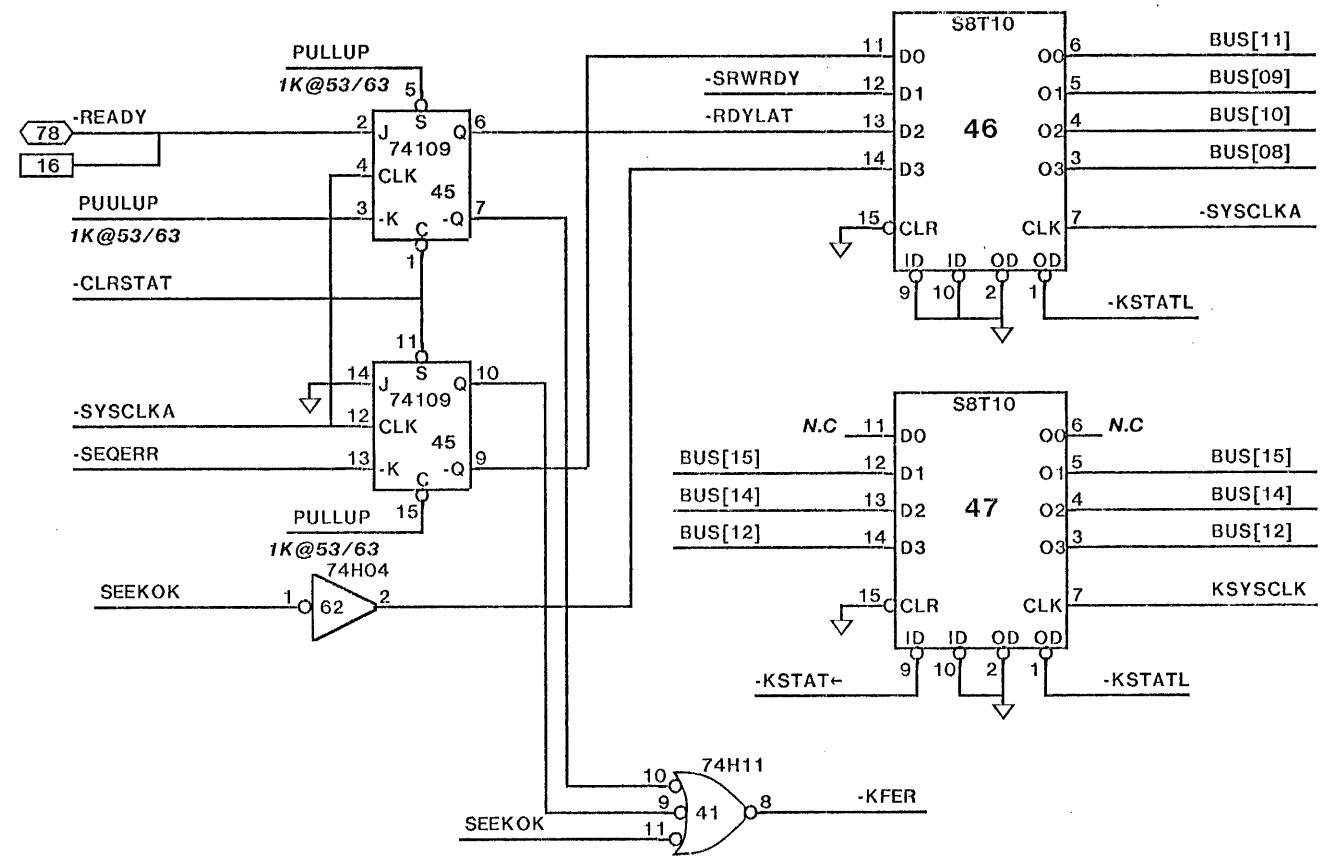


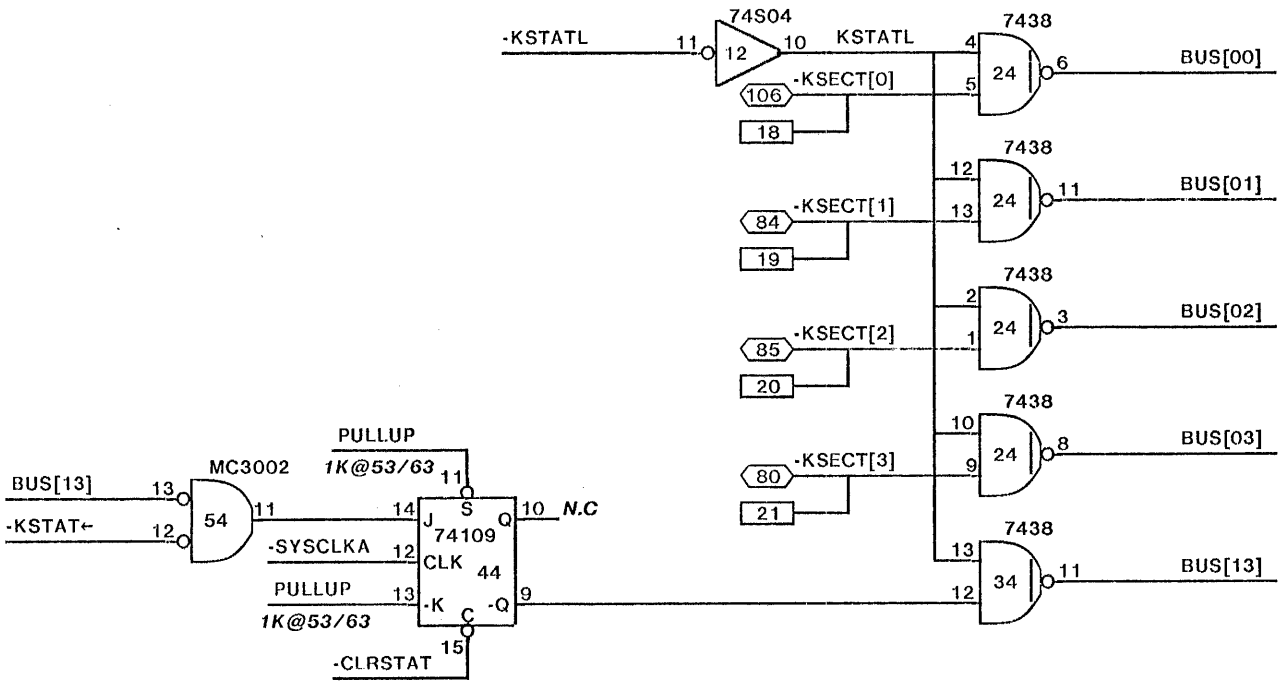
POWER ON RESET



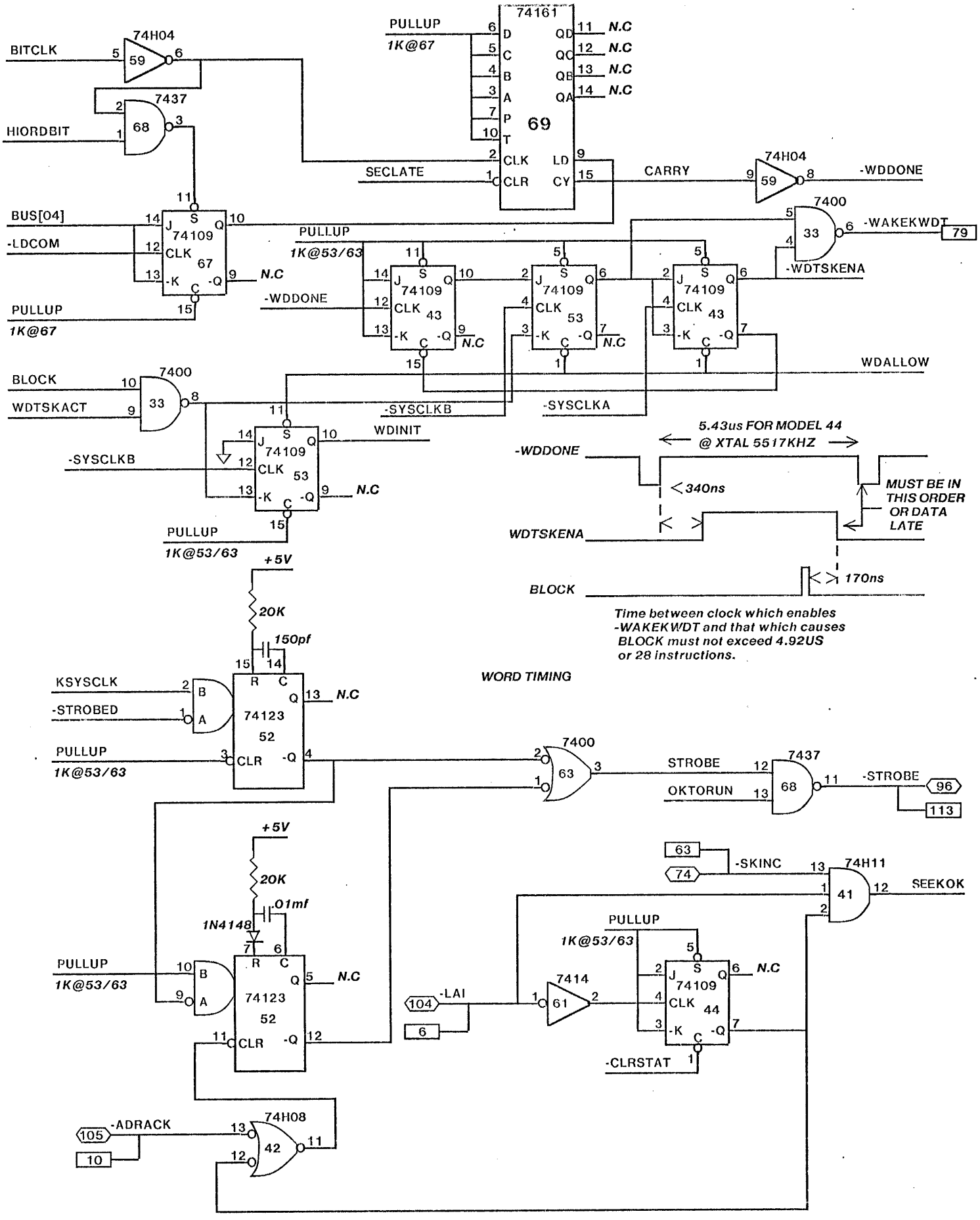


COMMAND REGISTER

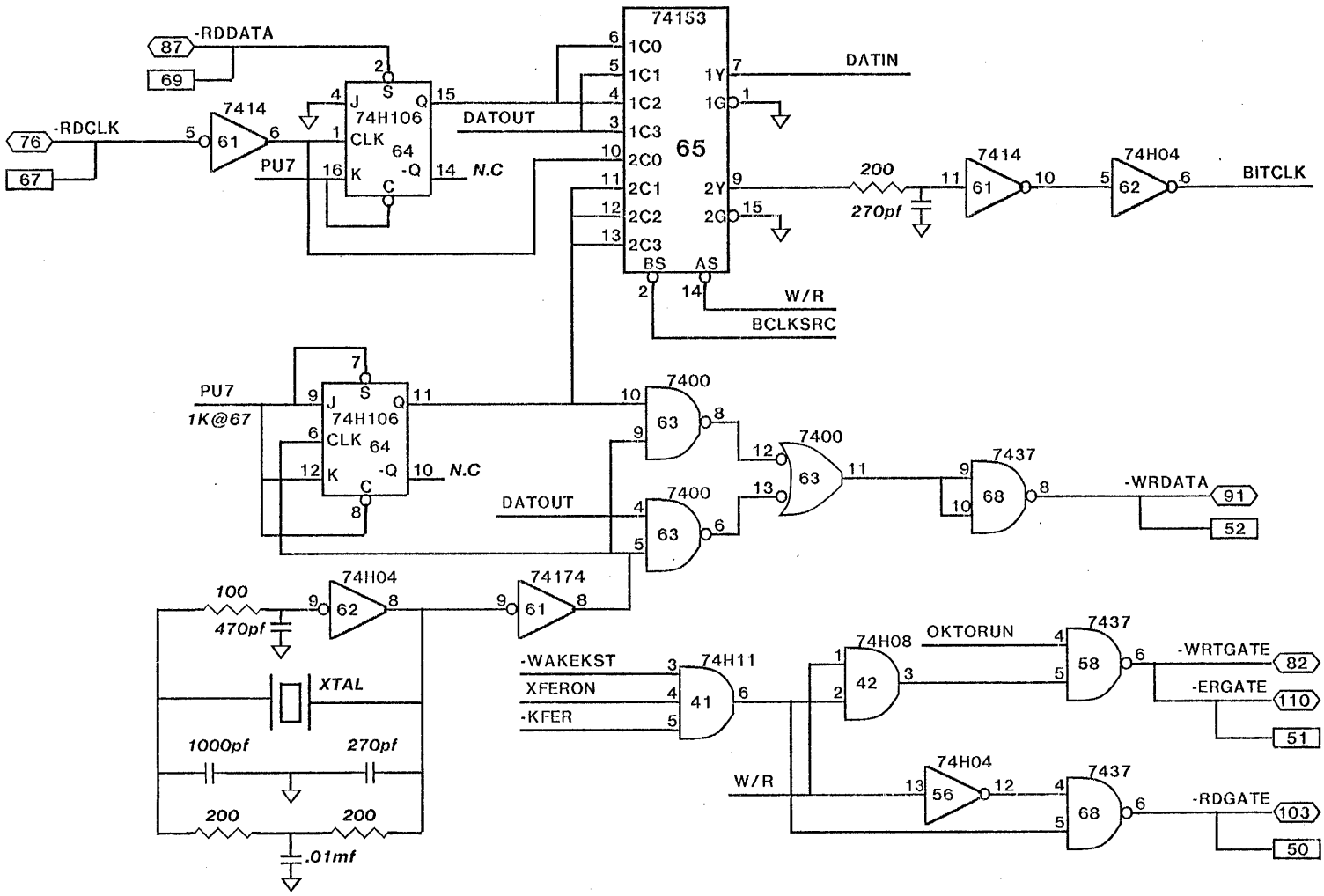

PULLUP
1K@53/63
-READY
78
16
74109
45
PUULUP
1K@53/63
-CLRSTAT
-SYSCLKA
-SEQERR
74H04
SEEKOK
62
S8T10
46
-SRWRDY
-RDYLAT
BUS[11]
BUS[09]
BUS[10]
BUS[08]
-SYSCLKA
-KSTATL
47
N.C
BUS[15]
BUS[14]
BUS[12]
KSYSCLK
-KSTAT←
74H11
41
-KFER


74S04
-KSTATL
KSTATL
7438
-KSECT[0]
106
18
BUS[00]
-KSECT[1]
84
19
BUS[01]
-KSECT[2]
85
20
BUS[02]
-KSECT[3]
80
21
BUS[03]
BUS[13]
34
MC3002
54
BUS[13]
-KSTAT←
PULLUP
1K@53/63
74109
44
-SYSCLKA
PULLUP
1K@53/63
-CLRSTAT
N.C

STATUS

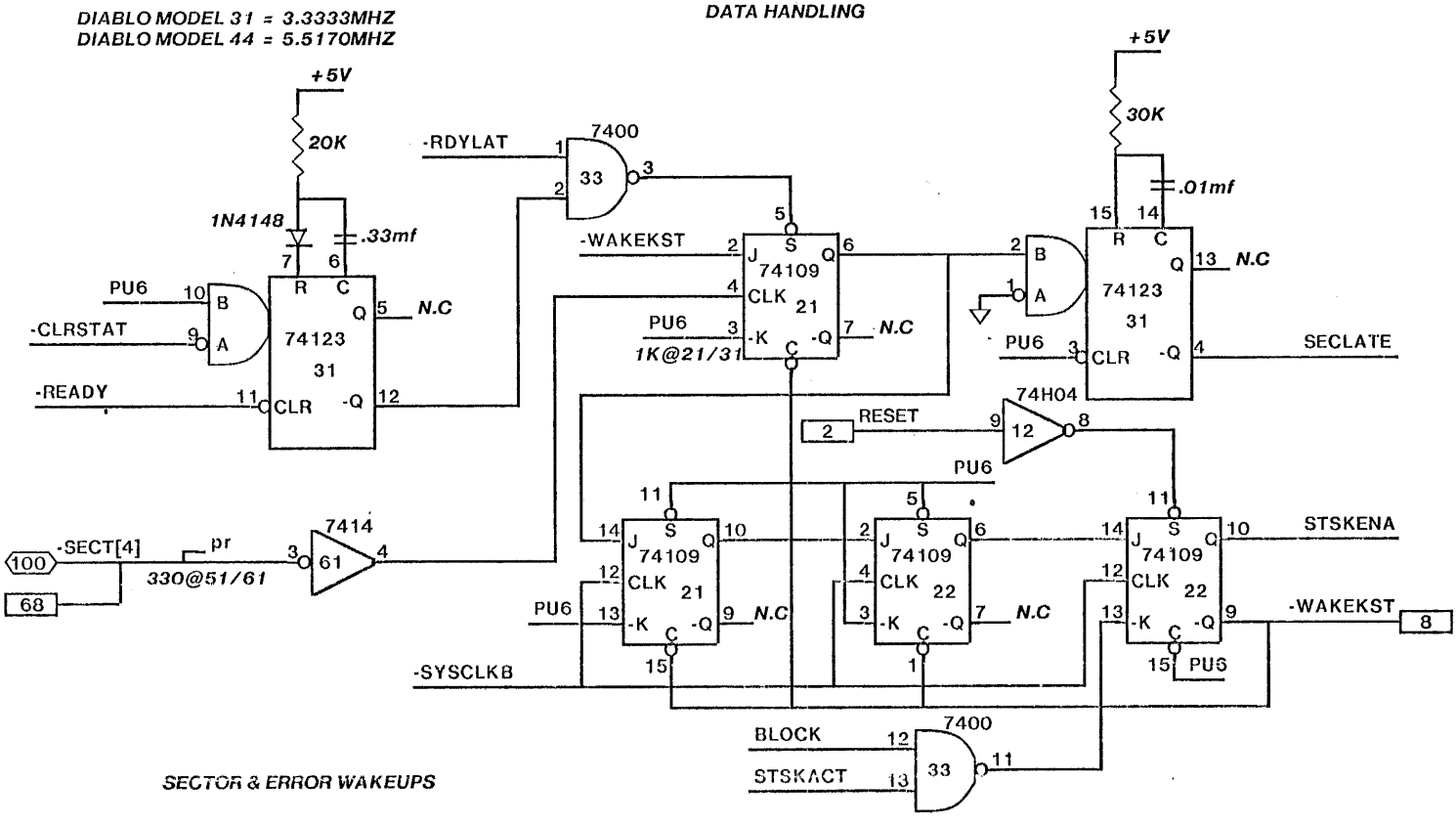


STROBE AND SEEK ERRORS

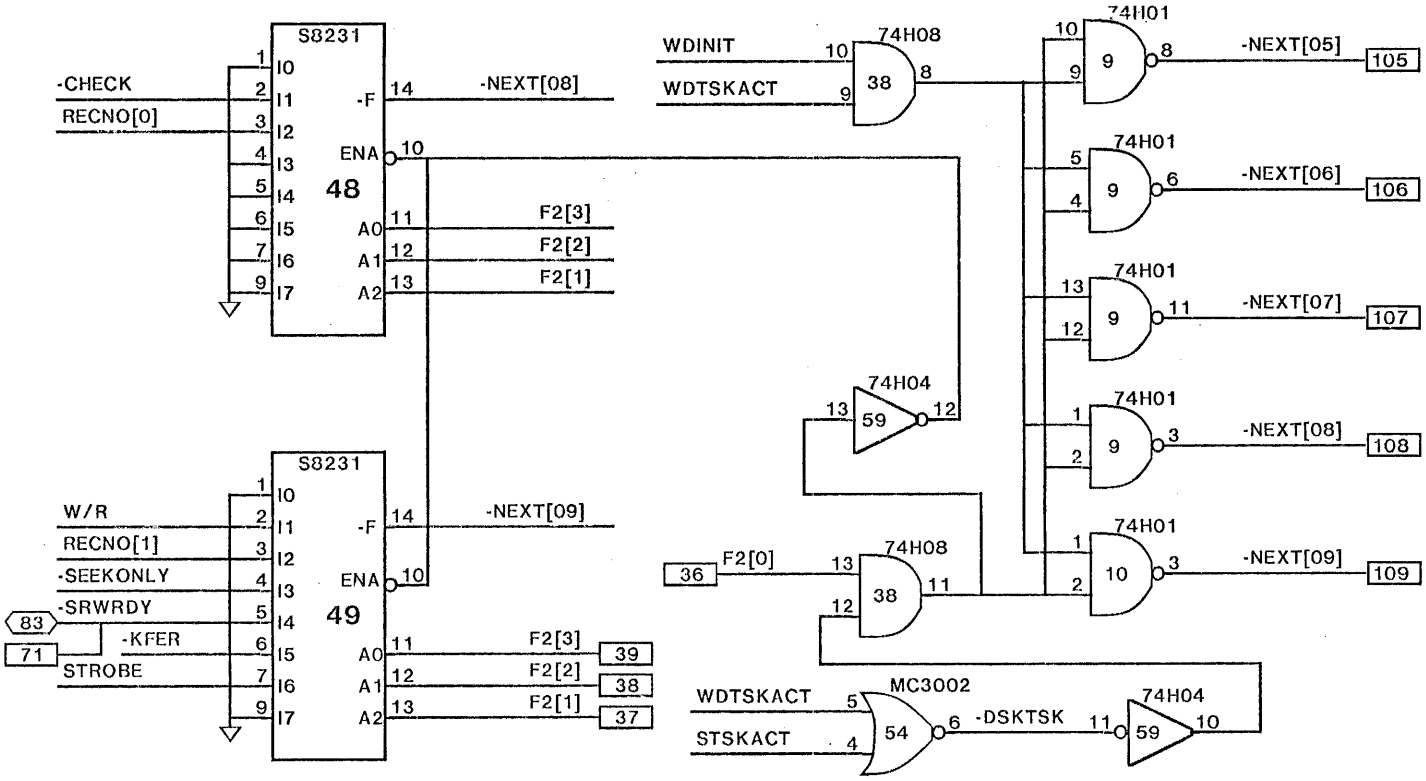


CRYSTAL FREQUENCY IS DISK DEPENDENT
DIABLO MODEL 31 = 3.3333MHZ
DIABLO MODEL 44 = 5.5170MHZ

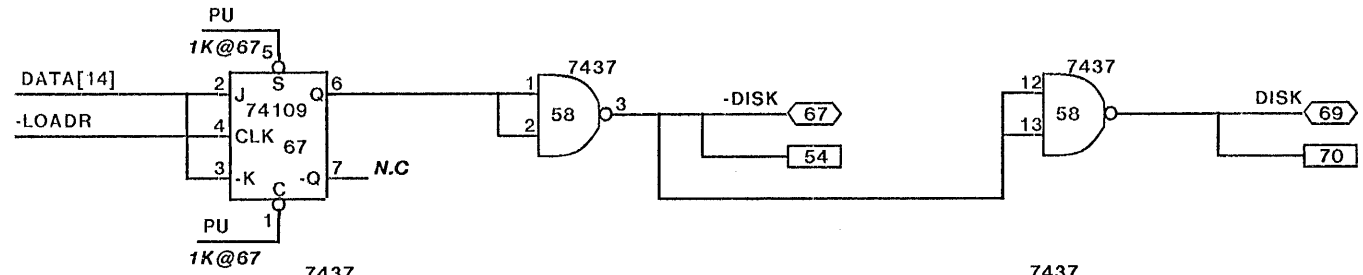
DATA HANDLING

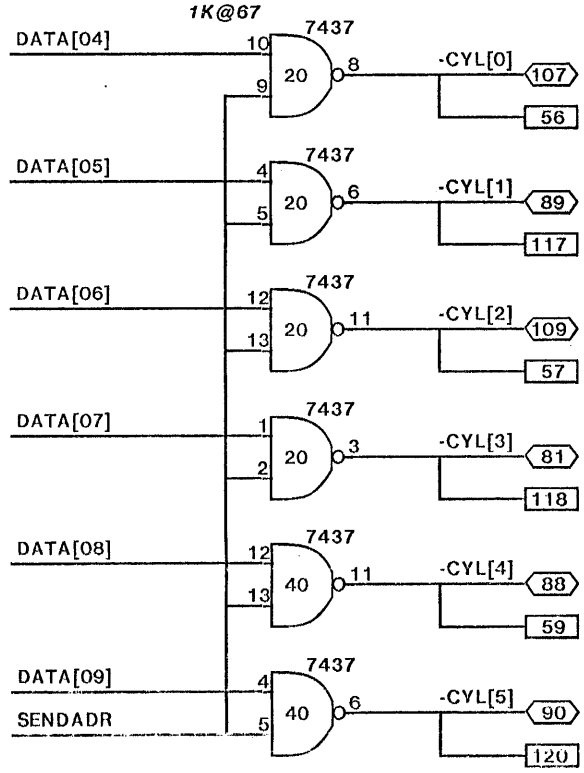


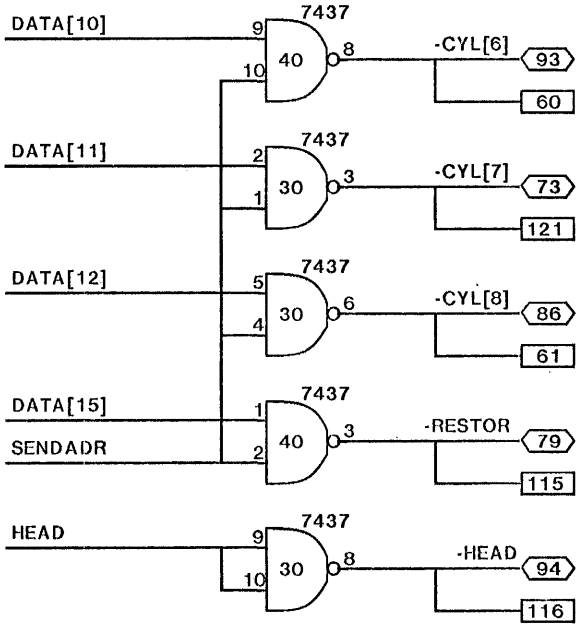
SECTOR & ERROR WAKEUPS



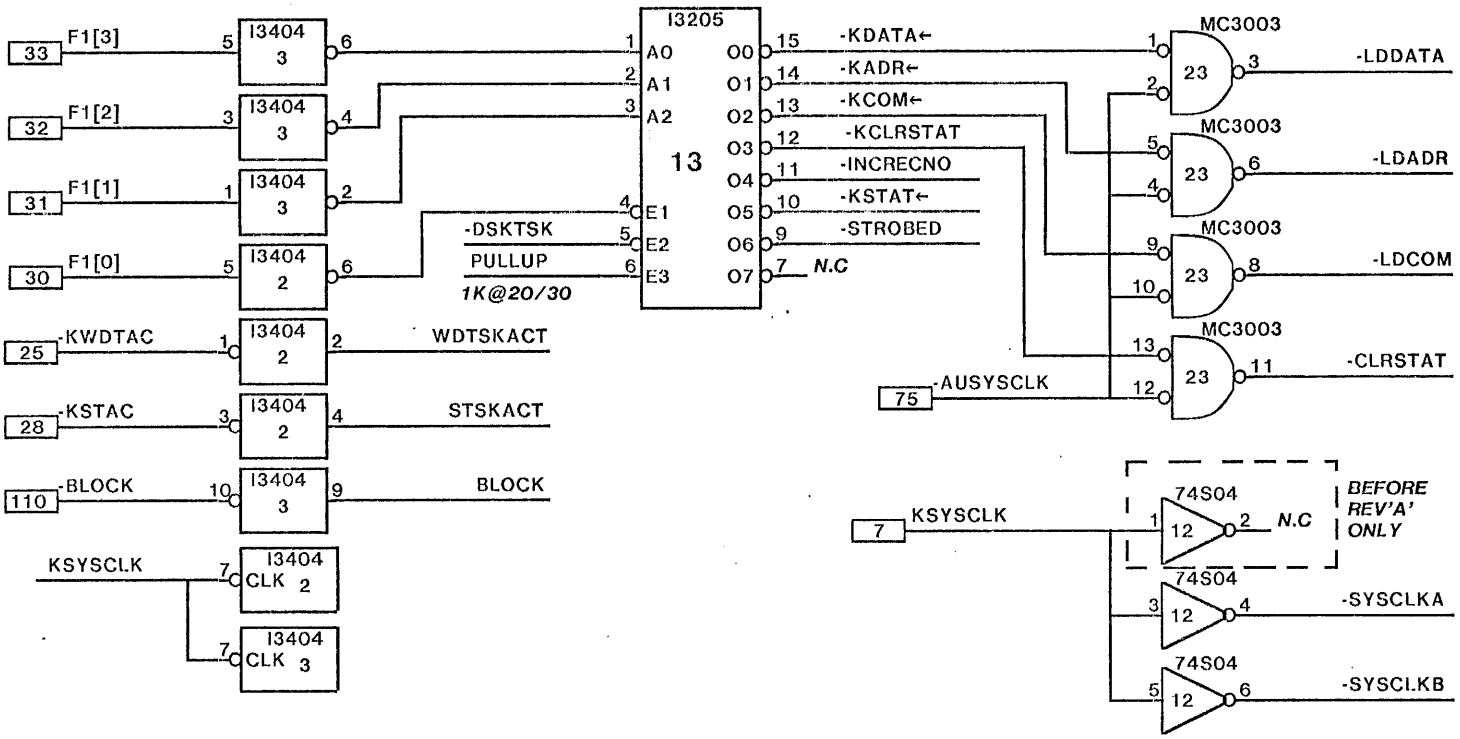
ADDRESS MODIFIERS

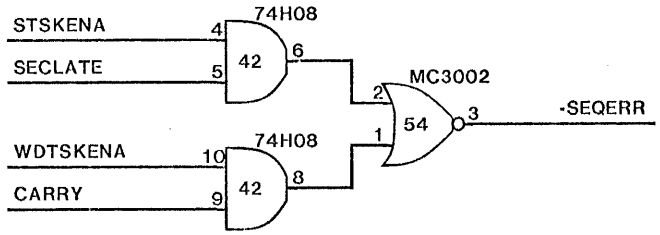


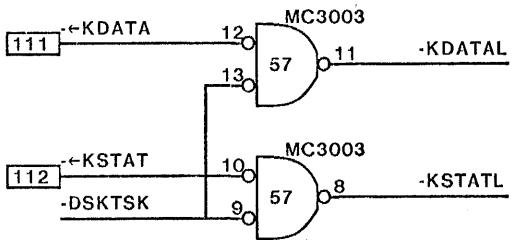




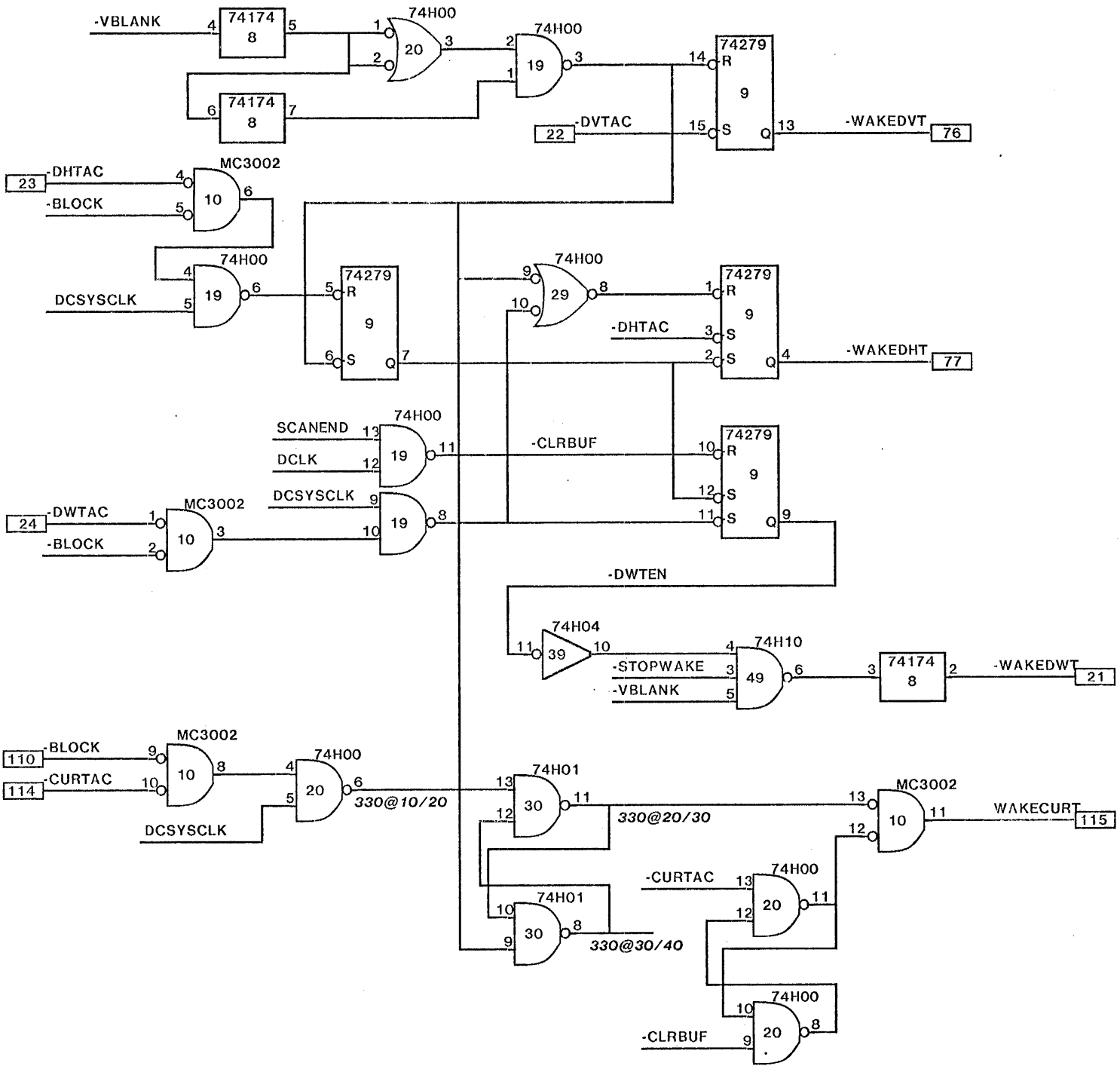
DISK ADDRESSING



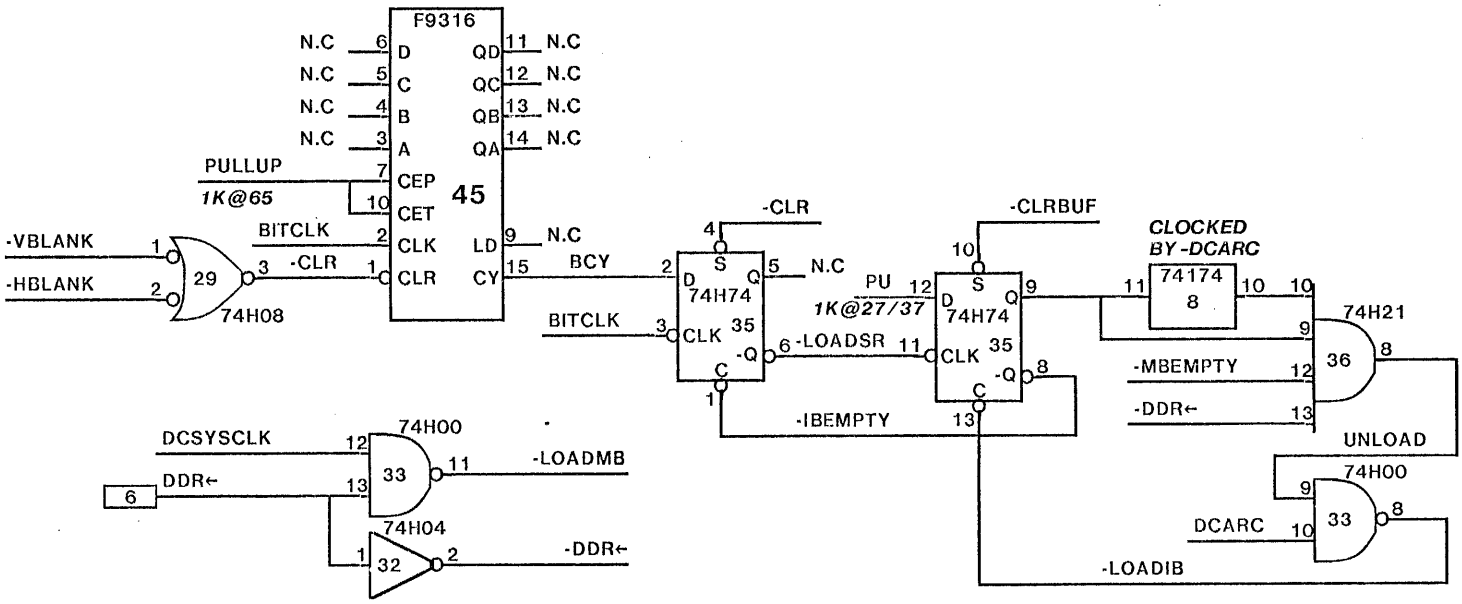


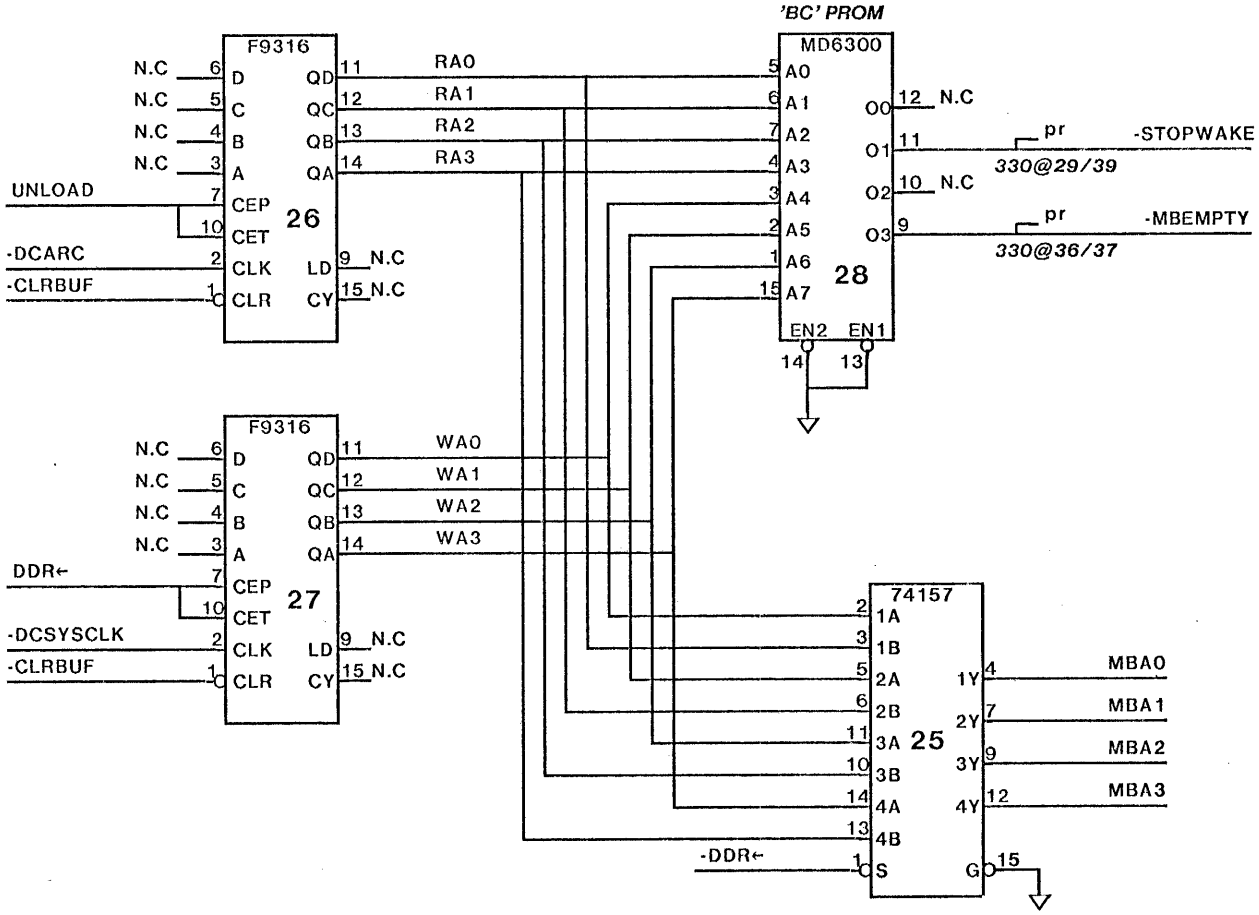


F DECODE AND CLOCKS

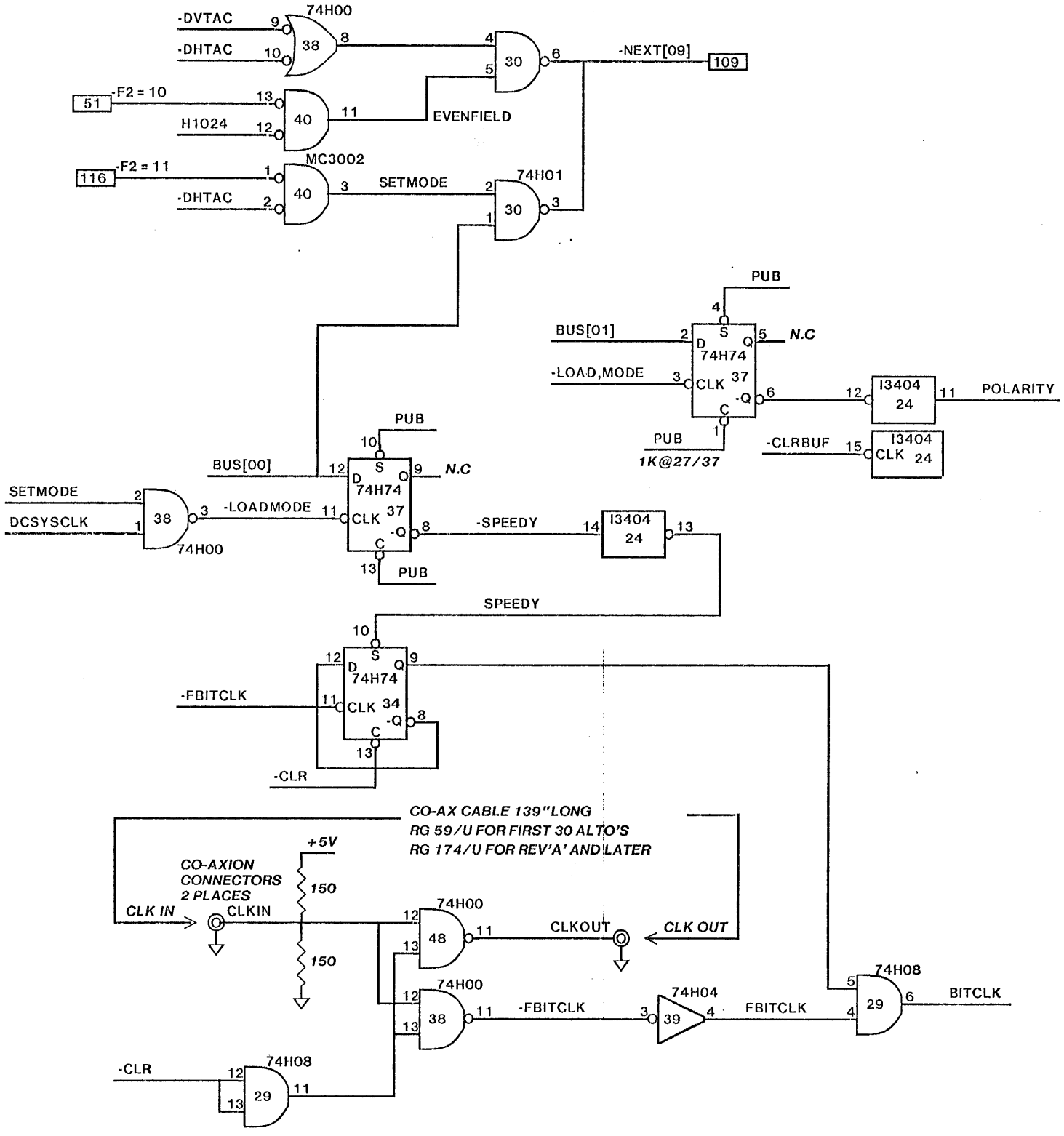

-VBLANK
74174 8
74H00 20
74H00 19
74279 9
-DVTAC
22
-WAKEDVT
76
-DHTAC
23
-BLOCK
MC3002 10
74H00 19
DCSYSCLK
74279 9
74H00 29
-DHTAC
-WAKEDHT
77
SCANEND
DCLK
74H00 19
-CLRBUF
DCSYSCLK
74H00 19
-DWTAC
24
-BLOCK
MC3002 10
-DWTEN
74H04 39
-STOPWAKE
-VBLANK
74H10 49
74174 8
-WAKEDWT
21
110
-BLOCK
114
-CURTAC
MC3002 10
74H00 20
330@10/20
DCSYSCLK
74H01 30
330@20/30
MC3002 10
WAKECURT
115
-CURTAC
74H00 20
74H01 30
330@30/40
74H00 20
-CLRBUF

WAKEUPS

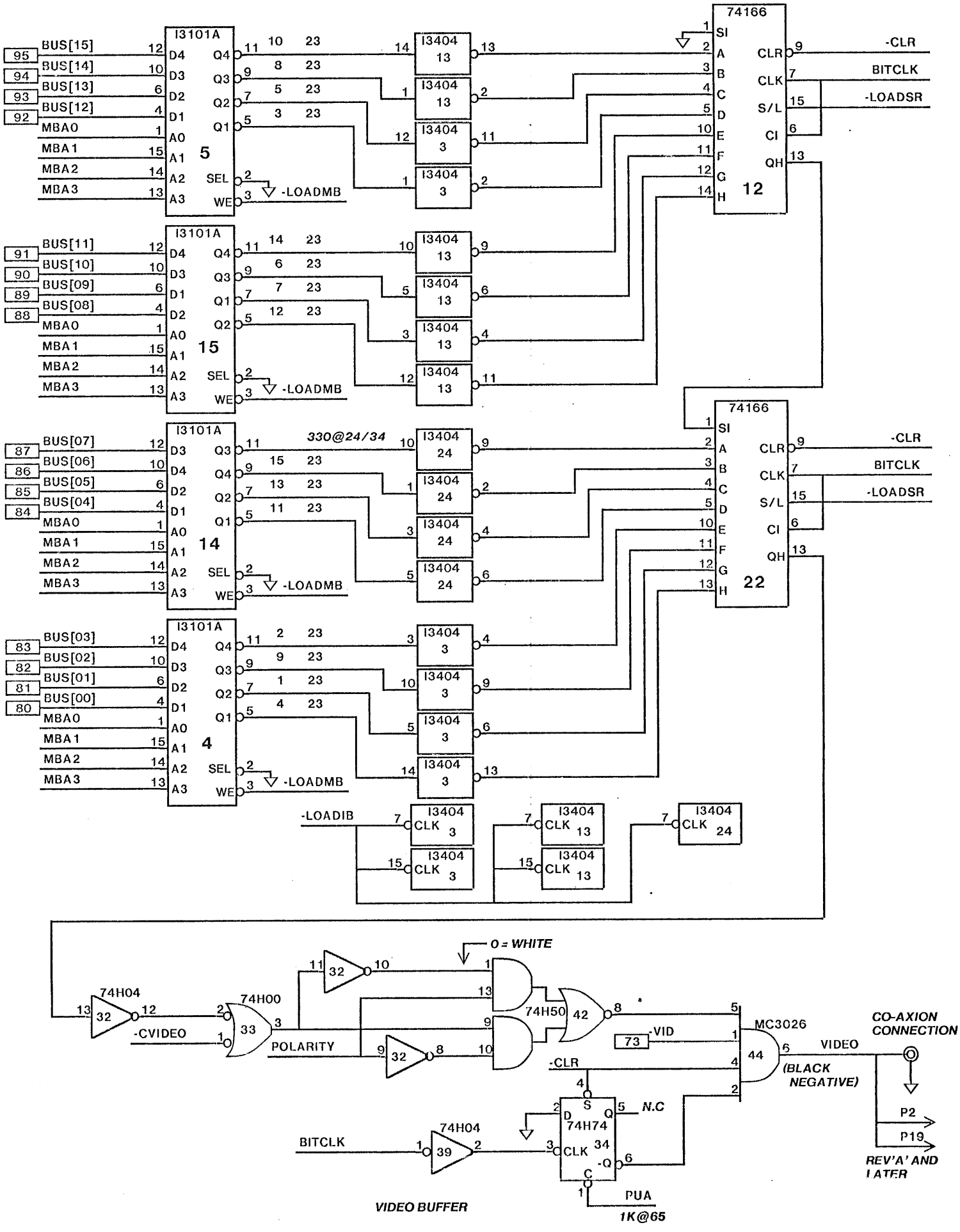


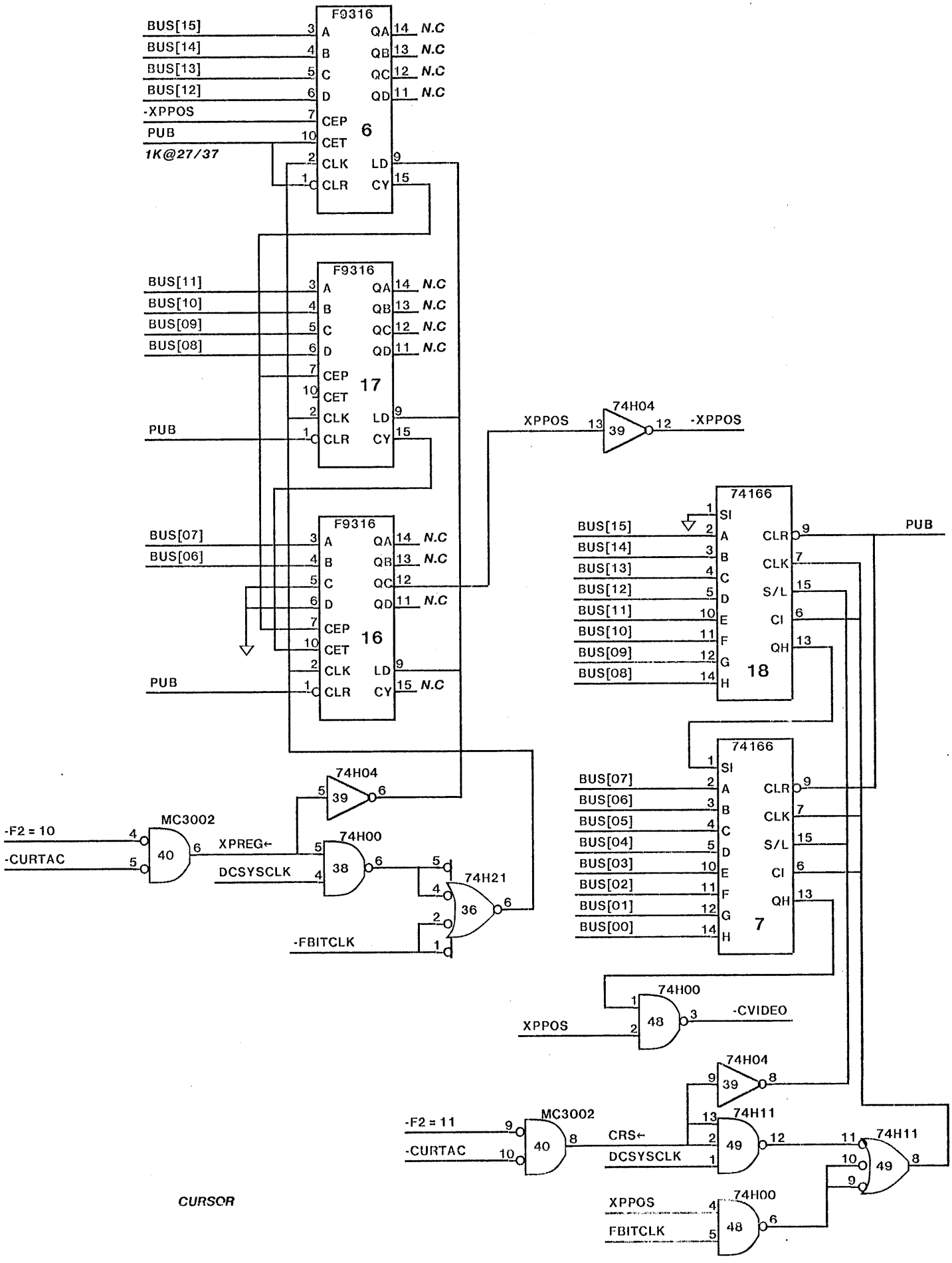


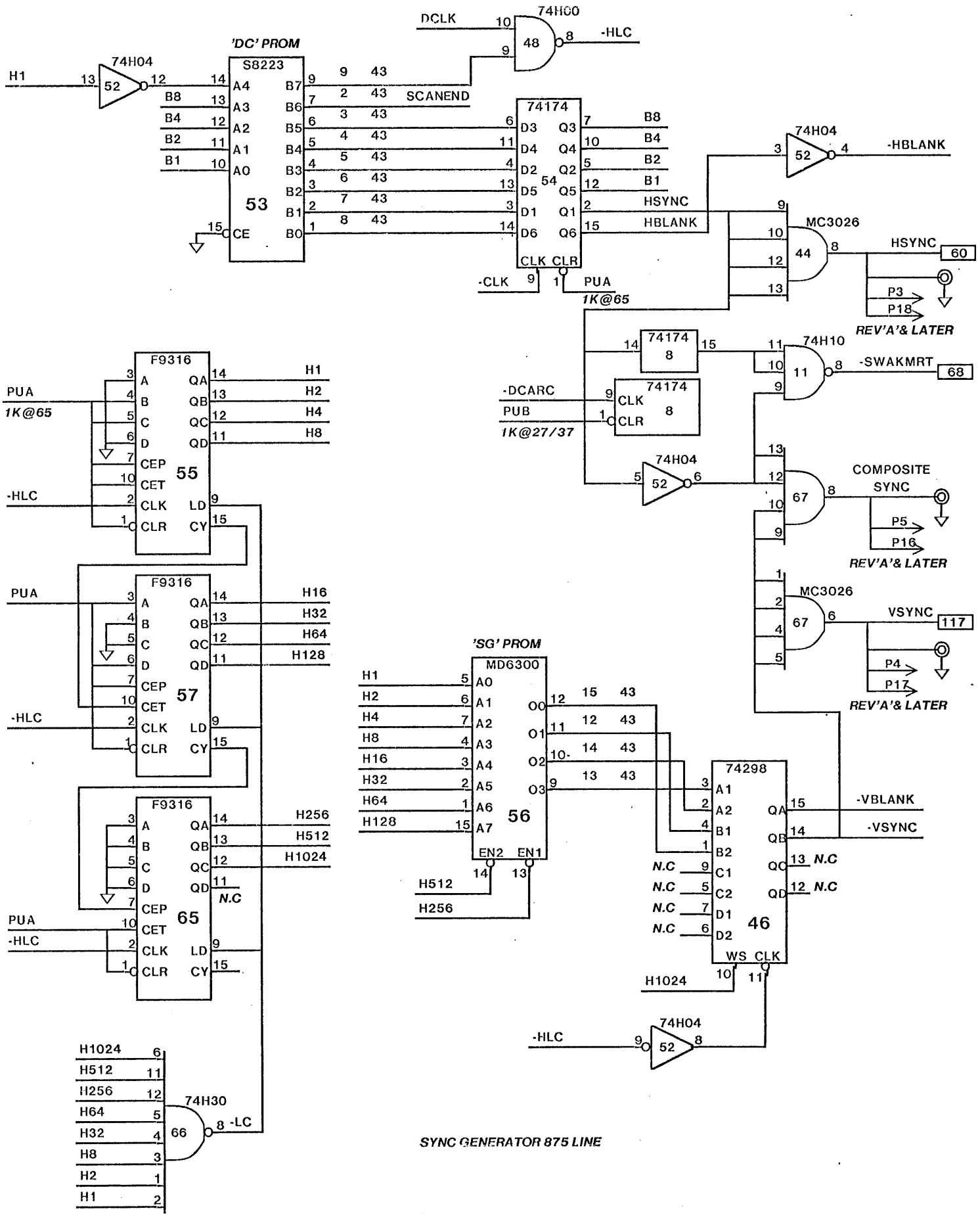
BUFFER CONTROL

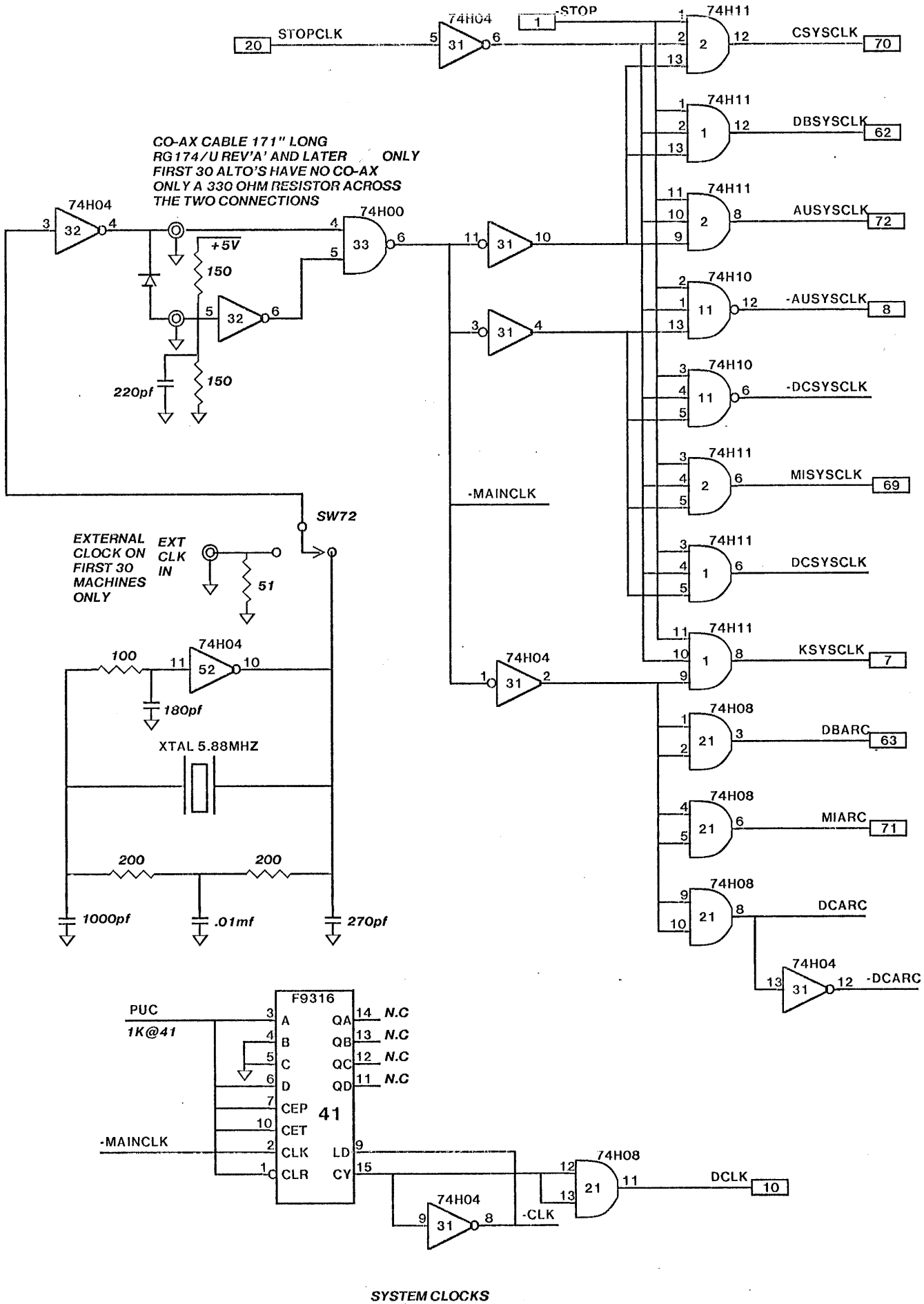


VIDEO BIT CLOCK

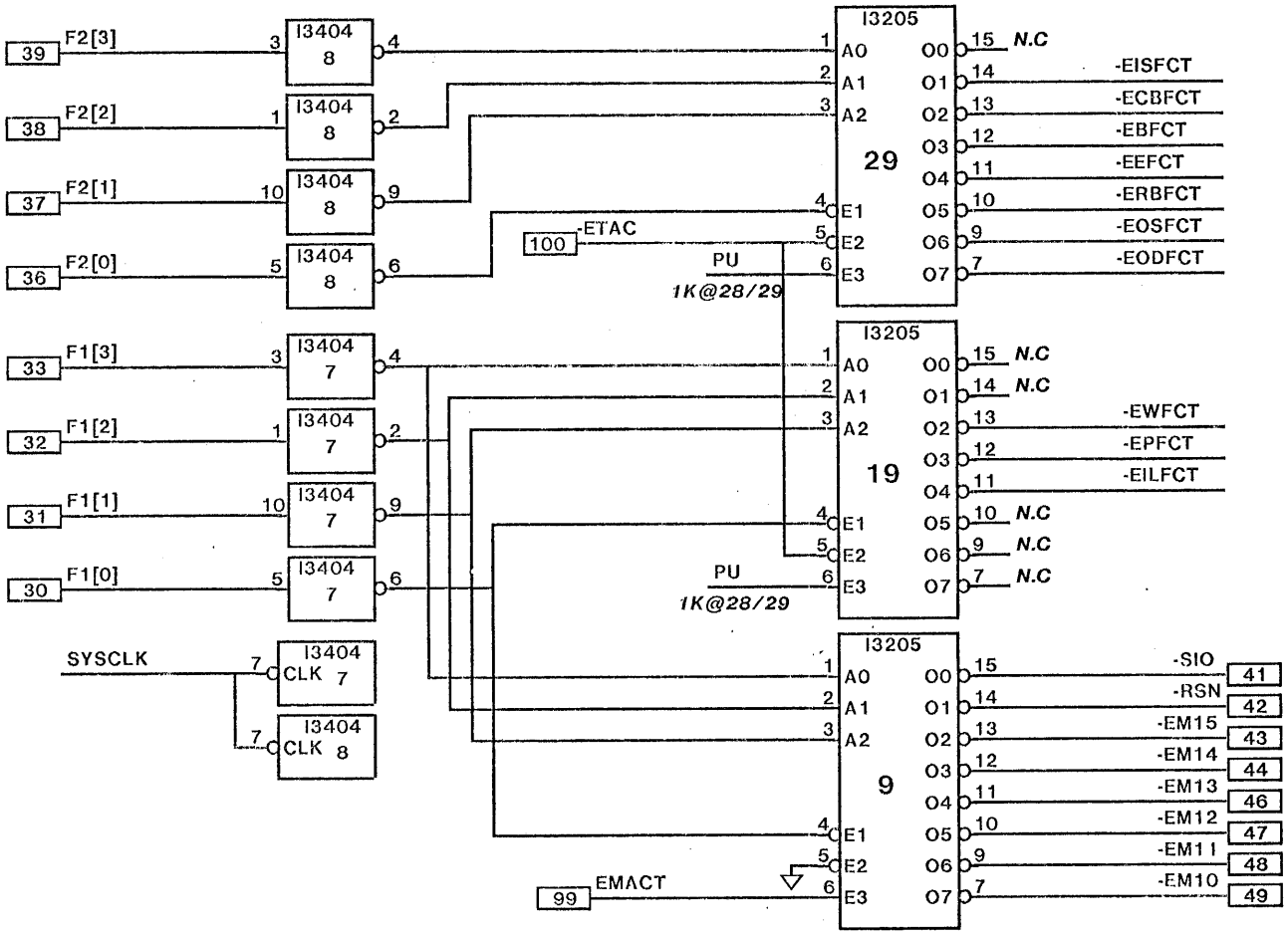

I3101A
5
BUS[15]
BUS[14]
BUS[13]
BUS[12]
MBA0
MBA1
MBA2
MBA3
D4
D3
D2
D1
A0
A1
A2
A3
Q4
Q3
Q2
Q1
SEL
WE
-LOADMB
I3404
13
3
74166
12
SI
A
B
C
D
E
F
G
H
CLR
CLK
S/L
CI
QH
-CLR
BITCLK
-LOADSR
I3101A
15
BUS[11]
BUS[10]
BUS[09]
BUS[08]
I3101A
14
BUS[07]
BUS[06]
BUS[05]
BUS[04]
330@24/34
I3404
24
74166
22
I3101A
4
BUS[03]
BUS[02]
BUS[01]
BUS[00]
-LOADIB
I3404
CLK
3
13
24
0 = WHITE
74H04
74H00
74H50
42
-CVIDEO
POLARITY
-VID
73
MC3026
44
-CLR
VIDEO
(BLACK
NEGATIVE)
CO-AXION
CONNECTION
P2
P19
REV'A' AND
LATER
N.C
74H74
BITCLK
PUA
1K@65
VIDEO BUFFER

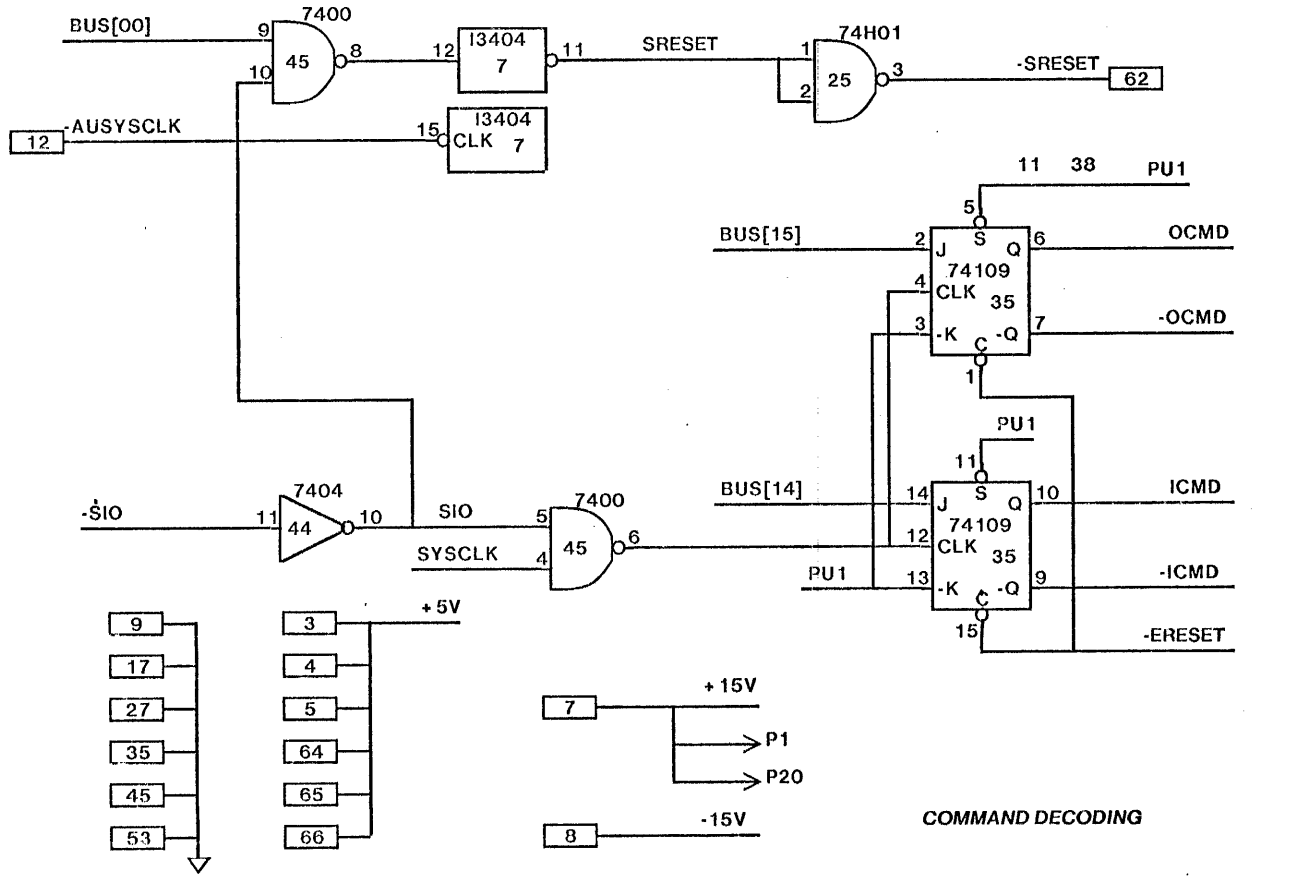

F9316
6
BUS[15]
BUS[14]
BUS[13]
BUS[12]
-XPPOS
PUB
1K@27/37
N.C
F9316
17
BUS[11]
BUS[10]
BUS[09]
BUS[08]
PUB
F9316
16
BUS[07]
BUS[06]
PUB
74H04
39
XPPOS
-XPPOS
74166
18
BUS[15]
BUS[14]
BUS[13]
BUS[12]
BUS[11]
BUS[10]
BUS[09]
BUS[08]
PUB
74166
7
BUS[07]
BUS[06]
BUS[05]
BUS[04]
BUS[03]
BUS[02]
BUS[01]
BUS[00]
MC3002
40
-F2 = 10
-CURTAC
XPREG←
74H00
38
DCSYSCLK
74H21
36
-FBITCLK
74H00
48
XPPOS
-CVIDEO
74H04
39
MC3002
40
-F2 = 11
-CURTAC
CRS←
74H11
49
DCSYSCLK
74H11
49
74H00
48
XPPOS
FBITCLK
CURSOR

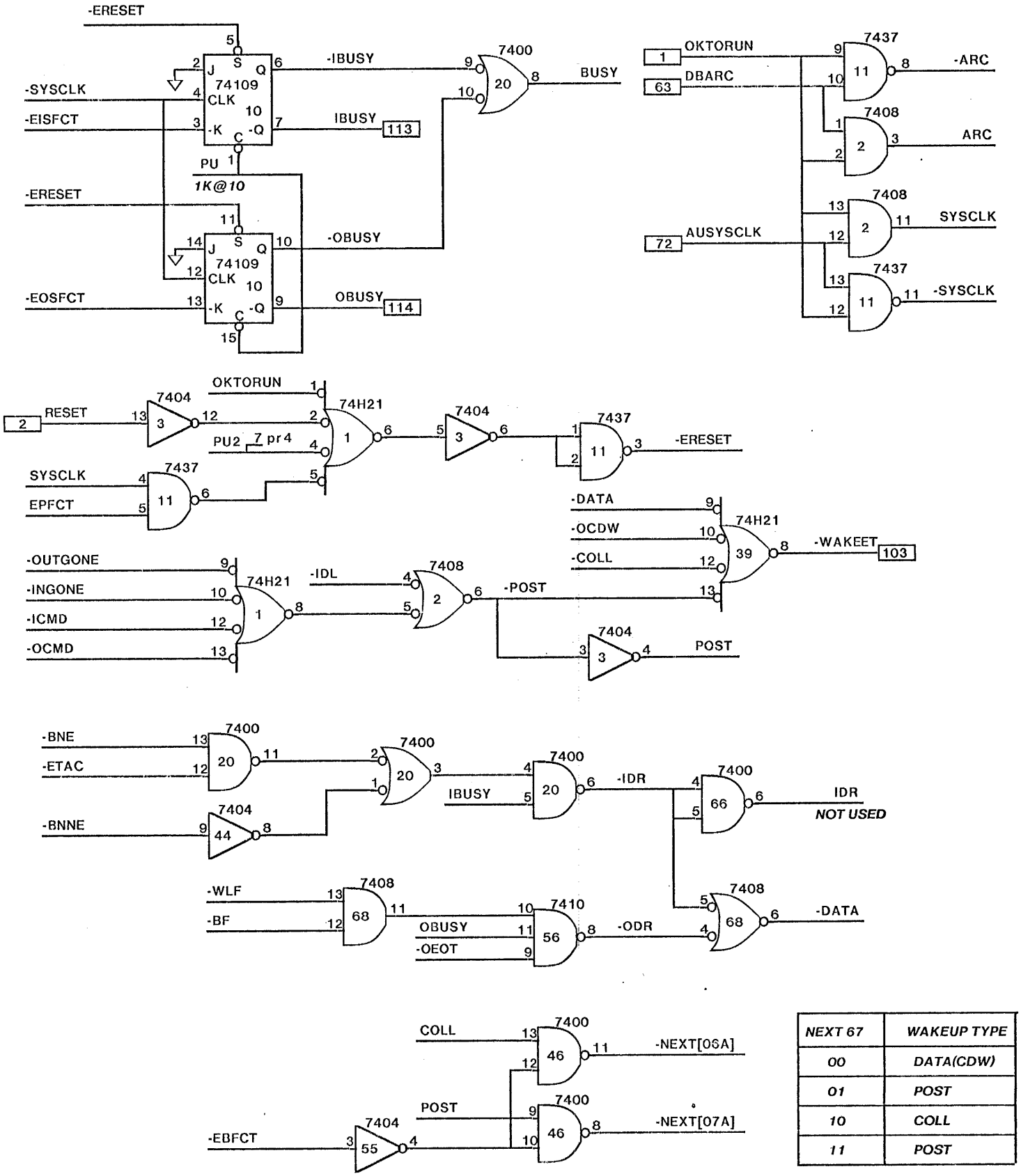

'DC' PROM
S8223
53
74H04
74H00
DCLK
-HLC
SCANEND
74174
54
HSYNC
HBLANK
-CLK
PUA
1K@65
74H04
-HBLANK
MC3026
44
HSYNC
60
P3
P18
REV'A'& LATER
74174
8
74H10
11
-SWAKMRT
68
-DCARC
PUB
1K@27/37
74174
8
74H04
COMPOSITE
SYNC
67
P5
P16
REV'A'& LATER
MC3026
67
VSYNC
117
P4
P17
REV'A'& LATER
F9316
55
F9316
57
F9316
65
PUA
1K@65
-HLC
H1
H2
H4
H8
H16
H32
H64
H128
H256
H512
H1024
N.C
'SG' PROM
MD6300
56
74298
46
-VBLANK
-VSYNC
74H30
66
-LC
74H04
SYNC GENERATOR 875 LINE



SYSTEM CLOCKS

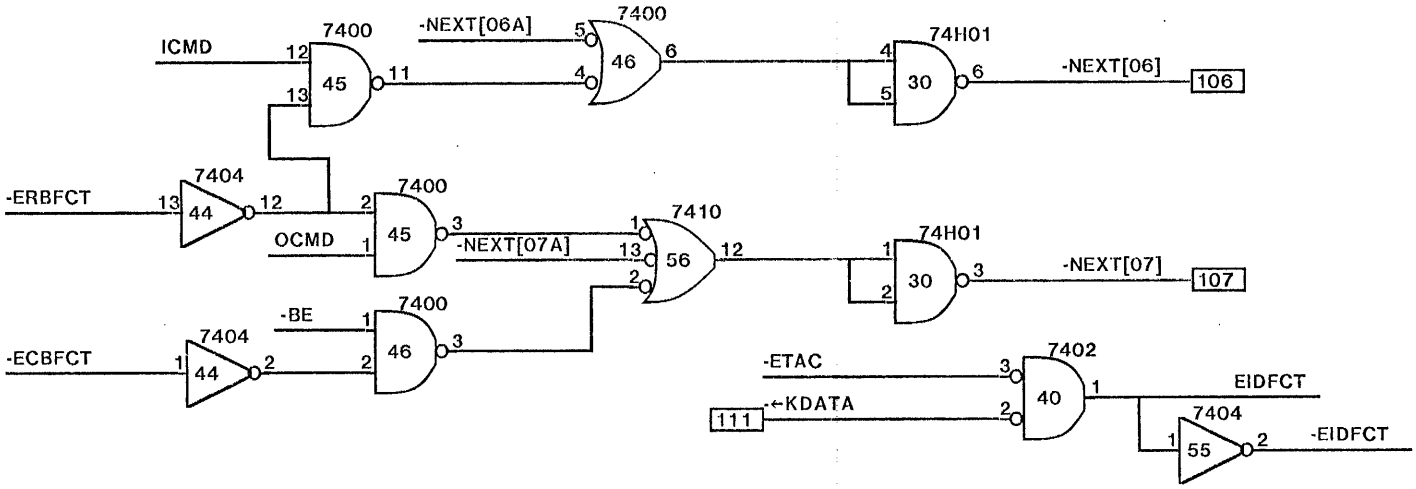

F2[3]
F2[2]
F2[1]
F2[0]
F1[3]
F1[2]
F1[1]
F1[0]
I3404
I3205
29
19
9
-ETAC
PU
1K@28/29
N.C
-EISFCT
-ECBFCT
-EBFCT
-EEFCT
-ERBFCT
-EOSFCT
-EODFCT
-EWFCT
-EPFCT
-EILFCT
SYSCLK
-SIO
-RSN
-EM15
-EM14
-EM13
-EM12
-EM11
-EM10
EMACT

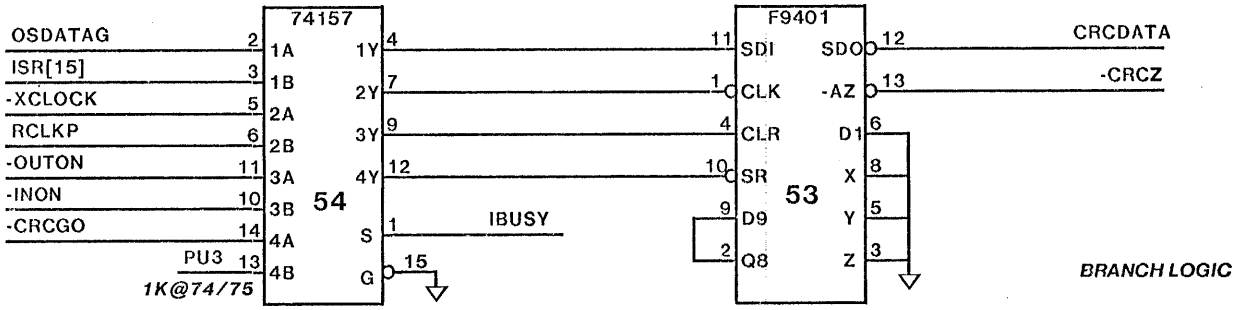

BUS[00]
-AUSYSCLK
SRESET
-SRESET
7400
74H01
I3404
BUS[15]
BUS[14]
OCMD
-OCMD
ICMD
-ICMD
-ERESET
PU1
74109
-SIO
SIO
SYSCLK
7404
+5V
+15V
-15V
P1
P20
COMMAND DECODING



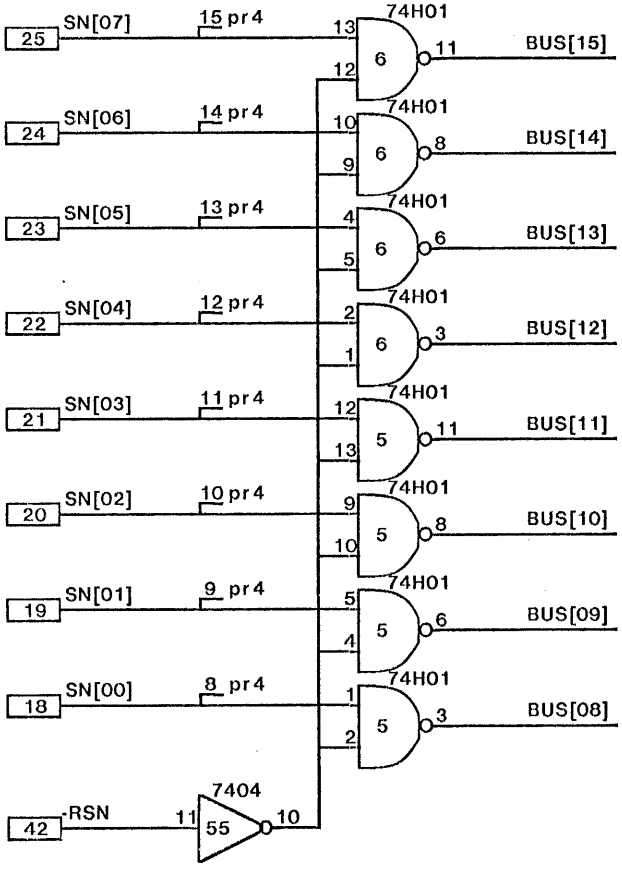
NEXT 67	WAKEUP TYPE
00	DATA(CDW)
01	POST
10	COLL
11	POST

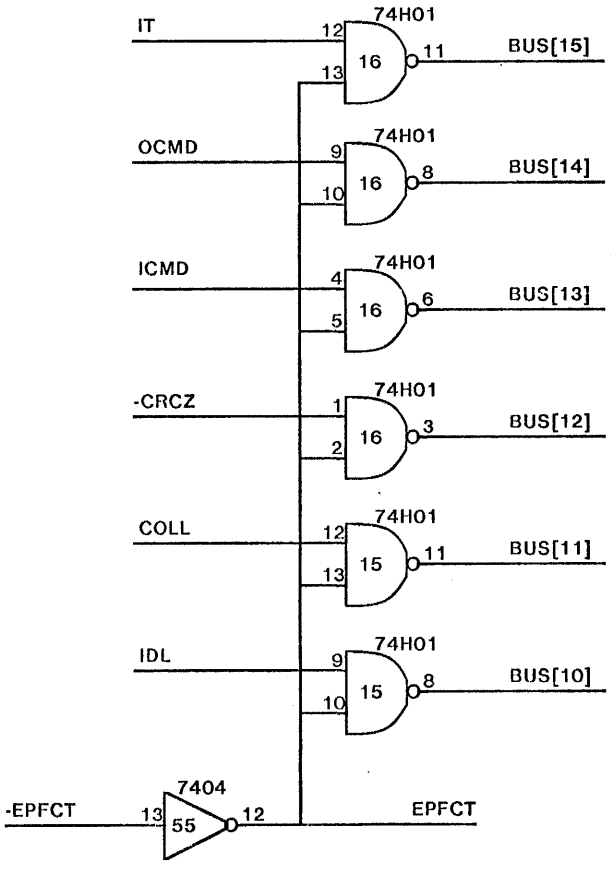
ALTO INTERFACE



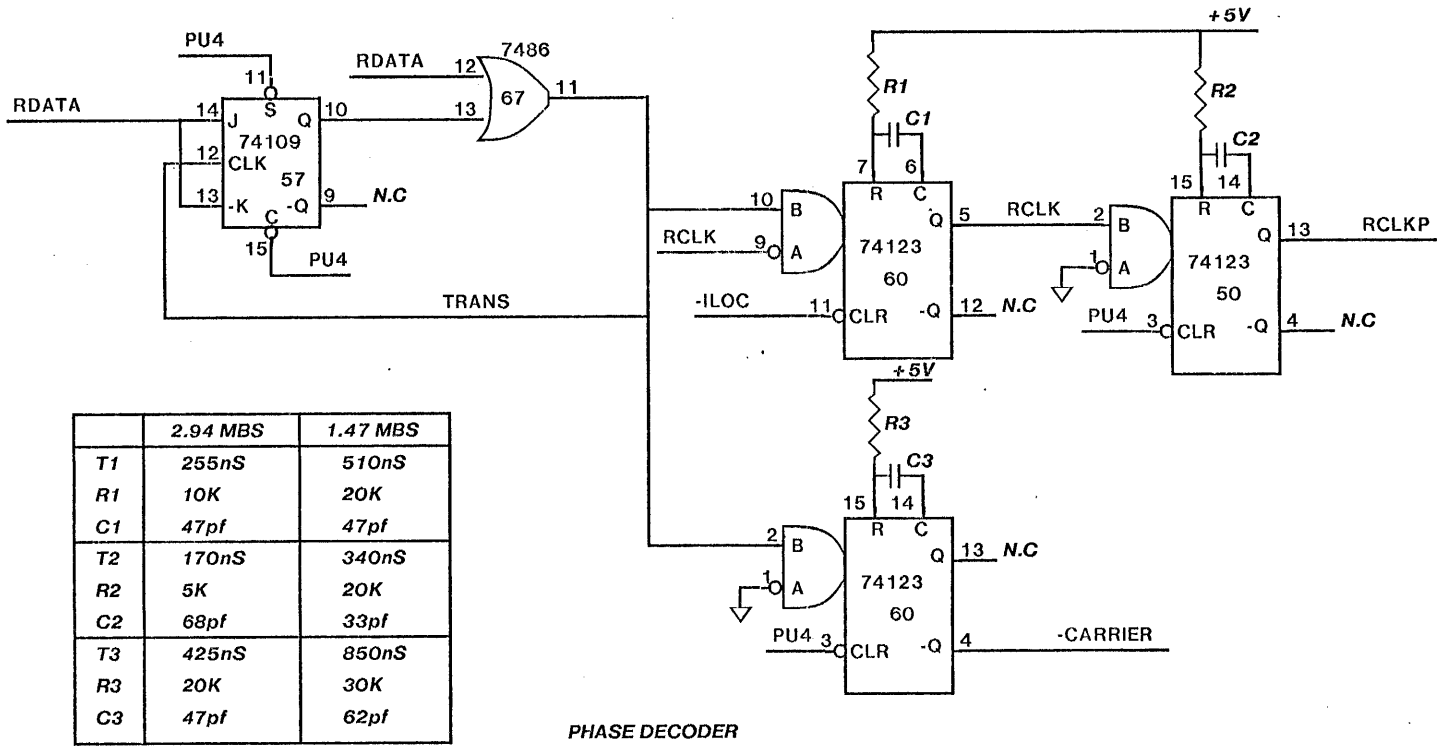


BRANCH LOGIC



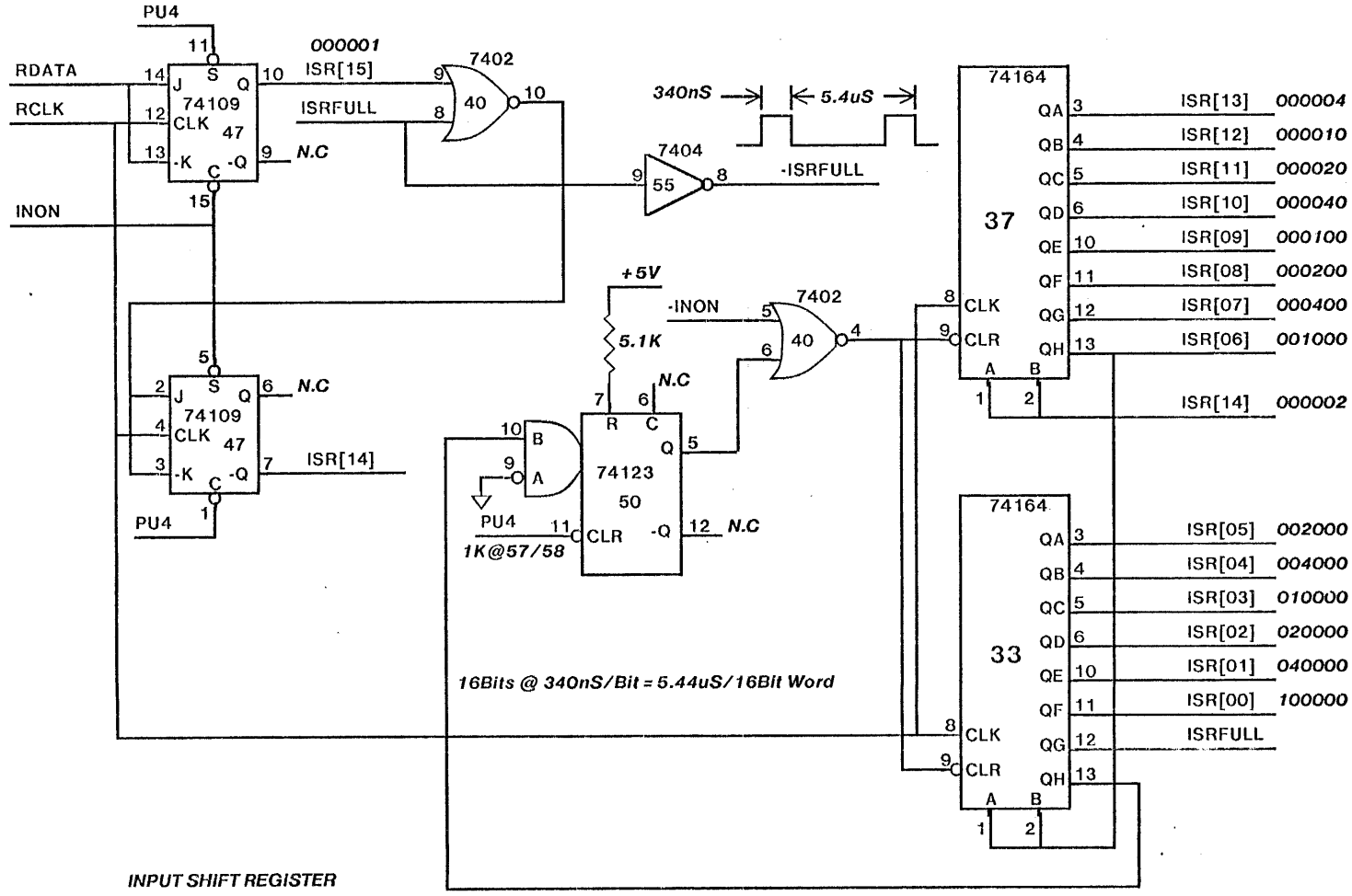


SERIAL NUMBER & STATUS

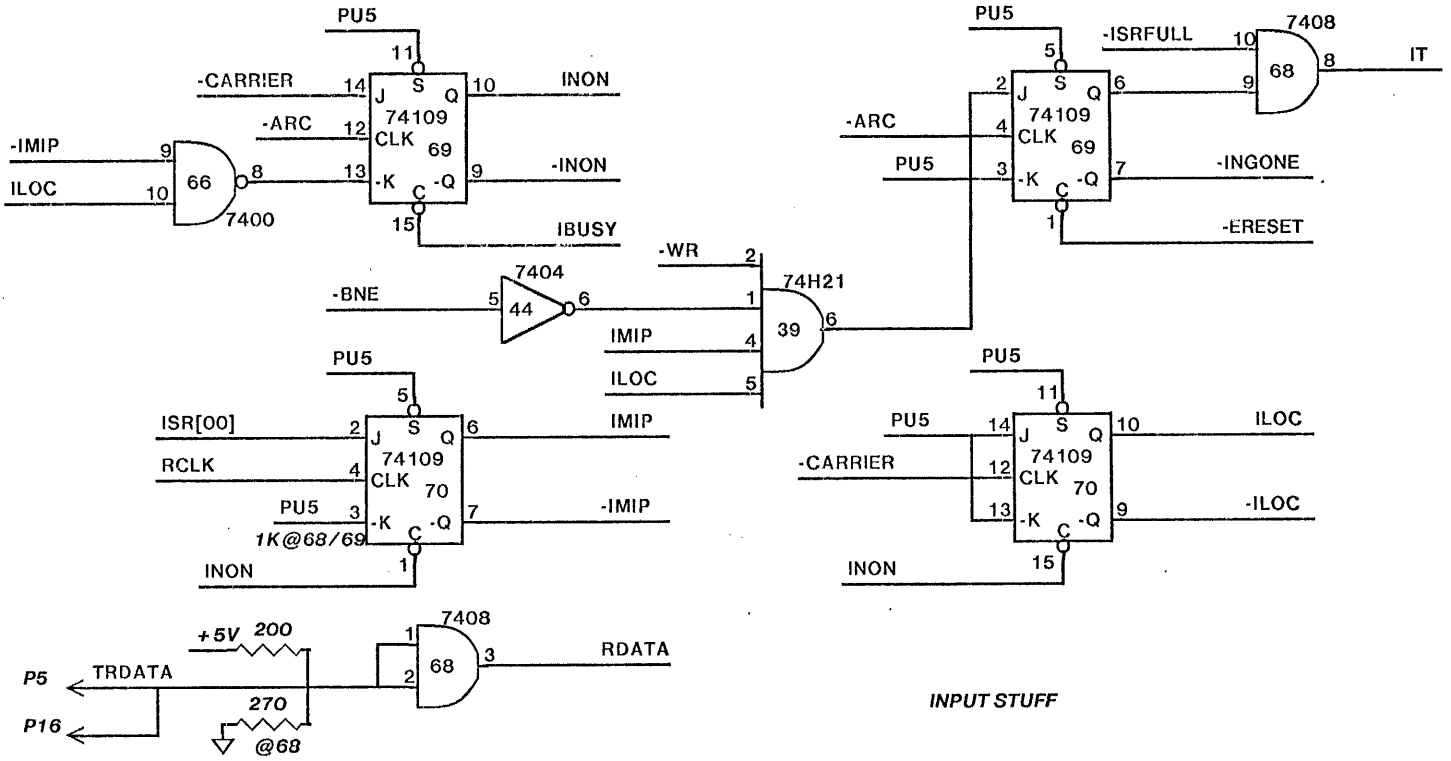


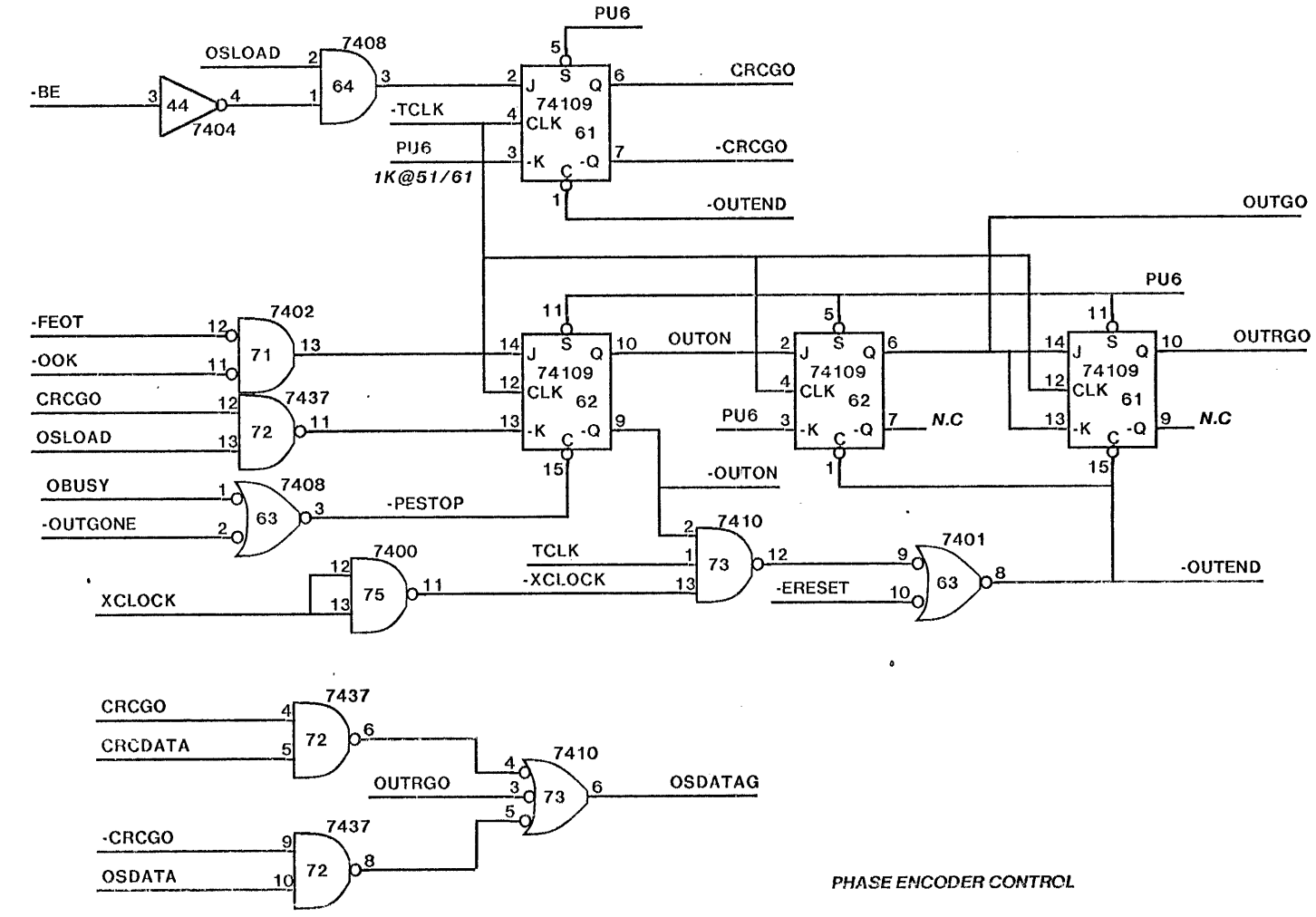
	2.94 MBS	1.47 MBS
T1	255nS	510nS
R1	10K	20K
C1	47pf	47pf
T2	170nS	340nS
R2	5K	20K
C2	68pf	33pf
T3	425nS	850nS
R3	20K	30K
C3	47pf	62pf

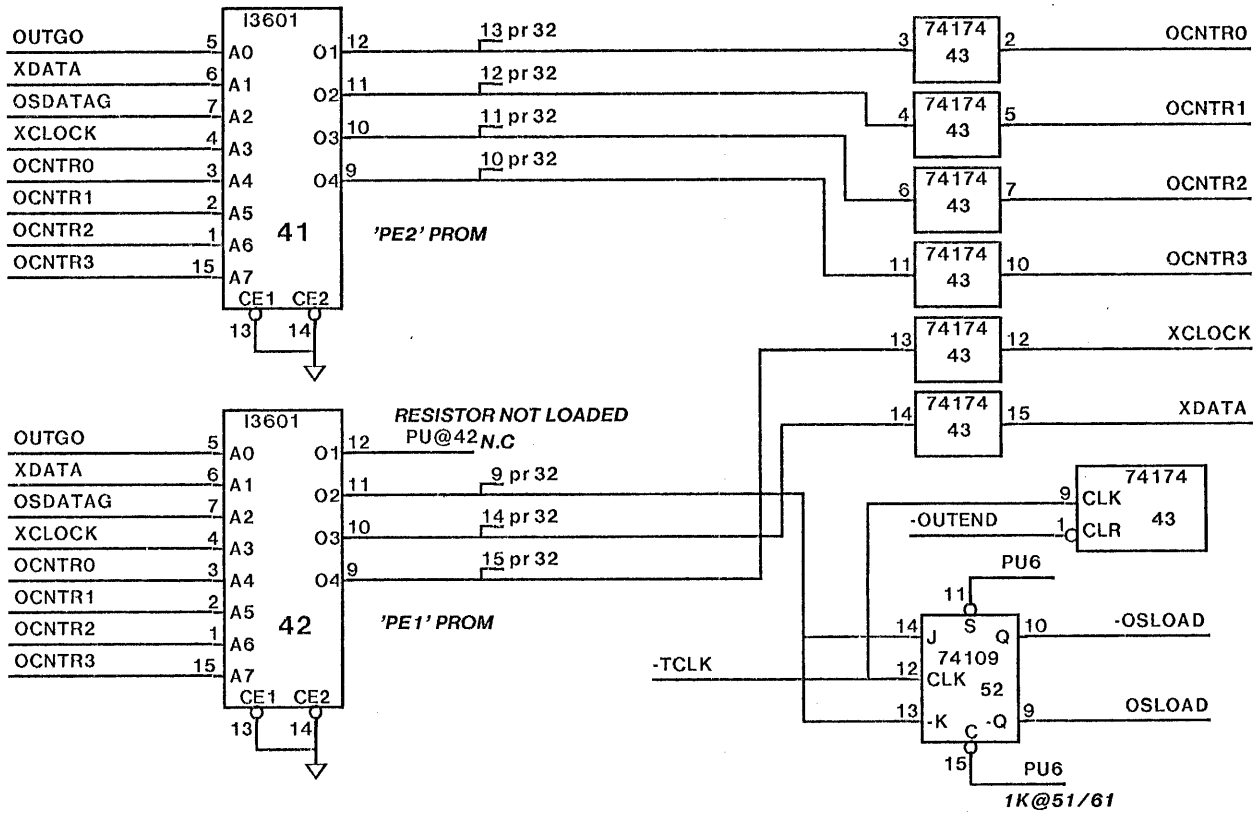
PHASE DECODER

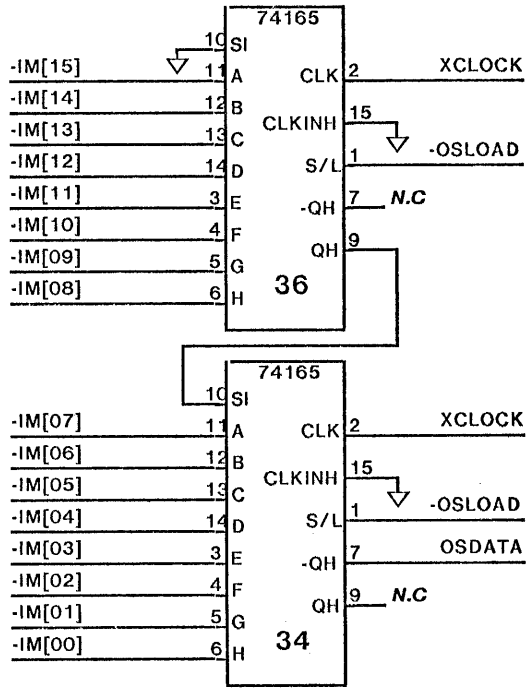


INPUT SHIFT REGISTER

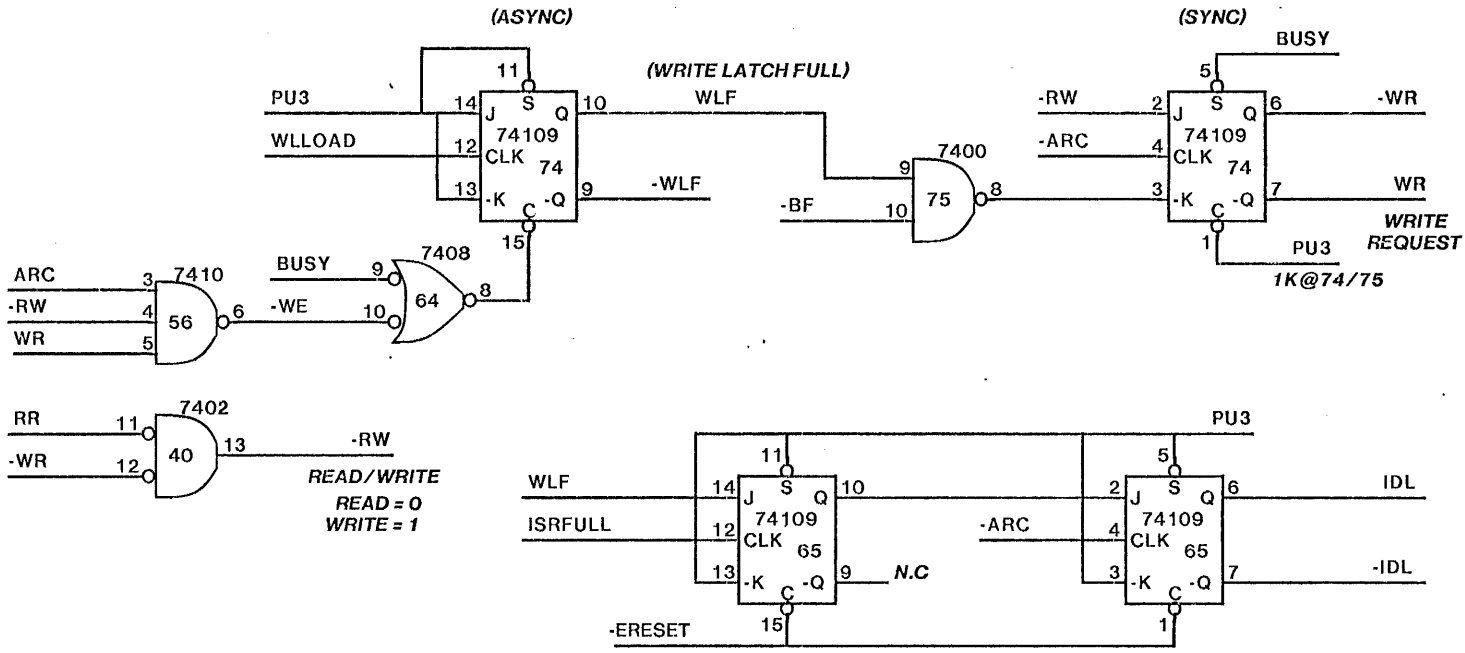

PU5
-CARRIER
-ARC
-IMIP
ILOC
66
7400
74109
CLK 69
INON
-INON
IBUSY
-WR
-BNE
7404
44
74H21
39
IMIP
ILOC
PU5
ISR[00]
RCLK
PU5
1K@68/69
INON
74109
CLK 70
IMIP
-IMIP
PU5
-ISRFULL
7408
68
IT
-ARC
PU5
74109
CLK 69
-INGONE
-ERESET
PU5
PU5
-CARRIER
74109
CLK 70
ILOC
-ILOC
INON
+5V 200
P5
TRDATA
P16
270
@68
7408
68
RDATA
INPUT STUFF

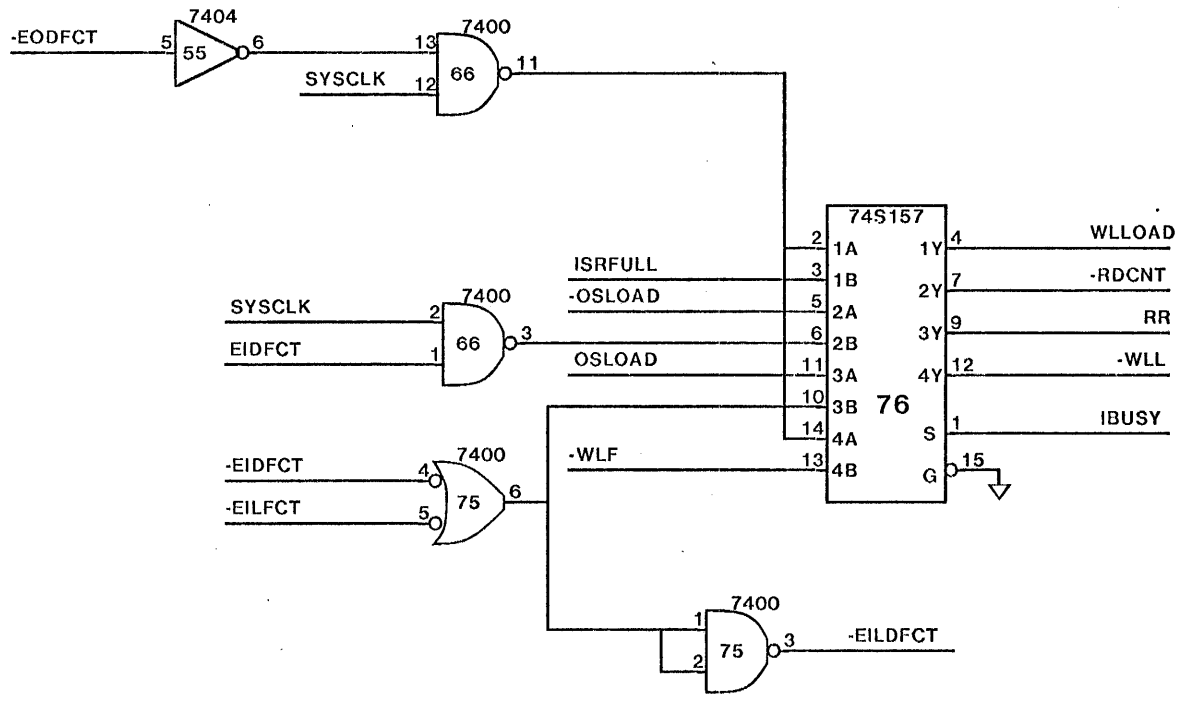

PU6
OSLOAD
7408
64
-BE
44
7404
-TCLK
PU6
1K@51/61
74109
CLK 61
CRCGO
-CRCGO
-OUTEND
OUTGO
PU6
-FEOT
-OOK
CRCGO
OSLOAD
7402
71
7437
72
74109
CLK 62
OUTON
PU6
N.C
74109
CLK 61
OUTRGO
N.C
OBUSY
-OUTGONE
7408
63
-PESTOP
-OUTON
7410
73
TCLK
-XCLOCK
7400
75
XCLOCK
7401
63
-ERESET
-OUTEND
CRCGO
CRCDATA
7437
72
OUTRGO
7410
73
OSDATAG
-CRCGO
OSDATA
7437
72
PHASE ENCODER CONTROL



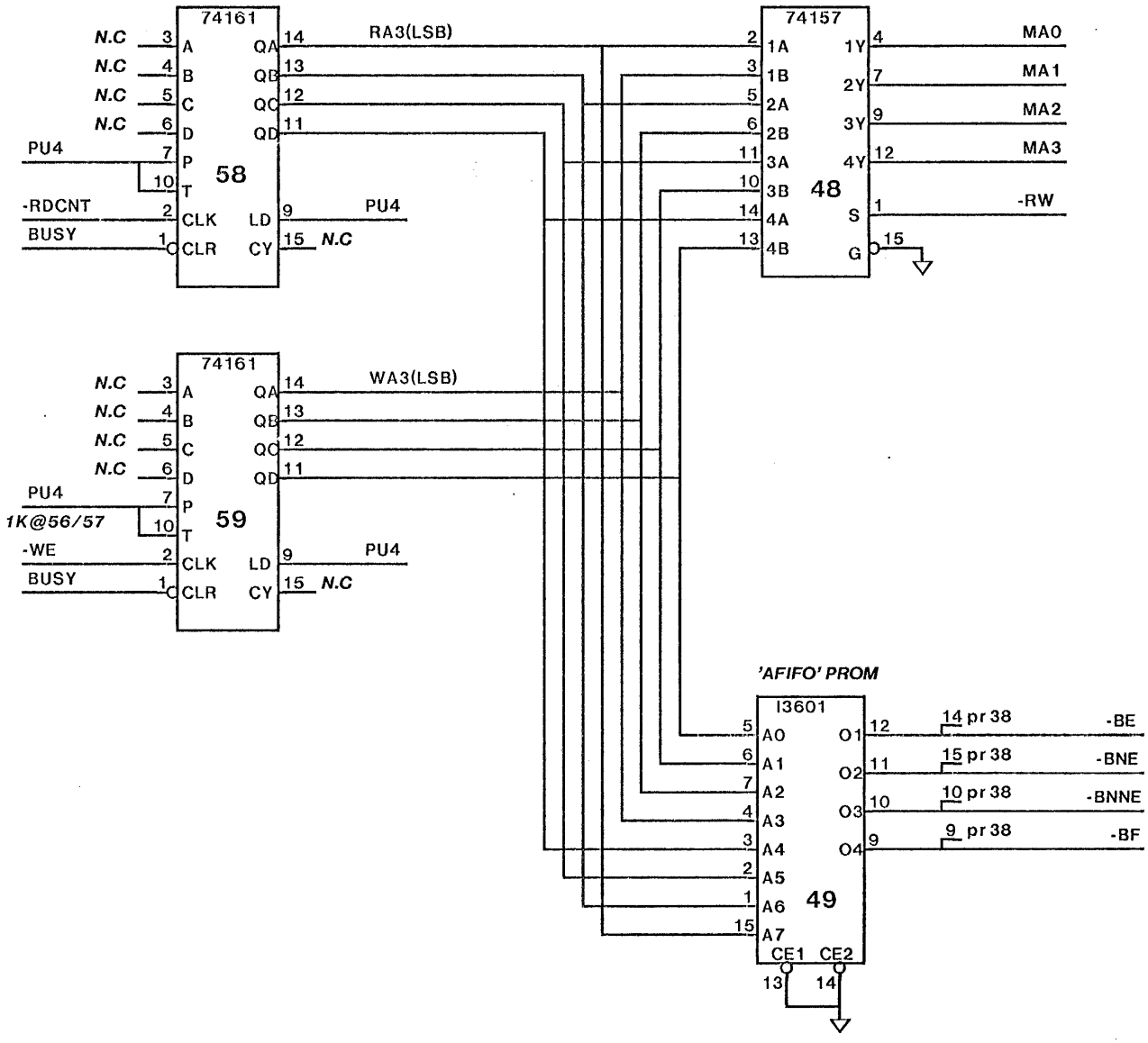


OUTPUT SHIFT REGISTER & ENCODER

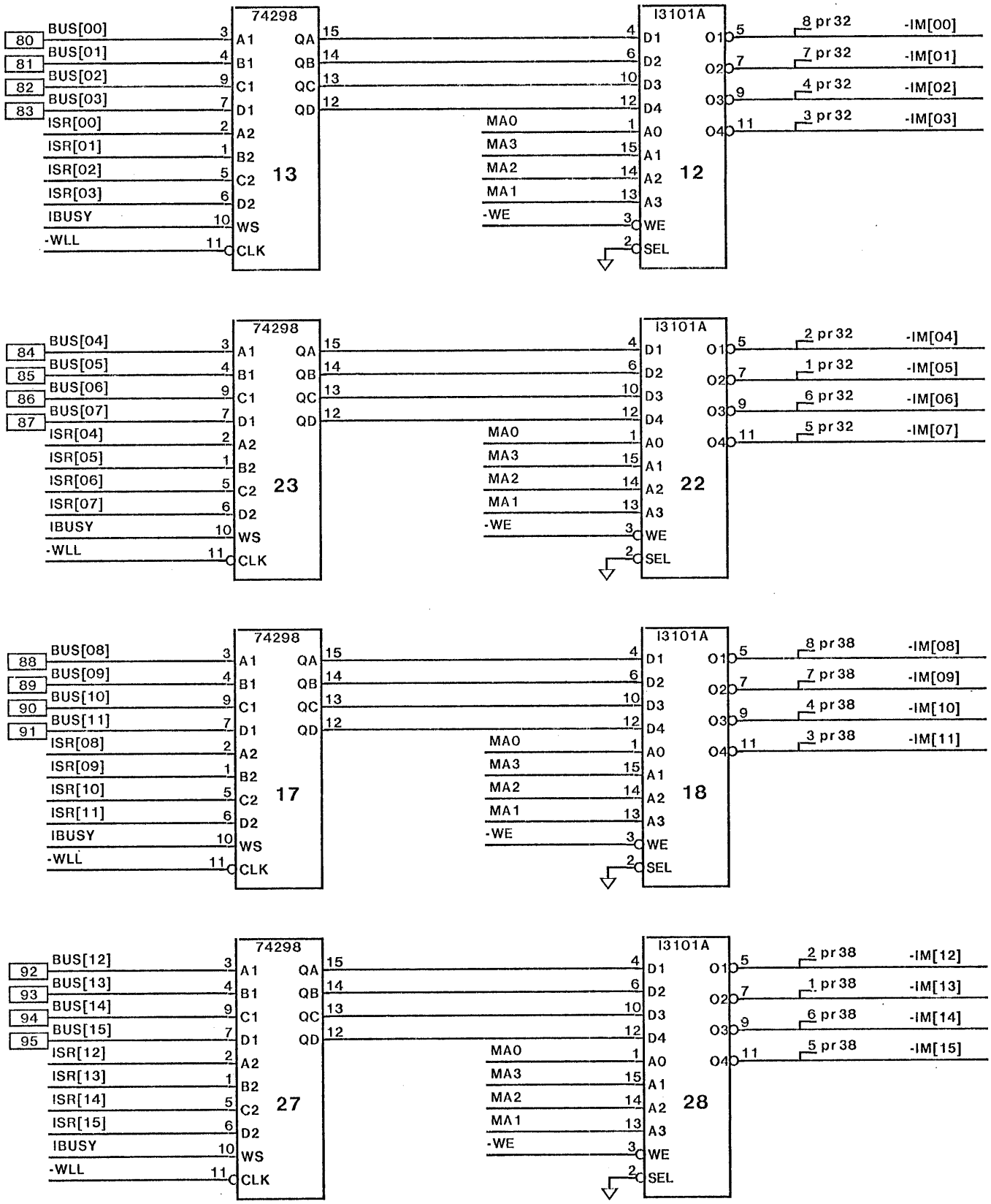




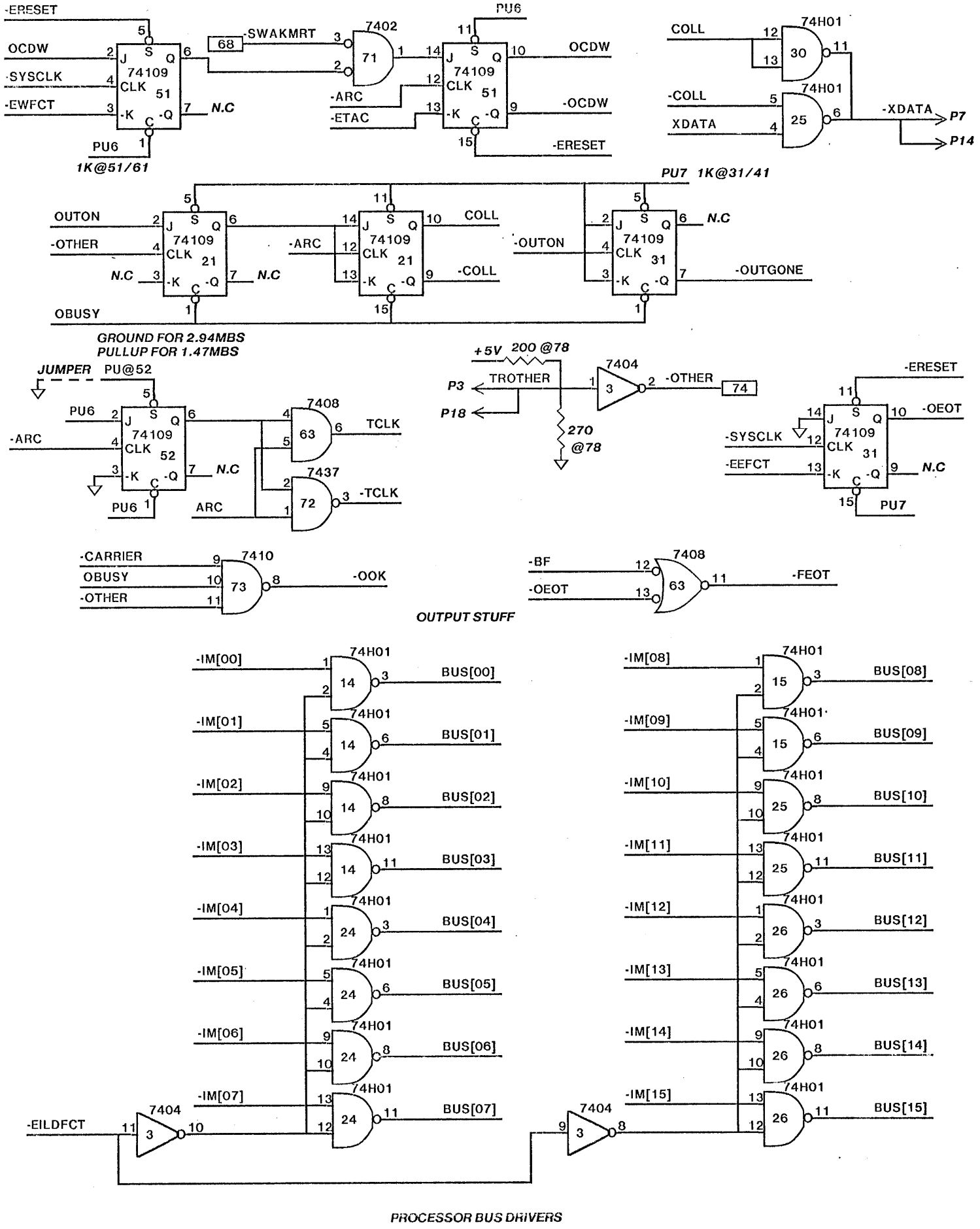
BUFFER CONTROL

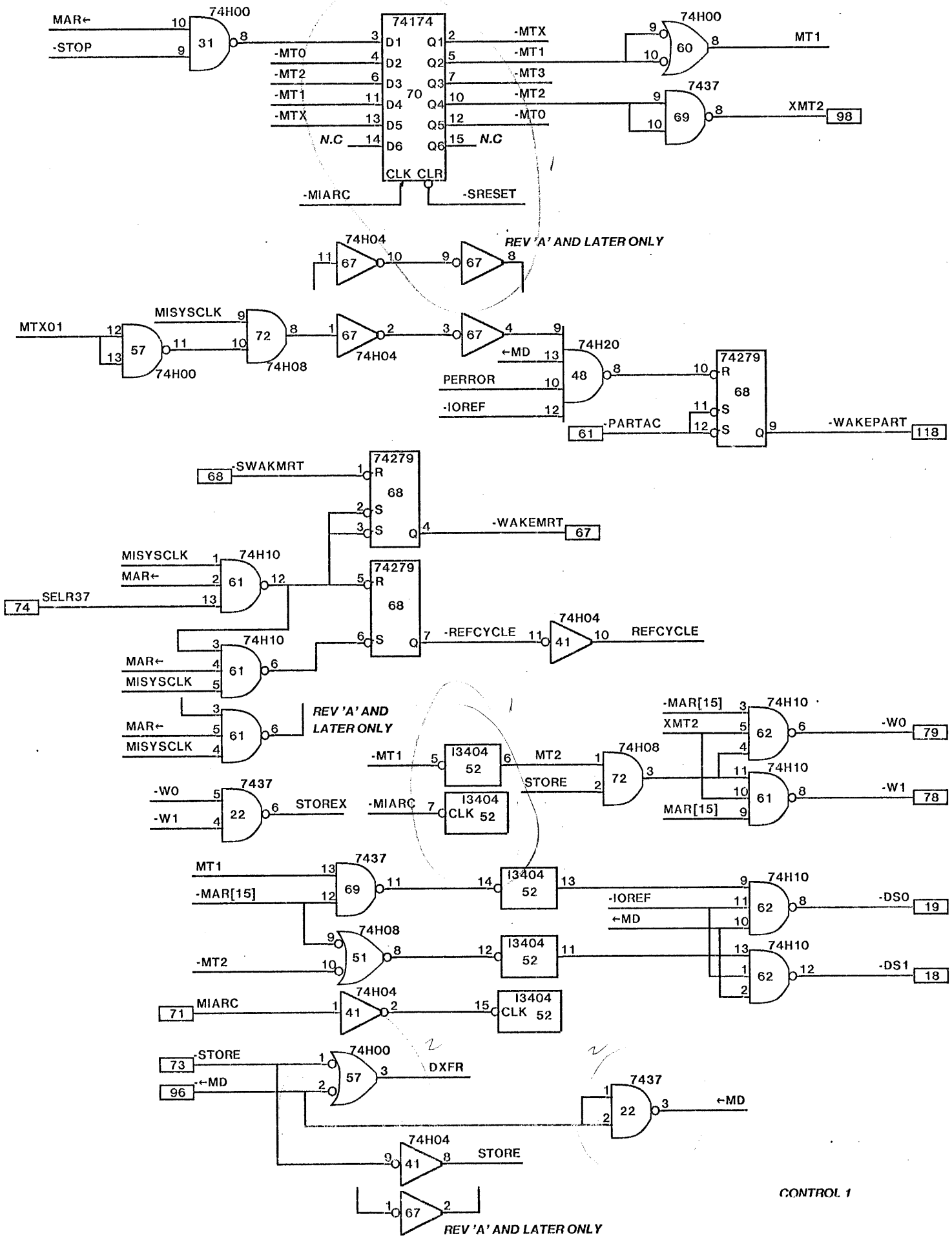


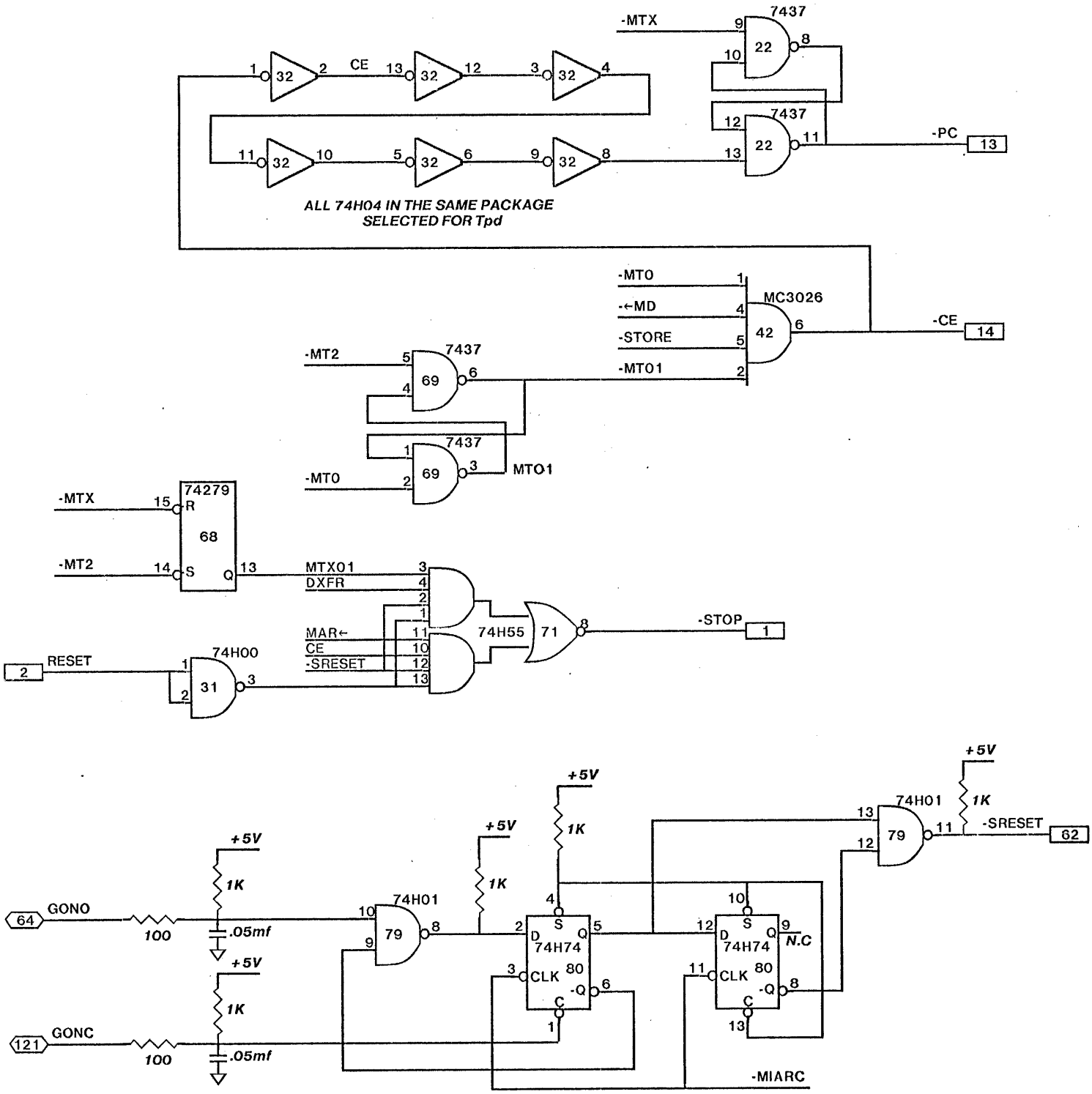
HALF DUPLEX BUFFER



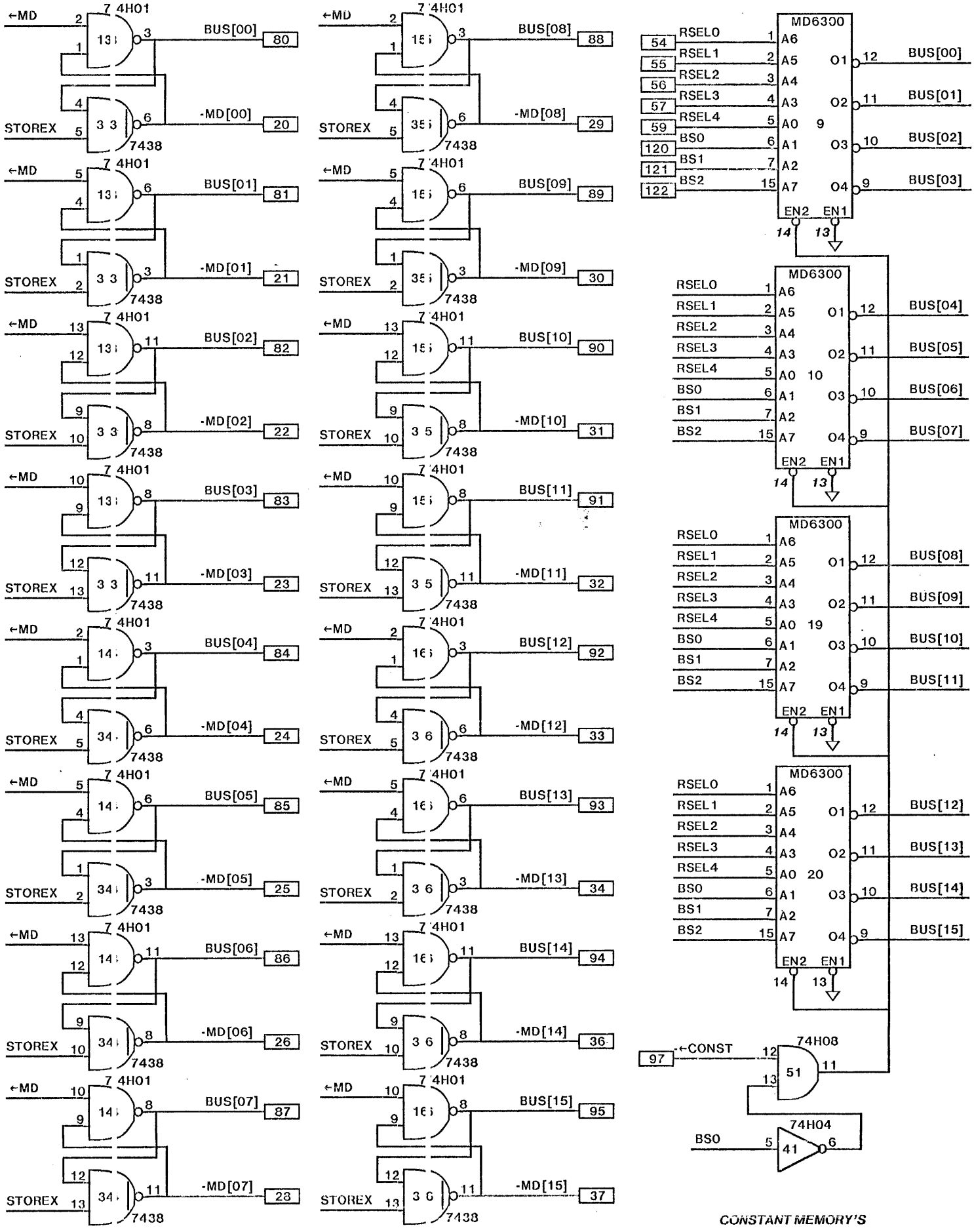
HALF DUPLEX BUFFER

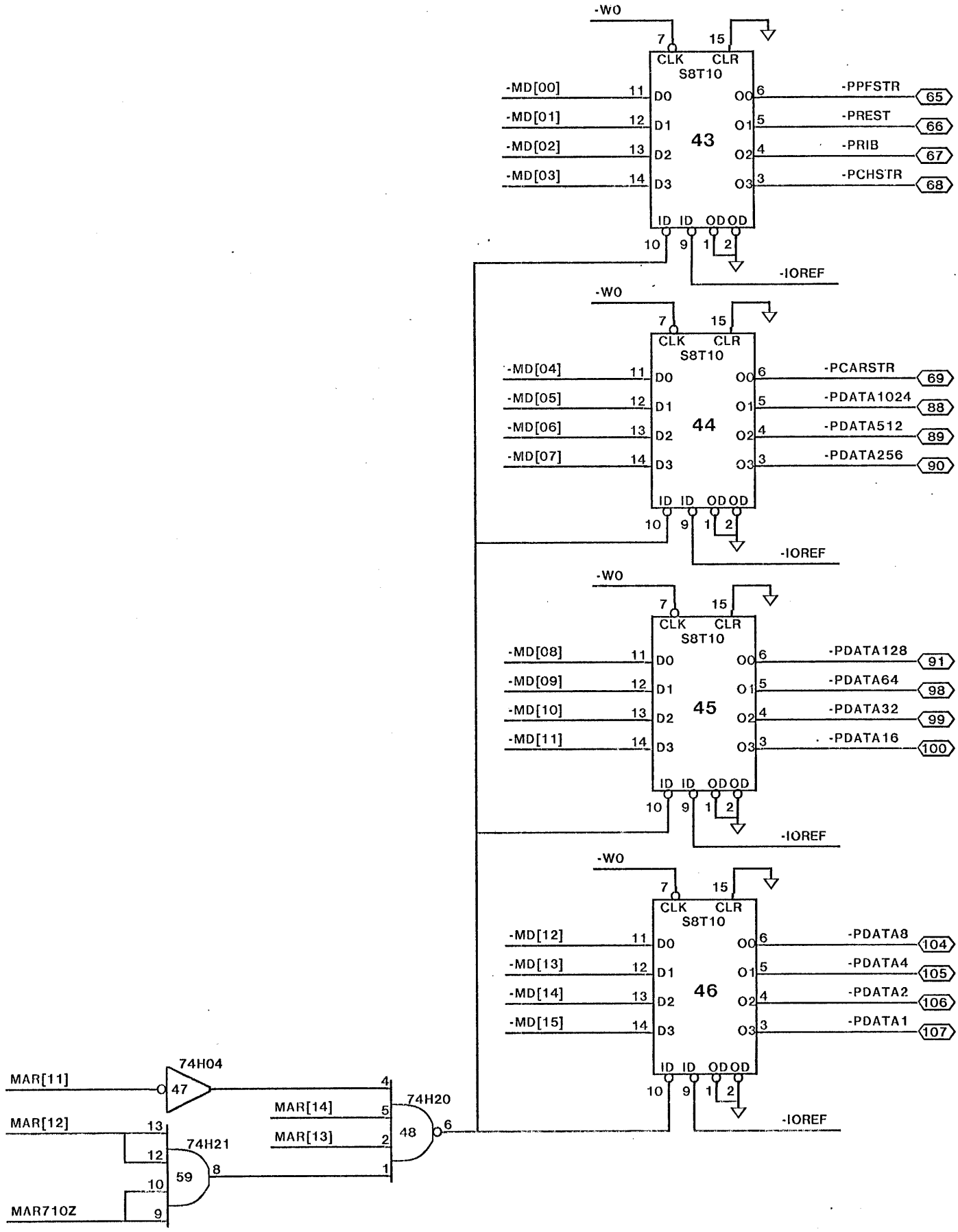

-ERESET
OCDW
-SYSCLK
-EWFCT
74109
CLK 51
-K -Q
N.C
PU6
1K@51/61
68
-SWAKMRT
7402
71
-ARC
-ETAC
PU6
OCDW
-OCDW
-ERESET
COLL
-COLL
XDATA
74H01
30
25
-XDATA
P7
P14
PU7 1K@31/41
OUTON
-OTHER
CLK 21
-ARC
COLL
-COLL
-OUTON
CLK 31
-OUTGONE
OBUSY
GROUND FOR 2.94MBS
PULLUP FOR 1.47MBS
JUMPER PU@52
CLK 52
7408
63
TCLK
7437
72
-TCLK
+5V 200 @78
P3
P18
TROTHER
7404
-OTHER
74
270
@78
-SYSCLK
-EEFCT
CLK 31
-OEOT
-CARRIER
OBUSY
-OTHER
7410
73
-OOK
-BF
-OEOT
-FEOT
OUTPUT STUFF
-IM[00]
-IM[01]
-IM[02]
-IM[03]
-IM[04]
-IM[05]
-IM[06]
-IM[07]
BUS[00]
BUS[01]
BUS[02]
BUS[03]
BUS[04]
BUS[05]
BUS[06]
BUS[07]
-EILDFCT
-IM[08]
-IM[09]
-IM[10]
-IM[11]
-IM[12]
-IM[13]
-IM[14]
-IM[15]
BUS[08]
BUS[09]
BUS[10]
BUS[11]
BUS[12]
BUS[13]
BUS[14]
BUS[15]
PROCESSOR BUS DRIVERS


MAR←
-STOP
74H00
31
74174
D1 Q1
D2 Q2
D3 Q3
D4 Q4
D5 Q5
D6 Q6
CLK CLR
70
-MT0
-MT2
-MT1
-MTX
N.C
N.C
-MTX
-MT1
-MT3
-MT2
-MT0
-MIARC
-SRESET
74H00
60
MT1
7437
69
XMT2
98
74H04
67
67
REV 'A' AND LATER ONLY
MTX01
MISYSCLK
57
72
74H00
74H08
74H04
←MD
PERROR
-IOREF
74H20
48
74279
68
-PARTAC
61
-WAKEPART
118
68
-SWAKMRT
-WAKEMRT
67
MISYSCLK
MAR←
SELR37
74
74H10
61
-REFCYCLE
41
REFCYCLE
REV 'A' AND LATER ONLY
-MAR[15]
XMT2
MAR[15]
62
-W0
79
-W1
78
-MT1
-MIARC
I3404
52
CLK 52
MT2
STORE
-W0
-W1
7437
22
STOREX
MT1
-MAR[15]
-MT2
74H08
51
-IOREF
←MD
-DS0
19
-DS1
18
MIARC
71
-STORE
73
←MD
96
DXFR
STORE
CONTROL 1
REV 'A' AND LATER ONLY

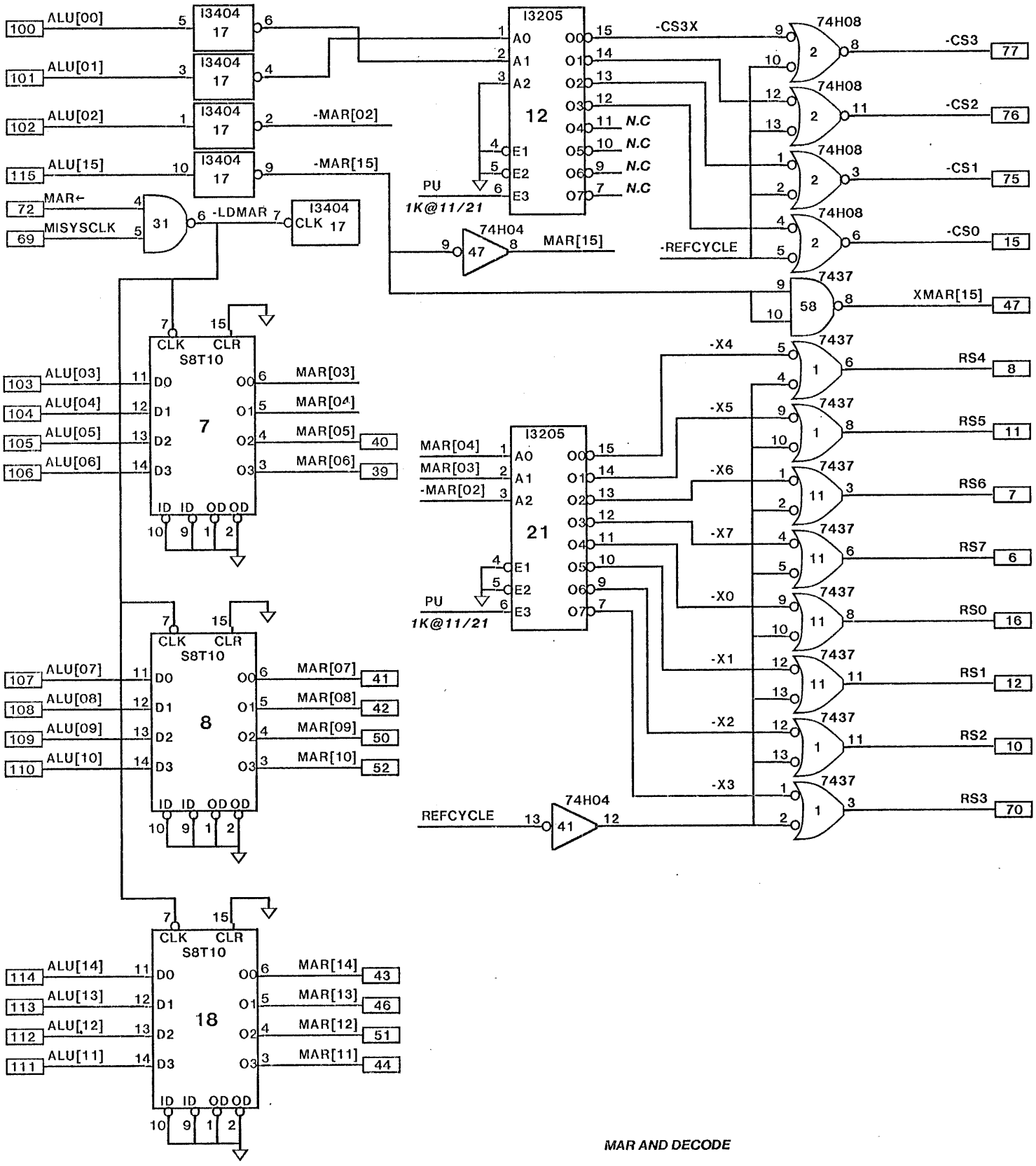

-MTX
7437
22
CE
32
-PC
13
ALL 74H04 IN THE SAME PACKAGE
SELECTED FOR Tpd
-MTO
-←MD
-STORE
MC3026
42
-CE
14
-MT2
7437
69
-MTO1
MTO1
74279
68
MTX01
DXFR
MAR←
CE
-SRESET
74H55
71
-STOP
1
RESET
2
74H00
31
+5V
1K
GONO
64
100
.05mf
GONC
121
74H01
79
74H74
80
N.C
-SRESET
62
-MIARC

CONTROL 2

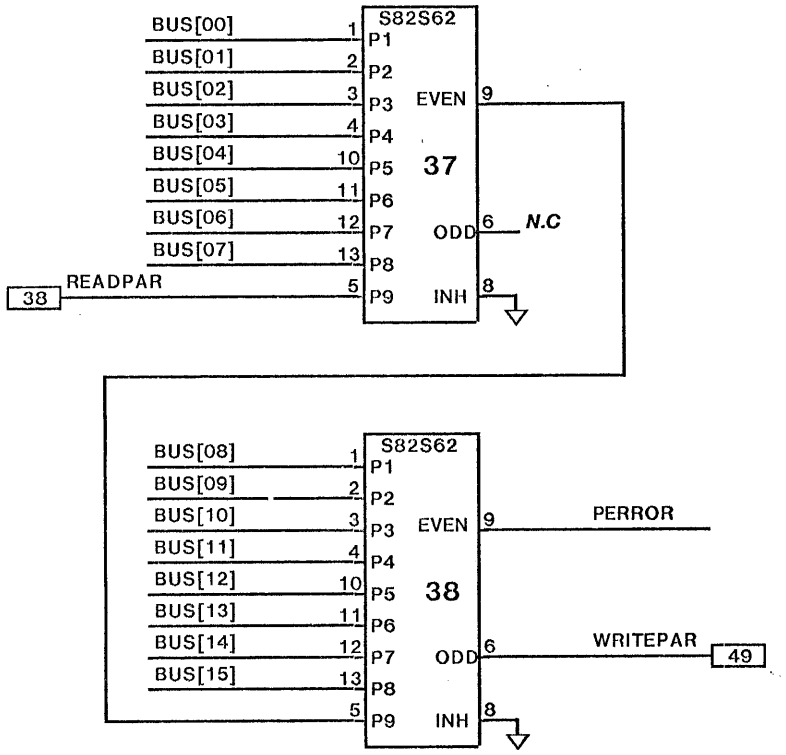

←MD
STOREX
BUS[00]
BUS[01]
BUS[02]
BUS[03]
BUS[04]
BUS[05]
BUS[06]
BUS[07]
BUS[08]
BUS[09]
BUS[10]
BUS[11]
BUS[12]
BUS[13]
BUS[14]
BUS[15]
-MD[00]
-MD[01]
-MD[02]
-MD[03]
-MD[04]
-MD[05]
-MD[06]
-MD[07]
-MD[08]
-MD[09]
-MD[10]
-MD[11]
-MD[12]
-MD[13]
-MD[14]
-MD[15]
7438
MD6300
RSEL0
RSEL1
RSEL2
RSEL3
RSEL4
BS0
BS1
BS2
EN2
EN1
74H08
74H04
←CONST
CONSTANT MEMORY'S
BUS DRIVERS
ALL -MD SIGNALS ARE PULLED UP WITH
330 OHM DISCRETE RESISTORS ON THE BOARD

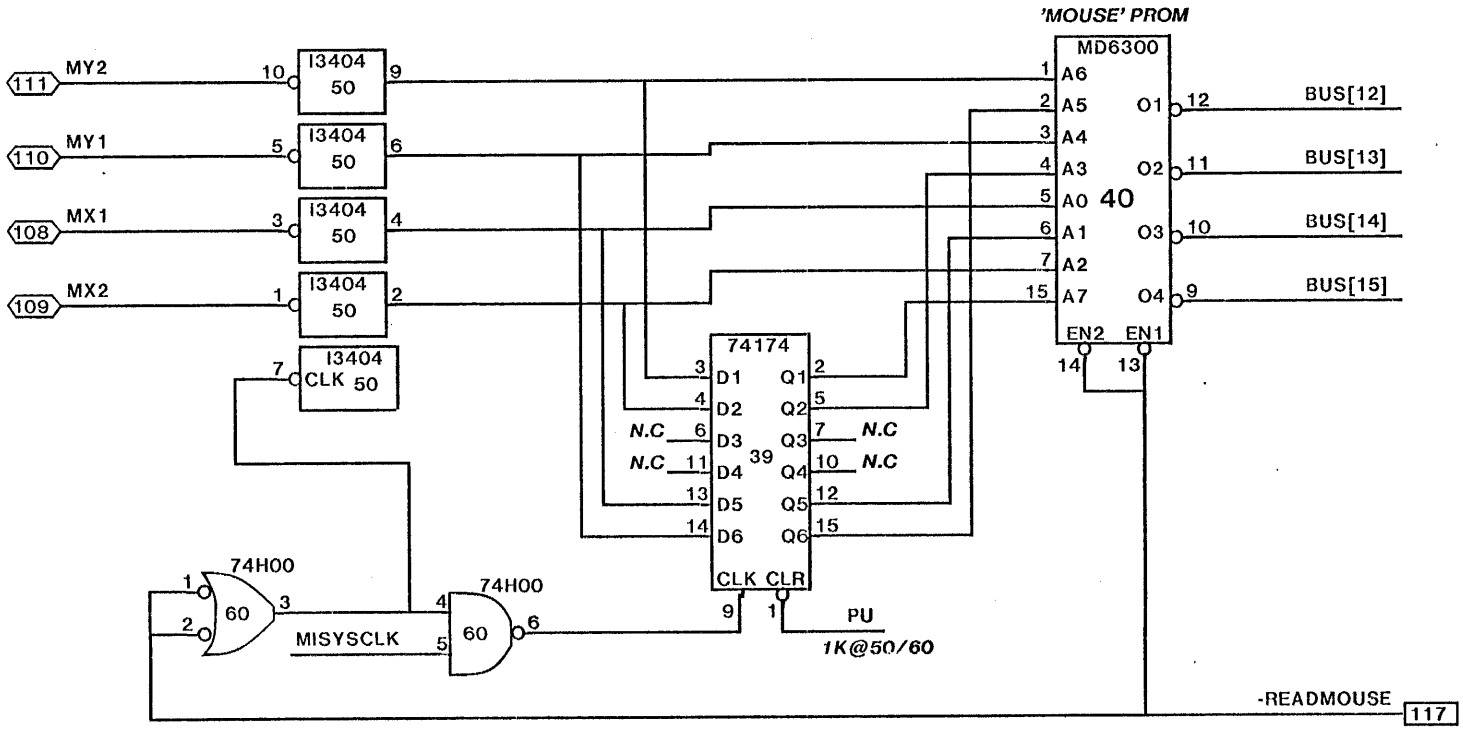


DIABLO PRINTER INTERFACE

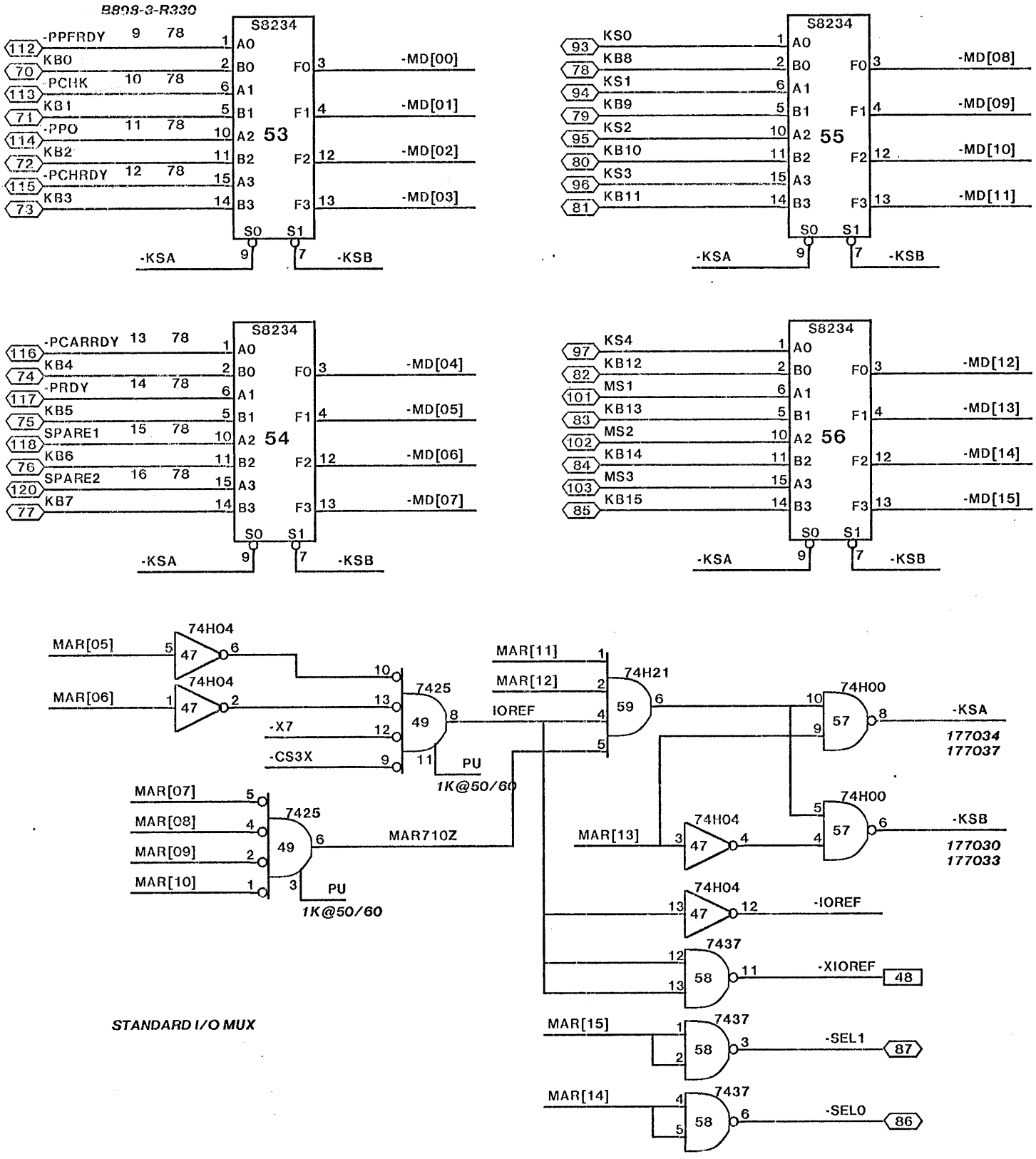


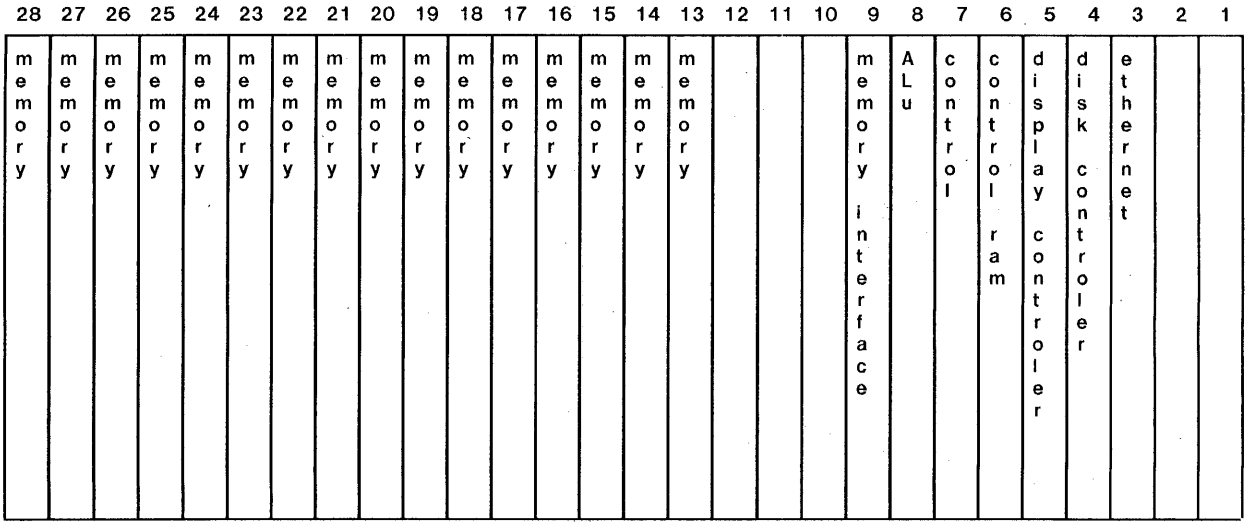
MAR AND DECODE

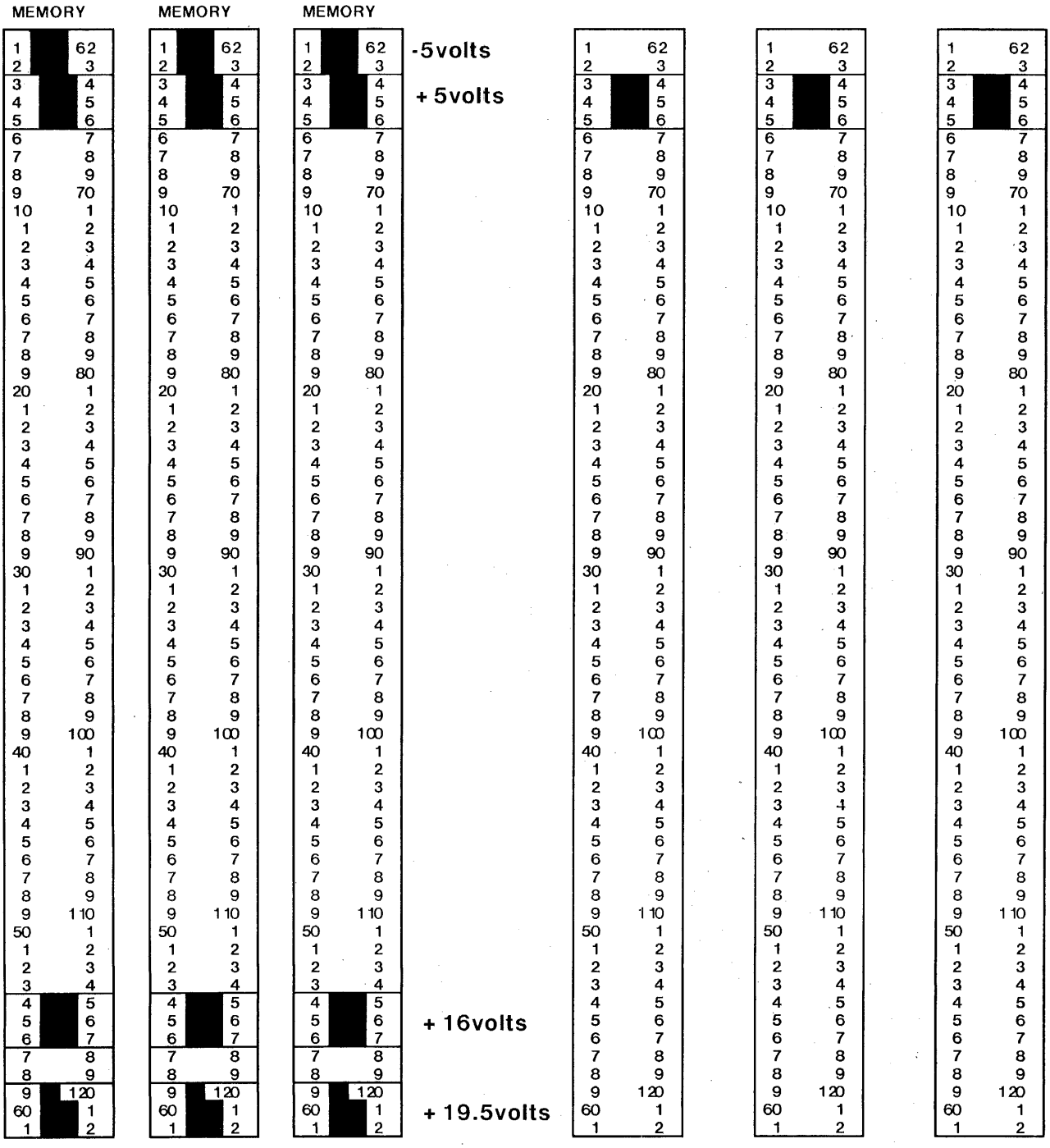




MOUSE AND PARITY


B808-3-R330
S8234
53
-PPFRDY
KB0
-PCHK
KB1
-PPO
KB2
-PCHRDY
KB3
-MD[00]
-MD[01]
-MD[02]
-MD[03]
-KSA
-KSB
S8234
55
KS0
KB8
KS1
KB9
KS2
KB10
KS3
KB11
-MD[08]
-MD[09]
-MD[10]
-MD[11]
-KSA
-KSB
S8234
54
-PCARRDY
KB4
-PRDY
KB5
SPARE1
KB6
SPARE2
KB7
-MD[04]
-MD[05]
-MD[06]
-MD[07]
-KSA
-KSB
S8234
56
KS4
KB12
MS1
KB13
MS2
KB14
MS3
KB15
-MD[12]
-MD[13]
-MD[14]
-MD[15]
-KSA
-KSB
74H04
74H04
7425
49
-X7
-CS3X
PU
1K@50/60
MAR[05]
MAR[06]
MAR[07]
MAR[08]
MAR[09]
MAR[10]
7425
49
MAR710Z
PU
1K@50/60
MAR[11]
MAR[12]
IOREF
74H21
59
74H00
57
-KSA
177034
177037
74H00
57
-KSB
177030
177033
MAR[13]
74H04
74H04
-IOREF
7437
58
-XIOREF
48
MAR[15]
7437
58
-SEL1
87
MAR[14]
7437
58
-SEL0
86
STANDARD I/O MUX


28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory
memory interface
ALU
control
control ram
display controler
disk controler
ethernet


MEMORY
MEMORY
MEMORY
-5volts
+ 5volts
+ 16volts
+ 19.5volts

Even nos. only pop.

28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory	memory				memory interface	ALU	control	control ram	display controller	disk controller	ethernet		

← LEFT SIDE

BACKPLANE VIEW FROM FRONT OF MACHINE

MEMORY	MEMORY	MEMORY				
1 62	1 62	1 62	-5volts	1 62	1 62	1 62
2 3	2 3	2 3		2 3	2 3	2 3
3 4	3 4	3 4	+5volts	3 4	3 4	3 4
4 5	4 5	4 5		4 5	4 5	4 5
5 6	5 6	5 6		5 6	5 6	5 6
6 7	6 7	6 7		6 7	6 7	6 7
7 8	7 8	7 8		7 8	7 8	7 8
8 9	8 9	8 9		8 9	8 9	8 9
9 70	9 70	9 70		9 70	9 70	9 70
10 1	10 1	10 1		10 1	10 1	10 1
1 2	1 2	1 2		1 2	1 2	1 2
2 3	2 3	2 3		2 3	2 3	2 3
3 4	3 4	3 4		3 4	3 4	3 4
4 5	4 5	4 5		4 5	4 5	4 5
5 6	5 6	5 6		5 6	5 6	5 6
6 7	6 7	6 7		6 7	6 7	6 7
7 8	7 8	7 8		7 8	7 8	7 8
8 9	8 9	8 9		8 9	8 9	8 9
9 80	9 80	9 80		9 80	9 80	9 80
20 1	20 1	20 1		20 1	20 1	20 1
1 2	1 2	1 2		1 2	1 2	1 2
2 3	2 3	2 3		2 3	2 3	2 3
3 4	3 4	3 4		3 4	3 4	3 4
4 5	4 5	4 5		4 5	4 5	4 5
5 6	5 6	5 6		5 6	5 6	5 6
6 7	6 7	6 7		6 7	6 7	6 7
7 8	7 8	7 8		7 8	7 8	7 8
8 9	8 9	8 9		8 9	8 9	8 9
9 90	9 90	9 90		9 90	9 90	9 90
30 1	30 1	30 1		30 1	30 1	30 1
1 2	1 2	1 2		1 2	1 2	1 2
2 3	2 3	2 3		2 3	2 3	2 3
3 4	3 4	3 4		3 4	3 4	3 4
4 5	4 5	4 5		4 5	4 5	4 5
5 6	5 6	5 6		5 6	5 6	5 6
6 7	6 7	6 7		6 7	6 7	6 7
7 8	7 8	7 8		7 8	7 8	7 8
8 9	8 9	8 9		8 9	8 9	8 9
9 100	9 100	9 100		9 100	9 100	9 100
40 1	40 1	40 1		40 1	40 1	40 1
1 2	1 2	1 2		1 2	1 2	1 2
2 3	2 3	2 3		2 3	2 3	2 3
3 4	3 4	3 4		3 4	3 4	3 4
4 5	4 5	4 5		4 5	4 5	4 5
5 6	5 6	5 6		5 6	5 6	5 6
6 7	6 7	6 7		6 7	6 7	6 7
7 8	7 8	7 8		7 8	7 8	7 8
8 9	8 9	8 9		8 9	8 9	8 9
9 110	9 110	9 110		9 110	9 110	9 110
50 1	50 1	50 1		50 1	50 1	50 1
1 2	1 2	1 2		1 2	1 2	1 2
2 3	2 3	2 3		2 3	2 3	2 3
3 4	3 4	3 4		3 4	3 4	3 4
4 5	4 5	4 5	+16volts	4 5	4 5	4 5
5 6	5 6	5 6		5 6	5 6	5 6
6 7	6 7	6 7		6 7	6 7	6 7
7 8	7 8	7 8		7 8	7 8	7 8
8 9	8 9	8 9		8 9	8 9	8 9
9 120	9 120	9 120		9 120	9 120	9 120
60 1	60 1	60 1	+19.5volts	60 1	60 1	60 1
1 2	1 2	1 2		1 2	1 2	1 2

BACK PANEL

	SMEM 11	MOSMEM 10	MEMINT 9	ARITH #8	CONTROL #7	DISPLAY 25	DISK 4
1	-5V	-5V	STOP		SRESET	DBSYSCLK STOP	DBSYSCLK
2	-5V	-5V	RESET		RESET	DBARC	DBARC RESET	*SKINC
3	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
4	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
5	+5V	+5V	+5V	+5V	+5V	+5V	+5V	+5V
6	RS7	RS7	RS7		DDR← WAKEMRT	DDR←	*LRI	*RDCLK
7	RS6	RS6	RS6	LOADL	LOADL LOADR	KSYSCLK	KSYSCLK	*SECT(4)
8	RS4	RS4	MISYSCLK	AUSYSCLK	WAKEKST LOADT	AUSYSCLK	WAKEKST	*PDATA
9	RS3	RS3	GND	GND	GND CSYSCLK	GND CSYSCLK	GND	*DISK
10	RS2	RS2	MIARC	IR(04)	IR(04) IR←	MIARC	*NORACK	*SRWRDY
11	RS5	RS5	MAR←	(01)	(01) MAR←	AUSYSCLK		
12	RS1	RS1	STORE	(02)	(02) STORE			
13	PC	PC	SELR37	(03)	(03) SELR37			
14	CE	CE	CS1	(04)	(04) DNS			
15	CS04	CS04	CS2	(05)	(05) WAKEDVT	WAKEDVT		
16	RS0	RS0	CS3	(06)	IR(06) WAKEDHT	WAKEDHT	*READY	
17	W1	W1	GND	GND	GND IR(07)	GND	GND	
18	DS1	DS1	W0	(08)	IR(08) WAKEKWDT		*KSECT(2)	WAKEKWDT
19	ME(02)	DS0	BUS(00)	(09)	BUS(00) IR(09)	BUS(00)	(1)	BUS(00)
20	MD(00)	MD(00)	(01)	(10)	(01) STOPCLK	STOPCLK	(2)	(01)
21	MD(01)	(01)	(02)	(11)	(02) WAKEDWT	WAKEDWT	*KSECT(3)	(02)
22	MD(03)	(02)	(03)	(12)	(03) DVTAC	DVTAC		(03)
23	MD(01)	(03)	(04)	(13)	(04) DHTAC	DHTAC		(04)
24	MD(04)	(04)	(05)	(14)	(05) DWTAC	DWTAC		(05)
25	MD(02)	(05)	(06)	IR(15)	(06) KWDTAC		KWDTAC	(06)
26	MD(03)	MD(06)	(07)	SHZERO	(07) SHZERO			(07)
27	ME(04)	GND	(08)	GND	(08) GND	GND	GND	(08)
28	MD(05)	MD(07)	(09)		(09) KSTAC		KSTAC	(09)
29	MD(04)	(08)	(10)		(10)			(10)
30	MD(05)	(09)	(11)		(11) FI(0)		FI(0)	(11)
31	MD(07)	MD(12)	(12)		(12) FI(1)		FI(1)	(12)
32	MD(06)	(11)	(13)		(13) FI(2)		FI(2)	(13)
33	MD(06)	(12)	(14)		(14) FI(3)		FI(3)	(14)
34	MD(07)	MD(11)	MD(13)	BUS(15)	ZEROBUS BUS(15)	BUS(15)		BUS(15)
35	MD(08)	MD(13)	GND	←MD	GND	GND	GND	
36	MD(09)	MD(14)	MD(14)	CONST←	F2(0)	CONST←	F2(0)	
37	MD(10)	MD(15)	MD(15)	←DISP	F2(1)	←DISP	F2(1)	
38	MD(11)	READPAR	READPAR	EMACT	F2(2)	EMACT	F2(2)	
39	MAR(02)	MAR(06)	MAR(06)	ALU(00)	ALU(00) F2(3)	NEXT(00)	F2(3)	
40	MAR(05)	MAR(05)	MAR(05)	(01) ALUF0	(01) ALUF0	(01)		
41	MAR(07)	MAR(07)	MAR(07)	(02) 1	(02) 1	(02)		
42	MAR(08)	MAR(08)	MAR(08)	(03) 2	(03) 2	(03)		
43	MAR(14)	MAR(14)	MAR(14)	(04) ALUF3	(04) ALUF3	(04)		
44	MAR(11)	MAR(11)	MAR(11)	(05) BSZO	(05) BSZO	(05)		NEXT(05)
45	MAR(13)	MAR(13)	GND	(06) GND	(06) GND	(06) GND	GND	NEXT(06)
46	MD(08)	MD(13)	MAR(13)	(07) LSHI	(07) LSHI	(07)		(07)
47	MD(09)	MD(14)		(08) RSHI	(08) RSHI	(08)		(08)
48	MD(10)	MD(15)		(09) LCY8	(09) LCY8	NEXT(09)	NEXT(09)	NEXT(09)
49	MD(11)	WritePar	WritePar	(10) LALUC0	(10) LALUC0	BLOCK	BLOCK	BLOCK
50	MAR(09)	MAR(09)	MAR(09)	(11) SH(00)	(11) SH(00)	←KDATA	*RDGATE	←KDATA
51	MAR(12)	MAR(12)	MAR(12)	(12)	(12) FZ←10	←KSTAT FZ←10	*WRTGATE	←KSTAT
52	MAR(10)	MAR(10)	MAR(10)	(13)	(13)		*WRTDATA	*STROBE
53	+16V	GND	(14)	GND	(14) GND	CURTAC GND	CURTAC GND	
54	+16V	RSEL4	ALU(15)	RSEL4	ALU(15) RSEL4	WAKECURT	WAKECURT *DISK	*RESTOR
55	+16V	1		1	FZ←11 1	FZ←11	FZ←11	*HEAD
56	+16V	2	READMOUS	2	2 READMOUS		*CYL(0)	*CYL(1)
57	+20V	3	WAKEPART	3	3 WAKEPART		*CYL(2)	*CYL(3)
58	—	—	—	—	—	—	—	—
59	+20V	RSEL4	BS0	RSEL4	RSEL4 BS0		*CYL(4)	*CYL(5)
60	+20V		BS1	L(15)	L(15) BS1		*CYL(6)	*CYL(7)
61	+20V	PARTAC	BS2		PARTAC BS2		*CYL(8)	

NoPins
NoPins
GND
GND

ALTO MEMORY ARRANGEMENT PRINTED CIRCUIT VERSION

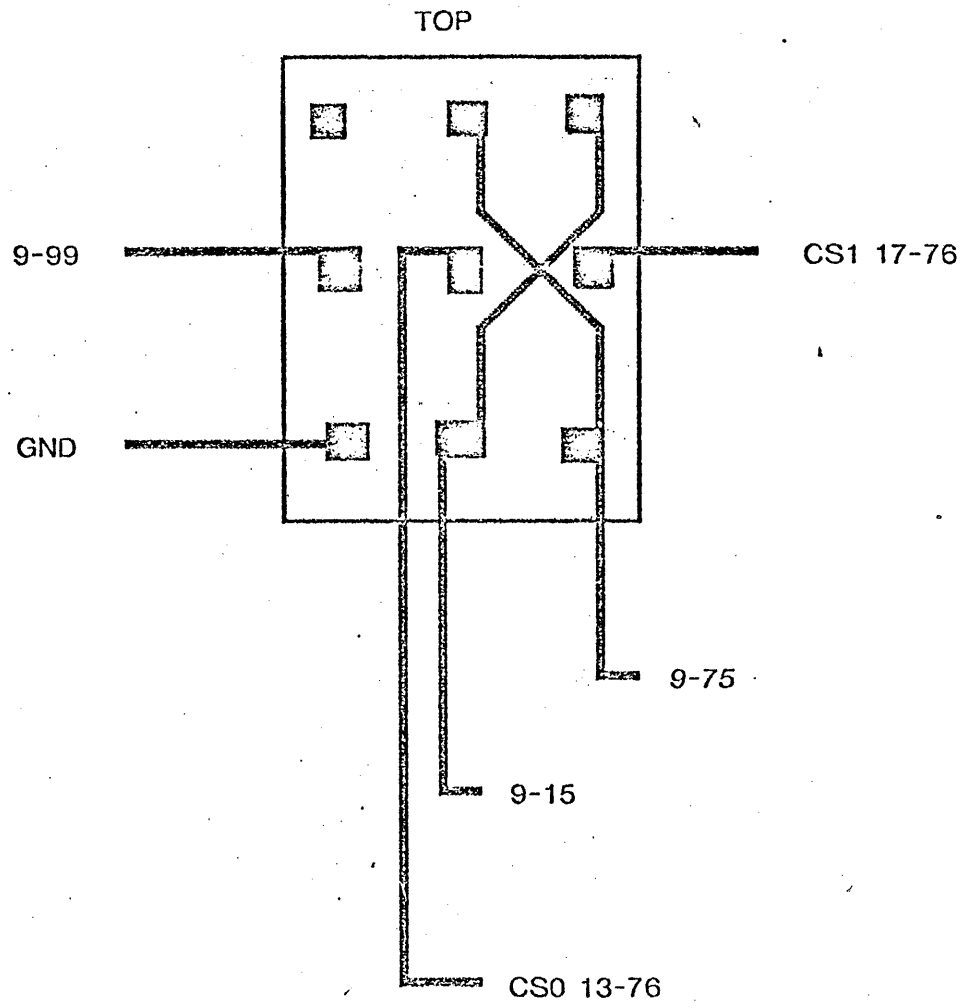
ADDRESS MINIMUM	ADDRESS MAXIMUM	CARD ROW	CARD SLOT
000000	003777	0	EVEN ADDRESSES
004000	007777	1	13 - BITS 0-11
010000	013777	2	14 - BITS 12-15 & PARITY
014000	017777	3	
020000	023777	4	ODD ADDRESSES
024000	027777	5	15 - BITS 0-11
030000	033777	6	16 - BITS 12-15 & PARITY
034000	037777	7	
040000	043777	0	EVEN ADDRESSES
044000	047777	1	17 - BITS 0-11
050000	053777	2	18 - BITS 12-15 & PARITY
054000	057777	3	
060000	063777	4	ODD ADDRESSES
064000	067777	5	19 - BITS 0-11
070000	073777	6	20 - BITS 12-15 & PARITY
074000	077777	7	
100000	103777	0	EVEN ADDRESSES
104000	107777	1	21 - BITS 0-11
110000	113777	2	22 - BITS 12-15 & PARITY
114000	117777	3	
120000	123777	4	ODD ADDRESSES
124000	127777	5	23 - BITS 0-11
130000	133777	6	24 - BITS 12-15 & PARITY
134000	137777	7	
140000	143777	0	EVEN ADDRESSES
144000	147777	1	25 - BITS 0-11
150000	153777	2	26 - BITS 12-15 & PARITY
154000	157777	3	
160000	163777	4	ODD ADDRESSES
164000	167777	5	27 - BITS 0-11
170000	173777	6	28 - BITS 12-15 & PARITY
174000	177777	7	

odd slots

EVEN SLOTS

WORD BIT	CARD COLUMN	WORD BIT	CARD COLUMN
0	0	12	7
1	1	13	8
2	2	14	9
3	3	15	10
4	4	PAR	11
5	5		
6	6		
7	7		
8	8		
9	9		
10	10		
11	11		

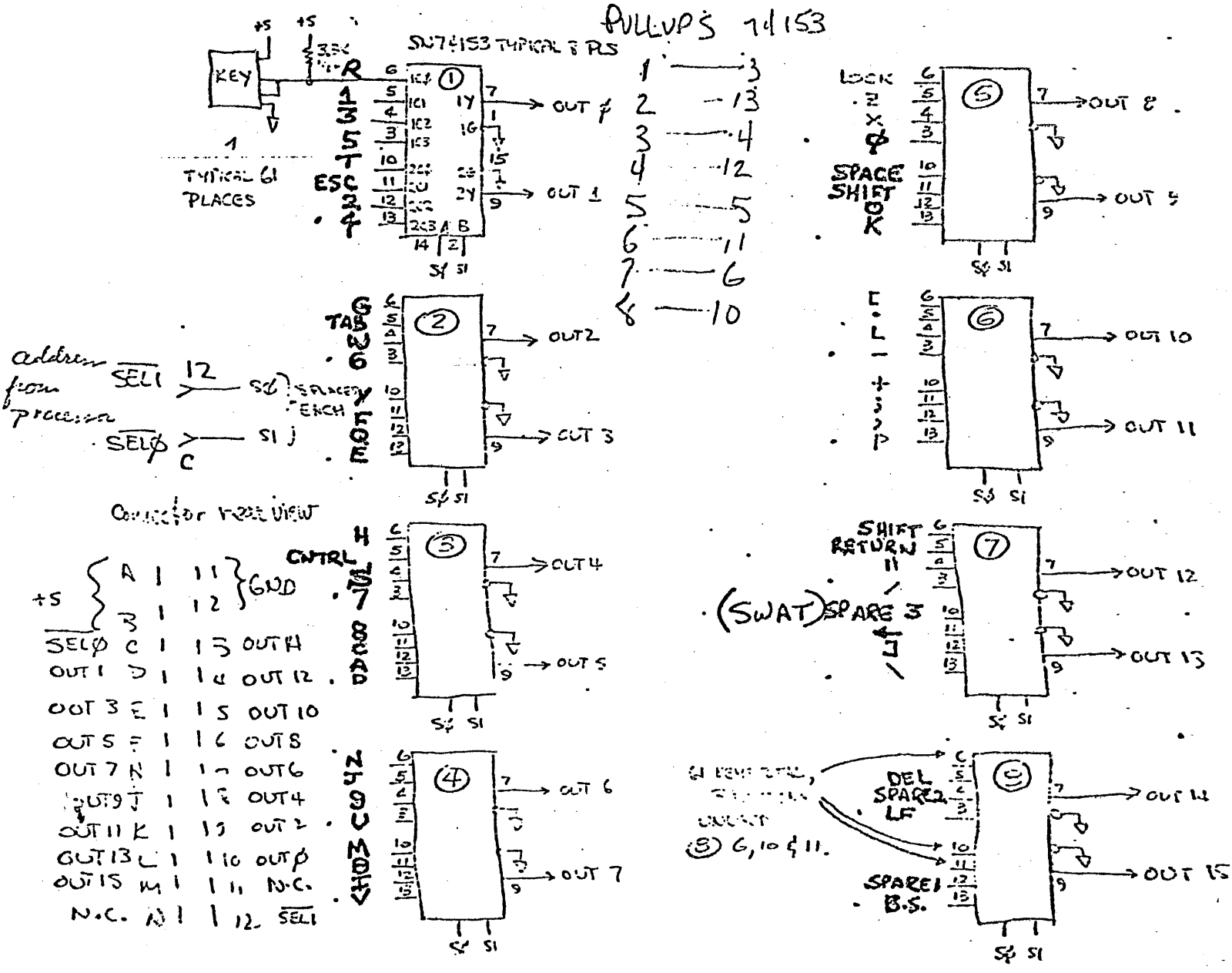
ALTO MEMORY SWITCH



12-19 Output 5/8 high when key depressed

KEYBOARD:

The keyboard has 61 keys. It will receive a 2 bit address from the processor which will select one of four groups of key signals to be gated to the 16 output lines. Output lines are low when key is depressed. The keyboard requires an 18 line (plus power) interface to the processor; 16 data lines and two address lines. The four groups include 16, 16, 16, and 13 keys respectively. The relation between keys and bits in the output word is not important, and will be determined primarily by PC layout considerations.



SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
GONO	A/ 1	#26	BUTTON NORMALLY OPEN CONTACT	BLUE/BLACK
KB0	2		D/ 10	VIOLET
KB1	3		D/ D	YELLOW/BLACK
KB2	4		D/ 9	BLUE
KB3	5		D/ E	YELLOW/BROWN
KB4	6		D/ 8	GREEN
KB5	7		D/ F	YELLOW/RED
KB6	8		D/ 7	YELLOW
KB7	9		D/ H	YELLOW/ORANGE
KB8	10		D/ 6	ORANGE
KB9	11		D/ J	YELLOW/GREEN
KB10	12		D/ 5	RED
KB11	13		D/ K	YELLOW/BLUE
KB12	14		D/ 4	BROWN
KB13	15		D/ L	YELLOW/VIOLET
KB14	16		D/ 3	BLACK
KB15	17		D/ M	YELLOW/GREY
SELØ'	18		D/ C	WHITE
SEL1'	19		D/ 12	GREY
KSØ	20		C/ 11	ORANGE/BLACK
KS1	21		C/ 10	ORANGE/BROWN
KS2	22		C/ 9	ORANGE/RED
KS3	23		C/ 8	ORANGE/BLUE
KS4	24		C/ 7	ORANGE/VIOLET
MS1	25		B/ 14	WHITE/BLACK
MS2	26		B/ 16	WHITE/BROWN
MS3	27		B/ 15	WHITE/RED
MX1	28		B/ 2	WHITE/ORANGE
MX2	29		B/ 1	WHITE/YELLOW
MY1	30		B/ 3	WHITE/GREEN
MY2	31	↓	B/ 4	WHITE/BLUE

CABLE: KEYBOARD CABLE (EXTERNAL)

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
GONC	A/ 32	#26	BUTTON NORMALLY CLOSED CONTACT	BLUE/BROWN
MOUSE +5	D/ A	#24	B/ 6	WHITE
MOUSE GROUND	D/ 1	#24	B/ 19	THESE ARE ISOLATED WIRES, NOT BL
KEYSET GROUND	D/ 1	#24	C/ 19	PART OF THE CABLE BLACK
KEYBOARD +5	A/35	#18	D/ A	WHITE
KEYBOARD -GND	A/37	#18	D/ 1	BLACK

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN
GOND	A/ 64	#24	B/ 1
P.PFSTR'	65		C/ 1
PREST'	66		C/ 2
PRIB'	67		C/ 3
PCHSTR'	68		C/ 4
PCARSTR'	69		C/ 5
KBØ	70		B/ 2
KB1	71		B/ 3
KB2	72		B/ 4
KB3	73		B/ 5
KB4	74		B/ 6
KB5	75		B/ 7
KB6	76		B/ 8
KB7	77		B/ 9
KB8	78		B/ 10
KB9	79		B/ 11
KB10	80		B/ 12
KB11	81		B/ 13
KB12	82		B/ 14
KB13	83		B/ 15
KB14	84		B/ 16
KB15	85		B/ 17
SELØ'	86		B/ 18
SEL1'	87		B/ 19
PDATA1024'	88		C/ 6
PDATA512'	89		C/ 7
PDATA256'	90		C/ 8
PDATA128'	91		C/ 9
KSØ	93		B/ 20
KS1	94		B/ 21
KS2	95		B/ 22

KEYBOARD / PRINTER INTERNAL CABLE

3 4 2/14/74

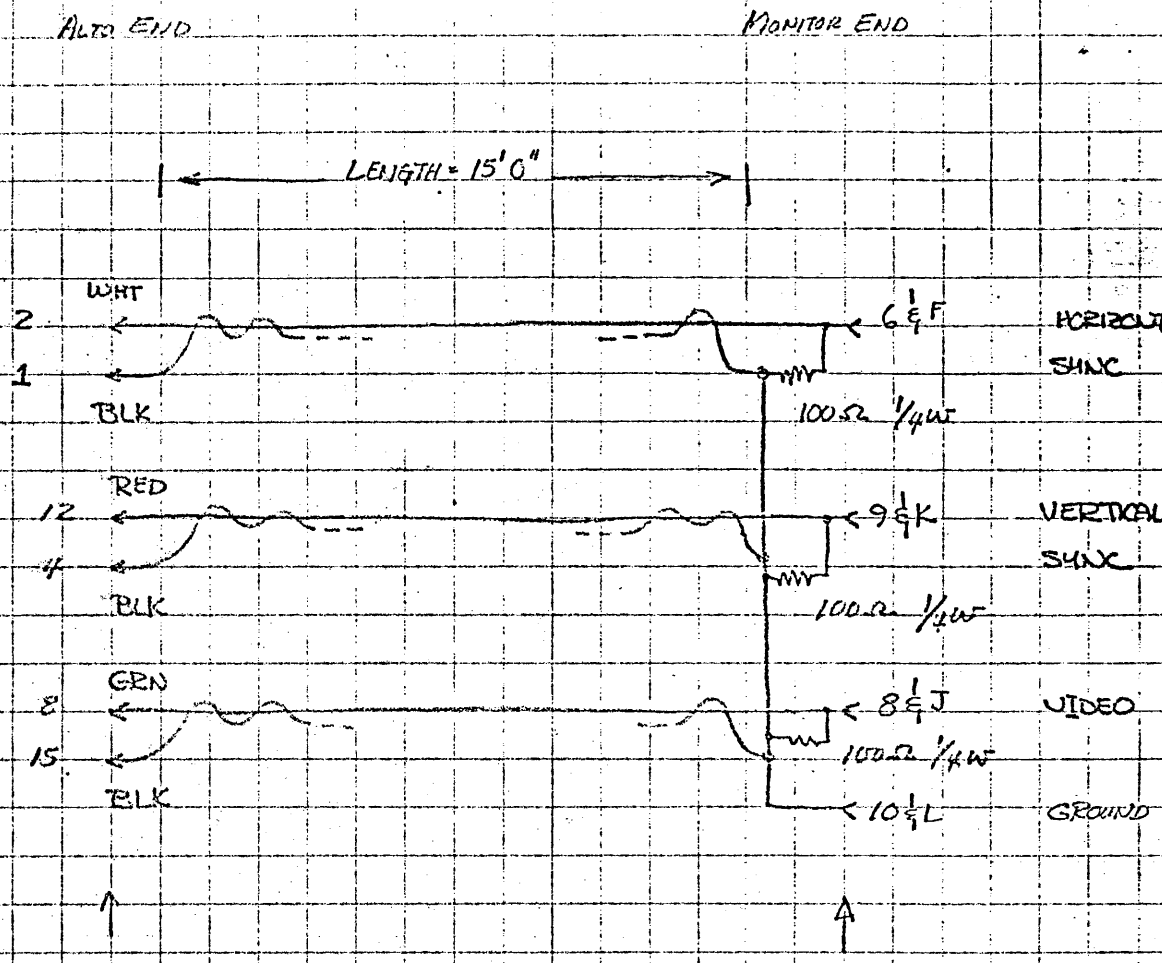
SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN
KS3	A/ 96	#24	B/ 23
KS4	97		B/ 24
PDATA4'	98		C/ 10
PDATA32'	99		C/ 11
PDATA16'	100		C/ 12
MS1	101		B/ 25
MS2	102		B/ 26
MS3	103		B/ 27
PDATA8'	104		C/ 13
PDATA4'	105		C/ 14
PDATA2'	106		C/ 15
PDATA1'	107		C/ 16
MX1	108		B/ 28
MX2	109		B/ 29
MY1	116		B/ 30
MY2	111		B/ 31
PPFRDY'	112		C/ 17
PCHK'	113		C/ 20
PPO'	114		C/ 21
PCHRDY'	115		C/ 22
PCARRDY'	116		C/ 23
PRDY'	117		C/ 24
SPARE1	~~118~~ 120		B/ 33
SPARE2	~~120~~ 122		B/ 34
GONC	121		B/ 32
PRINTER LOGIC GROUND	56		C/ 25
" " "	57		C/ 26
" " "	59		C/ 27
" " "	60		C/ 28
" " "	61		C/ 29

CABLE: KEYBOARD/PRINTER INTERNAL CABLE — PG 4 OF 4 — ALB 2/14/74

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
PRINTER POWER GROUND	D/ 2	#18	C/ 18	
PRINTER +15	D/ 4	#18	C/ 19	
PRINTER -15	D/ 1	#18	C/ 36	
PRINTER +5	D/ 3	#18	C/ 37	
KEYBOARD +5	A/ 1	#24	B/ 35	
KEYBOARD GND	A/55	"	B/37	

ALTO

DISPLAY EXTERNAL CABLE 1 OF 1 4-15-74 CT.



QTY:	CANNON PART:	CABLE: BELDEN # 9745	AMPHENOL #225-21031-101
(1)	DAC-15P SHELL		CONNECTOR
(1)	DA 51210-1 PLASTIC JUNCTION SHELL		
(6)	030-1952-000 PINS		
(1)	DA 51220-1 SLIDING LOCK RETAINER		1 REQD / SYSTEM

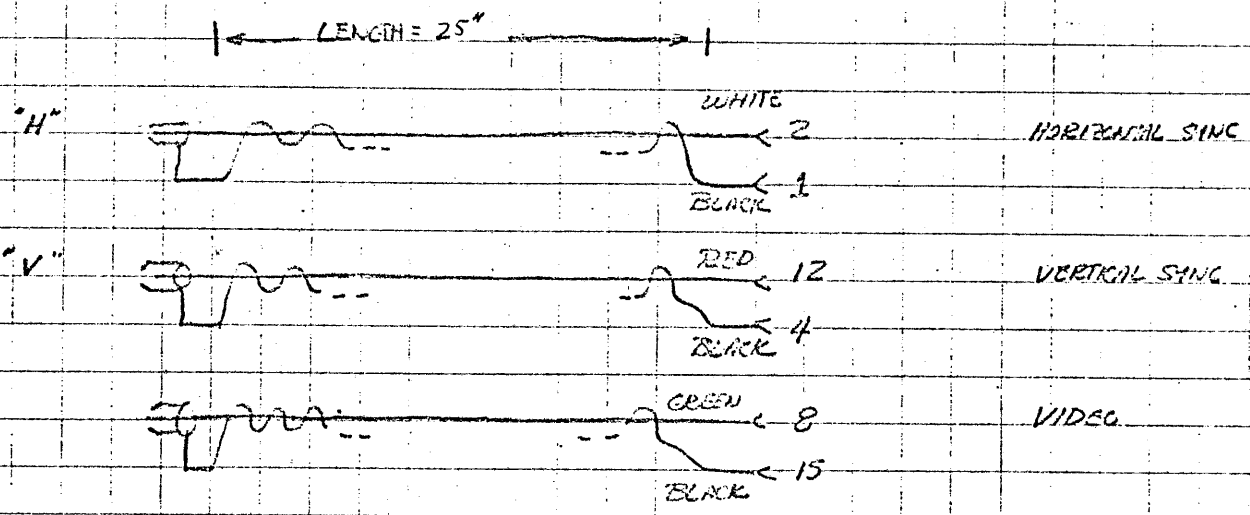
PIN INSERTION/EXTRACTION TOOL: CICT 20HDB

CRIMP TOOL M22520/1-01

LOCATOR TH185

A-10

DISPLAY INTERNAL CABLE 1 OF 1 4-15-71 CT.



CABLE: BELDEN #9775

CANNON DAC 15S SHELL

(3) AMP 20197-3 CONNECTOR PIN (6) 030-1953-000 FEMALE CONTACT

(3) AMP 329006 FERRULE

CRIMP TOOL IS AMP # 45634-3

1 REQ'D/SYSTEM

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
TERMINATOR +5	A/ 1		B/ PP	
GROUND	59		D	THESE PINS ARE COMMON ON THE PADDLEBOA
GROUND	60		DD	
GROUND	61		WW	
DISK'	67		R	
DISK	69		L	
CYL(7)'	73		N	
SKINC'	74		TT	
RDCLK'	76		A	
READY'	78		U	
RESTOR'	79		VV	
KSECT(3)	80		CC	
CYL(3)'	81		FF	
WRTGATE'	82		EE	
SRWRDY'	83		F	
KSECT(1)	84		KK	
KSECT (2)	85		JJ	
CYL(8)'	86		LL	
RDDATA'	87		C	
CYL (4)'	88		X	
CYL(1)'	89		BB	
CYL(5)'	90		J	
WRTDATA'	91		B	
CYL(6)'	93		RR	
HEAD'	94		AA	
STROBE'	96		SS	
SECT (4)'	100		W	
RDGATE'	103		E	
LAI'	104		XX	
ADRACK'	105		NN	

DISK PATH CABLE — Disk Data Cable — 3 of 3 — ALTO

SIGNAL	FROM CONNECTOR/PIN	VIA CABLE/COLOR	TO CONNECTOR/PIN	
KSECT(0)	A/ 106		B/ MM	
CYL(0)'	107		Z	
CYL(2)'	109		T	
ERGATE'	110		K	

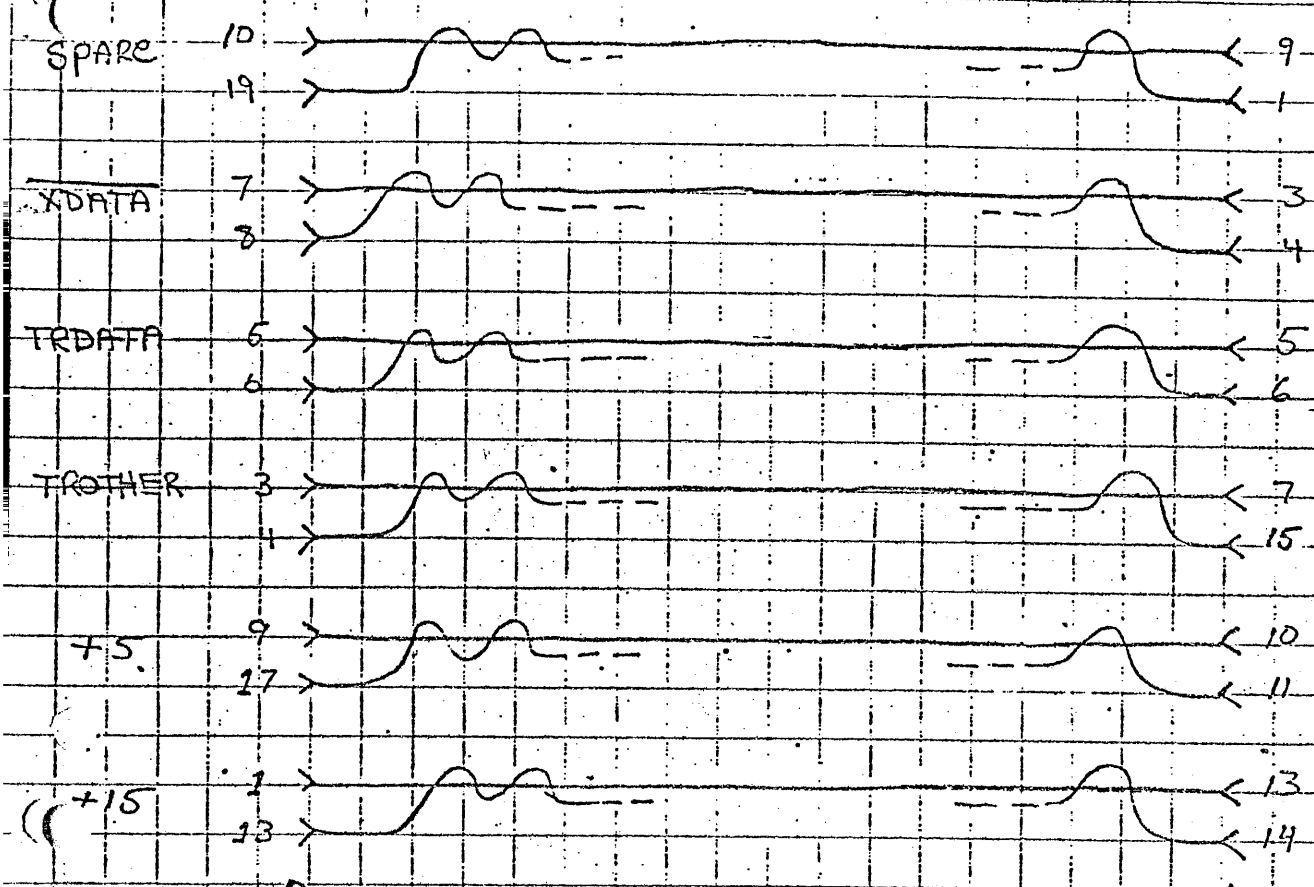
SIGNAL NAME	ALTO BUS INFORMATION	Alto 1 37 PIN CANNON	Alto 2 25 PIN CANNON	WIRE COLOR
-PPFSTR	BUSOUT(00)	1	13	
-PREST	BUSOUT(01)	2	25	
-PRIB	BUSOUT(02)	3	12	
-PCHSTR	BUSOUT(03)	4	24	
-PCARSTR	BUSOUT(04)	5	11	
-PDATA1024	BUSOUT(05)	6	23	
-PDATA512	BUSOUT(06)	7	10	
-PDATA256	BUSOUT(07)	8	22	
-PDATA128	BUSOUT(08)	9	9	
-PDATA64	BUSOUT(09)	10	21	
-PDATA32	BUSOUT(10)	11	8	
-PDATA16	BUSOUT(11)	12	20	
-PDATA8	BUSOUT(12)	13	7	
-PDATA4	BUSOUT(13)	14	19	
-PDATA2	BUSOUT(14)	15	6	
-PDATA1	BUSOUT(15)	16	18	
-PPFRDY	BUSIN(00)	17	5	
-PCHK	BUSIN(01)	20	17	
-PPO	BUSIN(02)	21	4	
-PCHRDY	BUSIN(03)	22	16	
-PCARRDY	BUSIN(04)	23	15	
-PRDY	BUSIN(05)	24	3	
PRINTERGND	LOGICGND	25	14	
PRINTERGND	LOGICGND	26	1	
PRINTERGND	LOGICGND	27		
PRINTERGND	LOGICGND	28		
PRINTERGND	LOGICGND	29		
POWERGND	LOGICGND	18		
PRINTER+15V	+15V	19		
PRINTER-15V	-15V	36		
PRINTER+5V	VCC	37		

ETHERNET INTERNAL CABLE 1 of 1 6/26/79 DB

ALTO I

Length 26"

1 to 1 for ALTO I



AMP

CABLE: BELDEN 8747

CANNON

QTY	PART
(1)	87133-6 SHELL
(10)	87165-1 Pins

CRIMP TOOL IS AMP 90289-1

EXTRACTION TOOL IS AMP 91084-1

QTY	PART
(1)	DAC 15S SHELL
(10)	030-1953-000 Female CONTACT
(2)	D53018 SLIDING LOCK P

1 Required / System

20	10
19	9
18	8
17	7
16	6
15	5
14	4
13	3
12	2
11	1

Pin numbering FOR AMP CONNECTOR — CABLE END SHOWN.

NOTE that the SOCKET IS NOT KEYED. Which ever way you position it IS OK.