Ultra-Small, Low-Power, SPI™-Compatible, 16-Bit Analog-to-Digital Converter and Temperature Sensor with Internal Reference

Check for Samples: ADS1118

FEATURES

- **Ultra-Small QFN Package: 2 mm × 1,5 mm × 0,4 mm**
- **Wide Supply Range: 2.0 V to 5.5 V**
- **Low Current Consumption:**
  - **Continuous Mode: Only 150 µA**
  - **Single-Shot Mode: Auto Power-Down**
- **Programmable Data Rate: 8 SPS to 860 SPS**
- **Single-Cycle Settling**
- **Internal Low-Drift Voltage Reference**
- **Internal Temperature Sensor: 0.5°C (max) Error**
- **Internal Oscillator**
- **Internal PGA**
- **Four Single-Ended or Two Differential Inputs**

APPLICATIONS

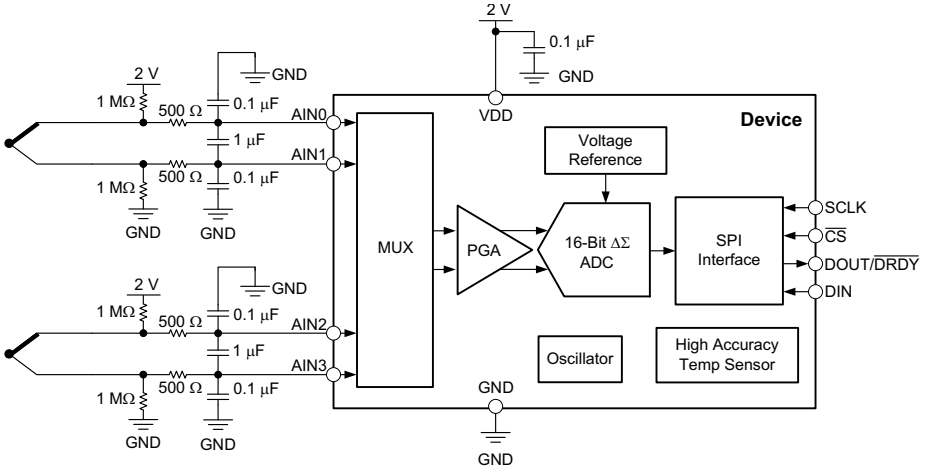
- **Temperature Measurement:**
  - **Thermocouple Measurement**
  - **Cold Junction Compensation**
  - **Thermistor Measurement**
- **Portable Instrumentation**
- **Factory Automation and Process Controls**

DESCRIPTION

The ADS1118 is a precision analog-to-digital converter (ADC) with 16 bits of resolution offered in an ultra-small, leadless QFN-10 package or an MSOP-10 package. The ADS1118 is designed with precision, power, and ease of implementation in mind. The ADS1118 features an integrated voltage reference and oscillator. Data are transferred via a serial peripheral interface (SPI). The ADS1118 operates from a single power supply ranging from 2.0 V to 5.5 V.

The ADS1118 can perform conversions at rates up to 860 samples per second (SPS). A programmable gain amplifier (PGA) is integrated in the ADS1118 that offers input ranges from as low as ±256 mV up to the supply rails, allowing both large and small signals to be measured with high resolution. The ADS1118 also features an input multiplexer (MUX) that provides two differential or four single-ended inputs. The ADS1118 can also function as a high-accuracy temperature sensor. This temperature sensor can be used for system-level temperature monitoring or cold junction compensation for thermocouples.

The ADS1118 operates either in continuous conversion mode or single-shot mode that automatically powers down after a conversion. Single-shot mode significantly reduces current consumption during idle periods. The ADS1118 is specified from –40°C to +125°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

SPI is a trademark of Motorola.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ORDERING INFORMATION

For the most current package and ordering information, see the Package Option Addendum at the end of this document, or visit the device product folder on www.ti.com.

ABSOLUTE MAXIMUM RATINGS(1)

		VALUE	UNIT
VDD to GND		–0.3 to +5.5	V
Analog input current		100, momentary	mA
		10, continuous	mA
Analog input voltage to GND		–0.3 to VDD + 0.3	V
DIN, DOUT/$\overline{\text{DRDY}}$, SCLK, $\overline{\text{CS}}$ voltage to GND		–0.3 to +5.5	V
Electrostatic discharge (ESD) ratings	Human body model (HBM) JEDEC standard 22, test method A114-C.01, all pins	±4000	V
	Charged device model (CDM) JEDEC standard 22, test method C101, all pins	±1000	V
Operating temperature range		–40 to +125	°C
Maximum junction temperature		+150	°C
Storage temperature range		–60 to +150	°C

(1) Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

PRODUCT FAMILY

DEVICE	RESOLUTION (Bits)	MAXIMUM SAMPLE RATE (SPS)	INPUT CHANNELS [Differential (Single-Ended)]	PGA	INTERFACE	SPECIAL FEATURES	PACKAGE DESIGNATOR MSOP, QFN
ADS1118	16	860	2 (4)	Yes	SPI	Temperature sensor	BBEI, SDQ
ADS1018	12	3300	2 (4)	Yes	SPI	Temperature sensor	BTNQ, SDZ
ADS1115	16	860	2 (4)	Yes	I^2C	Comparator	BOGI, N4J
ADS1114	16	860	1 (1)	Yes	I^2C	Comparator	BRNI, N5J
ADS1113	16	860	1 (1)	No	I^2C	None	BROI, N6J
ADS1015	12	3300	2 (4)	Yes	I^2C	Comparator	BRPI, N7J
ADS1014	12	3300	1 (1)	Yes	I^2C	Comparator	BRQI, N8J
ADS1013	12	3300	1 (1)	No	I^2C	None	BRMI, N9J

ELECTRICAL CHARACTERISTICS

Maximum and minimum specifications are at T_A = –40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale (FS) = ±2.048 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUT					
Full-scale input voltage range(1)	V_{IN} = (AIN_P) – (AIN_N)		See Table 2		
Analog input voltage	AIN_P or AIN_N to GND	GND		VDD	V
Differential input impedance			See Table 1		
Common-mode input impedance	FS = ±6.144 V(1)		8		MΩ
	FS = ±4.096 V(1), ±2.048 V		6		MΩ
	FS = ±1.024 V		3		MΩ
	FS = ±0.512V, ±0.256 V		100		MΩ
SYSTEM PERFORMANCE					
Resolution	No missing codes	16			Bits
Data rate (DR)			8, 16, 32, 64, 128, 250, 475, 860		SPS
Data rate variation	All data rates	–10		10	%
Output noise			See Typical Characteristics		
Integral nonlinearity	DR = 8 SPS, FS = ±2.048 V(2)			1	LSB
Offset error	FS = ±2.048 V, differential inputs		±0.1	±2	LSB
	FS = ±2.048 V, single-ended inputs		±0.25		LSB
Offset drift	FS = ±2.048 V		0.002		LSB/°C
Offset power-supply rejection	FS = ±2.048 V, with dc supply variation		0.2		LSB/V
Gain error(3)	FS = ±2.048 V at T_A = +25°C		0.01	0.15	%
Gain drift(3)(4)	FS = ±0.256 V		7		ppm/°C
	FS = ±2.048 V		5	40	ppm/°C
	FS = ±6.144 V(1)		5		ppm/°C
Gain power-supply rejection			10		ppm/V
PGA gain match(3)	Match between any two PGA gains		0.01	0.1	%
Gain match	Match between any two inputs		0.01	0.1	%
Offset match	Match between any two inputs		0.6		LSB
Common-mode rejection	At dc and FS = ±0.256 V		105		dB
	At dc and FS = ±2.048 V		100		dB
	At dc and FS = ±6.144 V(1)		90		dB
	f_{CM} = 50 Hz, DR = 860 SPS		105		dB
	f_{CM} = 60 Hz, DR = 860 SPS		105		dB
TEMPERATURE SENSOR					
Temperature sensor range		–40		+125	°C
Temperature sensor resolution			0.03125		°C/LSB
Temperature sensor accuracy	T_A = 0°C to +70°C		0.2	±0.5	°C
	T_A = –40°C to +125°C		0.4	±1	°C
	vs supply		0.03125	±0.25	°C/V

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V or 5.5 V (whichever is smaller) be applied to this device.
(2) Best-fit INL; covers 99% of full-scale.
(3) Includes all errors from onboard PGA and reference.
(4) Not production tested; ensured by characterization.

ELECTRICAL CHARACTERISTICS (continued)

Maximum and minimum specifications are at T_A = –40°C to +125°C, unless otherwise noted. Typical values are at T_A = +25°C. All specifications are at VDD = 3.3 V, data rate = 8 SPS, and full-scale (FS) = ±2.048 V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
DIGITAL INPUT/OUTPUT					
Logic level					
V_{IH}		0.7 VDD		VDD	V
V_{IL}		GND		0.2 VDD	V
V_{OH}	I_{OH} = 1 mA	0.8 VDD			V
V_{OL}	I_{OL} = 1 mA	GND		0.2 VDD	V
Input leakage					
I_H	V_{IH} = 5.5 V			±10	µA
I_L	V_{IL} = GND			±10	µA
POWER-SUPPLY REQUIREMENTS					
Power-supply voltage		2		5.5	V
Supply current	Power-down current at T_A = +25°C		0.5	2	µA
	Power-down current up to T_A = +125°C			5	µA
	Operating current at T_A = +25°C		150	200	µA
	Operating current up to T_A = +125°C			300	µA
Power dissipation	VDD = 5.0 V		0.9		mW
	VDD = 3.3 V		0.5		mW
	VDD = 2.0 V		0.3		mW
TEMPERATURE					
Storage temperature		–60		+150	°C
Specified temperature		–40		+125	°C

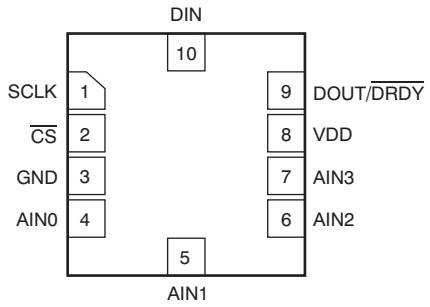
THERMAL INFORMATION

THERMAL METRIC(1)		ADS1118		UNITS
		MSOP (DGS)	QFN (RUG)	
		10 PINS	10 PINS	
θ_{JA}	Junction-to-ambient thermal resistance	186.8	245.2	°C/W
θ_{JCtop}	Junction-to-case (top) thermal resistance	51.5	69.3	
θ_{JB}	Junction-to-board thermal resistance	108.4	172.0	
ψ_{JT}	Junction-to-top characterization parameter	2.7	8.2	
ψ_{JB}	Junction-to-board characterization parameter	106.5	170.8	
θ_{JCbot}	Junction-to-case (bottom) thermal resistance	n/a	n/a	

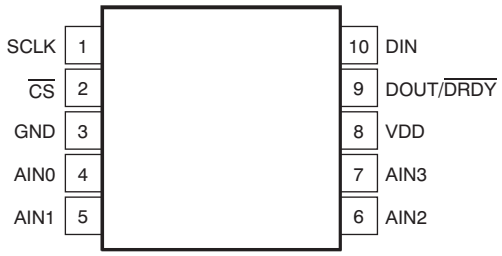
(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

PIN CONFIGURATIONS

RUG PACKAGE
QFN-10
(TOP VIEW)



DGS PACKAGE
MSOP-10
(TOP VIEW)



PIN DESCRIPTIONS

PIN #	PIN NAME	FUNCTION	DESCRIPTION
1	SCLK	Digital input	Serial clock input
2	$\overline{CS}$	Digital input	Chip select; active low
3	GND	Analog	Ground
4	AIN0	Analog input	Differential channel 1: positive input or single-ended channel 1 input
5	AIN1	Analog input	Differential channel 1: negative input or single-ended channel 2 input
6	AIN2	Analog input	Differential channel 2: positive input or single-ended channel 3 input
7	AIN3	Analog input	Differential channel 2: negative input or single-ended channel 4 input
8	VDD	Analog	Power supply: 2.0 V to 5.5 V
9	DOUT/$\overline{DRDY}$	Digital output	Serial data out combined with data ready; active low
10	DIN	Digital input	Serial data input

SPI TIMING CHARACTERISTICS

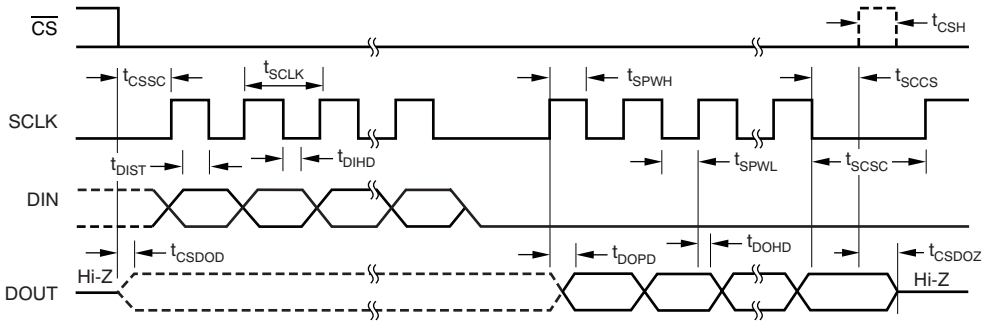


Figure 1. Serial Interface Timing

TIMING REQUIREMENTS: SERIAL INTERFACE TIMING

At T_A = –40°C to +125°C and VDD = 2.0 V to 5.5 V, unless otherwise noted.

SYMBOL	DESCRIPTION	MIN	MAX	UNIT
t_{CSSC}	$\overline{CS}$ low to first SCLK: setup time(1)	100		ns
t_{SCLK}	SCLK period	250		ns
t_{SPWH}	SCLK pulse width: high	100		ns
t_{SPWL}	SCLK pulse width: low(2)	100		ns
			28	ms
t_{DIST}	Valid DIN to SCLK falling edge: setup time	50		ns
t_{DIHD}	Valid DIN to SCLK falling edge: hold time	50		ns
t_{DOPD}	SCLK rising edge to valid new DOUT: propagation delay(3)		50	ns
t_{DOHD}	SCLK rising edge to DOUT invalid: hold time	0		ns
t_{CSDOD}	$\overline{CS}$ low to DOUT driven: propagation delay	100		ns
t_{CSDOZ}	$\overline{CS}$ high to DOUT Hi-Z: propagation delay	100		ns
t_{CSH}	$\overline{CS}$ high pulse	200		ns
t_{SCCS}	Final SCLK falling edge to $\overline{CS}$ high	100		ns

(1) $\overline{CS}$ can be tied low.
(2) Holding SCLK low longer than 28 ms resets the SPI interface.
(3) DOUT load = 20 pF || 100 kΩ to GND.

TYPICAL CHARACTERISTICS

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.

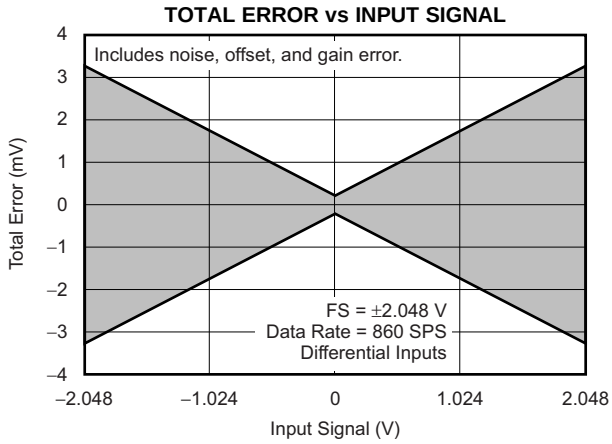


Figure 2.

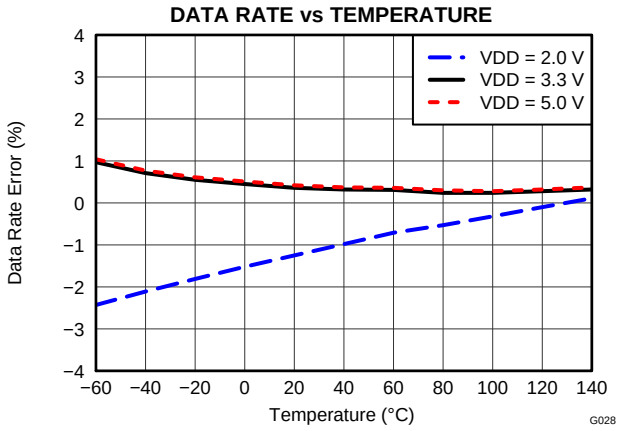


Figure 3.

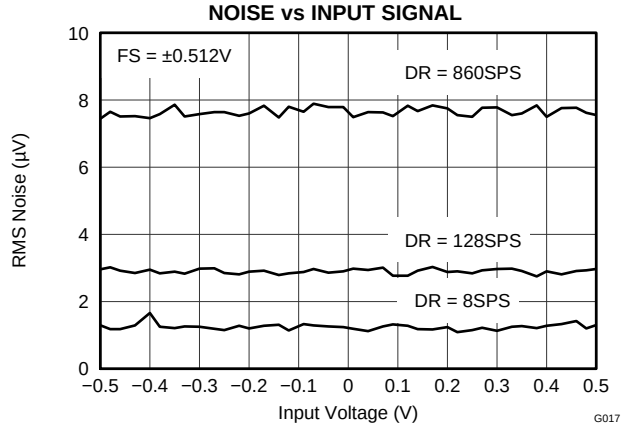


Figure 4.

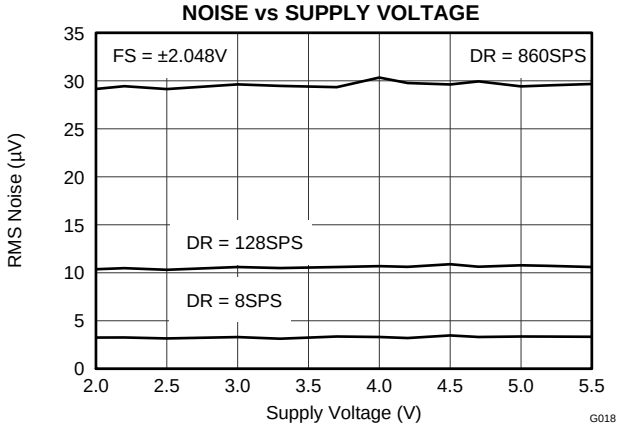


Figure 5.

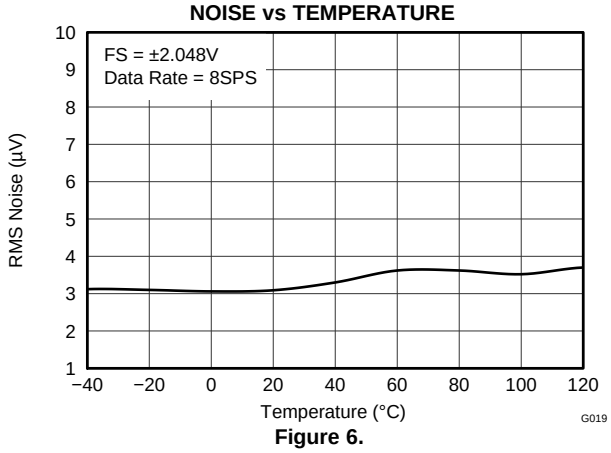


Figure 6.

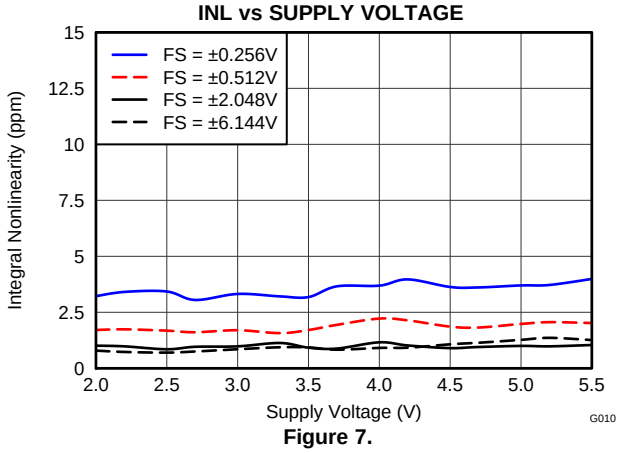
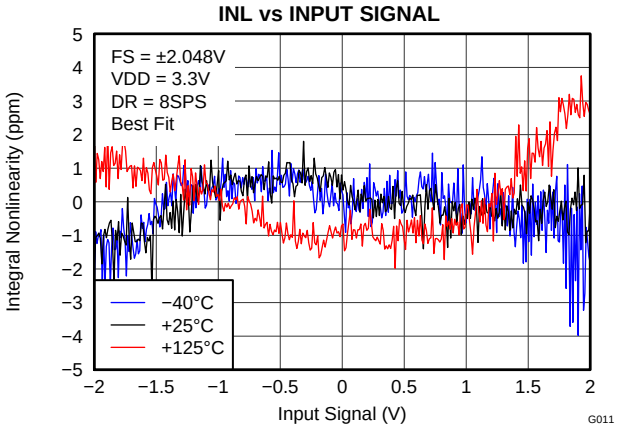


Figure 7.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.



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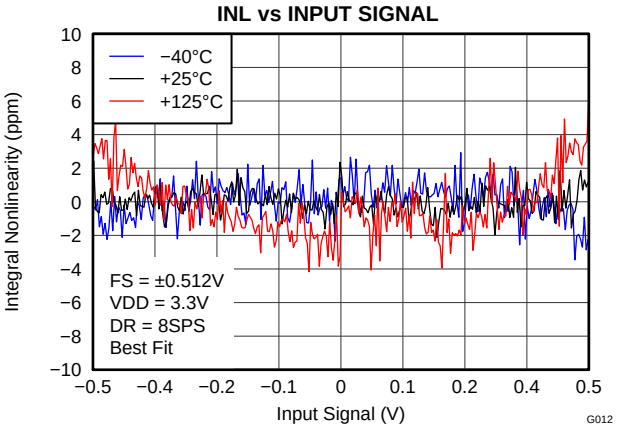

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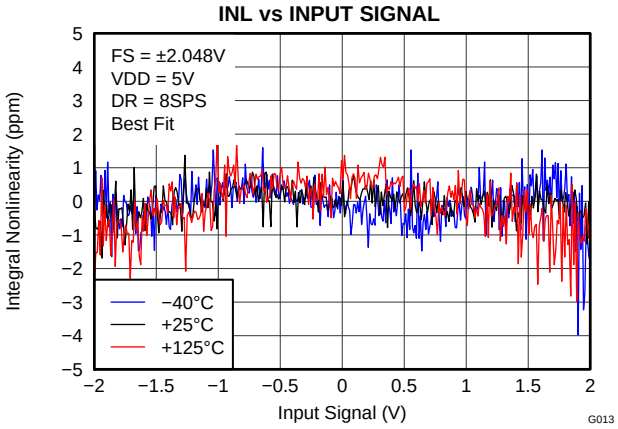

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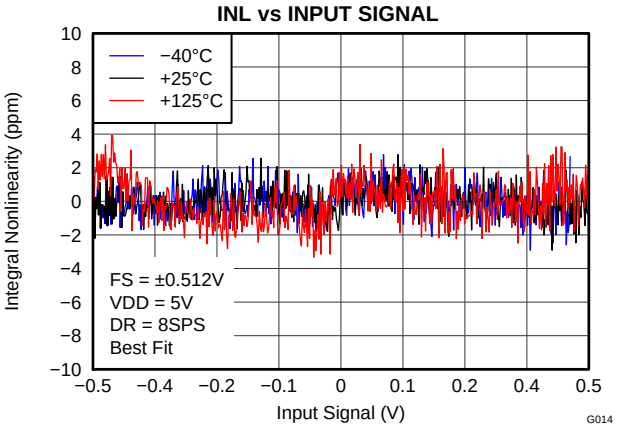

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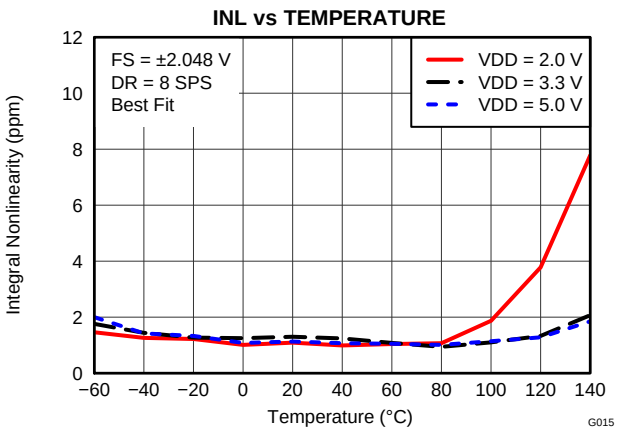


Figure 12.

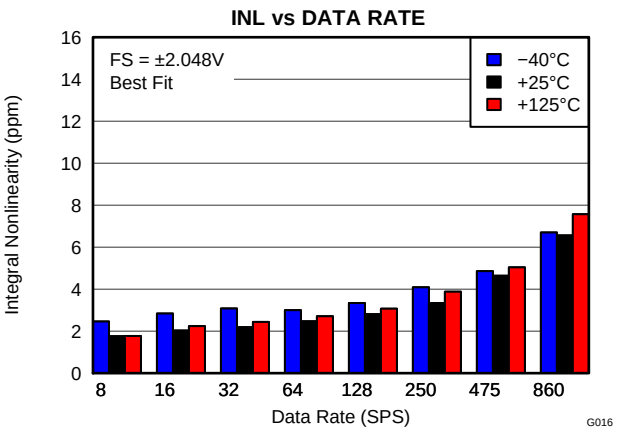


Figure 13.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.

SINGLE-ENDED OFFSET VOLTAGE vs TEMPERATURE

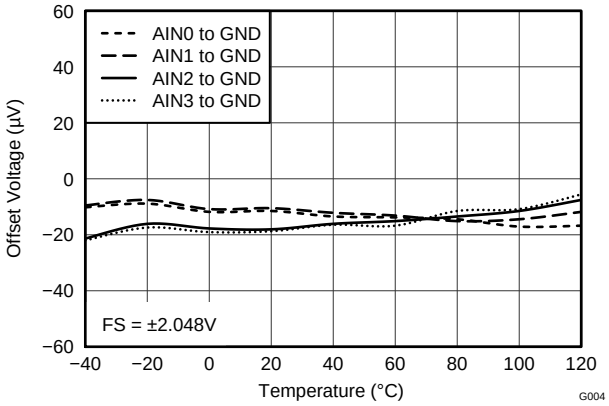


Figure 14.

SINGLE-ENDED OFFSET VOLTAGE vs SUPPLY

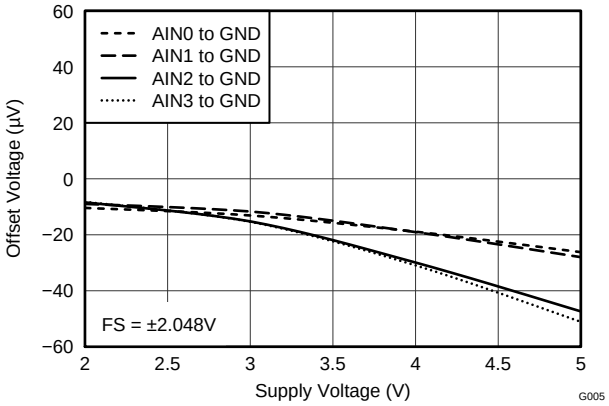


Figure 15.

DIFFERENTIAL OFFSET VOLTAGE vs TEMPERATURE

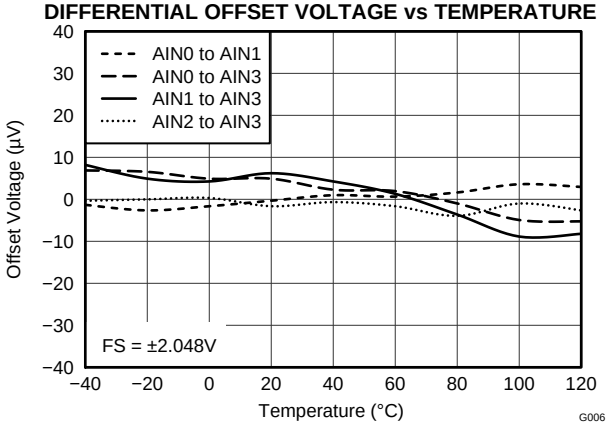


Figure 16.

DIFFERENTIAL OFFSET VOLTAGE vs SUPPLY

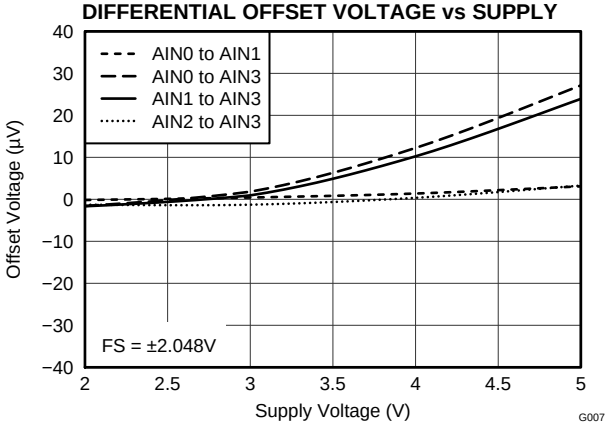


Figure 17.

OFFSET DRIFT HISTOGRAM

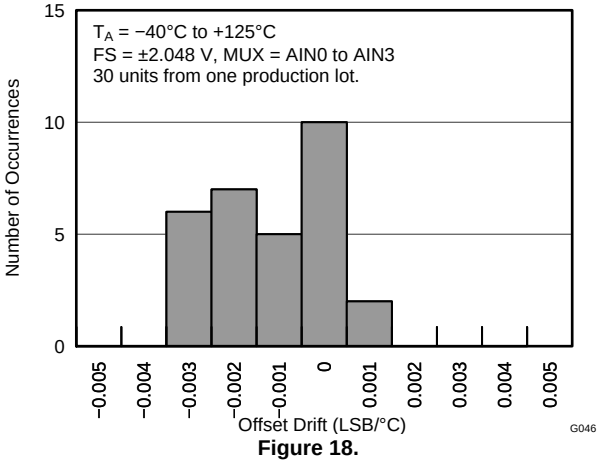


Figure 18.

OFFSET HISTOGRAM

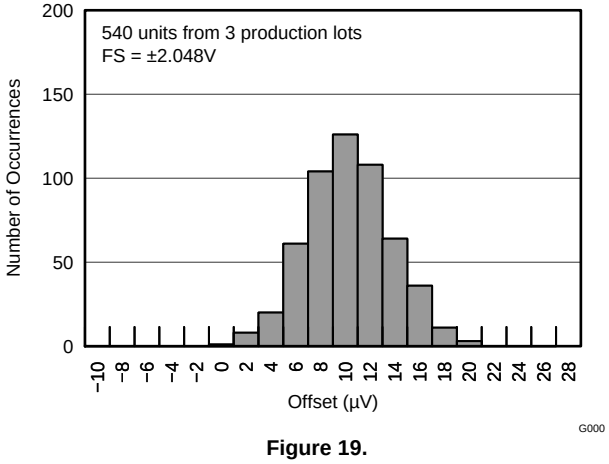


Figure 19.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.

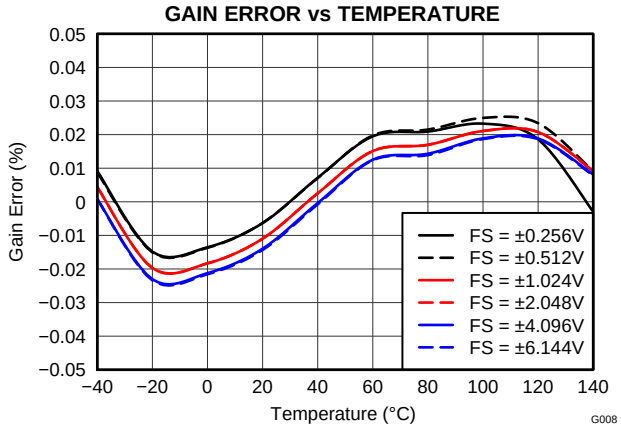


Figure 20.

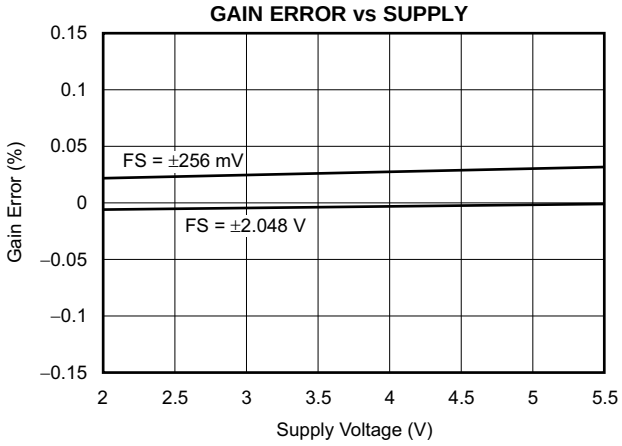
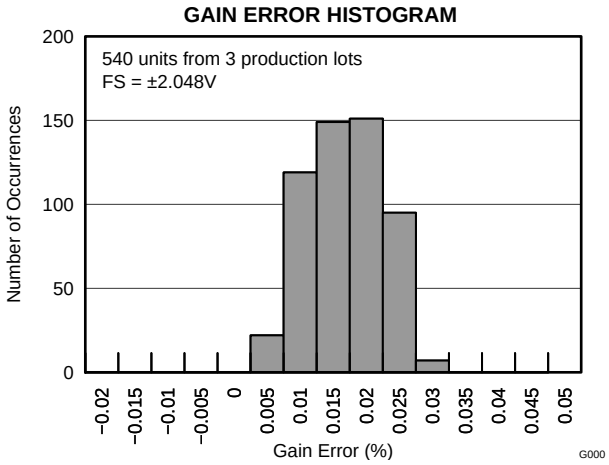


Figure 21.



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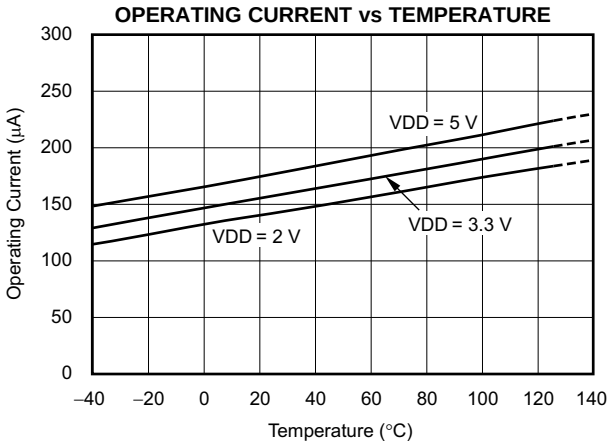


Figure 23.

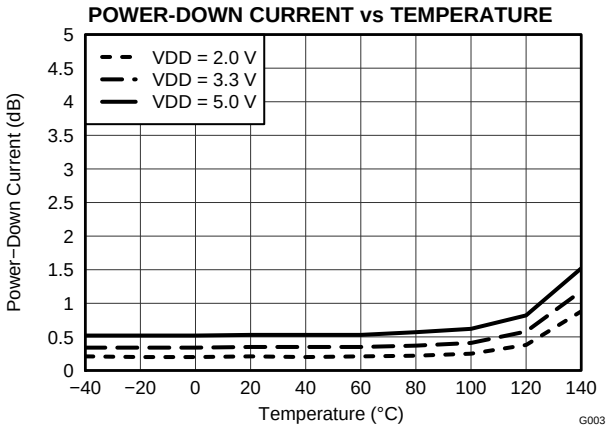


Figure 24.

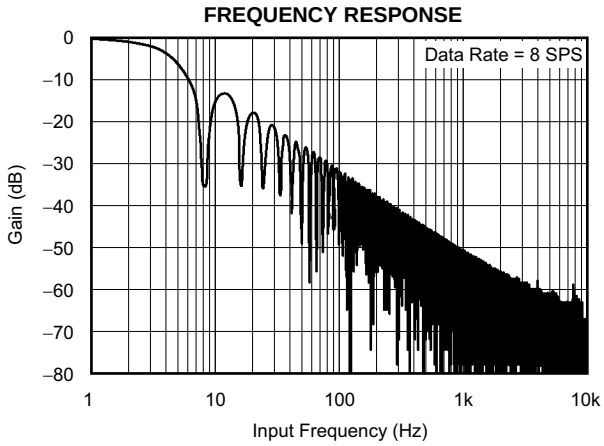


Figure 25.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.

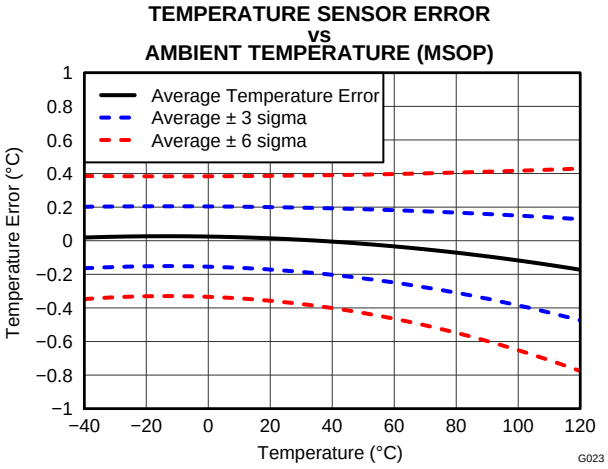


Figure 26.

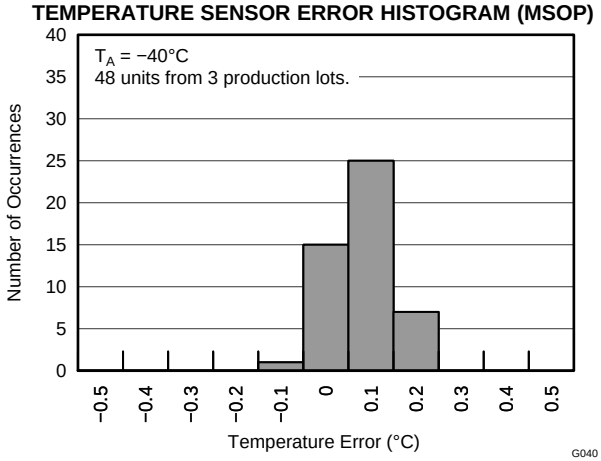


Figure 27.

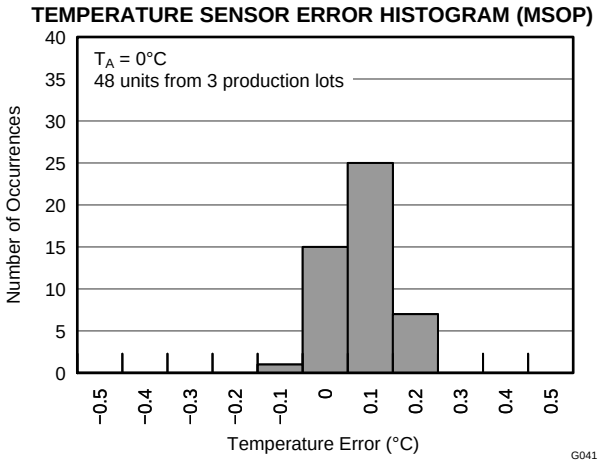


Figure 28.

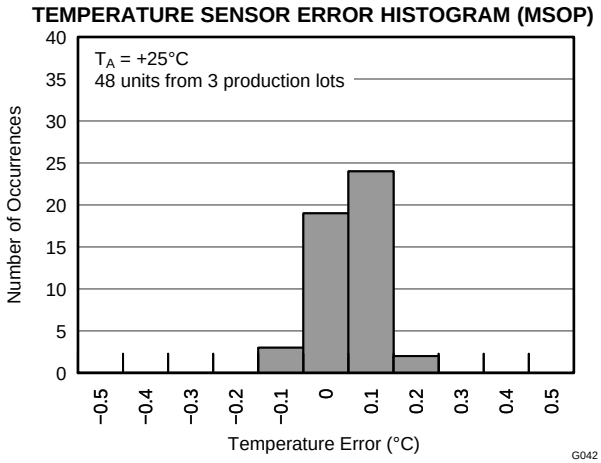


Figure 29.

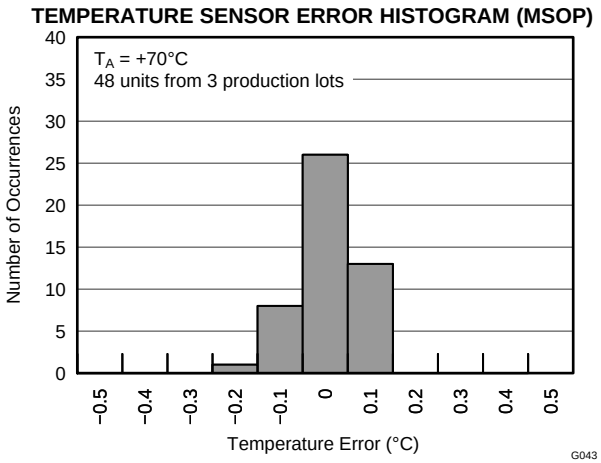


Figure 30.

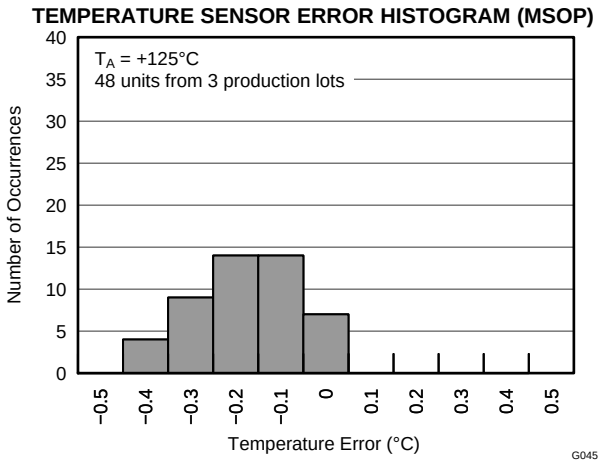


Figure 31.

TYPICAL CHARACTERISTICS (continued)

At T_A = +25°C and VDD = 3.3 V, unless otherwise noted.

TEMPERATURE SENSOR ERROR vs AMBIENT TEMPERATURE (QFN)

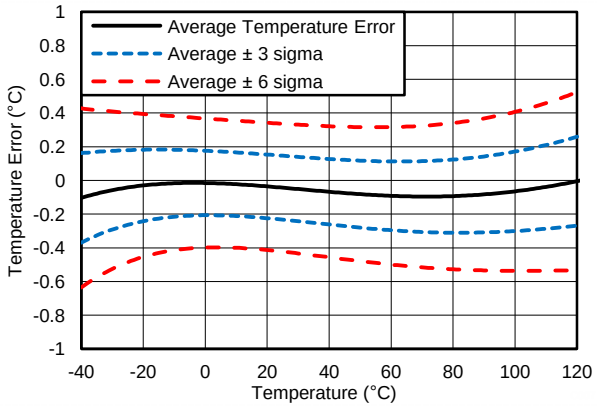


Figure 32.

TEMPERATURE SENSOR ERROR HISTOGRAM (QFN)

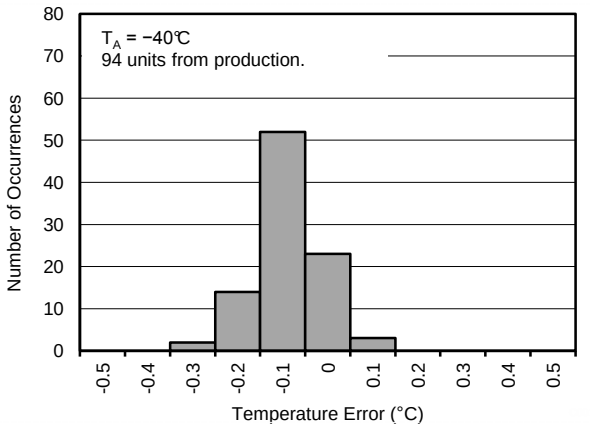


Figure 33.

TEMPERATURE SENSOR ERROR HISTOGRAM (QFN)

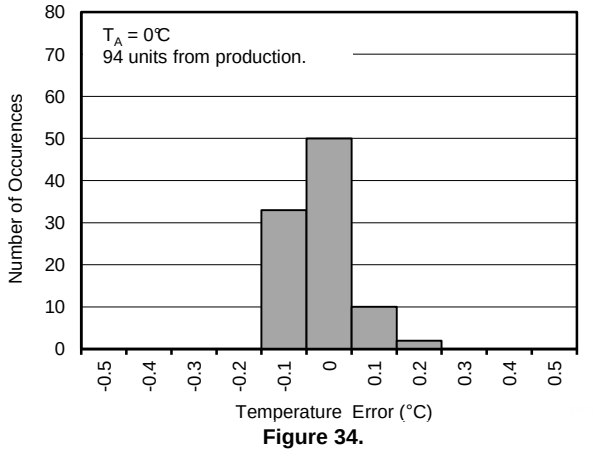


Figure 34.

TEMPERATURE SENSOR ERROR HISTOGRAM (QFN)

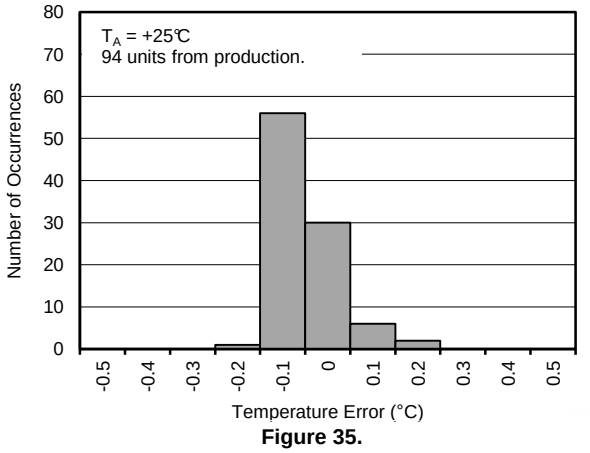


Figure 35.

TEMPERATURE SENSOR ERROR HISTOGRAM (QFN)

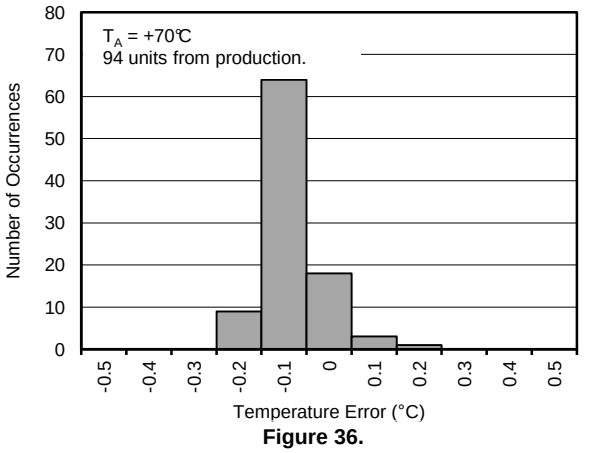


Figure 36.

TEMPERATURE SENSOR ERROR HISTOGRAM (QFN)

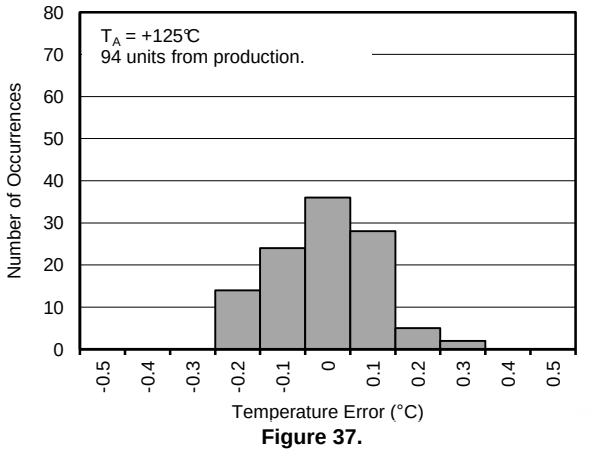


Figure 37.

OVERVIEW

The ADS1118 is a very small, low-power, 16-bit, delta-sigma (ΔΣ) analog-to-digital converter (ADC). The ADS1118 is extremely easy to configure and design into a wide variety of applications, and allows precise measurements to be obtained with very little effort. Both experienced and novice users of data converters find designing with the ADS1118 family to be intuitive and problem-free.

The ADS1118 consists of a ΔΣ ADC core with adjustable gain, an internal voltage reference, a clock oscillator, and an SPI. This device is also a highly linear and accurate temperature sensor. All of these features are intended to reduce required external circuitry and improve performance. Figure 38 shows the ADS1118 functional block diagram.

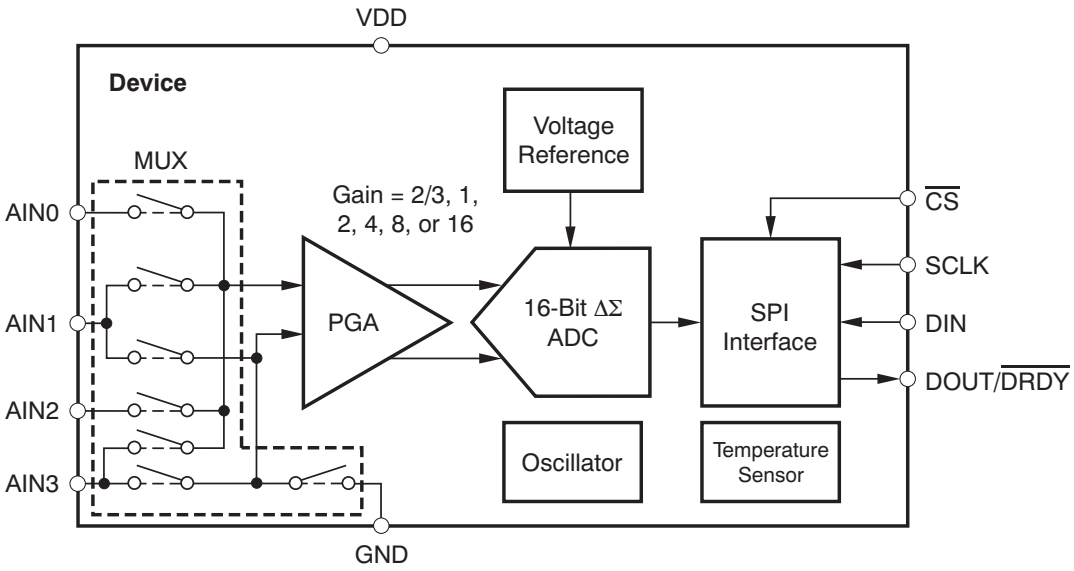


Figure 38. ADS1118 Functional Block Diagram

The ADS1118 ADC core measures a differential signal, V_{IN}, that is the difference of AIN_P and AIN_N. The converter core consists of a differential, switched-capacitor ΔΣ modulator followed by a digital filter. This architecture results in a very strong attenuation in any common-mode signals. Input signals are compared to the internal voltage reference. The digital filter receives a high-speed bitstream from the modulator and outputs a code proportional to the input voltage.

The ADS1118 has two available conversion modes: single-shot mode and continuous conversion mode. In single-shot mode, the ADC performs one conversion of the input signal upon request and stores the value to an internal conversion register. The device then enters a power-down state. This mode is intended to provide significant power savings in systems that require only periodic conversions or when there are long idle periods between conversions. In continuous conversion mode, the ADC automatically begins a conversion of the input signal as soon as the previous conversion is completed. The rate of continuous conversion is equal to the programmed data rate. Data can be read at any time and always reflect the most recently completed conversion.

MULTIPLEXER

The ADS1118 contains an input multiplexer, as shown in Figure 39. Either four single-ended or two differential signals can be measured. Additionally, AIN0, AIN1, and AIN2 may be measured differentially to AIN3. The multiplexer is configured by three bits (MUX[2:0], bits 14-12) in the Config register. When single-ended signals are measured, the negative input of the ADC is internally connected to GND by a switch within the multiplexer.

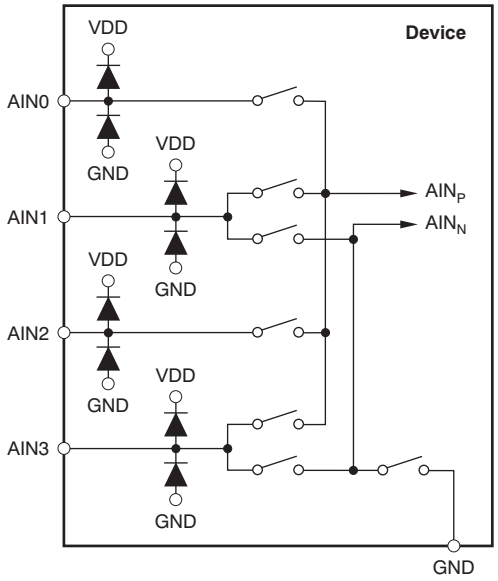


Figure 39. ADS1118 MUX

When measuring single-ended inputs, note that the negative range of the output codes is not used. These codes are intended for measuring negative differential signals, such as (AIN_P – AIN_N) < 0. Electrostatic discharge (ESD) diodes to VDD and GND protect the ADS1118 inputs. To prevent the ESD diodes from turning on, the absolute voltage on any input must stay within the range given in Equation 1:

GND – 0.3 V < AINx < VDD + 0.3 V (1)

If the voltages on the input pins can possibly violate these conditions, external Schottky clamp diodes and series resistors may be required to limit the input current to safe values (see the Absolute Maximum Ratings table). Although the analog inputs can support signals marginally above supply, under no circumstances should any analog or digital input or output be driven to greater than 5.5 V with respect to the GND pin.

Also, overdriving one unused input on the ADS1118 may affect conversions currently taking place on other input pins. If overdriving unused inputs is possible, TI recommends clamping the signal with external Schottky diodes.

ANALOG INPUTS

The ADS1118 uses a switched-capacitor input stage where capacitors are continuously charged and then discharged to measure the voltage between AIN_P and AIN_N. The capacitors used are small, and to external circuitry, the average loading appears resistive. This structure is shown in Figure 40. The resistance is set by the capacitor values and the rate at which they are switched. Figure 41 shows the on/off setting of the switches illustrated in Figure 40. During the sampling phase, switches S_1 are closed. This event charges C_{A1} to AIN_P, C_{A2} to AIN_N, and C_B to (AIN_P – AIN_N). During the discharge phase, S_1 is first opened and then S_2 is closed. Both C_{A1} and C_{A2} then discharge to approximately 0.7 V and C_B discharges to 0 V. This charging draws a very small transient current from the source driving the ADS1118 analog inputs. The average value of this current can be used to calculate the effective impedance (R_{eff}), where $R_{eff} = V_{IN} / I_{AVERAGE}$.

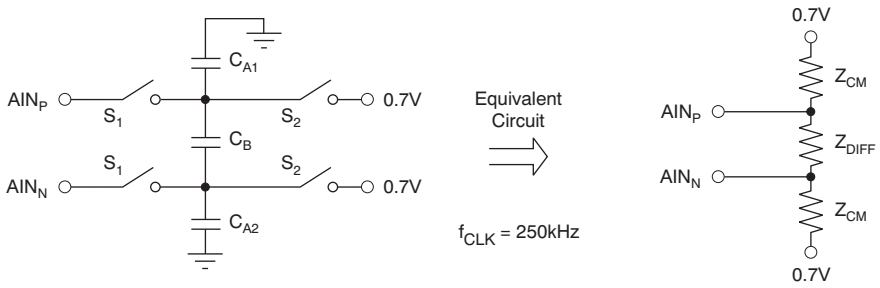


Figure 40. Simplified Analog Input Circuit

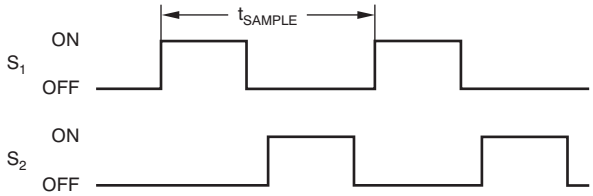


Figure 41. S_1 and S_2 Switch Timing for Figure 40

The common-mode input impedance is measured by applying a common-mode signal to the shorted AIN_P and AIN_N inputs and measuring the average current consumed by each pin. The common-mode input impedance changes depending on the PGA gain setting, but is approximately 6MΩ for the default PGA gain setting. In Figure 40, the common-mode input impedance is Z_{CM}.

The differential input impedance is measured by applying a differential signal to AIN_P and AIN_N inputs where one input is held at 0.7 V. The current that flows through the pin connected to 0.7 V is the differential current and scales with the PGA gain setting. In Figure 40, the differential input impedance is Z_{DIFF}. Table 1 describes the typical differential input impedance.

Table 1. Differential Input Impedance

FS (V)	DIFFERENTIAL INPUT IMPEDANCE
±6.144(1)(1)	22 MΩ
±4.096(1)(1)	15 MΩ
±2.048	4.9 MΩ
±1.024	2.4 MΩ
±0.512	710 kΩ
±0.256	710 kΩ

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3V be applied to this device.

The typical value of the input impedance cannot be neglected. Unless the input source has a low impedance, the ADS1118 input impedance may affect the measurement accuracy. For sources with high output impedance, buffering may be necessary. Note that active buffers introduce noise, and also introduce offset and gain errors. All of these factors should be considered in high-accuracy applications.

Because the clock oscillator frequency drifts slightly with temperature, the input impedances also drift. For many applications, this input impedance drift can be ignored, and the values given in Table 1 for typical input impedance are valid.

FULL-SCALE INPUT

A programmable gain amplifier (PGA) is implemented before the ADS1118 ΔΣ core. The PGA is configured by three bits (PGA[2:0], bits 11-9) in the Config register and can be set to gains of 2/3, 1, 2, 4, 8, and 16. Table 2 shows the corresponding full-scale (FS) ranges. However, analog input voltages may never exceed the analog input voltage limits given in the Electrical Characteristics table. In case a supply voltage of VDD greater than 4 V is used, the 2/3 PGA setting allows input voltages to extend up to the supply. Note though that in this case, or whenever the supply voltage is less than the FS range (for example, VDD = 3.3 V and PGA = 1), a full-scale ADC output code cannot be obtained. This inability means that some dynamic range is lost.

Table 2. PGA Gain and Corresponding Full-Scale Range

PGA SETTING	FS (V)
2/3	±6.144(1)
1	±4.096(1)
2	±2.048
4	±1.024
8	±0.512
16	±0.256

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

DATA FORMAT

The ADS1118 provides 16 bits of data in binary twos complement format. The positive full-scale input produces an output code of 7FFFh and the negative full-scale input produces an output code of 8000h. The output clips at these codes for signals that exceed full-scale. Table 3 summarizes the ideal output codes for different input signals. Figure 42 shows code transitions versus input voltage.

Table 3. Input Signal versus Ideal Output Code

INPUT SIGNAL, V_{IN} (AIN_P – AIN_N)	IDEAL OUTPUT CODE(1)
≥ FS (2^{15} – 1)/2^{15}	7FFFh
+FS/2^{15}	0001h
0	0
–FS/2^{15}	FFFFh
≤ –FS	8000h

(1) Excludes the effects of noise, INL, offset, and gain errors.

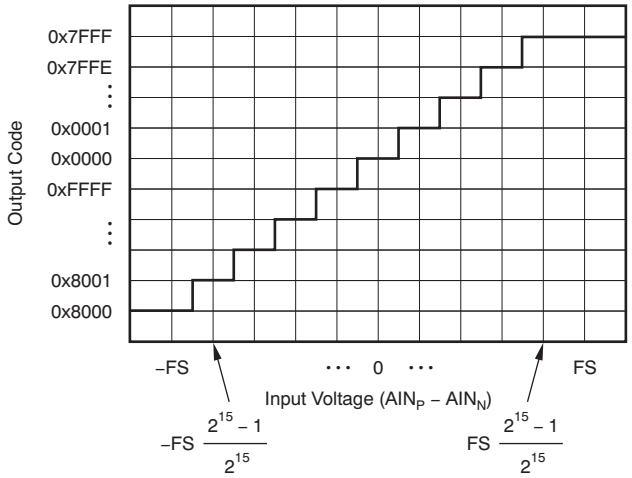


Figure 42. ADS1118 Code Transition Diagram

TEMPERATURE SENSOR

The temperature measurement mode of the ADS1118 is configured as a 14-bit result when enabled. Two bytes must be read to obtain data. The first byte is the most significant byte (MSB), followed by a second byte, the least significant byte (LSB). The first 14 bits are used to indicate temperature. That is, the 14-bit temperature result is left-justified within the 16-bit result register and the last two bits always read back as '0'. One 14-bit LSB equals 0.03125°C. Negative numbers are represented in binary twos complement format.

Table 4. 14-bit Temperature Data Format

TEMPERATURE (°C)	DIGITAL OUTPUT (BINARY)	HEX
128	01 0000 0000 0000	1000
127.96875	00 1111 1111 1111	0FFF
100	00 1100 1000 0000	0C80
80	00 1010 0000 0000	0A00
75	00 1001 0110 0000	0960
50	00 0110 0100 0000	0640
25	00 0011 0010 0000	0320
0.25	00 0000 0000 1000	0008
0	00 0000 0000 0000	0000
–0.25	11 1111 1111 1000	3FF8
–25	11 1100 1110 0000	3CE0
–55	11 1001 0010 0000	3920

Converting from Temperature to Digital Codes

For positive temperatures (for example, +50°C):

Twos complement is not performed on positive numbers. Therefore, simply convert the number to binary code in a 14-bit left justified format with the MSB = 0 to denote the positive sign.

Example: (+50°C)/(0.03125°C/count) = 1600 = 0640h = 00 0110 0100 0000

For negative temperatures (for example –25°C):

Generate the twos complement of a negative number by complementing the absolute binary number and adding 1. Then denote the negative sign with the MSB = 1.

Example:(|–25°C|)/(0.03125°C/count) = 800 = 0320h = 00 0011 0010 0000

Twos complement format: 11 1100 1101 1111 + 1 = 11 1100 1110 0000

Converting from Digital Codes to Temperature

To convert from digital codes to temperature, first check whether the MSB is a '0' or a '1'. If the MSB is a '0', simply multiply the decimal code by 0.03125°C to obtain the result. If the MSB = 1, subtract '1' from the result and complement all of the bits. Then multiply the result by –0.03125°C.

Example: ADS1118 reads back 0960h: 0960h has an MSB = 0.

(0960h) × (0.03125°C) = (2400) × (0.03125°C) = +75°C

Example: ADS1118 reads back 3CE0h: 3CE0h has an MSB = 1.

Complement the result: 3CE0h → 0320h

(0320h) × (–0.03125°C) = (800) × (–0.03125°C) = –25°C

ALIASING

As with any data converter, if the input signal contains frequencies greater than half the data rate, aliasing occurs. To prevent aliasing, the input signal must be bandlimited. However, some signals are inherently bandlimited. For example, the output of a thermocouple (which has a limited rate of change) is inherently bandlimited. Nevertheless, these signals can still contain noise and interference components. These components can fold back into the sampling band in the same way as with any other signal.

The ADS1118 digital filter provides some attenuation of high-frequency noise, but the frequency response of this 1st-order sinc filter cannot completely replace an anti-aliasing filter. For a few applications, some external filtering may be required; in such instances, a simple RC filter is adequate. When designing an input filter circuit, be sure to take into account the interaction between the filter network and the ADS1118 input impedance. TI recommends keeping the filter resistance value below 1 kΩ.

RESET AND POWER-UP

When the ADS1118 powers up, a reset is performed. As part of the reset process, the ADS1118 sets all of its bits in the Config register to the respective default settings. By default, the ADS1118 enters a power-down state at start-up. The device interface and digital blocks are active, but no data conversions are performed. The initial power-down state of the ADS1118 is intended to relieve systems with tight power-supply requirements from encountering a surge during power-up.

OPERATING MODES

The ADS1118 operates in one of two modes: continuous conversion or single-shot mode. The MODE bit in the Config register selects the respective operating mode.

Continuous Conversion Mode

In continuous conversion mode (MODE bit set to '0'), the ADS1118 continuously performs conversions. When a conversion completes, the ADS1118 places the result in the Conversion register and immediately begins another conversion.

Power-Down (Single-Shot Mode)

When the MODE bit in the Config register is set to '1', the ADS1118 enters power-down state and is configured to operate in single-shot mode. This condition is also the default state that the ADS1118 enters when power is first applied. In power-down state, the ADS1118 consumes no more than 2 μA of current. During this time, the device responds to commands, but does not perform any data conversions. The ADS1118 is held in power-down state until a '1' is written to the SS bit in the Config register. When the SS bit is asserted, the device powers up, resets the SS bit to '0', and starts a single conversion. When conversion data are ready for retrieval, the device powers down again. Writing a '1' to the SS bit while a conversion is ongoing has no effect. To exit this mode, simply write a '0' to the MODE bit in the Config register to start operating in continuous conversion mode.

DUTY CYCLING FOR LOW POWER

The noise performance of a ΔΣ ADC generally improves when lowering the output data rate because more samples of the internal modulator can be averaged to yield one conversion result. In applications where power consumption is critical, the improved noise performance at low data rates may not be required. For these applications, the ADS1118 supports duty cycling that can yield significant power savings by periodically requesting high data rate readings at an effectively lower data rate. For example, an ADS1118 in power-down state with a data rate set to 860 SPS can be operated by a microcontroller that instructs a single-shot conversion every 125 ms (8 SPS). Because a conversion at 860 SPS only requires approximately 1.2 ms, the ADS1118 enters power-down state for the remaining 123.8 ms. In this configuration, the ADS1118 consumes approximately 1/100th the power that it otherwise would consume in continuous conversion mode. The duty cycling rate is completely arbitrary and is defined by the master controller. The ADS1118 offers lower data rates that do not implement duty cycling and also offers improved noise performance if required.

SERIAL INTERFACE

The SPI-compatible serial interface consists of either four signals ($\overline{CS}$, SCLK, DIN, and DOUT/$\overline{DRDY}$), or three signals (in which case $\overline{CS}$ may be tied low). The interface is used to read conversion data, read and write registers, and control device operation.

CHIP SELECT ($\overline{CS}$)

The chip select ($\overline{CS}$) selects the ADS1118 for SPI communication. This feature is useful when multiple devices share the same serial bus. $\overline{CS}$ must remain low for the duration of the serial communication. When $\overline{CS}$ is taken high, the serial interface is reset, SCLK is ignored, and DOUT/$\overline{DRDY}$ enters a high-impedance state. In this state, DOUT/$\overline{DRDY}$ cannot provide data ready indication. In situations where multiple devices are present and DOUT/$\overline{DRDY}$ must be monitored, $\overline{CS}$ must be periodically lowered. At this point, the DOUT/$\overline{DRDY}$ pin either immediately goes high to indicate that no new data are available, or DOUT/$\overline{DRDY}$ immediately goes low to indicate that new data are present in the Conversion register and are available for transfer. New data can be transferred at any time without concern of data corruption. When a transmission starts, the current result is locked into the output shift register and does not change until the communication completes. This system avoids any possibility of data corruption. If the ADS1118 does not share the serial bus with another device, $\overline{CS}$ may be tied low.

SERIAL CLOCK (SCLK)

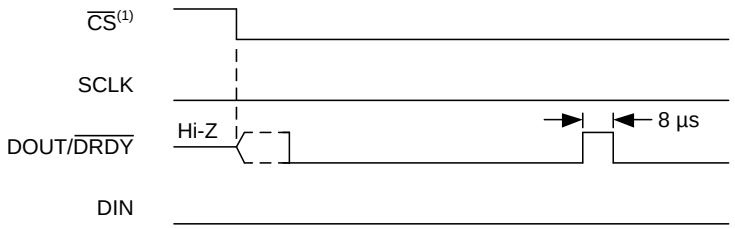
The serial clock (SCLK) features a Schmitt-triggered input and is used to clock data on the DIN and DOUT/$\overline{DRDY}$ pins into and out of the ADS1118. Even though the input has hysteresis, TI recommends keeping SCLK as clean as possible to prevent glitches from accidentally shifting the data. If SCLK is held low for 28 ms, the serial interface resets and the next SCLK pulse starts a new communication cycle. This timeout feature can be used to recover communication when a serial interface transmission is interrupted. When the serial interface is idle, hold SCLK low.

DATA INPUT (DIN)

The data input pin (DIN) is used along with SCLK to send data to the ADS1118. The device latches data on DIN on the SCLK falling edge. The ADS1118 never drives the DIN pin.

DATA OUTPUT AND DATA READY (DOUT/$\overline{DRDY}$)

The data output and data ready pin (DOUT/$\overline{DRDY}$) is used with SCLK to read conversion and register data from the ADS1118. DOUT/$\overline{DRDY}$ is also used to indicate that a conversion is completed and new data are available. This pin transitions low when new data are ready for retrieval. The data ready signal can be used to trigger a microcontroller to start reading data from the ADS1118. Data on DOUT/$\overline{DRDY}$ are shifted out on the SCLK rising edge. In continuous conversion mode, DOUT/$\overline{DRDY}$ transitions high again 8 µs before the next data ready signal (when DOUT/$\overline{DRDY}$ asserts low) if no data are retrieved from the device. This transition is shown in Figure 43. Data transmission must complete before DOUT/$\overline{DRDY}$ automatically returns high. By default, DOUT/$\overline{DRDY}$ is configured with a weak pull-up resistor if $\overline{CS}$ is high. This feature is intended to reduce the risk of DOUT/$\overline{DRDY}$ floating near midsupply and causing leakage current in the master device. Alternatively, the ADS1118 DOUT/$\overline{DRDY}$ pin can be configured in the Config register to go to a high-impedance state when $\overline{CS}$ is high. If the ADS1118 does not share the serial bus with another device, $\overline{CS}$ may be tied low.



(1) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 43. DOUT/$\overline{DRDY}$ Behavior Without Data Retrieval in Continuous Conversion Mode

REGISTERS

The ADS1118 has two registers that are accessible via the SPI port. The Conversion register contains the result of the last conversion. The Config register allows the user to change the ADS1118 operating modes and query the status of the devices.

Conversion Register

The 16-bit Conversion register contains the result of the last conversion in binary twos complement format. Following power-up, the Conversion register is cleared to '0', and remains '0' until the first conversion is completed. The register format is shown in Table 5.

Table 5. Conversion Register (Read-Only)

BIT	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
NAME	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

Config Register

The 16-bit Config register can be used to control the ADS1118 operating mode, input selection, data rate, PGA settings, and temperature sensor mode. The register format is shown in Table 6.

Table 6. Config Register (Read/Write)

15	14	13	12	11	10	9	8
SS	MUX2	MUX1	MUX0	PGA2	PGA1	PGA0	MODE
7	6	5	4	3	2	1	0
DR2	DR1	DR0	TS_MODE	PULL_UP_EN	NOP1	NOP0	NOT USED

Default = 058Bh.

Bit 15 **SS: Single-shot conversion start**

This bit is used to start a single conversion. SS can only be written when in power-down state and has no effect when a conversion is ongoing.

When writing:
0 = No effect
1 = Start a single conversion (when in power-down state)

Always reads back as '0' (default).

Bits[14:12] **MUX[2:0]: Input multiplexer configuration**

These bits configure the input multiplexer.

000 = AIN_P is AIN0 and AIN_N is AIN1 (default)	100 = AIN_P is AIN0 and AIN_N is GND
001 = AIN_P is AIN0 and AIN_N is AIN3	101 = AIN_P is AIN1 and AIN_N is GND
010 = AIN_P is AIN1 and AIN_N is AIN3	110 = AIN_P is AIN2 and AIN_N is GND
011 = AIN_P is AIN2 and AIN_N is AIN3	111 = AIN_P is AIN3 and AIN_N is GND

Bits[11:9] **PGA[2:0]: Programmable gain amplifier configuration**

These bits configure the programmable gain amplifier.

000 = FS is ±6.144 V(1)	100 = FS is ±0.512 V
001 = FS is ±4.096 V(1)	101 = FS is ±0.256 V
010 = FS is ±2.048 V (default)	110 = FS is ±0.256 V
011 = FS is ±1.024 V	111 = FS is ±0.256 V

(1) This parameter expresses the full-scale range of the ADC scaling. In no event should more than VDD + 0.3 V be applied to this device.

Bit 8 **MODE: Device operating mode**

This bit controls the ADS1118 operating mode.

0 = Continuous conversion mode
1 = Power-down and single-shot mode (default)

Bits[7:5] **DR[2:0]: Data rate**

These bits control the data rate setting.

000 = 8 SPS	100 = 128 SPS (default)
001 = 16 SPS	101 = 250 SPS
010 = 32 SPS	110 = 475 SPS
011 = 64 SPS	111 = 860 SPS

Bit 4 **TS_MODE: Temperature sensor mode**

This bit configures the ADC to convert temperature or input signals.

0 = ADC mode (default)
1 = Temperature sensor mode

Bit 3 **PULL_UP_EN: Pull-up enable**

This bit enables a weak pull-up resistor on the DOUT/$\overline{\text{DRDY}}$ pin. When enabled, a 400-kΩ resistor connects the bus line to supply. When disabled, the DOUT/$\overline{\text{DRDY}}$ pin floats.

0 = Pull-up resistor disabled on DOUT/$\overline{\text{DRDY}}$ pin
1 = Pull-up resistor enabled on DOUT/$\overline{\text{DRDY}}$ pin (default)

Bits[2:1] **NOP[1:0]: No operation**

The NOP[1:0] bits control whether data are written to the Config register or not. In order for data to be written to the Config register, the NOP[1:0] bits must be '01'. Any other value results in a NOP command. DIN can be held high or low during SCLK pulses without data being written to the Config register.

00 = Invalid data, do not update the contents of the Config register
01 = Valid data, update the Config register (default)
10 = Invalid data, do not update the contents of the Config register
11 = Invalid data, do not update the contents of the Config register

Bit 0 **Not used**

Always reads '1'

DATA RETRIEVAL

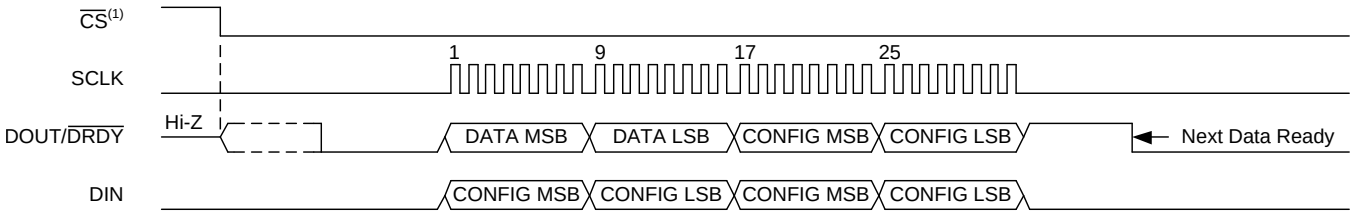
Data can be written to and read from the ADS1118 in the same manner in single-shot mode as in continuous conversion mode, without having to issue any commands. The mode in which ADS1118 operates in can be selected by the MODE bit in the Config register. Setting the MODE bit to '0' puts the device in continuous conversion mode. In this mode, the device is constantly starting new conversions even when $\overline{CS}$ is high. When configured for single-shot mode by setting the MODE bit to '1,' a new conversion only starts by writing a '1' to the SS bit.

The conversion data are always buffered, and retain the current data until replaced by new conversion data. Therefore, data can be read at any time without concern of data corruption. When DOUT/$\overline{DRDY}$ asserts low, indicating that new conversion data are ready, the conversion data are read by shifting the data out on DOUT/$\overline{DRDY}$. The MSB of the data (bit 15) on DOUT/$\overline{DRDY}$ is clocked out on the first SCLK rising edge. At the same time that the conversion result is clocked out of DOUT/$\overline{DRDY}$, new Config register data are latched on DIN on the SCLK falling edge.

The ADS1118 also offers the possibility of direct readback of the Config register settings in the same data transmission cycle. One complete data transmission cycle consists of either 32 bits (when the Config register data readback is used) or 16 bits. The short 16-bit cycle can only be used when the $\overline{CS}$ line can be controlled and is not permanently tied low.

32-Bit Data Transmission Cycle

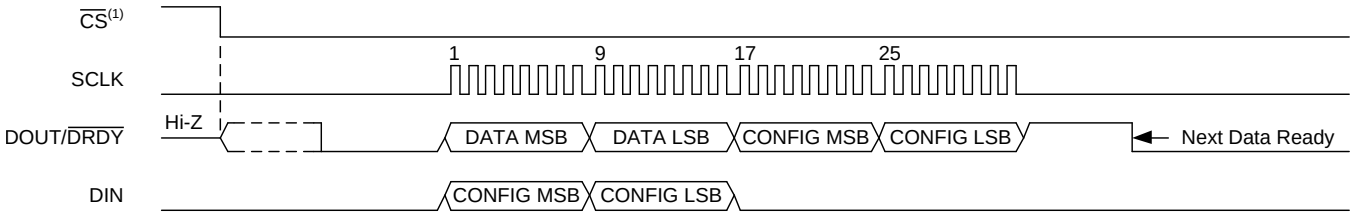
As shown in Figure 44, the data in a 32-bit data transmission cycle consists of four bytes: two bytes for the conversion result and an additional two bytes for the Config register readback. The MSB is always read first. Direct Config register data readback is only functional for the first two bytes that are written to the device in a data transmission cycle. Therefore, TI recommends writing the same Config register setting twice during one cycle.



(1) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 44. 32-Bit Data Transmission Cycle with Config Register Readback

Alternatively, DIN can be held either low or high for the second half of the data transmission cycle, as shown in Figure 45. When the ADS1118 is configured for continuous conversion mode by setting the MODE bit to '0', DIN can even be held either low or high for the entire transmission cycle as well if no changes to the device setup must be made.



(1) $\overline{CS}$ may be held low. If $\overline{CS}$ is low, DOUT/$\overline{DRDY}$ asserts low indicating new data are available.

Figure 45. 32-Bit Data Transmission Cycle: DIN Held Low

16-Bit Data Transmission Cycle

If Config register data are not required to be readback, the ADS1118 conversion data can also be clocked out in a short 16-bit data transmission cycle, as shown in Figure 46. Therefore, $\overline{CS}$ must be taken high after the 16th SCLK cycle. Taking $\overline{CS}$ high resets the SPI interface. The next time $\overline{CS}$ is taken low, data transmission starts with the currently buffered conversion result on the first SCLK rising edge. If DOUT/$\overline{DRDY}$ is low when data retrieval starts, the conversion buffer is already updated with a new result. Otherwise, if DOUT/$\overline{DRDY}$ is high, the same result from the previous data transmission cycle is read.

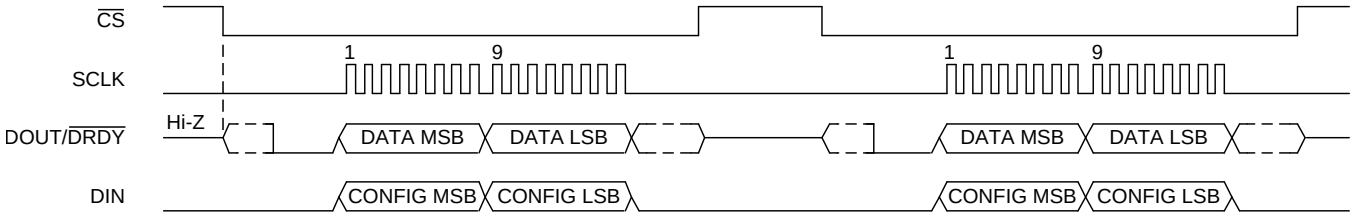


Figure 46. 16-Bit Data Transmission Cycle

APPLICATION INFORMATION

The following sections give example circuits and suggestions for using the ADS1118 in various situations.

BASIC CONNECTIONS AND LAYOUT CONSIDERATIONS

For many applications, connecting the ADS1118 is simple. A basic connection diagram for the ADS1118 is shown in Figure 47. Most microcontroller SPI peripherals can operate with the ADS1118. The interface operates in SPI mode 1 where CPOL = 0 and CPHA = 1. In SPI mode 1, SCLK idles low and data are launched or changed only on SCLK rising edges; data are latched or read by the master and slave on SCLK falling edges. Details of the SPI communication protocol employed by the ADS1118 can be found in the *SPI Timing Characteristics* section. Although not required, placing 49.9-Ω resistors in series with all of the digital pins is good practice. This resistance smooths sharp transitions, suppresses overshoot, and offers some overvoltage protection. Care must be taken to still meet all SPI timing requirements because the additional resistors interact with the bus capacitances present on the digital signal lines.

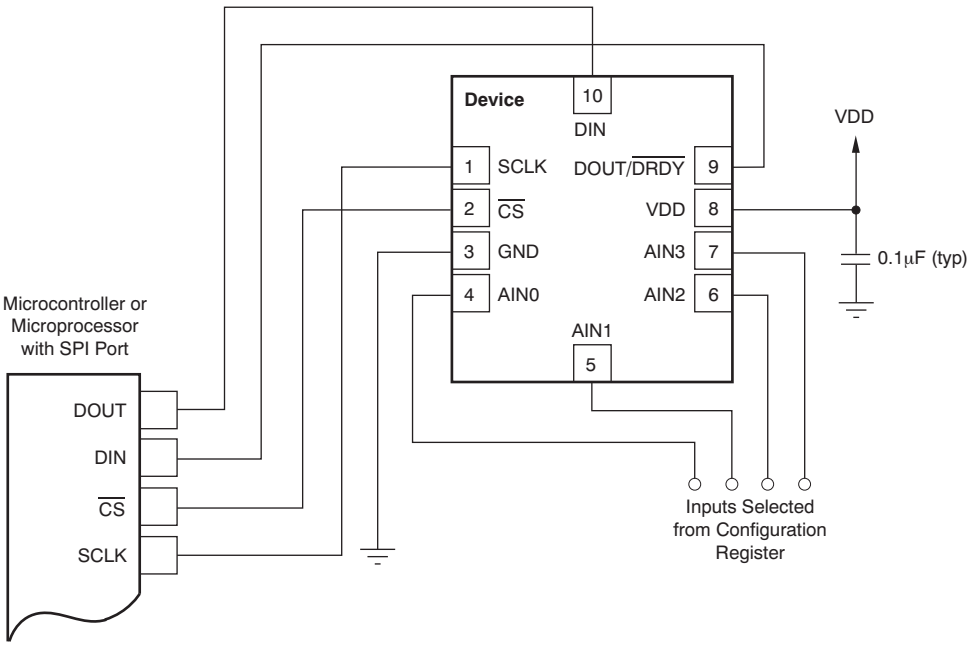


Figure 47. Typical Connections of the ADS1118

The fully-differential input of the ADS1118 is ideal for connecting to differential sources (such as thermocouples and thermistors) with a moderately low source impedance. Although the ADS1118 can read bipolar differential signals, the device cannot accept negative voltages on either input because every pin on the ADS1118 employs the use of ESD protection diodes. In the event that an input exceeds supply or drops below ground, these diodes begin to turn on. Therefore, thinking of the ADS1118 positive input as *noninverting*, and of the negative input as *inverting* may be helpful.

The 0.1-μF bypass capacitor supplies the momentary bursts of extra current required from the supply when the ADS1118 is converting. This bypass capacitor should be placed as close to the device as possible. For very sensitive systems, or systems in harsh noise environments, avoiding the use of vias for connecting the bypass capacitor may offer superior bypass and noise immunity.

TI recommends employing best design practices when laying out a printed circuit board (PCB) for both analog and digital components. This recommendation generally means that the layout should separate analog components [such as ADCs, amplifiers, references, digital-to-analog converters (DACs), and analog MUXs] from digital components [such as microcontrollers, complex programmable logic devices (CPLDs), field-programmable gate arrays (FPGAs), radio frequency (RF) transceivers, universal serial bus (USB) transceivers, and switching regulators]. An example of good component placement is shown in Figure 48. While Figure 48 provides a good example of component placement, the best placement for each application is unique to the geometries, components, and PCB fabrication capabilities being employed. That is, there is no single layout that is perfect for every design and careful consideration must always be used when designing with any analog components.

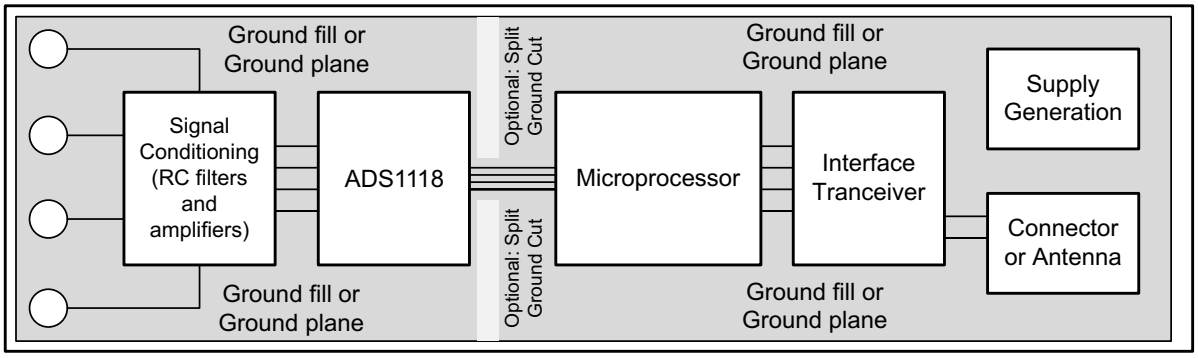
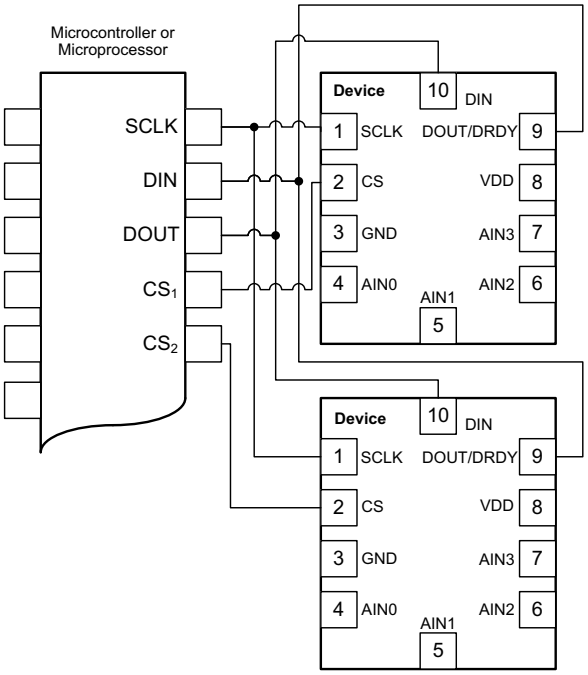


Figure 48. System Component Placement

The use of split analog and digital ground planes is not necessary for improved noise performance (although for thermal isolation this option is a worthwhile consideration). However, the use of a solid ground plane or ground fill in PCB areas with no components is essential for optimum performance. If the system being used employs a split digital and analog ground plane, TI generally recommends that the ground planes be connected together as close to the ADS1118 as possible. TI also strongly recommends that digital components, especially RF portions, be kept as far as practically possible from analog circuitry in a given system. Additionally, minimize the distance that digital control traces run through analog areas and avoid allowing these traces to be near sensitive analog components. Digital return currents usually flow through a ground path that is as close to the digital path as possible. If a solid ground connection to a plane is not available, these currents may find paths back to the source that interfere with analog performance. The implications that layout has on the temperature sensing functions are much more significant than they are for the ADC functions. Details on layout considerations for the temperature sensor can be found in the *Thermocouple Measurement with Cold Junction Compensation* section. For a detailed layout example, refer to the *ADS1118EVM User's Guide* (SBAU184).

CONNECTING MULTIPLE DEVICES

Connecting multiple ADS1118s to a single bus is simple. SCLK, DIN, and DOUT/$\overline{\text{DRDY}}$ can be safely shared by using a dedicated chip-select ($\overline{\text{CS}}$) for each SPI-enabled device. By default, when $\overline{\text{CS}}$ goes high for the ADS1118, DOUT/$\overline{\text{DRDY}}$ is pulled up to the supply of the ADS1118 by a weak 400 kΩ resistor. This feature is intended to prevent DOUT/$\overline{\text{DRDY}}$ from floating near mid-rail and causing excess current leakage on a microcontroller input. If the PULL_UP_EN bit in the Config register is set to '0', the DOUT/$\overline{\text{DRDY}}$ pin enters a 3-state mode when $\overline{\text{CS}}$ transitions high. The ADS1118 cannot issue a data ready pulse on DOUT/$\overline{\text{DRDY}}$ when $\overline{\text{CS}}$ is high. In order to evaluate when a new conversion is ready from the ADS1118 when using multiple devices, the master can periodically drop $\overline{\text{CS}}$ to the ADS1118. When $\overline{\text{CS}}$ goes low, the DOUT/$\overline{\text{DRDY}}$ pin immediately drives either high or low. If the DOUT/$\overline{\text{DRDY}}$ line drives low on a low $\overline{\text{CS}}$, new data are currently available for clocking out at any time. If the DOUT/$\overline{\text{DRDY}}$ line drives high, no new data are available and the ADS1118 returns the last read conversion result. Valid data can be retrieved from the ADS1118 at anytime without concern of data corruption. If a new conversion becomes available during data transmission, it is not available for readback until a new SPI transmission is initiated.



NOTE: Power and input connections omitted for clarity.

Figure 49. Connecting Multiple ADS1118s

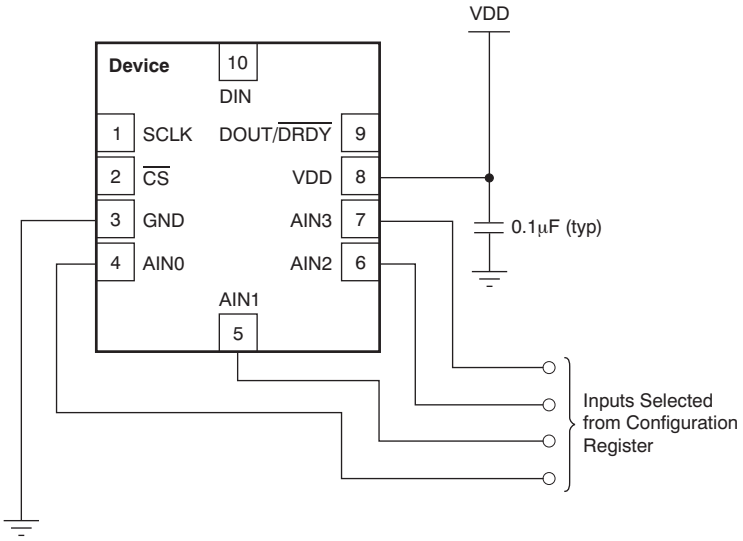
USING GPIO PORTS FOR COMMUNICATION

Most microcontrollers have programmable input/output (I/O) pins that can be set in software to act as inputs or outputs. If an SPI controller is not available, the ADS1118 can be connected to GPIO pins and the SPI bus protocol can be simulated. Using GPIO pins to generate the SPI interface only requires that the pins be configured as push or pull inputs or outputs. Furthermore, if the SCLK line is held low for more than 28 ms, the communication times out. This condition means that the GPIO ports must be capable of providing SCLK pulses with no more than 28 ms between pulses.

SINGLE-ENDED INPUTS

Although the ADS1118 has two differential inputs, the device can easily measure four single-ended signals. Figure 50 shows a single-ended connection scheme. The ADS1118 is configured for single-ended measurement by configuring the MUX to measure each channel with respect to ground. Data are then read out of one input based on the selection in the Config register. The single-ended signal can range from 0 V up to positive supply or +FS, whichever is lower. Negative voltages cannot be applied to this circuit because the ADS1118 can only accept positive voltages with respect to ground. The ADS1118 does not loose linearity within the input range.

The ADS1118 offers a differential input voltage range of ±FS. The single-ended circuit shown in Figure 50 however only uses the positive half of the ADS1118 FS input voltage range because it does not produce differentially negative inputs. Because only half of the FS range is used, one bit of resolution is lost. For optimal noise performance, TI recommends using differential configurations whenever possible. Differential configurations maximize the dynamic range of the ADC and provide strong attenuation of common-mode noise.



NOTE: Digital pin connections omitted for clarity.

Figure 50. Measuring Single-Ended Inputs

The ADS1118 is also designed to allow AIN3 to serve as a common point for measurements by adjusting the MUX configuration. AIN0, AIN1, and AIN2 can all be measured with respect to AIN3. In this configuration the ADS1118 can operate with inputs where AIN3 serves as the common point. This ability improves the usable range over the single-ended configuration because it allows negative differential voltages when GND < AIN3 < VDD; however, it does not offer attenuation of common-mode noise.

THERMOCOUPLE MEASUREMENT WITH COLD JUNCTION COMPENSATION

For an independent, two-channel thermocouple system, Figure 51 shows the basic connections. This circuit contains a simple low-pass, anti-aliasing filter, mid-point bias, and open detection. While the digital filter of the ADS1118 strongly attenuates high-frequency components of noise, TI generally recommends providing a first-order passive RC filter to further improve this performance. The differential RC filter formed by the 500 Ω resistors (R_{DIFFA} and R_{DIFFB}) and the 1 µF (C_{DIFF}) capacitor offers a cutoff frequency of approximately 320 Hz. Additional filtering can be achieved by increasing the differential capacitor or the resistance values. However, avoid increasing the filter resistance beyond 1 kΩ because the effects of the interaction with ADCs input impedance begin to affect the linearity and gain error of the ADS1118. Because of the high sampling rates supported by the ADS1118, simple post digital filtering in a microcontroller can alleviate the requirements of the analog filter and can also offer the flexibility to implement filter notches at 50 Hz or 60 Hz. Two 0.1 µF (C_{CMA} and C_{CMB}) capacitors are also added to offer attenuation of high-frequency common-mode noise components. Because mismatches in the common-mode capacitors cause differential noise, TI recommends that the differential capacitor be at least an order of magnitude (10x) larger than the common-mode capacitors.

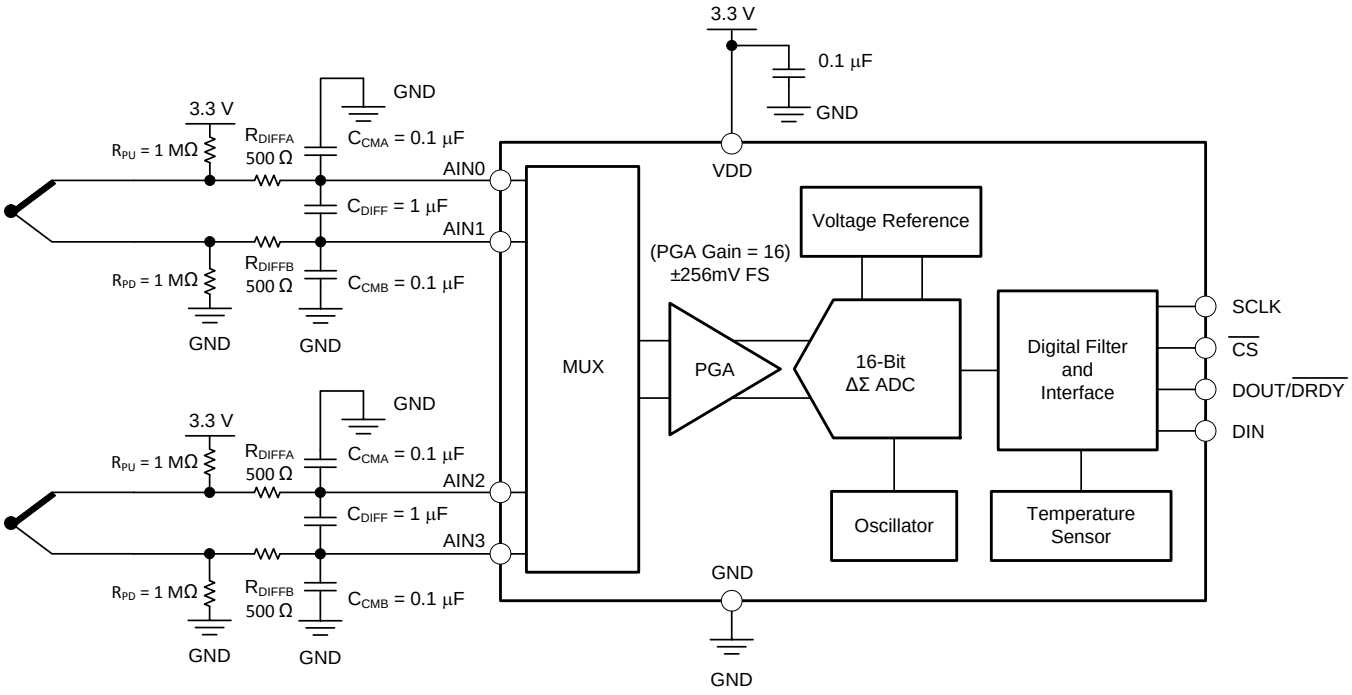


Figure 51. Two-Channel Thermocouple System

The two 1-MΩ resistors (R_{PU} and R_{PD}) serve two purposes. The first purpose is to offer a common-mode bias near midsupply. Although the ADS1118 does offer the ability to *float* the common-mode of a signal or connect any of the inputs to a common point such as ground or supply, TI generally recommends avoiding such situations. Connecting one of the inputs to a common point decreases performance by converting common-mode noise into differential signal noise that is not strongly attenuated. The second purpose of the 1-MΩ resistors is to offer a weak pull-up and pull-down for sensor open detection. In the event that a sensor is disconnected, the inputs to the ADC extend to supply and ground and yield a full-scale readout, indicating a sensor disconnection.

The procedure to actually achieve cold-junction compensation is simple and can be done in several ways. One way is to interleave readings between the thermocouple inputs and the temperature sensor. That is, acquire one on-chip temperature result for every thermocouple ADC voltage measured. If the cold junction is in a very stable environment, more periodic cold junction measurements may be sufficient. These operations yield two results for every thermocouple measurement and cold junction measurement cycle: the thermocouple voltage V_{TC} and the on-chip temperature T_{CJC}. In order to account for the cold junction, the temperature sensor within the ADS1118 must first be converted to a voltage proportional to the thermocouple currently being used yielding V_{CJC}. This conversion is generally accomplished by performing a reverse lookup on the table being used for the thermocouple voltage to temperature conversion. Then, adding the two voltages yields the thermocouple compensated voltage (V_{Actual}), where $V_{CJC} + V_{TC} = V_{Actual}$. V_{Actual} is then converted to temperature using the same lookup table as before, yielding T_{Actual}.

Thermocouple manufacturers usually supply a lookup table with their thermocouples that offer excellent accuracy for linearization of a specific type of thermocouple. The granularity on these lookup tables is generally very precise (at around 1°C for each lookup value). To save microcontroller memory and development time, an interpolation technique applied to these values can be used. By choosing 16 to 32 equally-spaced values from the manufacturer's lookup tables over a desired temperature range, using a simple linear approximation of intervals between is generally very precise.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision C (February 2013) to Revision D **Page**

- Deleted device graphic 1
- Changed bit 1 to NOP0 in Table 6 21
- Changed NOP bit description in Table 6: changes bits[2:0] to bits [2:1] and changed NOP to NOP[1:0] 22

Changes from Revision B (August 2012) to Revision C **Page**

- Updated document to current standards 1
- Changed Single-Shot Mode sub-bullet in Low Current Consumption Features bullet 1
- Changed Internal Temperature Sensor Features bullet 1
- Changed Description section 1
- Changed Product Family table 2
- Changed conditions for Electrical Characteristics table 3
- Changed Analog Input, *Full-scale input voltage range* parameter row in Electrical Characteristics table 3
- Changed footnotes 1 and 2 in Electrical Characteristics table 3
- Changed System Performance, *Integral nonlinearity* and *Gain Error* test conditions in Electrical Characteristics table 3
- Changed first two Temperature Sensor, *Temperature sensor accuracy* parameter test conditions in Electrical Characteristics table 3
- Changed Power-Supply Requirements, *Supply current* parameter test conditions in Electrical Characteristics table 4
- Added QFN (RUG) data to Thermal Information table 4
- Changed Function column name in Pin Descriptions table 5
- Changed footnote 3 of Timing Requirements: Serial Interface Timing table 6
- Updated Figure 3 7
- Updated Figure 12 8
- Changed title of Figure 14 to Figure 17 8
- Updated Figure 18 and Figure 24 9
- Changed conditions in Figure 27 to Figure 31 10
- Updated Figure 26 11
- Changed comments in Figure 33 to Figure 37 11
- Changed *Overview* section 13
- Changed *Multiplexer* section 14
- Changed *Full-Scale Input* section 16
- Added multiplication points to example equations in *Converting from Digital Codes to Temperature* section 18
- Changed *Aliasing*, *Reset and Power-Up*, *Operating Modes*, and *Duty Cycling for Low Power* sections 19
- Changed *Serial Interface*, *Chip Select*, *Serial Clock*, *Data Input*, and *Data Output and Data Ready* sections 20
- Changed *Registers* section 21
- Changed *Data Retrieval* section 23
- Changed *Application Information* section 25
- Updated Figure 51 29

Changes from Revision A (July 2011) to Revision B **Page**

- Added *(MSOP)* to titles of Figure 26 to Figure 31 11
- Added Figure 32 to Figure 37 12

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADS1118IDGSR	ACTIVE	VSSOP	DGS	10	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI	Samples
ADS1118IDGST	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	BBEI	Samples
ADS1118IRUGR	ACTIVE	X2QFN	RUG	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ	Samples
ADS1118IRUGT	ACTIVE	X2QFN	RUG	10	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 125	SDQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

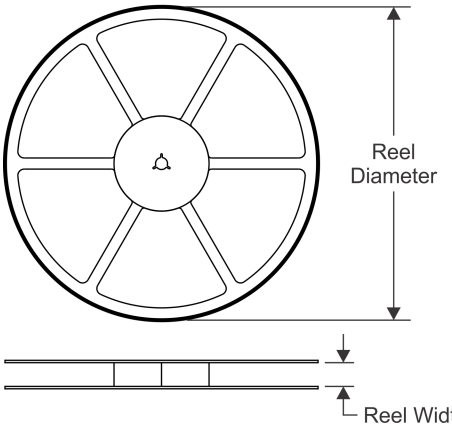
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

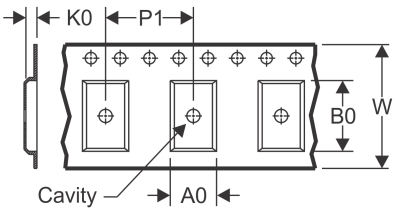
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

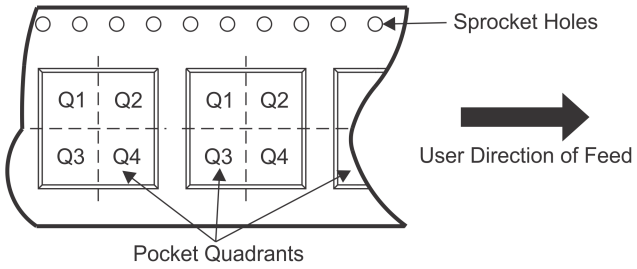


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

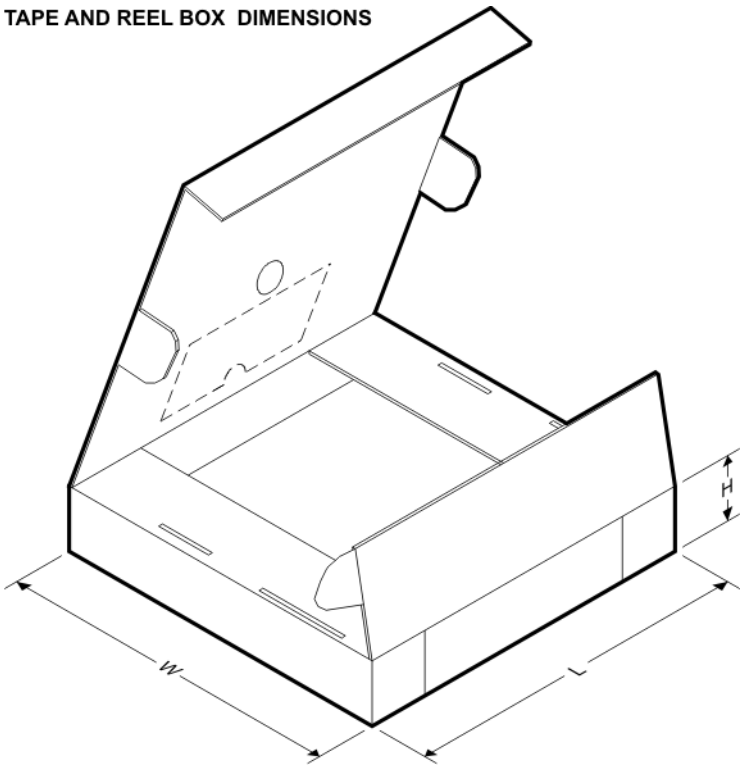
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
ADS1118IDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1118IDGST	VSSOP	DGS	10	250	180.0	12.4	5.3	3.3	1.3	8.0	12.0	Q1
ADS1118IRUGR	X2QFN	RUG	10	3000	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1
ADS1118IRUGT	X2QFN	RUG	10	250	179.0	8.4	1.75	2.25	0.65	4.0	8.0	Q1

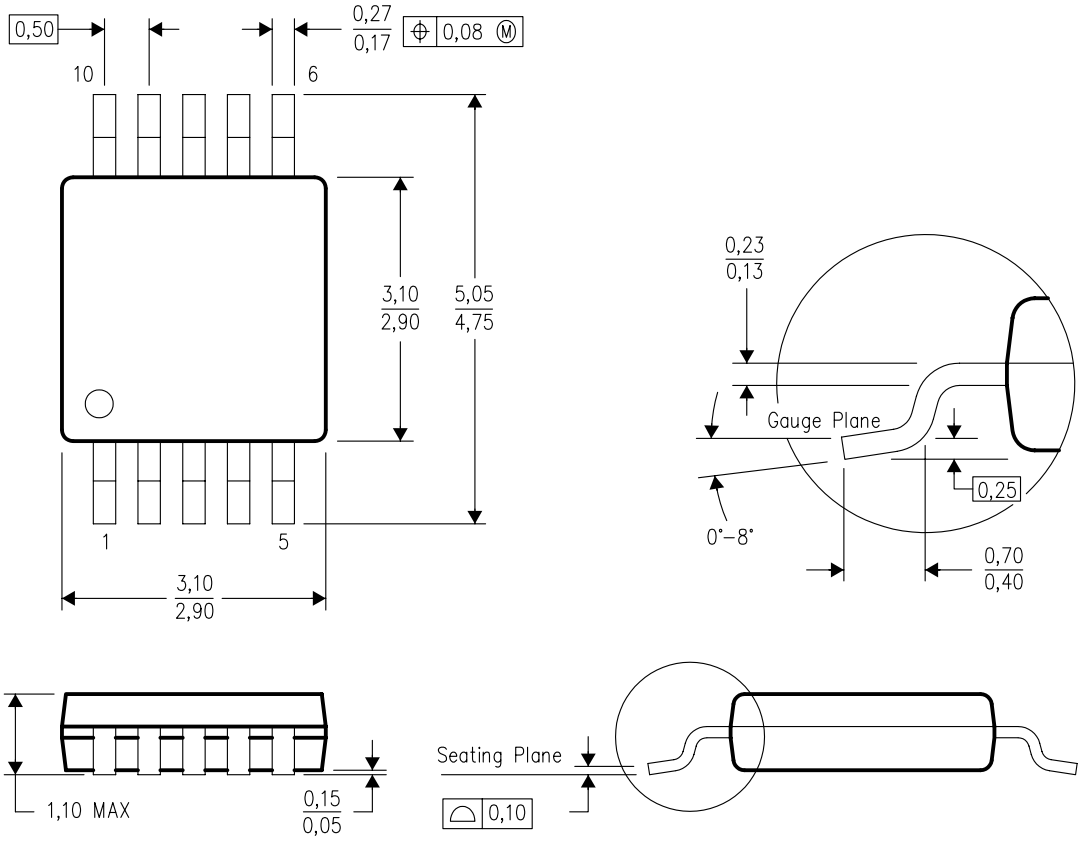
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
ADS1118IDGSR	VSSOP	DGS	10	2500	370.0	355.0	55.0
ADS1118IDGST	VSSOP	DGS	10	250	195.0	200.0	45.0
ADS1118IRUGR	X2QFN	RUG	10	3000	203.0	203.0	35.0
ADS1118IRUGT	X2QFN	RUG	10	250	203.0	203.0	35.0

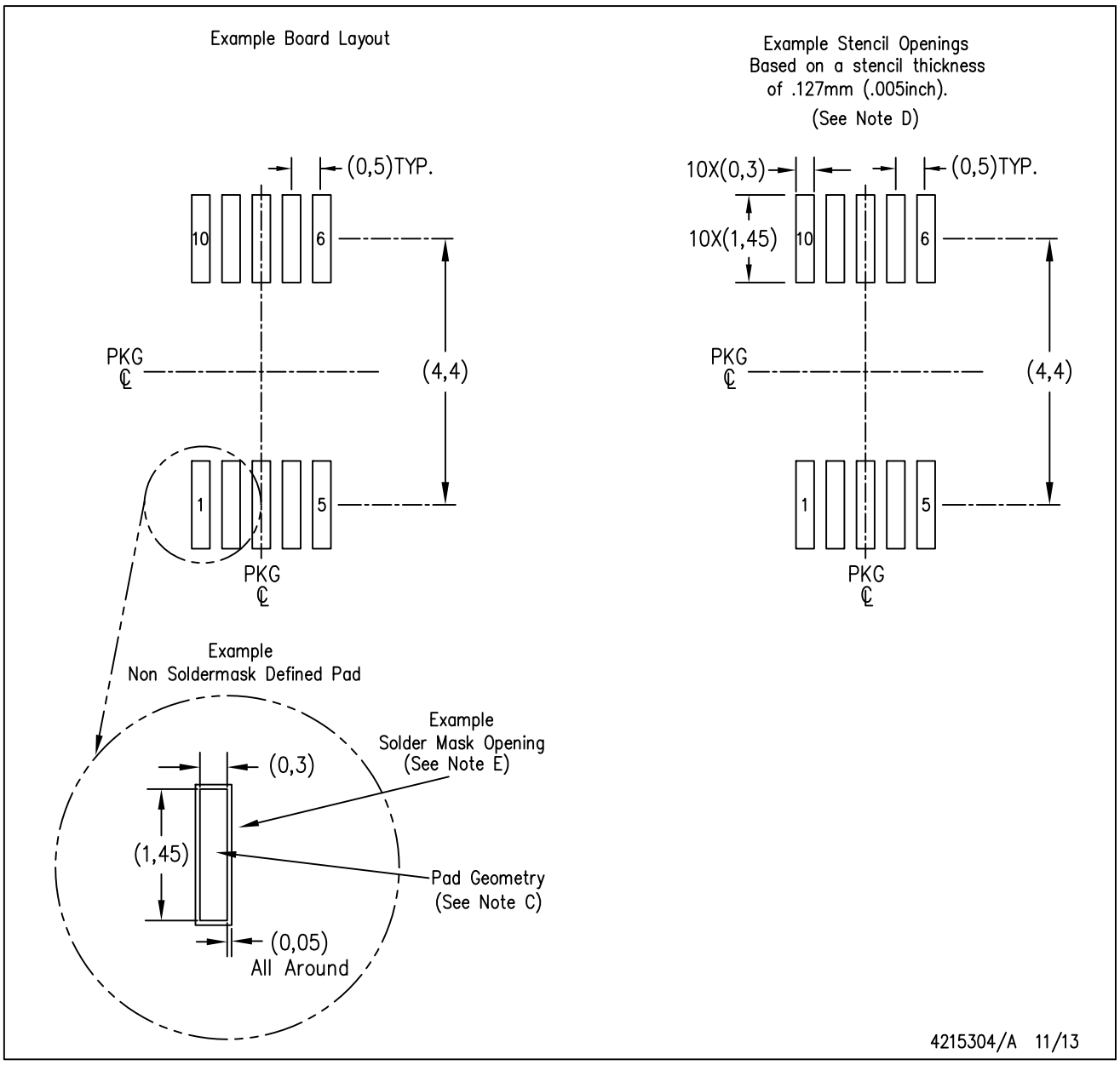
DGS (S–PDSO–G10) PLASTIC SMALL–OUTLINE PACKAGE



4073272/C 02/04

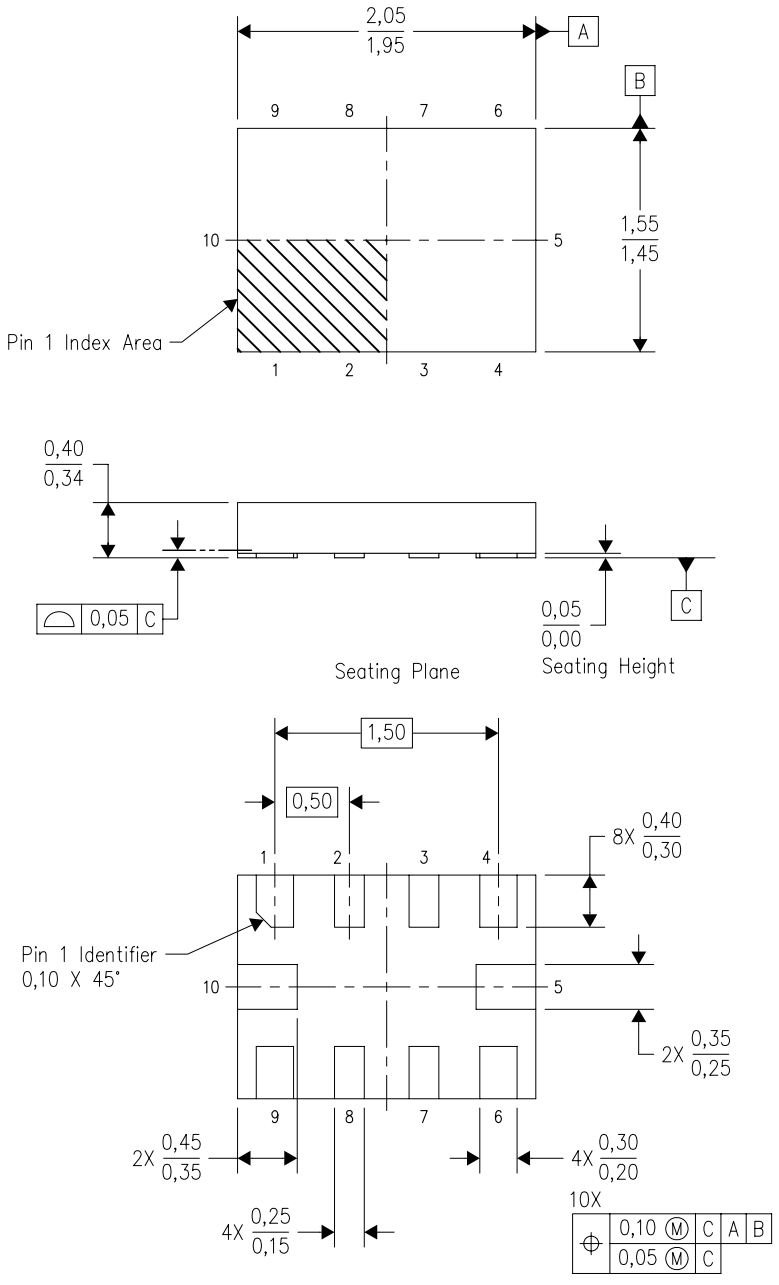
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC MO–187 variation BA.

DGS (S–PDSO–G10) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

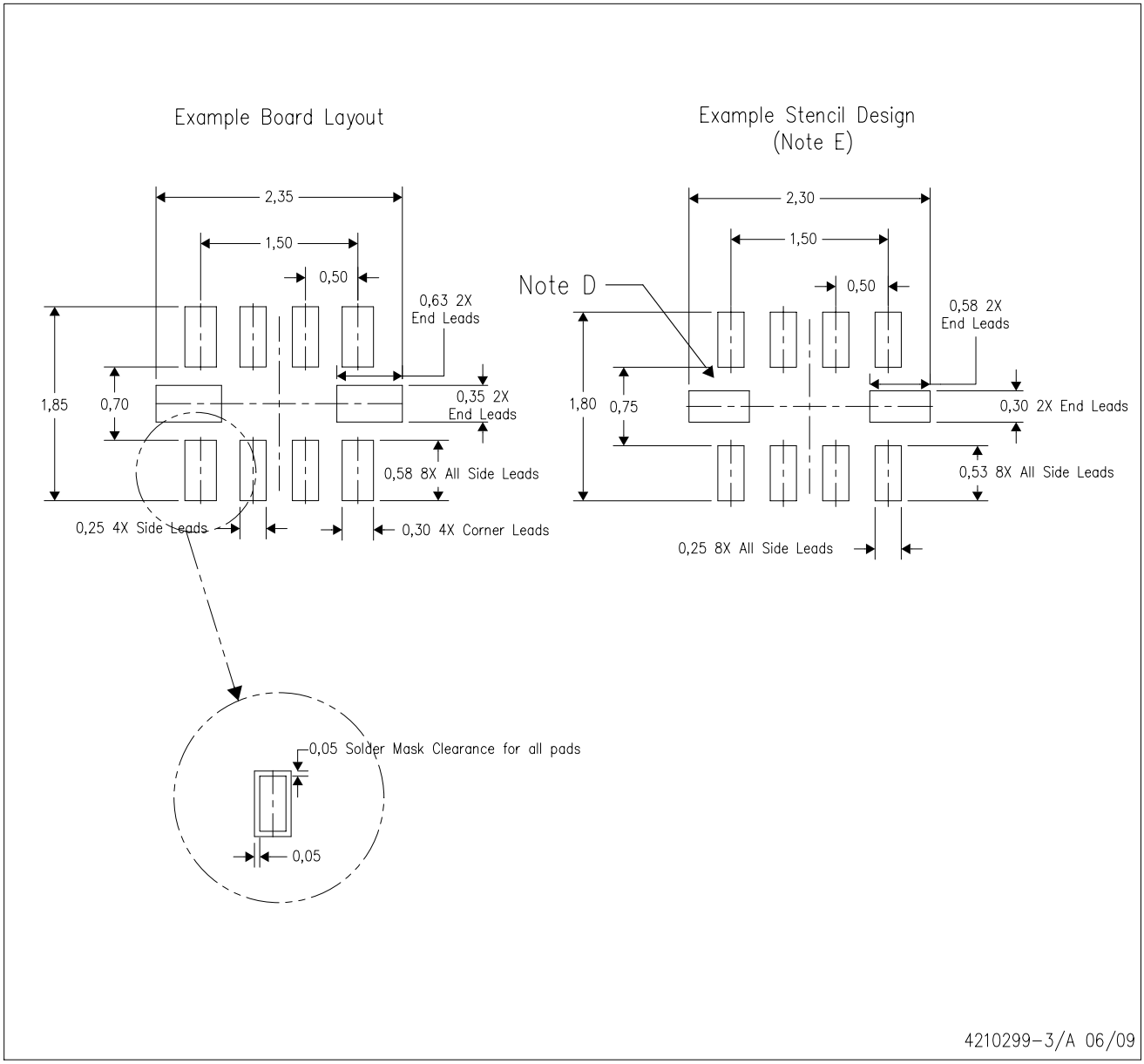
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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