

# Mandatory Task 2

MOSFET characteristics

Sebastian Hewes  
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# 1 Introduction

In this exercise the characteristics and regions of the MOSFET is investigated through mathematical approximations, simulations and measurements. The simulations are conducted in cadence and the mathematical approximations are done in MATLAB. The investigated transistors are made in a  $0.35\text{ }\mu\text{m}$  process and the mathematical approximations are done using typical values for this process.

**A MOSFET** has four different conducting regions depending on  $v_{GS}$  and  $v_{DS}$  as shown in Table 1.

Table 1: Different regions of the MOSFET

Region	NMOS		PMOS	
	$v_{GS}$	$v_{DS}$	$v_{GS}$	$v_{SD}$
Weak inversion triode region	$v_{GS} < V_{tn}$	$v_{DS} < v_{OV}$	$v_{SG} <  V_{tp} $	$v_{SD} <  v_{OV} $
Weak inversion active region	$v_{GS} < V_{tn}$	$v_{DS} > v_{OV}$	$v_{SG} <  V_{tp} $	$v_{SD} >  v_{OV} $
Strong inversion triode region	$v_{GS} > V_{tn}$	$v_{DS} < v_{OV}$	$v_{SG} >  V_{tp} $	$v_{SD} <  v_{OV} $
Strong inversion active region	$v_{GS} > V_{tn}$	$v_{DS} > v_{OV}$	$v_{SG} >  V_{tp} $	$v_{SD} >  v_{OV} $

Table 1 shows that the degree of inversion is dependent on the relationship between  $v_{GS}$  or  $v_{SG}$  and  $V_{tn(p)}$ , where  $V_{tn(p)}$  is the threshold voltage decided by the manufacturer. In this exercise  $v_S$  is grounded, so the only factor deciding the degree of inversion is  $v_G$ . Whether the transistor is in the triode or active region is determined by the relationship between  $v_{DS}$  or  $v_{SD}$  and  $v_{OV}$ , where the *overdrive voltage*,  $v_{OV}$ , is equal to  $v_{GS} - v_{tn}$  and  $v_{SG} - |V_{tp}|$  for NMOS and PMOS, respectively. If there is no drain current, the transistor is in the cut-off region. In order to best describe the relationship between the different parameters mathematically, two options present themselves:

**The transistor model introduced in Sedra and Smith, Microelectronic circuits** describes the relationship of  $i_D$ ,  $v_{DS}$  and  $v_{GS}$  for transistors in strong inversion only. In this model it is assumed that the transistor is in the cut-off region when the gate-to-source voltage  $v_{GS}$  is lower than  $V_{tn}$  or the source to gate voltage  $v_{SG}$  is higher than  $V_{tp}$  for NMOS and PMOS transistors, respectively. This, however, is not the case for real MOSFET transistors. A small drain current is present below the threshold voltage, a fact that is exploited in modern low-powered CMOS designs. The mathematical relationship between  $i_D$ ,  $v_{DS}$  and  $v_{GS}$  described in Sedra and Smith

microelectronic circuits also encounters problems describing a continuous transformation between the triode and active region as the regions are described with different mathematical equations. The relationship between  $i_D$ ,  $v_D$ ,  $v_S$  and  $v_G$  for an NMOS transistor is as shown in eq. 1 in the triode region and eq. 2 in the active region.

$$i_D = k_n(v_{OV} - \frac{1}{2}v_{DS})v_{DS} \quad (1)$$

$$i_D = \frac{1}{2}k_n v_{OV}^2 \quad (2)$$

Similar equations for the PMOS transistor is shown in eq. 3 for the triode region and eq. 4 for the active region.

$$i_D = k_p(|v_{OV}| - \frac{1}{2}v_{SD})v_{SD} \quad (3)$$

$$i_D = \frac{1}{2}k_p v_{OV}^2 \quad (4)$$

$k_{n(p)} = (\mu_{n(p)}C_{OX})(\frac{W}{L})$  is the MOSFET transconductance parameter, where  $\mu_{n(p)}$  is the mobility of free electrons at the surface of the channel,  $C_{OX}$  is the oxide capacitance, W is the width of the channel and L is the length of the channel.

**The EKV model** described in "Analog VLSI Signal Processing: Why, Where and How?"(1994) by Eric. A. Vittoz introduces a continuous mathematical approximation of  $i_D$  for all values of  $v_{GS}$  and  $v_{DS}$  unifying all four regions of operation in a simple set of equations. The equations are shown in eq. 5 and 6

$$i_{F(R)} = I_S \ln^2 \left[ 1 + \exp \left( \frac{v_G - V_{T0} - nv_{S(D)}}{2nV_T} \right) \right] \quad (5)$$

$$i_D = i_F - i_R \quad (6)$$

Where  $I_S = 2nk_{n(p)}V_T^2$  is the specific current of the transistor, n is the slope factor and  $V_{T0}$  is  $V_{tn(p)}$ . The equation reduces to the equations in Sedra and Smith for the triode and active region when in strong inversion.

## 2 Prelab

In order to be able to compare the measurements conducted on the CMOS transistor with a mathematical approximation, a MATLAB script was created to plot the relationship between  $i_D$ ,  $v_{DS}$  and  $v_{GS}$ . The EKV model was used both for the simplicity of using the same equations regardless of regions and to be able to calculate both weak and strong inversion regions.

### Parameters used in the approximations:

- $V_S = V_B = 0 \text{ V}$
- $n = 1$
- $V_{tn} = 0.57 \text{ V}$
- $V_{tp} = -0.71 \text{ V}$
- $\lambda L = 0.16 \frac{\mu\text{m}}{\text{V}}$  (for both P- and N-type)
- $W = 1 \mu\text{m}$
- $L = 1 \mu\text{m}$
- $k_n = 190 \frac{\mu\text{A}}{\text{V}^2}$
- $k_p = 55 \frac{\mu\text{A}}{\text{V}^2}$
- $V_T = 26 \text{ mV}$
- $V_{dd} = 3.3 \text{ V}$

All the approximations are done for the NMOS transistor.

### Task 1



1.  $i_D$  was plotted as a function of  $v_{GS}$  for a NMOS transistor in the active region. Table 1 specifies the conditions required to be in the active region. Note that the active region includes both strong and weak inversion. The common condition for both cases is that  $v_{DS} > v_{OV}$ . To achieve this,  $v_D$  was set to 3.3 V ( $V_{dd}$ ). Since  $v_{OV} = v_{GS} - V_{tn}$ ,  $v_{OV}$  is always going to be lower than  $v_{DS}$  when  $v_{GS}$  is swept from 0 →  $V_{dd}$

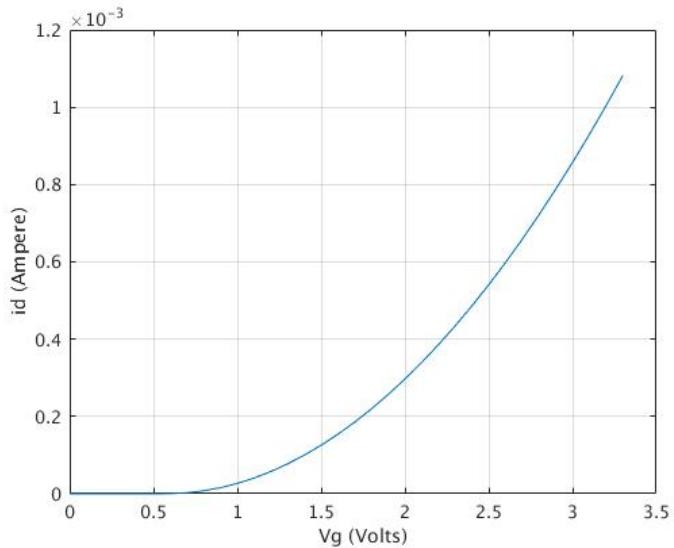


Figure 1: Relationship between  $i_D$  and  $v_{GS}$  in active region with linear axis

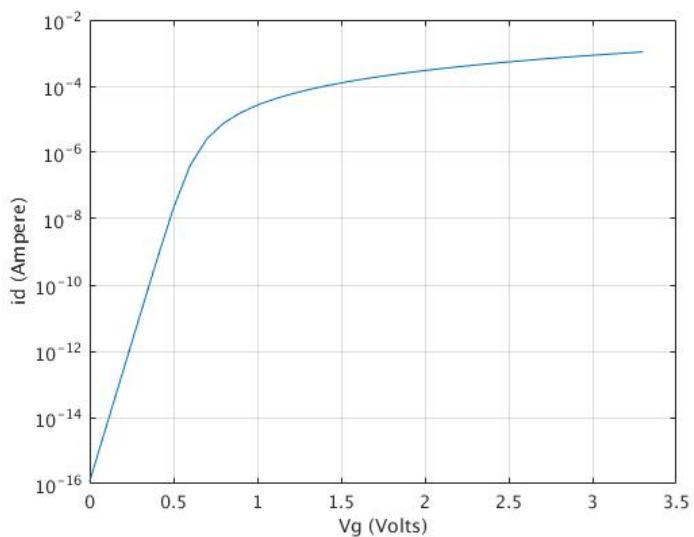


Figure 2: Relationship between  $i_D$  and  $v_{GS}$  in active region with logarithmic y axis

The curve is in the active region, since there is no value for  $v_{GS}$  that makes the overdrive voltage,  $V_{OV}$  higher than the drain to source voltage  $V_{GS}$ .

**2**  $i_D$  was also plotted as a function of  $v_{GS}$  in the triode region. From Table 1, the common condition for both weak and strong inversion in the triode region is that  $v_{DS} < v_{OV}$ .  $v_{OV}$  in the strong inversion is defined as  $v_{GS} - V_{tn}$ . In weak inversion, however,  $v_{OV}$  is approximated to be around  $4V_T = 104$  mV. With this in mind,  $v_{DS}$  was set to 50 mV. This value ensures that the transistor operates in the triode region for the whole weak inversion region, since  $v_{DS} < v_{OV}$ . However, a problem arises when  $v_{GS} = V_{tn}$ . Since the MOSFET transistor is symmetrical, the definition of the drain and the source is only based on the voltage difference between the two terminals. Hence  $v_{DS} = 0$  V does not make physical sense, since the drain and source are not defined when the voltage difference between them is 0 V. The terminal with the highest potential of the two is labeled the drain and vice versa. From this, it should also be obvious that  $v_{DS}$  cannot be negative. For  $v_{GS}$  values between  $v_{GS} = V_{tn}$  to  $v_{GS} = V_{tn} + 50$  mV the curve is actually in the active region, indicated by the red lines on the plots.

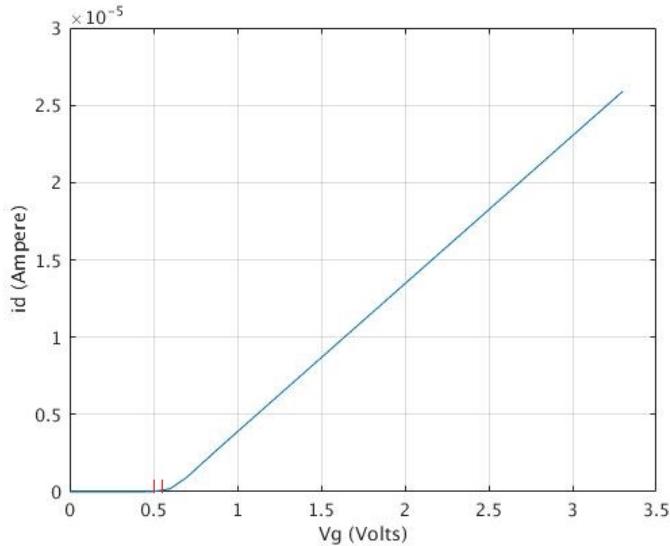


Figure 3: Relationship between  $i_D$  and  $v_{GS}$  in the triode region with linear axis

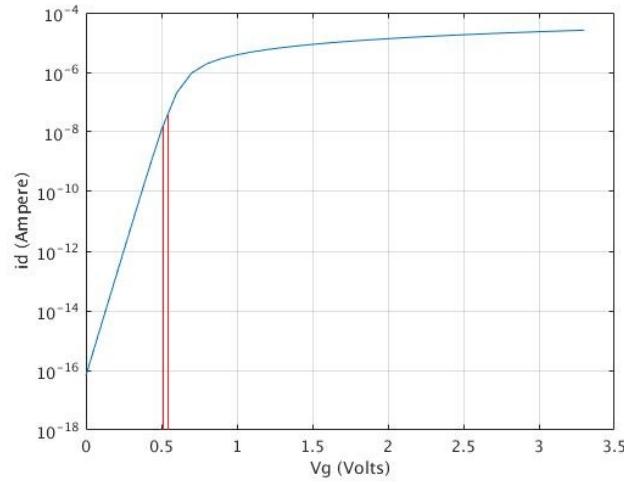


Figure 4: Relationship between  $i_D$  and  $v_{GS}$  in the triode region with logarithmic y axis

**3**  $i_D$  was plotted as a function of  $v_{DS}$  in strong inversion. To ensure that the transistor was in strong inversion  $v_{GS}$  had to be kept above the threshold voltage,  $V_{tn}$ . To compare the influence of  $V_G$  the gate voltage was set to values from  $0.8 \text{ V} \rightarrow 2.6 \text{ V}$  with increments of  $0.2 \text{ V}$  and  $v_{DS}$  was swept from  $0 \rightarrow V_{dd}$  for each  $V_G$  value.

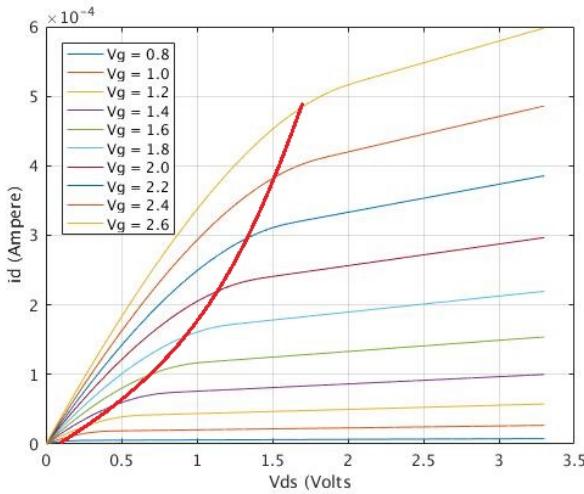


Figure 5: Relationship between  $i_D$  and  $v_{DS}$  in strong inversion with different gate voltages

The red line illustrate the approximately quadratic behaviour of the knee points. The knee point is allocated where the transistor transitions from the triode mode of operation to the active region.

**4**  $i_D$  was also plotted as a function of  $v_{DS}$  in weak inversion. To ensure that the transistor was in weak inversion  $v_{GS}$  had to be kept below the threshold voltage,  $V_{tn}$ . To compare the influence of  $V_G$  the gate voltage was set to values from  $0.1 \text{ V} \rightarrow 0.5 \text{ V}$  with increments of  $0.1 \text{ V}$  and  $v_{DS}$  was swept from  $0 \rightarrow V_{dd}$  for each  $V_G$  value. Because the currents are very small in weak inversion a logarithmic y-axis was used to demonstrate the different currents.

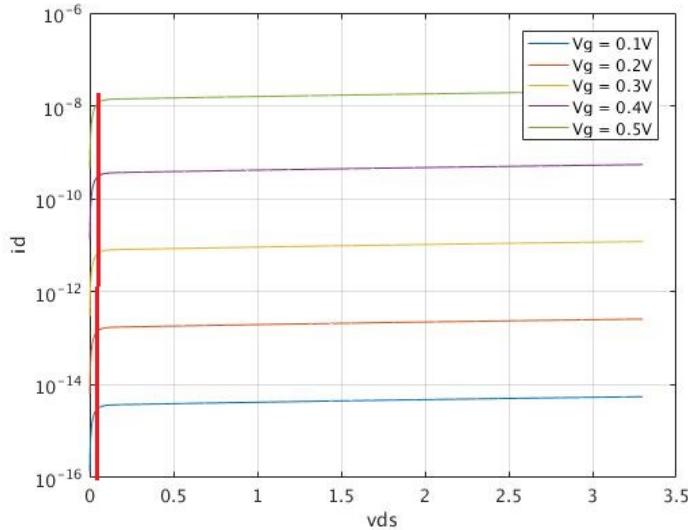


Figure 6: Relationship between  $i_D$  and  $v_{DS}$  in weak inversion with different gate voltages

As indicated by the red line in the plot, the behavior of the knee voltage is approximately constant in weak inversion. The overdrive voltage,  $v_{OV}$ , is no longer defined by the voltage difference between the gate and the source but is constant at around  $4V_T$ .

### 3 Simulation



To compare the mathematical approximations with the simulations in cadence, the same plots were created by importing the simulation data to MATLAB.

#### 3.1 Simulation results

- 1 A circuit simulating the NMOS transistor in the active region with  $v_{GS}$  sweeping from  $0 \text{ V} \rightarrow 3.3 \text{ V}$  was created. The schematic is shown in Figure 7, with it's respective plots shown in Figure 8 and Figure 9.

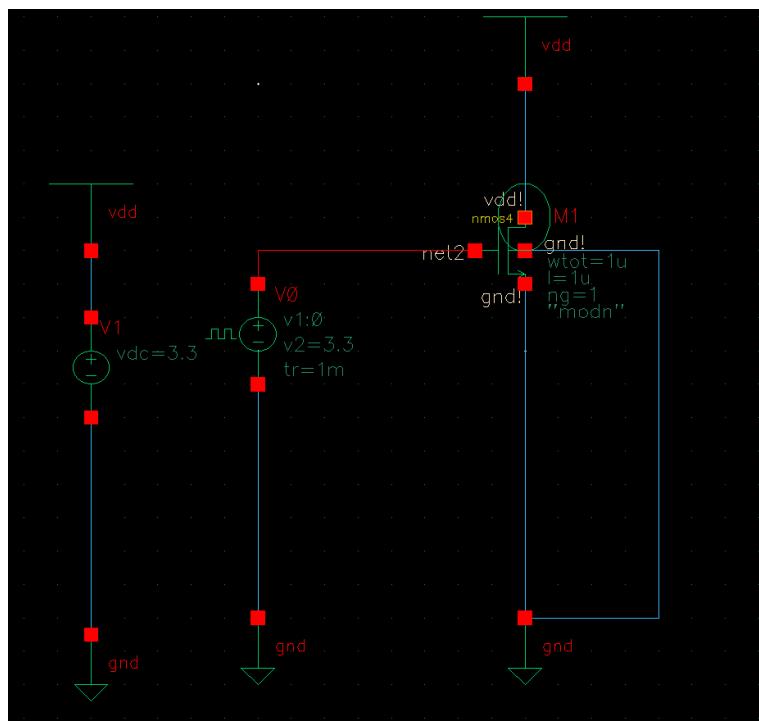


Figure 7: Cadence schematic of the circuit equivalent to the approximation in Task 1.1 (active region)

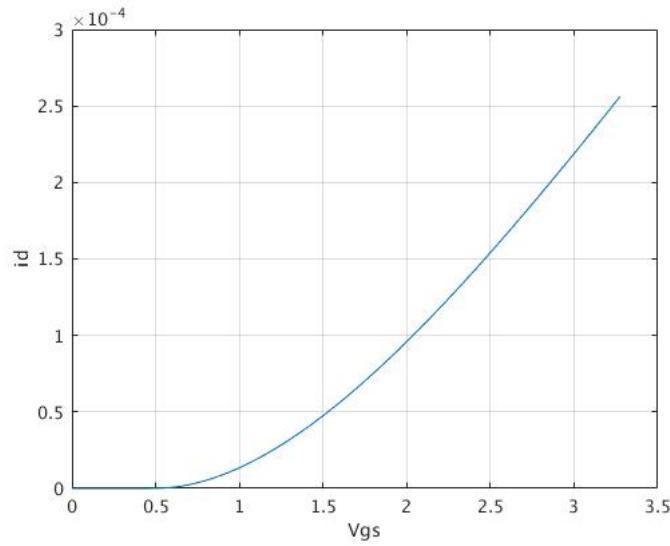


Figure 8: Simulated relationship between  $i_D$  and  $v_{GS}$  in the active region with linear y-axis

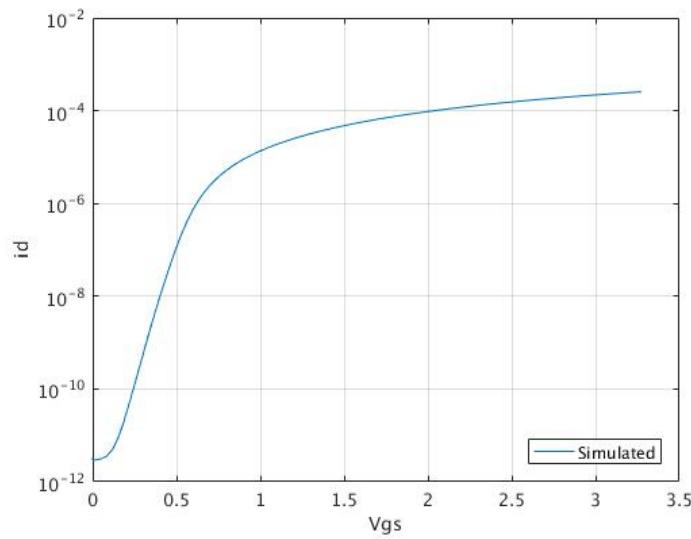


Figure 9: Simulated relationship between  $i_D$  and  $v_{GS}$  in the active region with logarithmic y-axis

**2** A circuit simulating the NMOS transistor in the triode region with  $v_{GS}$  sweeping from 0 V → 3.3 V was created. The schematic for simulating the triode region was the same as for simulating the active region, but with  $V_{dd}$  set to 50 mV. The results are shown in Figure 10 and Figure 11.

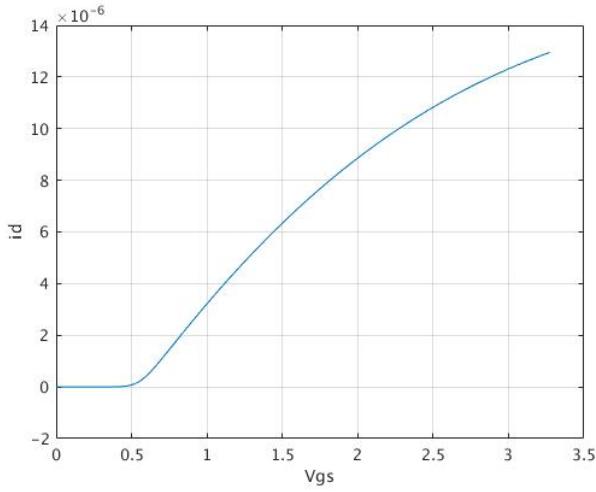


Figure 10: Simulated relationship between  $i_D$  and  $v_{GS}$  in the triode region with linear y-axis

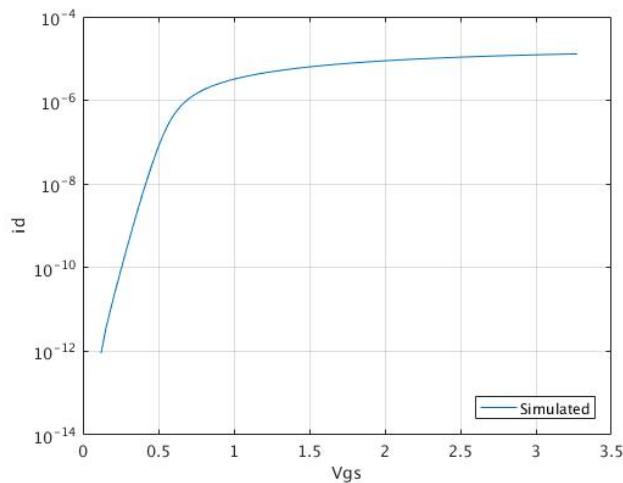


Figure 11: Simulated relationship between  $i_D$  and  $v_{GS}$  in the triode region with logarithmic y-axis

**3** A circuit simulating the NMOS transistor in with  $v_{DS}$  sweeping from  $0\text{V} \rightarrow 3.3\text{V}$  was created. The schematic is shown in Figure 12, with it's respective plots shown in Figure 13 and Figure 14.  $v_{GS}$  was set to values corresponding to the values used in Task 1, paragraph 3 (from  $0.8\text{V} \rightarrow 2.6\text{V}$  with increments of  $0.2\text{V}$ ).

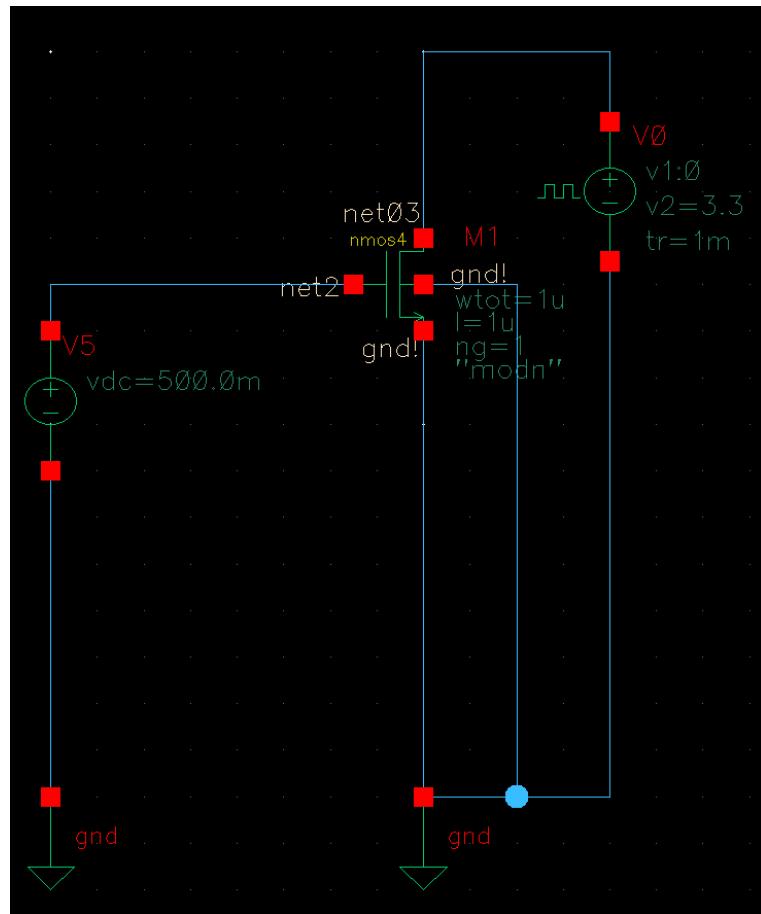


Figure 12: Cadence schematic of the circuit equivalent to the approximation in Task 1.3 (strong inversion)

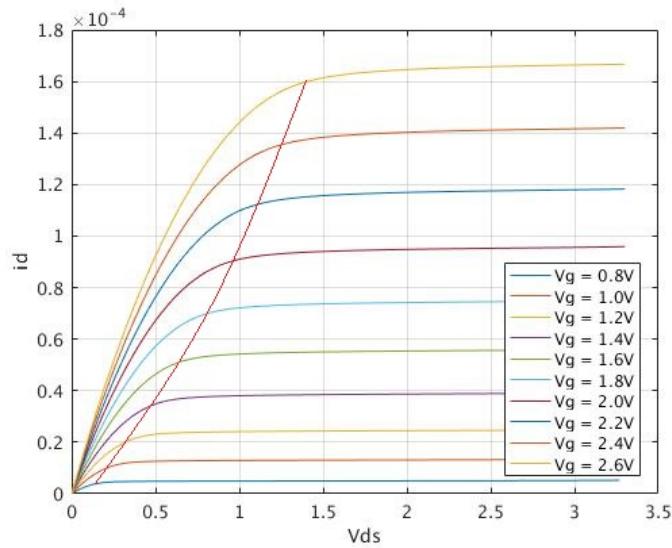


Figure 13: Simulated relationship between  $i_D$  and  $v_{DS}$  in strong inversion with linear y-axis and different  $v_{GS}$  values

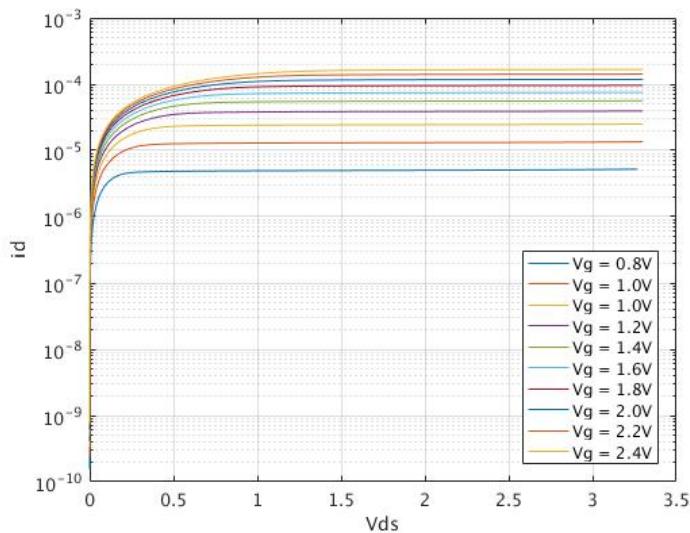


Figure 14: Simulated relationship between  $i_D$  and  $v_{GS}$  in strong inversion with logarithmic y-axis and different  $v_{GS}$  values

The knee-voltages seem to have a less quadratic relationship in the cadence simulations than in the EKV-model in strong inversion.

**4** A circuit simulating the NMOS transistor in weak inversion with  $v_{DS}$  sweeping from  $0\text{ V} \rightarrow 3.3\text{ V}$  was created. The schematic for simulating the weak inversion was the same as for simulating the strong inversion, but with  $V_{GS}$  set to values below the threshold voltage. The results are shown in Figure 15 and Figure 16.  $V_{GS}$  was set to values corresponding to the values used in Task 1 paragraph 4 (from  $0.1\text{ V} \rightarrow 0.5\text{ V}$  with increments of  $0.1\text{ V}$ ) for different simulations.

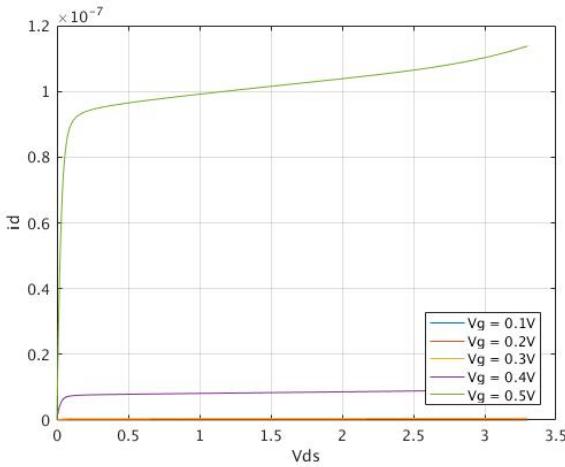


Figure 15: Simulated relationship between  $i_D$  and  $v_{DS}$  in weak inversion with linear y-axis and different  $v_{GS}$  values

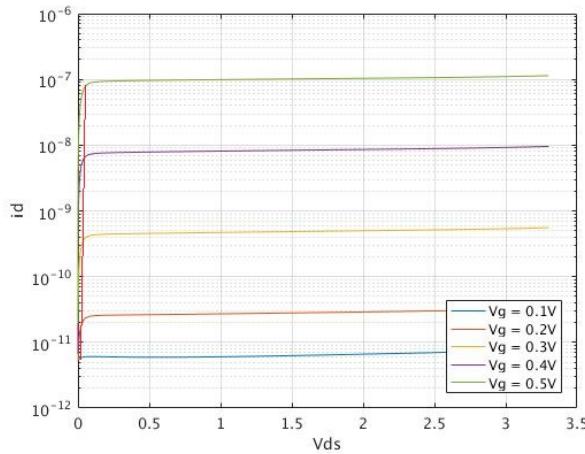


Figure 16: Simulated relationship between  $i_D$  and  $v_{GS}$  in weak inversion with logarithmic y-axis and different  $v_{GS}$  values

The knee-voltages in the cadence simulation are less constant than in the EKV-model in weak inversion.



### 3.2 Simulated values compared with the EKV model

The EKV-model and cadence plots were compared in the active region as shown in Figure 17 and 18. Changing the parameters to match in one of the regions made the values match worse with the other regions. Therefor the active region values were chosen to be matched and compared.

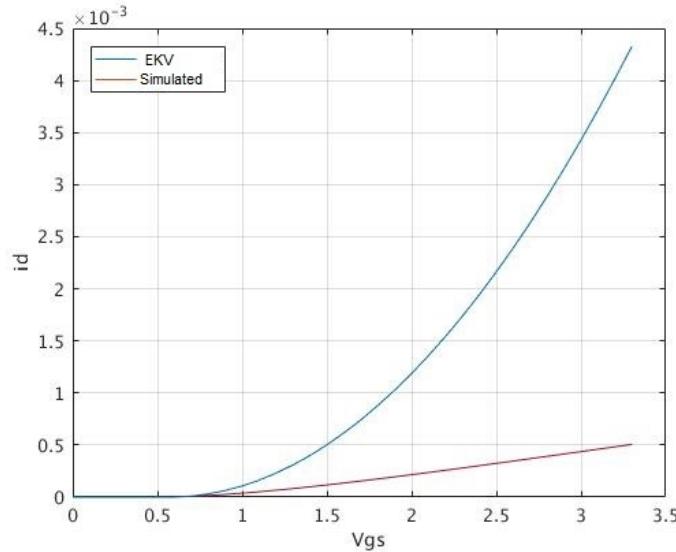


Figure 17: EKV-model with standard  $0.35\text{ }\mu\text{m}$  parameters compared with cadence simulation in the active region with linear y-axis

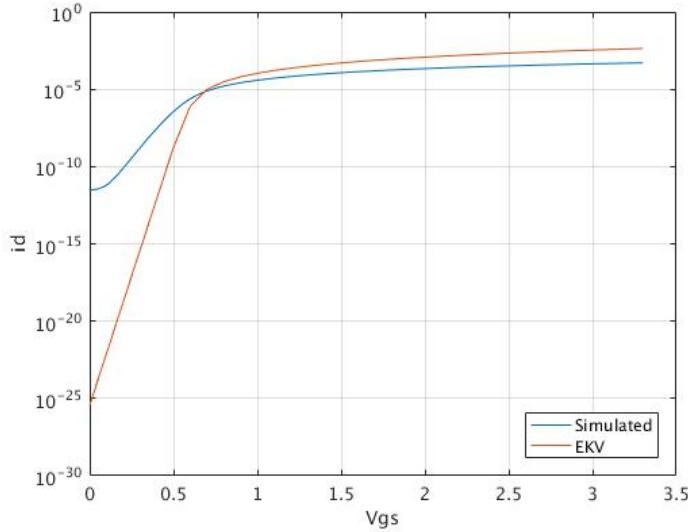


Figure 18: EKV-model with standard  $0.35\text{ }\mu\text{m}$  parameters compared with cadence simulation in the active region with logarithmic y-axis

From comparing the values, it was clear that the simulation had lower  $i_D$  values. The simulated curve also had a different knee-voltage, hence a different  $V_{tn}$ , and was more linear than the EKV-models curve.

To try to match the two approximations as much as possible the parameters  $k_n$ ,  $\lambda$ , and  $V_{tn}$  were adjusted to make them as similar as possible. To level the knee-voltage of the two graphs,  $V_{tn}$  was adjusted to  $0.47\text{ V}$  down from  $0.57\text{ V}$  which was set as the standard value. When these parameters were set, all that was left was to adjust  $k_n$  and  $\lambda$  so that  $i_D$  had appropriate values. To try to make the less EKV-models curve less exponential to match better with the simulated curve, the exponential factor,  $k_n$  was reduced and the linear factor,  $\lambda$ , was increased instead. This made the curve a lot more linear, but made the curves deviate from each other for higher values of  $v_{GS}$ . because of this,  $\lambda$  was set back to it's standard value ( $0.16\text{ }\frac{\mu\text{m}}{\text{V}}$ ). The best match was found by adjusting  $k_n$  and the appropriate value was found to be around  $50\text{ }\frac{\mu\text{A}}{\text{V}^2}$ . The results from changing the parameters are shown in Figure 19 and 20.

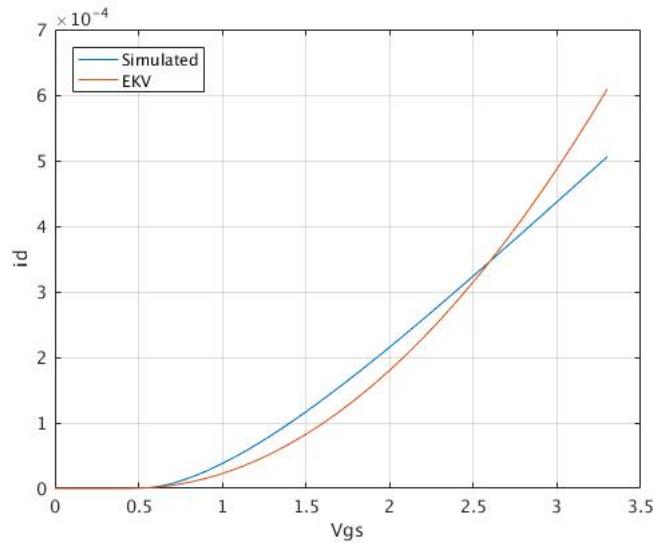


Figure 19: EKV-model with adjusted values to match cadence simulation in the active region with linear y-axis

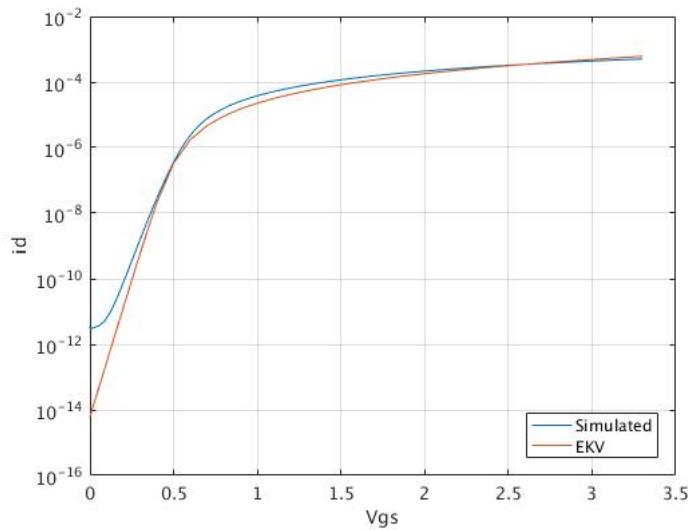


Figure 20: EKV-model with adjusted values to match cadence simulation in the active region with logarithmic y-axis

## 4 Measurements

In order to see how well Cadence and the EKV-model described the operation of a transistor a real device was tested. The device used in this experiment was the CD4007UBE. To have comparable results, the same exercises were performed as in task 1 and 2 with corresponding voltages . The pin-configuration found in the datasheet is shown in Figure 21.

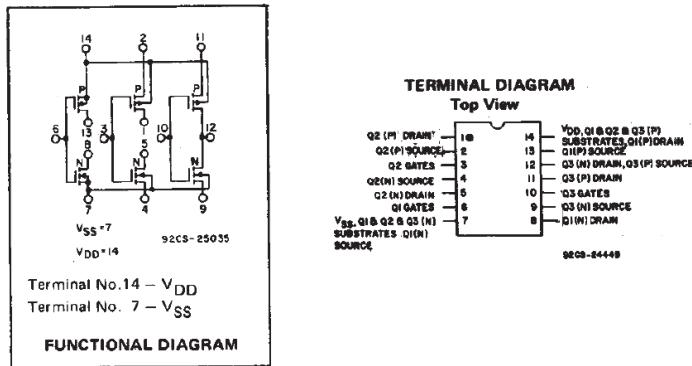


Figure 21: Pin-configuration and functional diagram of CD4007UBE

CD4007UBE connected on the breadboard and the equivalent circuit model is shown in Figure 22 where the blue wire is the drain, the white wire is the source and the green wire is the gate. The voltages  $v_{GS}$  and  $V_{dd}$  were controlled using the Agilent E3631A DC power supply.

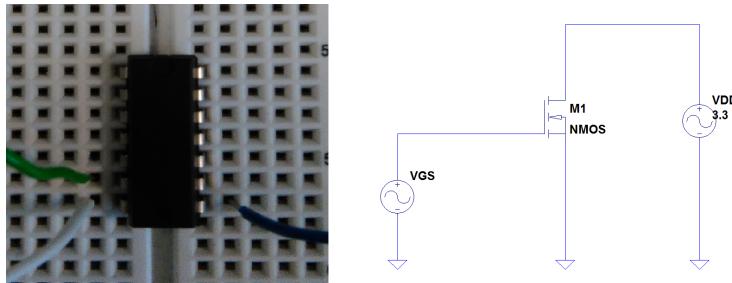


Figure 22: Schematic and breadboard setup

## 4.1 Experimental method



For all the plots in this section 330 values were measured with increments of 0.01 V in order to get a decent accuracy in the plots. Also, for all the measurements the source and bulk were connected to ground as indicated in Figure 22.

**Measuring  $i_D$  in the active region** was done by connecting channel 2 of the Agilent E3631 DC voltage source to the drain and setting the value to 3.3 V and by connecting channel 1 to the gate, sweeping from 0 → 3.3 V with increments of 0.01 V. The results are shown in Figure 23 and Figure 24.

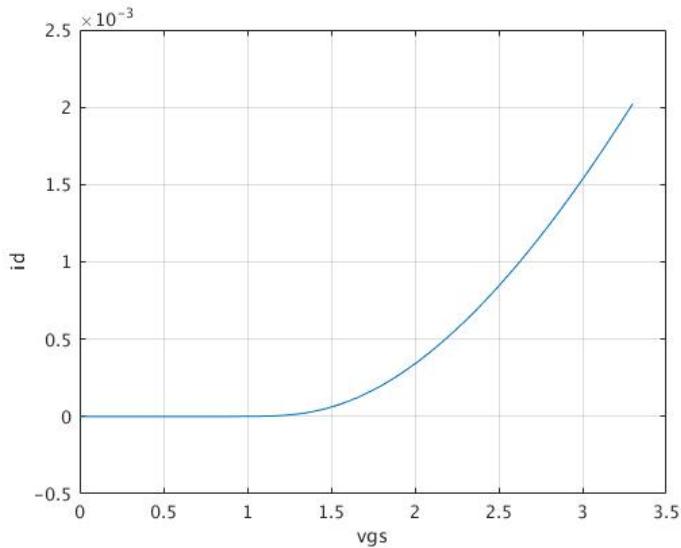


Figure 23: Measured  $i_D$  in the active region with linear y-axis

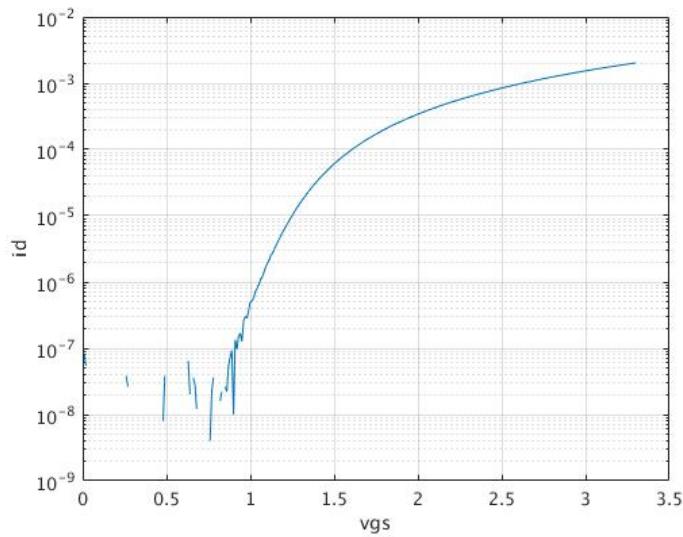


Figure 24: Measured  $i_D$  in the active region with logarithmic y-axis

**Measuring  $i_D$  in the triode region** was done by connecting channel 2 of the Agilent E3631 DC voltage source to the drain and setting the value to 50 mV and by connecting channel 1 to the gate, sweeping from 0 → 3.3 V with increments of 0.01 V. The results are shown in Figure 25 and Figure 26

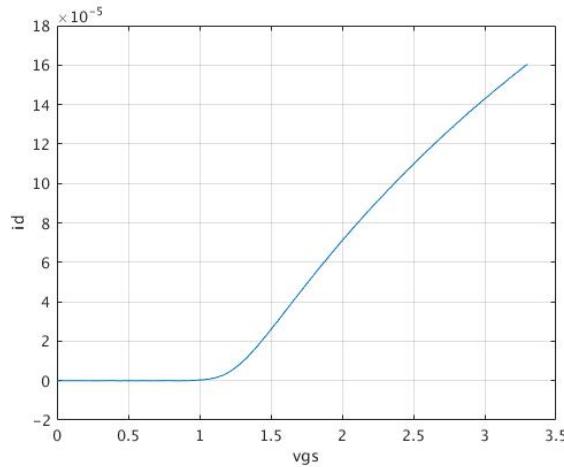


Figure 25: Measured  $i_D$  in the triode region with linear y-axis

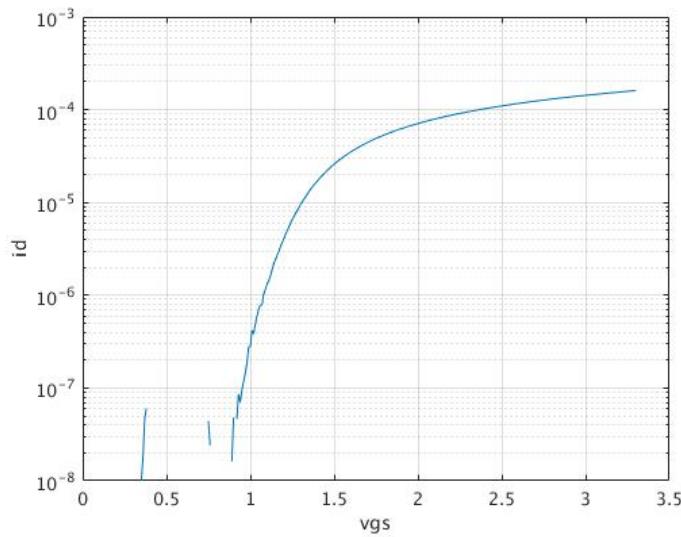


Figure 26: Measured  $i_D$  in the triode region with logarithmic y-axis

**Measuring  $i_D$  in strong inversion** was done by connecting channel 2 of the Agilent E3631 DC voltage source to the gate and setting the value to the values corresponding to the values task 1 paragraph, and by connecting channel 1 to the drain, sweeping from  $0 \rightarrow 3.3$  V with increments of 0.01 V. Figure 27 and Figure 28

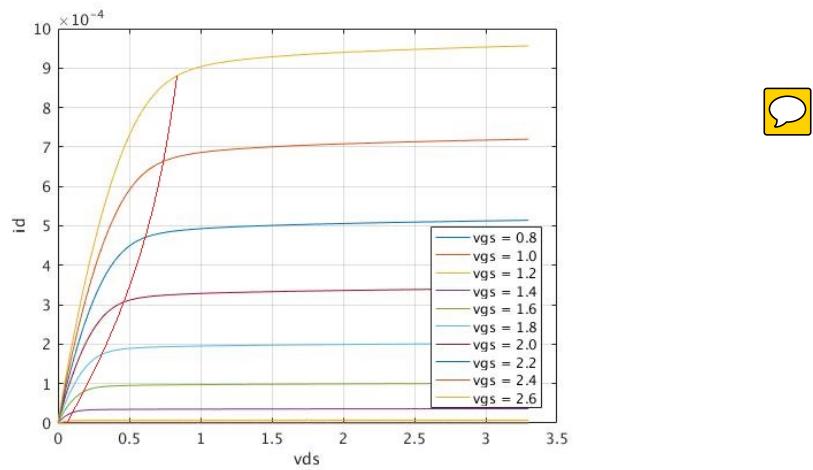


Figure 27: Measured  $i_D$  in strong inversion with linear y-axis

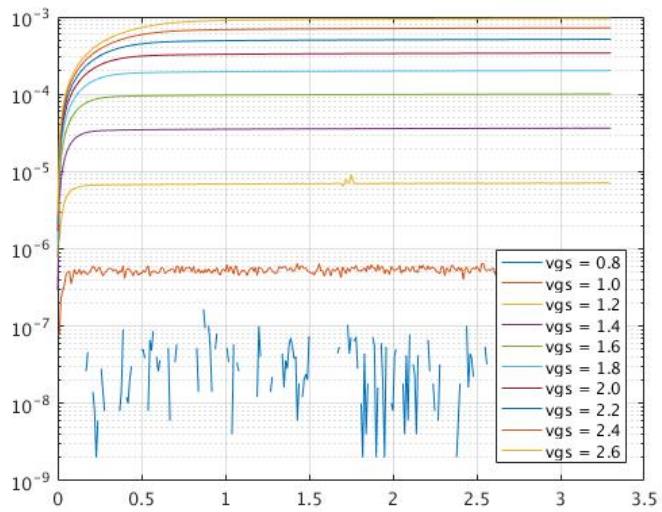


Figure 28: Measured  $i_D$  in strong inversion with logarithmic y-axis

**Measuring  $i_D$  in weak inversion** No currents in weak inversion are large enough to be measured by the Agilent 34401A multimeter. The multimeters resolution is too low, as indicated by the curves for  $v_{GS} = 0.8\text{ V}$  and  $1.0\text{ V}$  in strong inversion (Figure 28).



## 4.2 Comparing measurements with simulations and calculations

Since the active region was compared in task 2 it was logical to compare this region with the measured values as well. The measured values and the values from the EKV-model were plotted together as shown in Figure 29 and Figure 30.

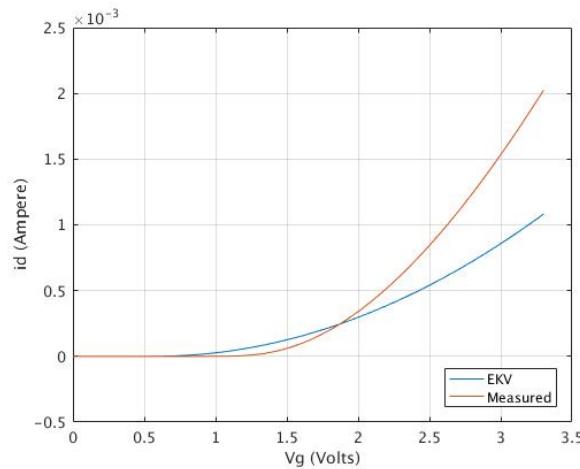


Figure 29: Comparing the measured values with the EKV-model in the active region with linear y-axis

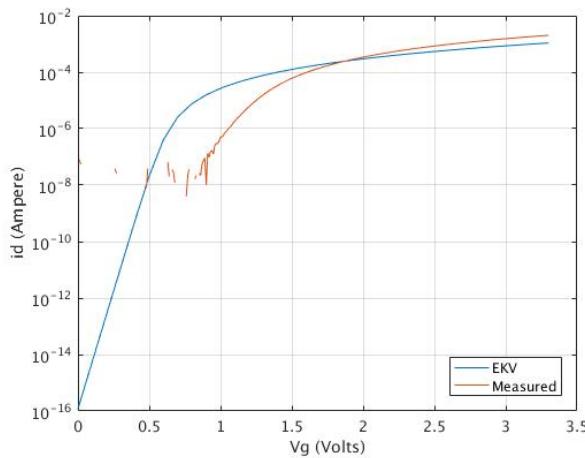


Figure 30: Comparing the measured values with the EKV-model in the active region with logarithmic y-axis

From the look of it, the EKV-model fits the measured values a lot better than when comparing the EKV-model to the cadence simulation. The measured values are actually higher than the EKV-models and has the same exponential behavior. The biggest difference in the curves is the knee-voltage. The real transistor seems to have a higher threshold voltage than the standard value used in the EKV-model.



### 4.3 Adjusting the EKV-Model to better fit the parameters of the transistor

To match the knee-voltage,  $V_{tn}$  was set to 1.0 V. To make the current levels match,  $k_n$  was set to  $250 \frac{\mu A}{V^2}$ , while  $\lambda$  was left alone. The results are shown in Figure 31 and Figure 32.

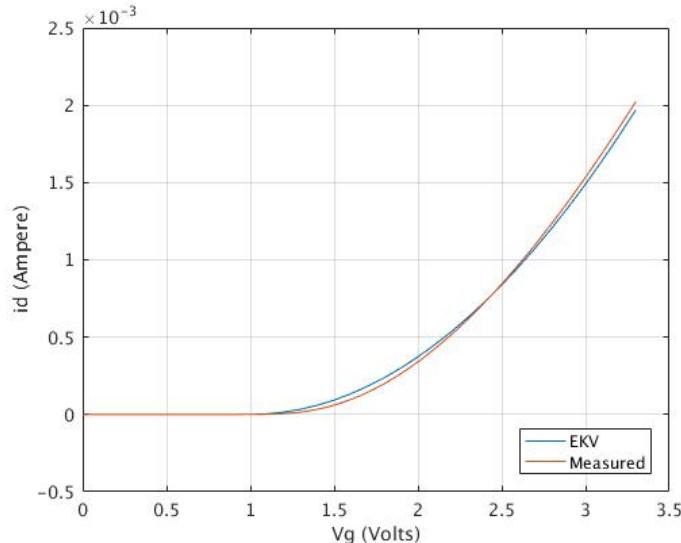


Figure 31: Comparing the measured values with the adjusted EKV-model in the active region with linear y-axis

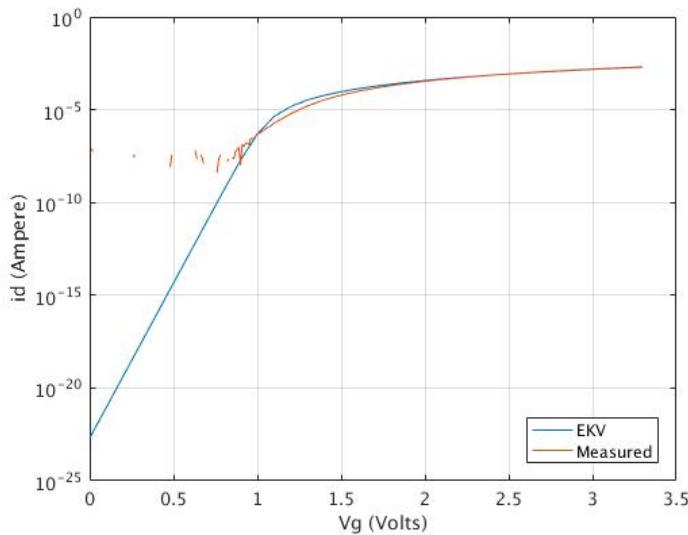


Figure 32: Comparing the measured values with the adjusted EKV-model in the active region with logarithmic y-axis

## 5 Common Source Amplifier

The NMOS transistor was connected as a common source amplifier, as shown in the schematic in Figure 33. The resistor values chosen were  $4.7\text{ k}\Omega$ ,  $470\text{ k}\Omega$  and  $2\text{ M}\Omega$ .  $V_{ss}$  was set to  $0\text{ V}$  and  $V_{dd}$  was set to  $3.3\text{ V}$ . The gate voltage  $v_G$  was swept from  $0\text{ V} \rightarrow 3.3\text{ V}$  to investigate the behavior of the amplifier with different resistances. Figure 34 shows the relationship between  $V_{out}$  and  $v_G$  for the different resistor values. Investigating the plot further, reveals the gain and the appropriate bias current listed in Table 2.



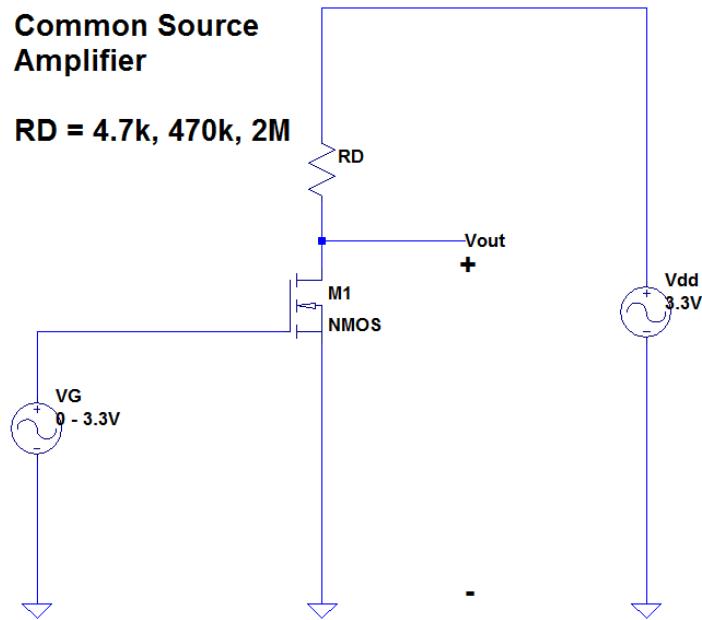


Figure 33: Schematic of the common source amplifier investigated in this task

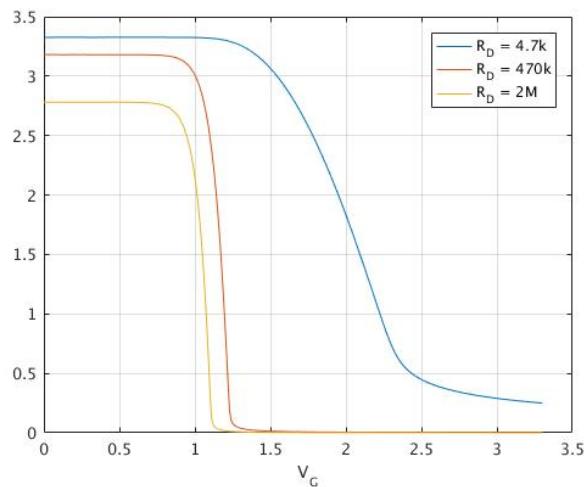


Figure 34: Measured output voltage while sweeping  $v_G$  from 0 V to  $V_{dd}$  with different values for  $R_D$

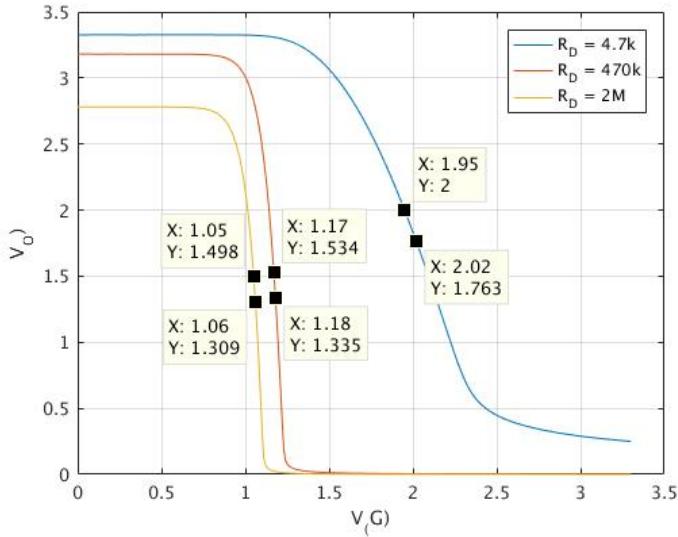


Figure 35: Measured output voltage while sweeping  $v_G$  from 0 V to  $V_{dd}$  with different values for  $R_D$  with points indicating the gain

From Figure 35 the gain is given by eq. 7

$$G_V = \frac{\Delta Y}{\Delta X} = \frac{y_2 - y_1}{x_2 - x_1} \quad (7)$$

Picking the operating point of the transistor was done graphically by finding the  $V_{GS}$  corresponding to the middle of the linear region of the amplifier for each resistor respectively. Figure 36 shows the operating points  $Q_n$  with respect to  $V_{GS}$  and  $V_{DS}$ . The operating points are determined by eq. 8

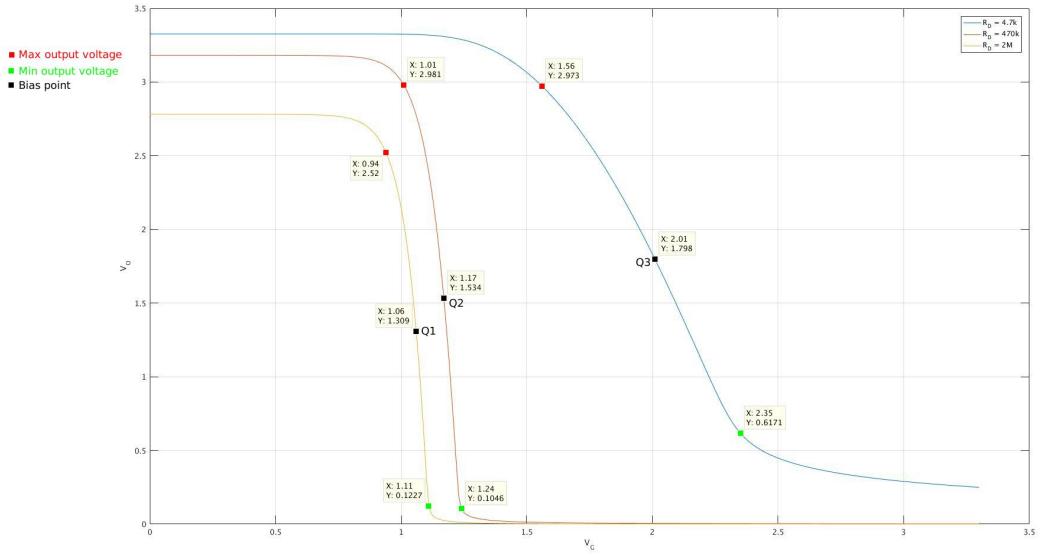


Figure 36: Measured output voltage while sweeping  $v_G$  from 0 V to  $V_{dd}$  with different values for  $R_D$  indicating the operating points

$$Q|_{V_{DS}} = \frac{\text{Max output voltage} - \text{Min output voltage}}{2} + \text{Min output voltage} \quad (8)$$

Where "Max output voltage" and "Min output voltage" are the two extremes of the linear region found graphically indicated by green and red points in Figure 36. From this the bias current  $I_D$  is can be found for each of the resistor values with ohm's law ( $I_D = \frac{Q_{V_{DS}}}{R_D}$ ).

Table 2: Gain and operation points for the different resistors

	<b>4.7 kΩ</b>	<b>470 kΩ</b>	<b>2 MΩ</b>
$A_V$	-3.4 V/V	-19.9 V/V	-18.9 V/V
$Q_{V_{GS}}$	2.0 V	1.2 V	1.1 V
$Q_{V_{DS}}$	1.8 V	1.5 V	1.3 V
$I_D$	0.38 mA	3.19 μA	0.65 μA

None of the resistors are biased in weak inversion, assuming the threshold voltage  $V_{tn} = 1$  V as indicated in task 5. The resistor value with the highest gain is the 470 kΩ resistor with -19.9 V/V. The small signal model for the circuit is shown in Figure 37. From the schematic it is clear that

the output voltage gain,  $A_V = g_m(R_D||r_o)$ , where  $g_m = k_n V_{OV}$ . Before the measurement was performed the  $2\text{ M}\Omega$  resistor was expected to have the highest gain, but when looking at the definition of the transconductance  $g_m$  it makes perfect sense that the  $470\text{ k}\Omega$  resistor gives a higher gain than the  $2\text{ M}\Omega$  resistor.

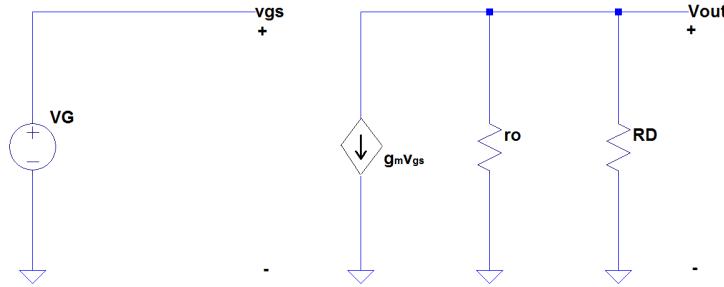


Figure 37: Small signal representation of the common source amplifier

Since the  $470\text{ k}\Omega$  and  $2\text{ M}\Omega$  resistors are so much greater than  $r_o$ ,  $(R_D||r_o)$  can be approximated to  $r_o$  and is therefore the same for both the resistors.  $g_m$ , however, is not constant for both the cases. Since the  $2\text{ M}\Omega$  resistor will cause a larger voltage drop than the  $470\text{ k}\Omega$  resistor with the same current running through it, the linear region is at a lower gate voltage. The rate at which  $v_{DS}$  is changing in correspondence with  $v_{GS}$  is directly proportional to the overdrive voltage ( $g_m = k_n V_{OV}$ ), which is lower in the linear region with the  $2\text{ M}\Omega$  resistor than with the  $470\text{ k}\Omega$  resistor. This reduction in transconductance and close to no difference in the total resistance explains why the  $470\text{ k}\Omega$  resistor gives the highest gain. The gain is often inversely proportional to the bandwidth of an amplifier, assuming that the gain bandwidth product is constant. This indicates that the resistor with the lowest gain will have the greatest bandwidth, which in this case is the  $4.7\text{ k}\Omega$  resistor.

## **6 References**

Sedra and Smith - Microelectronic circuits  
CD4007UBE Datasheet