INF3410 fall 2016 mandatory laboratory exercise

Writen by Raouad Sahraoui and Espen Otervik Granum

This lab is designed to give a feeling for the appropriateness of using models and simulations as opposed to measurements on a physical device. In this assignment, a simple EKV model is designed and a simulation of an NMOSFET is characterised. This characterization is compared with a cadence simulation and lastly compared to a real simulation of a physical CMOS chip (CD4007UBE)

Prelab

Per the EKV-paper[1] only three basic parameters are required for a first order characterization and modelling of a transistor, the parameters being: the gate threshold voltage(Vto), the slope factor (n) and the transfer parameter (β) which can be replaced with the specific current (I_S).

The bulk voltage is defined as gnd/0 V, and in this assignment $V_B=V_S$

The EKV-paper suggest that a uniform equation can be used to model with an acceptable precision in a wide range of currents:$I_{F(R)}I_S ln^2(1 + \exp(\frac{V_G - V_{TO} - nV_{S(D)}}{2nU_T}))$
From this equation, a model in matlab was constructed (see included EKV.m).

Task 1

The goal of the task is to plot I_D as a function of v_{GS} of a NMOS transistor in the *active region.* v_{GS} should be swept from 0 to VDD, and two curves should be produced, one linear and one with a logarithmic y-axis.

To ensure that we are in the active region, $v_{GS}>V_{TO}$ and $V_{DS}\geq(v_{GS}-V_{TO})$

$V_{Gs}>V_{TO}$, the drain current is well approximated by the quadratic, whereas for $V_G<V_{TO}$ (i.e., sub-threshold) the drain current depends approximately exponentially on V_{GS}. Thus, the drain current is not strictly zero below threshold, merely exponentially small.

[1] http://www.uio.no/studier/emner/matnat/ifi/INF3410/h16/materiale/vittoz94b.pdf

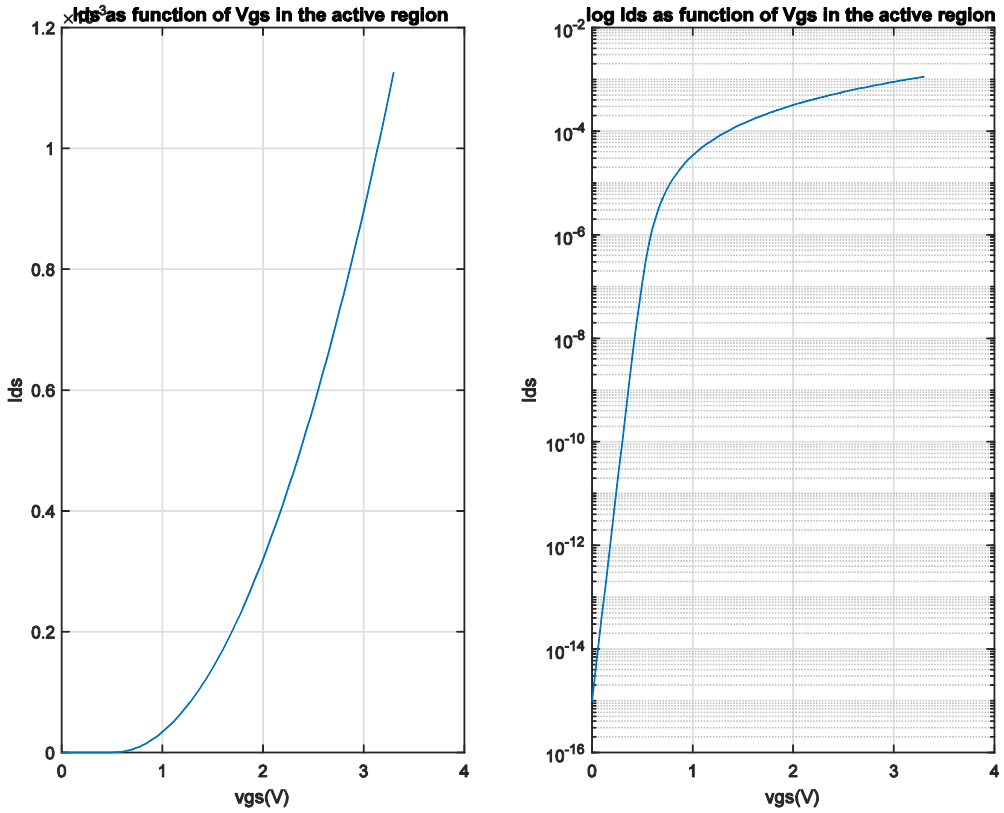


Figure 1: Ids vs Vgs in the active region

As figure 1 shows, the area from 0 to Vto is quadratic as predicted.

Task 1.2

The goal of the task is to plot I_D as a function of v_{GS} of a NMOS transistor in the *triode region.* v_{GS} should be swept from 0 to VDD, and two curves should be produced, one linear and one with a logarithmic y-axis.

To ensure that we are in the triode region, $v_{GS}>V_{TO}$ and $V_{DS}<(v_{GS}-V_{TO})$

In the triode region the MOSFET should act like a transistor, and give rise to an linear curve to the point where V_{DS} is less then $v_{GS}-V_{TO}$

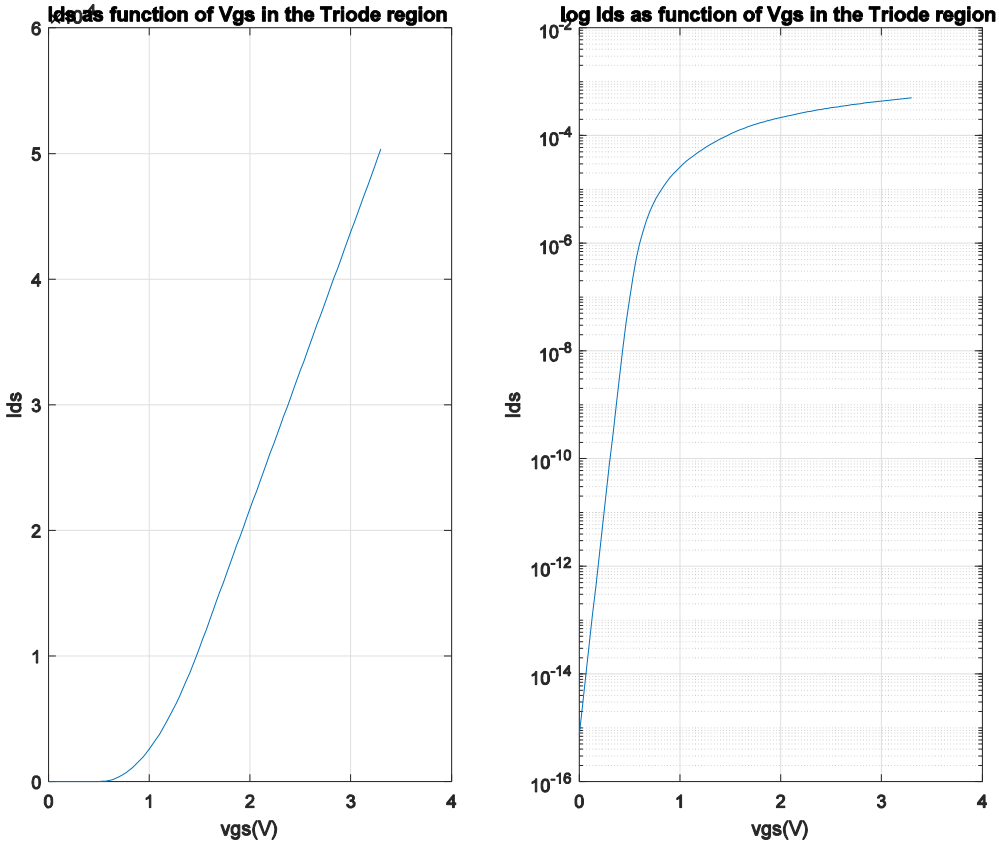


Figure 2: IDS as function of VGS in the triode region

As predicted we can clearly see a linear curve, the drain voltage has been set to 1 V

Task 1.3

The goal of this task is to plot I_D as a function of V_{DS} for at least five different V_{GS} and ensure that the plot is in strong inversion.
According to a text produced by R.R.Harrison[2] > The boundaries between weak, moderate, and strong inversion can be approximated in terms of voltages or currents. Of course, the boundaries between the areas are fuzzy, with no clean breaks. Here are two approximations sometimes used:

$V_{GS} > V_{TO} + 100mV$	Strong inversion
$V_{TO} + 100mV > V_{GS} > V_{TO} - 100mv$	Moderate inversion
$V_{GS} < V_{TO} - 100mV$	Weak inversion

These assumptions are used in the following tasks
V_{GS} is plotted from 1.1V to 3.3V

[2] http://www.ece.utah.edu/~harrison/ece5720/Subthreshold.pdf

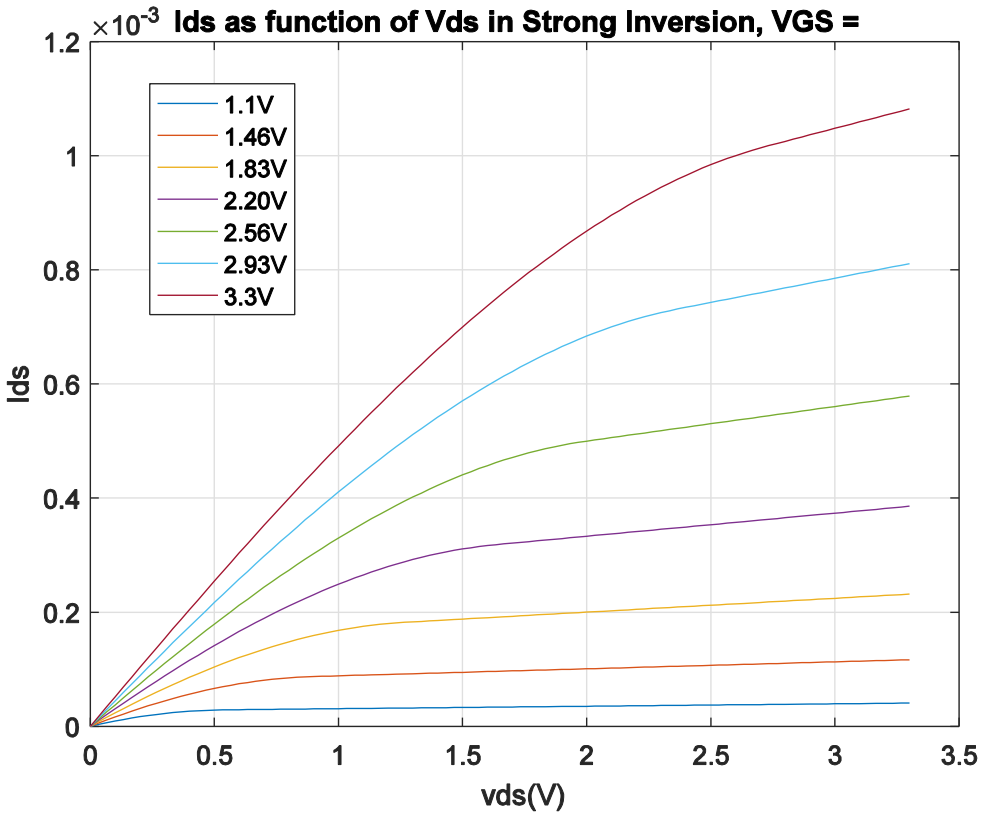


Figure 3: Ids VS VDS in strong invertion

Since all the voltages (V_{GS}) are larger then V_{TO} + 100 mV, we can assume that we are in strong inversion

Task 1.4

As task 1.3, Ids is plotted as a function of V_{DS} in weak inversion. As mentioned in the previous task, we assume that weak inversion is in the region $V_{GS} < V_{TO}$ - 100mV

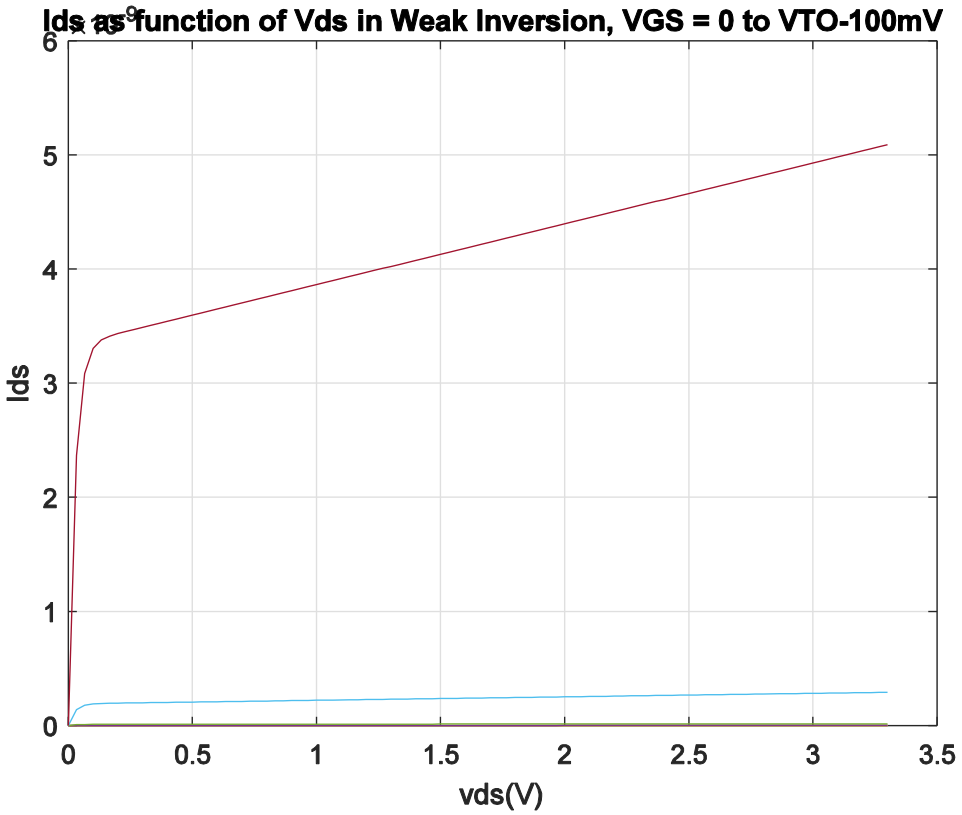


Figure 4: IDs as a function of VDS in weak inversion

Figure 4 shows us the the plot in weak inversion, but we can see that we are missing serval VGS voltages. They are indeed there but at a lower current and can be shown in figure 5.

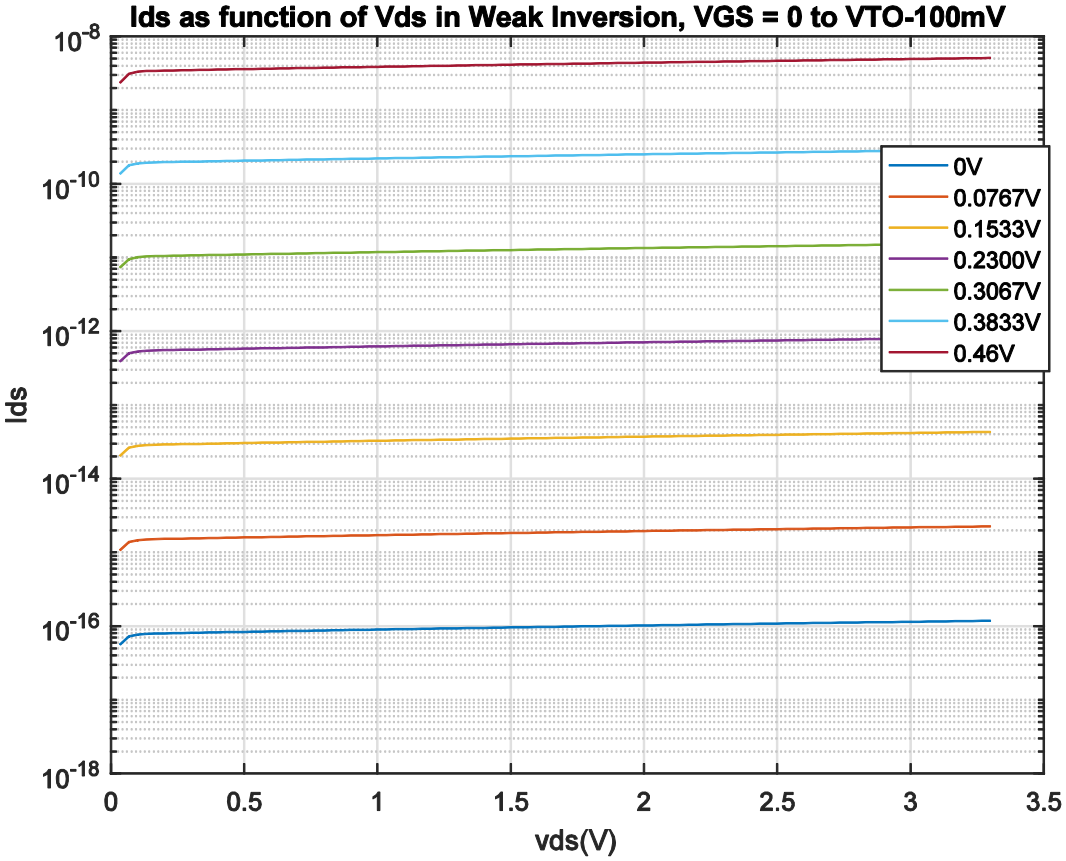


Figure 5: IDS as a function of VDS with a logarithmic Y-scale

It is expected that the spacing between the voltages should be equal, which seems to be doing.

Task 2

The same steps as in task 1 is to be repeated, but with the simulation program cadence. The same parameters as previous is still valid.

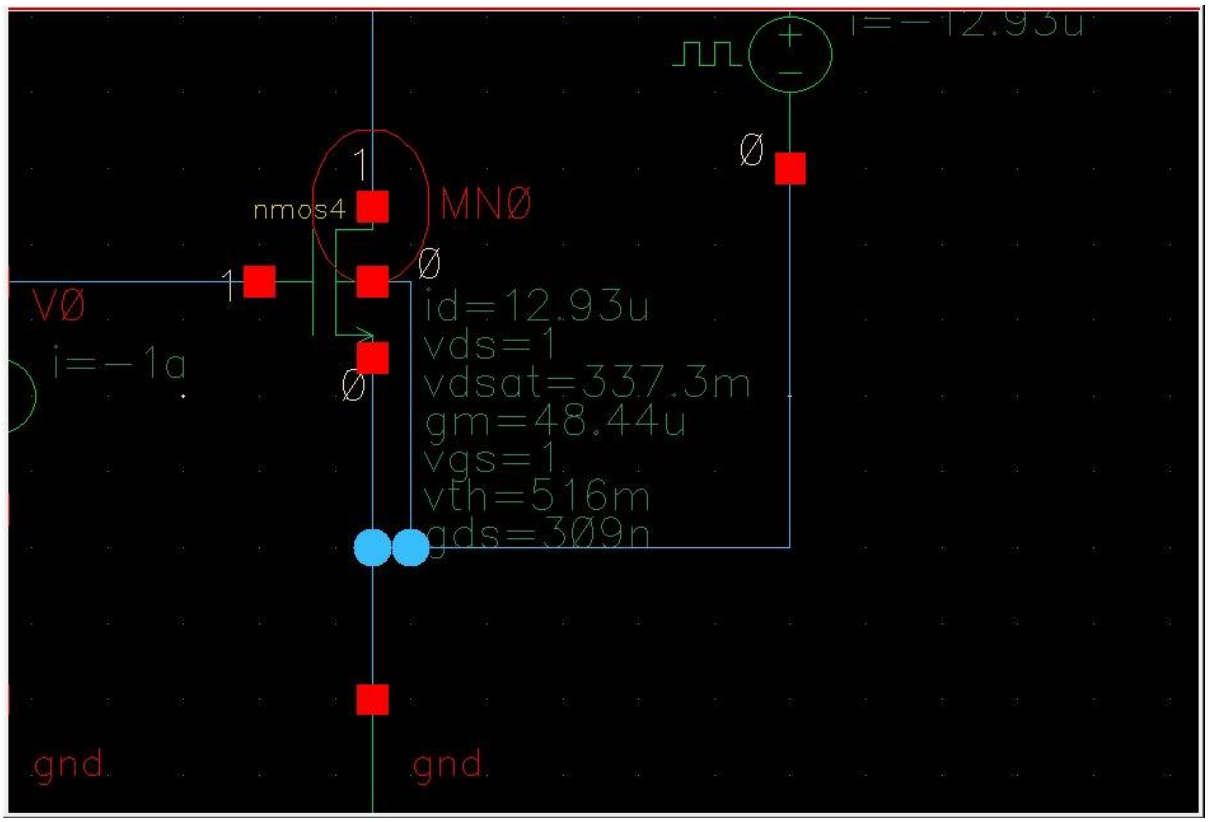


Figure 6: Cadence simulation setup

The goal of this task is to compare the EKV model to the cadence model.

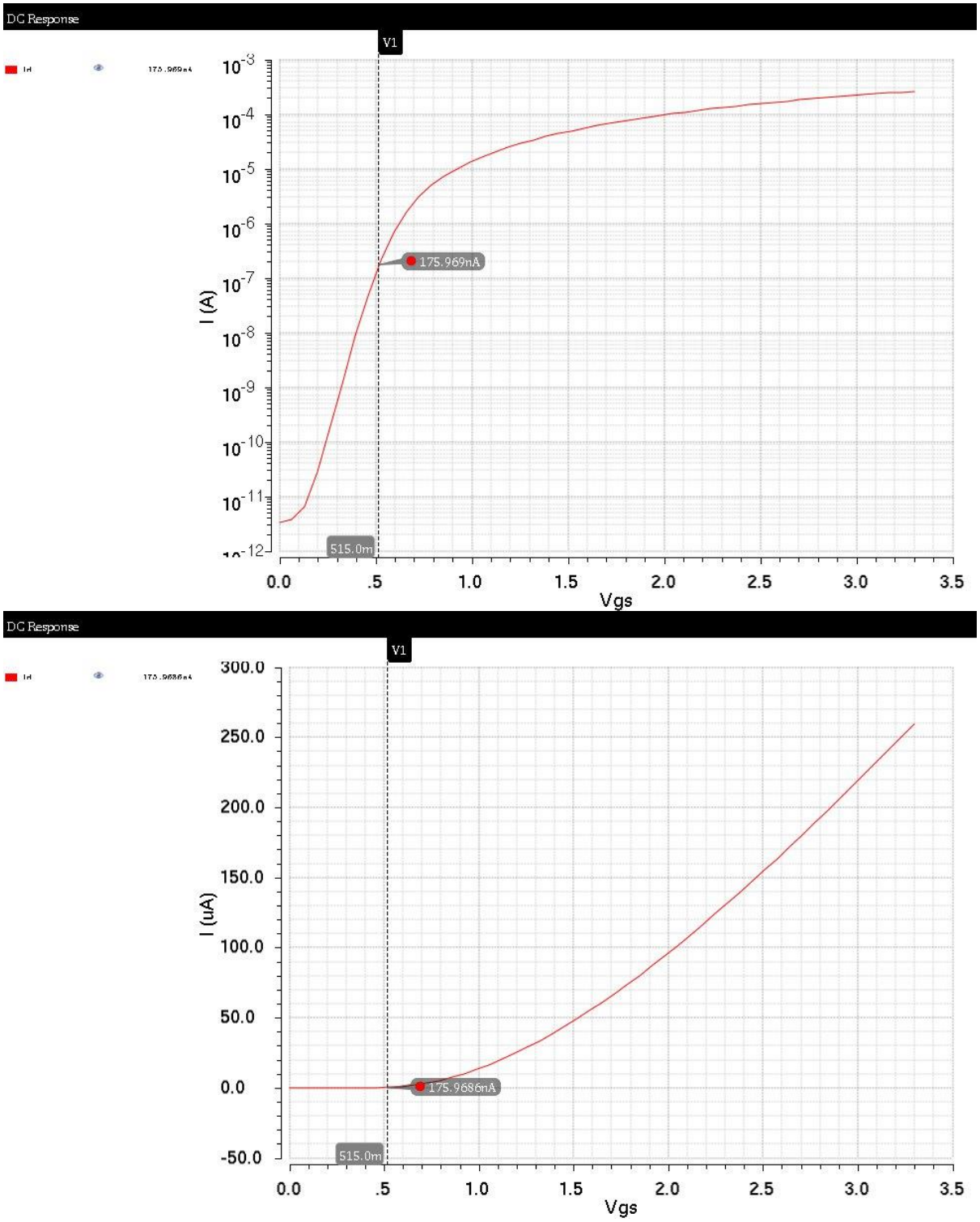


Figure 7: linear and logarithmic plot of ID as a function of VGS in the active area

Comparing figure 1 and figure 5, we can clearly see similarities. They both are quadratic, and the immediately difference is the drain to source current, which is lower in the cadence version. This is surly explained by the cadence model is more complete and have more factors to calculate the various currents etc. The EKV model starts of at a lower current (picture 1)

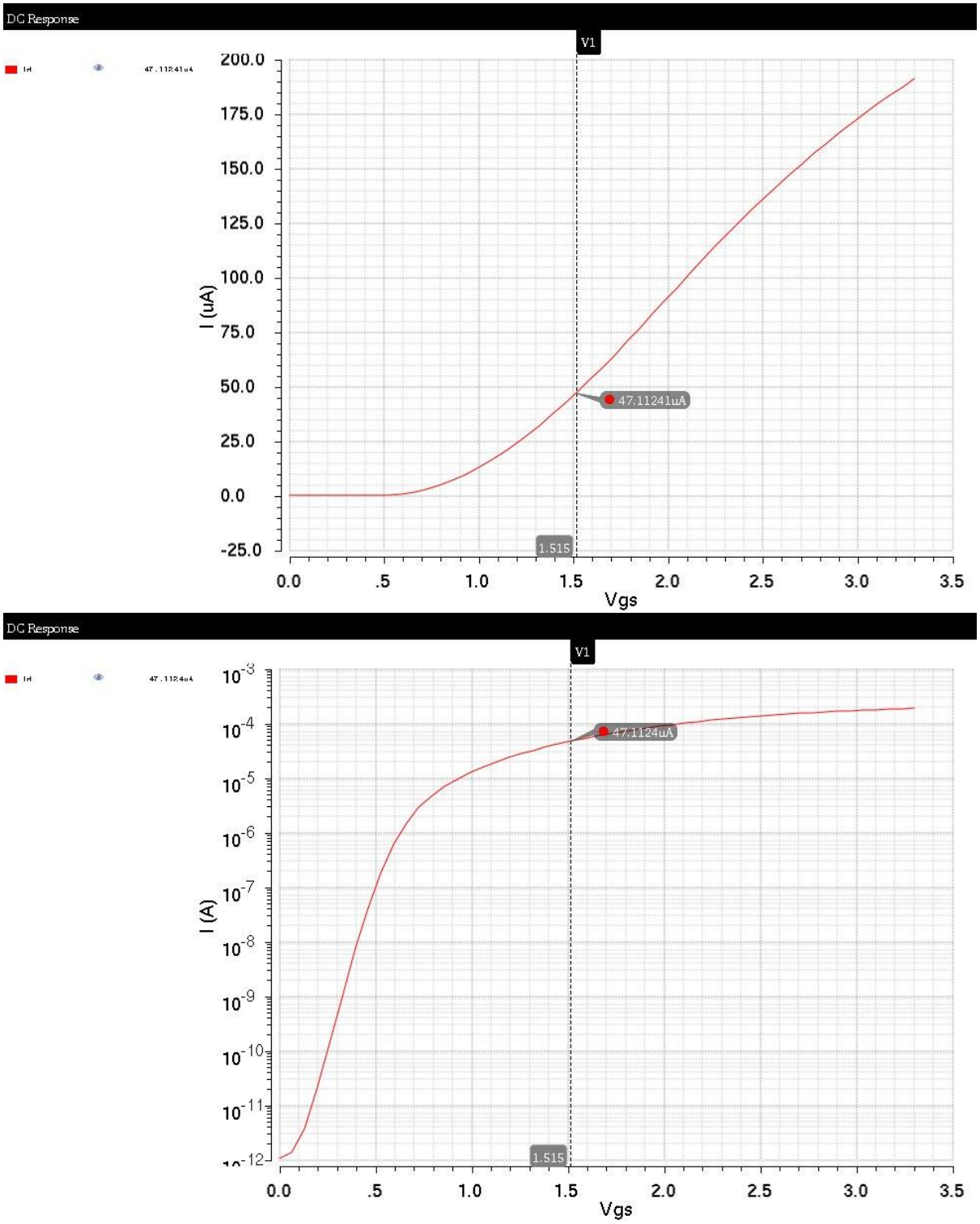


Figure 8: IDS as a function of VGS in the triode area

Comparing figure 2 with figure 5 we can see some different results. The linear curve in picture 5 is concave, but should be linear. The reason may be that cadence is set to long gate modulation.

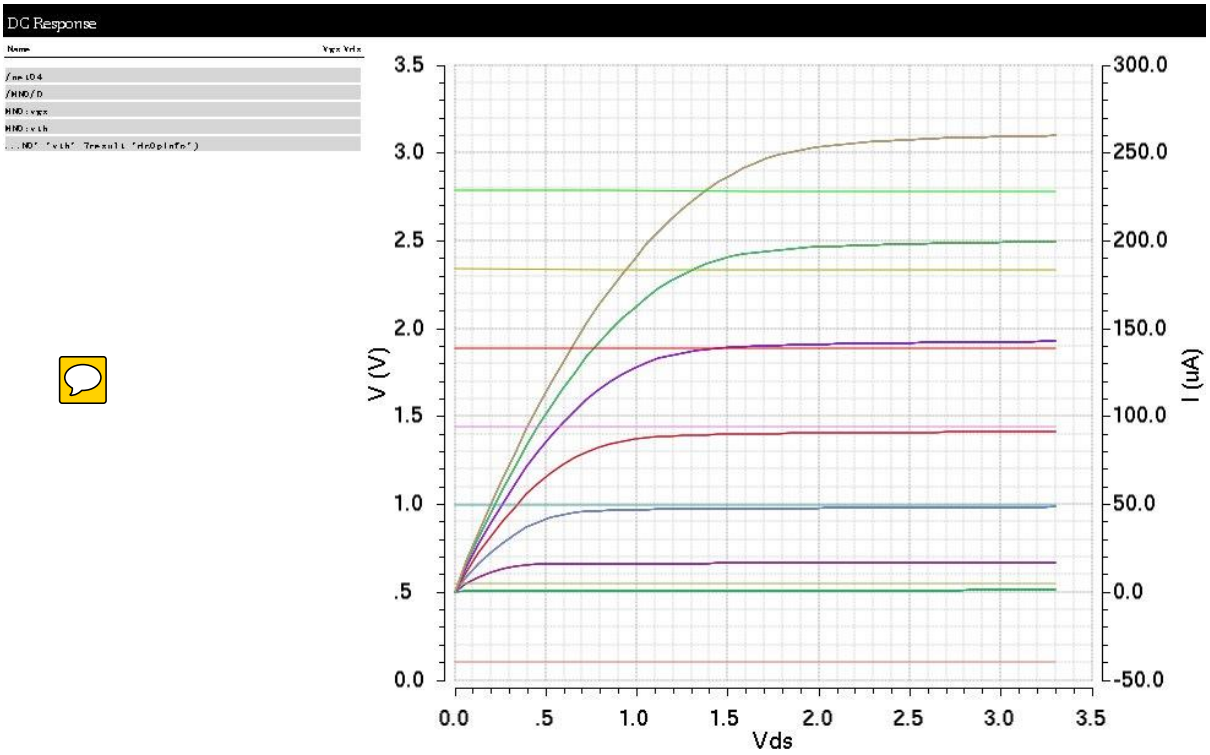


Figure 9: ID as a function of VDS in strong inversion.

On the left Y-axis is the Vg voltage and on the right side is the I_{DS} current.

Comparing figure 9 with figure 3, we can see a difference. It appears that the threshold voltage on the cadence model is higher than the EKV model. It looks like the cadence threshold voltage is a little above 1V compared to the EKV that had only 0.57 V.

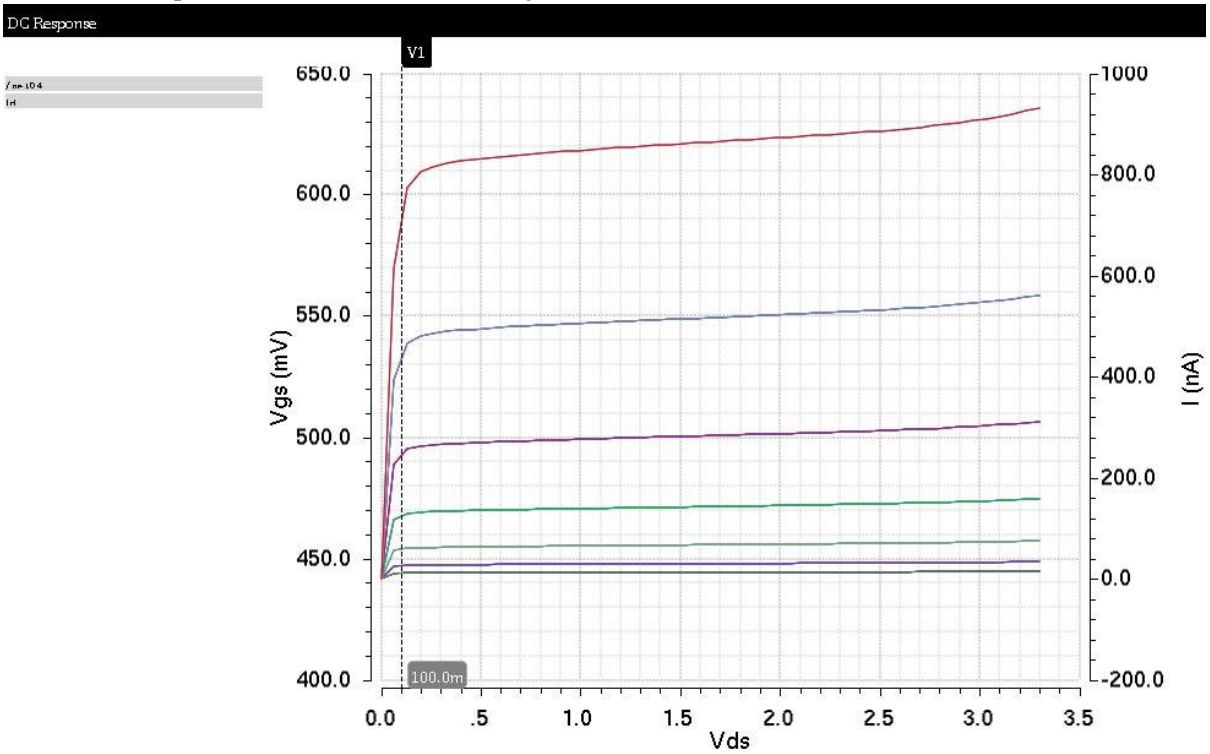


Figure 10: Id as a function of VDS in weak inversion

Comparing figure 10 and figure 5, we can see a reasonable approximation, but the spacing between the voltages in the cadence model is not as equally spaced as it should. This again could be the results of the cadence model, or wrong plotting etc.

Task 3

Here the cadence and the EKV-model are plotted together to compare and alternative adjust the EKV-Model. The curve looks like this :

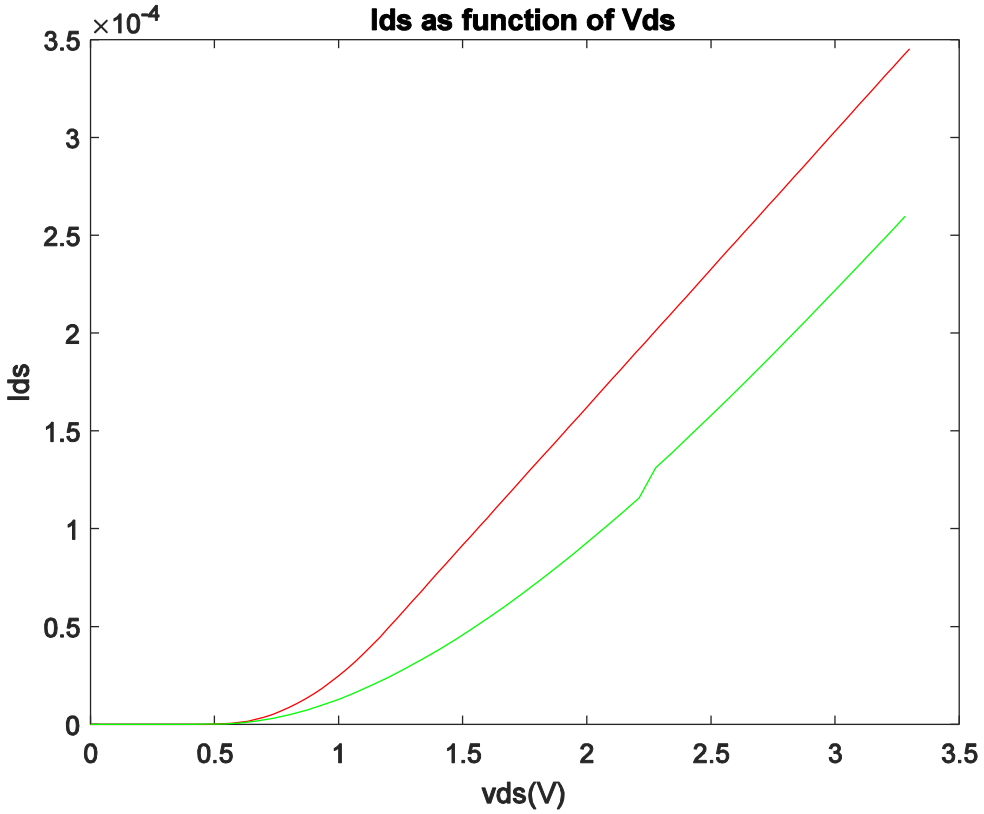


Figure 11: cadence model and EKV model plotted in the same curve. EKV is unadjusted

The green curve is loaded from cadence and plotted with the EKV-model. We can see that there is quite a difference, but this is expected.

By adjusting some parameters: Lambda = 0.016 and the $K_n=155*10^{-6}$ and V_{th} = 0.915

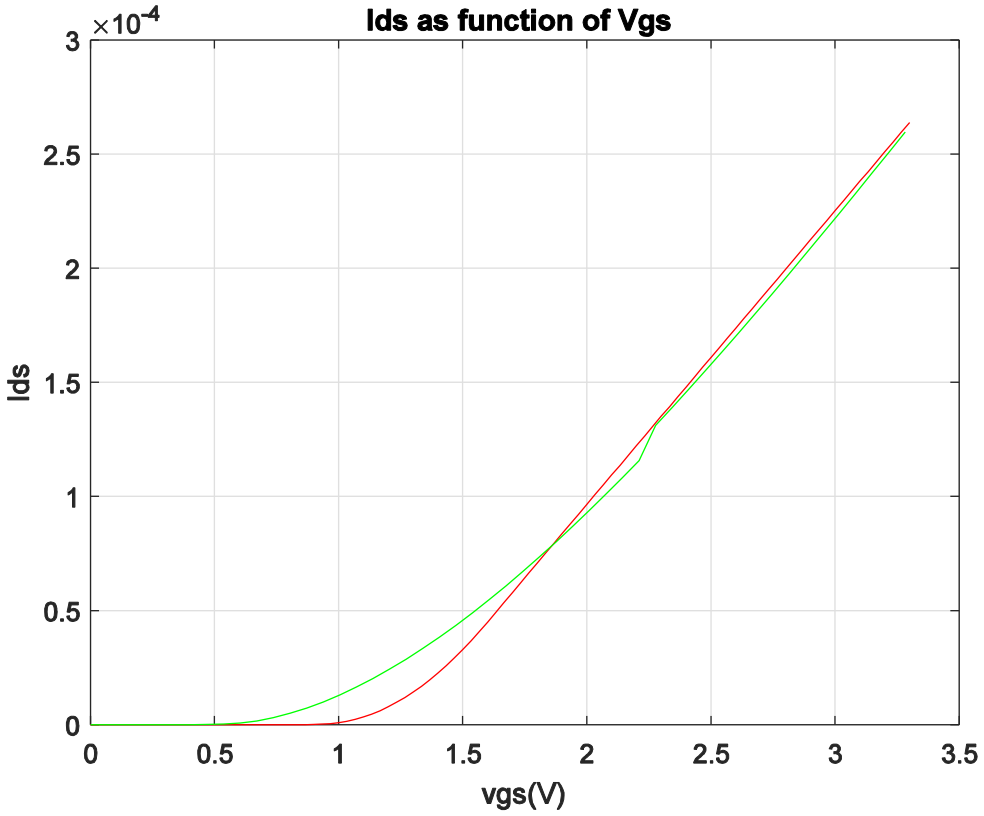


Figure 12: Adjusted EKV model

This is best adjustment for the EKV-model to cover the most of curve produced by cadence. It is not a perfect fit, but shows almost the same trend.

Task 4

The goal of this task is to measure on a real device. The task asked us to measure on a MC14007UBCP, but the actual chip the measurements was performed on was a CD4007UBE. A CMOS Dual Complementary Pair Plus Inverter that is similar to the MC14007UBCP.
The chip consists of three n-channel and three p-channel enhancement-type MOS transistors.
The data sheet was consorted and the connected as described.

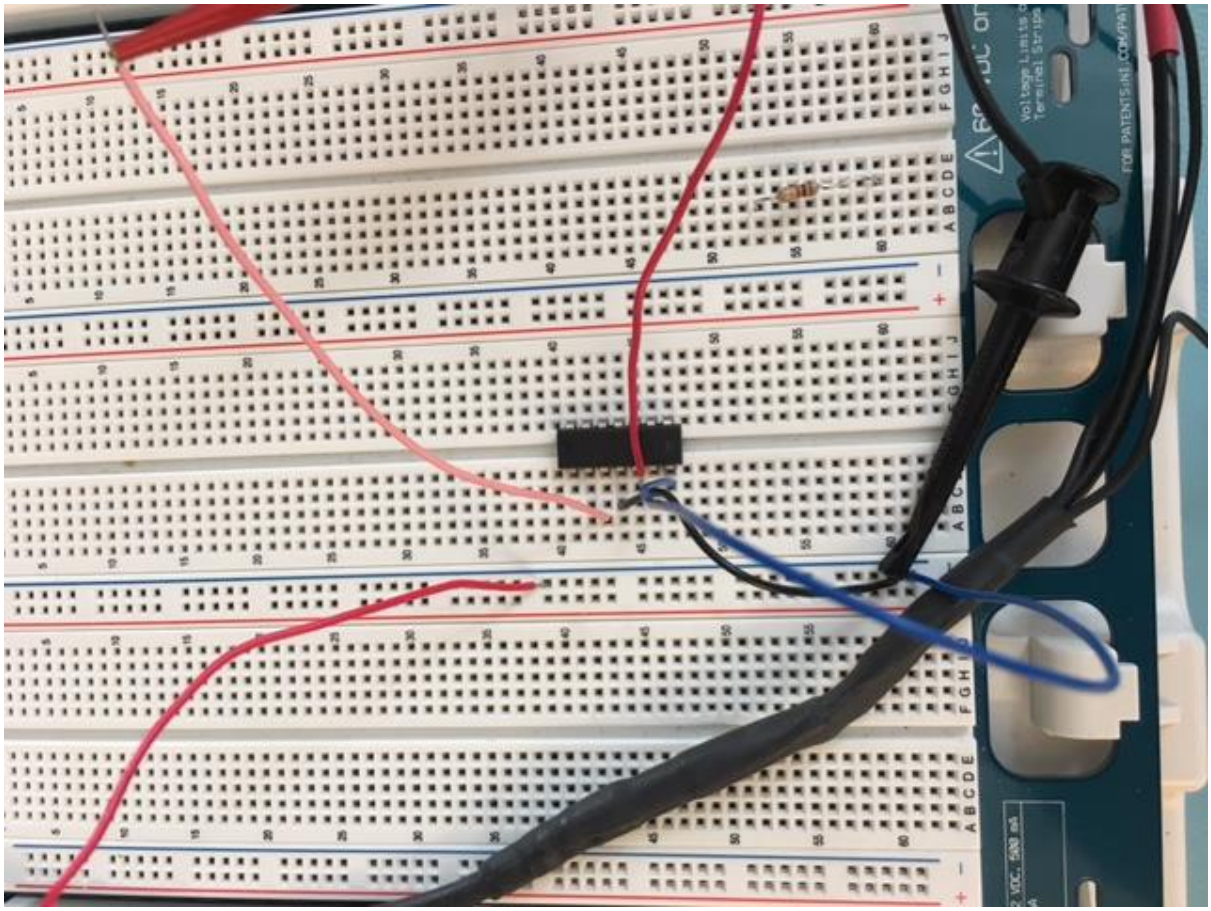


Figure 13: Setup of the IC.

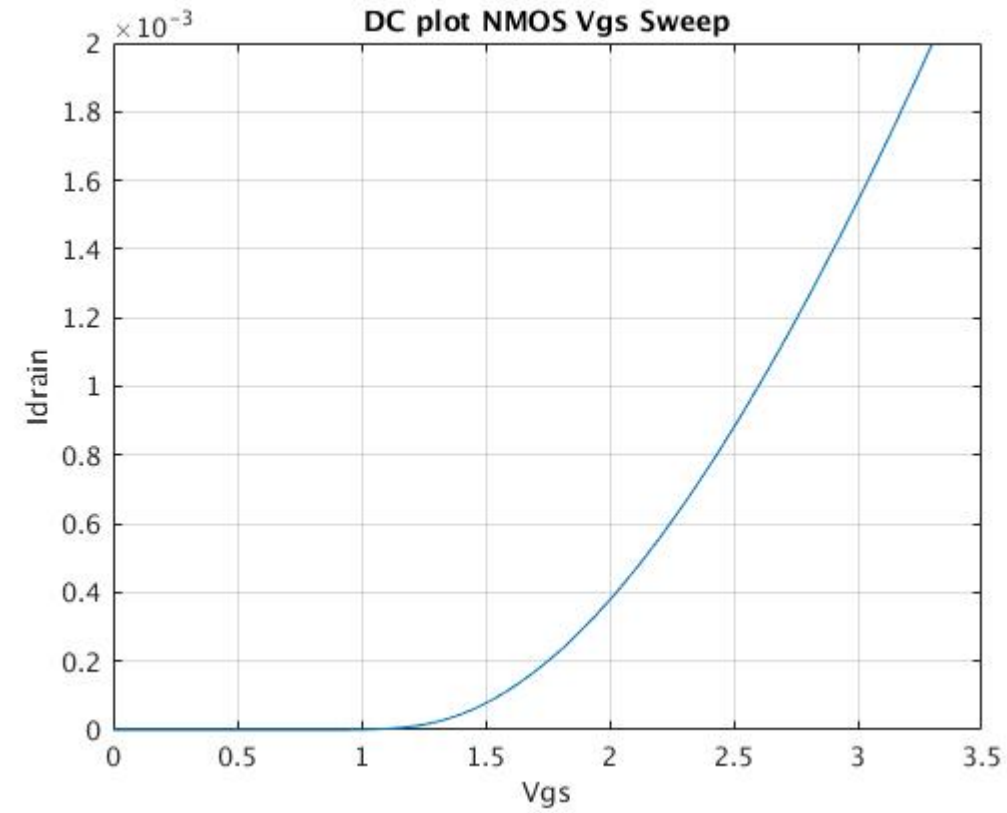
Pin 3: Gate → Sweep voltage

Pin 4: Source → GND

Pin 5: Drain → VDD

The data-sheet did not provide a voltage for the threshold, but by sweeping the voltage as a function of the function of the drain current, we can estimate the threshold voltage.

The threshold seems to be 1V. If so, then the active region is from V_{gs} = 1V to V_{gs} = 4.3V (V_{ds} + V_{to}) 100 measurement points in each plot.



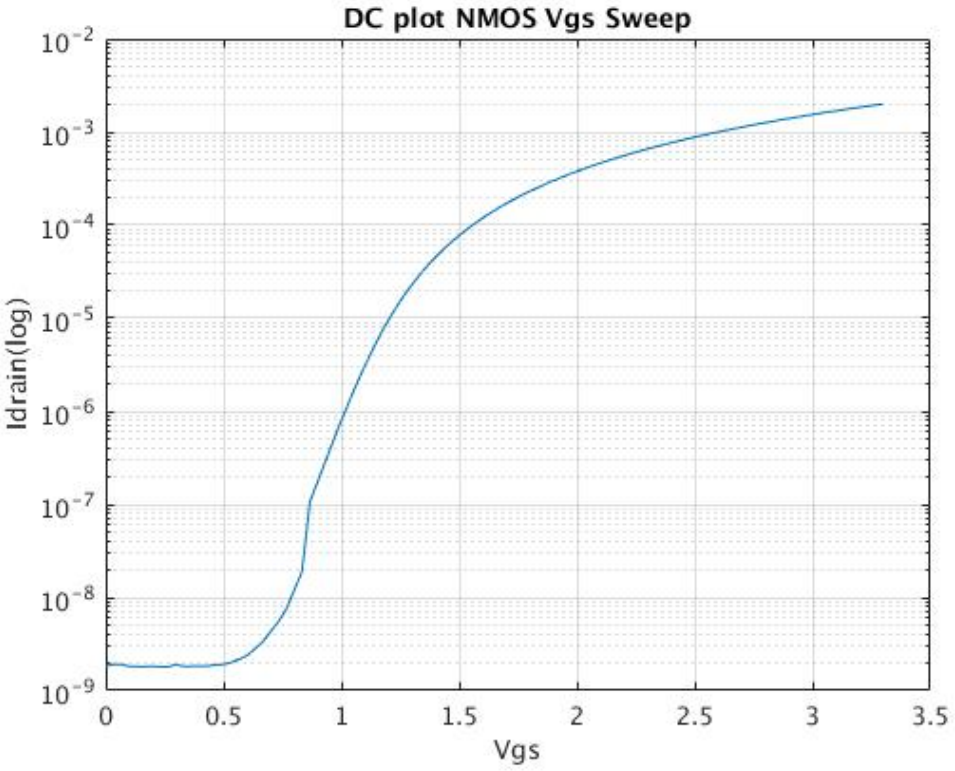


Figure 14: Plot in the active region

The Triode region would be wherever V_{gs} is larger than $V_{ds} + V_{to}$.

We supplied Vds with 1V, in this case the plot enters triode region when V_{gs} traverses to 2V

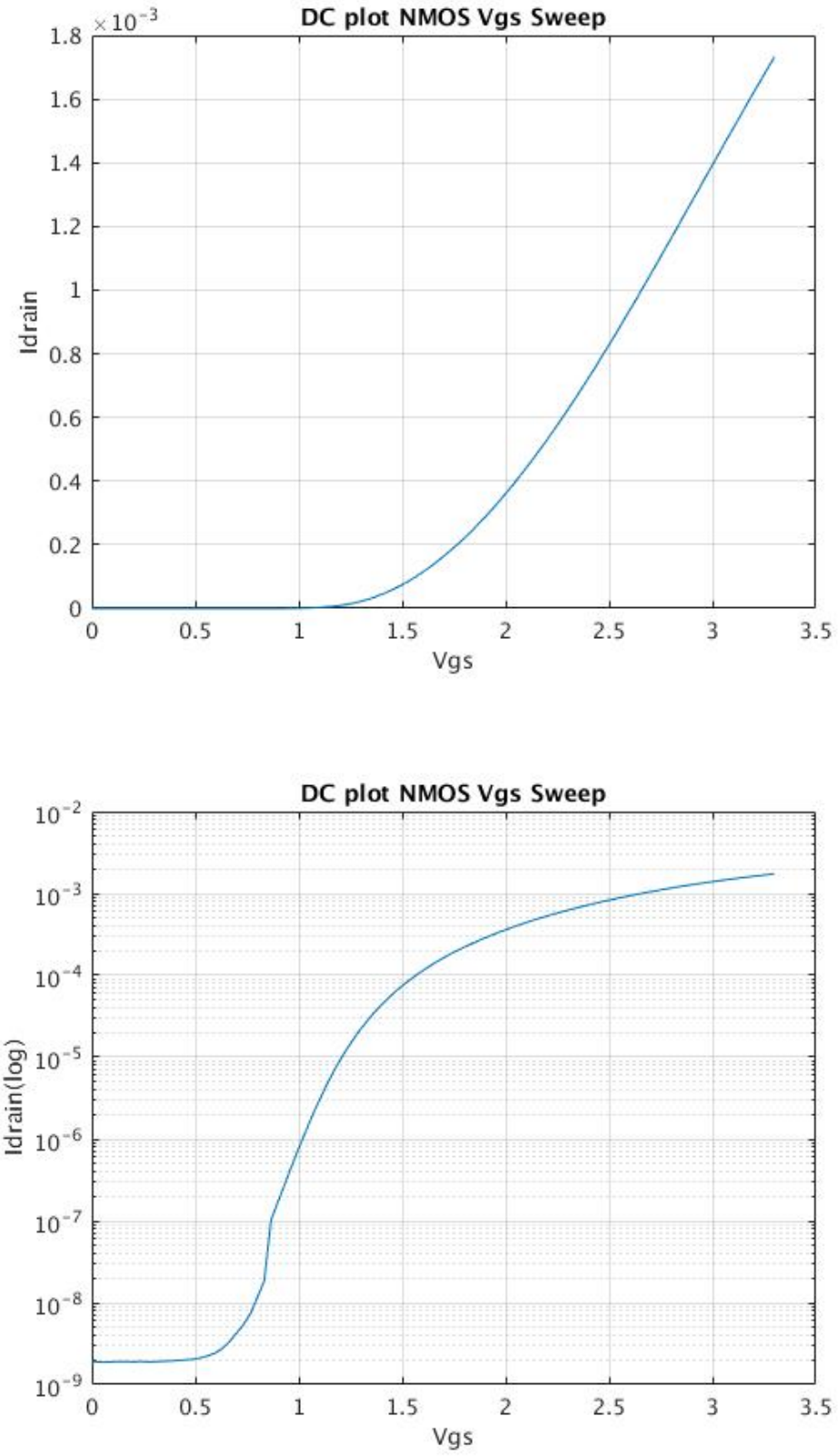


Figure 15: Plot in the triode region

As the EKV-output shows, the measurements of the physical IC shows similar characteristics. The active region (figure 14) shows a quadratic plot, and the triode region (figure 15) shows a quadratic plot up to 2 V where it changes to a linear plot

Here V_{gs} had 7 values ranging from 1.1V (V_{to} + 100 mV) to 3.3V

V_{ds} was swept from 0 to 3.3V

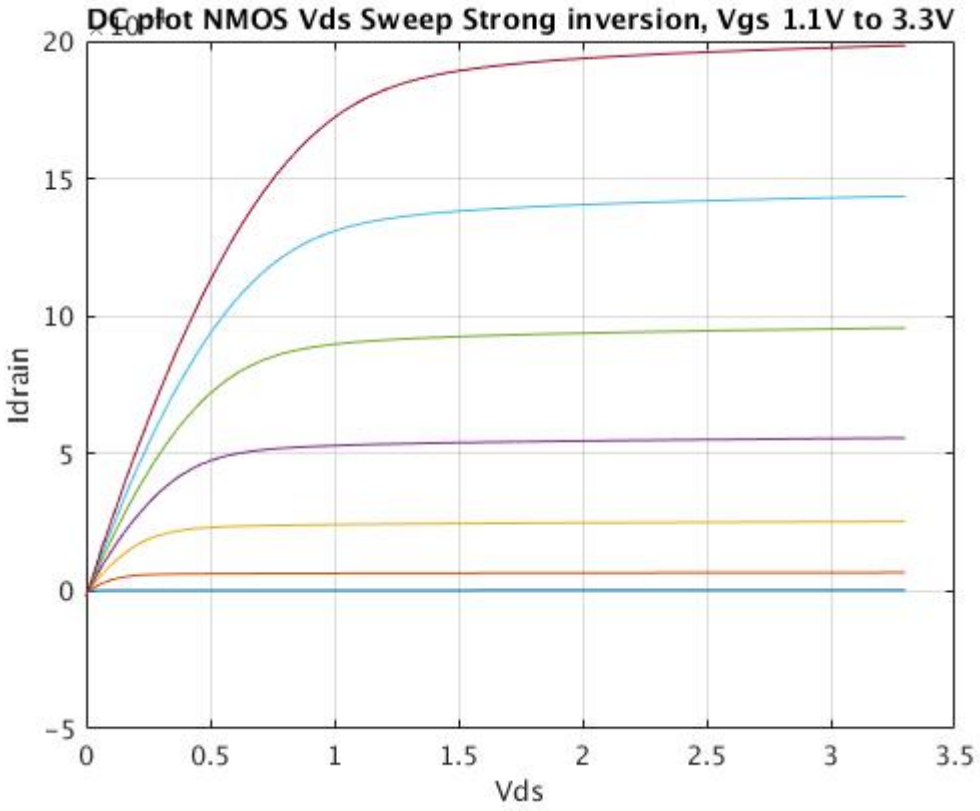


Figure 16: Id as a function of VDS in strong inversion (10e-4)

To sum up, figure 16 shows that:

1. Cutoff
   To operate an enhancement type MOSFET, we first must induce the channel. For NMOS, this means that

   $V_{GS} \geq V_{TO}$

   If $V_{GS} < V_{TO}$ there is no channel and the device is cutoff, ass seen in figure 16, when this is true, ID=IS=0

2. Triode. To operate in this mode, the channel must first be induced. V_{DS} must be small enough so the channel is continuous
   $V_{GD} > V_{TO}$. Another way to express the triode region: $V_{DS} < V_{GS}-V_{TO}$
3. Saturation. As mentioned above, the channel must be induced. $V_{DS} \geq V_{TO}$(Induce)
   Then the channel must be pinched off at the drain end: $V_{GD} \leq V_{TO}$ (Pinch off) or $V_{DS} \geq V_{GS}-V_{TO}$

Here V_{gs} has 7 values ranging from 0 to 0.9V

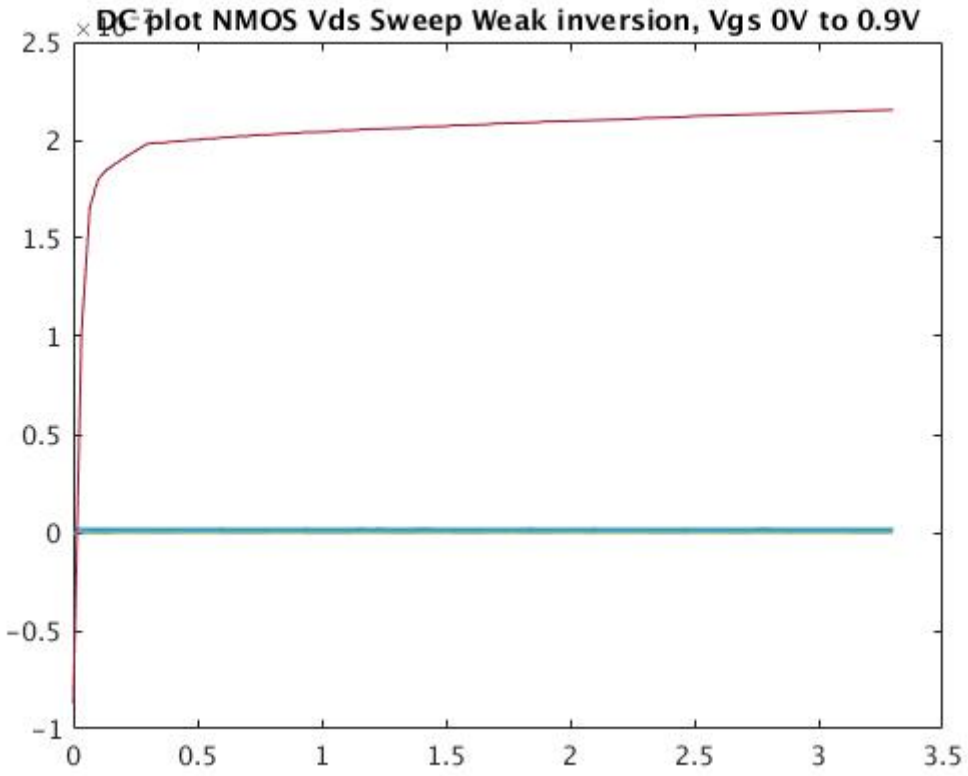
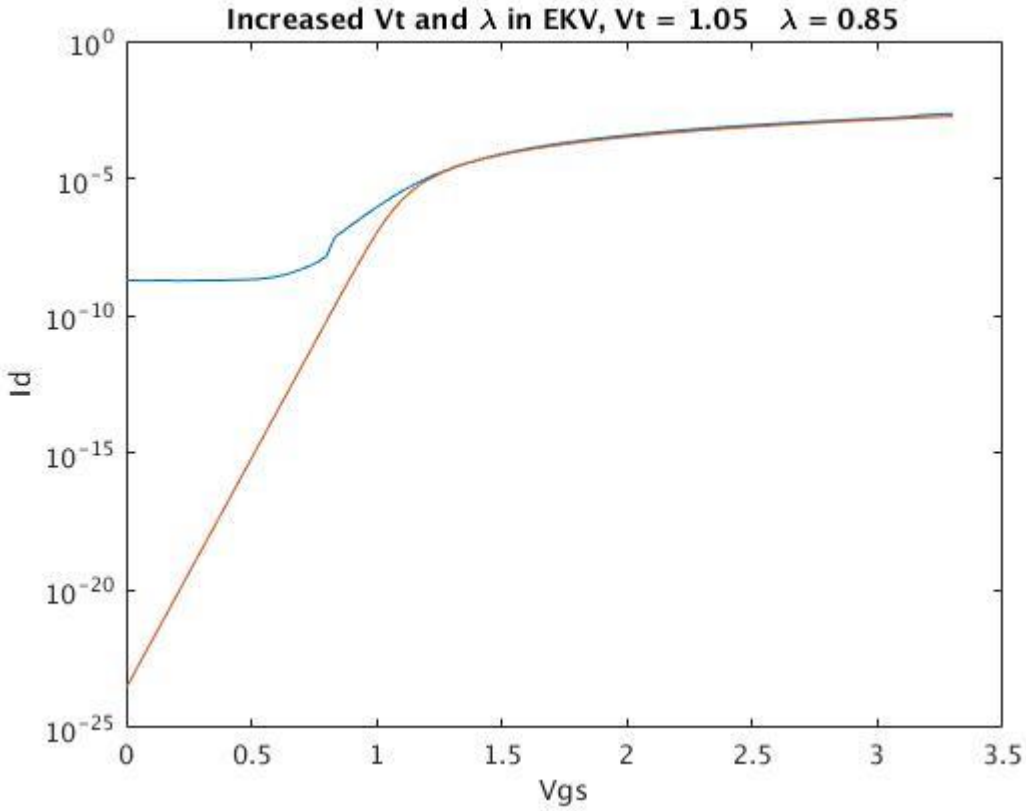


Figure 17: Sweep over weak inversion

There's only one value (0.9V) of V_{gs} that gave any real plot the others were virtually 0.

Task 5

Here the Lambda was changed to 0.85 and threshold voltage to 1.05V



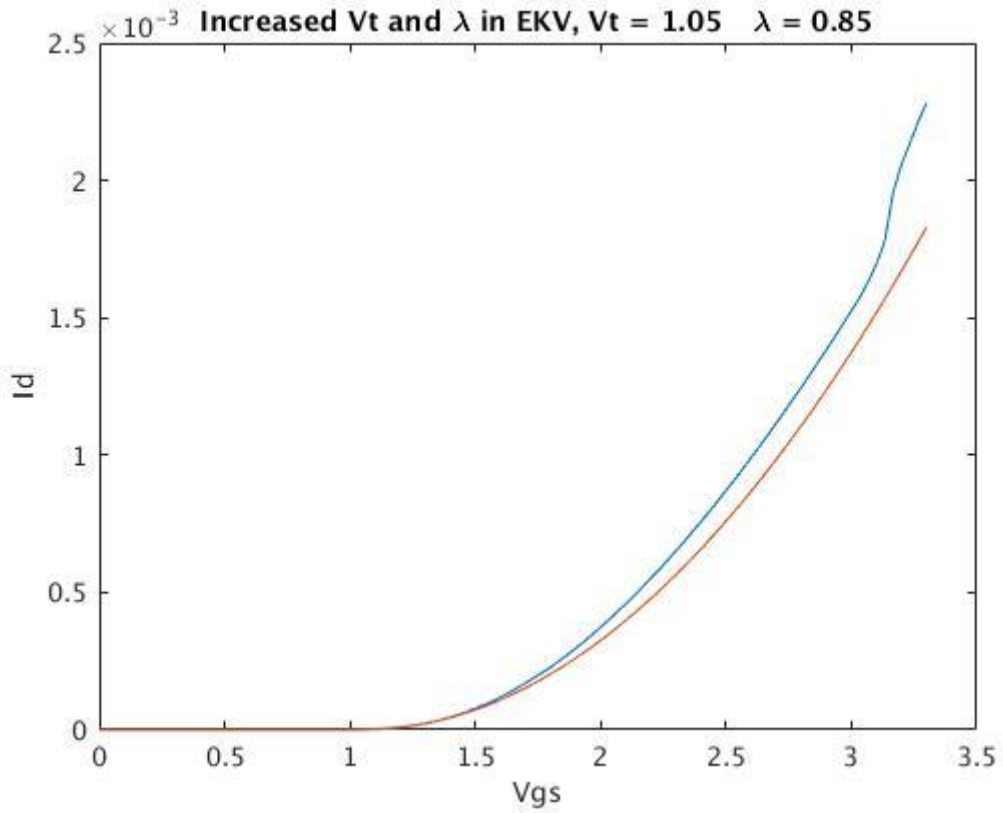


Figure 18: Modified EKV to match the measurement of a physical IC

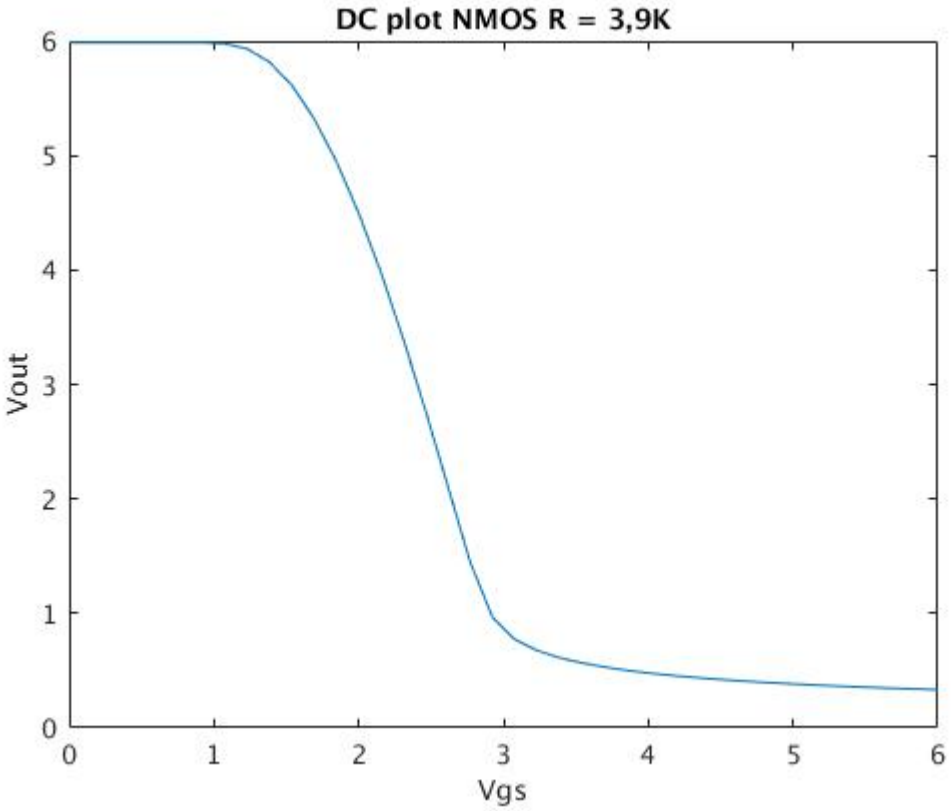
This is the best fit that could be produced. The red line is from the EKV and is fairly similar to the measured IC taking to the account that the EKV-model is very simple with minimal factors to create a model.

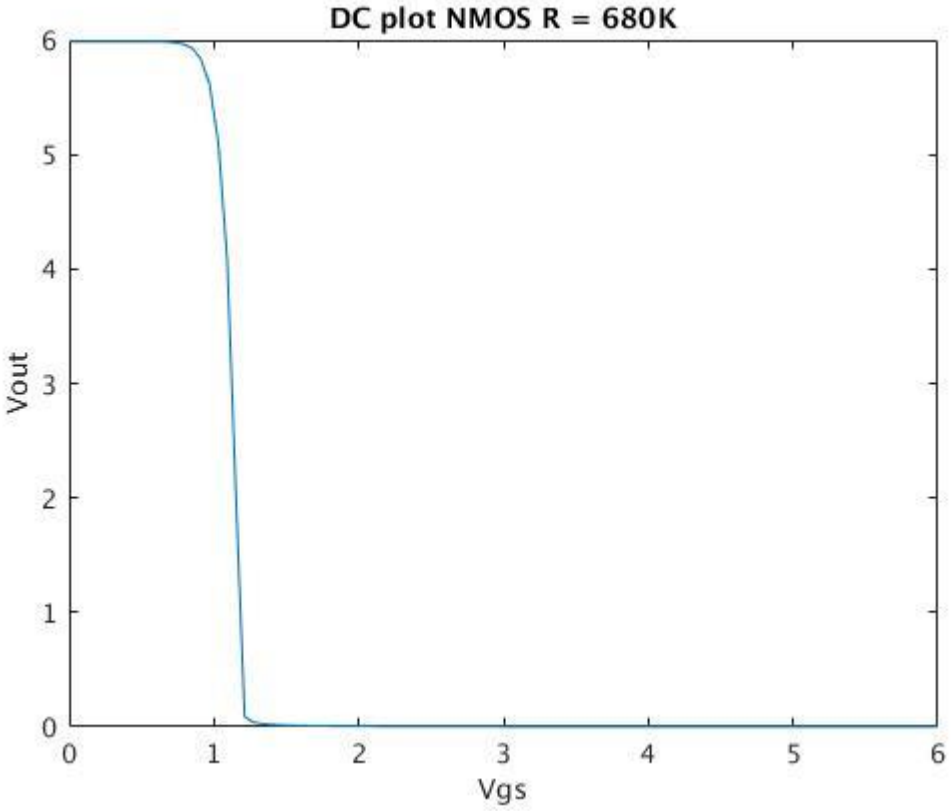
The cadence model is a better way of simulating NMOSFET than the EKV, this is because it is more accurate and incorporate more factors.

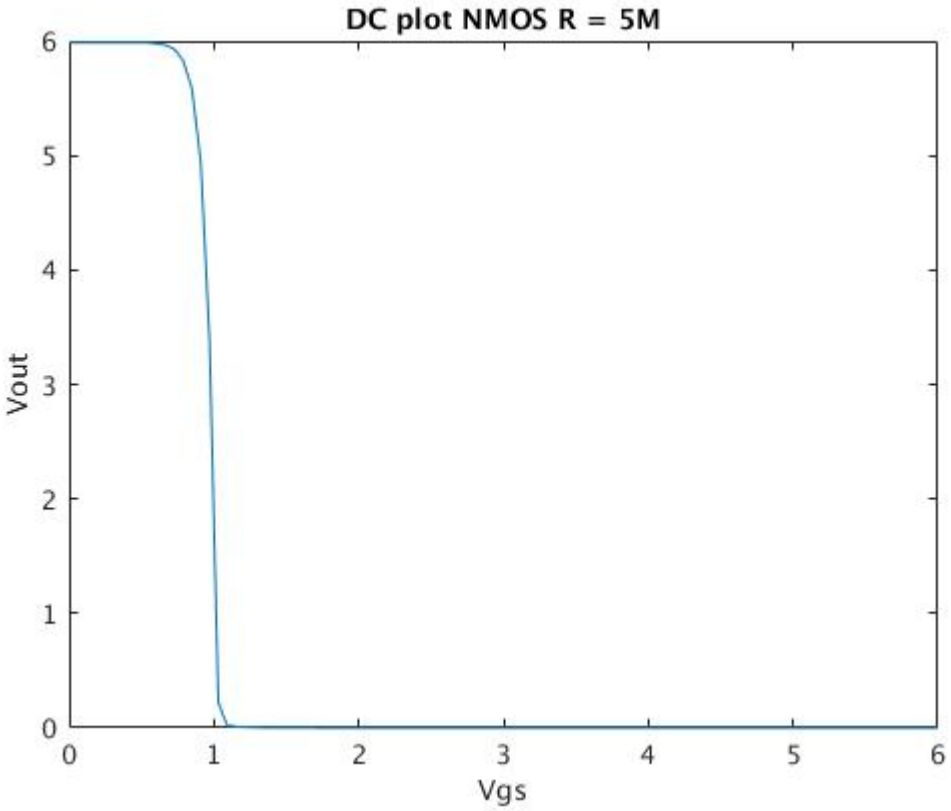
Task 6 Common Source Amplifier

The goal of this task is to construct a simple Common Source Amplifier and vary the resistor from kΩ to MΩ, and compare the behaviour.

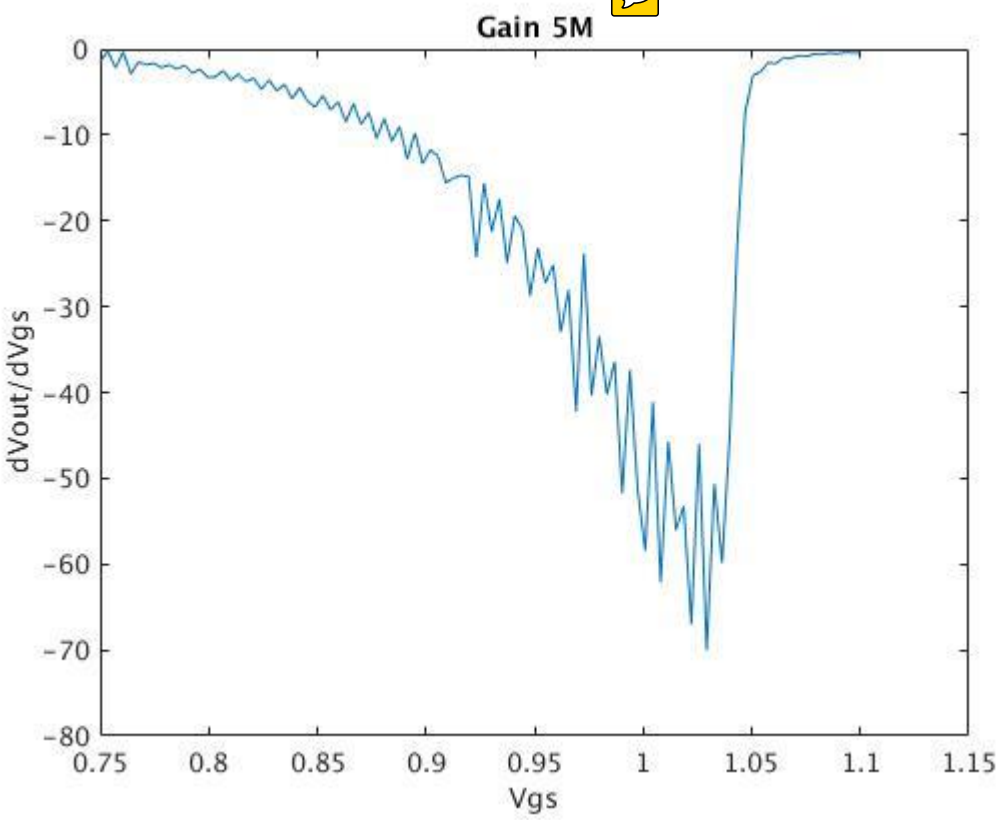
The common source amplifier is one of three amplifier topologies, used as a voltage or transconductance amplifier.


DC plot NMOS R = 3,9K
Vout
Vgs
0
1
2
3
4
5
6


DC plot NMOS R = 680K
Vout
Vgs
0
1
2
3
4
5
6


DC plot NMOS R = 5M
Vout
Vgs
0
1
2
3
4
5
6

The higher the resistor the steeper is the transition from cut-off to saturation, and the best resistor to choose in this case is R = 3.9 k.



The gain of the Common Source amplifier when a large resistor (5M) is chosen is about 70

A = - gm(R||rds)

If we chose a large R in order to have a high voltage gain Rout will be large as well. Typical values for Rout are 100 kOhm. This is not always good. Imagine that we connect a device – a load, such as speaker to the amplifier. We assume that the load is high, meaning that the resistance of the speaker is low (e.g. 8 Ohm) so that the amplifier needs to produce high currents to increase the load voltage. The higher the resistance, the lower Id is gained.

The bandwidth of the common source amplifier tends to be low due to the high capacitance resulting from the Miller effect. The Gate-Drain capacitance is multiplied by the factor $1+A_V$ which leads to a higher input capacitance end thusly reducing the overall bandwidth. This means that the lower the resistor, the higher bandwidth.