INF3410 - Analog Microelectronics

Mandatory Labratory Exercise 2

Characterizing Field Effect Transistors

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1 Introduction

In this lab we are looking at the nMOSFET transistor, characterizing its different regions, and looking at the drain current for each of these regions. In figure 1 we see the nMOS transistor, marked with its drain, gate and source, along with V_{ds}, V_{gs} and I_D, which we will be looking closely at in this lab.

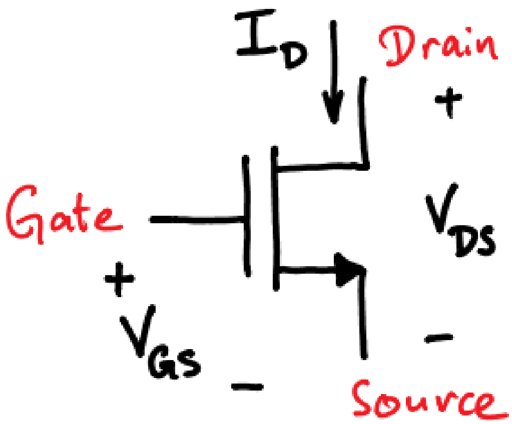


Figure 1: Diagram of an nMOS transistor with gate, source, drain and drain current

The nMOS transistor can be characterized by four regions of operation:

1 Weak inversion, active/saturation region:
$V_{gs} < V_{tn}$
$V_{ds} \geq V_{D_{sat}}$
$V_{D_{sat}} \approx 4V_T$
$4V_T \approx 4 \cdot 26mV = 104mV$

2 Weak inversion, triode/linear region:
$V_{gs} < V_{tn}$
$V_{ds} < V_{D_{sat}}$
$V_{D_{sat}} \approx 4V_T$
$4V_T \approx 4 \cdot 26mV = 104mV$

3 Strong inversion, active/saturation region:
$V_{gs} \geq V_{tn}$
$V_{ds} \geq V_{D_{sat}}$
$V_{D_{sat}} = V_{OV}$
$V_{OV} = V_{gs} - V_{tn}$

4 Strong inversion, triode/linear region:
$V_{gs} \geq V_{tn}$
$V_{ds} < V_{D_{sat}}$
$V_{D_{sat}} = V_{OV}$
$V_{OV} = V_{gs} - V_{tn}$

This is also illustrated in figure 2. We are using the nMOS transistor, but the principle is the same for all FET transistors.

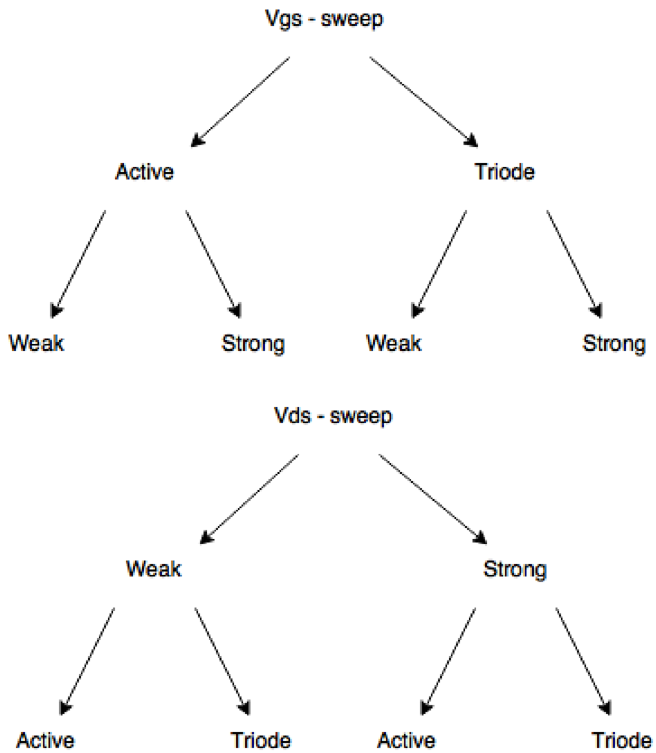


Figure 2: Diagram of regions of a FET transistor

2 EKV Model Calculation of a nMOS Transistor

2.1 Intro

We will in this task model a nMOS transistor in MATLAB using the EKV model:

$$I_D = i_F - i_R$$
$$i_{F(R)} = I_S \ln[1 + e(\frac{v_G - V_{tn} - n v_{S(D)}}{n V_T})]^2 (1 + \lambda V_{ds}),$$

where $I_S = 2n\beta V_T^2$ and with the simplifying assumption that $V_S = V_B = 0$ V.

2.2 Procedure

We are going to produce a number of plots for the nMOS transistor, one for each of the regions.

2.2.1 V_{ds} in Active region

We want to plot I_D as a function of V_{gs} in the active region, by sweeping V_{gs} from 0 to Vdd. We want a curve with both linear and logarithmic y-axis. For this we use $V_{ds} = V_{DD}$.

2.2.2 V_{ds} in Triode region

We want to plot I_D as a funcion of V_{gs} in the triode region, by sweeping V_{GS} from 0 to V_{DD}. We want a curve with both linear and logarithmic y-axis. For this we set $V_{ds} < V_{D_{sat}}$, where $V_{D_{sat}}$ in the weak inversion region is $\approx 4V_T$. We therefore set $V_{ds} = V_T$. We choose the $V_{D_{sat}}$ in weak inversion, since $V_{D_{sat}}$ in weak inversion is of a lower value than $V_{D_{sat}}$ in strong inversion.This way we get a plot in both weak and strong inversion.

2.2.3 V_{gs} in Strong inversion

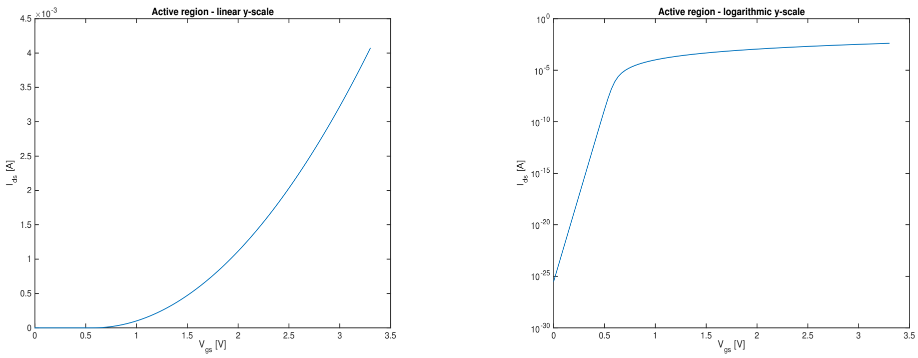
We want to plot I_D as a function of V_{ds} in strong inversion, by sweeping V_{ds} from 0 to V_{DD}. We want to plot for 5 different V_{gs}. For this we chose $\forall V_{gs} : V_{gs} > V_{tn}$.

2.2.4 V_{gs} in Weak inversion

We want to plot I_D as a function of V_{ds} in weak inversion, by sweeping V_{ds} from 0 toV_{DD}.We want to plot for 5 different V_{gs}. For this we chose $\forall V_{gs} : V_{gs} < V_{tn}$.

2.3 Results and Observations

2.3.1 V_{ds} in Active Region



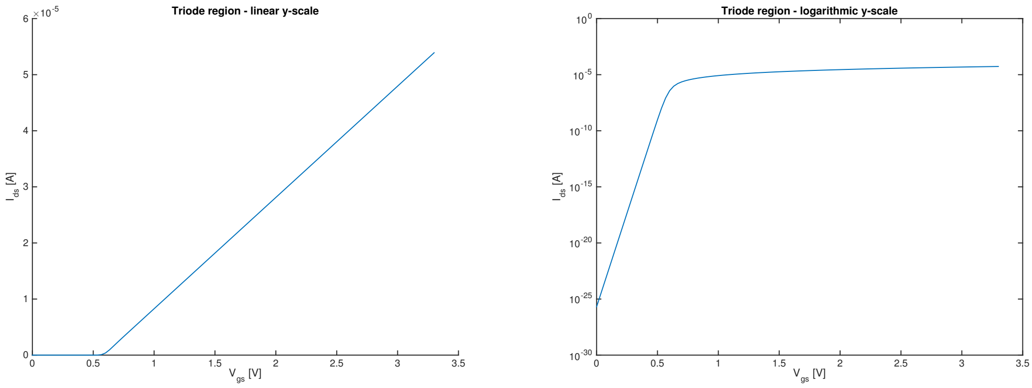
(a) Linear scale (b) Logarithmic scale

Figure 3: EKV: I_D as a function of V$_{gs}$ of a nMOS transistor in the active region.

We can observe from the graph in figure 3a that the current I_D grows exponentially. This is a sign that we are observing the active region. It is possible to stay within the active region at all times by choosing $V_{ds} = V_{DD}$. This ensures us that we will always have $V_{ds} > V_{D_{sat}}$. To be in the active region, the only demand is that the drain-source voltage is larger than the saturation voltage, whereas $V_{D_{sat}}$ is given by (1).

$$V_{D_{sat}} = \begin{cases} V_{gs} < V_{tn} : & 4V_T \\ V_{gs} \geq V_{tn} : & V_{OV} = V_{gs} - V_{tn} \end{cases} \tag{1}$$

2.3.2 V_{ds} in Triode Region



(a) Linear scale (b) Logarthmic scale

Figure 4: EKV: I_D as a function of V$_{gs}$ of a nMOS transistor in the active and triode region.

From the graph in figure 4a, we can observe that the current I_D grows linearly. This signifies that we are observing the triode/linear region, where linear seems to be a fitting name. We can ensure that we are working within the triode region, by ensuring that $V_{ds} < V_{D_{sat}}$. So when $V_{ds} < 4V_T$, it will be in the triode region at all times. If we compare the triode region to the active region in figure 5, we see that the active region has a much higher value for I_D than the value for I_D in the triode region. The difference is caused by an exponential increase of I_D in the active region, and a linear increase in the triode region. The value $V_{D_{sat}}$ will vary within the domain given in (1).

2.3.3 V_{gs} in Strong Inversion

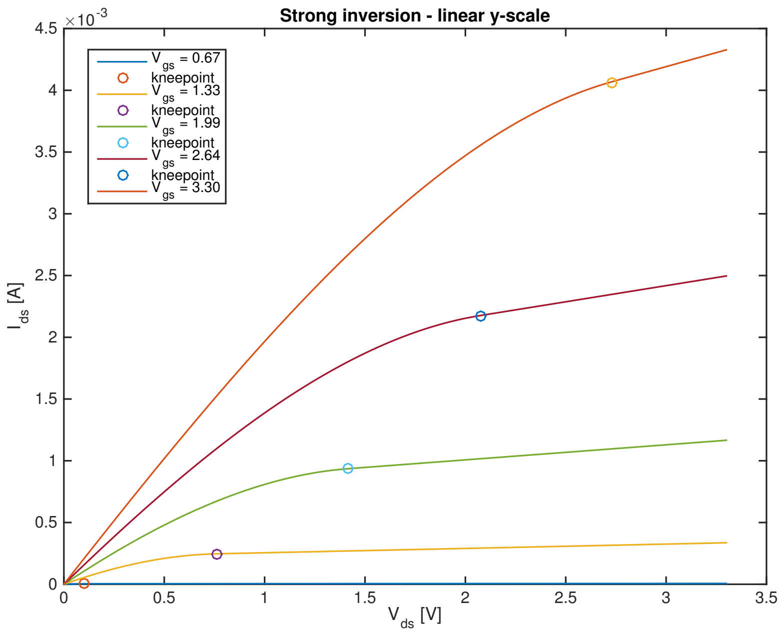


Figure 5: EKV: I_D as a function of V$_{ds}$ of a nMOS transistor in strong inversion.

From the graph in figure 5 we can observe the difference between 5 values of V_{gs} in strong inversion. To ensure the curve is in strong inversion we need to have $V_{gs} \geq V_{tn}$. We have a $V_{tn} = 0.57$ V so the values chosen for V_{gs} is in the range 0.67 to 3.3. We can observe the quadratic behaviour of the knee points by looking at the gap between the curves. The value of the knee points in strong inversion are $V_{D_{sat}} = V_{OV} = V_{gs} - V_{tn}$.

2.3.4 V_{gs} in Weak Inversion

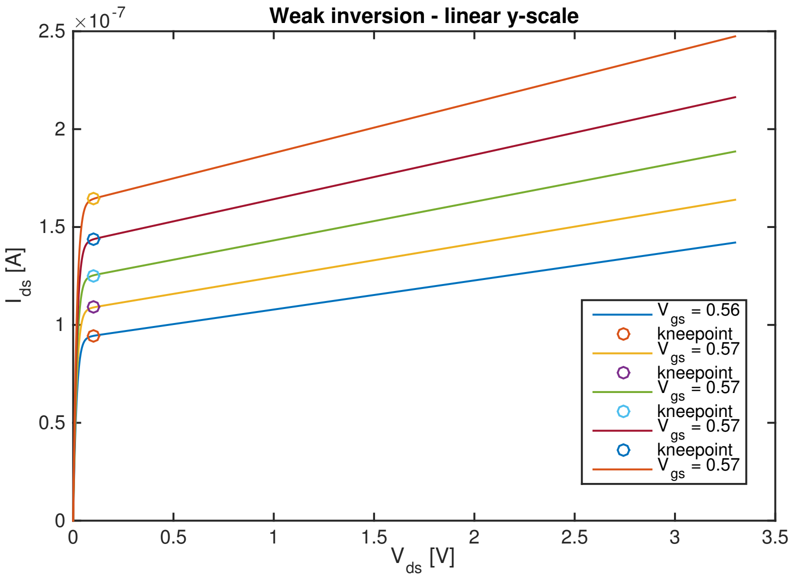


Figure 6: EKV: I_D as a function of V$_{ds}$ of a nMOS transistor in weak inversion.

From the graph in figure 6 we have 5 plots of 5 different V_{gs} values. We also have knee points plotted, which is $V_{D_{sat}}$. By observing the knee points, we notice that they all lie on the same value of V_{ds}, thus making the knee points constant. This is the case, because the value of $V_{D_{sat}} \approx 4V_T$ in weak inversion. We can also see from the graph that the increase in I_D for each change in V_{gs} behaves linearly, instead of an exponential increase like in strong inversion, in section 2.3.3. We can assure that we are in the region of weak inversion by only choosing values of V_{gs} that are close to V_{tn}.

3 Cadence simulation of a nMOS transistor

3.1 Intro

We will now repeat the procedure done in section 2 in a Cadence simulation of a $0.35\mu m$ process CMOS nFET. The schematics for the simulation is shown in figure 7.

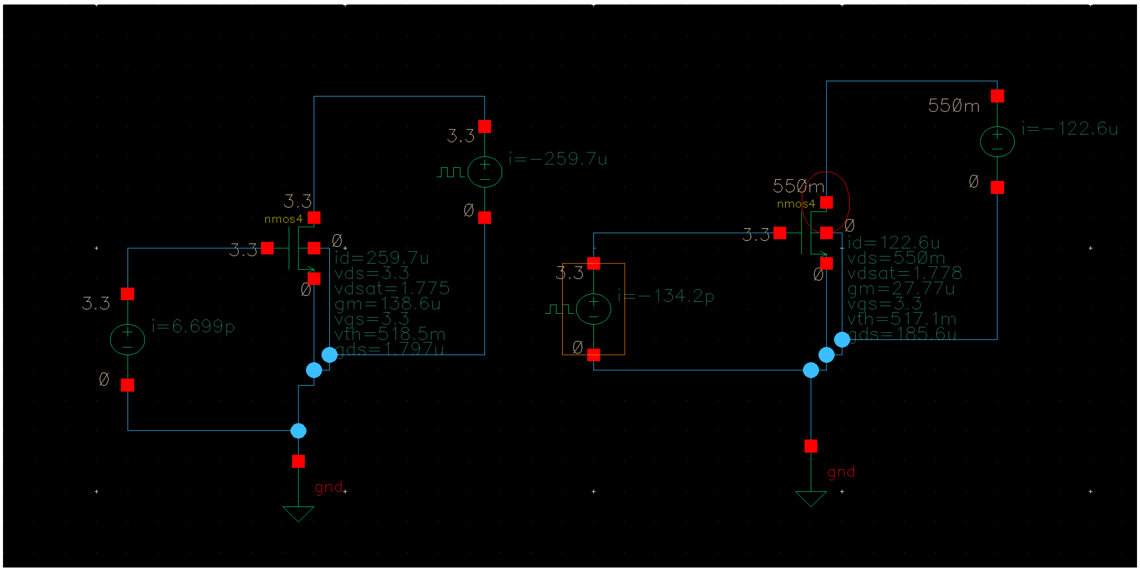
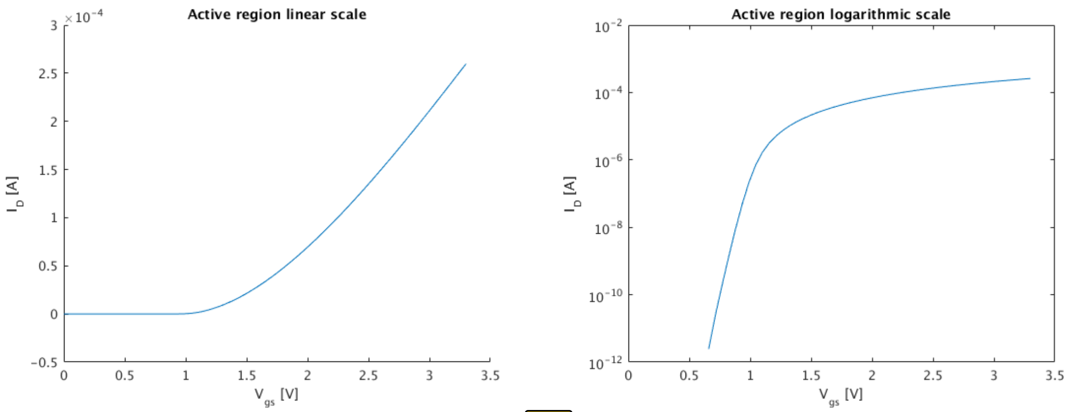


Figure 7

3.2 Results and Observations

3.2.1 V_{ds} in Active Region



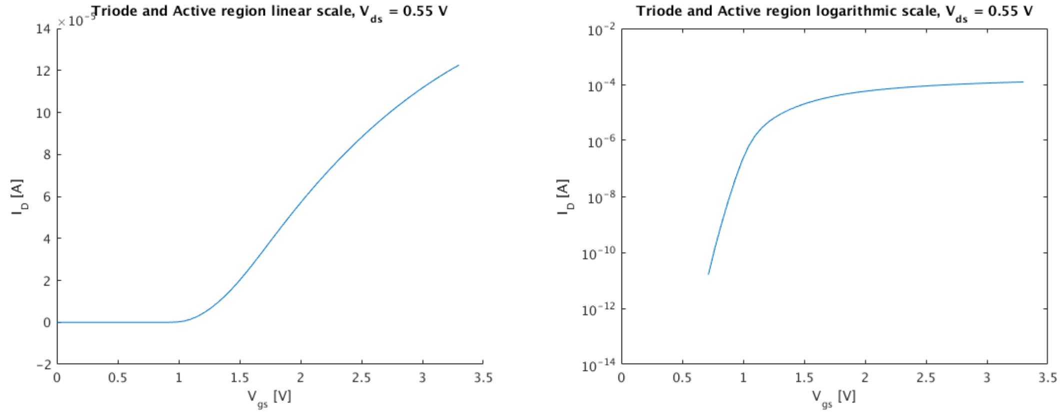
(a) Linear scale

(b) Logoarthmic scale

Figure 8: Cadence: I_D as a function of V$_{gs}$ of a nMOS transistor in the active region.

By observing the graph in figure 8a, we notice that the value of I_D behaves exponentially. If we compare the results we get from Cadence, and our MATLAB simulation in section 2.3.1, we can observe that both graphs have a similar increase, but different values for I_D. The difference in the two plots can be explained by the amount of variables used in Cadence, as it takes into account a lot of variables that our MATAB simulation ignores. We have ensured that by choosing a $V_{ds} = V_{DD}$.

3.2.2 V_{ds} in Triode Region



(a) Linear scale

(b) Logoarthmic scale

Figure 9: Cadence: I_D as a function of V$_{gs}$ of a nMOS transistor in the active and triode region.

If we observe the graph in figure 9a, we can see that the value of I_D is almost linear, but behaves somewhat logarithmic. This behaviour is most likely caused by our choice of $V_{ds} = 0.55V$ in Cadence. Our choice will result in a start in the active region, which then moves over to the triode region at $V_{ds} \leq V_{OV}$. At this point, which is approximately at $V_{gs} \approx 1.5V$, the graph will behave more linearly, and therefore result in the graph having a bump, and looking like it behaves somewhat logarithmic. If we compare our Cadence simulation of the triode region to the simulated MATLAB triode region in section 2.3.2, we see that they have almost the same shape, the biggest difference would be the I_D value of the plots, as the Cadence simulation still takes into account more factors than the MATLAB simulation. The other difference in the plots comes from the different choices of V_{ds} for the two situations.

3.2.3 V_{gs} in Strong Inversion

If we observe the graph in figure 10, we notice that the simulation of strong inversion given by Cadence has a much lower value for I_D than that given by MATLAB. This is caused by the extra factors of Cadences functions. One other difference in the graphs, is the location of the knee points. The knee points in the Cadence simulation are on a lower value of V_{ds} than the MATLAB equivalent. The difference in knee points could be caused by the extra factors that Cadence uses, as well as a difference in V_{tn} for the simulation. The V_{tn} that we used in the section 2 was larger than the given V_{tn} in the Cadence program.

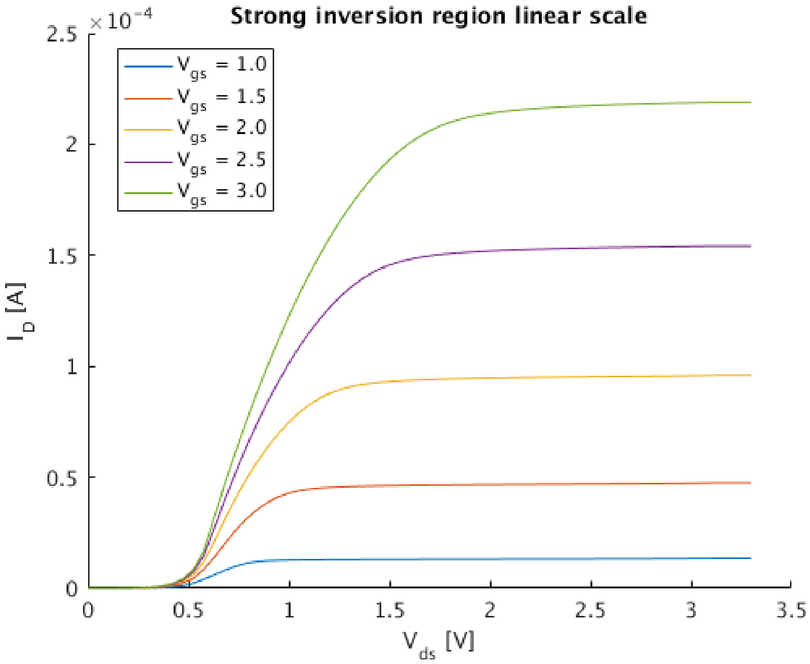


Figure 10: Cadence: I_D as a function of V$_{ds}$ of a nMOS transistor in strong inversion.

3.2.4 V_{gs} in Weak Inversion

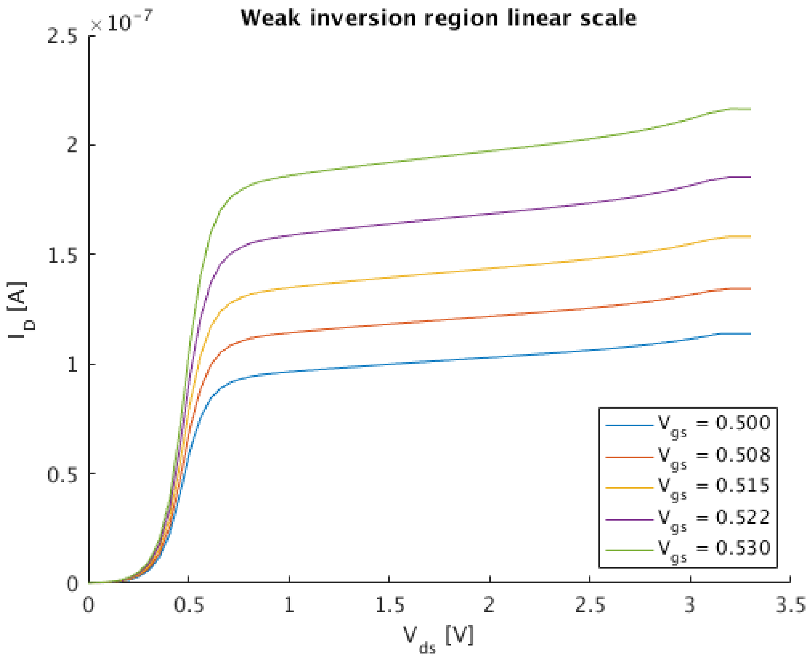


Figure 11: Cadence: I_D as a function of V$_{ds}$ of a nMOS transistor in weak inversion.

By observing the graph in figure 11, we notice that the value of I_D is in the same range as in section 2.3.4. This shows us that when the Cadence program enters weak inversion, the difference made by the extra factors decreases for weak inversion. We also notice that the different V_{gs} will only give a slight increase in I_D and that the knee points of the different values of V_{gs} are at approximately the same point. If we compare the plot to the plot in section 2.3.4, we will see that the biggest difference is where the I_D rises the most. This is most likely caused by a difference in the formulas used to calculate I_D.

3.3 Fitting Cadence with EKV Model

3.3.1 Intro

We want to compare the difference between the Cadence simulation and EKV model in section 2.

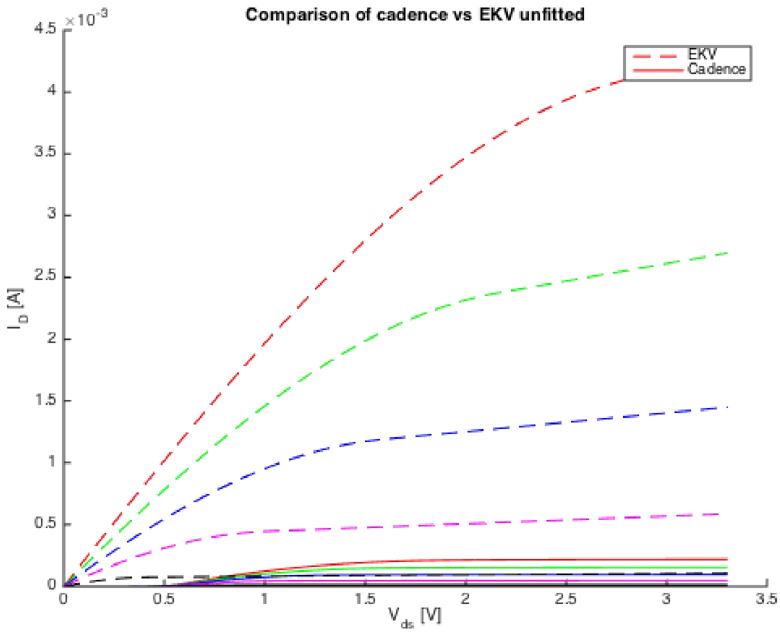
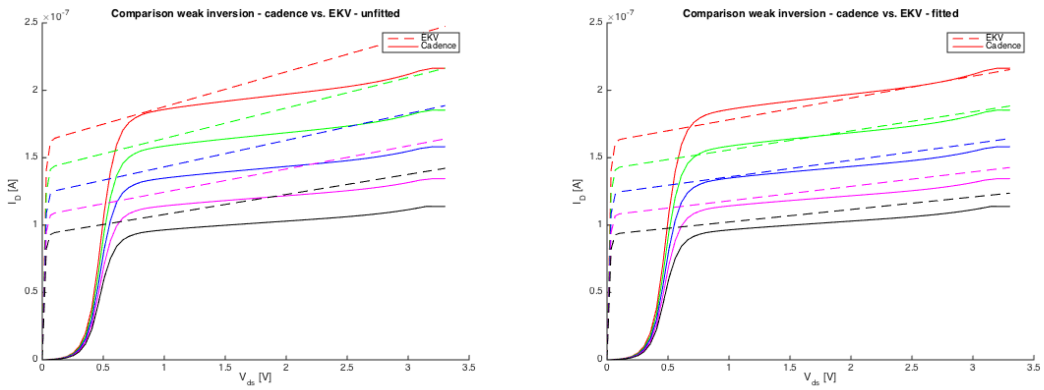


Figure 12: Comparison of I_D-V_{ds} characteristic of nMOS in strong inversion – EKV vs. Cadence

3.3.2 Results and Observations

We have plotted the simulation with the EKV model and the Cadence simulation in the same plot in figure 12. We observe that the value of I_D in the Cadence simulation is one decade lower than the I_D in the EKV model. We want to try and tune our EKV model to achieve a good fit with the Cadence simulation. Because of the difference in I_D we decided to use the plot in weak inversion when tuning the EKV model to achieve a fit with the Cadence simulation. The plots in weak inversion have the same scale. The results from Cadence and EKV model in weak inversion are plotted together in figure 13a. We experimented with tuning the different parameters β, λ and V_{tn}. Since the plots are in weak inversion, changing V_{tn} did not make any difference so we kept it at the value from the Cadence simulation. $V_{tn} = 0.519V$. Changing the value of β moves the graph in the up and down direction, but the plots were at the same level so we kept $\beta = 190\mu\frac{A}{V^2}$. Decreasing the parameter λ tilts the slope of the graph so we set $\lambda = 0.1V^{-1}$ to fit the two slopes. The fitted result can be seen in figure 13b.



(a) Unfitted (b) Fitted

Figure 13: Comparison of I_D-V_{ds} characteristic of nMOS in weak inversion – EKV vs. Cadence

3.4 Comments

We realised after the simulation that we should have used a $V_{ds} < 4V_T$ in section 3.2.2 in order to achieve a plot purely in the triode region in figure 9. We therefore have a plot with both triode and active region.

4 Measurement of a nMOS transistor

4.1 Intro

For this task we are making the same transistor characteristics as in section 2 and 3, but we are now measuring the current I_D. For this measurement we are using the integrated circuit CD4007UBE, which is equivalent to MC14007UBCP, at least in the pin assignments. We use MATLAB for setting and sweeping the power supplies. We first set up for a sweep of V_{gs}, thereafter V_{ds}.

4.2 Procedure

4.2.1 Sweep of V_{gs}

We begin by setting up the ELVIS board in accordance with figure 14. Here we use the variable power supply to set V_{ds}, and an external power supply to sweep V_{gs}. We used $V_{DD} = 5$ V For this exercise. For the first sweep to get the active region we set $V_{ds} = V_{DD}$. For the second sweep to get mostly triode region, we set $V_{ds} = 0.5$ V.

4.2.2 Sweep of V_{ds}

For the sweep of V_{ds} we set up the board in accordance to figure 15. Here we use two different, external power supplies, one for sweeping V_{ds}, and the other for setting different values of V_{gs} as we go.

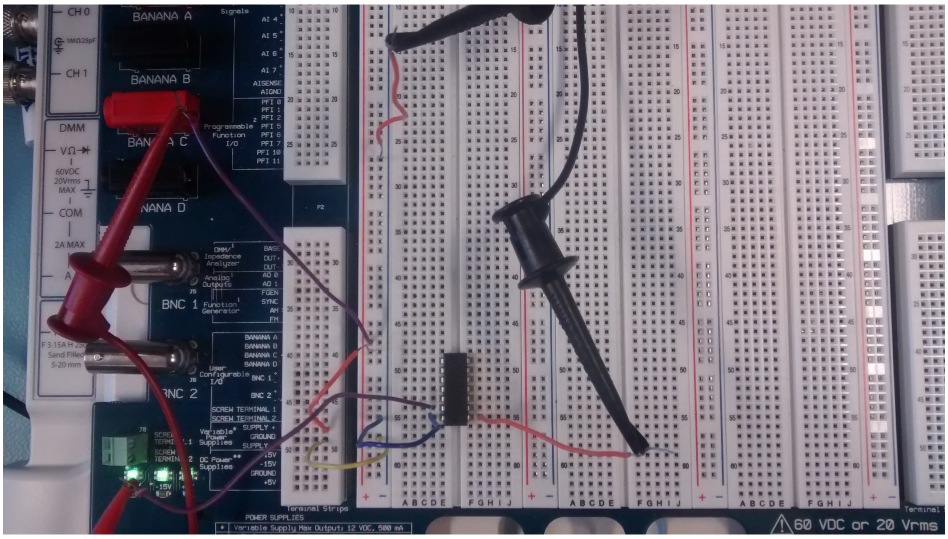


Figure 14: Setup for measurements of V_{gs} sweep.

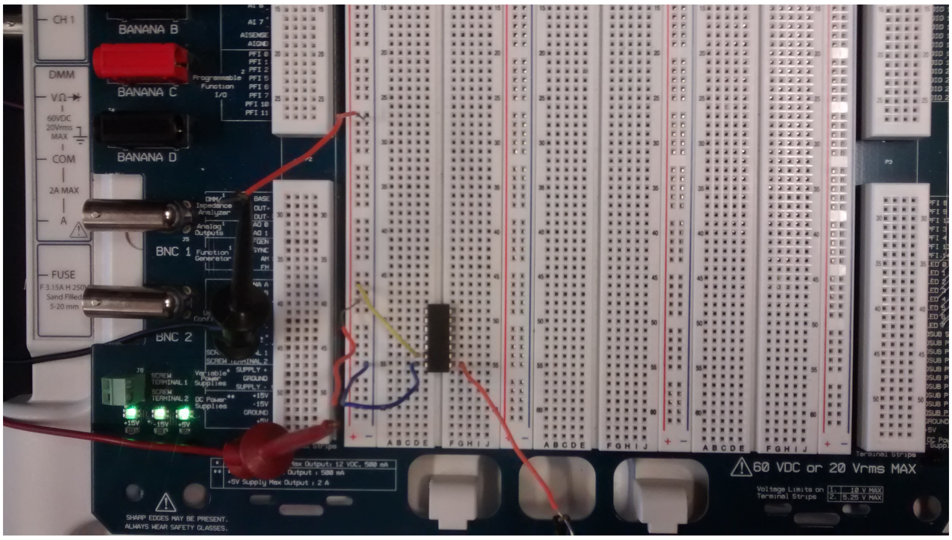
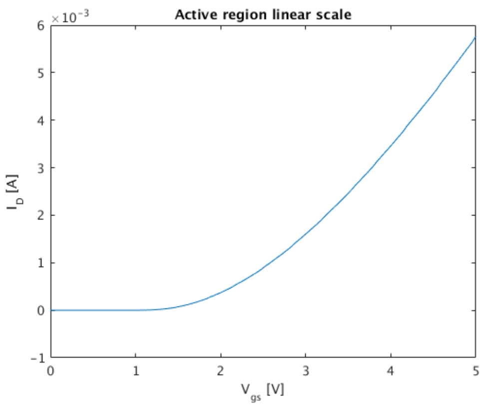


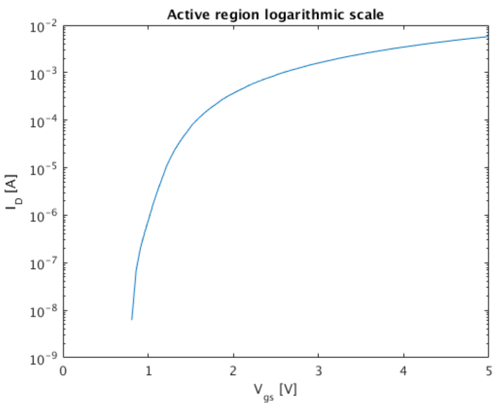
Figure 15: Setup for measurements of V_{ds} sweep.

4.3 Results and Observations

4.3.1 V_{ds} in Active Region



(a) Linear scale

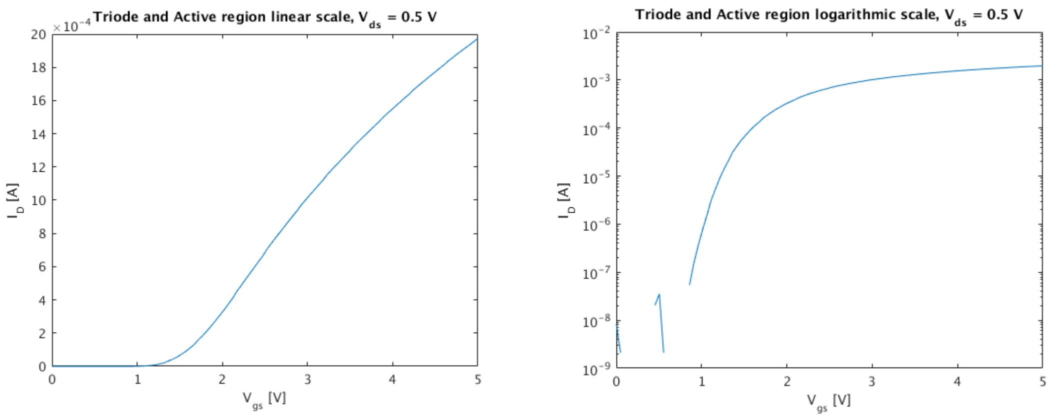


(b) Logoarthmic scale

Figure 16: Measurement: I_D as a function of V_{gs} of a nMOS transistor in the active region.

By observing the graph in 16a, we can see that the shape of the function I_D closely resembles that of the simulated MATLAB function in section 2.3.1. The biggest difference would be the highest point of I_D, but this difference has occurred due to a different choice of interval for V_{gs} and V_{ds}.

4.3.2 V_{ds} in Triode Region



(a) Linear scale

(b) Logoarthmic scale

Figure 17: Measurement: I_D as a function of V_{gs} of a nMOS transistor in the active and triode region.

We see in the graph in figure 17a that the plot closely resembles the Cadence plot in section 3.2.2 in it's shape. This is again due to our choice of V_{ds}. If we compare the plot to the plot in section 2.3.2, we see that the I_D value of the graph is a lot higher, this is due to being slightly in the active region, because of our choice of V_{ds}, and due to a larger interval of V_{gs}.

4.3.3 V_{gs} in Strong Inversion

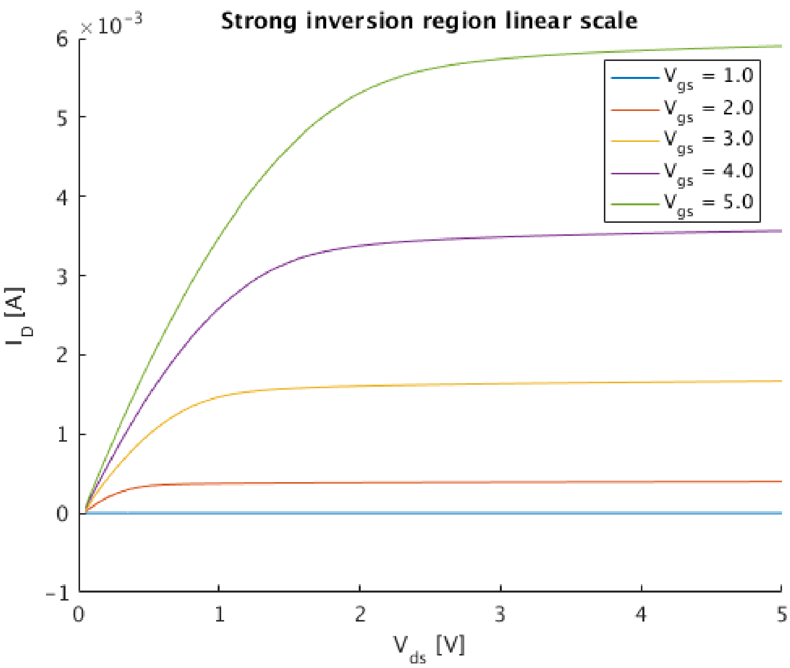


Figure 18: Cadence: I_D as a function of V_{ds} of a nMOS transistor in strong inversion.

The plot for the strong inversion can be seen in figure 18, we can again observe the quadratic behaviour of the knee points as we did in the previous sections. The curve is more similar to the Cadence simulation in section 3.2.3 than the EKV model in section 2.3.3, excluding the fact that the Cadence simulation has a slightly delayed start-up.

4.3.4 V_{gs} in Weak Inversion

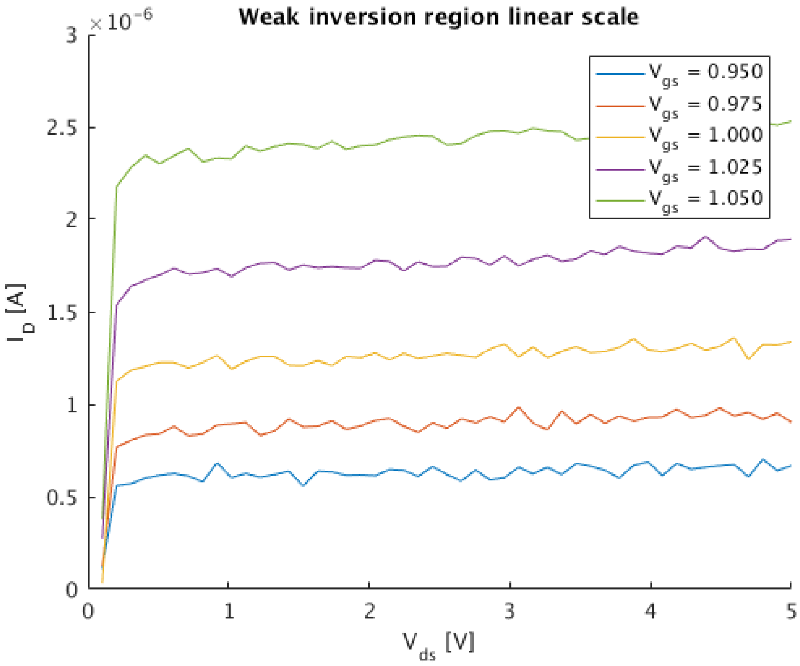


Figure 19: Cadence: I_D as a function of V$_{ds}$ of a nMOS transistor in weak inversion.

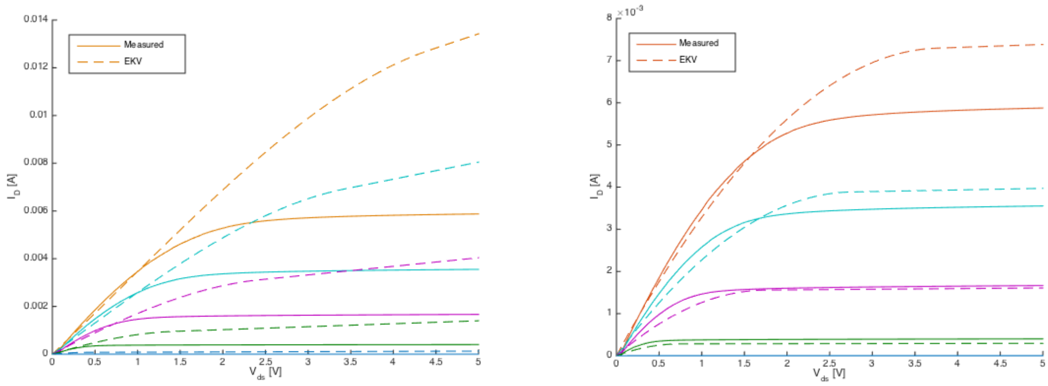
The plot for the weak inversion can be seen in figure 19. We can again see the linear behaviour in I_D for each increase of V_{gs}. The knee points are again approximately at a constant value of V_{ds}.

4.4 Fitting Measurements with EKV Model

In figure 20 we see the unfitted and fitted plot of the EKV model compared to the measured I_D. Here we have again adjusted the parameters β, λ and V_{tn}. Here λ adjusts the skew of the linear region, β adjusts the plots 'left' and 'right', and V_{tn} adjusts the plots 'up' and 'down'. The parameter values are shown in table 1.

Parameter	Unfitted	Fitted
β ($\frac{\mu A}{V^2}$)	190	250
λ ($\frac{1}{V}$)	0.16	0.01
V_{tn} (V)	0.57	1.25

Table 1: Parameter values of the comparison: EKV vs. Measurements



(a) Unfitted

(b) Fitted

Figure 20: Comparison of I_D-V_{ds} characteristic of nMOS in strong inversion – EKV vs. Measurements

4.5 Comments

In order to achieve a readable results for the weak inversion in figure 19 we had to use a V_{gs} in the range $0.950V$ to $1.050V$. The ampere meter could not read I_D lower than approximately 0.4μ A.

5 General Comments on nMOSFET transistor characteristics

We have not used the books naming conventions for the prefixes and suffixes of the currents and voltages, we've consistently used the names that we used in the plots.

6 Common Source Amplifier

6.1 Intro

We are using the same nMOSFET as in section 4, connecting its source to V_{ss}, its drain to a resistor and the other terminal of the resistor to V_{dd} to form a *common source amplifier*. We want to compare the behaviour of the nMOSFET for the 3 different resistors. The schematics can be seen in figure 21. We want to find the gain, A, and the bias current I_d at that point.

The current at the bias point is given by:

$$V_{ds} = V_{DD} - R_D I_D$$

$$I_D = \frac{V_{DD} - V_{ds}}{R_D}$$

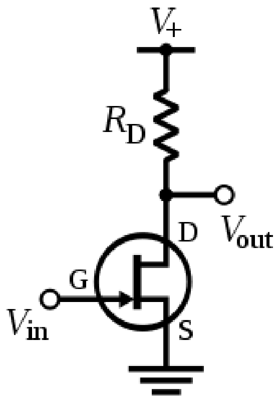


Figure 21: Schematics of a common source amplifier

6.2 Procedure

We connect the circuit in accordence to figure 22. We are now measuring V_{out} from figure 23 which is also V_{ds}. After measuing for $R_D = 4$ MΩ, we repeat the process for $R_D = 470$ kΩ, and finally for $R_D = 4.7$ kΩ.

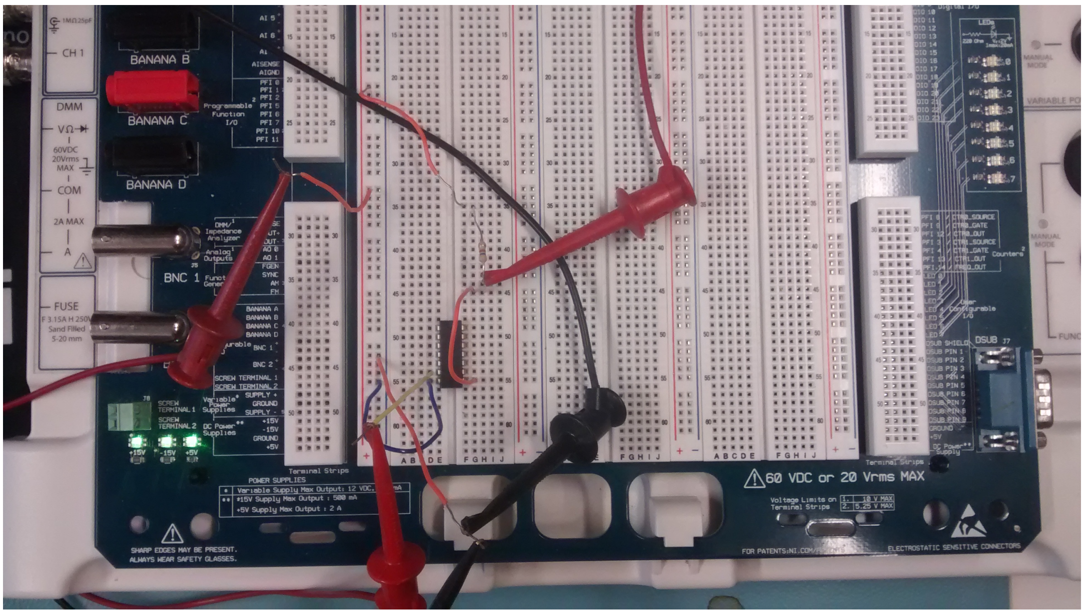


Figure 22: Set-up for characterizing a common source amplifier.

6.3 Results and Observations

The three different plots can be seen in figure 23. We have extracted values for the simulation and filled in table 2. The gain A, which is found by deriving the output in point Q, is also marked in the plot. We use the equations from the intro to calculate the I_D in the bias point.

$$I_D(4M\Omega) = \frac{5V - 0.7014V}{4M\Omega} = 1.07\mu A$$

$$I_D(470k\Omega) = \frac{5V - 1.618V}{470k\Omega} = 7.2\mu A$$

$$I_D(4.7k\Omega) = \frac{5V - 1.796V}{4.7k\Omega} = 681.7\mu A$$

The bias point is found in the point of the graph where the gain is the highest. We have posted the x and y values for the point Q in table 2. By looking at the table, we can see the value of V_{GS} in the bias point using the table.

We compare the values of V_{GS} in the bias point from table 2 with the values of v_{GS} measure in section 4.3.4. The circuit with $R_D = 4$ MΩ has a $V_{GS} = 1.003$ V which is in weak inversion based on the measurements. We have no exact value of V_{tn}, only that it is approximately 1, so we are not sure if the circuit with $R_D = 470$ kΩ is also biased in weak inversion.

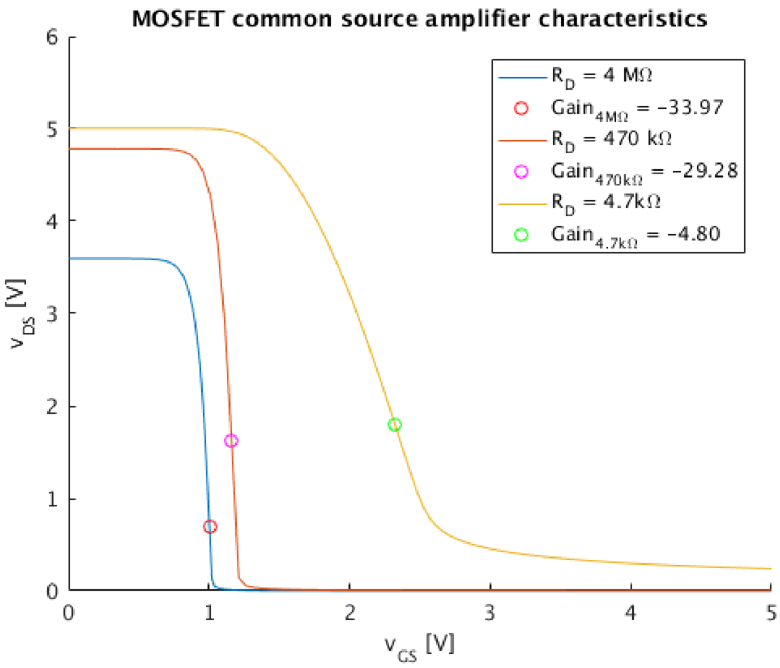


Figure 23: $V_{ds} - V_{gs}$ characteristics of a common source amplifier with different R_D values.

R_D (Ω)	V_{GS} (V)	V_{DS} (V)	Gain (V/V)
4 M	1.003	0.701	-33.97
470 k	1.162	1.618	-29.28
4.7 k	2.323	1.796	-4.80

Table 2: Values in the biassed point, Q.

When we look at the bandwidth of this amplifier, we can use the general term of GBP, Gain Bandwidth Product. The GBP principle is valid for any amplifier, which includes this common source amplifier. The GBP tells us that the product between the gain and the bandwidth of an amplifier is always constant. This means that a higher gain will result in a lower bandwidth and vice versa.

From this we can 'guess' that the amplifier with the least gain will have the highest bandwidth. In this case, that will be the amplifier with $R_D = 4.7$ kΩ.