Electrical noise – counter measures and calculation
Mandatory task 1

Rikesh Chauhan
rikesh.chauhan@fys.uio.no

1 LM741

1.1 Transient Analysis

Figure 1 is the given schematic of BJT amplifier LM741 for analysis.

Resistors $R11$ and $R12$ makes a negative feedback network. Input is applied in the positive terminal, so it is a non-inverting amplifier.

Since the gain of a non-inverting amplifier is given as

$$A_v = 1 + \frac{R11}{R22}$$

where $R11$ and $R12$ have values 10K and 1K, the gain is 11 in theory.

DC input is the biasing DC voltage of the amplifier. This value determines the gain of the amplifier. DC input should be applied within the linear range of the amplifier. If the DC input is too high or too low, the output voltage is clipped/saturated to either +ve or -ve power supply and thus output voltage range is reduced. Moreover the devices may enter into non-linear region when applied DC offset is beyond range. If the amplifier is biased with proper DC input and when AC input is applied, output is obtained which is AC signal times the gain of amplifier.

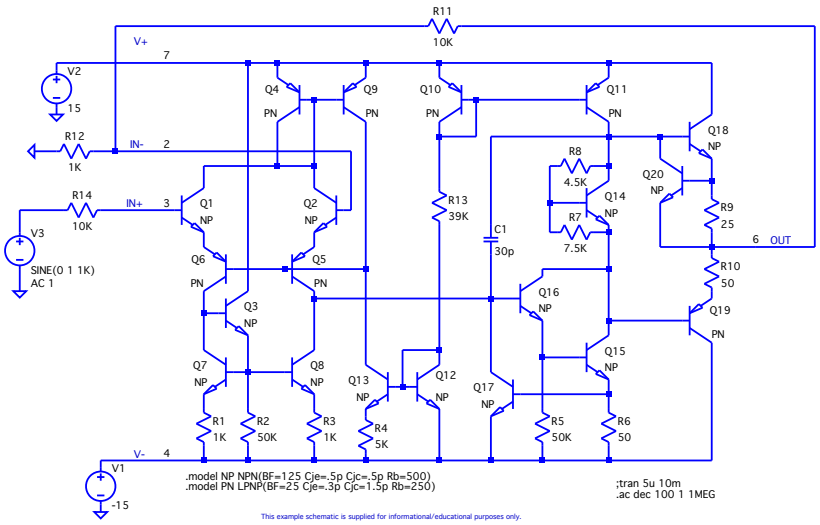

Figure 1: Schematic of LM741

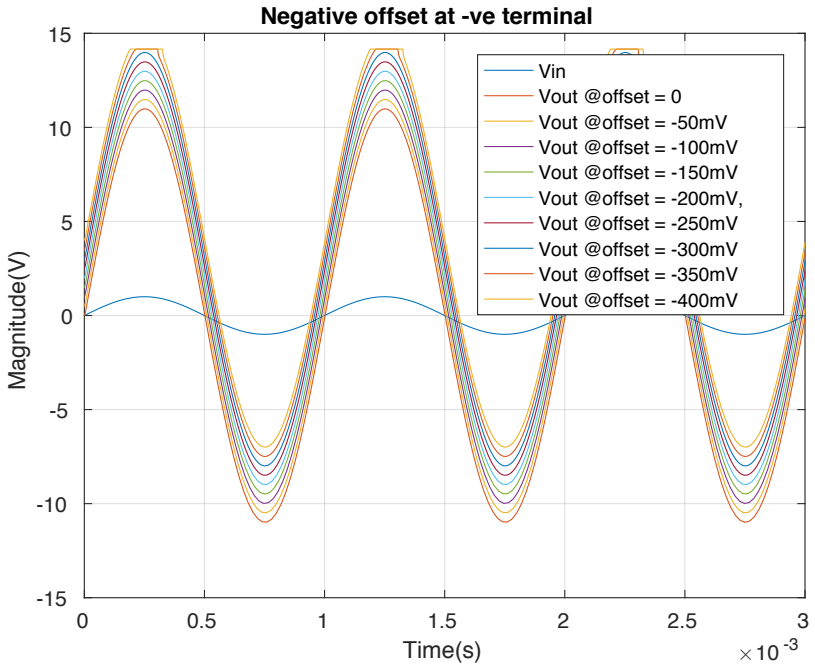

Figure 2: Vout with -ve offset at -ve terminal

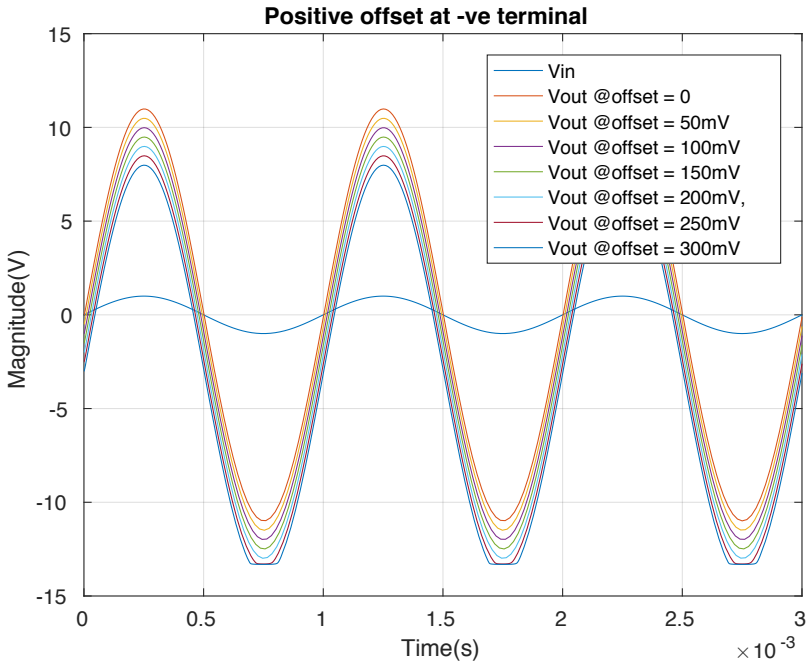

Figure 3: Vout with +ve offset at -ve terminal

From figure 3 and 2, it is seen that DC-offset interval is -300 mV to 200 mV. When the offset is beyond this interval the ouput saturates to maximum possible output range which is just below +ve and just above -ve supply. This drop in output voltage range is due to the drop in the output stage of amplifier.

1.2 AC Analysis

Figure 4 is the AC analysis of the amplifier. This shows that the DC gain is 20.8 dB and Gain Bandwith(GBW) is 700 KHz. The phase marign(PM) is 95°(180°minus phase at 0 dB gain).

The realtion between DC gain A_v and GBW is given as

$$GBW = A_v * BW$$

where BW is -3dB bandwidth.

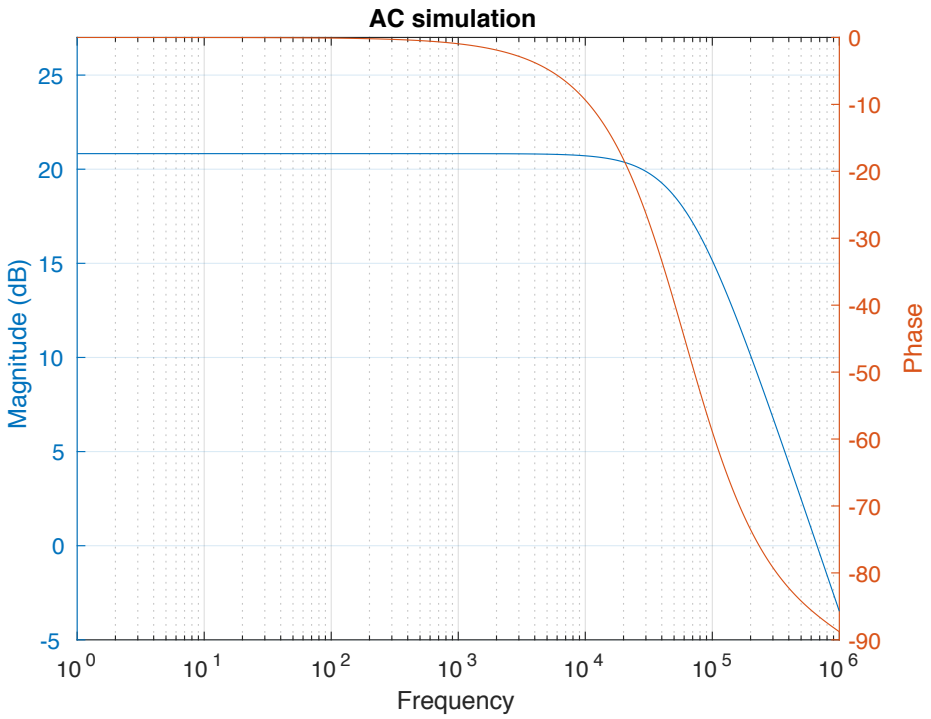

Figure 4: AC analysis of given opamp

1.3 DC-offset

Figure 5 shows the variation of DC gain for different +ve common mode (CM) voltages. Only the DC CM levels where the gain decreases are shown. It is seen from the plot that for DC CM of 14.992 V or less, the DC gain is at -6 dB or greater.

Similarly 6 shows the -ve DC CM where the gain decreases. It shows that for DC CM of -12.847 V or more, the DC gain is -6 dB or greater. It can be said that the minus terminal DC range of the amplifier is -12.847 V to 14.992 V where the gain is within -6 dB.

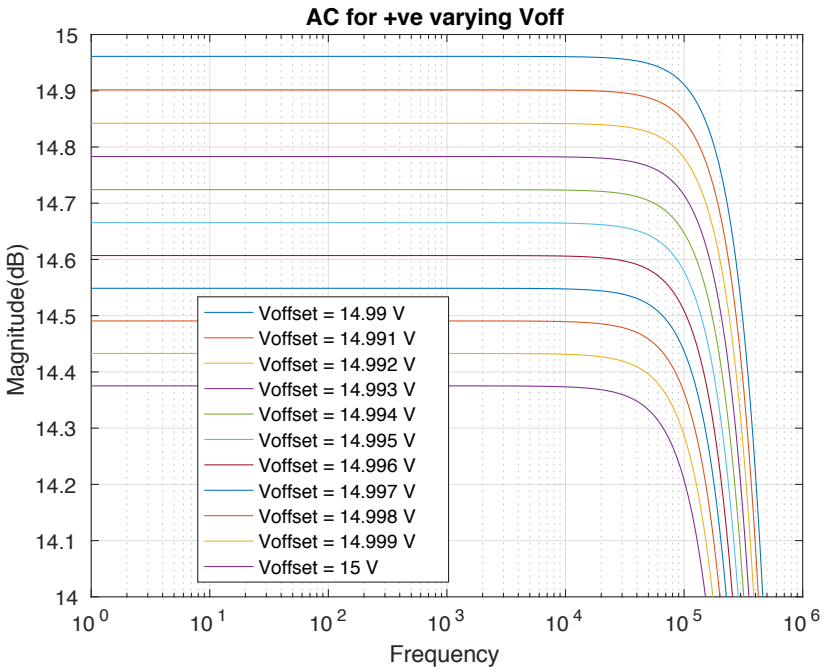

Figure 5: AC analysis with varying +ve offset

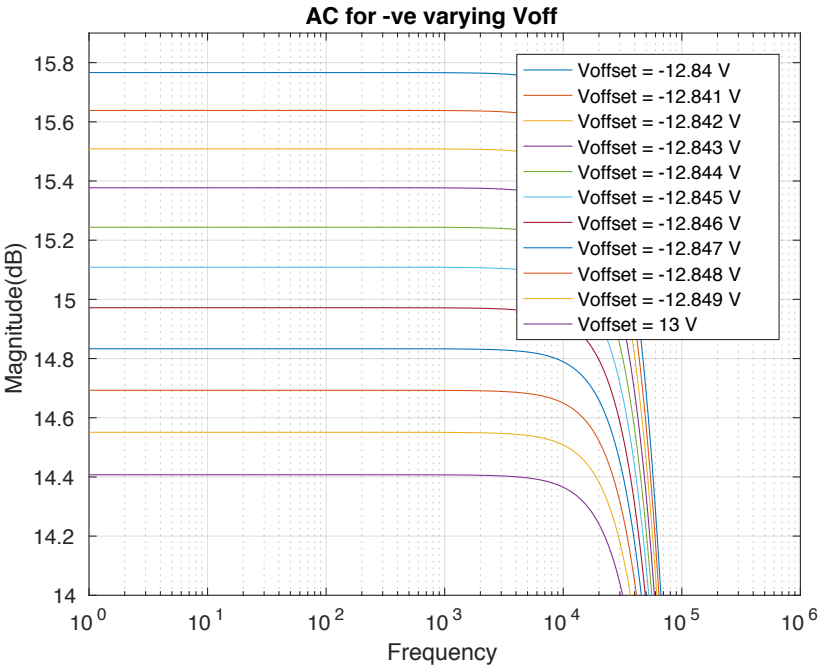

Figure 6: AC analysis with varying -ve offset

1.4 Load capacitance

Figure 7 is schematic and figure 8 is result of AC simulation with C_{load} step of 10pF from 10pF to 30pF. The plot shows that increase in load capacitor has significantly affected the phase by increasing it whereas the gain remains almost constant. This means PM has decreased.

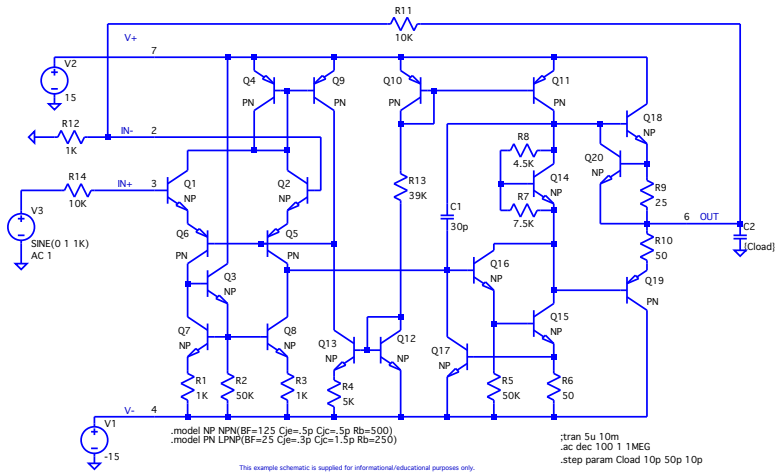

Figure 7: Schematic setup for ac simulation

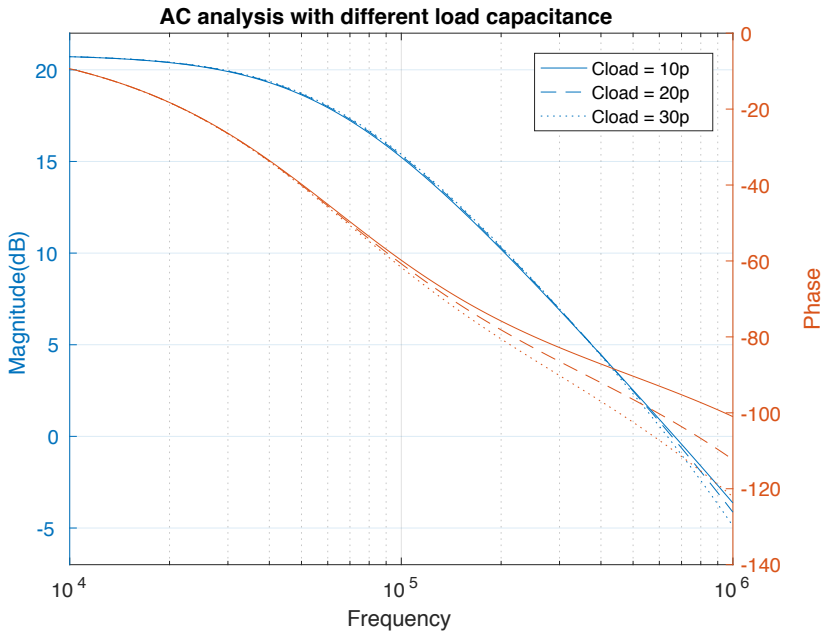

Figure 8: AC analysis with different load capacitance

2 Frequency characteristics of some curves

2.1 FFT with different sampling rates

A low pass (LP) RC filter is deigned. R and C values are arbitrarily chosen 1Ω and $1pF$ respectively so that it has a very high cutoff frequency.

A sine wave signal of period 1 ms and amplitude 1 V, as shown in figure 9, is applied at the input of the filter. This transient signal was sampled at 1/10 and 1/100 of the period and their corresponding FFT was done as shown in 10. FFT clearly shows how different sampling rates affects the frequency components of the same signal. Since a pure sine wave has only one frequency component, it is expected to see only it natural frequency in FFT. But figure 10 shows the harmonics too. It is because the sampled data of true sine wave is in-fact not representing it truly because of lower sampling rate. The strength of strongest unwanted frequency component is -40 dB. It can be concluded that the sampling rate of the measuring device actually affects the frequency components of signal. Instrument with low sampling frequency can give us misleading informations.

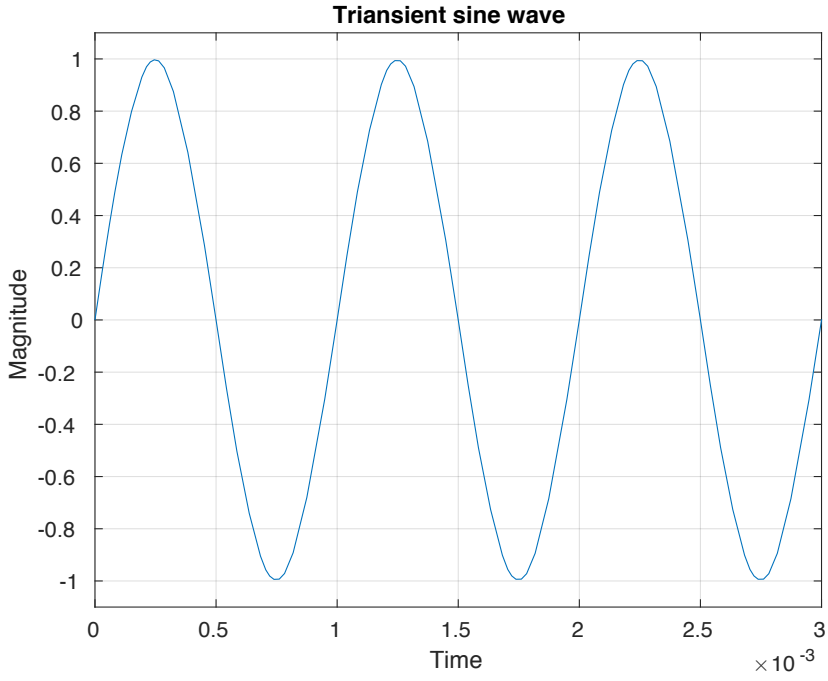

Figure 9: Sine wave

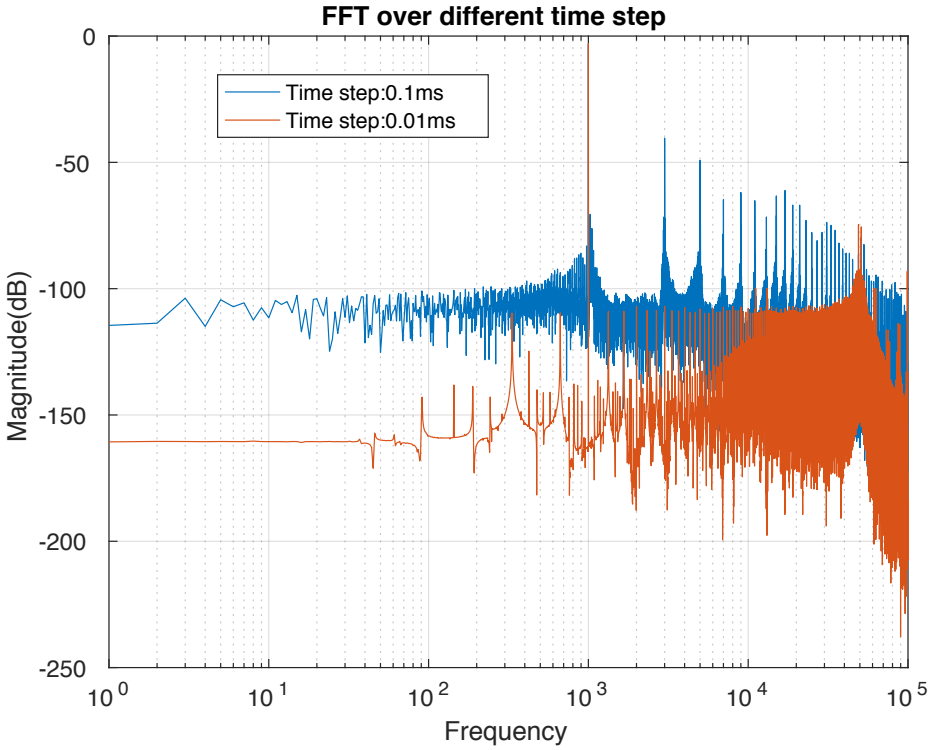

Figure 10: FFT of 9 with different time step

2.2 FFT of signals with different falling (T_f) and rising (T_r) time

Figure 11 shows three different signals with same frequency but with different rising and falling time. FFT of all signals were performed and their respective frequency components were obtained as illustrated by figure 12. It is seen that a triangular signal which has longer falling and rising time has dominant low frequency components but sharply falling higher frequency components. Similarly when the signal is square like with shorter rise and fall time, it has prominent higher frequency component.

The strongest fundamental frequency is 1KHz which has magnitude if -8 dB.

The clock edge should look like ramp like that of triangle pulse in order to reduce the high frequency component in the signal. However having a ramp with gently sloping edge reduces the speed of CMOS logic. Moreover the ON and OFF period may not be properly defined.

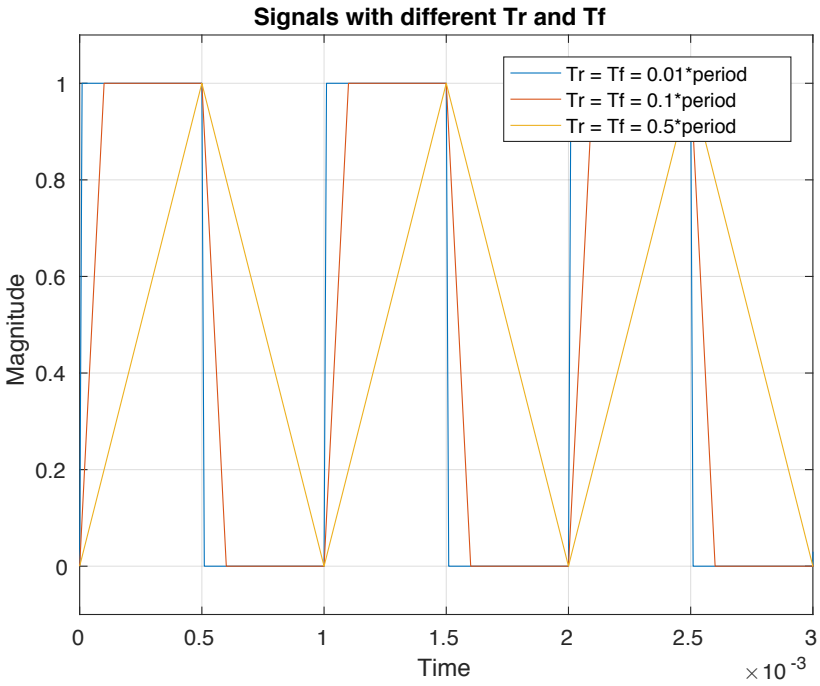

Figure 11: Signals with different rise and fall time

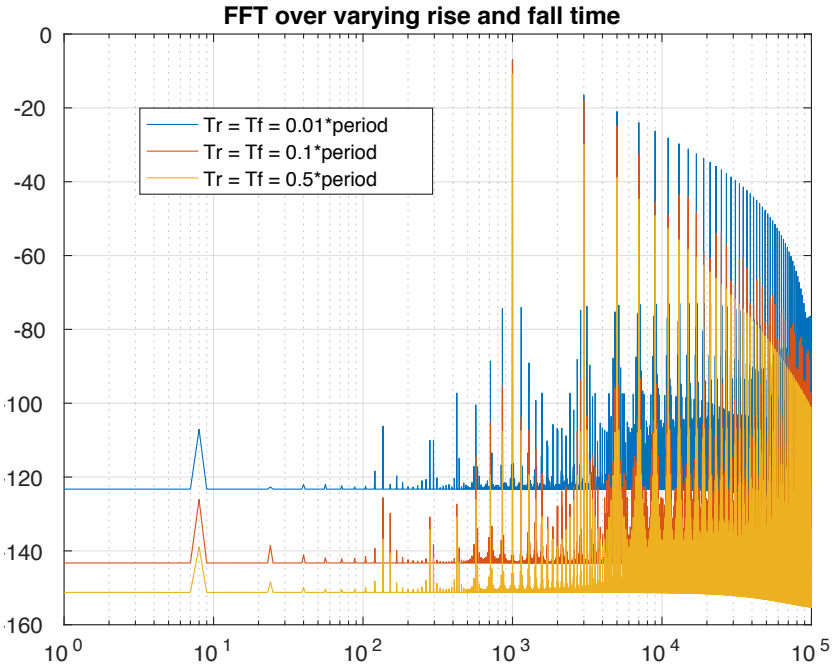

Figure 12: FFT of 11 signals

2.3 RC filter

RC filter shown in figure above is made to have cutoff at 5 times its natural frequency, ie 5 kHz. R and C values were obtained to be 1K and 25nF respectively. Square wave with frequency 1 KHz with rise and fall time of 1/100 of its period was applied as input and its output was observed as shown in figure 13. FFT of the both the input and output was done as in figure 14. The output signal has longer rise and fall time because of larger capacitor at the output. which means output has more low frequency components than the input which is clearly shown by the FFT plot.

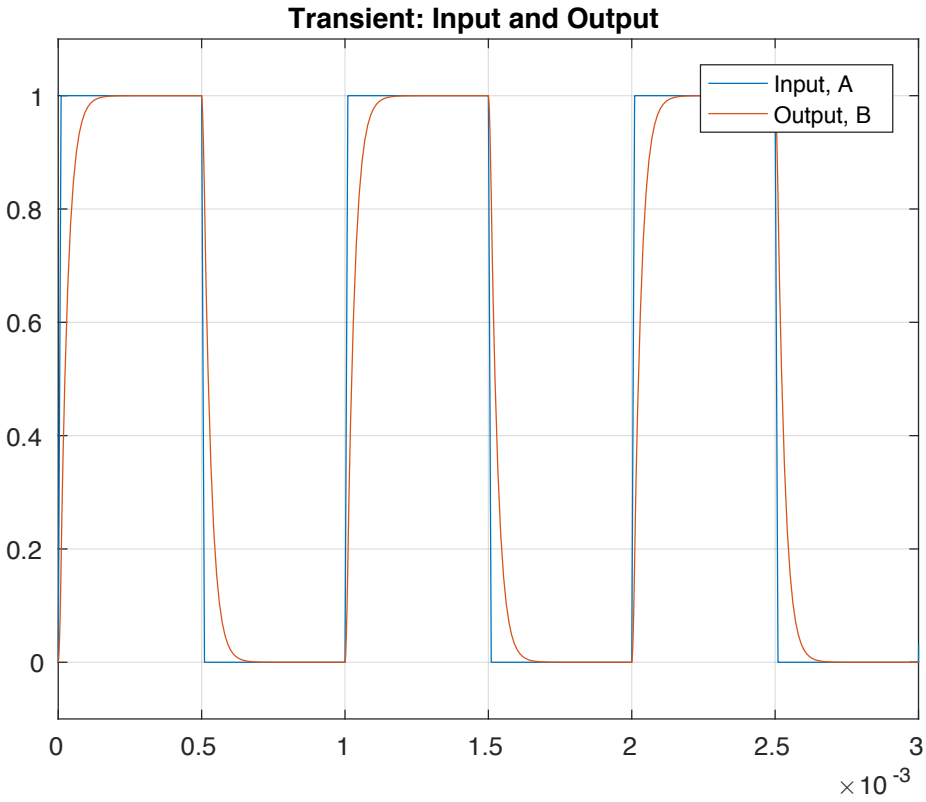

Figure 13: Input and output of LP filter

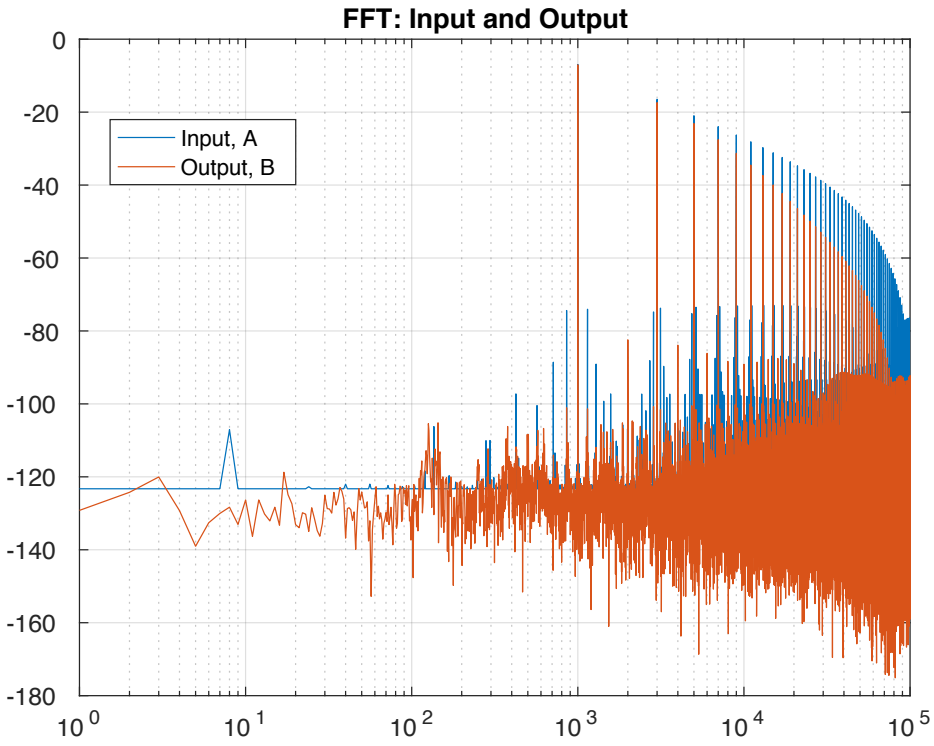

Figure 14: FFT of 13 signals

3 Decoupling capacitors

Given in the question that $L = 10nH$ for each capacitor, current spikes (triangular wave) of 0-1 A amplitude with $T_r = T_f = 5ns$, $Ton = 0$, period = 10 us, voltage at the output to be stable within 5% of 1.5 V and lower corner frequency at 1MHz.

3.1

Low frequency target impedance, $Z_t = kdV/dI$ is given as

$$Z_t = k\frac{dV}{dI}$$

where $k = 2$, $dV = 0.075V$ and $dI = 1A$. Hence $Z_t = 0.15\Omega$.

3.2

Number of capacitors required is given as

$$n = \frac{2L}{Z_t T_r}$$

where $L = 10nH$, $T_r = 5ns$. Hence $n = 27$. Then each inductor has inductance $370pH(L/n)$.

3.3

The total capacitance is given by the condition

$$\begin{aligned} \frac{1}{\omega C} &\leq Z_t \\ C &\geq \frac{1}{2\pi f Z_t} \end{aligned}$$

where $f = 1MHz$. Hence, $C = 1.1uF$ and hence each capacitor is 40 nF.

3.4

The high frequency corner decided by rise/fall time is given as

$$f = \frac{1}{\pi * T_r}$$

Hence is $f = 64MHz$.

3.5

Figure 15 is the schematic and figure 16 and 17 are transient and frequency simulation results. In the transient simulation, the voltage spikes due to the current spikes can be seen. The voltage spikes are between 40 mV to -55 mV, well below the requirement.

Similarly from the ac simulation, the lower and upper corner frequency can be noticed around 1 MHz and 64 MHz as calculated.

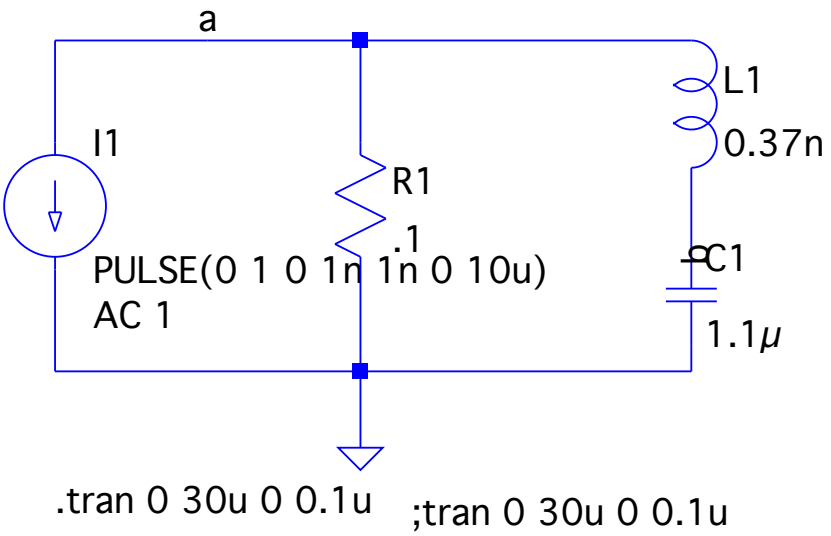

Figure 15: Schematic set up of a single decoupling capacitor

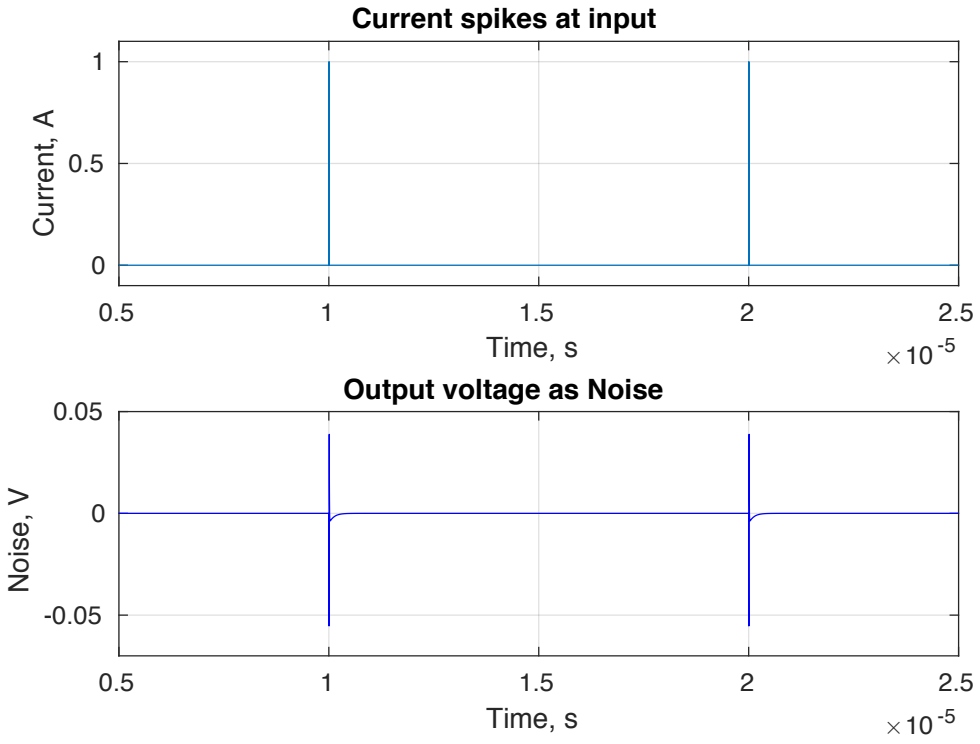

Figure 16: Current spikes input and voltage noise output

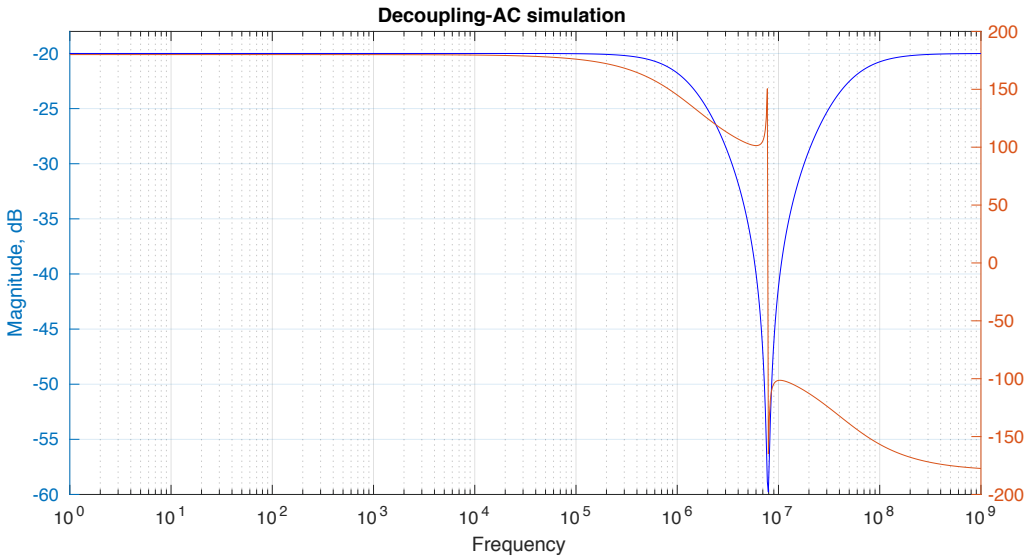

Figure 17: AC analysis of decoupled output

3.6

Figure 18 and 19 are transient and frequency simulation results with comparison between different Tr and Tf. The difference is seen only in the time domain because in spite of different rise and fall time, both the signal have same frequency and hence magnitude and phase are unaffected.

In case of transient signal in figure 18, it can be noticed that the voltage spikes due to the input current spikes of shorter Tr and Tf exceed our stability requirement. The spikes are close to 0.095 V whereas the requirement is to reduce it below 0.075 V.

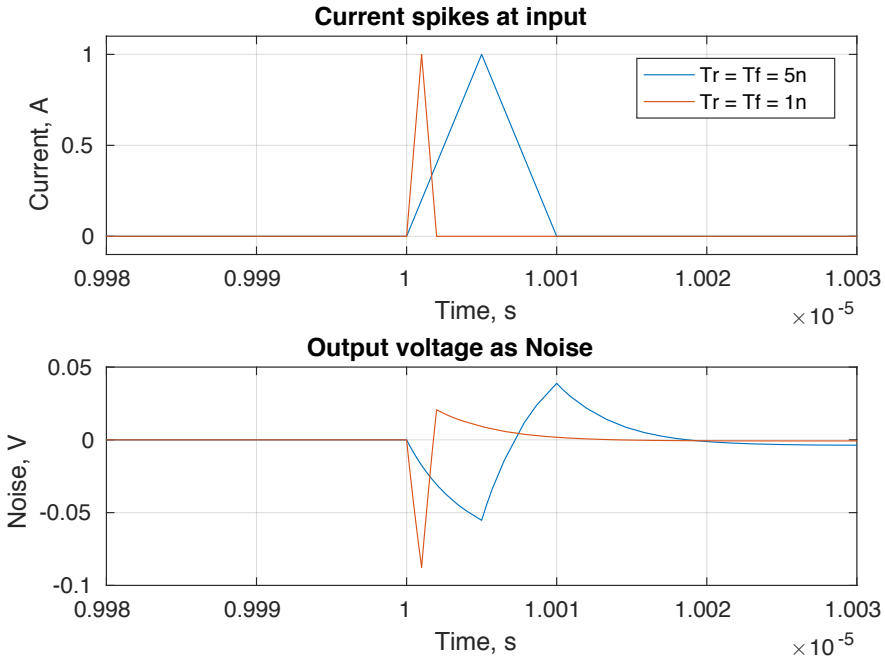

Figure 18: Current spikes with shorter Tr and Tf and voltage output as noise

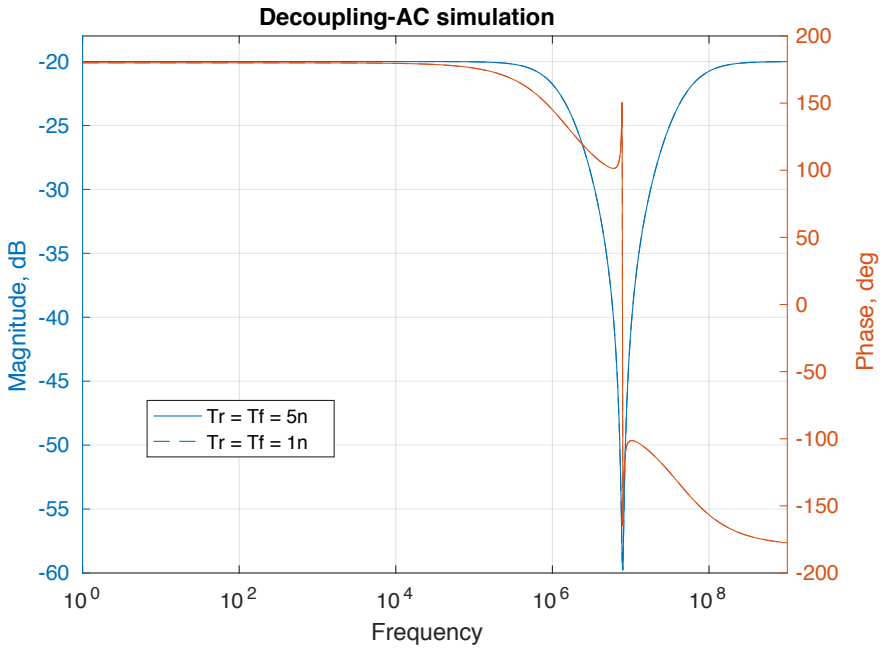

Figure 19: AC of decoupled output noise with different Tr and Tf

4 Parasitic capacitive coupling

4.1 Noise captured

Figure 20 is the two parallel conductors both of length 10 cm. The parasitic capacitance between the lines is 0.1 pF/cm. Conductor 1 carry a signal of 5 V swing and conductor 2 has a capacitor and resistor in parallel to ground of 10 pF and $10M\Omega$. To the right of figure 20 illustrates the equivalent parasitic coupling in terms of lumped capacitors, also shown in figure 21 .

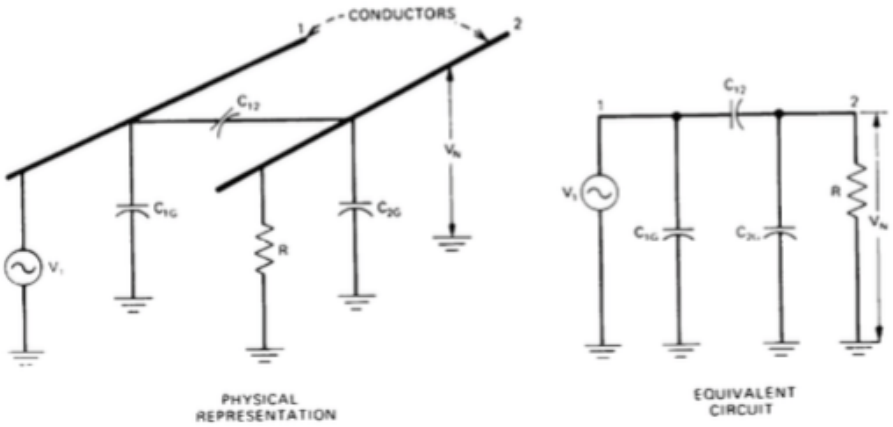

Figure 20: Capacitive coupling between two conductors

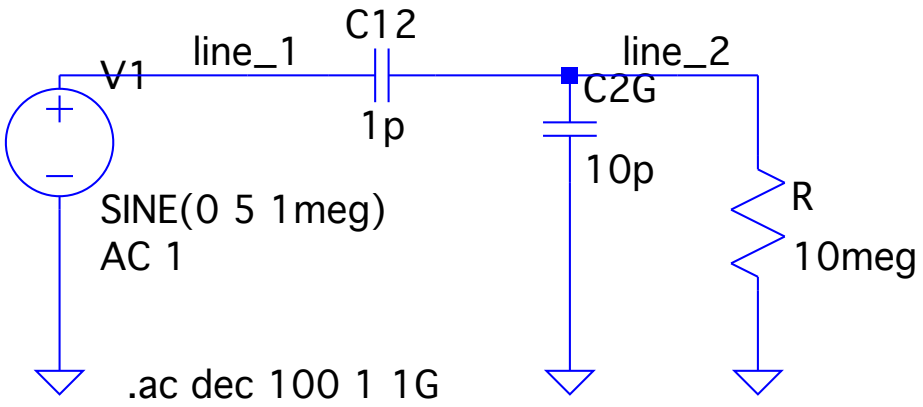

Figure 21: Schematic of capacitive coupling between two conductors

Similarly 22 shows the same two conductors where conductor 2 is shield. To the right is its equivalent circuit which is also shown is

figure 23. Here C_{12} is parasitic between conductor 1 and 2, which is 1pF without shield. C_{2G} is capacitor between conductor 2 and ground. R is a resistor connected between conductor 2 and ground. C_{2S} is parasitic between conductor 2 and shield which is 1 pF/cm.

In presence of shield, C_{12} decreases. If L be the length of shield, then

$$C_{12} = 1pF - 0.1pF/cm * L$$

Similarly with shield, C_{12} increases as

$$C_{2S} = 1pF * L$$

Whereas, C_{2G} being a physical component remains the same.

The worst case noise magnitude is given as below which is used for calculation. This is valid when shield does not cover all the length of the conductor. When there is no shield, we take $C_{2S} = 0$.

$$V_N = \frac{C_{12}}{C_{12} + C_{2G} + C_{2S}}$$

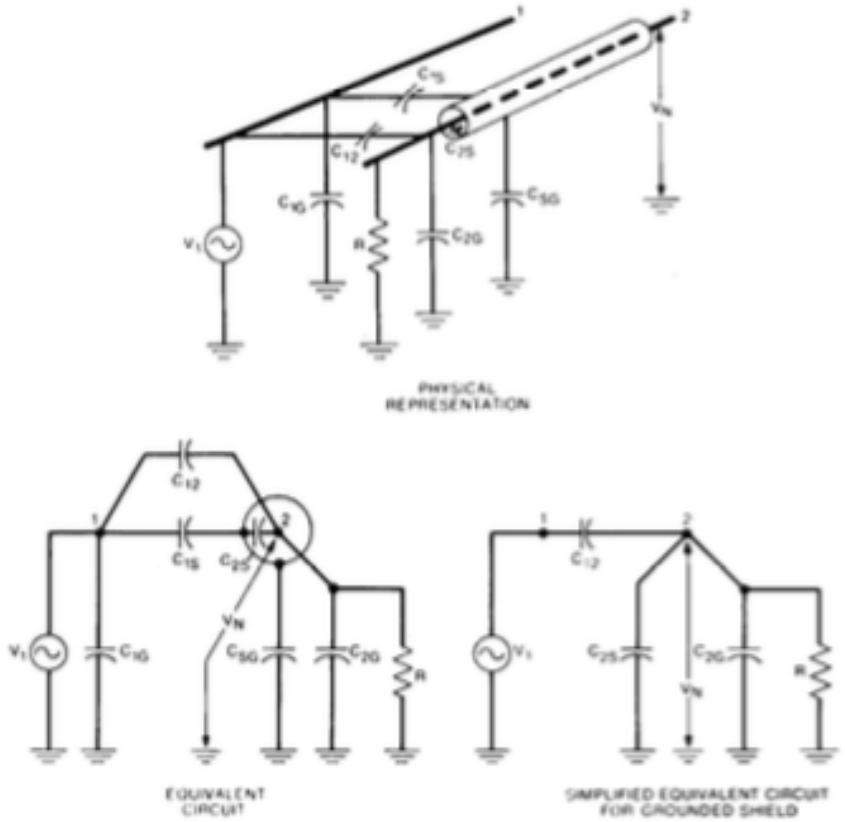

Figure 22: Capacitive coupling between two conductors with shielding

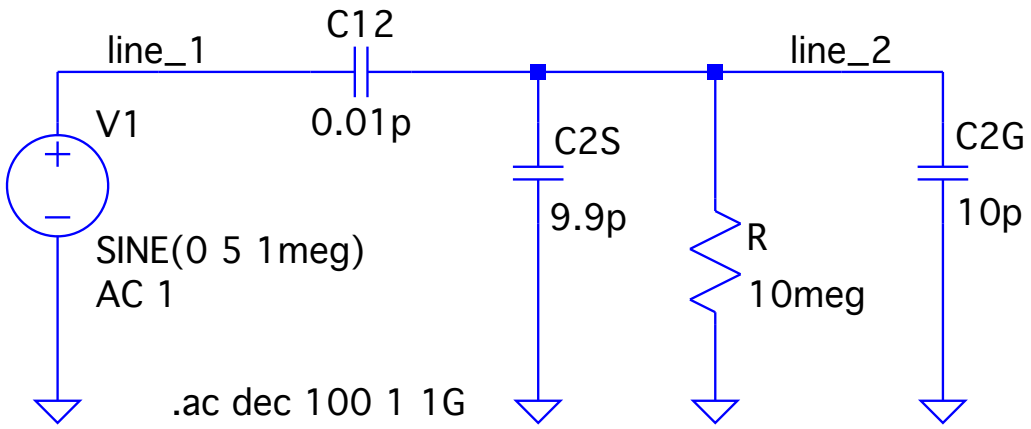

Figure 23: Schematic of capacitive coupling between two conductors with shielding

Noise received by conductor 2 with shield of varying length and without shield is analysed. Table 1 summarises the calculated values and 24 shows the simulated frequency response.

Table 1: Parasitic capacitance and shielding

L (cm)	$C_{12}(pF)$	$C_{2S}(pF)$	$C_{2G}(pF)$	Noise (dB) calculated
0	1	0	10	-20.8
2	0.8	2	10	-24.1
5	0.5	5	10	-29.8
9	0.1	9	10	-45.6
9.9	0.01	9.9	10	-66

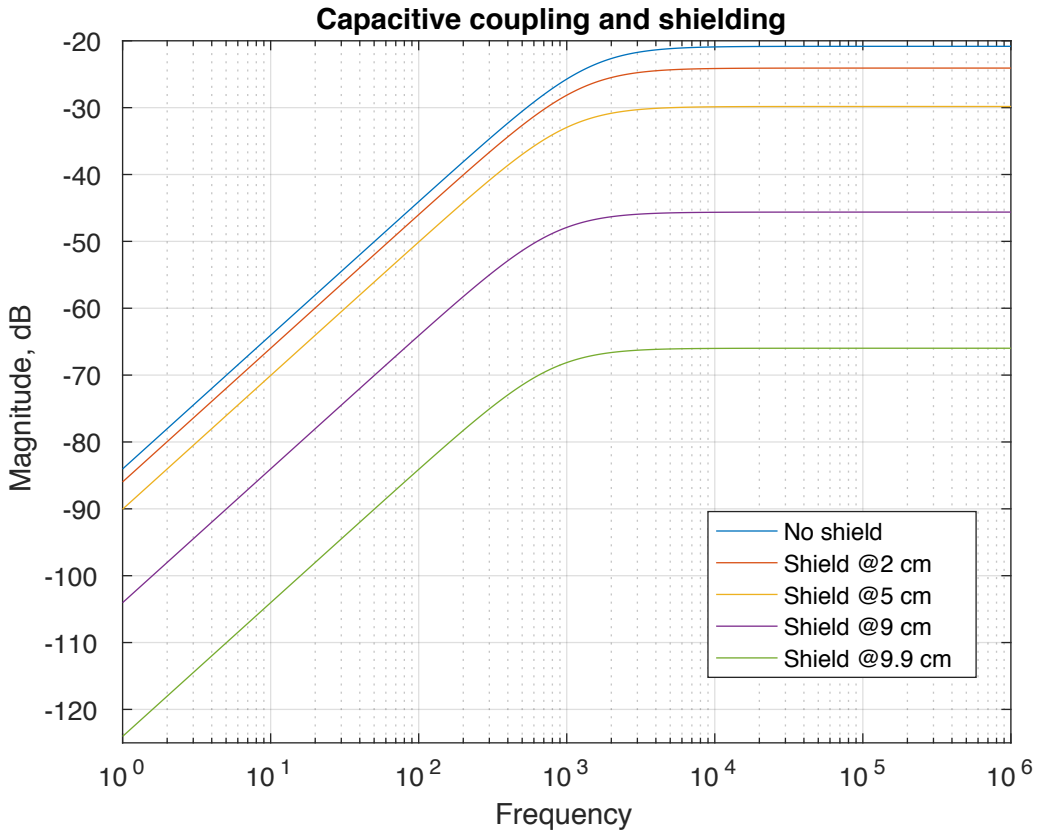

Figure 24: Frequency response of capacitive coupled noise voltage

From figure 24 and table 1, it is seen that simulated and calculated magnitude of noise is almost the same .Both shows that capacitive coupling decreases with increase in length of shield and hence the noise picked by conductor two. The plot also shows that corner frequency has decreased too.

5 Artificial source of transient analysis

5.1 BV sources

Figure 25 is the schematics of two BV sources and WH1 and WH2 in figure 26 are white noises generated using those sources in LTspice using WHITE function with same index. Since the subtracted noise in the last plot below is zero for all time, it looks like WHITE generate the same random value for same index and hence it cannot be considered as true white noise.

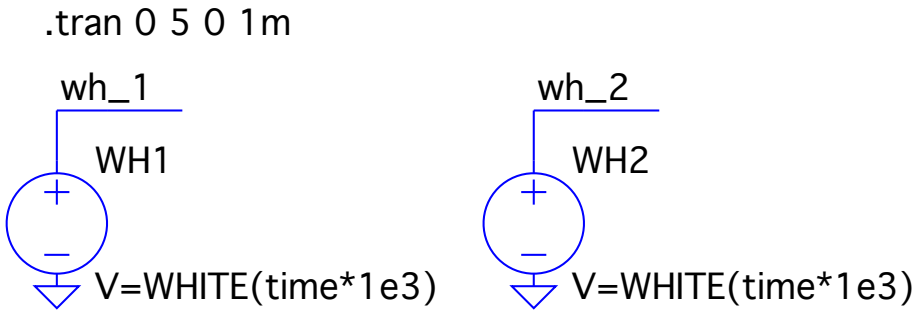

Figure 25: Schematics of BV white noise

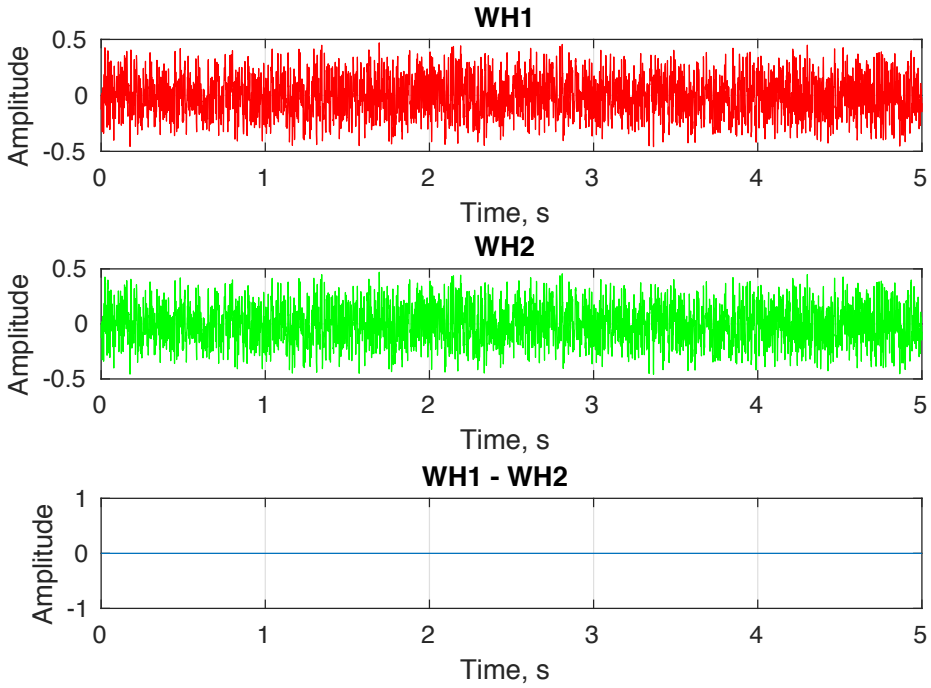

Figure 26: White noise from BV sources

5.2 BV sources with different time index

Figure 27 again illustrates the white noises from BV sources where WH2 is changed by 1. The subtraction of WH1 and WH2 is now neither zero nor constant, hence looks like these may be considered white noises. The amplitude is still within -0.5 to +0.5. The truth is white noise has a normal distribution and WH1 and WH2 distribution is not normal.

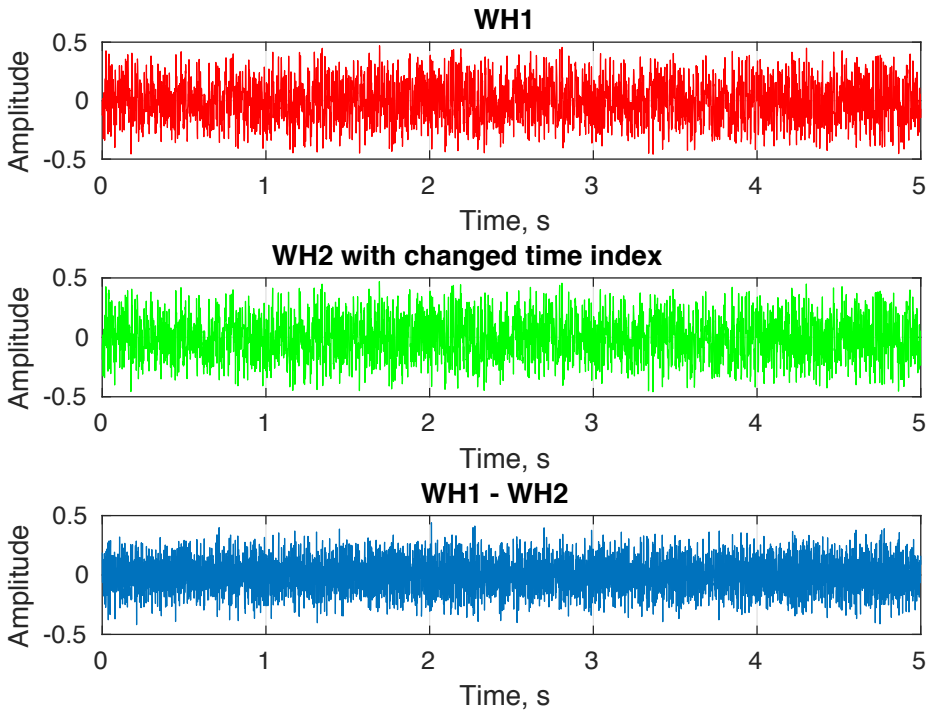

Figure 27: White noise from BV sources with different time index

5.3 Noise from file and BV source

Figure 29 is the comparison of noise generated from provided file and BV source. The FILE1 has larger amplitude and looks more normal whereas WH1 from BV source has smaller magnitude. The difference between these too looks even more random with some spikes grater in amplitude than FILE1. The schematic is shown in 28.

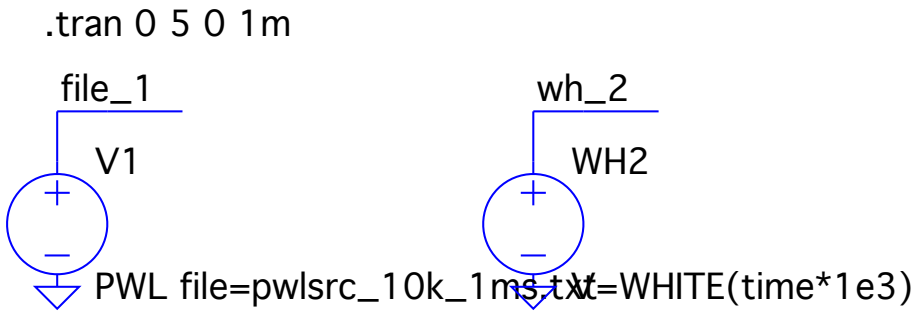

Figure 28: Schematic of file noise source and BV source

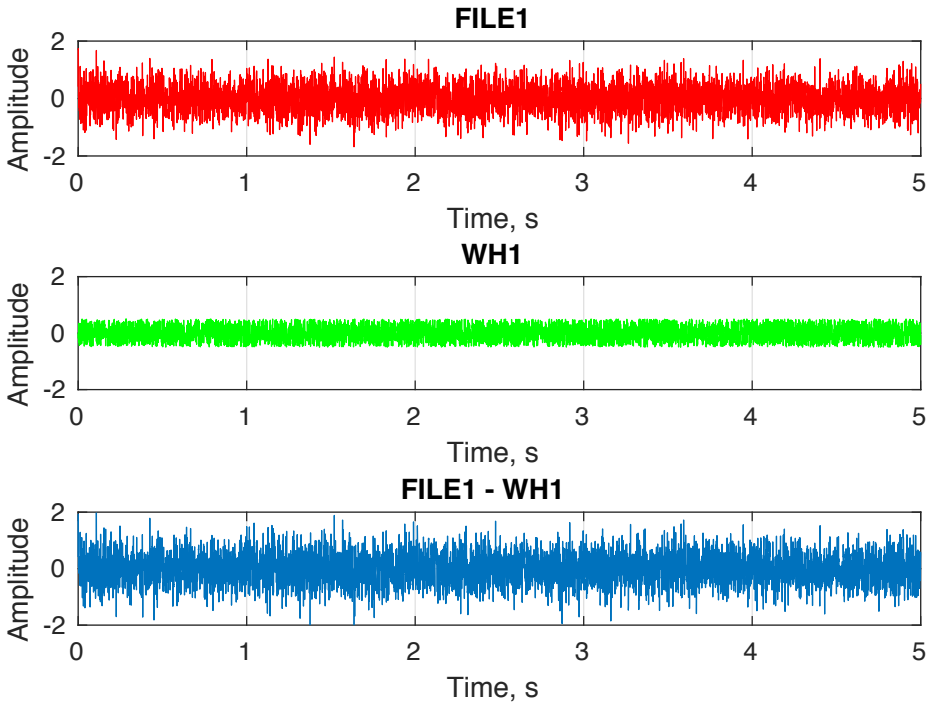

Figure 29: Noise from file and BV

5.4 FILE1 and delayed FILE1

Figure 31 illustrates noise from file, FILE1 and FILE2 which is delayed FILE1 by 1 ms. The set up as shown in 30 The difference in these signal looks like even more random with some spikes going beyond 2 V. It seems like the distribution is still normal with increase in deviation.

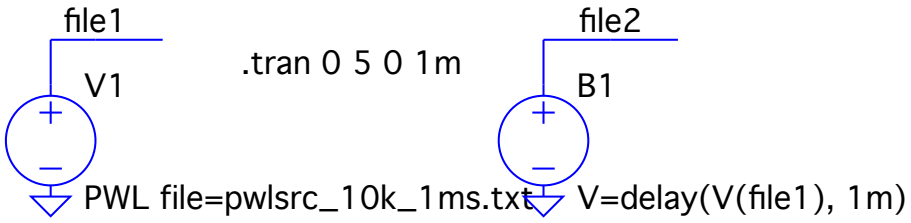

Figure 30: Schematic set up of file noise and its delay

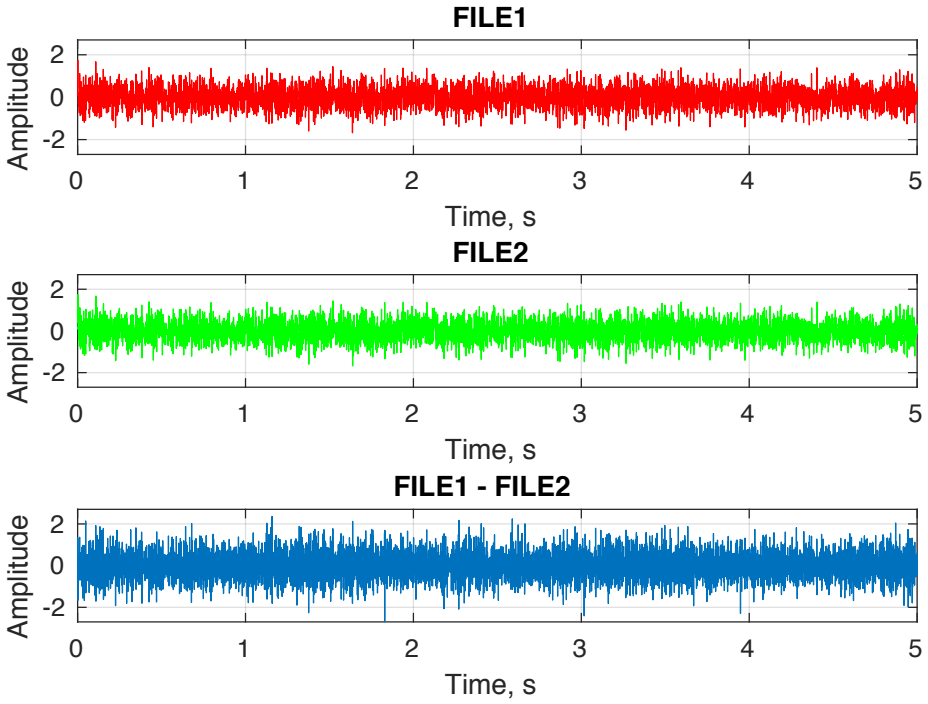

Figure 31: FILE1 and delayed FILE1