Integrated Low-Loss CMOS Active Rectifier for Wirelessly Powered Devices

Yat-Hei Lam, *Student Member, IEEE*, Wing-Hung Ki, *Member, IEEE*, and Chi-Ying Tsui, *Member, IEEE*

***Abstract*—A low-loss CMOS full-wave active rectifier is presented. It consists of two dynamically biased and symmetrically matched active diodes each realized by an nMOS switch driven by a 2-ns voltage comparator with reverse-current control. With a load of 1.8-kΩ, the rectified dc voltage is 3.22 V and 1.2 V for a 13.56 MHz ac sinusoidal input voltage of 3.5 V and 1.5 V respectively. It is fabricated in a 0.35-μm CMOS process with an active area of 0.0055 mm^2, with no low-threshold devices and on-chip passive components.**

***Index Terms*—AC–DC power conversion, radio-frequency identification (RFID), rectifiers, symmetrical matching, wireless power transmission.**

I. Introduction

WIRELESS devices such as biomedical implants [1]–[4] and radio-frequency identification (RFID) tags [5], [6] are powered by a wireless inductive link. Without an embedded battery, they can only be activated when placed near the transmitter. Fig. 1 shows the block diagram of a generic wirelessly powered system. The inductive coil or antenna captures the RF signal. The coupled energy is then passed to a resonance tuning circuit to generate a high ac voltage, followed by a rectifier to convert it into a dc voltage to power up the signal processor downstream. A rectifier with high efficiency is then essential in extending the reading distance and reducing the power requirement of the transmitter.

AC-to-dc conversion is conveniently achieved by diodes and capacitors. Single-diode half-wave rectifier is simple and full-wave rectifier with a diode bridge [Fig. 2(a)] makes better use of the ac input and gives a smaller output ripple voltage. They are commonly used in high-voltage applications where the diode forward voltage drop of 0.7 to 1 V is relatively low. However, for low-voltage integrated circuit applications, this forward drop significantly reduces the power conversion efficiency (PCE). Schottky diodes with a low forward drop could be used to enhance the efficiency. However, the production cost is high compared to a standard CMOS process.

In a CMOS-only implementation, the diodes can be replaced by diode-connected MOS transistors. Low threshold voltage ($V_{\rm t}$) transistors could be used in advanced CMOS processes, requiring extra cost for additional masks and fabrication steps. Alternatively, $V_{\rm t}$ cancellation technique in standard CMOS processes [7], [8] could reduce the turn-on threshold by additional biasing circuits. In both cases, the gate-to-drain voltages are fixed and the gate–drive voltages are controlled by their drain-to-source voltages that change only slightly from forward to reverse conduction. Therefore, the switches cannot be turned on and off completely and this leads to inefficient rectification. In [9], two diodes of the diode bridge rectifier are replaced by two cross-coupled pMOS transistors [Fig. 2(b)]. The gates of these pMOS transistors are driven by a larger voltage swing than diode-connected pMOS transistors and hence a higher on/off current ratio can be achieved. However, the bottom two diodes are still implemented by diode-connected nMOS transistors to block the reverse current, and the efficiency is not optimized. It would be advantageous if the diodes could be replaced by active circuitries that can be turned on fast when $|V_{\rm ac}| > V_{\rm dc}$, and turned off fast to avoid reverse-current leakage.

On-chip active rectification has been demonstrated in a highly efficient voltage doubler [10] by using active diode circuitries instead of passive diodes. High power-conversion efficiency (PCE) was achieved when operating at 1 MHz. However, many wirelessly powered devices operate at a much higher frequency, for example, in the 13.56-MHz Industrial, Scientific and Medical (ISM) band. Moreover, the generation of the biasing current is not trivial, as there is no dc supply when the wireless device is initially relaxed.

In this research, a low-loss CMOS active rectifier is presented. All the four power transistors are driven on and off completely, resulting in a much higher efficiency. The principle

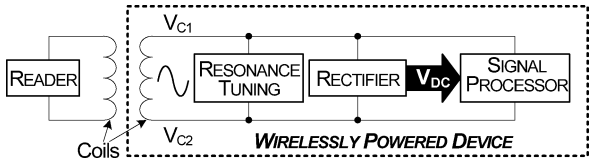

Fig. 1. Wirelessly powered system with inductive link.

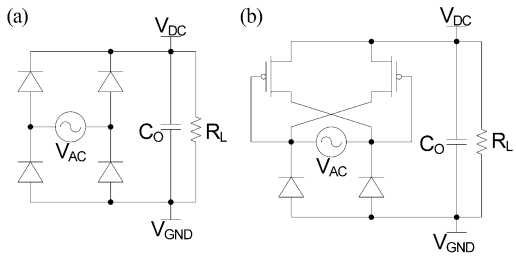

Fig. 2. Full-wave rectifier (a) with diodes, and (b) with cross-coupled pMOS.

Manuscript received April 13, 2006; revised September 20, 2006. This work was supported in part by the Research Grant Council under Grant CERG 614506. This paper was recommended by Associate Editor V. Kursun.

The authors are with the Department of Electronic and Computer Engineering, The Hong Kong University of Science and Technology, Hong Kong (e-mail: hylas@ece.ust.hk; eeki@ece.ust.hk; eetsui@ece.ust.hk).

Digital Object Identifier 10.1109/TCSII.2006.885400

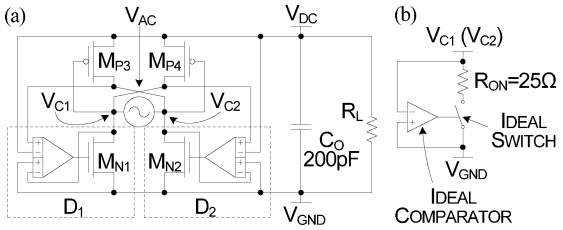

Fig. 3. Full-wave active rectifier (a) topology and (b) simulation model for D_1 and D_2.

of operation of the active rectifier using active diodes is presented in Section II. Implementation issues of the active diodes are discussed in Section III, and measurement results are shown in Section IV, followed by concluding remarks in Section V.

II. Switching Dynamics of Active Rectifier

To enhance the efficiency, we propose a full-wave active rectifier employing active diodes with very low forward drop to replace the bottom diodes of [9], as shown in Fig. 3(a). Now, D_1 (equivalently, $M_{\rm n1}$) should be turned on when $V_{C2} - V_{C1} > V_{\rm dc} - V_{\rm GND}$, or

$$V_{C2} - V_{\rm dc} > V_{C1} - V_{\rm GND}. \tag{1}$$

The above action is implemented by a 4-input comparator. Before discussing the exact circuitry, which will be presented in Section III, we first describe the switching dynamics of the active rectifier, using HSPICE for simulation. A 0.35-μm CMOS process is used, and the threshold voltage of pMOS transistors $|V_{\rm tp}|$ is 730 mV ($V_{\rm tn}$ of nMOS is 550 mV). The cross-coupled pMOS transistors have a W/L ratio of 240 μm/0.35-μm and the diodes D_1 and D_2 are modeled as two ideal switches with turn-on resistance $R_{\rm ON}$ of 25 Ω controlled by two ideal voltage comparators as shown in Fig. 3(b). The input ac voltage source is sinusoidal, with amplitude of 3 V and frequency of 13.56 MHz. Fig. 4 shows the simulated waveforms of V_{C1} and V_{C2} together with $V_{\rm dc}$ (solid black line), $|V_{\rm ac}|$ (solid gray line) and $V_{\rm GND}$ (the 0 V line) for study.

The electromagnetically induced source $V_{\rm ac} = V_{C1} - V_{C2}$ is sinusoidal and floating. For many oscilloscopes, $V_{\rm ac}$ cannot be measured directly, as the grounds of the oscilloscope and probes are common, such as the ground node $V_{\rm GND}$ shown in Fig. 3(a). From Fig. 4, we observe that the waveforms V_{C1} and V_{C2} with respect to $V_{\rm GND}$ look more like skewed and distorted sinusoids. The switching dynamics is discussed below.

When $V_{C1} > V_{C2}$, D_1 is reverse biased and is off, cutting the returned path for $M_{\rm p3}$, and so $M_{\rm p3}$ is also off. In this half-period, four transitions resulting in five states can be identified. At the start of the period $t = T_{00}$, $V_{\rm ac} = 0$, and all pMOS and diodes are off.

When $V_{C1} - V_{C2} = |V_{\rm tp}|$ at $t = T_{01}$, $M_{\rm p4}$ is gradually turned on, shorting V_{C1} to $V_{\rm dc}$. As such, the change in $V_{\rm ac}$ is reflected by the drop in V_{C2}. It should be noted that as D_2 is not turned on, no drain current flows in $M_{\rm p4}$. At $t = T_{02}$, $V_{\rm ac}$ is higher than $V_{\rm dc}$ such that V_{C2} drops below $V_{\rm GND}$, and the diode D_2 (with a very low forward drop) is then turned on. $V_{\rm dc}$ is charged up via D_2 and $M_{\rm p4}$, and conduction drop can be observed due to their finite resistance (Fig. 4). After $V_{\rm ac}$ reaches the peak, it starts to decrease and at $t = T_{03}$, V_{C2} rises above $V_{\rm GND}$, turning off D_2. As $V_{\rm ac}$ drops to $|V_{\rm tp}|$ at $t = T_{04}$, the gate drive of $M_{\rm p4}$ is insufficient to short V_{C1} to $V_{\rm dc}$, and V_{C1} starts to drop. All pMOS and diodes are off for the rest of the half-period. The operation of the rectifier in the second half-period is similar to that of the first half-period, except that $M_{\rm p3}$ and D_1 are responsible for the action. Table I tabulates all the switching actions in one complete period.

With a $V_{\rm ac}$ of 3 V and a load resistor of 1.8-kΩ, the ideal full-wave rectifier gives a $V_{\rm dc}$ of 2.75 V. However, $V_{\rm dc}$ drops to 2.23 V if the idealized diodes are replaced with diode-connected nMOS transistors, as shown in Fig. 5, giving a lower efficiency.

The simulation result in Fig. 4 shows that the conduction time is approximately 10 ns. A long turn-on time of the active diode reduces the conduction time and limits the maximum output current. Also, a long turn-off time leads to reverse charge leakage, hurting the power conversion efficiency and generates a larger ripple voltage at $V_{\rm dc}$. Thus, an active diode with short response time is essential and fast voltage comparators are critical in determining the performance of the active rectifier. Trimming after fabrication is undesirable in low-cost products such as RFID tags, and symmetrical structure and matched biasing technique should be employed to minimize systematic offset. Random offset could be reduced by having a simple circuitry with a low device count.

III. Integrated Low-Loss CMOS Active Diode

Fig. 6 shows the schematics of the active diode D_1 of our proposed active rectifier. The schematic of D_2 is similar with V_{C1} and V_{C2} interchanged. Each active diode is realized by an nMOS transistor controlled by a 4-input comparator. Note that there is no steady dc voltage supply in the rectifier system before it is activated, and hence, the 4-input comparators are designed to be self-powered and biased by the unsteady and distorted sinusoidal voltages V_{C1} and V_{C2} to ensure that the rectifier could start up before $V_{\rm dc}$ is charged up.

Now, from Fig. 3(a), when $M_{\rm p3}$ turns on, the upper inputs to the comparator of D_1 have the highest common mode voltage. Similarly, when $M_{\rm n1}$ turns on, the lower inputs to the comparator of D_1 have the lowest common mode voltage. Therefore, it is natural to employ common-gate structures for the input stages of the comparator to satisfy the above requirements. Transistors M_1 to M_8 serves as a 2-stage comparator with common-gate input stages. The low-side common-gate input stage formed by M_1, M_2 and M_7 monitors the voltage across $M_{\rm n1}$. The high side input stage formed by M_3, M_4 and M_8 monitors the voltage across $M_{\rm p3}$. The source of M_4 is connected to V_{C2} instead of $V_{\rm dc}$ to serve two purposes. First, when the rectifier is relaxed, $V_{\rm dc} = 0\ V$. The rectifier cannot start up when the source of M_4 is connected to $V_{\rm dc}$. For the present connection, D_1 will be activated whenever $V_{C2} > |V_{\rm tp}| + V_{\rm tn}$. Second, the bias current of the comparator will be zero when V_{C2} swings below $|V_{\rm tp}| + V_{\rm tn}$ (due to the diode-connected M_4 and M_2) or $2|V_{\rm tp}|$ (due to M_4 and M_6). As a result, only one active diode is activated at a time and the quiescent current is reduced. Hence, dynamic biasing is realized and with no extra startup circuitry. M_6 works as a bias limit resistor.

When two nMOS (or pMOS) transistors are matched, they have the same W/L ratio. When they are symmetrically

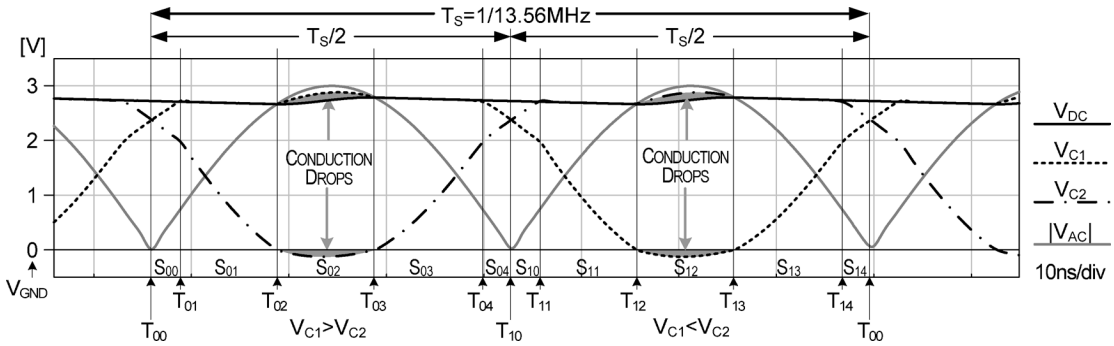

Fig. 4. Simulation result of full-wave rectifier with cross-coupled pMOS and idealized diode model.

TABLE I
DIODES AND POWER TRANSISTORS IN DIFFERENT STATES

	State	D_1	D_2	M_{P3}	M_{P4}
$V_{C1} > V_{C2}$	S_{00}	OFF	OFF	OFF	OFF
	S_{01}	OFF	OFF	OFF	**ON**
	S_{02}	OFF	**ON**	OFF	**ON**
	S_{03}	OFF	OFF	OFF	**ON**
	S_{04}	OFF	OFF	OFF	OFF
$V_{C1} < V_{C2}$	S_{10}	OFF	OFF	OFF	OFF
	S_{11}	OFF	OFF	**ON**	OFF
	S_{12}	**ON**	OFF	**ON**	OFF
	S_{13}	OFF	OFF	**ON**	OFF
	S_{14}	OFF	OFF	OFF	OFF

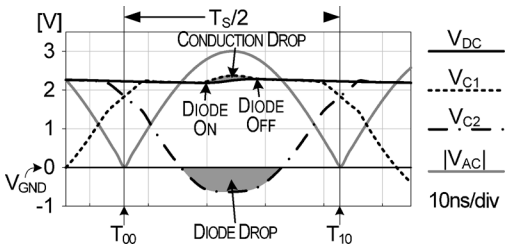

Fig. 5. Simulation result of full-wave rectifier with cross-coupled pMOS and diode connected nMOS.

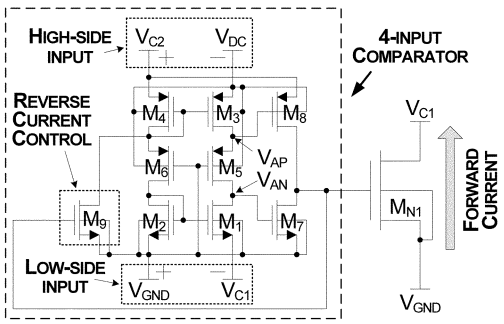

Fig. 6. Active diode with RCC.

matched, in addition to having the same W/L ratio, their respective drain, gate and source voltages are forced to be the same by proper biasing. Now, transistors M_1, M_3 and M_5 are symmetrically-matched with M_2, M_4 and M_6 to achieve low systematic offset. Transistor M_5 also serves two purposes. First, it is used to match with the bias-limiting transistor M_6. Second, it serves as a resistor such that $V_{\rm AP}$ and $V_{\rm AN}$ rise and fall with different time constants, thus generates a small dead-time between turning on and off M_7 and M_8, and reduces the shoot-through current during transient. From the simulation results shown in Fig. 4, we learn that the diode has to cut off quickly at $t = T_{03}$ (and T_{13}). Otherwise, there will be reverse current. In the proposed design, transistor M_9 is added and synchronized with $M_{\rm n1}$. When $M_{\rm n1}$ is turned on by the comparator, M_9 is turned on also and introduces a current offset to the comparator. Transistor M_3 is turned on harder and $V_{\rm AP}$ and $V_{\rm AN}$ rise faster to turn off $M_{\rm n1}$ earlier before it would be reversely biased, thus achieving reverse-current control (RCC). This technique effectively compensates for the delay of the comparator. Simulation and measurement results in Section IV show that under the same input ac voltage magnitude and loading condition, the rectifier with RCC produces a larger dc output voltage, higher power conversion efficiency and a lower output ripple voltage.

IV. SIMULATION AND MEASUREMENT RESULTS

The proposed full-wave active rectifier was fabricated in a 0.35-μm 4-Metal/2-Poly CMOS process, and the micrograph is shown in Fig. 7. The active area is 0.0055 mm^2 (0.1065 mm^2 including pads). All transistors (except M_5, M_6 and M_9 in D_1 and D_2) have minimum channel length to maximize the operation speed. The chip was carefully layout to have a symmetrical structure in minimizing potential unbalance in parasitic capacitances between V_{C1} and V_{C2}. An active rectifier without RCC (i.e., without M_9) was also fabricated for comparison.

To mimic the operation environment for measuring the performance of the active rectifier, an inductive power link was set up, as shown in Fig. 7. Two rectangular coils (50 mm × 60 mm), each with three turns, were etched on two printed circuit boards (PCBs). The measured inductance of each coil was around 900 nH. A signal generator was used to drive the primary coil on PCB 1 with a 13.56-MHz sinusoidal signal, and energy was then transferred to the secondary coil by inductive coupling. The two coils were aligned and separated by 50 mm to reduce capacitive coupling. A filtering capacitor $C_{\rm O}$ of 200 pF and a load resistor R_L of 1.8-kΩ were mounted on the secondary side (PCB 2). The coil with added resonance capacitors and parasitic capacitors of probes were designed to resonate at around 13.56 MHz. An SOIC package was used for the fabricated active rectifier and the chip was mounted on PCB 2. Measurements were taken by three probes with ground terminals connected to $V_{\rm GND}$ of the active rectifier. The voltage across the secondary coil at resonance ($V_{\rm ac}$) was obtained by subtracting V_{C2} from V_{C1}.

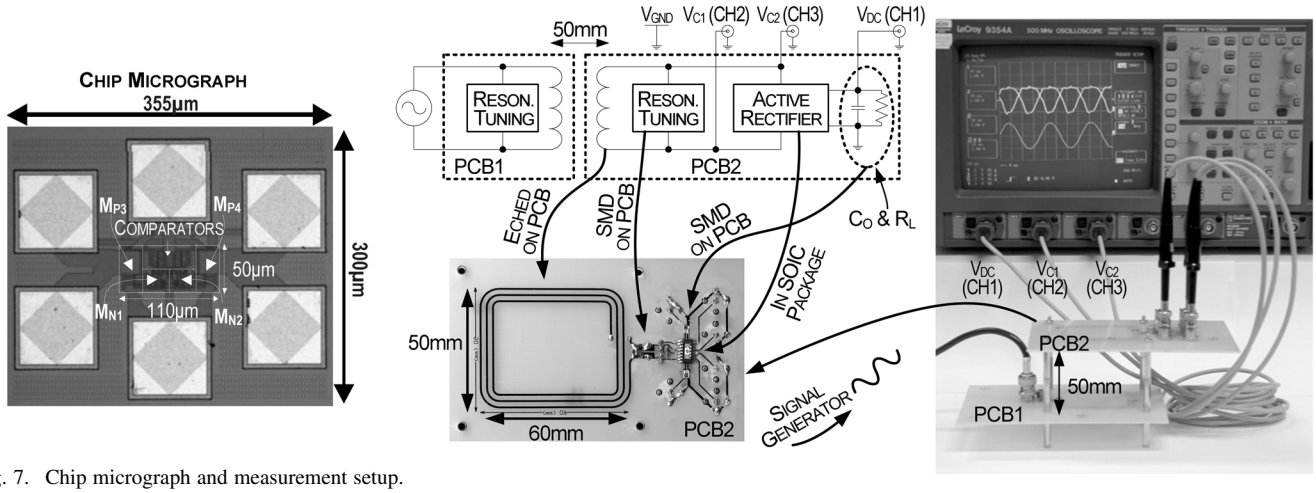

Fig. 7. Chip micrograph and measurement setup.

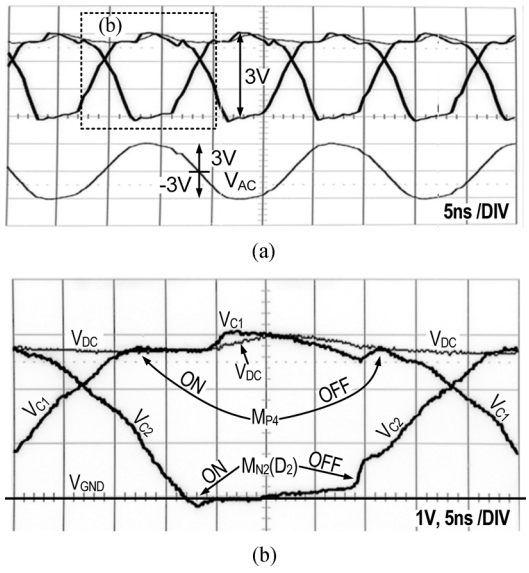

Fig. 8. (a) Measurement results of active rectifier without RCC. (b) Zoom-in view of the first half-cycle.

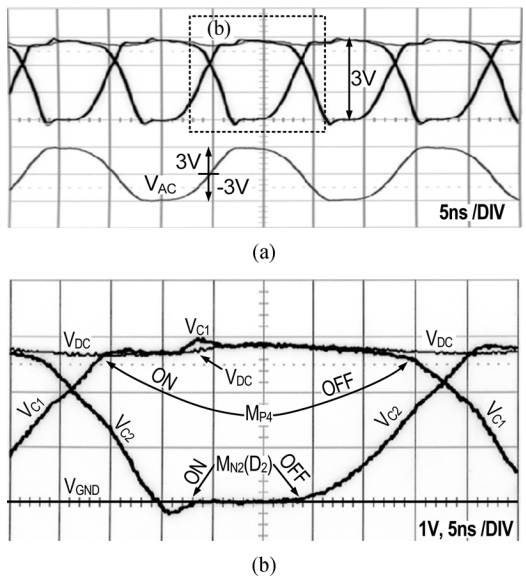

Fig. 9. (a) Measurement results of active rectifier with RCC. (b) Zoom-in view of the first half-cycle.

Fig. 8 shows the measurement results of the proposed active rectifier without RCC. Fig. 8(a) shows that the waveforms of V_{C1} and V_{C2} are similar with a phase shift of 180°, meaning that the active diodes D_1 and D_2 are well matched in on/off thresholds and turn-on/off times. The zoom-in waveform in Fig. 8(b) shows the details of the first half-cycle ($V_{C1} > V_{C2}$). A delay of less than 2 ns is observed for turning on $M_{\rm n2}$ of D_2. When $M_{\rm n2}$ is on, a large current passes through $M_{\rm p4}$ and V_{C1} is then higher than $V_{\rm dc}$, starving the current of M_3 in D_2, and makes $V_{\rm AP}$ and $V_{\rm AN}$ to drop fast, and turns on $M_{\rm n2}$ fast. Note that V_{C1} drops below $V_{\rm dc}$ before $M_{\rm p4}$ is turned off, lowering the rectified dc voltage and thus the efficiency.

Fig. 9 shows the measurement results of the active rectifier with RCC. It has a similar turn-on characteristic with the previous case. The addition of M_9 helps to deliver more current to M_3 (through M_4), thus charging up $V_{\rm AP}$ and $V_{\rm AN}$ earlier, and turns off $M_{\rm n2}$ just in time to prevent reverse current. This action is demonstrated by observing V_{C1} and $V_{\rm dc}$ in Fig. 9(b). V_{C1} does not drops below $V_{\rm dc}$ when $V_{\rm dc} - V_{C2}$ (gate drive voltage of $M_{\rm p4}$) is larger than $|V_{\rm tp}|$. By comparing the $V_{\rm dc}$ waveforms in

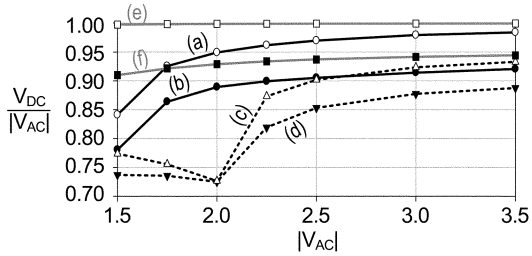

Fig. 10. Measured voltage conversation ratio $M = V_{\rm dc}/|V_{\rm ac}|$ versus $|V_{\rm ac}|$ at $f_s = 13.56$ MHz: (a) with RCC and unloaded, (b) with RCC and $R_L = 1.8\,\text{k}\Omega$, (c) without RCC and unloaded, and (d) without RCC and $R_L = 1.8\,\text{k}\Omega$. Grey lines are simulation results of the rectifier: (e) with ideal diodes and unloaded and (f) with ideal diodes and $R_L = 1.8\,\text{k}\Omega$.

Figs. 8(b) and 9(b), we conclude that the RCC scheme reduces the ripple voltage by half, and a higher dc voltage is obtained. Note that the peak of $V_{\rm ac}$ waveform shown in Fig. 9(a) is flattened due to the current drawn from the secondary coil with finite resistance.

Fig. 10 shows the measurement result of the conversion ratio $M = V_{\rm dc}/|V_{\rm ac}|$ versus the magnitude of the ac input. With the

TABLE II
PERFORMANCE SUMMARY

Chip Area	0.0055mm^2 (active chip area) 0.1065mm^2 (with bond pads)
Technology	0.35μm CMOS 4M2P process
$\lvert V_{tp}\rvert/V_{tn}$	0.73V/0.55V
Input AC frequency	<20MHz
Unloaded Average V_{DC} C_O =200pF	3.45V @ $\lvert V_{AC}\rvert$=3.5V 1.27V @ $\lvert V_{AC}\rvert$=1.5V
Average V_{DC} C_O =200pF, R_L=1.8KΩ	3.22V @ $\lvert V_{AC}\rvert$=3.5V 1.20V @ $\lvert V_{AC}\rvert$=1.5V

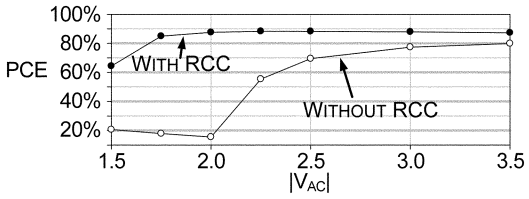

Fig. 11. Simulated power conversion efficiency versus $|V_{\rm ac}|$, $R_L = 1.8\ \text{k}\Omega$.

RCC, when the ac input is 3.5 V, $V_{\rm dc}$ is 3.45 V when unloaded ($M = 0.986$) and 3.22 V with $R_L = 1.8\ \text{k}\Omega$ ($M = 0.92$). Without RCC, $V_{\rm dc}$ drops to 3.25 V when unloaded ($M = 0.929$) and 3.1 V with $R_L = 1.8\ \text{k}\Omega$ ($M = 0.886$). The RCC scheme is effective in reducing the dropout voltage, even when the ac input is lower than 2 V. The rectifier works well with an ac input voltage as low as 1.5 V and a frequency up to 20 MHz. The ideal case shown in Fig. 3(b) with cross-coupled pMOS transistors, ideal diodes, and $R_{\rm ON} = 0.1\ \Omega$ were also simulated with no load and a load of 1.8-kΩ. The performance of the proposed rectifier with RCC is closer to the ideal case, especially at a high-input ac voltage magnitude, because a larger bias current and a larger gate–drive voltage are achieved. Table II summarizes the design parameters and the performance of the proposed active rectifier.

PCE of the proposed rectifier is simulated and the results are shown in Fig. 11. With $R_L = 1.8\ \text{k}\Omega$, the PCE is larger than 87% for an ac input of higher than 2 V. Without RCC, PCE is worse, especially at a low ac input voltage, due to a larger reverse-current leakage.

Fig. 12 shows the measured conversion ratio $M = V_{\rm dc}/|V_{\rm ac}|$ versus input frequency at $|V_{\rm ac}| = 3.5\ V$ and $R_L = 1.8\ \text{k}\Omega$. In the original design, $C_{\rm O}$ of 200 pF is optimized for 13.56-MHz operation. For lower operating frequency, larger $C_{\rm O}$ (2 nF) is required to maintain a high conversion ratio.

V. CONCLUSION

An integrated CMOS active rectifier for wirelessly powered devices is presented. A 4-input comparator with common gate input stages is proposed to effectively drive an nMOS power switch with a performance that matches a zero-threshold diode. Measurement results show that the proposed rectifier has a turn-on delay of less than 2 ns and reverse current is effectively eliminated by a simple RCC scheme. The proposed design could be employed in wirelessly powered biomedical implants and passive RFID tags.

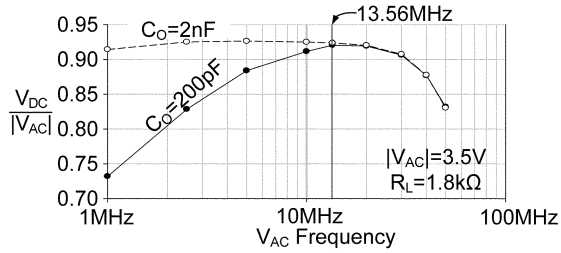

Fig. 12. Measured conversion ratio of the proposed rectifier with the change of input frequency.

REFERENCES

[1] M. Sawan, Y. Hu, and J. Coulombe, "Wirelessly powered and bidirectional data exchanged in smart medical microsystems," in *Proc. IEEE Custom Integr. Circuits Conf.*, San Jose, CA, Sep. 2005, pp. 5–12.

[2] Q. Huang and M. Oberle, "A 0.5-mW passive telemetry IC of biomedical applications," *IEEE J. Solid-State Circuits*, vol. 33, no. 7, pp. 937–946, Jul. 1998.

[3] S. Y. Lee and S. C. Lee, "An implantable wireless bidirectional communication microstimulator for neuromuscular stimulation," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2526–2538, Dec. 2005.

[4] Y. Hu and M. Sawan, "A fully integrated low-power BPSK demodulator for implantable medical devices," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 52, no. 12, pp. 2552–2562, Dec. 2005.

[5] D. Fredman, H. Heinrich, and D.-W. Duan, "A low-power CMOS integrated circuit for field-powered radio frequency identification tags," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1997, pp. 294–295, 474.

[6] S. Masui, E. Ishii, T. Iwawaki, Y. Sugawara, and K. Sawada, "A 13.56-MHz CMOS RF identification transponder integrated circuit with a dedicated CPU," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 1999, pp. 162–163.

[7] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suzuki, and S. Otaka, "A 950-MHz rectifier circuit for sensor networks with 10 m-distance," *IEEE J. Solid-State Circuits*, vol. 41, no. 1, pp. 35–41, Jan. 2006.

[8] H. Nakamoto *et al.*, "A passive UHF RFID tag LSI with 36.6% efficiency CMOS-only rectifier and current-mode demodulator in 0.35-μm FeRAM technology," in *Proc. IEEE Int. Solid-State Circuits Conf.*, Feb. 2006, pp. 310–311, 655.

[9] M. Ghovanloo and K. Najafi, "Fully integrated wideband high-current rectifiers for inductively powered devices," *IEEE J. Solid-State Circuits*, vol. 39, no. 11, pp. 1976–1984, Nov. 2004.

[10] Y.-H. Lam, W.-H. Ki, and C.-Y. Tsui, "An integrated 1.8- to 3.3-V regulated voltage doubler using active diodes and dual-loop voltage follower for switch-capacitive load," in *Proc. IEEE VLSI Circuits Symp.*, Jun. 2006, pp. 104–105.