An Integrated Power-Efficient Active Rectifier With Offset-Controlled High Speed Comparators for Inductively Powered Applications

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***Abstract*—We present an active full-wave rectifier with offset-controlled high speed comparators in standard CMOS that provides high power conversion efficiency (PCE) in high frequency (HF) range for inductively powered devices. This rectifier provides much lower dropout voltage and far better PCE compared to the passive on-chip or off-chip rectifiers. The built-in offset-control functions in the comparators compensate for both turn-on and turn-off delays in the main rectifying switches, thus maximizing the forward current delivered to the load and minimizing the back current to improve the PCE. We have fabricated this active rectifier in a 0.5-μm 3M2P standard CMOS process, occupying 0.18 mm^2 of chip area. With 3.8 V peak ac input at 13.56 MHz, the rectifier provides 3.12 V dc output to a 500 Ω load, resulting in the PCE of 80.2%, which is the highest measured at this frequency. In addition, overvoltage protection (OVP) as safety measure and built-in back telemetry capabilities have been incorporated in our design using detuning and load shift keying (LSK) techniques, respectively, and tested.**

***Index Terms*—Active rectifier, back telemetry, high speed comparators, implantable microelectronic devices, inductive power transmission, load shift keying, offset control, RFID.**

I. Introduction

IMPLANTABLE microelectronic devices (IMD) powered by internal batteries suffer from their large volume, limited lifetime, replacement hardship, and cost. Therefore, they are only suitable for medical treatments with ultra low power requirements, such as pacing the heart, which have extended battery lifetimes in the range of several years [1]. On the other hand, there are treatments, such as neuroprostheses like cochlear and retinal implants, which require orders of magnitude higher currents for stimulation or recording regardless of the circuit efficiency [2]. There are also applications such as radio frequency identification (RFID), in which the size and cost of neither primary nor secondary (i.e., rechargeable) batteries are justified [3]. To address these limitations, wireless power transmission techniques using inductive links have been utilized to supply size-, cost-, and power-constrained devices and applications.

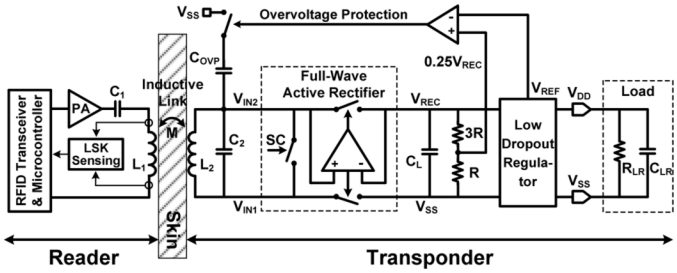

Fig. 1. Block diagram of an inductively powered implantable microelectronic device (IMD) with emphasis on the power transmission/conditioning circuitry.

Inductively powered systems in general consist of three main components: reader, inductive link, and transponder, as shown in Fig. 1. On the reader side, which is also the power transmitter, a power amplifier drives the primary coil, L_1, at the power carrier frequency, f_c. This signal is induced on to the secondary coil, L_2, through the inductive link, and generates an ac voltage across the transponder resonance circuit, L_2 and C_2. Following the L_2C_2 tank, there is always a rectifier to convert the ac signal to dc ($V_{\rm REC}$) for supplying the rest of the transponder. The efficiency and performance of this rectifier, which is the focus of this article, is key to the overall power efficiency of the system, because all the usable received power passes through it. Since the dc voltage varies significantly with the coils' relative distance, d, and alignment, a low dropout regulator often follows the rectifier for providing a constant supply voltage, V_{DD}, to the IMD or RFID load.

Considering the power flow from the external energy source (i.e., the battery) to the load, R_{LR}, the total power conversion efficiency (PCE) can be calculated from

$$\eta_{\rm total} = \eta_{PA} \times \eta_{\rm link} \times \eta_{\rm rectifier} \times \eta_{\rm regulator} \qquad (1)$$

where η_{PA}, $\eta_{\rm link}$, $\eta_{\rm rectifier}$, and $\eta_{\rm regulator}$ are the efficiencies of the power amplifier, inductive link, rectifier, and regulator, respectively. Achieving higher PCE ($\eta_{\rm total}$) is very important in inductively powered applications because it allows IMDs to operate with smaller received power from a larger distance. Lower received power also reduces the risk of tissue damage from overheating [2]. In the IMD applications, $\eta_{\rm link}$ is limited due to the size constraint of the secondary coil [4]. The regulator, on the other hand, already has a high $\eta_{\rm regulator}$ because of its

Manuscript received June 25, 2010; revised October 08, 2010; accepted December 08, 2010. Date of publication January 31, 2011; date of current version July 27, 2011. This work was supported in part by the National Institute of Health Grants 1R01NS062031, 5R21EB009437, and the National Science Foundation under Award ECCS-824199. This paper was recommended by Associate Editor J. S. Chang.

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Digital Object Identifier 10.1109/TCSI.2010.2103172

low dropout topology. Therefore, improving the rectifier PCE ($\eta_{\text{rectifier}}$) is a key factor for safe IMD operation.

Passive rectifiers using diodes or diode-connected transistors have been used in the past for inductively powered applications [5]–[9]. However, PN junction diodes induce large forward voltage drops and power dissipation. Schottky diodes have low dropout voltages [10]. However, they have a high leakage current, they are not available in most standard CMOS processes, and may need extra fabrication steps. Their reverse breakdown voltages may not be high enough either. Several V_{Th} cancellation techniques have been proposed to reduce the passive diode voltage drop [11]–[14]. However, these are sensitive to process variations and still unable to provide high PCE. Therefore, active synchronous rectifiers using comparator controlled rectifying switches are currently considered the most promising solutions for increasing the PCE in ASICs [15]–[24]. In these rectifiers, voltage drop across the main rectifying switches is much lower than the diode voltage drop, dissipating less power within the rectifier. We previously reported power efficient active rectifiers using phase lead in [16] and [24]. The maximum operating frequency of those rectifiers, however, was limited to 1–2 MHz. Active rectifiers need significantly faster comparators to drive their switches at the right times for higher carrier frequencies, such as 13.56 MHz in the Industrial, Scientific, and Medical (ISM) band, and maximize the forward current flow, while minimizing the reverse currents.

In this paper, we propose an integrated power efficient active rectifier with offset-controlled high speed comparators for inductively powered applications. Comparators are equipped with offset control functions to compensate for both turn-on and turn-off delays, optimizing the power transfer from the secondary coil to the load (regulator). Section II presents the operating principles and the PCE analysis of our new active rectifier architecture. Section III describes the concept, implementation, and effects of the proposed offset-control functions on the high speed comparators. The simulation and measurement results are depicted in Section IV, followed by conclusions in Section V.

II. Active Rectifier Architecture

A. Operating Principle and Implementation

The new full-wave active rectifier employs a pair of high-speed comparators (CMP_1 and CMP_2) to drive the main rectifying elements (P_1 and P_2) in Fig. 2. Ideally, the input voltage of the rectifier, $V_{\text{IN}} = V_{\text{IN1}} - V_{\text{IN2}}$, has a sinusoidal waveform. Hence, P_1 and P_2 turn on alternatively depending on the polarity and amplitude of V_{IN}.

When $V_{\text{IN}} > V_{ThN}$ (the NMOS threshold voltage) and $|V_{\text{IN}}| < V_{\text{REC}}$, the positive feedback operation of the cross-coupled NMOS pair (N_1 and N_2) connects V_{IN2} to V_{SS} through N_2 and turns off N_1. In this case, CMP_2 output goes high because $V_{\text{REC}} > V_{SS}$, and P_2 is turned off. P_1 also remains off as long as $|V_{\text{IN}}| < V_{\text{REC}}$. When $|V_{\text{IN}}| > V_{\text{REC}}$, CMP_1 output goes low and turns P_1 on. Therefore, current flows from V_{IN1} to V_{REC}, and charges the rectifier's resistive/capacitive load ($R_L C_L$). In the next half cycle, when $V_{\text{IN}} < -V_{ThN}$, V_{IN1} is connected to V_{SS} through N_1, N_2 turns off, and both P_1 and P_2 are also initially off for the period of $|V_{\text{IN}}| < V_{\text{REC}}$. Then, after $|V_{\text{IN}}| > V_{\text{REC}}$, CMP_2 turns P_2 on and current flows from V_{IN2} to V_{REC} to charge the resistive/capacitive load again.

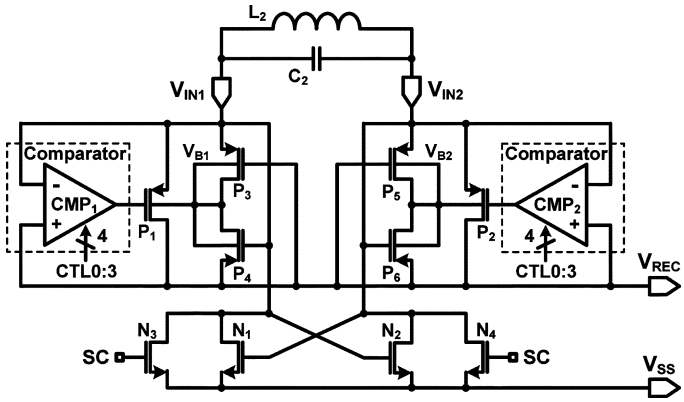


Fig. 2. Schematic diagram of our active rectifier including offset-controlled high speed comparators, dynamic body biasing, and load shift keying (LSK) back telemetry functions.

To avoid latch-up and substrate leakage problems among P_1 and P_2, potentials at their separated N-well body terminals (V_{B1} and V_{B2}) need to be the highest potentials on-chip. We adopted the dynamic body bias control technique from [6] and [25] by utilizing auxiliary PMOS transistors, P_3 to P_6. With this method, V_{B1} and V_{B2} are automatically connected to the highest potential between the input voltages, V_{IN1} and V_{IN2}, and the output voltage, V_{REC}, of the rectifier.

B. Back Telemetry and Overvoltage Protection

To add back telemetry capability, which is desired to inform the reader about the status of the IMD, deliver measured biosignals, or close the power control loop [26], [27], we have employed the load shift keying (LSK) scheme by shorting the secondary coil, L_2, with the short-coil (SC) data signal [9]. A pair of NMOS switches, N_3 and N_4, has been added in parallel to the cross-coupled N_1 and N_2, respectively. When the data signal is high, the input nodes of the rectifier are shorted together, leading to increased secondary quality factor, Q_2, and increased voltage across the primary coil, L_1. Back telemetry data from the transponder to the reader is detected by sensing these variations across the external LSK sensing block in Fig. 1.

V_{IN} highly depends on the coils mutual coupling, M, which is in turn highly dependent on the coils separation, d, and alignment [4]. Loading variations also change Q_2 and affect V_{IN} even when M is constant. Unexpected variations in M and R_{LR} may cause V_{REC} to exceed the safe voltage limits of the application or fabrication process and result in transistor breakdown. To prevent this problem, we have added an overvoltage protection (OVP) circuit to the rectifier by comparing a quarter of V_{REC} with a constant reference voltage. When V_{IN} exceeds a certain level, the comparator output goes high and a detuning capacitor (C_{OVP}) is added in parallel across the secondary tank circuit, as shown in Fig. 1, to reduce V_{IN} by detuning it. The advantage of this method over current leakage based techniques [10] is that no extra heat is dissipated within the ASIC and IMD as a result of this protective safety measure.

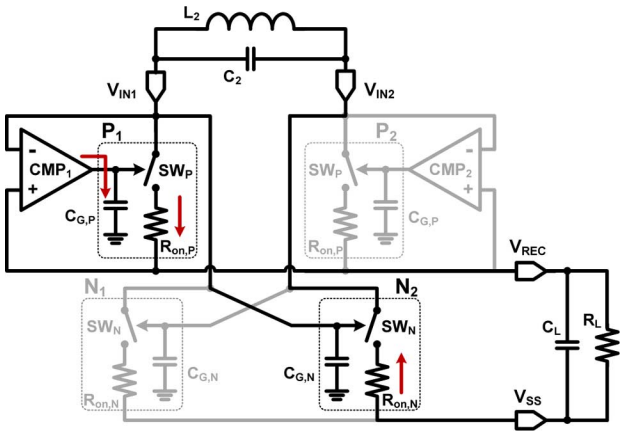


Fig. 3. Simplified schematic diagram of the active rectifier depicting the current path and power dissipating components when $V_{\rm IN1} - V_{\rm IN2} > V_{\rm REC}$.

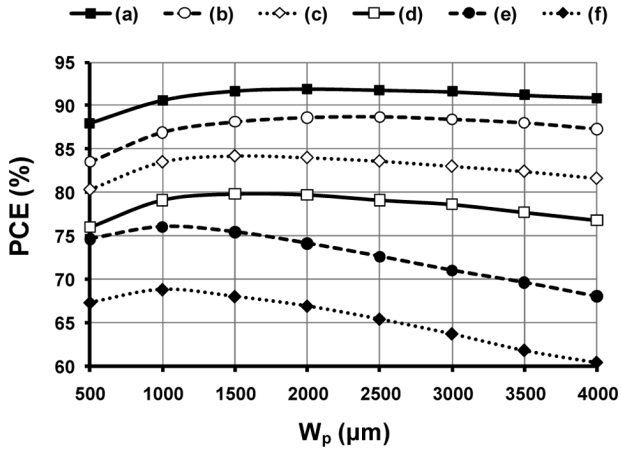


Fig. 4. Calculated rectifier power conversion efficiency (PCE) versus W_p depending on the comparator delays when $V_{\rm REC} = 3.2$ V and $R_L = 500\ \Omega$. Curve-a: $T_{PHL} = 0$ ns and $T_{PLH} = 0$ ns; Curve-b: $T_{PHL} = 5$ ns and $T_{PLH} = 0$ ns; Curve-c: $T_{PHL} = 0$ ns and $T_{PLH} = 3$ ns; Curve-d: $T_{PHL} = 3$ ns and $T_{PLH} = 3$ ns; Curve-e: $T_{PHL} = 0$ ns and $T_{PLH} = 4$ ns; and Curve-f: $T_{PHL} = 4$ ns and $T_{PLH} = 4$ ns.

C. PCE Analysis and Considerations

PCE depends on the size of the rectifying PMOS and the cross-coupled NMOS pairs because these transistors are in the main current path. For example, when $V_{\rm IN1} - V_{\rm IN2} > V_{\rm REC}$, P_1 and N_2 turn on and open a current path to the load, as shown in Fig. 3. In this case, the total lost power, $P_{\rm Loss,total}$, will be dominated by the switching loss of $P_1(P_{{\rm Loss},Cgp})$, $R_{\rm on}$ loss of $P_1(P_{{\rm Loss},Ronp})$, and $R_{\rm on}$ loss of $N_2(P_{{\rm Loss},Ronn})$. Since the gate of N_2 is always connected to the input node of the rectifier, there is negligible switching loss for charging and discharging the gate capacitance of N_2. Therefore, $P_{\rm Loss,total}$ can be approximated by

$$\begin{aligned} P_{\rm Loss,total} &= P_{{\rm Loss},C_{gp}} + P_{{\rm Loss},R_{onp}} + P_{{\rm Loss},R_{onn}} \\ &= C_{gp}V_{\rm REC}^2 2f_c + I_p^2 R_{onp} D_{\rm eff} \\ &\quad + I_n^2 R_{onn} D_{\rm eff} \\ &= W_p C_{gp}^* V_{\rm REC}^2 2f_c + \left(\frac{V_{\rm REC}}{R_L D_{\rm eff}}\right)^2 \\ &\quad \times D_{\rm eff}\left(R_{onp} + R_{onn}\right) \end{aligned} \tag{2}$$

where C_{gp}^* is the gate capacitance per unit width of P_1, f_c is the carrier frequency (13.56 MHz), $D_{\rm eff}$ is the effective duty cycle including comparator delay, and W_p is the width of P_1.

In this design, we have assumed $W_n = W_p$ for the sake of simplicity. However, we have also proven in [24] that the optimal size ratio of the PMOS and NMOS transistors can be found from

$$\left(\frac{W_p}{W_n}\right)_{opt} = \sqrt{\frac{K_n \cdot (V_{\rm REC} - V_{ThN})}{K_p \cdot (V_{\rm REC} - |V_{ThP}|)}} \tag{3}$$

where $K_p = \mu_p C_{\rm ox}$ and $K_n = \mu_n C_{\rm ox}$ are the PMOS and NMOS transconductances, respectively. One should note that even though larger transistor size decreases the $R_{\rm on}$ loss, it increases the switching loss and comparator delays due to the larger gate capacitance. Therefore, the main rectifying transistors have an optimal size for minimum power dissipation depending on f_c and R_L, which should also comply with the total chip area that is allocated to the rectifier [24].

T_{PHL} and T_{PLH}, the turn-on and turn-off delays of $\rm CMP_{1,2}$, affect the rectifier PCE because these delays hinder $P_{1,2}$ switches from turning on and off at proper times and cause back current. Our model considers the size of the rectifying transistors and comparator delays to estimate the maximum PCE. In the Appendix, we have defined W_p, $R_{onp} + R_{onn}$, and $D_{\rm eff}$ as functions of the switching duty cycle (D), T_{PHL}, and T_{PLH}, and differentiated (2) with respect to D to minimize $P_{\rm Loss,total}$. With the power loss from (2), we can estimate the maximum PCE of the rectifier

$$\eta_{\rm rectifier} = \frac{P_{\rm Load}}{P_{\rm Load} + P_{\rm Loss,total} + 2P_{\rm Comparator}} \tag{4}$$

where $P_{\rm Load}$ is the output power, and $P_{\rm Comparator}$ is the total power consumption of each comparator excluding the charging and discharging power consumption of $P_{1,2}$ gates, which has already been considered in $P_{\rm Loss,total}$.

Fig. 4 shows the calculated rectifier PCE versus W_p for various comparator delays, using parameters from the ON Semi 0.5-μm standard CMOS process. In this calculation, we assume that $P_{\rm Load} = 20$ mW, $V_{\rm REC} = 3.2$ V, $R_L = 500\ \Omega$, and $P_{\rm Comparator} = 0.1$ mW, which are based on the simulation results. It can be seen that with $W_p = 2100\ \mu$m and $T_{PHL} = T_{PLH} = 0$ ns, the rectifier achieves the highest PCE of 92%. This is the theoretical upper limit for the PCE that can be obtained by choosing optimized transistor width and eliminating the effect of comparators' delay by utilizing offset-controlled high speed comparators that are described in Section III.

III. Offset-Controlled High Speed Comparators

A. Concept of the Offset-Control Function

In order to drive the large rectifying PMOS transistors at high operating frequency of 13.56 MHz, high speed comparators with low power consumption and high driving capability are required. Typically, the comparator operating speed is limited by its propagation delay, T_P, which is how quickly the output responds to a change at the input. In this rectifier application,

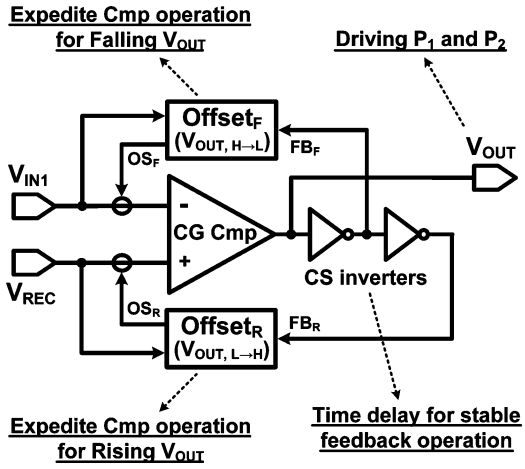
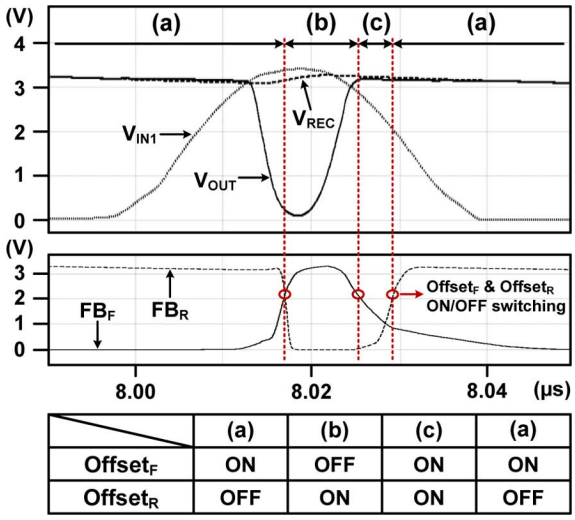


Fig. 5. Block diagram of the high speed comparator employing offset control functions for both falling and rising $V_{\rm OUT}$ transitions.



	(a)	(b)	(c)	(a)
$Offset_F$	ON	OFF	ON	ON
$Offset_R$	OFF	ON	ON	OFF

Fig. 6. Simulated waveforms and timing diagram showing the operation of the offset-control blocks in the high speed comparators.

the comparator propagation delay adversely affects the PCE. Due to T_{PHL}, the comparators turn $P_{1,2}$ on too late and reduce the input power that could otherwise be transferred to the load during this delay. Moreover, due to T_{PLH}, comparators lag in turning $P_{1,2}$ off, and current can instantaneously flow from C_L back to the secondary coil when $V_{\rm IN} < V_{\rm REC}$.

Since it is not possible to reduce T_P to zero, in order to overcome such limitations, we have utilized offset control function in the high speed comparators used in this rectifier. Fig. 5 shows the block diagram of this comparator, which consists of a common-gate type comparator (CG Cmp), two offset-control blocks ($\rm Offset_F$ and $\rm Offset_R$), and current-starved (CS) inverters. Offset-control blocks inject a programmable offset current, OS_F and OS_R, to the inputs of the CG comparator alternately depending on the state of the $V_{\rm OUT}$ feedback signals, FB_F and FB_R. Therefore, $V_{\rm OUT}$ expedites the falling or rising transition by sensing them ahead of time.

Segment-(a) in Fig. 6 exhibits a falling $V_{\rm OUT}$ transition, occurring when $|V_{\rm IN}| = |V_{\rm IN1} - V_{\rm IN2}| > V_{\rm REC}$. At this point, the CG comparator output, $V_{\rm OUT}$, falls to turn on P_1 (or P_2). FB_F is low during this period, and only the $\rm Offset_F$ block operates to inject offset current to the negative input of the CG comparator. With the help of $\rm Offset_F$, $V_{\rm OUT}$ can be forced to fall even before $|V_{\rm IN}|$ exceeds $V_{\rm REC}$ at the end of segment-a, compensating for the comparators' turn-on delay. It is important, however, to note that $\rm Offset_F$ has to be turned off after the $V_{\rm OUT}$ falling transition so that it does not affect the following $V_{\rm OUT}$ rising transition. Otherwise, $\rm Offset_F$ can delay the rising $V_{\rm OUT}$ transition, which is counterproductive. This is why in Fig. 5 the $\rm Offset_F$ block receives a feedback signal from $V_{\rm OUT}$ and properly turns off after every falling transition of $V_{\rm OUT}$.

On the other hand, during the $V_{\rm OUT}$ rising transition in segment-(b), when $|V_{\rm IN}| < V_{\rm REC}$, FB_R that has gone low after $V_{\rm OUT}$ falling, turns on the $\rm Offset_R$ block. The $\rm Offset_R$ block injects offset current to the positive input of the CG comparator and can force $V_{\rm OUT}$ to start rising even before $|V_{\rm IN}|$ falls below $V_{\rm REC}$. This helps P_1 (or P_2) to turn off at a proper time and prevents the back current.

If the $\rm Offset_R$ block turns on just after $V_{\rm OUT}$ starts to fall, this instantaneous negative feedback mechanism hinders $V_{\rm OUT}$ from falling down fully and causes $V_{\rm OUT}$ to fluctuate. To avoid this problem, we have added two current-starved inverters in the feedback loop to add a delay between $V_{\rm OUT}$, FB_F, and FB_R transitions, thus assuring stable comparator feedback operation. This delay does not need to be precise as long as it is less than one carrier cycle period. It results in a short period, segment-(c), during which both $\rm Offset_F$ and $\rm Offset_R$ blocks are on.

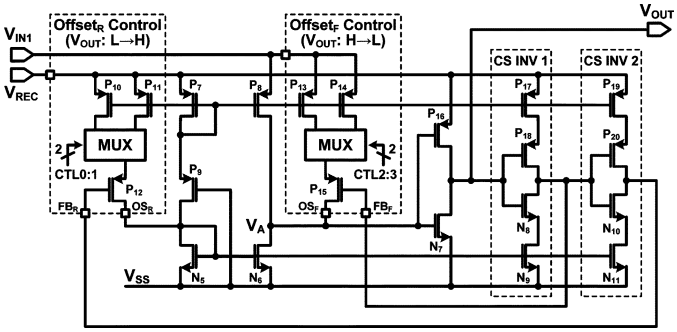


Fig. 7. Schematic diagram of the high speed comparator with two offset-control functions, $\rm Offset_F$ for the $V_{\rm OUT}$ falling edge and $\rm Offset_R$ for the $V_{\rm OUT}$ rising edge.

B. Circuit Implementation

Fig. 7 shows the schematic diagram of the high speed comparator with two offset-control functions, $\rm Offset_F$ and $\rm Offset_R$. Without considering offset-control blocks and CS inverters, it basically works as a simple common-gate comparator with start-up capability [15]. Two input voltages, $V_{\rm REC}$ and $V_{\rm IN1}$, are applied to the sources of input transistors, P_7 and P_8, respectively. When $V_{\rm IN1} > V_{\rm REC}$, the current flowing through P_8 becomes larger than that of P_7. Therefore, the gate voltage of the output inverter, V_A, rapidly increases, and $V_{\rm OUT}$ falls to turn P_1 on. The $\rm Offset_F$ and $\rm Offset_R$ blocks are implemented by using current sources, P_{13}–P_{14} and P_{10}–P_{11}, within the comparator, MUXs, and the control switches, P_{15} and P_{12}. These blocks inject offset currents to the comparator inputs alternatively, inducing the desired timing. For example, when $V_{\rm OUT}$ is high, P_{15} turns on, and an offset current flows into

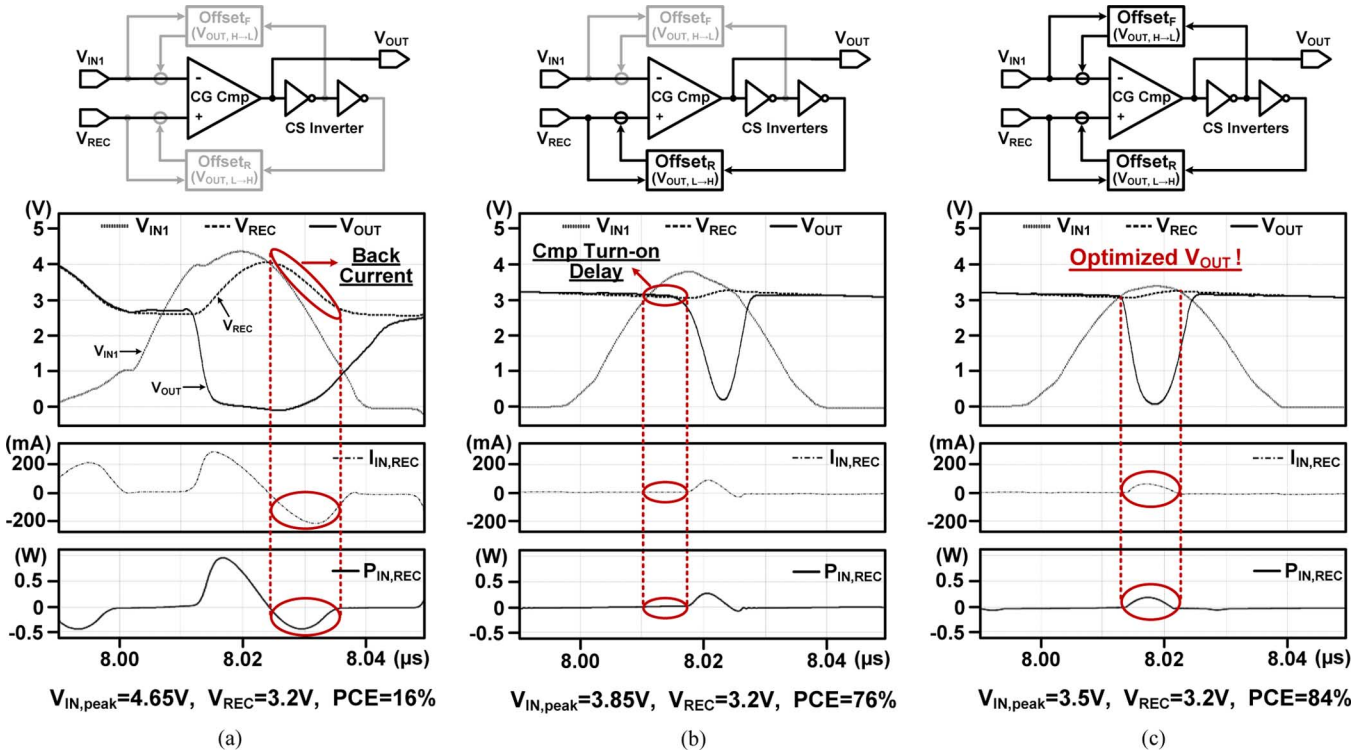


Fig. 8. Simulation results of the active rectifier showing waveforms of the input/output voltages, input current, and input power with $V_{\rm REC} = 3.2$ V and $R_L = 500\ \Omega$, (a) without any offset-control function, (b) with only Offset_R function, and (c) with both Offset_F and Offset_R functions.

the comparator positive input branch $(V_{\rm REC})$ through OS_F, causing V_A to increase. Therefore, $V_{\rm OUT}$ starts to fall earlier before $V_{\rm IN1}$ exceeds $V_{\rm REC}$. The offset current is programmable by using 2-bit off-chip control signals per offset-control block, CTL0:1 and CTL2:3, in order to adjust the rectifier timing in response to process variations.

C. Effects of Offset-Control Functions on PCE

Simulation results depicting the relationship between the PCE and offset-control functions are shown in Fig. 8. To understand the effects of the offset-control functions better, we have overlapped the rectifier input/output voltages, input current, and input power waveforms while adjusting $V_{\rm IN}$ amplitude to achieve a constant $V_{\rm OUT} = 3.2$ V for $R_L = 500\ \Omega$. Fig. 8(a) shows that with no comparator offset-control function in place, the back current resulting from the turn-off delay severely degrades the PCE. This back current can be prevented by using the Offset_R function, as shown in Fig. 8(b). Even though Offset_R improves the PCE significantly, the input power to the rectifier is still being reduced due to the comparators' turn-on delay, T_{PHL}. Therefore, there is room to further improve the rectifier PCE as well as voltage conversion efficiency (VCE) by using both Offset_F and Offset_R functions to compensate for T_{PHL} and T_{PLH} delays, respectively. Fig. 8(c) clearly shows that with both functions in place $V_{\rm OUT}$ transitions happen at the right times, and the PCE is maximized.

Since the offset-control blocks consume additional power to provide the offset currents, the power overhead for employing these functions needs to be considered. Fig. 9 shows the simulated comparator power consumption versus $V_{\rm REC}$ and its break down between the two blocks. When $V_{\rm REC}$ increases, the power consumption of the CG comparator, curve-(b) also increases, contributing a large portion of the comparator power consumption, curve-(a). This is because both the static current of the CG comparator and the shoot-through current of the output inverter increase with $V_{\rm REC}$. Moreover, since the comparator offsets have been tuned for $V_{\rm REC} = 3.12$ V, power consumption becomes more severe at higher $V_{\rm REC}$. On the other hand, curve-(c), the offset-control blocks' power consumption shows a mild increase when $V_{\rm REC}$ increases. It is because the offset-control blocks consume only dynamic power for a short period. For $V_{\rm REC} = 3.12$ V, the entire high speed comparator consumes 135 μW, 40 μW of which is the power consumption of the offset-control blocks. The entire comparator power consumption is little affected by the load conditions as long as $V_{\rm REC}$ is fixed.

D. Startup Capability

Since no supply voltage is available before the active rectifier starts its operation, it is necessary for the rectifier to have self startup capability. Our high speed comparator, shown in Fig. 7, has a common-gate input stage, in which the two comparator input voltages, $V_{\rm IN1}$ and $V_{\rm REC}$, are also the positive supply voltages. Hence the rectifier sinusoidal input voltage, $V_{\rm IN1,2}$, guarantees that the rectifier reliably starts up even before $V_{\rm REC}$ is sufficiently charged up. For example, when $V_{\rm REC} = 0$ V, the input voltage of the output inverter, V_A, follows $V_{\rm IN1}$ through P_8, since N_6 is turned off. Therefore, when $V_{\rm IN1} > V_{ThN7}$, $V_{\rm OUT}$ of the comparator will be connected to V_{SS} through N_7 leading the rectifying PMOS to turn on and charge $V_{\rm REC}$.

Since the comparator bias current is generated by P_7–P_9–N_5 branch, it properly turns on when $V_{\rm REC} > V_{ThP7} + V_{ThN5}$.

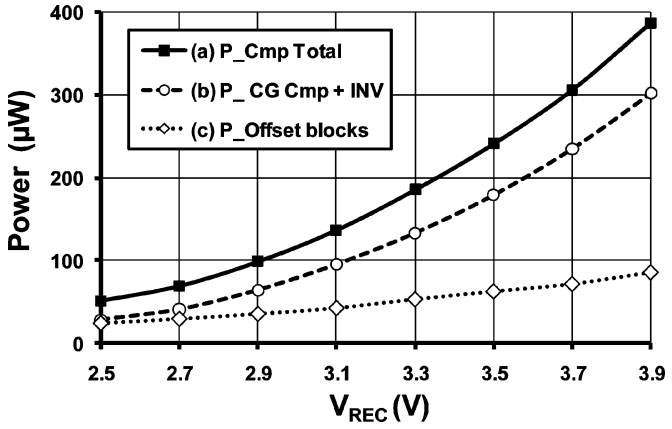


Fig. 9. Simulated power consumption of the comparator versus $V_{\rm REC}$ showing power overheads for employing the offset-control functions ($f_c = 13.56$ MHz, $R_L = 500\ \Omega$, and $C_L = 10\ \mu$F). Curve (a) shows the total power consumption of the high speed comparator, (b) is the power consumption of the CG comparator and CS inverters, and (c) indicates the consumption of the offset-control blocks.

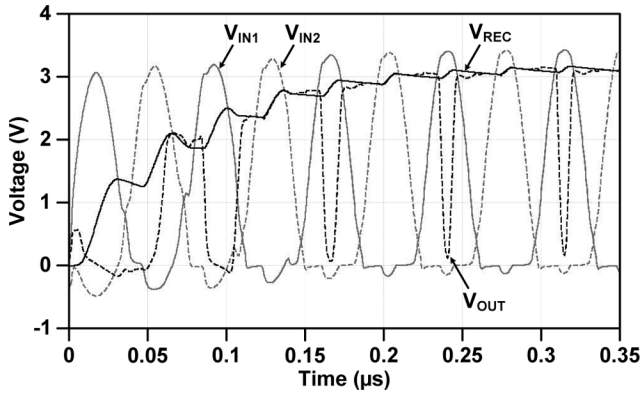


Fig. 10. Simulated waveforms for self startup operation of the active rectifier ($f_c = 13.56$ MHz, $V_{\rm IN,peak} = 3.4$ V, $V_{\rm REC} = 3.12$ V, $R_L = 500\ \Omega$, and $C_L = 2.5$ nF).

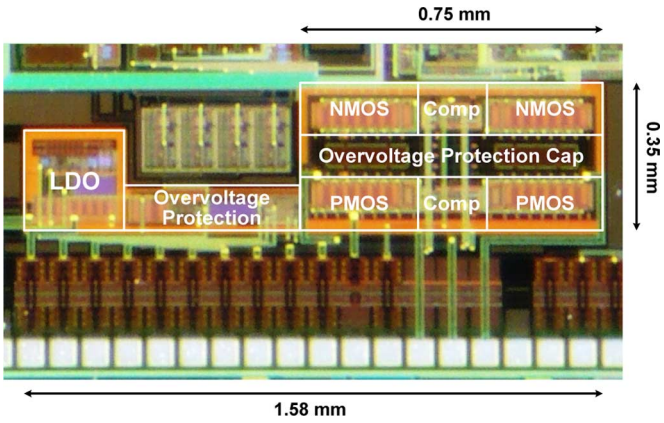


Fig. 11. Fabricated chip micrograph and its floor plan, including the active rectifier, overvoltage protection circuit, and low dropout regulator.

On the other hand, when $0 < V_{\rm REC} < V_{ThP7} + V_{ThN5}$, the comparator still turns on the rectifying PMOS for conducting current to $V_{\rm REC}$, as explained above, but it does not turn them off at the right time, resulting in back current. Now, if $V_{\rm IN,peak}$ is high enough (> 2.9 V in our design), then it will be sufficient for charging $V_{\rm REC}$ to surpass the $V_{ThP7} + V_{ThN5}$ level even in the presence of the back current. While $V_{\rm REC}$ is being charged, the gate voltage of $N_{5,6}$ also increases, and V_A decreases to turn off the rectifying PMOS during $V_{\rm IN1} < V_{\rm REC}$. Moreover, the comparator operation and the rectifier PCE move towards their optimal points as $V_{\rm REC}$ increases toward the target value of 3.12 V. Therefore, once $V_{\rm REC}$ exceeds $V_{ThP7} + V_{ThN5}$, it can easily charge up to 3.12 V. Fig. 10 shows simulated waveforms for the rectifier self startup process, which guarantees that $V_{\rm REC}$ is charged up to 3.12 V when $V_{\rm IN,peak} = 3.4$ V (3.8 V in measurements). In this design, for an input voltage of $V_{\rm IN,peak} = 2.9$ V (3.2 V in meas.), the suboptimal operation of the rectifier results in $V_{\rm REC} = 2.5$ V.

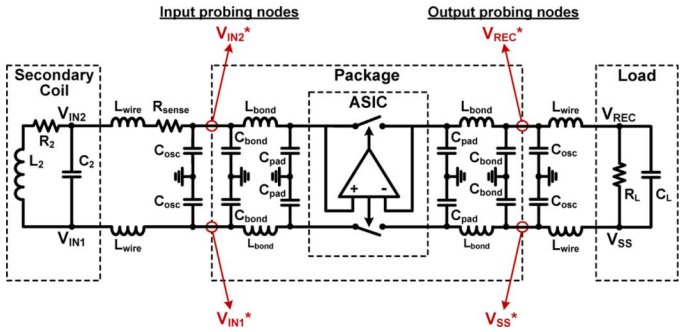


Fig. 12. Lumped model of the circuit used in active rectifier simulations, showing capacitive and inductive parasitic components of the wire-bond and external interconnects. It is important to note that because of these parasitics, voltages measured on the coil or load, V_{XY}, are not exactly the same as those measured on the ASIC package (LQFP176), $V_{XY}{}^*$.

IV. Simulation and Measurement Results

The active rectifier was fabricated in the ON Semiconductor 0.5-μm 3M2P standard CMOS process (minimum transistor length of 0.6 μm) for its relatively high voltage handling capability. Fig. 11 shows the chip micrograph, which includes the active rectifier, overvoltage protection circuit, and the low dropout regulator, occupying 0.4 mm^2 of the Si area with $W_p/L_p = W_n/L_n = 2100\ \mu$m/0.6 μm. Since each comparator offset-control function can be enabled or disabled by external control lines, we were able to evaluate the rectifier performance with and without the comparator offset functions.

A. Measured Waveforms and Parasitic Effects

Fig. 12 shows the lumped model of the circuit used in the rectifier measurements with emphasis on the inductive and capacitive parasitic components, which combined with the measurement instrument (oscilloscope) parasitic, cause distortion in the measured waveforms at this relatively high operating frequency ($f_c = 13.56$ MHz). For instance, when the rectifier starts conducting, there is a sudden drop in $V_{\rm IN1} - V_{\rm IN2}$, and when it stops conducting, the stored energy in the interconnect inductors cause a sudden voltage hike across the rectifier inputs. Therefore, it is important to note that the voltages measured across the coil or load, V_{XY}, are not exactly the same as those measured on the rectifier packaged IC pins, V^*_{XY} (LQFP176). For example, $L_{\rm bond}$, the parasitic inductance of the wirebond, and $L_{\rm wire}$, the parasitic inductance of the external interconnects, cause the rectifier input voltage at the package, $V^*_{\rm IN1} - V^*_{\rm IN2}$, to be distorted and have a peak voltage higher than the sinusoidal input voltages at the secondary coil, $V_{\rm IN1} - V_{\rm IN2}$.

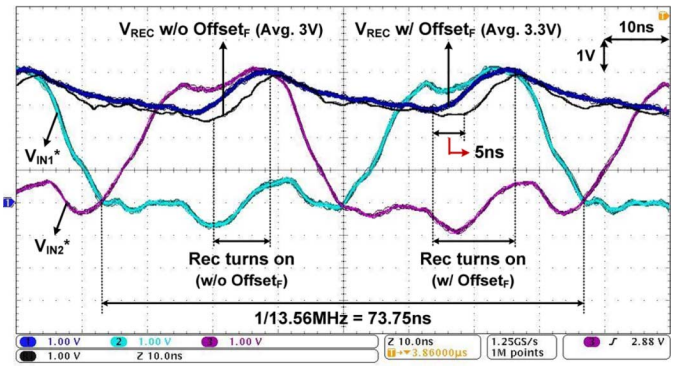


Fig. 13. Measured waveforms of the input and output voltages of the rectifier with and without the Offset_F function ($f_c = 13.56$ MHz, $V_{\text{IN,peak}} = 4.1$ V, $R_L = 500\ \Omega$, and $C_L = 100$ pF).

Moreover, the instantaneous input current flows into the rectifier through the parasitic inductors only during the rectifier turn-on, which is much shorter than one operating cycle (see Fig. 8(c). Therefore, the frequency components, which affect the parasitic inductors and distort the voltage waveforms, are effectively much higher than the carrier frequency at 13.56 MHz. Unfortunately, this effect has not been considered in the recent literature on active rectifiers, and consequently, depending on how the measurements are done, the reported results on the rectifier efficiency might have been optimistic.

Fig. 13 shows the active rectifier measured input and output voltage waveforms. In these measurements we refrained from directly probing V_{OUT} because it could load and affect the comparator performance. Instead, C_L was reduced from 10 μF to 100 pF to better show the effects of offset-control functions. For all measurements and simulations in this section, we enabled the Offset_R to prevent the back currents. When the Offset_F function was enabled, V_{REC} started to increase ~ 5 ns earlier than without Offset_F. This comparison, which is consistent with the simulation results in Fig. 8, shows that the comparators turn the rectifier on faster to deliver current for a longer time period. Therefore, the Offset_F function not only improves the PCE but also reduces the rectifier dropout voltage, V_{drop}, which is defined as the difference between $V_{\text{IN1,peak}}{}^*$ and V_{REC}. There is also a small phase shift between the ripple on V_{REC} and $V_{\text{IN1,2}}{}^*$ due to the parasitic components.

B. PCE and Dropout Voltage Measurements

We measured the PCE and V_{drop} by sweeping 1) V_{REC}; 2) R_L connected directly across the rectifier, substituting the regulator; and 3) f_c. In order to measure the rectifier input current, we connected a small resistor, $R_{\text{sense}} = 10\ \Omega$, in series with the rectifier input as a current sensor and differentially measured the voltage across it. The rectifier input power was calculated offline by integrating the instantaneous product of the input current and voltage samples. The output power for the PCE was obtained by measuring the $V_{\text{REC,RMS}}$. The peak input voltage, $V_{\text{IN,peak}}$, can be expressed as the sum of V_{REC} and V_{drop}.

Fig. 14 shows the measured and simulated PCE and V_{drop} versus V_{REC} with $C_L = 10$ μF, $R_L = 500\ \Omega$, and $f_c = 13.56$ MHz. All simulated results in this section are postlayout and include the estimated parasitic components of the LQFP176 package (see Fig. 12). Fig. 14(a) shows that for $V_{\text{REC}} = 3.12$ V,

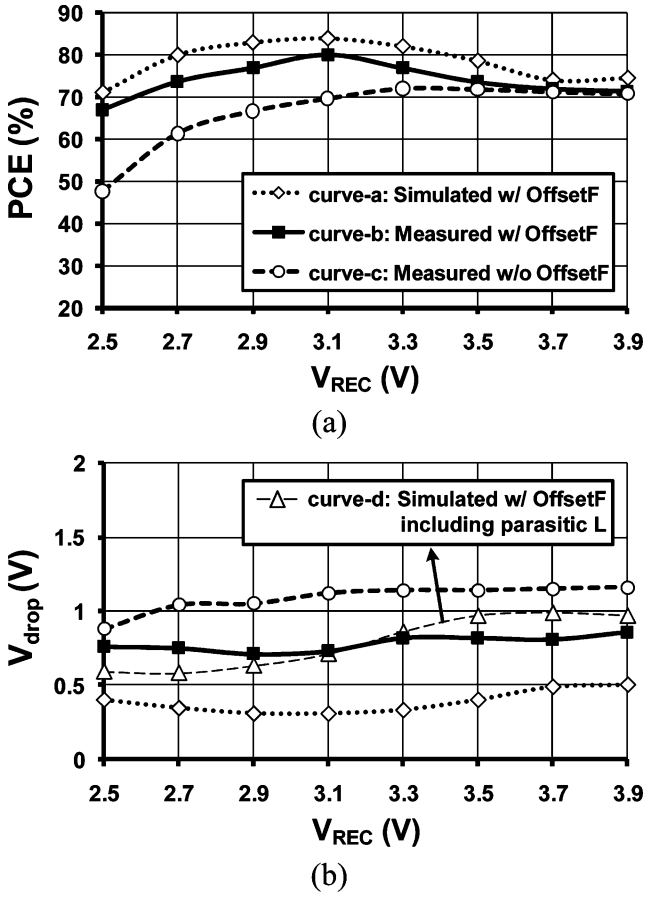


Fig. 14. Measured and simulated (a) PCE and (b) V_{drop} versus V_{REC} when $R_L = 500\ \Omega$, $C_L = 10$ μF, and $f_c = 13.56$ MHz.

the maximum PCE with both offset-control functions was measured to be 80.2% (curve-b), which was slightly lower than the maximum postlayout simulated PCE of 84.5% (curve-a) and schematic simulated PCE of 87% due to the effects of parasitics and the current sensing resistor. The measured PCE without Offset_F (curve-c) is $\sim 10\%$ lower than the PCE with Offset_F. When V_{REC} was higher or lower than 3.12 V, the PCE gradually decreased because the comparator offsets were only adjusted for $V_{\text{REC}} = 3.1$–3.2 V. For other V_{REC} values, the comparator offsets can be easily readjusted using CTL0:3 in Fig. 2.

In Fig. 14(b), the measured V_{drop} with Offset_F (curve-b) shows 0.7 V dropout, which is 0.4 V higher than the simulated V_{drop} with Offset_F (curve-a). This is due to the interconnect inductances increasing $V^*_{\text{IN1,peak}}$ as explained earlier. For example, $V^*_{\text{IN1,peak}}$ was measured ~ 250 mV higher than $V_{\text{IN1,peak}}$ in Fig. 12 after shorting R_{sense}. By including these parasitic inductors in our simulations ($L_{\text{bond}} + L_{\text{wire}} = 25$ nH), we were able to verify the cause of V_{drop} variations by producing results (curve-d) that were closer to the measured V_{drop} (curve-b). V_{drop} is also affected by the output current, I_{REC}, and PCE. In Fig. 14(b), a higher V_{REC} with fixed R_L requires higher I_{REC} through the rectifier, which generates a larger voltage drop across the rectifying transistors, increasing V_{drop}. Furthermore, a rectifier with lower PCE requires more current from the coil to reach a certain V_{REC}, which also increases V_{drop}. Overall, measured and simulated results clearly showed that V_{drop} is reduced by using both offset-control functions.

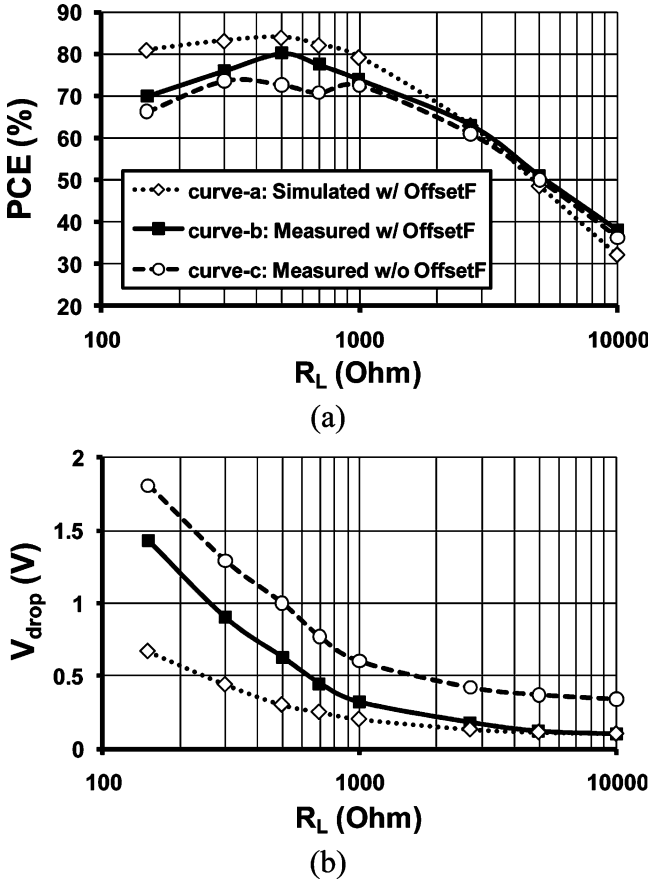


Fig. 15. Measured and simulated (a) PCE and (b) $V_{\rm drop}$ versus R_L with $V_{\rm REC} = 3.12$ V, $C_L = 10\ \mu$F, and $f_c = 13.56$ MHz.

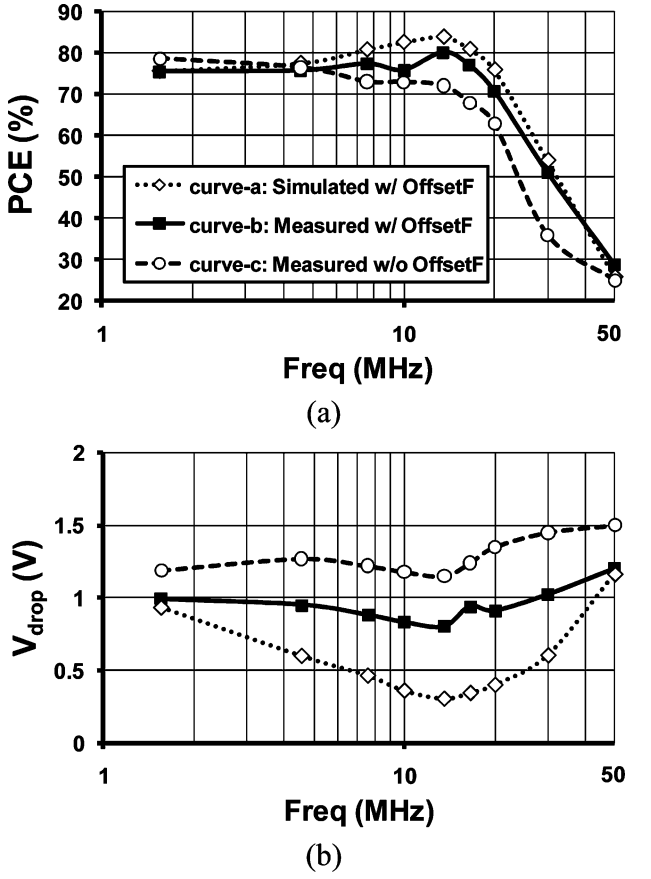


Fig. 16. Measured and simulated (a) PCE and (b) $V_{\rm drop}$ versus f_c with $V_{\rm REC} = 3.12$ V, $C_L = 10\ \mu$F, and $R_L = 500\ \Omega$.

Fig. 15(a) shows the measured and simulated PCE versus R_L with $C_L = 10\ \mu$F, $V_{\rm REC} = 3.12$ V, and $f_c = 13.56$ MHz. As R_L increases, the rectifier output power for the same $V_{\rm REC}$ decreases. Therefore, the rectifier internal power dissipation for switch losses, $P_{\rm Loss,total}$, and comparators, $P_{\rm Comparator}$, become more significant in (4) and reduce the PCE. The measured and simulated $V_{\rm drop}$ versus R_L in Fig. 15(b) shows that $V_{\rm drop}$ decreases by increasing R_L. It is because larger R_L requires smaller $I_{\rm REC}$, leading to smaller voltage drop across the rectifying transistors.

Fig. 16(a) shows the measured and simulated PCE versus f_c with $C_L = 10\ \mu$F, $V_{\rm REC} = 3.12$ V, and $R_L = 500\ \Omega$. The transistor dimensions and comparator offsets of our rectifier were optimized for operating at 13.56 MHz. Therefore, the PCE decreases at higher frequencies due to the comparator delays. At lower frequencies, the PCE also decreases a little bit since the fixed comparator offset turns off the rectifier earlier. Fig. 16(b) shows the measured and simulated $V_{\rm drop}$ versus f_c. Even though $I_{\rm REC}$ is fixed in these experiments, the PCE variation by frequency also affects $V_{\rm drop}$. Therefore, lower PCE at higher frequencies leads to higher $V_{\rm drop}$.

C. Back Telemetry Measurements

To demonstrate the built-in back telemetry capability of our active full-wave rectifier, we applied a random stream of serial data bits at 500 kbps and 0.2 μs pulse width (10% duty cycle) to the rectifier short-coil (SC) input terminal (see Fig. 2). A pair of planar spiral coils with $d = 4$ cm were used similar to the setup described in [26] (see Fig. 1 and Table II). The LSK back telemetry data was recovered using a commercial RFID reader ASIC (TRF7960) from Texas Instruments (Dallas, TX). In Fig. 17, measured waveforms from top show the data signal applied to SC, voltages across the load ($R_L C_L = 500\ \Omega \| 10\ \mu$F), secondary coil ($V_{\rm IN1}$), primary coil ($V_{L1}$), and recovered serial data bit stream at TRF7960 output, which has $\sim 1.2\ \mu$s delay with respect to SC. Shorting L_2 with SC $=$ High in Fig. 1 results in a sudden drop in $V_{\rm IN1}$ and increased current in L_1, which also increases the voltage across L_1 [9]. Current and voltage variations in L_1 are detected by the RFID reader and amplitude shift keying (ASK) demodulated to recover the LSK back telemetry data. It can be seen in Fig. 17 that $V_{\rm REC}$ remains constant during the LSK operation because of the large $C_L(10\ \mu$F) and small SC duty cycle (10%).

D. Overvoltage Protection Measurements

The OVP circuit is activated when $V_{\rm REC}$ increases above a certain threshold voltage, $V_{\rm threshold} = 4.4$ V, which is determined by comparing $0.25V_{\rm REC}$ with a reference voltage, $V_{\rm REF} = 1.1$ V, generated by the regulator. The comparator in Fig. 1 connects $C_{\rm OVP}$ to V_{SS} to deviate the resonance frequency of L_2C_2 from 13.56 MHz and decrease $V_{\rm IN1,2}$ as well as $V_{\rm REC}$. Once $V_{\rm REC}$ is reduced, $C_{\rm OVP}$ is disconnected and the L_2C_2 can return back to 13.56 MHz, unless $V_{\rm REC} > V_{\rm threshold}$ condition is persistent. This closed-loop mechanism regulates

TABLE I
FULL-WAVE RECTIFIER BENCHMARKING

Publication		[28]	2006 [15]	2007 [10]	2008 [16]	2009 [14]	2009 [17]	2009 [18]	**This work**
Technology		Discrete (1N4148)	0.35 µm CMOS	0.5 µm (Schottky)	0.5 µm CMOS	0.18 µm CMOS	0.18 µm CMOS	0.35 µm CMOS	**0.5 µm CMOS**
$V_{IN,\,peak}$ (V)		6	3.5	5	5	0.8	1.25	2.4	**3.8**
V_{REC} (V)		4.3	3.22	4.2	4.36	1.8	0.96	2.08	**3.12**
R_L (kΩ)		1.3	1.8	2.8	1	270	2	0.1	**0.5**
f_c (MHz)		13.56	13.56	4	0.1~2	13.56	10	0.2~1.5	**13.56**
Area (mm^2)		3.08	0.0055	N/A	0.4	0.83	0.86	0.4	**0.18**
PCE (%)	Simulation	N/A	87	N/A	90.4	N/A	N/A	87	**87**
	Measurement	50	N/A	75	84.8	54.9	76	N/A	**80.2**

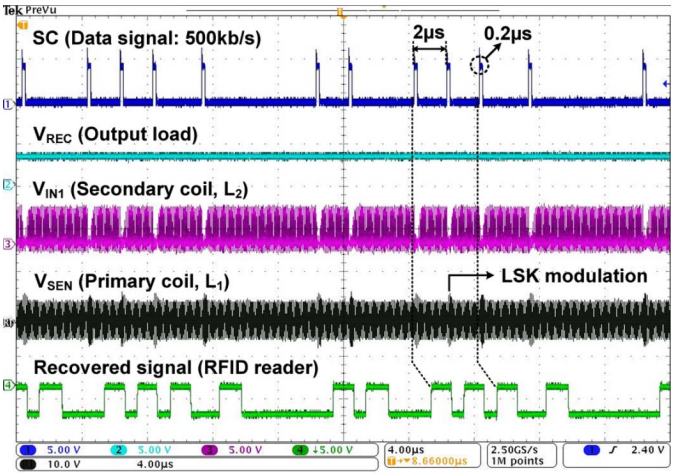


Fig. 17. Measured waveforms showing the active rectifier's built-in LSK back telemetry capability through its short-coil (SC) input terminal (data signal = 500 kbps with 10% duty cycle, $R_L = 500\ \Omega$, and $C_L = 10\ \mu$F). Data was recovered across the primary coil using a commercial RFID reader ASIC (TRF7960, Texas Instruments, Dallas, TX).

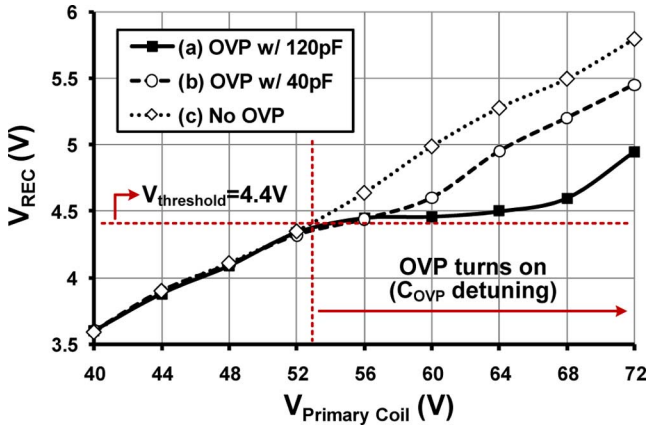


Fig. 18. Measured $V_{\rm REC}$ versus primary coil voltage, V_{L1}, with overvoltage protection (OVP) circuit in Fig. 1 using $C_{\rm OVP} = 120$ pF (curve-a), $C_{\rm OVP} = 40$ pF (curve-b), and without overvoltage protection (curve-c) when $R_L C_L = 500\ \Omega \| 10\ \mu$F.

$V_{\rm REC}$ around $V_{\rm threshold}$ as long as the input voltage is too high without dissipating extra heat within the rectifier. However, the amount of frequency deviation depends on $C_{\rm OVP}$ value. To cope with larger input voltages, larger $C_{\rm OVP}$ is required. Fig. 18 shows the measured $V_{\rm REC}$ versus V_{L1} for two $C_{\rm OVP}$ values. It can be seen that with the frequency deviation resulted from $C_{\rm OVP} = 40$ pF, the rectifier can be protected against V_{L1} up to ~ 60 V, while $C_{\rm OVP} = 120$ pF can protect the rectifier against V_{L1} up to ~ 68 V. In practice, V_{L1} is often constant and a sudden reduction in d or $I_{\rm REC}$ activates the OVP circuit.

TABLE II
ADDITIONAL ACTIVE RECTIFIER AND LDO SPECIFICATIONS

V_{ThN} / V_{ThP}	0.78 V / 0.92 V
Nominal rectifier output power	20 mW
Minimum rectifier input voltage	3.2 V (2.9 V*)
Ripple rejection capacitor (C_L)	10 µF (ESR = 80 mΩ)
Output ripple	80 mV_{pp}
Comparator power consumption	135 µW*
Comparator turn-on delay with $Offset_F$	0.75 ~ 1.5 ns*
Comparator turn-off delay with $Offset_R$	-0.7 ~ 0.5 ns*
Primary coil diameter / inductance (L_1)	16.8 cm / 0.88 µH
Secondary coil diameter / inductance (L_2)	3.0 cm / 0.41 µH
LDO / BGR current consumption	17 µA* / 7 µA*
LDO output / dropout voltage	3 V / 150 mV
Size of rectifying switches ($W_p/L_p = W_n/L_n$)	2100 µm / 0.6 µm
Total area on chip	0.4 mm^2

*From simulation

E. Performance Summary and Comparison

Table I shows the full-wave rectifier benchmarking table, comparing our work with previously reported rectifiers. It can be seen that despite its relatively large feature length process and size, the active rectifier reported here, to the best of our knowledge, provides the highest measured PCE = 80.2% ever reported at 13.56 MHz, thanks to its high speed comparators that are equipped with offset-control functions for both rising and falling edges. With an input peak voltage of 3.8 V, this rectifier can deliver more than 20 mW at $V_{\rm REC} = 3.12$ V, which is required for high power IMDs such as the implantable multichannel wireless neural recording and stimulating system that is being developed in our lab [26]. By shortening the connection between L_2 and the rectifier input port when they are both embedded in an IMD and thus reducing the parasitic components shown in Fig. 12, we expect the rectifier PCE to move closer to the simulated level of 87%. Further, migrating to a smaller feature length process is expected to further improve the PCE and bandwidth by lowering the threshold voltages and comparator delays. Table II summarizes some additional specifications of the rectifier and LDO that are not listed in Table I.

V. Conclusions

An integrated power-efficient full-wave active rectifier equipped with offset-controlled high speed comparators has been presented for inductively powered applications, such as RFID and IMD. The main switches in this rectifier are driven by a pair of comparators, which keep them closed precisely when $V_{\mathrm{IN1,2}} > V_{\mathrm{REC}}$, while compensating for both turn-on and turn-off propagation delays of the comparators by a pair of programmable offsets. As a result, the rectifier conducts for the maximum possible period of time and delivers maximum forward current to the load, while minimizing the back current.

In addition, the sizes of the rectifying transistors were optimized for minimizing their R_{on} and switching losses at the rectifier operating frequency. We have reported the highest measured PCE of 80.2% with 3.12 V dc output across a 500 Ω load from a 3.8 V ac input at 13.56 MHz. The rectifier's built-in LSK back telemetry capability can be utilized for communication, such as establishing a closed loop wireless power transmission system to adjust the transmitted power for a constant rectifier output voltage [27]. The rectifier has also been equipped with a detuning-based overvoltage protection circuit, which is a necessary safety feature for situations in which the rectifier input signal has grown too large as a result of the coils being too close or the load current being too small.

Appendix

In this section we derive (2) and (4) for PCE analysis using simplified rectifier waveforms, shown in Fig. 19. D is the rectifier switching duty cycle, D_{charge} is the charging duty cycle, $T = 1/2\ f_c$ is the period of the full-wave rectified signal, and T_{PHL} and T_{PLH} are the delays in high-to-low and low-to-high transitions of the comparator output (V_{OUT}), respectively. In this model, we assume: 1) V_{IN} is sinusoidal, 2) R_L is constant, 3) C_L is large enough to maintain V_{REC} almost constant despite the rectifier operation, and 4) the rising and falling times of the comparator output are negligible compared to T (or they have been included in T_{PHL} and T_{PLH}). The rectifier turns on (i.e., conducts) from T_a to $T_d = DT$ and turns off from T_d to $T_e = T - DT$. The assumption is that the additional charge that is stored in C_L during DT maintains V_{REC} constant while the rectifier is supplying R_L for the entire period of T. Therefore,

$$\int_{T_a}^{T_d} I_{\mathrm{in}}(t)dt = \int_{T_a}^{T_d} \left(\frac{V_{\mathrm{IN}}(t) - V_{\mathrm{REC}}}{R_{onp} + R_{onn}}\right) dt = \int_{T_a}^{T_e} \left(\frac{V_{\mathrm{REC}}}{R_L}\right) dt = \frac{V_{\mathrm{REC}}}{R_L} T \tag{5}$$

where $T_a = (T - DT + T_{PHL} + T_{PLH})/2$, $T_d = (T + DT + T_{PHL} + T_{PLH})/2$, and $T_e = (3T - DT + T_{PHL} + T_{PLH})/2$ are indicated on Fig. 19. The sinusoidal input voltage, V_{IN}, can be expressed as

$$V_{\mathrm{IN}}(t) = V_{\mathrm{IN,peak}} \sin\left(\frac{\pi}{T}t\right) = \frac{V_{\mathrm{REC}}}{\sin\left((T_a - T_{PHL})\frac{\pi}{T}\right)} \sin\left(\frac{\pi}{T}t\right). \tag{6}$$

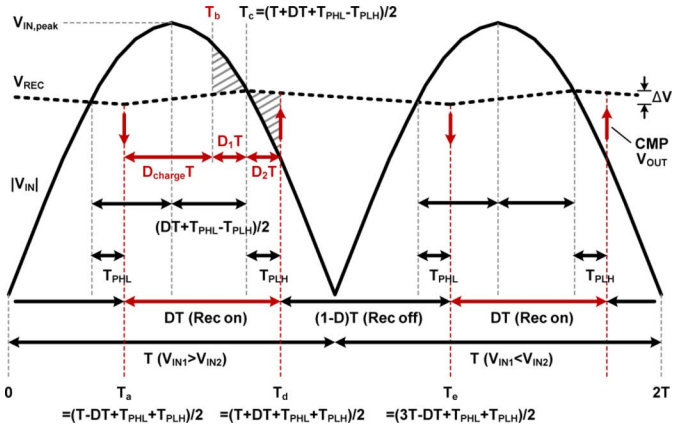


Fig. 19. Simplified voltage waveforms of the active rectifier used in the PCE theoretical analysis. To simplify the equations, we have assumed $\Delta V \to 0$ V.

Using (6) in (5), $R_{onp} + R_{onn}$ can be expressed as a function of D

$$R_{onp} + R_{onn} = R_L \left(\frac{\frac{1}{\pi}\left(\cos\left(T_a\frac{\pi}{T}\right) - \cos\left(T_d\frac{\pi}{T}\right)\right)}{\sin\left((T_a - T_{PHL})\frac{\pi}{T}\right)} - D\right). \tag{7}$$

If $T_{PLH} = 0$, D_{charge} would be the same as D because the rectifier only supplies $R_L C_L$ during its conducting period. However, with $T_{PLH} > 0$, the back current can discharge C_L when $V_{\mathrm{REC}} > |V_{\mathrm{IN}}|$. In Fig. 19, the back current from T_c to $T_d(D_2T)$ discharges C_L as much as the forward current from T_b to $T_c(D_1T)$ charges C_L. Therefore, D_{charge} can be derived as a function of D by obtaining T_b

$$\begin{cases} I_{\mathrm{in}} = I_{C_L,\mathrm{charge}} + I_{R_L} & T_b < t < T_c \\ I_{\mathrm{in}} = I_{C_L,\mathrm{discharge}} + I_{R_L} & T_c < t < T_d \end{cases} \tag{8}$$

$$\int_{T_b}^{T_c} I_{C_L,\mathrm{charge}}(t)dt + \int_{T_c}^{T_d} I_{C_L,\mathrm{discharge}}(t)dt = \int_{T_b}^{T_d} \left(\frac{V_{\mathrm{IN}}(t) - V_{\mathrm{REC}}}{R_{onp} + R_{onn}} - \frac{V_{\mathrm{REC}}}{R_L}\right) dt = 0. \tag{9}$$

By solving (5)–(9) for T_b using MATLAB, D_{charge} can be expressed as

$$D_{\mathrm{charge}} = D - \left(\frac{T_d - T_b}{T}\right). \tag{10}$$

Note that even though the input current from T_b to T_d does not affect V_{REC}, R_{on} power losses still occur during this period $(D_1T + D_2T)$. Therefore, the R_{on} loss term with D_{eff} in (2) can be represented as

$$P_{\mathrm{Loss},R_{onp}} + P_{\mathrm{Loss},R_{onn}} = \left(\frac{V_{\mathrm{REC}}}{R_L D_{\mathrm{eff}}}\right)^2 D_{\mathrm{eff}}\left(R_{onp} + R_{onn}\right)$$

$$= \left(\left(\frac{V_{\mathrm{REC}}}{R_L D_{\mathrm{charge}}} \right)^2 D_{\mathrm{charge}} + \left(\frac{1}{D_1 T} \int_{T_b}^{T_c} I_{\mathrm{in}}(t)dt \right)^2 D_1 + \left(\frac{1}{D_2 T} \int_{T_c}^{T_d} I_{\mathrm{in}}(t)dt \right)^2 D_2 \right) (R_{onp} + R_{onn}) \quad (11)$$

where the first, second, and third terms of the right-hand side equation correspond to the R_{on} loss during $D_{\mathrm{charge}}T$, D_1T, and D_2T, respectively. If $T_{PLH} = 0$, the second and third terms will be eliminated because $T_b = T_c = T_d$. Therefore, using (5)–(11), the R_{on} loss in (2) can be expressed as a function of D.

$R_{onp} + R_{onn}$ can also be represented as a function of $W_p = W_n$

$$R_{onp} + R_{onn} = \frac{1}{W_p} \left(\frac{L_{\min}}{k_p(V_{\mathrm{REC}} - |V_{ThP}|)} + \frac{L_{\min}}{k_n(V_{\mathrm{REC}} - V_{ThN})} \right) \quad (12)$$

where $L_{\min}$ is the length of the PMOS and NMOS transistors. By substituting W_p with (12), the switching loss term, $P_{\mathrm{Loss},Cgp}$, in (2) can be expressed as a function of D

$$P_{\mathrm{Loss},C_{gp}} = W_p C_{gp}^* V_{\mathrm{REC}}^2 2f_c = C_{gp}^* V_{\mathrm{REC}}^2 2f_c \times \frac{1}{R_{onp} + R_{onn}} \times \left(\frac{L_{\min}}{k_p(V_{\mathrm{REC}} - |V_{ThP}|)} + \frac{L_{\min}}{k_n(V_{\mathrm{REC}} - V_{ThN})} \right). \quad (13)$$

Therefore, by substituting (11) and (13) in (2) and differentiating it with respect to D, we can obtain the optimized D for minimum power loss inside the rectifier. Using the optimal D, the optimal W_p can be derived from (7) and (12), and the maximum PCE can be calculated from (4) by minimizing the power loss in (2).

ACKNOWLEDGMENT

The authors would like to thank M. Kiani for helping with the back telemetry setup, U. Jow for the coil designs, as well as other members of the GT-Bionics Lab for their constructive comments.

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