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Reviser : M. C. Lee (PDS)  Revising Line Manager : Y. C. Harn  Approvals:  Please refer EDW workflow to see detail approval records				<p>Title</p> <p style="text-align: center;"><b>TSMC 90NM/85NM CMOS LOGIC/MS/RF AND 80NM CMOS LOGIC/MS DESIGN RULE (CLN90G/GT/LP, CMN90G/GT/LP, CLN85G/LP, CMN85G/LP, CLN80GC/GT/HS/LP, CMN80GC)</b></p> <p>Document No. : T-N90-LO-DR-001</p> <table> <tr> <td>Contents</td> <td>:</td> <td>698</td> </tr> <tr> <td>Attach.</td> <td>:</td> <td>0</td> </tr> <tr> <td>Total</td> <td>:</td> <td>698</td> </tr> </table>	Contents	:	698	Attach.	:	0	Total	:	698
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(B)	06-30-03	120326087	W. T. Weng	Modify document title from "TSMC 90NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOW K 1.0V/1.8V, 1.0V/2.5V, 1.0V/3.3V, 1.0V/1.8V/3.3V DESIGN RULE " to "TSMC 90NM CMOS LOGIC DESIGN RULE"
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1.2	04-06-04	E120200413273	S. S. Peng	Delete high speed (HS) technology and added high performance (GT) technology. Please see Appendix A for other revisions from Ver 1.1 to 1.2.
				<p>Title</p> <p style="text-align: center;"><b>TSMC 90NM/85NM CMOS LOGIC/MS/RF AND 80NM CMOS LOGIC/MS DESIGN RULE (CLN90G/GT/LP, CMN90G/GT/LP, CLN85G/LP, CMN85G/LP, CLN80GC/GT/HS/LP, CMN80GC)</b></p> <p>Document No. : T-N90-LO-DR-001</p>

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# 1 Introduction

This chapter has been divided into the following topics:

- 1.1 Overview
- 1.2 Reference documentation

## 1.1 Overview

This document provides all the rules and reference information for the design and layout of integration circuits using the TSMC 90 nm/ 85nm/ 80nm CMOS/MM\_RF LOGIC 1P9M (single poly, 9 metal layers), salicide, Cu technology.

- **CLN90 offers G/GT/LP process.**
  - **CLN90G:** provide a general-purpose product for applications with a 1.0V core design, and with 1.8V, 2.5V, or 3.3V capable I/O's.
  - **CLN90LP:** provide a low-power product for applications with a 1.2V core design, and with 2.5V or 3.3V capable I/O's, and with ultra low V<sub>t</sub> (ULV<sub>t</sub>) device.
  - **CLN90GT:** provide a front-end high-performance product for applications with a 1.2V core design, and with 1.8V or 2.5V capable I/O's.
- **CLN85 offers G/LP process** – 94% shrinkage from CLN90 layout dimensions.
  - **CLN85G:** provides CLN90G general purpose products with 94% linear shrinkage for the die area saving purpose. CLN85G offers dual-gate oxide process for 1.0V core and, 1.8V, 2.5V, or 3.3V I/O devices, and triple-gate oxide process for 1.0V core, 1.8V and 3.3V I/O device.
  - **CLN85LP:** provides CLN90LP low power products with 94% linear shrinkage for the die area saving purpose. CLN85LP offers dual-gate oxide process for 1.2V core and, 2.5V or 3.3V I/O devices, and with ultra low V<sub>t</sub> (ULV<sub>t</sub>) device.
- **CLN80 offers GC/GT/HS/LP process** – 90% shrinkage from CLN90 layout dimensions.
  - **CLN80GC:** provides CLN90G products with 90% shrinkage for die area saving purpose. CLN80GC offers dual-gate oxide process for 1.0V core and, 2.5V or 3.3V I/O devices.
  - **CLN80GT:** provides CLN90GT products with 90% shrinkage for die area saving purpose. CLN80GT offers dual-gate oxide process for 1.2V core and, 1.8V or 2.5V I/O devices.
  - **CLN80HS:** provides CLN90GT product with 90% shrinkage for high-speed performance requirement by aggressive device design. CLN80HS offers dual gate oxide processes for 1.05V core and, 1.8V or 2.5V I/O devices.
  - **CLN80LP:** provides CLN90LP products with 90% shrinkage for die area saving purpose. CLN80LP offers dual-gate oxide process for 1.2V core and 2.5V I/O devices.
- **CMN90 offers G/GT/LP with extra process steps for mixed-signal (MS) process and G/LP for RF process. It includes metal-insulator-metal (MIM) capacitor and ultra thick metal (UTM; 34KA) for inductor.**
  - **CMN90G for MS:** provide a general-purpose product for applications with a 1.0V core design, and with 1.8V, 2.5V, or 3.3V capable I/O's.
  - **CMN90LP for MS:** provide a low-power product for applications with a 1.2V core design, and with 2.5V or 3.3V capable I/O's, and with ultra low V<sub>t</sub> (ULV<sub>t</sub>) device. No mis-matching model and RF model are supported for ultra low V<sub>t</sub> device.
  - **CMN90GT for MS:** provide a front-end high-performance product for applications with a 1.2V core design, and with 1.8V or 2.5V capable I/O's.
  - **CMN90G for RF:** provide a general-purpose product for performance applications with a 1.0V core design, and with 2.5V, or 3.3V capable I/O's.
  - **CMN90LP for RF:** provide a low-power product for applications with a 1.2V core design, and with 2.5V or 3.3V capable I/O's, and with ultra low V<sub>t</sub> (ULV<sub>t</sub>) device. No mis-matching model and RF model are supported for ultra low V<sub>t</sub> device.

- CMN85 offers G/LP with extra process steps for mixed-signal (MS) process. It includes metal-insulator-metal (MIM) capacitor and ultra thick metal (UTM; 34KA) for inductor in G/LP. Only mixed-signal (base band) SPICE model is supported, and no RF SPICE model is supported. – 94% shrinkage from CMN90 layout dimensions.
  - CMN85G for MS: provide CMN90G general purpose products with 94% linear shrinkage for the die area saving purpose. CMN85G offers dual-gate oxide process for 1.0V core and, 2.5V, or 3.3V I/O devices.
  - CMN85LP for MS: provide CMN90LP low power products with 94% linear shrinkage for the die area saving purpose. CMN85LP offers dual-gate oxide process for 1.2V core and, 2.5V, or 3.3V I/O devices, and with ultra low V<sub>t</sub> (ULVt) device. No mis-matching model and RF model are supported for ultra low V<sub>t</sub> device.
  - CMN85G for RF: provide CMN90G general purpose products with 94% linear shrinkage for the die area saving purpose. CMN85G offers dual-gate oxide process for 1.0V core and, 2.5V, or 3.3V I/O devices.
  - CMN85LP for RF: provide CMN90LP low power products with 94% linear shrinkage for the die area saving purpose. CMN85LP offers dual-gate oxide process for 1.2V core and, 2.5V, or 3.3V I/O devices, and with ultra low V<sub>t</sub> (ULVt) device. No mis-matching model and RF model are supported for ultra low V<sub>t</sub> device.
- CMN80 offers GC with extra process steps for mixed-signal (MS) process. It includes metal-insulator-metal (MIM) capacitor – 90% shrinkage from CMN90 layout dimensions.
  - CMN80GC for MS: Provides CMN90G products with 90% shrinkage for die area saving purpose. CMN80GC offers dual-gate oxide process for 1.0V core and, 2.5V or 3.3V I/O devices.

## 1.2 Reference Documentation

Table 1.2.1 Reference Documents

Content	Reference Documentation
Reference flow	<ul style="list-style-type: none"> <li>Please download it from TSMC-Online</li> </ul>
Lead free flip chip rule	<ul style="list-style-type: none"> <li>TBD</li> </ul>
1T MIM rules	<ul style="list-style-type: none"> <li><b>T-N90-CE-DR-002:</b> <i>TSMC 90 NM CMOS EMBEDDED MEMORY 1T-MIM LOGIC BASED HIGH PERFORMANCE 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V 1.2&amp;3.3V DESIGN RULE</i></li> <li><b>T-N90-CE-DR-003:</b> <i>TSMC 90 NM CMOS EMBEDDED MEMORY 1T-MIM LOGIC BASED LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;1.8/1.2&amp;2.5/1.2&amp;3.3V DESIGN RULE</i></li> </ul>
Metal fuse rule	<ul style="list-style-type: none"> <li><b>T-N90-LO-DR-003:</b> <i>TSMC 90NM LOGIC TOP METAL FUSE DESIGN RULE</i></li> <li><b>T-000-CL-DR-005:</b> <i>TSMC AI FUSE DESIGN RULE (0.13UM/90NM/65NM)</i></li> </ul>
Wire bond and flip chip related rules	<ul style="list-style-type: none"> <li><b>T-000-CL-DR-002:</b> <i>TSMC WIRE BOND, FLIP CHIP, AND INTERCONNECTION DESIGN RULE</i></li> </ul>
X-metal rule	<ul style="list-style-type: none"> <li><b>T-N90-CL-DR-013:</b> <i>TSMC 90NM CMOS LOGIC X-METAL (XMX) DESIGN RULE</i></li> </ul>
WLCSP rule	<ul style="list-style-type: none"> <li><b>T-000-BP-DR-005</b> <i>TSMC BUMPING POST PASSIVATION INTERCONNECT DESIGN RULE</i></li> <li><b>Q-RAS-02-02-083</b> <i>BUMP EM IMAX RULE (FOR TSMC'S BUMP LINE PROCESS ONLY)</i></li> </ul>
WLCSP DRC deck	<ul style="list-style-type: none"> <li><b>T-000-BP-DR-005-X1</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC BUMPING POST PASSIVATION INTERCONNECT DRC (CALIBRE) COMMAND FILE</i></li> </ul>
N80 ULVt rule	<ul style="list-style-type: none"> <li><b>T-N80-CL-DR-008</b> <i>TSMC 80NM CMOS LOGIC ULTRA LOW VT DESING RULE (CLN80GC)</i></li> </ul>
N80 ULVt DRC deck	<ul style="list-style-type: none"> <li><b>T-N80-CL-DR-008-X1</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC 80 NM CMOS LOGIC ULTRA LOW VT DRC (CALIBRE) COMMAND FILE</i></li> </ul>
GDS layer usage	<ul style="list-style-type: none"> <li><b>T-N90-LO-LE-001:</b> <i>TSMC 90 NM GDS LAYERUSAGE DESCRIPTION FILE</i></li> </ul>
DRC deck	<ul style="list-style-type: none"> <li><b>T-N90-LO-DR-001-X1:</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC 90NM/ 85NM/ 80NM CMOS LOGIC/ MS_RF DRC COMMAND FILE</i></li> </ul>
Dummy pattern generation utility	<ul style="list-style-type: none"> <li><b>T-N90-LO-DR-001-X2:</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC 90NM DUMMY OD/PO GENERATION UTILITY</i></li> <li><b>T-N90-LO-DR-001-X3:</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC 90NM DUMMY METAL) GENERATION UTILITY</i></li> <li><b>T-N80-CL-DR-001-X2:</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC 80NM DUMMY OD/PO GENERATION UTILITY</i></li> </ul>
DFM utility	<ul style="list-style-type: none"> <li><b>T-N90-LO-DR-001-X4:</b> (<i>X</i> is the code of EDA tool, please refer to TSMC-Online for the details) <i>TSMC 90NM DFM LAYOUT ENHANCEMENT UTILITY</i></li> </ul>
SPICE	<ul style="list-style-type: none"> <li><b>T-N90-LO-SP-001:</b> <i>TSMC 90NM LOGIC GENERAL PURPOSE 1P9M SALICIDE 1.0V/1.8V Cu_LOW K HD BEOL SPICE MODELS (CLN90G)</i></li> <li><b>T-N90-LO-SP-002:</b> <i>TSMC 90NM LOGIC GENERAL PURPOSE 1P9M SALICIDE 1.0V/2.5V Cu_LOW K HD BEOL SPICE MODELS (CLN90G)</i></li> <li><b>T-N90-LO-SP-003:</b> <i>TSMC 90NM LOGIC GENERAL PURPOSE 1P9M SALICIDE 1.0V/3.3V Cu_LOW K HD BEOL SPICE MODELS (CLN90G)</i></li> </ul>

Content	Reference Documentation
	<ul style="list-style-type: none"> <li>• <i>T-N90-CL-SP-005:</i> TSMC 90NM LOGIC GENERAL PURPOSE 1P9M SALICIDE 1.0V/1.8V/3.3V Cu_LOW K HD BEOL SPICE MODELS (CLN90G)</li> <li>• <i>T-N90-LO-SP-008:</i> TSMC 90NM LOGIC LOW POWER 1P9M SALICIDE 1.2V/2.5V Cu_LOW K HD BEOL SPICE MODELS (CLN90LP)</li> <li>• <i>T-N90-LO-SP-009:</i> TSMC 90NM LOGIC LOW POWER 1P9M SALICIDE 1.2V/3.3V Cu_LOW K HD BEOL SPICE MODELS (CLN90LP)</li> <li>• <i>T-N90-CL-SP-010:</i> TSMC 90NM LOGIC LOW POWER 1P9M SALICIDE 1.2V Cu_LOW K HD BEOL SPICE MODELS (CLN90LP Low VT)</li> <li>• <i>T-N90-CL-SP-013:</i> TSMC 90NM CMOS LOGIC HIGH PERFORMANCE 1P9M SALICIDE Cu_LOW K 1.2V/2.5V HD BEOL SPICE MODELS (CLN90GT)</li> <li>• <i>T-N90-CL-SP-028:</i> TSMC 90NM LOGIC HIGH PERFORMANCE 1P9M SALICIDE 1.2&amp;1.8V CU_LOW K HD BEOL SPICE MODELS (CLN90GT)</li> <li>• <i>T-N90-CL-SP-035:</i> TSMC 90NM LOGIC 1P9M Low-K 2XTM + Al RDL BEOL SPICE MODELS</li> <li>• <i>T-N85-CL-SP-001:</i> TSMC 85 NM LOGIC LOW POWER 1P9M+Al_RDL SALICIDE 1.2V/3.3V CU_LOW K HD BEOL SPICE MODELS 85LP</li> <li>• <i>T-N85-CL-SP-002:</i> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M+Al_RDL SALICIDE CU_LOWK 1.0&amp;3.3V HD BEOL SPICE MODEL(CLN85G)</li> <li>• <i>T-N85-CL-SP-003:</i> TSMC 85 NM CMOS LOGIC LOW POWER 1P9M+Al_RDL SALICIDE CU_LOWK 1.2&amp;2.5V HD BEOL SPICE MODEL 85LP</li> <li>• <i>T-N85-CL-SP-004:</i> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M+Al_RDL SALICIDE CU_LOWK 1.0&amp;1.8V HD BEOL SPICE MODELS 85G</li> <li>• <i>T-N85-CL-SP-006:</i> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M+Al_RDL SALICIDE 1.0&amp;2.5V CU_LOWK HD BEOL SPICE MODEL 85G</li> <li>• <i>T-N85-CL-SP-007:</i> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M+Al_RDL SALICIDE CU_LOWK 1.0&amp;1.8&amp;3.3V HD BEOL SPICE MODEL 85G</li> <li>• <i>T-N85-CM-SP-001:</i> TSMC 85 NM CMOS MIXED SIGNAL MS LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V SPICE MODEL</li> <li>• <i>T-N85-CM-SP-002:</i> TSMC 85 NM CMOS MIXED SIGNAL MS LOW POWER 1P9M SALICIDE CU_LOWER K 1.2&amp;3.3V SPICE MODEL</li> <li>• <i>T-N85-CM-SP-003:</i> TSMC 85 NM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P9M SALICIDE CU_LOWER K 1.0&amp;2.5V SPICE MODEL</li> <li>• <i>T-N85-CM-SP-004:</i> TSMC 85 NM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P9M SALICIDE CU_LOWER K 1.0&amp;3.3V SPICE MODEL</li> <li>• <i>T-N80-CL-SP-001:</i> TSMC 80NM LOGIC HIGH PERFORMANCE 1P9M SALICIDE 1.2V/2.5V Cu_LOW K HD BEOL SPICE MODELS (CLN80GT)</li> <li>• <i>T-N80-CL-SP-002:</i> TSMC 80NM LOGIC HIGH SPEED 1P9M SALICIDE 1.05V/1.8V CU_LOW K HD BEOL SPICE MODELS (CLN80HS)</li> <li>• <i>T-N80-CL-SP-003:</i> TSMC 80 NM LOGIC HIGH PERFORMANCE 1P9M SALICIDE 1.2&amp;1.8V CU_LOW K HD BEOL SPICE MODELS (CLN80GT)</li> <li>• <i>T-N80-CL-SP-004:</i> TSMC 80NM LOGIC HIGH SPEED 1P9M SALICIDE 1.05V/2.5V CU_LOW K HD BEOL SPICE MODELS (CLN80HS)</li> <li>• <i>T-N80-CL-SP-005:</i> TSMC 80NM LOGIC LOW POWER 1P9M+Al_RDL SALICIDE 1.2V/2.5V Cu_LOW K HD BEOL SPICE MODELS (CLN80LP)</li> <li>• <i>T-N80-CL-SP-014:</i></li> </ul>

Content	Reference Documentation
	<p>TSMC 80NM LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M+AL_RDL SALICIDE 1.0V/2.5V CU_LOW K HD BEOL SPICE MODELS (CLN80GC)</p> <ul style="list-style-type: none"> <li>• T-N80-CL-SP-015: TSMC 80NM LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M+AL_RDL SALICIDE 1.0V/3.3V CU_LOW K HD BEOL SPICE MODELS (CLN80GC)</li> <li>• T-N90-CM-SP-001: TSMC 90NM CMOS MIXED SIGNAL MS LOW POWER 1P9M SALICIDE 1.2V/2.5V Cu_LOW K HD BEOL SPICE MODELS (CMN90LP)</li> <li>• T-N90-CM-SP-003: TSMC 90NM CMOS MIXED SIGNAL MS LOW POWER 1P9M SALICIDE 1.2V/3.3V Cu_LOW K HD BEOL SPICE MODELS (CMN90LP)</li> <li>• T-N90-CM-SP-004: TSMC 90 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V SPICE MODEL</li> <li>• T-N90-CM-SP-005: TSMC 90NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;3.3V SPICE MODEL</li> <li>• T-N90-CM-SP-007: TSMC 90NM CMOS MIXED SIGNAL MS HIGH PERFORMANCE 1P9M+AL_RDL SALICIDE 1.2V/2.5V Cu_LOW K HD BEOL SPICE MODELS (CMN90GT)</li> <li>• T-N90-CM-SP-011: TSMC 90NM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P9M+AL_RDL SALICIDE 1.0V/1.8V/3.3V CU_LOW K HD BEOL SPICE MODELS (CMN90G)</li> <li>• T-N90-CM-SP-012: TSMC 90NM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P9M+AL_RDL SALICIDE 1.0V/2.5V CU_LOW K HD BEOL SPICE MODELS (CMN90G)</li> <li>• T-N90-CM-SP-013: TSMC 90 NM CMOS MIXED SIGNAL RF GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V SPICE MODEL</li> <li>• T-N90-CM-SP-016: TSMC 90 NM CMOS MIXED SIGNAL RF GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V SPICE MODEL</li> <li>• T-N90-CM-SP-021: TSMC 90NM CMOS MIXED SIGNAL MS HIGH PERFORMANCE 1P9M+AL_RDL SALICIDE 1.2V/1.8V Cu_LOW K HD BEOL SPICE MODELS (CMN90GT)</li> <li>• T-N80-CM-SP-001: TSMC 80 NM MIXED SIGNAL MS GENERAL PURPOSE CONSUMER PLATFORM 1P9M+AL_RDL SALICIDE 1.0V/2.5V CU_LOW K HD BEOL SPICE MODELS (CMN80GC)</li> <li>• T-N80-CM-SP-002: TSMC 80 NM MIXED SIGNAL MS GENERAL PURPOSE CONSUMER PLATFORM 1P9M+AL_RDL SALICIDE 1.0V/3.3V CU_LOW K HD BEOL SPICE MODELS (CMN80GC)</li> </ul>
Device formation examples and LVS properties	<ul style="list-style-type: none"> <li>• T-N90-CL-LS-001 TSMC 90 NM CMOS LOGIC GENERAL PURPOSE DEVICE FORMATION EXAMPLES AND LVS PROPERTIES</li> <li>• T-N85-CL-LS-001: TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE 1.0&amp;3.3V DEVICE FORMATION EXAMPLES AND LVS PROPERTIES</li> <li>• T-N80-CL-LS-001 TSMC 80 NM CMOS LOGIC GENERAL PURPOSE ENHANCED 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V DEVICE FORMATION EXAMPLES AND LVS PROPERTIES</li> </ul>
LVS	<ul style="list-style-type: none"> <li>• T-N90-CL-LS-001-X1: (X is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 90NM CMOS LOGIC LVS COMMAND FILE</li> <li>• T-N85-CL-LS-001-X1: (X is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 85 NM CMOS LOGIC LVS COMMAND FILE</li> <li>• T-N80-CL-LS-001-X1: (X is the code of EDA tool, please refer to TSMC-Online for the details) TSMC 80 NM CMOS LOGIC GENERAL PURPOSE ENHANCED 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V DEVICE FORMATION EXAMPLES AND LVS COMMAND FILE</li> </ul>
PDK	<ul style="list-style-type: none"> <li>• T-N90-LO-SP-002-K1: TSMC 90NM CMOS LOGIC GENERAL PURPOSE PDK (CLN90G, CLN90GT, CLN90LP, CMN90LP)</li> <li>• T-N85-CL-SP-001-K1:</li> </ul>

Content	Reference Documentation
	<p>TSMC 85 NM LOGIC LOW POWER 1P9M+AL_RDL SALICIDE 1.2V/3.3V CU_LOWK HD BEOL PDK (CLN85LP) (INCLUDES: CLN85LP 1.2V/2.5V; CLN85LP 1.2V/3.3V)</p> <ul style="list-style-type: none"> <li>• T-N85-CL-SP-006-K1: TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M+AL_RDL SALICIDE 1.0&amp;2.5V CU_LOWK HD BEOL PDK (CLN85G) (INCLUDES: CLN85G 1.0&amp;3.3V; CLN85G 1.0&amp;1.8&amp;3.3V; CLN85G 1.0&amp;1.8V; CLN85G 1.0&amp;2.5V)</li> <li>• T-N80-CL-SP-014-K1: TSMC 80NM LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M AL_RDL SALICIDE 1.0V/2.5V CU_LOWK HD BEOL PDK</li> <li>• T-N85-CM-SP-002-K1 TSMC 85 NM CMOS MIXED SIGNAL MS LOW POWER 1P9M SALICIDE CU_LOWERK 1.2&amp;3.3V PDK(CMN85LP) (INCLUDES:CMN85LP 1.2V/2.5V: CMN85LP 1.2V/3.3V)</li> <li>• T-N85-CM-SP-003-K1 TSMC 85 NM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P9M SALICIDE CU_LOWERK 1.0&amp;2.5V PDK(CMN85G) (INCLUDES:CMN85G 1.0V/2.5V: CMN85G 1.0V/3.3V)</li> <li>• T-N90-CM-SP-004-K1: TSMC 90 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V PDK</li> <li>• T-N90-CM-SP-005-K1: TSMC 90 NM CMOS MIXED SIGNAL RF LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;3.3V PDK</li> <li>• T-N90-CM-SP-013-K1: TSMC 90 NM CMOS MIXED SIGNAL RF GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V PDK</li> </ul>
SRAM	<ul style="list-style-type: none"> <li>• T-000-CL-RP-002: TSMC Embedded SRAM Redundancy Implementation rule</li> <li>• T-N90-LO-CL-001: TSMC 90NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0V/1.8V 1.0V/2.5V 1.0V/3.3V EMBEDDED 6T SRAM CELL LAYOUT</li> <li>• T-N90-CL-CL-002: TSMC 90 NM CMOS LOGIC LOW POWER 1P9M SALICIDE 1.2/1.2&amp;1.8/1.2&amp;2.5/1.2&amp;2.5&amp;3.3/1.2&amp;3.3V 6T SRAM CELL LAYOUT &amp; MODEL</li> <li>• T-N90-CL-CL-003: TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SILICIDE CU_LOWK 1.0&amp;1.8&amp;2.5/ 1.0&amp;1.8&amp;3.3/ 1.0&amp;2.5/ 1.0&amp;3.3/1.0/3.3/1.0V 6T SRAM CELL LAYOUT &amp; MODEL-ULTRA-HIGH-DENSITY</li> <li>• T-N90-CL-CL-005: TSMC 90 NM CMOS LOGIC HIGH PERFORMANCE 1P9M SALICIDE CU_LOWK 1.2/ 1.2&amp;1.8/ 1.2&amp;2.5/ 1.2&amp;2.5&amp;3.3/ 1.2&amp;3.3V 6T SRAM CELL LAYOUT &amp; MODEL</li> <li>• T-N80-CL-CL-001: TSMC 80 NM CMOS LOGIC HIGH PERFORMANCE 1P9M SALICIDE CU_LOWK 1.2 6T/8T SRAM CELL LAYOUT &amp; MODEL</li> <li>• T-N80-CL-CL-002: TSMC 80 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2V 6T SRAM CELL LAYOUT &amp; MODEL</li> <li>• T-N80-CL-CL-003: TSMC 80 NM CMOS LOGIC HIGH SPEED 1P9M SALICIDE CU_LOWK 1.05/1.8/1.05/2.5V 6T SRAM CELL LAYOUT &amp; MODEL</li> <li>• T-N80-CL-CL-007: TSMC 80 NM CMOS LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M SALICIDE CU_LOWK 1.0V 6T/8T SRAM CELL LAYOUT &amp; MODE</li> </ul>
Latch up	<ul style="list-style-type: none"> <li>• T-N90-CL-CR-002: TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V LATCH-UP CHARACTERIZATION REPORT</li> </ul>
Qualification report	<ul style="list-style-type: none"> <li>• T-N90-CL-QR-002: TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P6M SALICIDE CU_LOWK 1.0&amp;2.5V QUALIFICATION REPORT-FAB12</li> <li>• T-N90-CL-QR-019: TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P7M SALICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT-FAB12</li> <li>• T-N90-CL-QR-012: TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8&amp;3.3V QUALIFICATION REPORT-FAB12</li> <li>• T-N90-CL-QR-011:</li> </ul>

Content	Reference Documentation
	<p><i>TSMC 90NM CMOS LOGIC HIGH PERFORMANCE (GT) 1P6M SALICIDE CU_LOW K 1.2/2.5V RELIABILITY QUALIFICATION REPORT -FAB12</i></p> <ul style="list-style-type: none"> <li>• <i>T-N90-CL-QR-008:</i> <i>TSMC 90 NM CMOS LOGIC LOW POWER 1P6M SALICIDE CU_LOW K 1.2V&amp;2.5V PROCESS QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N90-CL-QR-009:</i> <i>TSMC 90 NM CMOS LOGIC LOW POWER 1P6M SALICIDE CU_LOWK 1.2&amp;3.3V PROCESS QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N90-CL-QR-022:</i> <i>TSMC 90 NM CMOS LOGIC SALICIDE CU_LOWK 2XTM PROCESS QUALIFICATION REPORT--Fab12</i></li> <li>• <i>T-N90-CL-QR-023:</i> <i>TSMC 90 NM CMOS LOGIC HIGH PERFORMANCE 1P9M SALICIDE CU_FSG/CU_LOWK 1.2&amp;2.5V ELECTRICAL FUSE IP QUALIFICATION REPORT</i></li> <li>• <i>T-N90-CL-QR-022:</i> <i>TSMC 90 NM CMOS LOGIC SALICIDE CU_LOWK 2XTM PROCESS QUALIFICATION REPORT--Fab12</i></li> <li>• <i>T-N90-CL-QR-025:</i> <i>TSMC 90NM WIRE BOND (NON CUP) PACKAGE WITH EUTECTIC BGA QUALIFICATION REPORT</i></li> <li>• <i>T-N90-CL-QR-026:</i> <i>TSMC 90NM WIRE BOND CUP PACKAGE QUALIFICATION REPORT</i></li> <li>• <i>T-N90-CL-QR-027:</i> <i>TSMC 90 NM CMOS LOGIC HIGH PERFORMANCE (GT) 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N90-CL-QR-028:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V QUALIFICATION REPORT-FAB12 PHASE-3</i></li> <li>• <i>T-N90-CL-QR-029:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N90-CL-QR-035:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8&amp;3.3V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N90-CL-QR-039:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 0P3M SALICIDE X-METAL 1.2&amp;2.5V ROUTING QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N90-CL-QR-042:</i> <i>TSMC 90 NM CMOS LOGIC LOW POWER 1P7M SILICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N90-CL-QR-052:</i> <i>TSMC 90NM WIRE BOND (NON CUP) PACKAGE WITH LEAD FREE BGA QUALIFICATION REPORT</i></li> <li>• <i>T-N90-CL-QR-053:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V PROCESS QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N90-CL-QR-054:</i> <i>TSMC 90NM CMOS LOGIC GENERAL PURPOSE 1P3M SALICIDE CU_LOWK 1.0V/1.8V PROCESS QUALIFICATION REPORT -FAB12</i></li> <li>• <i>T-N90-CL-QR-057:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V AL FUSE WITH DUAL PASSIVATION SCHEME RELIABILITY PRODUCT QUALIFICATION REPORT - Fab12</i></li> <li>• <i>T-N90-CL-QR-059:</i> <i>TSMC 90 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;3.3V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N90-CL-QR-065:</i> <i>TSMC 90 NM CMOS LOGIC GENERAL PURPOSE CU_LOWK QUALIFICATION REPORT-2XTM PROCESS- FAB14</i></li> <li>• <i>T-N90-CL-QR-069:</i> <i>TSMC 90 NM CMOS LOGIC LOW POWER 1P6M SALICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT- FAB12</i></li> <li>• <i>T-N85-CL-QR-001:</i> <i>TSMC 85 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOW_K 1.2&amp;3.3V PROCESS QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N85-CL-QR-002:</i> <i>TSMC 85 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOW_K 1.2&amp;3.3V PROCESS QUALIFICATION REPORT-FAB12</i></li> </ul>

Content	Reference Documentation
	<p><i>TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V PROCESS QUALIFICATION REPORT - FAB14</i></p> <ul style="list-style-type: none"> <li>• <i>T-N85-CL-QR-003:</i> <i>TSMC 85 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.0V/2.5V HIGH DENSITY (1K BITS) ELECTRICAL FUSE IP QUALIFICATION REPORT</i></li> <li>• <i>T-N85-CL-QR-004:</i> <i>TSMC 85 NM CMOS LOGIC GRNERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0V/2.5V HIGH DENSITY (1K BITS) ELECTRICAL FUSE IP QUALIFICATION REPORT</i></li> <li>• <i>T-N85-CL-QR-005:</i> <i>TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N85-CL-QR-007:</i> <i>TSMC 85 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N85-CL-QR-008:</i> <i>TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N85-CL-QR-009:</i> <i>TSMC 85 NM CMOS LOGIC LOW POWER 1P9M SALICIDE LOWK AND CU 1.2&amp;2.5V QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N85-CL-QR-010:</i> <i>TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8&amp;3.3V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N80-CL-QR-001:</i> <i>TSMC 80 NM CMOS LOGIC GENERAL PURPOSE (GT) 1P9M SALICIDE CU_LOW K 1.2/2.5V QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N80-CL-QR-002:</i> <i>TSMC 80 NM CMOS LOGIC HIGH SPEED 1P9M SALICIDE CU_LOWK 1.05/1.8V QUALIFICATION REPORT - FAB12</i></li> <li>• <i>T-N80-CL-QR-003:</i> <i>TSMC 80 NM CMOS LOGIC HIGH SPEED 1P9M SALICIDE CU_LOWK 1.05&amp;2.5V QUALIFICATION REPORT - FAB12</i></li> <li>• <i>T-N80-CL-QR-005:</i> <i>TSMC 80 NM CMOS LOGIC GENERAL PURPOSE (GT) 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT- FAB14</i></li> <li>• <i>T-N80-CL-QR-007:</i> <i>TSMC 80NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOW K 1.2/2.5V QUALIFICATION REPORT - FAB14</i></li> <li>• <i>T-N80-CL-QR-008:</i> <i>TSMC 80NM CMOS LOGIC GENERAL PURPOSE (GC) 1P9M SALICIDE CU_LOW K 1.0/2.5V QUALIFICATION REPORT - FAB12</i></li> <li>• <i>T-N80-CL-QR-009:</i> <i>TSMC 80NM CMOS LOGIC GENERAL PURPOSE (GC) 1P9M SALICIDE CU_LOW K 1.0/3.3V QUALIFICATION REPORT - FAB12</i></li> <li>• <i>T-N80-CL-QR-010:</i> <i>TSMC 80 NM CMOS LOGIC GENERAL PURPOSE (GC) 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V QUALIFICATION REPORT-FAB14</i></li> <li>• <i>T-N80-CL-QR-011:</i> <i>TSMC 80 NM CMOS LOGIC GENERAL PURPOSE (GC) 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V QUALIFICATION REPORT - FAB14</i></li> <li>• <i>T-N80-CL-QR-012:</i> <i>TSMC 80 NM CMOS LOGIC 1P9M SALICIDE CU_LOWK TOP METAL FUSE QUALIFICATION REPORT -FAB14</i></li> <li>• <i>T-N80-CL-QR-015:</i> <i>TSMC 80 NM CMOS LOGIC GENERAL PURPOSE CU_LOWK QUALIFICATION REPORT-2XTM PROCESS-FAB12</i></li> <li>• <i>T-N80-CL-QR-016:</i> <i>TSMC 80 NM CMOS LOGIC GENERAL PURPOSE QUALIFICATION REPORT-2XTM PROCESS-FAB14</i></li> <li>• <i>T-N90-CM-QR-003:</i> <i>TSMC 90NM CMOS MIXED SIGNAL RF GENERAL PURPOSE 1P9M SALICIDE CU_LOW K 1.2/2.5V QUALIFICATION REPORT-FAB12</i></li> <li>• <i>T-N90-CM-QR-004:</i> <i>TSMC 90 NM CMOS MIXED SIGNAL MS LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V QUALIFICATION REPORT-FAB12</i></li> </ul>

Content	Reference Documentation
Brief process flow	<ul style="list-style-type: none"> <li>• <b>T-N90-CL-PF-001:</b> TSMC 90 NM CMOS LOGIC LOW POWER 1P6M SALICIDE CU_LOWK 1.2&amp;2.5V (or 1.2&amp;3.3V) BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-002:</b> TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8&amp;3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-004:</b> TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-007:</b> TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-008:</b> TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-009:</b> TSMC 90 NM CMOS LOGIC HIGH PERFORMANCE (GT) 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-013:</b> TSMC 90 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-014:</b> TSMC 90 NM CMOS LOGIC HIGH PERFORMANCE (GT) 1P9M SALICIDE CU_LOWK 1.2&amp;1.8V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-015:</b> TSMC 90 NM CMOS LOGIC HIGH PERFORMANCE (GT) CD PUSH 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V BRIEF PROCESS FLOW</li> <li>• <b>T-N90-CL-PF-019:</b> TSMC 90 NM CMOS LOGIC LOW POWER 1P6M SALICIDE CU_FSG 1.2&amp;3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N85-CL-PF-002:</b> TSMC 85 NM CMOS LOGIC LOW POWER 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V (OR 1.2&amp;3.3V) BRIEF PROCESS FLOW</li> <li>• <b>T-N85-CL-PF-008:</b> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N85-CL-PF-009:</b> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;1.8&amp;3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N85-CL-PF-010:</b> TSMC 85 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.0&amp;2.5V BRIEF PROCESS FLOW</li> <li>• <b>T-N80-CL-PF-003:</b> TSMC 80 NM CMOS LOGIC GENERAL PURPOSE 1P9M SALICIDE CU_LOWK 1.2&amp;2.5V BRIEF PROCESS FLOW</li> <li>• <b>T-N80-CL-PF-005:</b> TSMC 80 NM CMOS LOGIC HIGH SPEED 1P10M SALICIDE CU_LOWK 1.05/1.8V BRIEF PROCESS FLOW</li> <li>• <b>T-N80-CL-PF-006:</b> TSMC 80 NM CMOS LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M SALICIDE CU_LOWK 1.0/NA/3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N80-CL-PF-007:</b> TSMC 80 NM CMOS LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M SALICIDE CU_LOWK 1.0&amp;3.3V BRIEF PROCESS FLOW</li> <li>• <b>T-N80-CL-PF-010:</b> TSMC 80 NM CMOS LOGIC GENERAL PURPOSE CONSUMER PLATFORM 1P9M SALICIDE NBL/PBL EPI CU_LOWK 1.0&amp;2.5V BRIEF PROCESS FLOW (CLN80GC)</li> <li>• <b>T-N90-CM-PF-001:</b> TSMC 90 NM CMOS MIXED SIGNAL MS GENERAL PURPOSE 1P9M SALICIDE CU_LOWK BRIEF PROCESS FLOW</li> </ul>
Testline Layout Guideline	<ul style="list-style-type: none"> <li>• <b>E-MSS-02-02-024</b> <b>TSMC TEST LINE LAYOUT USER GUIDELINE</b></li> </ul>

## 2 Technology Overview

This chapter provides information about the following:

- 2.1 Semiconductor process (including front-end and back-end features)
- 2.2 Devices
- 2.3 Power supply and operation temperature ranges
- 2.4 Cross-section
- 2.5 Metallization options

### 2.1 Semiconductor Process

The process consists of the front-end features and the back-end features.

#### 2.1.1 Front-End Features

- **Shallow trench isolation (STI)**  
Used for active isolation to reduce active pitch (OD pitch)
- **Retrograde twin well CMOS technology on P- substrate (epitaxy wafer) (substrate resistivity of 8-12 Ω·cm)**  
For a low well sheet resistance and enhancement of latch-up behavior (compared to conventionally diffused wells). Also provides for a good control of short parasitic field transistors.
- **Triple well, Deep N-Well (optional)**  
For isolating P-Well from the substrate
- **Dual gate oxide and triple gate oxide process**
  - Dual gate oxide (1.0V/2.5V, 1.0V/3.3V, 1.0V/1.8V, 1.2V/1.8V, 1.2V/2.5V, 1.2V/3.3V, 1.05V/1.8V, 1.05V/2.5V)
  - Triple gate oxide (1.0V/1.8V/3.3V)
- **N+/P+ poly gate**  
Allows symmetrical design of NMOS and PMOS devices
- **Multiple V<sub>t</sub> devices for low leakage or high performance requirements**  
These devices may be mixed on the same die.
- **Native devices with different gate oxide and application voltage**
- **N90 SRAM cells in different process**

Process Type	N90G		N90GT		N90LP	
SRAM <sup>†</sup>	UHD	DP	UHD	DP	UHD	HD
Cell Size	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.15um <sup>2</sup>

- **N85 SRAM cells in different process:**

Process Type	N85G		N85LP		
SRAM <sup>†</sup>	UHD	DP	UHD	SP	DP
Cell Size (N90 drawn dimension)	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.15um <sup>2</sup>	1.99um <sup>2</sup>

<sup>†</sup> UHD: Ultra High Density; DP: Dual Port; SP: Single Port

- N80 SRAM cells in different process:**

Process Type	CLN80GC		CLN80GT		CLN80HS		CLN80LP
SRAM <sup>†</sup>	UHD	DP	UHD	DP	UHD	DP	SP
Cell Size (N90 drawn dimension)	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	1.15um <sup>2</sup>

<sup>†</sup> UHD: Ultra High Density; HD: High Density; DP: Dual Port; SP: Single Port

- Self-aligned Co-silicided drain, source and gate**

Cobalt silicide is designed to connect N+ and P+ gates; furthermore, it drastically reduces gate and S/D serial resistance. Self-aligned silicide on source/drain structures allows butting straps with only one minimally sized contact.

- Unsilicided N+/P+ poly and OD resistors**

Silicide protection (requires one additional mask, RPO) is used to prevent silicide formation over the active and poly area.

- NW resistor**

Two kinds of NW resistor: 1) NW resistor within OD, and 2) NW resistor under STI

- Varactor**

MOS varactor provides 1.0V/1.2V/1.8V/2.5V/3.3V NMOS-in-NW capacitor structure.

## 2.1.2 Back-End Features

- **Tungsten contact connecting poly or OD to first metal level**
- **3-9 Cu metal levels, plus last metal level in Al pad**
- **2 kinds of top metal:**
  - Mn (3XTM): top metal pitch with 3 times of Mx pitch with 8500Å thickness.
  - My (2XTM): top metal pitch with 2 times of Mx pitch with 5600Å thickness.
    - 2XTM provides higher metal routing density at the expense of IR drop. You need to evaluate the impact of IR drop to their devices. Normally, 2XTM is less suitable for high speed applications.
  - UTM: top metal for inductor metal, W/S=2µm/2µm, thickness=34000 Å, for CMN90/ CMN85, not for CMN80.
- **AP-MD layer can be used as interconnection. Two kinds of AP-MD thickness, 14.5K and 28K, are offered. CAD layer (42;0) of both AP-MD is the same.**

	Mask ID	CAD Layer	Thickness (Å)	Remark
AP	307	42	14500	Cannot use for interconnection, RDL
			28000	
AP_MD	309	42	14500	Can use for interconnection, RDL
			28000	

- One or two thick last (top) Cu metal layers at a relaxed pitch for power, clock, busses, and major interconnect signal distribution
- Tight pitch levels for routing on thin Cu for the other metal levels below the thick level
- Chemical mechanical polishing (CMP) for enhanced planarization (STI, contact, metals, vias, passivation)
- Dual damascene copper interconnection, for metal-2 to the last (top) metal
- Low K (<3.0) inter-metal dielectric for thin metal
- Metal oxide metal (MOM) capacitor
  - Use metal lines to design metal capacitor.
- Metal-insulator-metal (MIM) capacitor for Mixed Signal and RF process:
  - Use the PEOX USG film as the dielectric film of MiM capacitors and use TaN/AICu as the capacitor metal plate. 3 kinds of MiM process are supported:  $1.0\text{fF}/\mu\text{m}^2$ ,  $1.5\text{fF}/\mu\text{m}^2$ ,  $2.0\text{fF}/\mu\text{m}^2$ . Only one kind of MIM capacitor can be used in the chip.
- High-Q copper inductor for N90 RF process:
  - Have ultra thick Cu (UTM, 34 KÅ) process for inductor metal.
- **TSMC N80 generation does not support inductor devices.**
- **Wire bond or flip chip terminals**
- **Laser fuse**

	Cu top metal fuse	AP fuse
3XTM	Available	Available
2XTM	Not allowed	Available

- **Electrical fuse**

The IP of electrical fuse is provided. Please contact your account manager to get the related information. Besides, the IP can't be shrunk at N80.

## 2.2 Devices

The technology provides multiple V<sub>t</sub> devices, and optional thin and thick gate oxide native devices.

**Table 2.2.1 Available Vt/ MOM/ MIM/ Inductor in each technology**

Core	CLN90			CLN85		CLN80			
	G (1.0V)	LP (1.2V)	GT (1.2V)	G (1.0V)	LP (1.2V)	GC (1.0V)	GT (1.2V)	HS (1.05V)	LP (1.2V)
*High Vt	V	V	V	V	V	V	V	V	V
STD Vt	V	V	V	V	V	V	V	V	V
*Low Vt	V	V	V	V	V	V	-	V	-
Ultra low Vt	-	V	-	-	V	-	-	-	-
Native	V	V	V	V	V	V	V	V	-
MiM	-	-	-	-	-	-	-	-	-
MoM	V	V	V	V	V	V	V	V	V
Inductor	-	-	-	-	-	-	-	-	-

Core	CMN90 for MS			CMN85 for MS		CMN80 for MS		CMN90 for RF	
	G (1.0V)	LP (1.2V)	GT (1.2V)	G (1.0V)	LP (1.2V)	GC (1.0V)	G (1.0V)	LP (1.2V)	
*High Vt	V	V	V	V	V	V	-	-	-
STD Vt	V	V	V	V	V	V	V	V	
*Low Vt	V	V	V	V	V	V	-	-	-
Ultra low Vt	-	V	-	-	V	-	-	V	
Native	V	V	V	V	V	V	-	-	-
MiM	V	V	V	V	V	V	V	V	
MoM	V	V	V	V	V	V	V	V	
Inductor	-	-	-	V	V	-	V	V	

**Table Notes:**

1. Different implant process to form High Vt device:

	CLN90			CLN85		CLN80			CMN90 for MS		CMN85 for MS		CMN80 for MS		CMN90 for RF		
	G	LP	GT	G	LP	GC	GT	HS	LP	G	LP	GT	G	LP	GC	G	LP
VTH_P	127 Well	127 Well	125 LDD	127 Well	127 Well	127 Well	127 Well	125 LDD	127 Well	127 Well	127 Well	125 LDD	127 Well	127 Well	127 Well	127 Well	127 Well
VTH_N	128 Well	126 LDD	128 Well	128 Well	128 Well	128 Well	128 Well	128 Well	128 Well	128 Well	128 Well						

2. Different approaches to form Low Vt device:

Core	N90			N85			N80	
	G	LP	GT	G	LP	GC	HS	
VTL_N (mask ID:118)/ VTL_P(mask ID:117) implant	Yes		No	No		Yes	No	Yes
GDS layer name (number) to tape out VTL_N / VTL_P mask	VTL_N (12)/ VTL_P (13)		No	No	VTL_N (12)/ VTL_P (13)	No	VTL_N (12)/ VTL_P (13)	VTL_N (12)/ VTL_P (13)
Logical operation to push PO gate dimension	No		Yes	Yes	No	Yes	No	No
GDS layer name (number) in PO logical operation to recognize low Vt device	No	PSPO (17;51)	VTL_N (12)/ VTL_P (13)	No	PSPO (17;51)	No	No	No

## 2.3 Power Supply and Operation Temperature Ranges

Table 2.3.1 Power Supplies

	CLN90						CLN85			
	G		LP		GT		G		LP	
	Normal power supply	*Max power supply								
Core (thin oxide) (overdrive)	1.0V (1.2V)	1.1V (1.26V)	1.2V (1.4V)	1.32 (1.47)	1.2V	1.26V	1.0V (1.2V)	1.1V (1.26V)	1.2V (1.4V)	1.32 (1.47)
I/O (thick oxide)	1.8V	1.98V	-		1.8V	1.98V	3.3V	3.63V	3.3V	3.63V
	2.5V	2.75V								
	3.3V	3.63V	3.3V	3.63V	-	-	1.8V	1.98V	-	-
	1.8V and 3.3V	-	-	-	-	-	1.8V and 3.3V	-	-	-

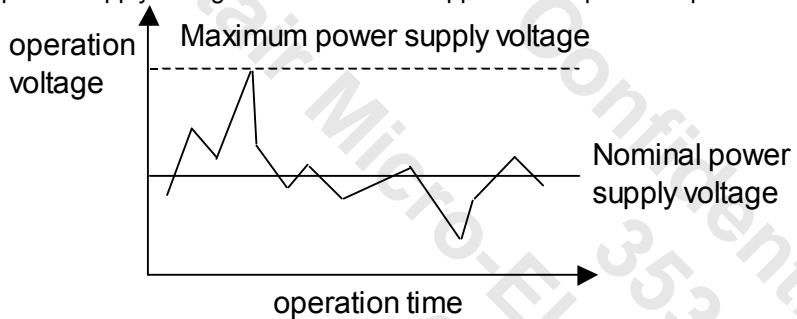
	CLN80							
	GC		GT		HS		LP	
	Normal power supply	*Max power supply						
Core (thin oxide) (overdrive)	1.0V (1.2V)	1.1V (1.26V)	1.2V	1.26V	1.05V	1.1V	1.2V (1.4V)	1.32 (1.47)
I/O (thick oxide)	-	-	1.8V	1.98V	1.8V	1.98V	-	-
	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V	2.5V	2.75V
	3.3V	3.63V	-	-	-	-	-	-
	-	-	-	-	-	-	-	-

	CMN90 for MS						CMN85 for MS				CMN80 for MS	
	G		LP		GT		G		LP		GC	
	Normal power supply	*Max power supply										
Core (thin oxide) (overdrive)	1.0V (1.2V)	1.1V (1.26V)	1.2V (1.4V)	1.32 (1.47)	1.2V	1.26V	1.0V (1.2V)	1.1V (1.26V)	1.2V (1.4V)	1.32 (1.47)	1.0V (1.2V)	1.1V (1.26V)
I/O (thick oxide)	1.8V	1.98V	-	-	1.8V	1.98V	3.3V	3.63V	3.3V	3.63V	-	-
	2.5V	2.75V										
	3.3V	3.63V	3.3V	3.63V	-	-	-	-	-	-	3.3V	3.63V
	1.8V and 3.3V	-	-	-	-	-	-	-	-	-	-	-

	CMN90 for RF			
	G		LP	
	Normal power supply	*Max power supply	Normal power supply	*Max power supply
<b>Core (thin oxide) (overdrive)</b>	1.0V (1.2V)	1.26V	1.2V (1.4V)	1.32 (1.47)
<b>I/O (thick oxide)</b>	-	-	-	-
	2.5V	2.75V	2.5V	2.75V
	3.3V	3.63V	3.3V	3.63V
	-	-	-	-

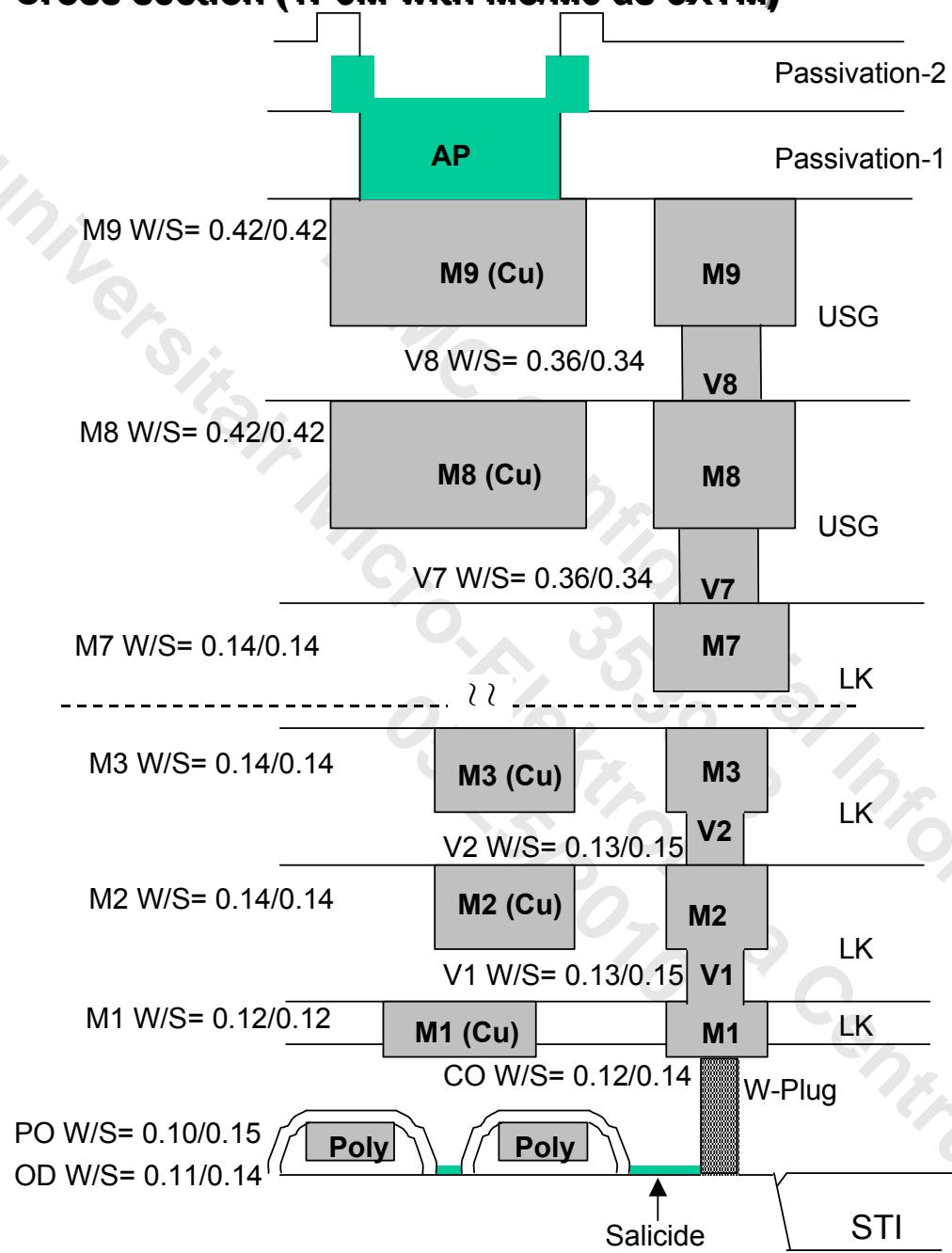
The operation temperature range is -40°C to 125°C (junction temperature).

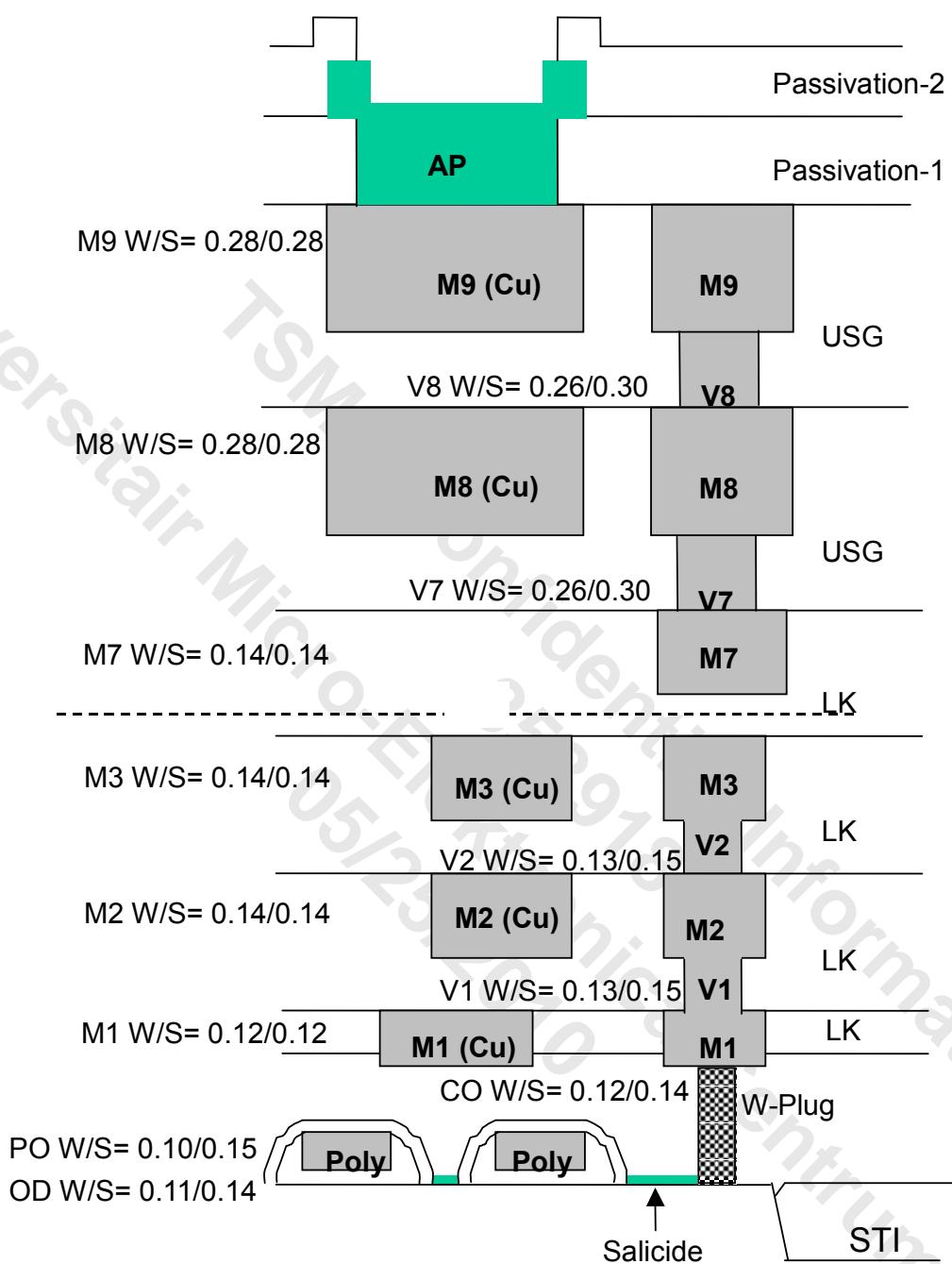
For more information of over-drive voltage, please refer to section 12.2.1: Guidelines for Overdrive Voltage. Maximum power supply voltage means variation upper limit of product operation voltage.



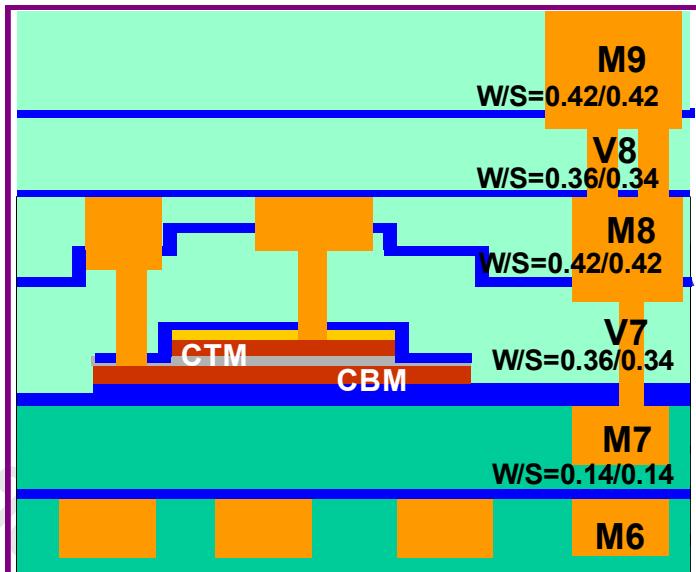
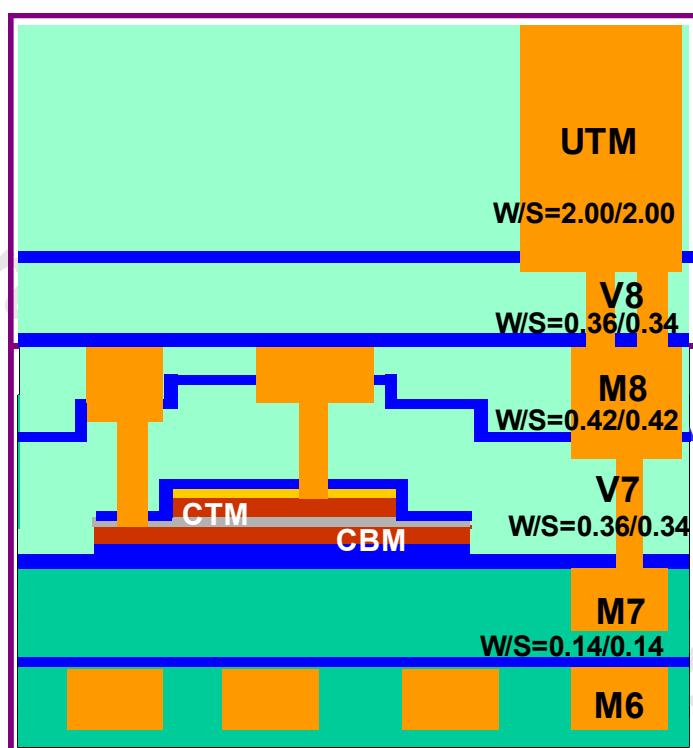
## 2.4 Cross-section

### Cross section (1P9M with M8/M9 as 3XTM)

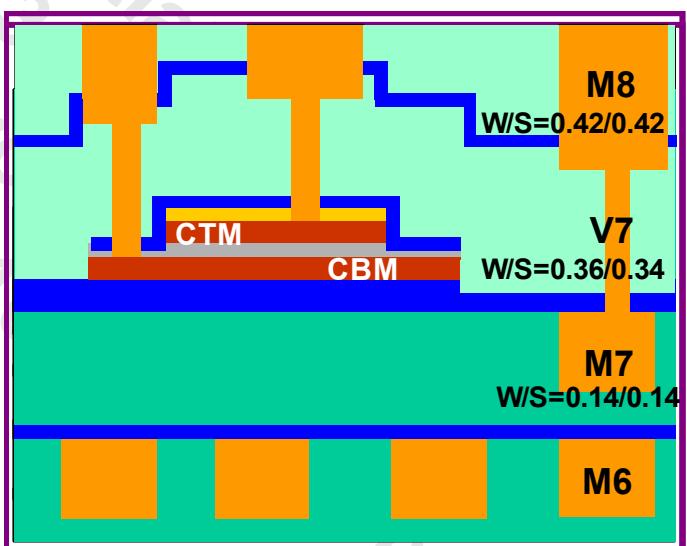
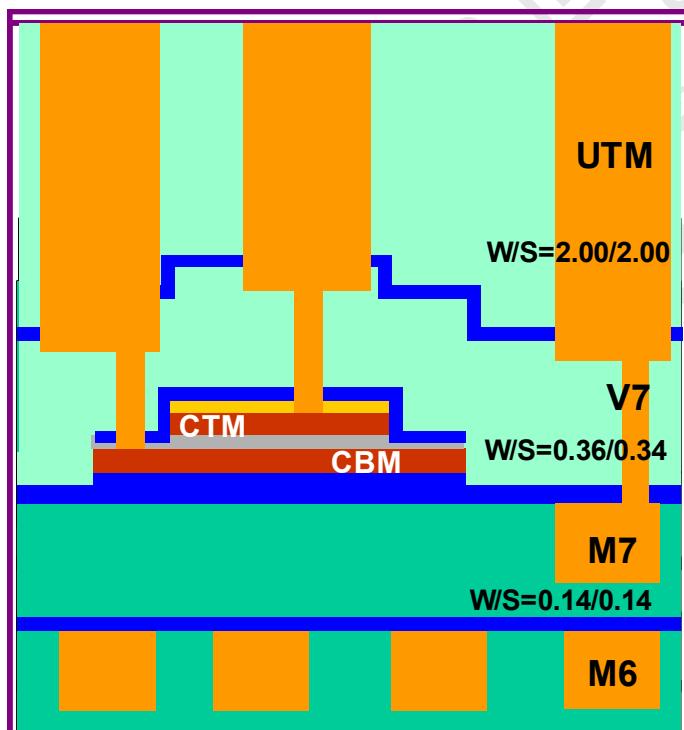


**Cross section (1P9M with M8/M9 as 2XTM)**

(1) 1P9M: MIM between M7 and M8 with UTM (34KÅ) (2) 1P9M: MIM between M7 and M8, without UTM



(3) 1P8M: MIM between M7 and M8 (M8 is UTM) (4) 1P8M: MIM between M7 and M8, without UTM



## 2.5 Metallization Options

The general 90/85/80 nm logic process offers a single poly and nine metal layers (1P9M). In addition to 1P9M, please refer to the following tables for the other metallization options.

**Table 2.5.1 Naming for Different Metal Thicknesses**

Metal type	Code	W/S ( $\mu\text{m}$ )						Thickness ( $\text{\AA}$ )						Mask layers
		CLN90	CLN85	CLN80	CMN90	CMN85	CMN80	CLN90	CLN85	CLN80	CMN90	CMN85	CMN80	
M1	M1	0.12/ 0.12	0.12/ 0.12	0.12/ 0.12	0.12/ 0.12	0.12/ 0.12	0.12/ 0.12	2400	2400	2300	2400	2400	2300	M1 (360) only
Inter-layer Metal	Mx	0.14/ 0.14	0.14/ 0.14	0.14/ 0.14	0.14/ 0.14	0.14/ 0.14	0.14/ 0.14	3100	3100	2600	3100	3100	2600	M2~M7 (380, 381, 384, 385, 386, 387), maximum: six layers
Top Metal (3XTM)	Mn	0.42/ 0.42	0.42/ 0.42	0.42/ 0.42	0.42/ 0.42	0.42/ 0.42	0.42/ 0.42	8500	8500	8500	8500	8500	8500	M3~M9 (381, 384, 385, 386, 387, 388, 389), maximum: two layers
Top Metal (2XTM)	My	0.28/ 0.28	0.28/ 0.28	0.28/ 0.28	0.28/ 0.28	Not offer	0.28/ 0.28	5600	5600	5600	Not offer	Not offer	Not offer	M3~M9 (381, 384, 385, 386, 387, 388, 389), maximum: two layers
Top Metal	UTM	Not offer	Not offer	Not offer	2.0/ 2.0	2.0/ 2.0	Not offer	Not offer	Not offer	Not offer	34000	34000	Not offer	M4~M9 (384, 385, 386, 387, 388, 389), maximum: one layers
AP-MD	AP-MD	3/2	3/2	3/2	3/2	3/2	3/2	14500	14500	14500	14500	14500	14500	AP-MD(307 or 309) Max: one layer. 14.5K and 28K $\text{\AA}$ are offered.
								28000	28000	28000	28000	28000	28000	

Mn and My can not be used on the same die.

**Table 2.5.2 Naming for Different Via Types**

Via type	Code	W/S ( $\mu\text{m}$ )						Mask layers			
		CLN90	CLN85	CLN80	CMN90	CMN85	CMN80				
Inter-layer Via	Vx	0.13/ 0.15	0.13/ 0.15	0.13/ 0.15	0.13/ 0.15	0.13/ 0.15	0.13/ 0.15	VIA1~VIA6 (378, 379, 373, 374, 375, 376), maximum: six layers			
Top Via (3XTM) (UTM)	Vn	0.36/ 0.34	0.36/ 0.34	0.36/ 0.34	0.36/ 0.34	0.36/ 0.34	0.36/ 0.34	VIA2~VIA8 (379, 373, 374, 375, 376, 377, 372), maximum: two layers for 3XTM maximum: one layers for UTM			
Top Via (2XTM)	Vy	0.26/ 0.30	0.26/ 0.30	0.26/ 0.30	0.26/ 0.30	0.26/ 0.30	Not offer	0.26/ 0.30	VIA2~VIA8 (379, 373, 374, 375, 376, 377, 372), maximum: two layers		
RV*	RV	3/3	3/3	3/3	3/3	3/3	3/3	3/3	RV (306), max: one layer		

Vn and Vy can not be used on the same die.

- \*: 1. With AP-MD process, CBD (mask 306)/ AP-MD (mask 309)/ CB2 (mask 308) are used. RV is needed to connect AP-MD and Mtop when AP-MD is an additional interconnection layer.
- 2. Without AP-MD process, CB (CBD) (mask 107)/ AP (mask 307)/ CB(CBD) (mask 107) are used and no RV layer is used. CB layer is for interconnection usage.

**Table 2.5.3 Metallization Options for 3XTM for CLN90/ CLN85/ CLN80**

Metal /Via	Total Number of Metal Layers (3XTM)									
	3	4	5	6	7	8	9			
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx	Vx	Vx	Vx	Vx	Vx	Vx
M2	Mx	Mx	Mx	Mx	Mx	Mx	Mx	Mx	Mx	Mx
VIA2	<b>Vn</b>	Vx	<b>Vn</b>	Vx						
M3	<b>Mn</b>	Mx	<b>Mn</b>	Mx						
VIA3		<b>Vn</b>	<b>Vn</b>	Vx	<b>Vn</b>	Vx	Vx	Vx	Vx	Vx
M4		<b>Mn</b>	<b>Mn</b>	Mx	<b>Mn</b>	Mx	Mx	Mx	Mx	Mx
VIA4				<b>Vn</b>	<b>Vn</b>	Vx	<b>Vn</b>	Vx	Vx	Vx
M5				<b>Mn</b>	<b>Mn</b>	Mx	<b>Mn</b>	Mx	Mx	Mx
VIA5					<b>Vn</b>	<b>Vn</b>	Vx	<b>Vn</b>	Vx	Vx
M6					<b>Mn</b>	<b>Mn</b>	Mx	<b>Mn</b>	Mx	Mx
VIA6							<b>Vn</b>	<b>Vn</b>	Vx	<b>Vn</b>
M7							<b>Mn</b>	<b>Mn</b>	Mx	<b>Mn</b>
VIA7									<b>Vn</b>	<b>Vn</b>
M8									<b>Mn</b>	<b>Mn</b>
VIA8										<b>Vn</b>
M9										<b>Mn</b>
RV	V	V	V	V	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V	V	V	V	V

**Table 2.5.4 Metallization Options for 2XTM for CLN90/ CLN85/ CLN80**

Metal /Via	Total Number of Metal Layers (2XTM)									
	3	4	5	6	7	8	9			
M1	M1	M1	M1	M1	M1	M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx	Vx	Vx	Vx	Vx	Vx	Vx
M2	Mx	Mx	Mx	Mx	Mx	Mx	Mx	Mx	Mx	Mx
VIA2	<b>Vy</b>	Vx	<b>Vy</b>	Vx						
M3	<b>My</b>	Mx	<b>My</b>	Mx						
VIA3		<b>Vy</b>	<b>Vy</b>	Vx	<b>Vy</b>	Vx	Vx	Vx	Vx	Vx
M4		<b>My</b>	<b>My</b>	Mx	<b>My</b>	Mx	Mx	Mx	Mx	Mx
VIA4				<b>Vy</b>	<b>Vy</b>	Vx	<b>Vy</b>	Vx	Vx	Vx
M5				<b>My</b>	<b>My</b>	Mx	<b>My</b>	Mx	Mx	Mx
VIA5					<b>Vy</b>	<b>Vy</b>	Vx	<b>Vy</b>	Vx	Vx
M6					<b>My</b>	<b>My</b>	Mx	<b>My</b>	Mx	Mx
VIA6						<b>Vy</b>	<b>Vy</b>	Vx	<b>Vy</b>	Vx
M7							<b>My</b>	<b>My</b>	Mx	<b>My</b>
VIA7								<b>Vy</b>	<b>Vy</b>	<b>Vy</b>
M8								<b>My</b>	<b>My</b>	<b>My</b>
VIA8										<b>Vy</b>
M9										<b>My</b>
RV	V	V	V	V	V	V	V	V	V	V
AP-MD	V	V	V	V	V	V	V	V	V	V

**Table 2.5.5 Table of Metallization Options for Mn or UTM (one Mn or UTM layers above MIM) for CMN90/CMN85:**

Metal /Via	Total Number of Metal Layers				
	4	5	6	7	8
<b>M1</b>	M1	M1	M1	M1	M1
<b>VIA1</b>	Vx	Vx	Vx	Vx	Vx
<b>M2</b>	Mx	Mx	Mx	Mx	Mx
<b>VIA2</b>	Vx	Vx	Vx	Vx	Vx
<b>M3</b>	Mx	Mx	Mx	Mx	Mx
<b>VIA3</b>	<b>Vn</b>	Vx	Vx	Vx	Vx
<b>M4</b>	<b>Mn/UTM</b>	Mx	Mx	Mx	Mx
<b>VIA4</b>		<b>Vn</b>	Vx	Vx	Vx
<b>M5</b>		<b>Mn/UTM</b>	Mx	Mx	Mx
<b>VIA5</b>			<b>Vn</b>	Vx	Vx
<b>M6</b>			<b>Mn/UTM</b>	Mx	Mx
<b>VIA6</b>				<b>Vn</b>	Vx
<b>M7</b>				<b>Mn/UTM</b>	Mx
<b>VIA7</b>					<b>Vn</b>
<b>M8</b>					<b>Mn/UTM</b>
<b>RV</b>	V	V	V	V	V
<b>AP-MD</b>	V	V	V	V	V
<b>MIM location</b>	<b>M3~M4</b>	<b>M4~M5</b>	<b>M5~M6</b>	<b>M6~M7</b>	<b>M7~M8</b>

**Note:**

1. The mark “————” in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mn, or between Mx and UTM. MIM can not be located between Mn and UTM.

**Table 2.5.6 Table of Metallization Options for Mn without UTM (Two Mn layers above MIM) for CMN90/CMN85:**

Metal /Via	Total Number of Metal Layers				
	5	6	7	8	9
M1	M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx	Vx
M2	Mx	Mx	Mx	Mx	Mx
VIA2	Vx	Vx	Vx	Vx	Vx
M3	Mx	Mx	Mx	Mx	Mx
VIA3	<b>Vn</b>	Vx	Vx	Vx	Vx
M4	<b>Mn</b>	Mx	Mx	Mx	Mx
VIA4	<b>Vn</b>	<b>Vn</b>	Vx	Vx	Vx
M5	<b>Mn</b>	<b>Mn</b>	Mx	Mx	Mx
VIA5		<b>Vn</b>	<b>Vn</b>	Vx	Vx
M6		<b>Mn</b>	<b>Mn</b>	Mx	Mx
VIA6			<b>Vn</b>	<b>Vn</b>	Vx
M7			<b>Mn</b>	<b>Mn</b>	<b>Mx</b>
VIA7				<b>Vn</b>	<b>Vn</b>
M8				<b>Mn</b>	<b>Mn</b>
VIA8					<b>Vn</b>
M9					<b>Mn</b>
RV	V	V	V	V	V
AP-MD	V	V	V	V	V
MIM location	M3~M4	M4~M5	M5~M6	M6~M7	M7~M8

**Note:**

1. The mark “————” in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mn. MIM can not be located between Mn and Mn.

**Table 2.5.7 Table of Metallization Options for Mn with UTM (Mn+UTM layers above MIM) for CMN90/CMN85:**

Metal /Via	Total Number of Metal Layers				
	5	6	7	8	9
M1	M1	M1	M1	M1	M1
VIA1	Vx	Vx	Vx	Vx	Vx
M2	Mx	Mx	Mx	Mx	Mx
VIA2	Vx	Vx	Vx	Vx	Vx
M3	Mx	Mx	Mx	Mx	Mx
VIA3	<b>Vn</b>	Vx	Vx	Vx	Vx
M4	<b>Mn</b>	Mx	Mx	Mx	Mx
VIA4	<b>Vn</b>	<b>Vn</b>	Vx	Vx	Vx
M5	<b>UTM</b>	<b>Mn</b>	Mx	Mx	Mx
VIA5		<b>Vn</b>	<b>Vn</b>	Vx	Vx
M6		<b>UTM</b>	<b>Mn</b>	Mx	Mx
VIA6			<b>Vn</b>	<b>Vn</b>	Vx
M7			<b>UTM</b>	<b>Mn</b>	<b>Mx</b>
VIA7				<b>Vn</b>	<b>Vn</b>
M8				<b>UTM</b>	<b>Mn</b>
VIA8					<b>Vn</b>
M9					<b>UTM</b>
RV	V	V	V	V	V
AP-MD	V	V	V	V	V
MIM location	M3~M4	M4~M5	M5~M6	M6~M7	M7~M8

**Note:**

1. The mark “————” in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mn. MIM can not be located between Mn and UTM.

Table 2.5.8 Table of Metallization Options for Mn (one Mn layers above MIM) for CMN80:

Metal /Via	Total Number of Metal Layers				
	4	5	6	7	8
<b>M1</b>	M1	M1	M1	M1	M1
<b>VIA1</b>	Vx	Vx	Vx	Vx	Vx
<b>M2</b>	Mx	Mx	Mx	Mx	Mx
<b>VIA2</b>	Vx	Vx	Vx	Vx	Vx
<b>M3</b>	Mx	Mx	Mx	Mx	Mx
<b>VIA3</b>	<b>Vn</b>	Vx	Vx	Vx	Vx
<b>M4</b>	<b>Mn</b>	Mx	Mx	Mx	Mx
<b>VIA4</b>		<b>Vn</b>	Vx	Vx	Vx
<b>M5</b>		<b>Mn</b>	Mx	Mx	Mx
<b>VIA5</b>			<b>Vn</b>	Vx	Vx
<b>M6</b>			<b>Mn</b>	Mx	Mx
<b>VIA6</b>				<b>Vn</b>	Vx
<b>M7</b>				<b>Mn</b>	Mx
<b>VIA7</b>					<b>Vn</b>
<b>M8</b>					<b>Mn</b>
<b>RV</b>	V	V	V	V	V
<b>AP-MD</b>	V	V	V	V	V
<b>MIM location</b>	<b>M3~M4</b>	<b>M4~M5</b>	<b>M5~M6</b>	<b>M6~M7</b>	<b>M7~M8</b>

**Note:**

1. The mark “—” in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mn.

**Table 2.5.9 Table of Metallization Options for Mn (Two Mn layers above MIM) for CMN80:**

Metal /Via	Total Number of Metal Layers				
	5	6	7	8	9
<b>M1</b>	M1	M1	M1	M1	M1
<b>VIA1</b>	Vx	Vx	Vx	Vx	Vx
<b>M2</b>	Mx	Mx	Mx	Mx	Mx
<b>VIA2</b>	Vx	Vx	Vx	Vx	Vx
<b>M3</b>	Mx	Mx	Mx	Mx	Mx
<b>VIA3</b>	<b>Vn</b>	Vx	Vx	Vx	Vx
<b>M4</b>	<b>Mn</b>	<b>Mn</b>		Mx	Mx
<b>VIA4</b>	<b>Vn</b>	<b>Vn</b>	Vx	Vx	Vx
<b>M5</b>	<b>Mn</b>	<b>Mn</b>	Mx	Mx	Mx
<b>VIA5</b>		<b>Vn</b>	<b>Vn</b>	Vx	Vx
<b>M6</b>		<b>Mn</b>	<b>Mn</b>	Mx	Mx
<b>VIA6</b>			<b>Vn</b>	<b>Vn</b>	Vx
<b>M7</b>			<b>Mn</b>	<b>Mn</b>	Mx
<b>VIA7</b>				<b>Vn</b>	<b>Vn</b>
<b>M8</b>				<b>Mn</b>	<b>Mn</b>
<b>VIA8</b>					<b>Vn</b>
<b>M9</b>					<b>Mn</b>
<b>RV</b>	V	V	V	V	V
<b>AP-MD</b>	V	V	V	V	V
<b>MIM location</b>	<b>M3~M4</b>	<b>M4~M5</b>	<b>M5~M6</b>	<b>M6~M7</b>	<b>M7~M8</b>

**Note:**

1. The mark “————” in the above table stands for MIM layer.
2. MIM must be placed between Mx and Mn. MIM can not be located between Mn and Mn.

**Table 2.5.10 Top metal numbers of 3XTM or 2XTM for wirebond and flip chip**

	3XTM	2XTM	UTM
Wire bond	1or 2 layers of 3XTM	1or 2 layers of 2XTM	1 layer of UTM
Wire bond with AP RDL (AP-MD)	1or 2 layers of 3XTM + AP-MD	1or 2 layers of 2XTM + AP-MD	1 layer of UTM+ AP-MD
Flip Chip with Cu RDL (MD)	1or 2 layers of 3XTM + MD (3XTM)	1 or 2 layers of 2XTM + MD (2XTM)	Not allow MD above UTM.
Flip Chip without Cu RDL	1or 2 layers of 3XTM	2 layers of 2XTM	1 layer of UTM
Flip Chip with AP RDL (AP-MD)	1or 2 layers of 3XTM + AP-MD	2 layers of 2XTM + AP-MD	1 layer of UTM+ AP-MD

# 3 General Layout Information

This chapter provides the following general layout information:

- 3.1 Mask information, key process sequence, and CAD layers.
- 3.2 Dummy pattern fill CAD layer
- 3.3 Special layer summary
- 3.4 Device truth tables
- 3.5 Mask requirements for device options (High/Std/Low  $V_t$ )
- 3.6 Design geometry restrictions
- 3.7 Design hierarchy guidelines

## 3.1 Mask Information, Key Process Sequence, and CAD Layers

Tables in the section 3.1 list masks and corresponding masking steps.

1. Additionally, **optional masks** include DNW, VTL\_N, VTL\_P, VTH\_N, VTH\_P, ESD, VIAD, MD, CBD, and FW.
2. The **VTC\_N** mask is a default mask generated from a logic operation (SRM NOT NW) for those who use certain SRAM cell IP. Please see the “Special Layer Summary” section in this chapter for information about the SRM layer.
3. TSMC uses NW and OD2 (OD\_18, OD\_25, OD\_33) to generate **NW1V, NW2V (DGO/TGO), PW1V, and PW2V (DGO/TGO)** masks by logical operations. Designers can draw NW only.
4. Layer P1V and P2V are only for tsmc internal use.
5. TSMC uses NP, PP, and other layers to generate **N1V, N2V (DGO/TGO), P1V, P2V (DGO/TGO), N3V (TGO), and P3V (TGO)** masks by logical operations. Designers do not need to draw these masks.
6. SEALRING layer (CAD layer: 162) is a must for VIAx if either you add sealring by themselves or metal fuse is used. SEALRING layer (CAD layer: 162) is only allowed in sealring and fuse protection ring.
7. In the table of section 3.1, “\*” means optional mask. “#” means non-design level mask which is no need to draw (or design) this layer. This non-design level mask is generated by logical operation from other drawn layers.
8. An **AI pad** is a reverse tone of CB with bias. However, in a flip-chip product, AI pad is a drawn layer.

The **Mask Name column** lists names that are reserved for standard mask steps. These names should not be used for another purpose in tapeout files without prior authorization from TSMC.

The **CAD Layer column** lists CAD layer numbers. To obtain all related CAD layer usage information, please refer to TSMC Document *T-N90-LO-LE-001*.



**Warning:** A CAD layer number must be less than, or equal to, 255. If the number is greater than 255, the mask making will fail.

**Table 3.1.1 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN90G**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V (DGO)	191	D	Derived	<b>1.0V/1.8V:</b> NW, NT_N <b>1.0V/2.5V:</b> OD_25, NW, NT_N <b>1.0V/3.3V:</b> OD_33, NW, NT_N	1.0V and 1.8V P-Well for DGO process.
4*#	PW1V (TGO)	191	D	Derived	<b>1.0V/1.8/3.3V:</b> OD_33, NW, NT_N	1.0V and 1.8V P-Well for TGO process.
5*	VTH_N	128	C	67	-	1.0V high Vt NMOS implantation.
6*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
7#	PW2V (DGO)	193	C	Derived	<b>1.0V/1.8V:</b> No need <b>1.0V/2.5V:</b> OD_25, NW, NT_N <b>1.0V/3.3V:</b> OD_33, NW, NT_N	2.5V, or 3.3V P-Well for DGO process.
8*#	PW2V (TGO)	193	C	Derived	<b>1.0V/1.8/3.3V:</b> OD_33, NW, NT_N	3.3V P-Well for TGO process..
9#	NW1V (DGO)	192	C	Derived	NW, NT_N	1.0V and 1.8V N-Well for DGO process.
10*#	NW1V (TGO)	192	C	Derived	NW, NT_N	1.0V, 1.8V, and 3.3V N-Well for TGO process.
11*	VTH_P	127	C	68	-	1.0V high Vt PMOS implantation.
12#	NW2V (DGO)	194	C	Derived	<b>1.0V/1.8V:</b> NW, OD_18, NT_N <b>1.0V/2.5V:</b> NW, OD_25, NT_N <b>1.0V/3.3V:</b> NW, OD_33, NT_N	1.8V, 2.5V, or 3.3V N-Well for DGO process..
13*#	NW2V (TGO)	194	C	Derived	<b>1.0V/1.8/3.3V:</b> OD_33, OD_18, NW, NT_N	1.8V and 3.3V N-Well for TGO process..
14	OD2 (DGO)	132	D	16,41, 15	<b>1.0V/1.8V:</b> OD_18 <b>1.0V/2.5V:</b> OD_25 <b>1.0V/3.3V:</b> OD_33	1.8V, 2.5V, or 3.3V thick oxide for DGO process.
15*	OD2 (TGO)	132	D	16,15	<b>1.0V/1.8/3.3V:</b> OD_18, OD_33	1.8V and 3.3V thick oxide for TGO process.
16*	OD3 (TGO)	131	C	16	<b>1.0V/1.8/3.3V:</b> OD_18	1.8V thick oxide for TGO process.
17	NP	198	C	Derived	NP, SRM, POFUSE	Pre-doped N+ poly. (Dual use layer)
18	PO	130	D	Derived	<b>1.0V/1.8V:</b> PO, OD, OD_18, NP, PP, SRM, DPO <b>1.0V/2.5V:</b> PO, OD, OD_25, NP, PP, SRM, DPO <b>1.0V/3.3V:</b> PO, OD, OD_33, NP, PP, SRM, DPO <b>1.0V/1.8V/3.3V:</b> PO, OD, OD_18, OD_33, NP, PP, SRM, DPO	Poly-Si.
19#	N2V (DGO)	116	C	Derived	<b>1.0V/1.8V:</b> NP, NW, OD_18, RH, VAR <b>1.0V/2.5V:</b> NP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> NP, NW, OD_33, RH, VAR	1.8V, 2.5V, or 3.3V NLDD implantation for DGO process.
20*#	N2V (TGO)	116	C	Derived	<b>1.0V/1.8V/3.3V:</b> NP, NW, OD_33, RH, VAR	3.3V NLDD implantation for TGO process.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
21#	N1V	114	C	Derived	<b>1.0V/1.8V:</b> NP, NW, OD_18, RH, VAR, N1V <b>1.0V/2.5V:</b> NP, NW, OD_25, RH, VAR, N1V <b>1.0V/3.3V:</b> NP, NW, OD_33, RH, VAR, N1V <b>1.0V/1.8V/3.3V:</b> NP, NW, OD_18, OD_33, RH, VAR, N1V	1.0V NLDD implantation.
22*	VTL_N	118	D	Derived	<b>1.0V/1.8V:</b> OD_18, NW, VTL_N, RH, VAR <b>1.0V/2.5V:</b> OD_25, NW, VTL_N, RH, VAR <b>1.0V/3.3V:</b> OD_33, NW, VTL_N, RH, VAR <b>1.0V/1.8V/3.3V:</b> OD_18, OD_33, NW, VTL_N	1.0V low Vt NMOS implantation.
23*#	N3V (TGO)	158	C	Derived	<b>1.0V/1.8V/3.3V:</b> NP, NW, OD_18, RH, VAR	1.8V NLDD implantation for TGO process.
24#	P2V (DGO)	115	C	Derived	<b>1.0V/1.8V:</b> PP, NW, OD_18, RH, VAR <b>1.0V/2.5V:</b> PP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> PP, NW, OD_33, RH, VAR	1.8V, 2.5V, or 3.3V PLDD implantation for DGO process.
25*#	P2V (TGO)	115	C	Derived	<b>1.0V/1.8V/3.3V:</b> PP, NW, OD_33, RH, VAR	3.3V PLDD implantation for TGO process.
26*#	P3V (TGO)	157	C	Derived	<b>1.0V/1.8V/3.3V:</b> PP, NW, OD_18, RH, VAR	1.8V PLDD implantation for TGO process.
27#	P1V	113	C	Derived	<b>1.0V/1.8V:</b> PP, NW, OD_18, RH, VAR, P1V <b>1.0V/2.5V:</b> PP, NW, OD_25, RH, VAR, P1V <b>1.0V/3.3V:</b> PP, NW, OD_33, RH, VAR, P1V <b>1.0V/1.8V/3.3V:</b> PP, NW, OD_18, OD_33, RH, VAR, P1V	1.0V PLDD implantation.
28*	VTL_P	117	C	Derived	<b>1.0V/1.8V:</b> OD_18, NW, VTL_P, RH, VAR <b>1.0V/2.5V:</b> OD_25, NW, VTL_P, RH, VAR <b>1.0V/3.3V:</b> OD_33, NW, VTL_P, RH, VAR <b>1.0V/1.8V/3.3V:</b> OD_18, OD_33, NW, VTL_P	1.0V low Vt PMOS implantation.
29	NP	198	C	Derived	NP, SRM, POFUSE	N+ implantation. (Dual use layer)
30	PP	197	C	25	-	P+ implantation.
31*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
32	RPO	155	D	29	-	Silicide protection.
33	CO	156	C	30	-	Contact window from M1 to OD or PO.
34	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
35	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
36	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
37	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
38	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
39	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.
40	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
41	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
42	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
43	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
44	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
45	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
46	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
47	VIA7	377	C	Derived	-	Via7 hole between M8 and M7.
48	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
49	VIA8	372	C	Derived	-	Via8 hole between M9 and M8.
50	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

51	CB	107	C	43	-	Bonding pad.
52#	AP	307	D	Derived	CB	Al pads.
53*	FW_Cu	395	C	95;0	-	Metal fuse window.
54	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

51*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
52*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
53	CBD	107	C	169	-	Passivation opening on bump pads.
54	AP	307	D	42	-	Al pads.
55*	FW_Cu	395	C	95;0	-	Metal fuse window.
56	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL
53*	FW_AP	30A	C	95;20	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL for flip chip.
53*	FW_AP	30A	C	95;20	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL
53	FW_Cu	395	C	95;0	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL for flip chip.
53	FW_Cu	395	C	95;0	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

**Table 3.1.2 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN90GT**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.2V/1.8V:</b> NW, NT_N <b>1.2V/2.5V:</b> OD_25, NW, NT_N	1.2V P-Well.
4*	VTH_N	128	C	Derived	VTH_N, SRM, NW	1.2V high Vt NMOS implantation.
5*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
6#	PW2V	193	C	Derived	<b>1.2V/1.8V:</b> No <b>1.2V/2.5V:</b> OD_25, NW, NT_N	1.8V or 2.5V P-Well.
7#	NW1V	192	C	Derived	NW, NT_N	1.2V N-Well.
8#	NW2V	194	C	Derived	<b>1.2V/1.8V:</b> NW, OD_18, NT_N <b>1.2V/2.5V:</b> NW, OD_25, NT_N	1.8V or 2.5VN-Well.
9	OD3	131	C	16	<b>1.2V/1.8V:</b> OD_18 <b>1.2V/2.5V:</b> No	1.8V thick oxide
10	OD2	132	D	16 41	<b>1.2V/1.8V:</b> OD_18 <b>1.2V/2.5V:</b> OD_25	2.5V thick oxide.
11	NP	198	C	Derived	NP, SRM, POFUSE	Pre-doped N+ poly. (Dual use layer)
12	PO	130	D	Derived	<b>1.2V/1.8V:</b> PO, OD, OD_18, NP, NT_N, VTL_N, PP, VTL_P, SRM, DPO <b>1.2V/2.5V:</b> PO, OD, OD_25, NP, NT_N, VTL_N, PP, VTL_P, SRM, DPO	Poly-Si.
13#	N2V	116	C	Derived	<b>1.2V/1.8V:</b> NP, NW, OD_25, RH, VAR <b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR	1.8V or 2.5V NLDD implantation.
14#	N1V	114	C	Derived	<b>1.2V/1.8V:</b> NP, NW, OD_25, RH, VAR, N1V <b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR, N1V	1.2V NLDD implantation.
15#	P2V	115	C	Derived	<b>1.2V/1.8V:</b> PP, NW, OD_25, RH, VAR <b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR	1.8V or 2.5V PLDD implantation.
16*	VTH_P	125	C	Derived	VTH_P, SRM, NW	1.2V high Vt PMOS implantation.
17#	P1V	113	C	Derived	<b>1.2V/1.8V:</b> PP, NW, OD_25, RH, VAR, P1V <b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR, P1V	1.2V PLDD implantation.
18	NP	198	C	Derived	NP, SRM, POFUSE	N+ implantation. (Dual use layer)
19	PP	197	C	25	-	P+ implantation.
20*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
21	RPO	155	D	29	-	Silicide protection.
22	CO	156	C	30	-	Contact window from M1 to OD or PO.
23	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
24	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
25	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
26	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
27	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
28	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
29	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
30	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
31	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
32	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
33	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
34	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
35	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
36	VIA7	377	C	57	-	Via7 hole between M8 and M7.
37	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
38	VIA8	372	C	58	-	Via8 hole between M9 and M8.
39	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

40	CB	107	C	43	-	Bonding pad.
41#	AP	307	D	Derived	CB	Al pads.
42*	FW_Cu	395	C	95;0	-	Metal fuse window.
43	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

40*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
41*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
42	CBD	107	C	169	-	Passivation opening on bump pads.
43	AP	307	D	42	-	Al pads.
44*	FW_Cu	395	C	95;0	-	Metal fuse window.
45	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

40	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
41	AP-MD	309	D	42	-	AP RDL
42*	FW_AP	30A	C	95;20	-	Metal fuse window.
43	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

40	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
41	AP-MD	309	D	42	-	AP RDL for flip chip.
42*	FW_AP	30A	C	95;20	-	Metal fuse window.
43	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

40	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
41	AP-MD	309	D	42	-	AP RDL
42	FW_Cu	395	C	95;0	-	Metal fuse window.
43	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

40	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
41	AP-MD	309	D	42	-	AP RDL for flip chip.
42	FW_Cu	395	C	95;0	-	Metal fuse window.
43	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

**Table 3.1.3 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN90LP**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.2V/2.5V:</b> OD_25, NW, NT_N <b>1.2V/3.3V:</b> OD_33, NW, NT_N	1.2V P-Well.
4*	VTH_N	128	C	67	-	1.2V high Vt NMOS implantation.
5*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
6#	PW2V	193	C	Derived	<b>2V/2.5V:</b> OD_25, NW, NT_N <b>1.2V/3.3V:</b> OD_33, NW, NT_N	2.5V, or 3.3V P-Well.
7#	NW1V	192	C	Derived	NW, NT_N	1.2V N-Well.
8*	VTH_P	127	C	68	-	1.2V high Vt PMOS implantation.
9#	NW2V	194	C	Derived	<b>1.2V/2.5V:</b> NW, OD_25, NT_N <b>1.2V/3.3V:</b> NW, OD_33, NT_N	2.5V, or 3.3V N-Well.
10	OD2	132	D	41 15	<b>1.2V/2.5V:</b> OD_25 <b>1.2V/3.3V:</b> OD_33	2.5V, or 3.3V thick oxide.
11	NP	198	C	Derived	NP, SRM, POFUSE	Pre-doped N+ poly. (Dual use layer)
12	PO	130	D	Derived	<b>1.2V/2.5V:</b> PO, OD, OD_25, NP, PP, PSPO, SRM, DPO <b>1.2V/3.3V:</b> PO, OD, OD_33, NP, PP, PSPO, SRM, DPO	Poly-Si.
13#	N2V	116	C	Derived	<b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR <b>1.2V/3.3V:</b> NP, NW, OD_33, RH, VAR	2.5V, or 3.3V NLDD implantation.
14#	N1V	114	C	Derived	<b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR, N1V <b>1.2V/3.3V:</b> NP, NW, OD_33, RH, VAR, N1V	1.2V NLDD implantation.
15#	ULVT_N	11R	D	Derived	<b>1.2V/2.5V:</b> OD_25, NW, VTL_N, RH, VAR <b>1.2V/3.3V:</b> OD_33, NW, VTL_N, RH, VAR	1.2V Ultra low Vt NMOS implantation.
16#	P2V	115	C	Derived	<b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR <b>1.2V/3.3V:</b> PP, NW, OD_33, RH, VAR	2.5V, or 3.3V PLDD implantation.
17#	P1V	113	C	Derived	<b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR, P1V <b>1.2V/3.3V:</b> PP, NW, OD_33, RH, VAR, P1V	1.2V PLDD implantation.
18	ULVT_P	11Q	C	Derived	<b>1.2V/2.5V:</b> OD_25, NW, VTL_P, RH, VAR <b>1.2V/3.3V:</b> OD_33, NW, VTL_P, RH, VAR	1.2V Ultra low Vt PMOS implantation.
19	NP	198	C	Derived	NP, SRM	N+ implantation. (Dual use layer)
20	PP	197	C	25	-	P+ implantation.
21*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
22	RPO	155	D	29	-	Silicide protection.
23	CO	156	C	30	-	Contact window from M1 to OD or PO.
24	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
25	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
26	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
27	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
28	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
29	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.
30	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
31	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
32	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
33	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
34	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
35	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
36	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
37	VIA7	377	C	57	-	Via7 hole between M8 and M7.
38	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
39	VIA8	372	C	58	-	Via8 hole between M9 and M8.
40	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

41	CB	107	C	43	-	Bonding pad.
42#	AP	307	D	Derived	CB	Al pads.
43*	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

41*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
42*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
43	CBD	107	C	169	-	Passivation opening on bump pads.
44	AP	307	D	42	-	Al pads.
45*	FW_Cu	395	C	95;0	-	Metal fuse window.
46	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL
43*	FW_AP	30A	C	95;20	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL for flip chip.
43*	FW_AP	30A	C	95;20	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL
43	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL for flip chip.
43	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

**Table 3.1.4 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN85G**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V (DGO)	191	D	Derived	<b>1.0V/1.8V:</b> NW, NT_N <b>1.0V/2.5V:</b> OD_25, NW, NT_N <b>1.0V/3.3V:</b> OD_33, NW, NT_N	1.0V and 1.8V P-Well for DGO process.
4*#	PW1V (TGO)	191	D	Derived	<b>1.0V/1.8/3.3V:</b> OD_33, NW, NT_N	1.0V and 1.8V P-Well for TGO process.
5*	VTH_N	128	C	67	-	1.0V high Vt NMOS implantation.
6*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
7#	PW2V (DGO)	193	C	Derived	<b>1.0V/1.8V:</b> No need <b>1.0V/2.5V:</b> OD_25, NW, NT_N <b>1.0V/3.3V:</b> OD_33, NW, NT_N	2.5V, or 3.3V P-Well for DGO process.
8*#	PW2V (TGO)	193	C	Derived	<b>1.0V/1.8/3.3V:</b> OD_33, NW, NT_N	3.3V P-Well for TGO process..
9#	NW1V (DGO)	192	C	Derived	NW, NT_N	1.0V and 1.8V N-Well for DGO process.
10*#	NW1V (TGO)	192	C	Derived	NW, NT_N	1.0V, 1.8V, and 3.3V N-Well for TGO process.
11*	VTH_P	127	C	68	-	1.0V high Vt PMOS implantation.
12#	NW2V (DGO)	194	C	Derived	<b>1.0V/1.8V:</b> NW, OD_18, NT_N <b>1.0V/2.5V:</b> NW, OD_25, NT_N <b>1.0V/3.3V:</b> NW, OD_33, NT_N	1.8V, 2.5V, or 3.3V N-Well for DGO process..
13*#	NW2V (TGO)	194	C	Derived	<b>1.0V/1.8/3.3V:</b> OD_33, OD_18, NW, NT_N	1.8V and 3.3V N-Well for TGO process..
14	OD2 (DGO)	132	D	16,41, 15	<b>1.0V/1.8V:</b> OD_18 <b>1.0V/2.5V:</b> OD_25 <b>1.0V/3.3V:</b> OD_33	1.8V, 2.5V, or 3.3V thick oxide for DGO process.
15*	OD2 (TGO)	132	D	16,15	<b>1.0V/1.8/3.3V:</b> OD_18, OD_33	1.8V and 3.3V thick oxide for TGO process.
16*	OD3 (TGO)	131	C	16	<b>1.0V/1.8/3.3V:</b> OD_18	1.8V thick oxide for TGO process.
17	NP	198	C	Derived	NP, SRM, POFUSE	Pre-doped N+ poly. (Dual use layer)
18	PO	130	D	Derived	<b>1.0V/1.8V:</b> PO, OD, OD_18, NP, PP, SRM, DPO <b>1.0V/2.5V:</b> PO, OD, OD_25, NP, PP, SRM, DPO <b>1.0V/3.3V:</b> PO, OD, OD_33, NP, PP, SRM, DPO <b>1.0V/1.8V/3.3V:</b> PO, OD, OD_18, OD_33, NP, PP, SRM, DPO	Poly-Si.
19#	N2V (DGO)	116	C	Derived	<b>1.0V/1.8V:</b> NP, NW, OD_18, RH, VAR <b>1.0V/2.5V:</b> NP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> NP, NW, OD_33, RH, VAR	1.8V, 2.5V, or 3.3V NLDD implantation for DGO process.
20*#	N2V (TGO)	116	C	Derived	<b>1.0V/1.8V/3.3V:</b> NP, NW, OD_33, RH, VAR	3.3V NLDD implantation for TGO process.
21#	N1V	114	C	Derived	<b>1.0V/1.8V:</b> NP, NW, OD_18, RH, VAR, N1V <b>1.0V/2.5V:</b> NP, NW, OD_25, RH, VAR, N1V <b>1.0V/3.3V:</b> NP, NW, OD_33, RH, VAR, N1V <b>1.0V/1.8V/3.3V:</b> NP, NW, OD_18, OD_33, RH, VAR, N1V	1.0V NLDD implantation.
22*	VTL_N	118	D	Derived	<b>1.0V/1.8V:</b> OD_18, NW, VTL_N, RH, VAR <b>1.0V/2.5V:</b> OD_25, NW, VTL_N, RH, VAR <b>1.0V/3.3V:</b> OD_33, NW, VTL_N, RH, VAR <b>1.0V/1.8V/3.3V:</b> OD_18, OD_33, NW, VTL_N	1.0V low Vt NMOS implantation.
23*#	N3V (TGO)	158	C	Derived	<b>1.0V/1.8V/3.3V:</b> NP, NW, OD_18, RH, VAR	1.8V NLDD implantation for TGO process.
24#	P2V (DGO)	115	C	Derived	<b>1.0V/1.8V:</b> PP, NW, OD_18, RH, VAR <b>1.0V/2.5V:</b> PP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> PP, NW, OD_33, RH, VAR	1.8V, 2.5V, or 3.3V PLDD implantation for DGO process.
25*#	P2V (TGO)	115	C	Derived	<b>1.0V/1.8V/3.3V:</b> PP, NW, OD_33, RH, VAR	3.3V PLDD implantation for TGO process.
26*#	P3V (TGO)	157	C	Derived	<b>1.0V/1.8V/3.3V:</b> PP, NW, OD_18, RH, VAR	1.8V PLDD implantation for TGO process.
27#	P1V	113	C	Derived	<b>1.0V/1.8V:</b> PP, NW, OD_18, RH, VAR, P1V <b>1.0V/2.5V:</b> PP, NW, OD_25, RH, VAR, P1V	1.0V PLDD implantation.

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Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
					<b>1.0V/3.3V:</b> PP, NW, OD_33, RH, VAR, P1V <b>1.0V/1.8V/3.3V:</b> PP, NW, OD_18, OD_33, RH, VAR, P1V	
28*	VTL_P	117	C	Derived	<b>1.0V/1.8V:</b> OD_18, NW, VTL_P, RH, VAR <b>1.0V/2.5V:</b> OD_25, NW, VTL_P, RH, VAR <b>1.0V/3.3V:</b> OD_33, NW, VTL_P, RH, VAR <b>1.0V/1.8V/3.3V:</b> OD_18, OD_33, NW, VTL_P	1.0V low Vt PMOS implantation.
29	NP	198	C	Derived	NP, SRM, POFUSE	N+ implantation. (Dual use layer)
30	PP	197	C	25	-	P+ implantation.
31*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
32	RPO	155	D	29	-	Silicide protection.
33	CO	156	C	30	-	Contact window from M1 to OD or PO.
34	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
35	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
36	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
37	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
38	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
39	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.
40	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
41	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
42	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
43	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
44	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
45	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
46	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
47	VIA7	377	C	Derived	-	Via7 hole between M8 and M7.
48	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
49	VIA8	372	C	Derived	-	Via8 hole between M9 and M8.
50	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

51	CB	107	C	43	-	Bonding pad.
52#	AP	307	D	Derived	CB	Al pads.
53*	FW_Cu	395	C	95;0	-	Metal fuse window.
54	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

51*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
52*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
53	CBD	107	C	169	-	Passivation opening on bump pads.
54	AP	307	D	42	-	Al pads.
55*	FW_Cu	395	C	95;0	-	Metal fuse window.
56	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL
53*	FW_AP	30A	C	95;20	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL for flip chip.
53*	FW_AP	30A	C	95;20	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL
53	FW_Cu	395	C	95;0	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

51	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
52	AP-MD	309	D	42	-	AP RDL for flip chip.
53	FW_Cu	395	C	95;0	-	Metal fuse window.
54	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

**Table 3.1.5 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN85LP**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.2V/2.5V:</b> OD_25, NW, NT_N <b>1.2V/3.3V:</b> OD_33, NW, NT_N	1.2V P-Well.
4*	VTH_N	128	C	67	-	1.2V high Vt NMOS implantation.
5*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
6#	PW2V	193	C	Derived	<b>2V/2.5V:</b> OD_25, NW, NT_N <b>1.2V/3.3V:</b> OD_33, NW, NT_N	2.5V, or 3.3V P-Well.
7#	NW1V	192	C	Derived	NW, NT_N	1.2V N-Well.
8*	VTH_P	127	C	68	-	1.2V high Vt PMOS implantation.
9#	NW2V	194	C	Derived	<b>1.2V/2.5V:</b> NW, OD_25, NT_N <b>1.2V/3.3V:</b> NW, OD_33, NT_N	2.5V, or 3.3V N-Well.
10	OD2	132	D	41	<b>1.2V/2.5V:</b> OD_25	2.5V, or 3.3V thick oxide.
				15	<b>1.2V/3.3V:</b> OD_33	
11	NP	198	C	Derived	NP, SRM, POFUSE	Pre-doped N+ poly. (Dual use layer)
12	PO	130	D	Derived	<b>1.2V/2.5V:</b> PO, OD, OD_25, NP, PP, PSPO, SRM, DPO <b>1.2V/3.3V:</b> PO, OD, OD_33, NP, PP, PSPO, SRM, DPO	Poly-Si.
13#	N2V	116	C	Derived	<b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR <b>1.2V/3.3V:</b> NP, NW, OD_33, RH, VAR	2.5V, or 3.3V NLDD implantation.
14#	N1V	114	C	Derived	<b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR, N1V <b>1.2V/3.3V:</b> NP, NW, OD_33, RH, VAR, N1V	1.2V NLDD implantation.
15#	ULVT_N	11R	D	Derived	<b>1.2V/2.5V:</b> OD_25, NW, UVTL_N, RH, VAR <b>1.2V/3.3V:</b> OD_33, NW, UVTL_N, RH, VAR	1.2V Ultra low Vt NMOS implantation.
16#	P2V	115	C	Derived	<b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR <b>1.2V/3.3V:</b> PP, NW, OD_33, RH, VAR	2.5V, or 3.3V PLDD implantation.
17#	P1V	113	C	Derived	<b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR, P1V <b>1.2V/3.3V:</b> PP, NW, OD_33, RH, VAR, P1V	1.2V PLDD implantation.
18	UVTL_P	11Q	C	Derived	<b>1.2V/2.5V:</b> OD_25, NW, UVTL_P, RH, VAR <b>1.2V/3.3V:</b> OD_33, NW, UVTL_P, RH, VAR	1.2V Ultra low Vt PMOS implantation.
19	NP	198	C	Derived	NP, SRM	N+ implantation. (Dual use layer)
20	PP	197	C	25	-	P+ implantation.
21*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
22	RPO	155	D	29	-	Silicide protection.
23	CO	156	C	30	-	Contact window from M1 to OD or PO.
24	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
25	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
26	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
27	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
28	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
29	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.
30	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
31	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
32	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
33	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
34	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
35	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
36	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
37	VIA7	377	C	57	-	Via7 hole between M8 and M7.
38	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
39	VIA8	372	C	58	-	Via8 hole between M9 and M8.
40	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

41	CB	107	C	43	-	Bonding pad.
42#	AP	307	D	Derived	CB	Al pads.
43*	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

41*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
42*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
43	CBD	107	C	169	-	Passivation opening on bump pads.
44	AP	307	D	42	-	Al pads.
45*	FW_Cu	395	C	95;0	-	Metal fuse window.
46	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL
43*	FW_AP	30A	C	95;20	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL for flip chip.
43*	FW_AP	30A	C	95;20	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL
43	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL for flip chip.
43	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

Table 3.1.6 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN80GC

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, SRM, NP, DPSRM, SRAMDMY_PE, PP, PO, CO, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.0V/2.5V:</b> OD_25, NW, NT_N, SRM <b>1.0V/3.3V:</b> OD_33, NW, NT_N, SRM	1.0 V P-Well.
4	VTL_N	118	C	Derived	<b>1.0V/2.5V:</b> OD_25, NW, VTL_N, SRM, NT_N, RH, VAR <b>1.0V/3.3V:</b> OD_33, NW, VTL_N, SRM, NT_N, RH, VAR	1.0V low Vt NMOS implantation.
5*	VTH_N	128	C	67		1.0V high Vt NMOS implantation.
6*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
7#	PW2V	193	C	Derived	<b>1.0V/2.5V:</b> OD_25, NW, NT_N, SRM <b>1.0V/3.3V:</b> OD_33, NW, NT_N, SRM	2.5V or 3.3V P-Well.
8#	NW1V	192	C	Derived	NW, NT_N, SRM	1.0V N-Well.
9	VTH_P	127	C	68	-	1.0V high Vt PMOS implantation.
10#	NW2V	194	C	Derived	<b>1.0V/2.5V:</b> NW, OD_25, NT_N, SRM <b>1.0V/3.3V:</b> NW, OD_33, NT_N, SRM	2.5V or 3.3V N-Well.
11	OD2 (DGO)	132	D	41,15	<b>1.0V/3.3V:</b> OD_25 <b>1.0V/3.3V:</b> OD_33	2.5V or 3.3V thick oxide.
12	NP	198	C	Derived	NP, SRM	Pre-doped N+ poly. (Dual use layer)
13	PO	130	D	Derived	<b>1.0V/2.5V:</b> PO, OD, OD_25, NP, PP, SRM, SRAMDMY_PE, DPSRM, DPO <b>1.0V/3.3V:</b> PO, OD, OD_33, NP, PP, SRM, SRAMDMY_PE, DPSRM, DPO	Poly-Si.
14#	N2V	116	C	Derived	<b>1.0V/2.5V:</b> NP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> NP, NW, OD_33, RH, VAR	2.5V or 3.3V NLDD implantation.
15#	N1V	114	C	Derived	<b>1.0V/2.5V:</b> NP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> NP, NW, OD_33, RH, VAR	1.0V NLDD implantation.
16#	P2V	115	C	Derived	<b>1.0V 2.5V:</b> PP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> PP, NW, OD_33, RH, VAR	2.5V or 3.3V PLDD implantation.
17#	P1V	113	C	Derived	<b>1.0V/2.5V:</b> PP, NW, OD_25, RH, VAR <b>1.0V/3.3V:</b> PP, NW, OD_33, RH, VAR	1.0V PLDD implantation.
18	VTL_P	117	C	Derived	<b>1.0V/2.5V:</b> OD_25, NW, VTL_P, SRM, RH, VAR <b>1.0V/3.3V:</b> OD_33, NW, VTL_P, SRM, RH, VAR	1.0V low Vt PMOS implantation.
19	NP	198	C	Derived	NP, SRM	N+ implantation. (Dual use layer)

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
20	PP	197	C	25	-	P+ implantation.
21*	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
22	RPO	155	D	29	-	Silicide protection.
23	CO	156	C	Derived	CO, SEALRING, PMDMY, FW, SRM, NP, NW, OD	Contact window from M1 to OD or PO.
24	M1	360	C	Derived	M1, DM1_O, DM1	1 <sup>st</sup> metal for interconnection.
25	VIA1	378	C	Derived	VIA1, SEALRING, PMDMY, FW	Via1 hole between M2 and M1.
26	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
27	VIA2	379	C	Derived	VIA2, SEALRING, PMDMY, FW	Via2 hole between M3 and M2.
28	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
29	VIA3	373	C	Derived	VIA3, SEALRING, PMDMY, FW	Via3 hole between M4 and M3.
30	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
31	VIA4	374	C	Derived	VIA4, SEALRING, PMDMY, FW	Via4 hole between M5 and M4.
32	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
33	VIA5	375	C	Derived	VIA5, SEALRING, PMDMY, FW	Via5 hole between M6 and M5.
34	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
35	VIA6	376	C	Derived	VIA6, SEALRING, PMDMY, FW	Via6 hole between M7 and M6.
36	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
37	VIA7	377	C	Derived	VIA7, SEALRING, PMDMY, FW	Via7 hole between M8 and M7.
38	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
39	VIA8	372	C	Derived	VIA8, SEALRING, PMDMY, FW	Via8 hole between M9 and M8.
40	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

41	CB	107	C	43	-	Bonding pad.
42#	AP	307	D	Derived	CB	Al pads.
43*	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

41*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
42*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
43	CBD	107	C	169	-	Passivation opening on bump pads.
44	AP	307	D	42	-	Al pads.
45*	FW_Cu	395	C	95;0	-	Metal fuse window.
46	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL
43*	FW_AP	30A	C	95;20	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL for flip chip.
43*	FW_AP	30A	C	95;20	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL
43	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

41	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
42	AP-MD	309	D	42	-	AP RDL for flip chip.
43	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

Table 3.1.7 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN80GT

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, SRM, NP, DPSRM, SRAMDMY_PE, PP, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.2V/1.8V:</b> OD_18, NW, NT_N, SRM <b>1.2V/2.5V:</b> OD_25, NW, NT_N, SRM	1.2V P-Well.
4*	VTH_N	128	C	Derived	VTH_N, SRM, NW	1.2V high Vt NMOS implantation.
5#	VTC_N	112	C	Derived	SRM, NW, SRM	SRAM cell NMOS Vt.
6#	PW2V	193	C	Derived	<b>1.2V/1.8V:</b> OD_18, NW, NT_N, SRM <b>1.2V/2.5V:</b> OD_25, NW, NT_N, SRM	1.8V or 2.5V P-Well.
7#	NW1V	192	C	Derived	NW, NT_N, SRM	1.2V N-Well.
8#	NW2V	194	C	Derived	<b>1.2V/1.8V:</b> NW, OD_18, NT_N, SRM <b>1.2V/2.5V:</b> NW, OD_25, NT_N, SRM	1.8V or 2.5V N-Well.
9	OD2 (DGO)	132	D	16, 41	<b>1.2V/1.8V:</b> OD_18 <b>1.2V/2.5V:</b> OD_25	1.8V or 2.5V thick oxide.
10	NP	198	C	26	NP, SRM	Pre-doped N+ poly. (Dual use layer)
11	PO	130	D	Derived	<b>1.2V/1.8V:</b> PO, OD, OD_18, NP, SRAMDMY_PP, SRM, DPO <b>1.2V/2.5V:</b> PO, OD, OD_25, NP, SRAMDMY_PE, DPSRM, PP, SRM, DPO	Poly-Si.
12#	N2V	116	C	Derived	<b>1.2V/1.8V:</b> NP, NW, OD_18, RH, VAR <b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR	1.8V or 2.5V NLDD implantation.
13#	N1V	114	C	Derived	<b>1.2V/1.8V:</b> NP, NW, OD_18, RH, VAR <b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR	1.2V NLDD implantation.
14#	P2V	115	C	Derived	<b>1.2V/1.8V:</b> PP, NW, OD_18, RH, VAR <b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR	1.8V or 2.5V PLDD implantation.
15*	VTH_P	125	C	Derived	VTH_P, SRM, NW	1.2V high Vt PMOS implantation.
16#	P1V	113	C	Derived	<b>1.2V/1.8V:</b> PP, NW, OD_18, RH, VAR <b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR	1.2V PLDD implantation.
17	NP	198	C	Derived	NP, SRM	N+ implantation. (Dual use layer)
18	PP	197	C	25	-	P+ implantation.
19#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
20	RPO	155	D	29	-	Silicide protection.
21	CO	156	C	Derived	CO, SEALRING, PMDMY, FW, SRM, NP, NW, OD	Contact window from M1 to OD or PO.
22	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
23	VIA1	378	C	Derived	VIA1, SEALRING, PMDMY, FW,	Via1 hole between M2 and M1.
24	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
25	VIA2	379	C	Derived	VIA2, SEALRING, PMDMY, FW,	Via2 hole between M3 and M2.
26	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
27	VIA3	373	C	Derived	VIA3, SEALRING, PMDMY, FW,	Via3 hole between M4 and M3.
28	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
29	VIA4	374	C	Derived	VIA4, SEALRING, PMDMY, FW,	Via4 hole between M5 and M4.
30	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
31	VIA5	375	C	Derived	VIA5, SEALRING, PMDMY, FW,	Via5 hole between M6 and M5.
32	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
33	VIA6	376	C	Derived	VIA6, SEALRING, PMDMY, FW,	Via6 hole between M7 and M6.
34	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
35	VIA7	377	C	Derived	VIA7, SEALRING, PMDMY, FW,	Via7 hole between M8 and M7.
36	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
37	VIA8	372	C	Derived	VIA8, SEALRING, PMDMY, FW,	Via8 hole between M9 and M8.
38	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

39	CB	107	C	43	-	Bonding pad.
40#	AP	307	D	Derived	CB	Al pads.
41*	FW_Cu	395	C	95;0	-	Metal fuse window.
42	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

39*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
40*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
41	CBD	107	C	169	-	Passivation opening on bump pads.
42	AP	307	D	42	-	Al pads.
43*	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL
41*	FW_AP	30A	C	95;20	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL for flip chip.
41*	FW_AP	30A	C	95;20	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL
41	FW_Cu	395	C	95;0	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL for flip chip.
41	FW_Cu	395	C	95;0	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

Table 3.1.8 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN80HS

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, SRM, SRAMDMY_PE, NW, NP, DPSRM, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.05V/1.8V:</b> OD_18, NW, NT_N, SRM <b>1.05V/2.5V:</b> OD_25, NW, NT_N, SRM	1.05V P-Well.
4*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
5#	PW2V	193	C	Derived	<b>1.05V/1.8V:</b> OD_18, NW, NT_N, SRM <b>1.05V/2.5V:</b> OD_25, NW, NT_N, SRM	1.8V or 2.5V P-Well.
6#	NW1V	192	C	Derived	NW, NT_N, SRM	1.05V and 1.8V N-Well.
7#	NW2V	194	C	Derived	<b>1.05V/1.8V:</b> NW, OD_18, NT_N, SRM <b>1.05V/2.5V:</b> NW, OD_25, NT_N, SRM	1.8V or 2.5V N-Well.
8*	OD_DECAP	135	C	118	-	Decoupling capacitor device region
9	OD2 (DGO)	132	D	16, 41	<b>1.05V/1.8V:</b> OD_18 <b>1.05V/2.5V:</b> OD_25	1.8V or 2.5V thick oxide.
10	NP	198	C	Derived	NP, SRM	Pre-doped N+ poly. (Dual use layer)
11	PO	130	D	Derived	<b>1.05V/1.8V:</b> PO, OD, OD_18, NP, PP, SRM, SRAMDMY_PE, DPSRM, DPO <b>1.05V/2.5V:</b> PO, OD, OD_25, NP, PP, SRM, SRAMDMY_PE, DPSRM, DPO	Poly-Si.
12#	N2V	116	C	Derived	<b>1.05V/1.8V:</b> NP, NW, OD_18, RH, VAR <b>1.05V/2.5V:</b> NP, NW, OD_25, RH, VAR	1.8V or 2.5V NLDD implantation.
13*	VTH_N	126	C	Derived	VTH_N, SRM, NW	1.05V high Vt NMOS implantation.
14#	N1V	114	C	Derived	<b>1.05V/1.8V:</b> NP, NW, OD_18, RH, VAR <b>1.05V/2.5V:</b> NP, NW, OD_25, RH, VAR	1.05V NLDD implantation.
15*	VTL_N	118	C	Derived	<b>1.05V/1.8V:</b> VTL_N, OD_18, NW, RH, VAR <b>1.05V/2.5V:</b> VTL_N, OD_25, NW, RH, VAR	1.05V Low Vt NMOS implant
16#	P2V	115	C	Derived	<b>1.05V/1.8V:</b> PP, NW, OD_18, RH, VAR <b>1.05V/2.5V:</b> PP, NW, OD_25, RH, VAR	1.8V or 2.5V PLDD implantation.
17*	VTH_P	125	C	Derived	VTH_P, SRM, NW	1.05V high Vt PMOS implantation.
18#	P1V	113	C	Derived	<b>1.05V/1.8V:</b> PP, NW, OD_18, RH, VAR <b>1.05V/2.5V:</b> PP, NW, OD_25, RH, VAR	1.05V PLDD implantation.
19*	VTL_P	117	C	Derived	<b>1.05V/1.8V:</b> VTL_P, OD_18, NW, RH, VAR <b>1.05V/2.5V:</b> VTL_P, OD_25, NW, RH, VAR	1.05V Low Vt PMOS implant
20	NP	198	C	Derived	NP, SRM	N+ implantation. (Dual use layer)
21	PP	197	C	25	-	P+ implantation.
22*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
23	RPO	155	D	29	-	Silicide protection.
24	CO	156	C	Derived	CO, SEALRING, PMDMY, FW, SRM, NP, NW, OD	Contact window from M1 to OD or PO.
25	M1	360	C	Derived	M1, DM1	1st metal for interconnection.
26	VIA1	378	C	Derived	VIA1, SEALRING, PMDMY, FW,	Via1 hole between M2 and M1.
27	M2	380	C	Derived	M2, DM2	2nd metal for interconnection.
28	VIA2	379	C	Derived	VIA2, SEALRING, PMDMY, FW,	Via2 hole between M3 and M2.
29	M3	381	C	Derived	M3, DM3	3rd metal for interconnection.
30	VIA3	373	C	Derived	VIA3, SEALRING, PMDMY, FW,	Via3 hole between M4 and M3.
31	M4	384	C	Derived	M4, DM4	4th metal for interconnection.
32	VIA4	374	C	Derived	VIA4, SEALRING, PMDMY, FW,	Via4 hole between M5 and M4.
33	M5	385	C	Derived	M5, DM5	5th metal for interconnection.
34	VIA5	375	C	Derived	VIA5, SEALRING, PMDMY, FW,	Via5 hole between M6 and M5.
35	M6	386	C	Derived	M6, DM6	6th metal for interconnection.
36	VIA6	376	C	Derived	VIA6, SEALRING, PMDMY, FW,	Via6 hole between M7 and M6.
37	M7	387	C	Derived	M7, DM7	7th metal for interconnection.
38	VIA7	377	C	Derived	VIA7, SEALRING, PMDMY, FW,	Via7 hole between M8 and M7.
39	M8	388	C	Derived	M8, DM8	8th metal for interconnection.
40	VIA8	372	C	Derived	VIA8, SEALRING, PMDMY, FW,	Via8 hole between M9 and M8.
41	M9	389	C	Derived	M9, DM9	9th metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

42	CB	107	C	43	-	Bonding pad.
43#	AP	307	D	Derived	CB	Al pads.
44*	FW_Cu	395	C	95;0	-	Metal fuse window.
45	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

42*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
43*	MD	383	C	Derived	MD, DMD	Metal (Mn+1) for redistribution interconnection.
44	CBD	107	C	169	-	Passivation opening on bump pads.
45	AP	307	D	42	-	Al pads.
46*	FW_Cu	395	C	95;0	-	Metal fuse window.
47	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

42	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
43	AP-MD	309	D	42	-	AP RDL
44*	FW_AP	30A	C	95;20	-	Metal fuse window.
45	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

42	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
43	AP-MD	309	D	42	-	AP RDL for flip chip.
44*	FW_AP	30A	C	95;20	-	Metal fuse window.
45	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

42	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
43	AP-MD	309	D	42	-	AP RDL
44	FW_Cu	395	C	95;0	-	Metal fuse window.
45	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

42	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
43	AP-MD	309	D	42	-	AP RDL for flip chip.
44	FW_Cu	395	C	95;0	-	Metal fuse window.
45	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

**Table 3.1.9 Mask Name and ID, Key Process Sequence, and CAD Layer for CLN80LP**

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	OD	120	D	Derived	OD, SRM, PO, CO, DPSRM, SRAMDMY_PE, DOD	Thin oxide for device, and interconnection.
2*	DNW	119	C	1	-	Deep N-Well.
3#	PW1V	191	D	Derived	<b>1.2V/2.5V:</b> OD_25, NW	1.2 V P-Well.
4*	VTH_N	128	C	67	-	1.2V high Vt NMOS implantation.
5*#	VTC_N	112	C	Derived	SRM, NW	SRAM cell NMOS Vt.
6#	PW2V	193	C	Derived	<b>1.2V/2.5V:</b> OD_25, NW	2.5V P-Well.
7#	NW1V	192	C	Derived	NW	1.2V N-Well.
8	VTH_P	127	C	68	-	1.2V high Vt PMOS implantation.
9#	NW2V	194	C	Derived	<b>1.2V/2.5V:</b> NW, OD_25	2.5V N-Well.
10	OD2 (DGO)	132	D	41	<b>1.2V/2.5V:</b> OD_25	2.5V thick oxide.
11	NP	198	C	Derived	NP, SRM	Pre-doped N+ poly. (Dual use layer)
12	PO	130	D	Derived	<b>1.2V/2.5V:</b> PO, OD, OD_25, NP, PP, SRM, DPO	Poly-Si.
13#	N2V	116	C	Derived	<b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR	2.5V NLDD implantation.
14#	N1V	114	C	Derived	<b>1.2V/2.5V:</b> NP, NW, OD_25, RH, VAR	1.2V NLDD implantation.
15#	P2V	115	C	Derived	<b>1.2V or 2.5V:</b> PP, NW, OD_25, RH, VAR	2.5V PLDD implantation.
16#	P1V	113	C	Derived	<b>1.2V/2.5V:</b> PP, NW, OD_25, RH, VAR	1.2V PLDD implantation.
17	NP	198	C	Derived	NP, SRM	N+ implantation. (Dual use layer)
18	PP	197	C	25	-	P+ implantation.
19*#	ESD	111	C	Derived	OD, NP, RPO, NW, PO, ESD3	ESD implantation.
20	RPO	155	D	29	-	Silicide protection.
21	CO	156	C	Derived	CO, SEALRING, PMDMY, FW, SRM, NP, NW	Contact window from M1 to OD or PO.
22	M1	360	C	Derived	M1, DM1_O, DM1	1 <sup>st</sup> metal for interconnection.
23	VIA1	378	C	Derived	VIA1, SEALRING, PMDMY, FW,	Via1 hole between M2 and M1.
24	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
25	VIA2	379	C	Derived	VIA2, SEALRING, PMDMY, FW,	Via2 hole between M3 and M2.
26	M3	381	C	Derived	M3, DM3_O, DM3	3 <sup>rd</sup> metal for interconnection.
27	VIA3	373	C	Derived	VIA3, SEALRING, PMDMY, FW,	Via3 hole between M4 and M3.
28	M4	384	C	Derived	M4, DM4_O, DM4	4 <sup>th</sup> metal for interconnection.
29	VIA4	374	C	Derived	VIA4, SEALRING, PMDMY, FW,	Via4 hole between M5 and M4.
30	M5	385	C	Derived	M5, DM5_O, DM5	5 <sup>th</sup> metal for interconnection.
31	VIA5	375	C	Derived	VIA5, SEALRING, PMDMY, FW,	Via5 hole between M6 and M5.
32	M6	386	C	Derived	M6, DM6_O, DM6	6 <sup>th</sup> metal for interconnection.
33	VIA6	376	C	Derived	VIA6, SEALRING, PMDMY, FW,	Via6 hole between M7 and M6.
34	M7	387	C	Derived	M7, DM7_O, DM7	7 <sup>th</sup> metal for interconnection.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
35	VIA7	377	C	Derived	VIA7, SEALRING, PMDMY, FW,	Via7 hole between M8 and M7.
36	M8	388	C	Derived	M8, DM8	8 <sup>th</sup> metal for interconnection.
37	VIA8	372	C	Derived	VIA8, SEALRING, PMDMY, FW,	Via8 hole between M9 and M8.
38	M9	389	C	Derived	M9, DM9	9 <sup>th</sup> metal for interconnection.

## FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

39	CB	107	C	43	-	Bonding pad.
40#	AP	307	D	Derived	CB	Al pads.
41*	FW_Cu	395	C	95;0	-	Metal fuse window.
42	CB	107	C	43	-	Bonding pad.

## FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

39*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
40*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
41	CBD	107	C	169	-	Passivation opening on bump pads.
42	AP	307	D	42	-	Al pads.
43*	FW_Cu	395	C	95;0	-	Metal fuse window.
44	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL
41*	FW_AP	30A	C	95;20	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL for flip chip.
41*	FW_AP	30A	C	95;20	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL
41	FW_Cu	395	C	95;0	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

39	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
40	AP-MD	309	D	42	-	AP RDL for flip chip.
41	FW_Cu	395	C	95;0	-	Metal fuse window.
42	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

**Table 3.1.10 Mask Name and ID, Key Process Sequence, and CAD Layer for CMN90**

- The following tables provide the N90 backend process mask sequence with additional information regarding CTM/CBM or Mu mask.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
2	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
3	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
4	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
5	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
6	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.
7	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
8	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
9	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
10	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
11	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
12	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
13	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
14	VIA7	377	C	57	-	Via7 hole between M8 and M7.
15	CTM®	182	D	77	-	MiM capacitor top metal plate
16	CBM®	183	D	88	-	MiM capacitor bottom metal plate
17	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
18	VIA8	372	C	58	-	Via8 hole between M9 and M8.
19	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.
				Derived	UTM, DUTM	Ultra thick metal for inductor/interconnection.

FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

20	CB	107	C	43	-	Bonding pad.
21#	AP	307	D	Derived	CB	Al pads.
22*	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB	107	C	43	-	Bonding pad.

FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

20*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
21*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
22	CBD	107	C	169	-	Passivation opening on bump pads.
23	AP	307	D	42	-	Al pads.
24*	FW_Cu	395	C	95;0	-	Metal fuse window.
25	CBD	107	C	169	-	Passivation opening on bump pads.

FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL
22*	FW_AP	30A	C	95;20	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL for flip chip.
22*	FW_AP	30A	C	95;20	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL
22	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL for flip chip.
22	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

Note: The mark “@“ is for CTM/CBM placement and can refer to Table 2.5.5, 2.5.6 and 2.5.7

**Table 3.1.11 Mask Name and ID, Key Process Sequence, and CAD Layer for CMN85**

- The following tables provide the N85 backend process mask sequence with additional information regarding CTM/CBM or Mu mask.

Key Process Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Description
1	M1	360	C	Derived	M1, DM1_O, DM1	1 <sup>st</sup> metal for interconnection.
2	VIA1	378	C	Derived	VIA1, SEALRING	Via1 hole between M2 and M1.
3	M2	380	C	Derived	M2, DM2_O, DM2	2 <sup>nd</sup> metal for interconnection.
4	VIA2	379	C	Derived	VIA2, SEALRING	Via2 hole between M3 and M2.
5	M3	381	C	Derived	M3, DM3_O, DM3	3 <sup>rd</sup> metal for interconnection.
6	VIA3	373	C	Derived	VIA3, SEALRING	Via3 hole between M4 and M3.
7	M4	384	C	Derived	M4, DM4_O, DM4	4 <sup>th</sup> metal for interconnection.
8	VIA4	374	C	Derived	VIA4, SEALRING	Via4 hole between M5 and M4.
9	M5	385	C	Derived	M5, DM5_O, DM5	5 <sup>th</sup> metal for interconnection.
10	VIA5	375	C	Derived	VIA5, SEALRING	Via5 hole between M6 and M5.
11	M6	386	C	Derived	M6, DM6_O, DM6	6 <sup>th</sup> metal for interconnection.
12	VIA6	376	C	Derived	VIA6, SEALRING	Via6 hole between M7 and M6.
13	M7	387	C	Derived	M7, DM7_O, DM7	7 <sup>th</sup> metal for interconnection.
14	VIA7	377	C	57	-	Via7 hole between M8 and M7.
15	CTM <sup>®</sup>	182	D	77	-	MiM capacitor top metal plate
16	CBM <sup>®</sup>	183	D	88	-	MiM capacitor bottom metal plate
17	M8	388	C	Derived	M8, DM8_O, DM8	8 <sup>th</sup> metal for interconnection.
18	VIA8	372	C	58	-	Via8 hole between M9 and M8.
19	M9	389	C	Derived	M9, DM9_O, DM9	9 <sup>th</sup> metal for interconnection.
				Derived	UTM, DUTM	Ultra thick metal for inductor/interconnection.

FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

20	CB	107	C	43	-	Bonding pad.
21#	AP	307	D	Derived	CB	Al pads.
22*	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB	107	C	43	-	Bonding pad.

FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

20*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
21*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
22	CBD	107	C	169	-	Passivation opening on bump pads.
23	AP	307	D	42	-	Al pads.
24*	FW_Cu	395	C	95;0	-	Metal fuse window.
25	CBD	107	C	169	-	Passivation opening on bump pads.

FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL
22*	FW_AP	30A	C	95;20	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL for flip chip.
22*	FW_AP	30A	C	95;20	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL
22	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL for flip chip.
22	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

Note: The mark “@“ is for CTM/CBM placement and can refer to Table 2.5.5, 2.5.6 and 2.5.7

**Table 3.1.12 Mask Name and ID, Key Process Sequence, and CAD Layer for CMN80**

- The following tables provide the N80 backend process mask sequence with additional information regarding CTM/CBM or Mu mask.

<b>Key Process Sequence</b>	<b>Mask Name</b>	<b>Mask ID</b>	<b>Digitized Area (Dark or Clear)</b>	<b>CAD Layer</b>	<b>Reference Layer in Logical Operation</b>	<b>Description</b>
1	M1	360	C	Derived	M1, DM1_O, DM1	1st metal for interconnection.
2	VIA1	378	C	Derived	VIA1, SEALRING, PMDMY, FW,	Via1 hole between M2 and M1.
3	M2	380	C	Derived	M2, DM2_O, DM2	2nd metal for interconnection.
4	VIA2	379	C	Derived	VIA2, SEALRING, PMDMY, FW,	Via2 hole between M3 and M2.
5	M3	381	C	Derived	M3, DM3_O, DM3	3rd metal for interconnection.
6	VIA3	373	C	Derived	VIA3, SEALRING, PMDMY, FW,	Via3 hole between M4 and M3.
7	M4	384	C	Derived	M4, DM4_O, DM4	4th metal for interconnection.
8	VIA4	374	C	Derived	VIA4, SEALRING, PMDMY, FW,	Via4 hole between M5 and M4.
9	M5	385	C	Derived	M5, DM5_O, DM5	5th metal for interconnection.
10	VIA5	375	C	Derived	VIA5, SEALRING, PMDMY, FW,	Via5 hole between M6 and M5.
11	M6	386	C	Derived	M6, DM6_O, DM6	6th metal for interconnection.
12	VIA6	376	C	Derived	VIA6, SEALRING, PMDMY, FW,	Via6 hole between M7 and M6.
13	M7	387	C	Derived	M7, DM7_O, DM7	7th metal for interconnection.
14	VIA7	377	C	57	VIA7, SEALRING, PMDMY, FW,	Via7 hole between M8 and M7.
15	CTM®	182	D	77	-	MiM capacitor top metal plate
16	CBM®	183	D	88	-	MiM capacitor bottom metal plate
17	M8	388	C	Derived	M8, DM8_O, DM8	8th metal for interconnection.
18	VIA8	372	C	58	VIA8, SEALRING, PMDMY, FW,	Via8 hole between M9 and M8.
19	M9	389	C	Derived	M9, DM9_O, DM9	9th metal for interconnection.
				Derived	UTM, DUTM	Ultra thick metal for inductor/interconnection.

FBEOL option1: Wire bond without {AP Fuse or AP RDL (AP-MD)}

20	CB	107	C	43	-	Bonding pad.
21#	AP	307	D	Derived	CB	Al pads.
22*	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB	107	C	43	-	Bonding pad.

FBEOL option2: Flip chip without {AP Fuse or AP RDL (AP-MD)}

20*	VIAD	371	C	167	-	Via hole (VIAn) to connect Mn and MD for redistribution.
21*	MD	383	C	Derived	MD, DMD_O, DMD	Metal (Mn+1) for redistribution interconnection.
22	CBD	107	C	169	-	Passivation opening on bump pads.
23	AP	307	D	42	-	Al pads.
24*	FW_Cu	395	C	95;0	-	Metal fuse window.
25	CBD	107	C	169	-	Passivation opening on bump pads.

## FBEOL option3: Wire bond with {AP Fuse or AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	RV, CB, FW_AP	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL
22*	FW_AP	30A	C	95;20	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option4: Flip chip with {AP Fuse or AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	RV, CBD, FW_AP	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL for flip chip.
22*	FW_AP	30A	C	95;20	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option5: Wire bond with {Cu Fuse and AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	CB, RV	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL
22	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

## FBEOL option6: Flip chip with {Cu Fuse and AP RDL (AP-MD)}

20	CB-VD	306	C	Derived	CBD, RV	Passivation via hole between Mn and AP-MD.
21	AP-MD	309	D	42	-	AP RDL for flip chip.
22	FW_Cu	395	C	95;0	-	Metal fuse window.
23	CB2	308	C	86	-	Passivation-2 opening for flip chip with AP RDL

Note: The mark “@“ is for CTM/CBM placement and can refer to Table 2.5.8 and 2.5.9

Table 3.1.13 Mask Name/ ID/ Grade/ Type, OPC, and PSM

Mask Name	Mask ID	Mask Grade	Mask Type	OPC	PSM	Non-design level mask
OD	120	J	ASF	A	B	
DNW	119	E	DSF	B	B	
PW1V	191	G	DSF	B	B	Yes
VTH_N	128	G	DSF	A	B	
VTC_N	112	G	DSF	B	B	Yes
PW2V	193	G	DSF	B	B	Yes
NW1V	192	G	DSF	B	B	Yes
VTH_P	127	G	DSF	A	B	
NW2V	194	G	DSF	B	B	Yes
OD2	132	D	DSF	B	B	
OD3	131	D	DSF	B	B	
NP	198	G	DSF	A	B	
PO	130	J	ASF	A	C	
N2V	116	G	DSF	A	B	Yes
VTH_N	126	G	DSF	A	B	
N1V	114	G	DSF	A	B	Yes
VTL_N	118	G	DSF	A	B	
N3V (TGO)	158	G	DSF	A	B	Yes
P2V (DGO)	115	G	DSF	A	B	Yes
P2V (TGO)	115	G	DSF	A	B	Yes
P3V (TGO)	157	G	DSF	A	B	Yes
VTH_P	125	G	DSF	A	B	
P1V	113	G	DSF	A	B	Yes
VTL_P	117	G	DSF	A	B	
NP	198	G	DSF	A	B	
PP	197	G	DSF	A	B	
ESD	111	D	DSF	B	B	Yes
RPO	155	E	DSF	B	B	
CO	156	J	ASF	A	C	
M1	360	J	ASF	A	B	
VIA1	378	I (N90/N85)	DSF	A	C	
		J (N80)	ASF	A	C	
M2	380	I	DSF	A	B	
VIA2	379	I (N90/N85)	DSF	A	C	
		J (N80)	ASF	A	C	
M3	381	I	DSF	A	B	
VIA3	373	I (N90/N85)	DSF	A	C	
		J (N80)	ASF	A	C	
M4	384	I	DSF	A	B	
VIA4	374	I (N90/N85)	DSF	A	C	
		J (N80)	ASF	A	C	
M5	385	I	DSF	A	B	
VIA5	375	I (N90/N85)	DSF	A	C	
		J (N80)	ASF	A	C	
M6	386	I	DSF	A	B	
VIA6	376	I (N90/N85)	DSF	A	C	
		J (N80)	ASF	A	C	
M7	387	I	DSF	A	B	
VIA7 (3XTM)	377	F	DSF	B	B	
CTM	182	G	DSF	B	B	
CBM	183	E	DSF	B	B	
M8 (3XTM)	388	F	DSF	B	B	
VIA8 (3XTM)	372	F	DSF	B	B	
M9 (3XTM)	389	F	DSF	B	B	

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Mask Name	Mask ID	Mask Grade	Mask Type	OPC	PSM	Non-design level mask
VIAD (3XTM)	371	F	DSF	B	B	
MD (3XTM)	383	F	DSF	B	B	
VIA7(2XTM)	377	F	DSF	B	B	
M8 (2XTM)	388	G	DSF	A	B	
VIA8 (2XTM)	372	F	DSF	B	B	
M9 (2XTM)	389	G	DSF	A	B	
VIAD (2XTM)	371	F	DSF	B	B	
MD (2XTM)	383	G	DSF	A	B	
CB	107	A	DSF	B	B	
CBD	107	A	DSF	B	B	
AP	307	A	DSF	B	B	Yes
FW_Cu	395	A	DSF	B	B	
FW_AP	30A	A	DSF	B	B	
CB-VD	306	D	DSF	B	B	
AP-MD	309	D	DSF	B	B	
CB2	308	A	DSF	B	B	

Category	Abbreviation	Description
Mask type:	DSF	DUV scanner
	ASF	193nm scanner
OPC:	B	Non-OPC (Binary)
	A	OPC
PSM:	B	Non-PSM (Binary)
	C	PSM

## 3.2 Dummy Pattern Fill CAD Layers

The layers in Table 3.2.1 are for planarization (dummy fill) geometry. The CAD layer designators are specified according to the GDS *layer;datatype* format.

**Table 3.2.1 CAD Layers for Dummy Patterns**

Layer Name	CAD Layer;datatype	Layer Name	CAD Layer;datatype
DOD	6;1	-	-
DPO	17;1	-	-
DM1	31;1	DM1_O	31;7
DM2	32;1	DM2_O	32;7
DM3	33;1	DM3_O	33;7
DM4	34;1	DM4_O	34;7
DM5	35;1	DM5_O	35;7
DM6	36;1	DM6_O	36;7
DM7	37;1	DM7_O	37;7
DM8	38;1	DM8_O	38;7
DM9	39;1	DM9_O	39;7
DMD	168;1	DMD_O	168;7

In the TSMC utility, 2 kinds of dummy metal are generated, DMx and DMx\_O.

- DMx\_O: OPC dummy metal. DMx\_O is the same as real metal, Mx.
  - ◆ DMx\_O receives OPC. In the MT form, you needs to combine DMx\_O into the real metal, like (Mx OR DMx\_O).
  - ◆ DMx\_O needs to meet all Mx rules.
- The distinction between Mx, DMx, and DMx\_O

	Mx	DMx	DMx_O
GDS datatype	0	1	7
Do OPC modification on it	Yes	No	Yes
Refer to it during OPC	Yes	Yes	Yes
Follow Mx rule	Yes	No	Yes

### 3.3 Special Recognition CAD Layer Summary

Table 3.3.1 lists special layers for N90 DRC recognition or MT form purpose. If you would not follow the TSMC default CAD layer numbers, be sure that you change the layer mapping in the related deck, like DRC/LVS and so on, to be sure that the deck can work correctly. Some CAD layer designators include a GDS datatype according to the GDS *layer;datatype* format.

The column "Tape out required layer" indicates that this layer must be noted on the mask tapeout to provide information for mask making.

**Table 3.3.1 Special Layer Summary**

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
<b>General</b>					
NWDMY	114;0	NW resistor dummy layer for DRC and LVS. The NW region covered by both NWDMY and RPO layers is the "NW within OD resistor." The NW region covered by only NWDMY is the "NW under STI resistor."	NWROD and NWRSTI rules	✓	
Ncap_NTN	11;20	DRC needs NCAP_NTN to waive the NMOS capacitor with same potential. DRC also flag NCAP_NTN and OD outside of the NCAP_NTN in the same NT_N.	NT_N rules	✓	
PSPO	17;51	Recognition layer for LP low Vt device, and to generate poly logical operation in LP low Vt process.	LP Low Vt rule	✓	✓
RH	117	For OD, PO resistors	OD and PO resistor guidelines		✓
VAR	143	This layer is for MOS type varactors.	VAR rules	✓	✓
LOGO	158	LOGO and product labels layer for DRC	Logo rules	✓	
SEALRING	162	Covers the seal ring region and metal fuse protection ring region. This layer is a must for tape out of VIAx, if either you add sealring by themselves or metal fuse is used.	Seal ring rules	✓	✓
CSRDMY	166	For stress relief pattern rule check.	Chip corner rules	✓	
CDUDMY	165	Covers the CDU pattern in the 10 µm assembly isolation beside the seal ring.	CDU rule	✓	
BJTDMY	110	Cover BJT device	Analog layout rule	✓	
<b>MOM</b>					
MOMDMY_1	155;1	Dummy layer for M1 MOM region	MOM rules	✓	
MOMDMY_2	155;2	Dummy layer for M2 MOM region	MOM rules	✓	
MOMDMY_3	155;3	Dummy layer for M3 MOM region	MOM rules	✓	
MOMDMY_4	155;4	Dummy layer for M4 MOM region	MOM rules	✓	
MOMDMY_5	155;5	Dummy layer for M5 MOM region	MOM rules	✓	
MOMDMY_6	155;6	Dummy layer for M6 MOM region	MOM rules	✓	
MOMDMY_7	155;7	Dummy layer for M7 MOM region	MOM rules	✓	
MOMDMY_8	155;8	Dummy layer for M8 MOM region	MOM rules	✓	
MOMDMY_9	155;9	Dummy layer for M9 MOM region	MOM rules	✓	
MOMDMY_AP	155;20	Dummy layer for AP MOM region	MOM rules	✓	
RTMOMDMY	155;21	Dummy layer for RTMOM	PO.R.4/ PO.L.1	✓	

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
<b>MS_RF</b>					
CTMDMY	148;110	Dummy layer for defined MiM capacitor 1.0fF/um <sup>2</sup> . Its size is equal to the CBM layer size up by 10 µm per side.	CTM and CBM rule	✓	
CTMDMY	148;115	Dummy layer for defined MiM capacitor 1.5fF/um <sup>2</sup> . Its size is equal to the CBM layer size up by 10 µm per side.	CTM and CBM rule	✓	
CTMDMY	148;120	Dummy layer for defined MiM capacitor 2.0fF/um <sup>2</sup> . Its size is equal to the CBM layer size up by 10 µm per side	CTM and CBM rule	✓	
CTMDMY	148;0	Dummy layer for defined MiM capacitor region. Use for DRC. Its size is equal to the CBM layer size up by 10 µm per side	CTM and CBM rule	✓	
CTMDMY (drawing 1)	148;10	LVS dummy layer for putting BB/RF devices under 2T BB MIMCAPs.			
INDDMY	144	Dummy layer for inductor	UTM rule, dummy rule	✓	
RFDMY	161	RFDMY is a required dummy layer for LVS/DRC device recognition and SPICE simulation. RFDMY should completely cover the RF devices that require a TSMC RF model.	SBD rules	✓	
RFDMY (drawing 1)	161;10	LVS dummy layer for putting BB/RF devices under RF MIMCAPs with shielding.			
SBDDMY	113;0	A layer for DRC, LVS and creating mask logic operation. Use "SBDDMY" to fully cover schottky barrier diode.	Schottky Barrier Diode (SBD) Layout Rules	✓	✓
<b>SRAM</b>					
SRM	50	SRM is used to generate the VTC_N mask. Covers the SRAM cell array. The edge of the SRM layer should be aligned to the boundary of the SRAM cell array, which may include storage, strapping, and dummy edge cells.	SRAM rules	✓	✓
SRAMDML	186;0	SRAM DRC violation waiver layer. Layers VIA1 and below covered by this layer are DRC waived. In the TSMC DRC deck, both SRM and SRAMDML can waive SRAM DRC violations under layers VIA1 and below. If SRM is not in SRAM library, please use SRAMDML to waive SRAM DRC violations under VIA1. Before using SRAMDML, please make sure that TSMC has reviewed the SRAM library to avoid real violations that are automatically waived by the SRAMDML marker layer.		✓	
SRAMDML_PE	186;1	Cover the pass-gate transistors of SRAM cell. SRAMDML (186;1) is used to generate the OD/PO mask of CLN80GT/HS technology.	OD and PO (N80GT/N80HS)		✓
SRAMDML	186;4	SRAM periphery DRC layer can only be used in the word decoder of TSMC SRAM (0.999um <sup>2</sup> and 1.15um <sup>2</sup> ). This layer is only to waive CO.S.3 and G.1. And the SRAM must be reviewed by TSMC's R&D		✓	

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
		and PE even if you use TSMC cell.			
DPSRM	74;0	Cover Dual port SRAM cell array	OD and PO		✓
<b>ESD/Latch-up</b>					
LUPWDMY	255;1	Some design structure may fail the DRC check in LUP.1g, LUP.2g, LUP.3.1g, LUP.3.2g, LUP.3.3g, LUP.3.4g, LUP.4g, LUP.5.1g, LUP.5.2g, LUP.5.3g, LUP.5.4g. You can use LUPWDMY to waive these violations as they are silicon proven at package level. Don't use this layer before silicon proven, and consult tsmc if you have any DRC violation.	Latch up rules		
SDI	122	SDI is a required DRC dummy (marker) layer to check I/O ESD and latch-up guidelines. The SDI layer must cover all I/O MOS (OD) regions that are connected to pads.	ESD guidelines	✓	
ESD3	147	This layer is required for ESD implant mask generation.	ESD guidelines		✓
VDDDMY	255;4	Dummy Layer for Power(Vdd) PAD	Latch up rules	✓	
VSSDMY	255;5	Dummy Layer for Ground(Vss) PAD	Latch up rules	✓	
M1(pin)	131;0	Metal1 pin for text layer	Latch up rules	✓	
M2(pin)	132;0	Metal2 pin for text layer	Latch up rules	✓	
M3(pin)	133;0	Metal3 pin for text layer	Latch up rules	✓	
M4(pin)	134;0	Metal4 pin for text layer	Latch up rules	✓	
M5(pin)	135;0	Metal5 pin for text layer	Latch up rules	✓	
M6(pin)	136;0	Metal6 pin for text layer	Latch up rules	✓	
M7(pin)	137;0	Metal7 pin for text layer	Latch up rules	✓	
M8(pin)	138;0	Metal8 pin for text layer	Latch up rules	✓	
M9(pin)	139;0	Metal9 pin for text layer	Latch up rules	✓	
MD(pin)	159;0	MD pin for text layer	Latch up rules	✓	
<b>Dummy utility</b>					
ODBLK	150;20	Dummy OD exclusion marker layer	DOD rules	✓	
POBLK	150;21	Dummy PO exclusion marker layer	DPO rules	✓	
DMxEXCL	150;x	Dummy Mx exclusion marker layer	DMx rules	✓	
DMDEXCL	150;15	Dummy MD exclusion marker layer	DMx rules	✓	
<b>DFM</b>					
RRuleRequire	182;1	Dummy layer for DFM Action-Required rules	DFM Recommendation	✓	
RRuleRecommend	182;2	Dummy layer for DFM Recommended recommendation	DFM Recommendation	✓	
RRuleAnalog	182;3	Dummy layer for Analog rules, recommendations, and guidelines for Analog Designs	Chapter 5	✓	
RRuleGuideline	182;4	Dummy layer for DFM guideline check	DFM guideline	✓	
excludeRRuleRequire	182;11	DRC dummy layer for excluding DFM Action-Required recommendation check.	DFM Action-Required	✓	
excludeRRuleRecommended	182;12	DRC dummy layer for excluding DFM DFM Recommended recommendation check	DFM Recommended	✓	
excludeRRuleAnalog	182;13	DRC dummy layer for excluding DFM Recommended Dimension check for Analog Designs	Rules and Recommendations for Analog Designs	✓	
excludeRRuleGuideline	182;14	DRC dummy layer for excluding DFM guideline check	DFM guideline	✓	

Special Layer Name	TSMC Default CAD Layer	Description	Associated With	DRC	Tape out required layer
<b>FUSE</b>					
PMDMY	106	Dummy layer to cover metal fuse protection ring structure for DRC. For details, please refer to Doc.: <i>T-N90-LO-DR-003</i> (Fuse Rule).	Fuse rules	✓	
LMARK	109	This layer is for laser repair alignment mark opening. For details, please refer to Doc.: <i>T-N90-LO-DR-003</i> (Fuse Rule).	Fuse rules	✓	
POFUSE	156;0	Poly fuse implant layer, cover all poly fuse regions.			✓
<b>Pad</b>					
WBDMY	183;0	CUP pad region marker layer for N90 CUP relative rule check	CUP rules	✓	

## 3.4 Device Truth Tables

This section contains the device truth tables for:

- CLN90 Logic General Purpose (G) technology
- CLN90 Low Power (LP) technology
- CLN90 High Performance (GT) technology
- CLN85 Logic General Purpose (G) technology
- CLN85 Low Power (LP) technology
- CLN80 General Purpose Consumer Platform (GC) technology
- CLN80 High Performance (GT) technology
- CLN80 High Speed (HS) technology
- CLN80 Low Power (LP) technology
- CMN90
- CMN85
- CMN80

**Table 3.4.1 Table Legend for Device Truth Tables**

- |          |                                  |
|----------|----------------------------------|
| <b>0</b> | Does not cover the structures    |
| <b>1</b> | Covers or matches the structures |
| *        | Don't care                       |

### 3.4.1 CLN90 General Purpose (G)

Table 3.4.2

Device	SPICE Name	Design Levels												Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_33	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY
NMOS (1.0V)	nch	*	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
PMOS (1.0V)	pch	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0
High Vt NMOS (1.0V)	nch_hvt	*	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0
High Vt PMOS (1.0V)	pch_hvt	*	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0
Low Vt NMOS (1.0V)	nch_lvt	*	1	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0
Low Vt PMOS (1.0V)	pch_lvt	*	1	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0
I/O NMOS (3.3V)	nch_33	*	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0
I/O PMOS (3.3V)	pch_33	*	1	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0
1.8V I/O NMOS (DGO, TGO)	nch_18	*	1	0	0	0	0	1	1	0	0	0	0	1	0	0	0	0
1.8V I/O PMOS (DGO,TGO)	pch_18	*	1	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0
Native NMOS (1.0V)	nch_na	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (3.3V)	nch_na33	0	1	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (1.8V DGO, TGO)	nch_na18	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	*	0	0	0	0	0	1	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	*	0	0	0	0	0	0	1	0	0	0
P-Well Contact	*	1	0	0	*	*	*	*	0	0	0	0	0	0	1	0	0	0
N-Well Contact	*	1	1	0	*	*	*	*	0	0	0	0	0	1	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	0	0	1	0	0	0	0	1	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	0	0	1	0	0	0	0	0	1	0	0	0
Silicided N+ OD Resistor	rmod	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Unsilicided N+ PO Resistor	rmpolywo	*	0	*	0	0	0	0	1	0	0	0	0	1	0	1	1	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	0	1	0	0	0	0	0	1	1	1	0
Unsilicided N+ OD Resistor	modwo	*	1	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 $\mu\text{m}^2$ ) npn5 (5x5 $\mu\text{m}^2$ ) npn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	0	1	0	0	0	0	1	0	0	0	1
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	0	0	1	1	0	0	0	0	1	0	0	0	1
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	1	0	1	0	0	0	0	1	0	0	0	1
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	1	1	0	1	0	0	0	0	1	0	0	0	1

### 3.4.2 CLN90 Low Power (LP)

Table 3.4.3

Device	SPICE Name	Design Levels												Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_33	POLY	VTH_N	VTH_P	ULVT_N	ULVT_P	N+	P+	RPO	RH	NWDMY	VAR
NMOS (1.2V)	Nch	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
PMOS (1.2V)	Pch	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0
Low Vt NMOS (1.2V)	nch_lvt	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	1
Ultra Low VT NMOS (1.2V)	nch_ulvt	*	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1
Low Vt PMOS (1.2V)	pch_lvt	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	1
Ultra Low VT PMOS (1.2V)	pch_ulvt	*	1	1	0	0	0	1	0	0	0	1	0	1	0	0	0	1
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0
I/O NMOS (3.3V)	nch_33	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0
I/O PMOS (3.3V)	pch_33	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (3.3V)	nch_na33	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	0	0	1	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	0	0	1	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	0	0	1	0	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	0	1	0	0	0	0	0	1	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	0	1	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	1	1	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 um <sup>2</sup> ) pnp5 (5x5 um <sup>2</sup> ) pnp10 (10x10 um <sup>2</sup> )	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 um <sup>2</sup> ) npn5 (5x5 um <sup>2</sup> ) npn10 (10x10 um <sup>2</sup> )	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0	0
1.2V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	1	0
2.5V Varactor (NMOS Capacitor)	Nmoscap25	0	1	1	0	1	1	1	0	0	0	0	1	0	0	0	1	0
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	1	1	1	0	0	0	0	1	0	0	0	1	0

### 3.4.3 CLN90 High Performance (GT)

Table 3.4.4

Device	SPICE Name	Design Levels												Special Layers			
		DNW	OD	NW	NT_N	OD_25	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY
NMOS (1.2V)	nch	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0
PMOS (1.2V)	pch	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0
Low Vt NMOS (1.2V)	nch_lvt	*	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0
Low Vt PMOS (1.2V)	pch_lvt	*	1	1	0	0	0	1	0	0	0	1	0	1	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0
I/O NMOS (1.8V)	nch_18	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0
I/O PMOS (1.8V)	pch_18	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (1.8V)	nch_na18	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	0	0	1	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0
P-Well Contact	*	1	0	0	*	*	0	0	0	0	0	0	0	1	0	0	0
N-Well Contact	*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0
Silicided N+ OD Resistor	rnod	*	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	0	1	0	0	0	0	1	0	1	1	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	1	1	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	1
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 $\mu\text{m}^2$ ) npn5 (5x5 $\mu\text{m}^2$ ) npn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	0	0	0	1	1	1	0	0
1.2V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	1
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	1
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	0	1	0	0	0	0	1	0	0	0	1

### 3.4.4 CLN85 General Purpose (G)

Table 3.4.5

Device	SPICE Name	Design Levels												Special Layer				
		DNW	OD	NW	NT_N	OD_25	OD_33	OD_18	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY
NMOS (1.0V)	nch	*	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
PMOS (1.0V)	pch	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0
High Vt NMOS (1.0V)	nch_hvt	*	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0
High Vt PMOS (1.0V)	pch_hvt	*	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0
Low Vt NMOS (1.0V)	nch_lvt	*	1	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0
Low Vt PMOS (1.0V)	pch_lvt	*	1	1	0	0	0	0	1	0	0	0	1	0	1	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	0	1	0	0	0	0	1	0	0	0	0
I/O NMOS (3.3V)	nch_33	*	1	0	0	0	1	0	1	0	0	0	0	1	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0
I/O PMOS (3.3V)	pch_33	*	1	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0
1.8V I/O NMOS (DGO, TGO)	nch_18	*	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0
1.8V I/O PMOS (DGO,TGO)	pch_18	*	1	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0
Native NMOS (1.0V)	nch_na	0	1	0	1	0	0	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (3.3V)	nch_na33	0	1	0	1	0	1	0	1	0	0	0	0	1	0	0	0	0
Native I/O NMOS (1.8V DGO, TGO)	nch_na18	0	1	0	1	0	0	1	1	0	0	0	0	0	1	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	*	0	0	0	0	0	1	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	*	0	0	0	0	0	0	1	0	0	0
P-Well Contact	*	1	0	0	*	*	*	0	0	0	0	0	0	0	1	0	0	0
N-Well Contact	*	1	1	0	*	*	*	0	0	0	0	0	0	1	0	0	0	0
Silicided N+ PO Resistor	rnpoly	*	0	*	0	0	0	0	1	0	0	0	0	1	0	0	0	0
Silicided P+ PO Resistor	rppoly	*	0	*	0	0	0	0	1	0	0	0	0	0	1	0	0	0
Silicided N+ OD Resistor	rnod	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Silicided P+ OD Resistor	rpod	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0
Unsilicided N+ PO Resistor	rnpolywo	*	0	*	0	0	0	0	1	0	0	0	0	1	0	1	1	0
Unsilicided P+ PO Resistor	rppolywo	*	0	*	0	0	0	0	1	0	0	0	0	0	1	1	1	0
Unsilicided N+ OD Resistor	rnodwo	*	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Unsilicided P+ OD Resistor	rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0
NW Resistor (under STI)	rnwsti	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	1
NW Resistor (under OD)	rnwod	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 $\mu\text{m}^2$ ) npn5 (5x5 $\mu\text{m}^2$ ) npn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	0	0	1	1	0	0	0	0	0	1	0	0	0
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	1	0	1	0	0	0	0	0	1	0	0	0
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	1	1	0	1	0	0	0	0	0	1	0	0	0

### 3.4.5 CLN85 Low Power (LP)

Table 3.4.6

Device	SPICE Name	Design Levels												Special Layer					
		DNW	OD	NW	NT_N	OD_25	OD_33	POLY	VTH_N	VTH_P	ULVT_N	ULVT_P	N+	P+	RPO	RH	NWDMY	VAR	PSPO
NMOS (1.2V)	Nch	*	1	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
PMOS (1.2V)	Pch	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	0	0	1	0	1	0	0	0	1	0	0	0	0
Low Vt NMOS (1.2V)	nch_lvt	*	1	0	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
Ultra Low VT NMOS (1.2V)	nch_ulvt	*	1	0	0	0	0	0	1	0	0	1	0	1	0	0	0	0	1
Low Vt PMOS (1.2V)	pch_lvt	*	1	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	1
Ultra Low VT PMOS (1.2V)	pch_ulvt	*	1	1	0	0	0	0	1	0	0	0	0	1	0	1	0	0	1
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	0	1	0	0	0	0	0	1	0	0	0	0	0
I/O NMOS (3.3V)	nch_33	*	1	0	0	0	0	1	1	0	0	0	0	0	1	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	0	1	0	0	0	0	0	0	1	0	0	0	0
I/O PMOS (3.3V)	pch_33	*	1	1	0	0	0	1	1	0	0	0	0	0	0	1	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	0	1	0	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	1	0	1	0	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (3.3V)	nch_na33	0	1	0	1	0	0	1	1	0	0	0	0	1	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	0	0	0	1	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	0	0	0	1	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	0	0	0	1	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	0	0	0	0	1	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	0	1	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	0	1	0	0	0	0	0	0	1	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	0	1	1	1	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 um <sup>2</sup> ) pnp5 (5x5 um <sup>2</sup> ) pnp10 (10x10 um <sup>2</sup> )	0	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 um <sup>2</sup> ) npn5 (5x5 um <sup>2</sup> ) npn10 (10x10 um <sup>2</sup> )	1	1	1	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
1.2V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0	1
2.5V Varactor (NMOS Capacitor)	Nmoscap25	0	1	1	0	1	1	1	0	0	0	0	0	1	0	0	0	0	1
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	1	1	1	0	0	0	0	0	1	0	0	0	0	1

### 3.4.6 CLN80 General Purpose Consumer Platform (GC)

Table 3.4.7 CLN80GC Device Truth Table

Device	SPICE Name	Design Levels												Special Layers				
		DNW	OD	NW	NT_N	OD_25	OD_33	POLY	VTH_N	VTH_P	VTL_N	NTL_P	N+	P+	RPO	RH	NWDMY	VAR
NMOS (1.0V)	Nch	*	1	0	0	0	0	1	0	0	0	0	1	0	0	0	0	0
PMOS (1.0V)	Pch	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
High Vt NMOS (1.0V)	Nch_hvt	*	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0
High Vt PMOS (1.0V)	Pch_hvt	*	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0
Low Vt NMOS (1.0V)	Nch_lvt	*	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0
Low Vt PMOS (1.0V)	Pch_lvt	*	1	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0
I/O NMOS (2.5V)	Nch_25	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0
I/O NMOS (3.3V)	Nch_33	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0
I/O PMOS (2.5V)	Pch_25	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0
I/O PMOS (3.3V)	Pch_33	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0
Native NMOS (1.0V)	Nch_na	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (2.5V)	Nch_na25	0	1	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (3.3V)	Nch_na33	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	0	0	1	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	0	0	1	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	0	1	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	1	1	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	0	0	1	0	0	0	1	0
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	0	0	1	0	1	0	1	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 $\mu\text{m}^2$ ) npn5 (5x5 $\mu\text{m}^2$ ) npn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
1.0V Varactor (NMOS Capacitor)	nmoscap	0	1	1	0	0	0	1	0	0	0	0	1	0	0	0	0	1
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	0	1	0	0	0	0	1	0	0	0	0	1
3.3V Varactor (NMOS Capacitor)	nmoscap33	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1

### 3.4.7 CLN80 High Performance (GT)

Table 3.4.8 CLN80GT Device Truth Table

Device	SPICE Name	Design Levels										Special Layers				
		DNW	OD	NW	NT_N	OD_18	OD_25	POLY	VTH_N	VTH_P	N+	P+	RPO	RH	NWDMY	VAR
NMOS (1.2V)	Nch	*	1	0	0	0	0	1	0	0	1	0	0	0	0	0
PMOS (1.2V)	Pch	*	1	1	0	0	0	1	0	0	0	1	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	0	1	1	0	1	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	1	0	0	0	0
I/O NMOS (1.8V)	nch_18	*	1	0	0	1	0	1	0	0	1	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	0	1	1	0	0	1	0	0	0	0	0
I/O PMOS (1.8V)	pch_18	*	1	1	0	1	0	1	0	0	0	0	1	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	0	1	1	0	0	0	0	1	0	0	0
Native NMOS (1.2V)	nch_na	0	1	0	1	0	0	1	0	0	1	0	0	0	0	0
Native I/O NMOS (1.8V)	nch_na18	0	1	0	1	1	0	1	0	0	1	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	0	1	1	0	0	1	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	1	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	1	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	1	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	1	0	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	0	1	0	0	1	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	0	1	0	0	0	1	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	1	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	0	1	0	0	1	0	1	1	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	0	1	0	0	0	1	1	1	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	1	1	1	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	1	0	0	0	1	0
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	1	0	1	0	1	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	0	1	1	0	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 $\mu\text{m}^2$ ) npn5 (5x5 $\mu\text{m}^2$ ) npn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	0	1	1	0	0	0	0
1.2V Varactor (NMOS Capacitor)	Nmoscap	0	1	1	0	0	0	1	0	0	1	0	0	0	0	1
1.8V Varactor (NMOS Capacitor)	nmoscap18	0	1	1	0	1	0	1	0	0	1	0	0	0	0	1
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	0	1	1	0	0	1	0	0	0	0	1

### 3.4.8 CLN80 High Speed (HS)

Table 3.4.9 CLN80HS Device Truth Table

Device	SPICE Name	Design Levels												Special Layers				
		DNW	OD	NW	NT_N	OD_18	OD_25	POLY	VTH_N	VTH_P	VTL_N	VTL_P	N+	P+	RPO	RH	NWDMY	VAR
NMOS (1.2V)	Nch	*	1	0	0	0	0	1	0	0	0	0	0	1	0	0	0	0
PMOS (1.2V)	Pch	*	1	1	0	0	0	1	0	0	0	0	0	1	0	0	0	0
High Vt NMOS (1.05V)	nch_hvt	*	1	0	0	0	0	1	1	0	0	0	1	0	0	0	0	0
High Vt PMOS (1.05V)	pch_hvt	*	1	1	0	0	0	1	0	1	0	0	0	1	0	0	0	0
Low Vt NMOS (1.2V)	nch_lvt	*	1	0	0	0	0	1	0	0	1	0	1	0	0	0	0	0
Low Vt PMOS (1.2V)	pch_lvt	*	1	1	0	0	0	1	0	0	0	1	0	1	0	0	0	0
I/O NMOS (1.8V)	nch_18	*	1	0	0	1	0	1	0	0	0	0	1	0	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	0	1	1	0	0	0	0	1	0	0	0	0	0
I/O PMOS (1.8V)	pch_18	*	1	1	0	1	0	1	0	0	0	0	0	1	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	0	1	1	0	0	0	0	0	1	0	0	0	0
Native NMOS (1.05V)	nch_na	0	1	0	1	0	0	1	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (1.8V)	nch_na18	0	1	0	1	1	0	1	0	0	0	0	1	0	0	0	0	0
Native I/O NMOS (2.5V)	nch_na25	0	1	0	1	0	1	1	0	0	0	0	1	0	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	*	0	0	0	0	0	1	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	*	0	0	0	0	0	0	1	0	0	0	0
P-Well Contact		*	1	0	0	*	*	0	0	0	0	0	0	1	0	0	0	0
N-Well Contact		*	1	1	0	*	*	0	0	0	0	0	1	0	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	0	1	0	0	0	0	1	0	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	0	1	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	0	1	0	0	0	0	0	1	1	1	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	0	0	0	1	1	1	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	0	0	0	0	1	0	0	0	1
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	0	0	0	0	1	0	1	0	1
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	pn2 (2x2 $\mu\text{m}^2$ ) pn5 (5x5 $\mu\text{m}^2$ ) pn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	0	0	0	1	1	0	0	0	0
1.8VVaractor (NMOS Capacitor)	nmoscap18	0	1	1	0	1	0	1	0	0	0	0	1	0	0	0	0	1
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	0	1	1	0	0	0	0	1	0	0	0	0	1

### 3.4.9 CLN80 Low Power (LP)

Table 3.4.10 CLN80LP Device Truth Table

Device	SPICE Name	Design Levels										Special Layers			
		DNW	OD	NW	NT_N	OD_25	POLY	VTH_N	VTH_P	N+	P+	RPO	NWDMY	RH	VAR
NMOS (1.2V)	Nch	*	1	0	0	0	1	0	0	1	0	0	0	0	0
PMOS (1.2V)	Pch	*	1	1	0	0	1	0	0	0	1	0	0	0	0
High Vt NMOS (1.2V)	nch_hvt	*	1	0	0	0	1	1	0	1	0	0	0	0	0
High Vt PMOS (1.2V)	pch_hvt	*	1	1	0	0	1	0	1	0	1	0	0	0	0
I/O NMOS (2.5V)	nch_25	*	1	0	0	1	1	0	0	1	0	0	0	0	0
I/O PMOS (2.5V)	pch_25	*	1	1	0	1	1	0	0	0	1	0	0	0	0
N+/PW Junction Diode	NDIO	*	1	0	0	*	0	0	0	1	0	0	0	0	0
P+/NW Junction Diode	PDIO	*	1	1	0	*	0	0	0	0	1	0	0	0	0
P-Well Contact		*	1	0	0	*	0	0	0	0	1	0	0	0	0
N-Well Contact		*	1	1	0	*	0	0	0	1	0	0	0	0	0
Silicided N+ PO Resistor	Rnpoly	*	0	*	0	0	1	0	0	1	0	0	0	0	0
Silicided P+ PO Resistor	Rppoly	*	0	*	0	0	1	0	0	0	1	0	0	0	0
Silicided N+ OD Resistor	Rnod	*	1	0	0	0	0	0	0	1	0	0	0	0	0
Silicided P+ OD Resistor	Rpod	*	1	1	0	0	0	0	0	0	1	0	0	0	0
Unsilicided N+ PO Resistor	Rnpolywo	*	0	*	0	0	1	0	0	1	0	1	1	0	0
Unsilicided P+ PO Resistor	Rppolywo	*	0	*	0	0	1	0	0	0	1	1	1	0	0
Unsilicided N+ OD Resistor	Rnodwo	*	1	0	0	0	0	0	0	1	0	1	1	0	0
Unsilicided P+ OD Resistor	Rpodwo	*	1	1	0	0	0	0	0	0	1	1	1	0	0
NW Resistor (under STI)	Rnwsti	0	1	1	0	0	0	0	0	1	0	0	0	1	0
NW Resistor (under OD)	Rnwod	0	1	1	0	0	0	0	0	1	0	1	0	1	0
Vertical PNP (P+/NW/Psub) (constant emitter size)	pnp2 (2x2 $\mu\text{m}^2$ ) pnp5 (5x5 $\mu\text{m}^2$ ) pnp10 (10x10 $\mu\text{m}^2$ )	0	1	1	0	0	0	0	0	1	1	0	0	0	0
Vertical NPN (N+/PW/DNW) (constant emitter size)	npn2 (2x2 $\mu\text{m}^2$ ) npn5 (5x5 $\mu\text{m}^2$ ) npn10 (10x10 $\mu\text{m}^2$ )	1	1	1	0	0	0	0	0	1	1	0	0	0	0
1.2V Varactor (NMOS Capacitor)	Nmoscap	0	1	1	0	0	1	0	0	1	0	0	0	0	1
2.5V Varactor (NMOS Capacitor)	nmoscap25	0	1	1	0	1	1	0	0	1	0	0	0	0	1

### 3.4.10 CMN90 Device Truth Table

**Table 3.4.11 CMN90 Device Truth Table**

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### 3.4.11 CMN85 Device Truth Table

Table 3.4.12 CMN85 Device Truth Table

Device	SPICE Name	Design Levels															Special Layer								
		DNW	NW	OD	NT_N	POLY	N+	P+	RPO	CO	M1	M2	M3	M4	M5	VIA5	M8	CTM	CBM	VIA8	M9 (or UTM)	POBLK			
Inductor	spiral_std	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1	1	0	0	0	0
	spiral_sym	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0	1	1	1	0	0
	spiral_sym_ct	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	1	0	0	1	1	1	0
MIM_w/i shield	mimcap_um_1p5_sin_rf	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	0	0	
MIM_w/o shield	mimcap_wo_um_1p5_sin_rf	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1	1	0	0	1	

### 3.4.12 CMN80 Device Truth Table

Table 3.4.13 CMN80 Device Truth Table

Device	SPICE Name	Design Levels																		Special Layer								
		DNW	NW	OD	NT_N	POLY	N+	P+	RPO	CO	M1	M2	M3	M4	M5	VIA5	M6	M7	VIA7	VIA8	M9	CTMDMY	RFDMY	ODBLK	PUBLK			
MIM_w/i shield	mimcap_um_1p5_sin_rf	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	1	1	1	1	0	0	1	1	0	0
MIM_w/o shield	mimcap_wo_um_1p5_sin_rf	1	1	1	0	0	0	0	0	1	1	0	0	0	0	0	0	1	1	1	1	1	0	0	1	1	1	1

### 3.5 Mask Requirement for Device options (High/STD/Low VT)

Table 3.5.1 N90

Device	Mask Requirements	
	Well	LDD
STD Vt + I/O(DGO)	4 masks PW1V/2V, NW1V/2V	4 masks N1V/2V, P1V/2V
STD Vt + I/O(TGO)	G: 4 masks PW1V/2V, NW1V/2V	G: 6 masks N1V/2V/3V, P1V/2V/3V
STD Vt + Low Vt + I/O (DGO)	4 masks PW1V/2V, NW1V/2V	G: 6 masks N1V/2V, P1V/2V, VTL_N/P
		GT, LP: 4 masks N1V/2V, P1V/2V
STD Vt + Low Vt + I/O (TGO)	G: 4 masks PW1V/2V, NW1V/2V	G: 8 masks N1V/2V/3V, P1V/2V/3V, VTL_N/P
STD Vt + Low Vt + Ultra Low VT+ High Vt + I/O (DGO)	6 masks PW1V/2V, NW1V/2V, VTH_N/P	6 masks N1V/2V, P1V/2V, ULVT_N/P
STD Vt + High Vt + I/O (DGO)	G, LP: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	G, LP: 4 masks N1V/2V, P1V/2V
	GT: 5 masks PW1V/2V, NW1V/2V, VTH_N	GT: 5 masks N1V/2V, P1V/2V, VTH_P
STD Vt + High Vt + I/O (TGO)	G: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	G: 6 masks N1V/2V/3V, P1V/2V/3V
STD Vt + Low Vt + High Vt + I/O (DGO)	G: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	G: 6 masks N1V/2V, P1V/2V, VTL_N/P
	GT: 5 masks PW1V/2V, NW1V/2V, VTH_N	GT: 5 masks N1V/2V, P1V/2V, VTH_P
	LP: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	LP: 4 masks N1V/2V, P1V/2V
STD Vt + Low Vt + High Vt + I/O (TGO)	G: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	G: 8 masks N1V/2V/3V, P1V/2V/3V, VTL_N/P

Table 3.5.2 N85

Device	Mask Requirements	
	Well	LDD
STD Vt + I/O(DGO)	4 masks PW1V/2V, NW1V/2V	4 masks N1V/2V, P1V/2V
STD Vt + I/O(TGO)	G: 4 masks PW1V/2V, NW1V/2V	G: 6 masks N1V/2V/3V, P1V/2V/3V
STD Vt + Low Vt + I/O (DGO)	4 masks PW1V/2V, NW1V/2V	G: 6 masks N1V/2V, P1V/2V, VTL_N/P
		LP: 4 masks N1V/2V, P1V/2V
STD Vt + Low Vt + I/O (TGO)	G: 4 masks PW1V/2V, NW1V/2V	G: 8 masks N1V/2V/3V, P1V/2V/3V, VTL_N/P
STD Vt + High Vt + I/O (DGO)	G, LP: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	G, LP: 4 masks N1V/2V, P1V/2V
STD Vt + High Vt + I/O (TGO)	G: 6 masks PW1V/2V, NW1V/2V, VTH_N/P	G: 6 masks N1V/2V/3V, P1V/2V/3V
STD Vt +	G: 6 masks	G: 6 masks

Mask Requirements		
Device	Well	LDD
Low Vt + High Vt + I/O (DGO)	PW1V/2V,NW1V/2V,VTH_N/P	N1V/2V,P1V/2V,VTL_N/P
STD Vt + Low Vt + High Vt + I/O (TGO)	G: 6 masks PW1V/2V,NW1V/2V,VTH_N/P	G: 8 masks N1V/2V/3V,P1V/2V/3V,VTL_N/P
STD Vt + Low Vt + Ultra Low VT+ High Vt + I/O (DGO)	LP: 6 masks PW1V/2V,NW1V/2V,VTH_N/P	LP: 6 masks N1V/2V, P1V/2V, ULVT_N/P

**Table 3.5.3 N80GC**

Mask Requirements		
Device	Well	LDD
STD Vt + I/O(DGO)*	4 masks PW1V/2V, NW1V/2V	4 masks N1V/2V,P1V/2V
STD Vt + High Vt + I/O (DGO)	6 masks PW1V/2V,NW1V/2V,VTH_N,VTH_P	4 masks N1V/2V, P1V/2V
STD Vt + Low Vt + I/O (DGO)	5 masks PW1V/2V,NW1V/2V, VTL_N	5 masks N1V/2V, P1V/2V, VTL_P
Low Vt + STD Vt + High Vt + I/O (DGO)	7 masks PW1V/2V,NW1V/2V,VTH_N, VTL_N, VTH_P	5 masks N1V/2V, P1V/2V, VTL_P

**Table 3.5.4 N80GT**

Mask Requirements		
Device	Well	LDD
STD Vt + I/O(DGO)*	4 masks PW1V/2V, NW1V/2V	4 masks N1V/2V,P1V/2V
STD Vt + High Vt + I/O (DGO)	5 masks PW1V/2V,NW1V/2V,VTH_N	5 masks N1V/2V, P1V/2V, VTH_P

**Table 3.5.5 N80HS**

Mask Requirements		
Device	Well	LDD
STD Vt + I/O(DGO)**	4 masks PW1V/2V, NW1V/2V	4 masks N1V/2V,P1V/2V
STD Vt + High Vt + I/O (DGO)	4 masks PW1V/2V,NW1V/2V	6 masks N1V/2V,P1V/2V,VTH_N/P
STD Vt + Low Vt + I/O (DGO)	4 masks PW1V/2V,NW1V/2V	6 masks N1V/2V,P1V/2V, VTL_N/P
Low Vt + STD Vt + High Vt + I/O (DGO)	4 masks PW1V/2V,NW1V/2V	8 masks N1V/2V,P1V/2V,VTH_N/P, VTL_N/P

**Table 3.5.6 N80LP**

Mask Requirements		
Device	Well	LDD
STD Vt + I/O(DGO)*	4 masks PW1V/2V, NW1V/2V	4 masks N1V/2V,P1V/2V
STD Vt + High Vt + I/O (DGO)	6 masks PW1V/2V,NW1V/2V,VTH_N,VTH_P	4 masks N1V/2V, P1V/2V

\* For N80GC/GT/LP SRAM, VTC\_N and VTH\_P mask are mandatory.

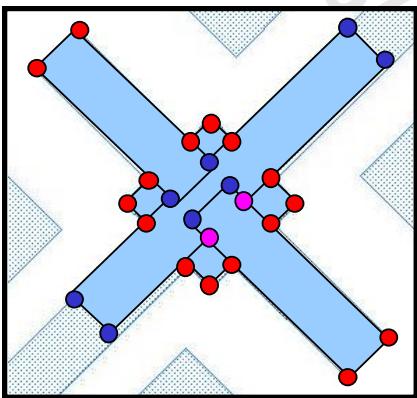
\*\* For N80HS SRAM, VTC\_N, VTH\_N and VTH\_P mask are mandatory.

## 3.6 Design Geometry Restrictions

### 3.6.1 Design Geometry Rules

Table 3.6.1

Rule No.	Description															
G.1	The design grid must be an integer multiple of 0.005 μm except PO & CO layers inside the layer 186;4. 0.005μm deviation is allowed for 45-degree polygon dimensions. DRC will not flag UBM/ CBD/PM/CB2/PM2/PPI layers when vertexes of polygon are larger than 100.															
G.2	Shapes with acute angles between line segments are not allowed.															
G.3	Only shapes that are orthogonal or on a 45-degree angle are allowed.															
G.4	Don't use the following GDS layer;datatype. They are reserved for tsmc internal mask making. <table border="1" data-bbox="293 763 769 954"> <thead> <tr> <th>layer</th><th>datatype</th><th>Example</th></tr> </thead> <tbody> <tr> <td>6</td><td>161~165</td><td>6;161</td></tr> <tr> <td>17</td><td>161~165</td><td>17;161</td></tr> <tr> <td>31~39</td><td>161~165</td><td>31;161</td></tr> <tr> <td>168</td><td>161~165</td><td>168;161</td></tr> </tbody> </table>	layer	datatype	Example	6	161~165	6;161	17	161~165	17;161	31~39	161~165	31;161	168	161~165	168;161
layer	datatype	Example														
6	161~165	6;161														
17	161~165	17;161														
31~39	161~165	31;161														
168	161~165	168;161														
G.5g <sup>U</sup>	For OD, PO, VTL_N, VTL_P, VTH_N, VTH_P, NP, PP, M1, Mx, all vertices and intersections of 45-degree polygon must be on an integer multiple of 0.005 μm except PO inside the layer 186;4.															

Figure 3.6.1 Illustration for G.5g<sup>U</sup>.

### 3.6.1.1 DBU guideline

Recommend to use 1nm as layout database unit (DBU) when streaming out GDS. TSMC's technology files adopt 1nm DBU by default. If further DBU setting is considered, please consult it with TSMC for guidelines to modify default setting of TSMC's technology files.

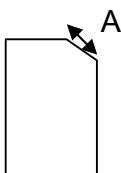
### 3.6.2 OPC Recommendations and Guidelines

The following OPC recommendations are very important tips to reduce OPC and mask-making cycle time (or physical verification) and ensure the best silicon performance:

- **Make certain that the design is DRC clean (free of all DRC violations).**
- **Do not use circles, oval shapes, or logos of arbitrary geometry (Figure 3.6.2).** Use rectangular or 45-degree polygons to write words, logos, and other marks that are not part of the circuit.
- **Verify that all line ends are rectangular.**
- **Limit cell names to 64 or fewer characters.**
- **Use a well-organized, hierarchical layout structure.**

**Avoid redundant or excessive overlaps of polygons from two, or more than two, different cells or cell placements.** For example, avoid forming a straight line from numerous cell placements, with each one contributing a little piece. Refer to the “Design Hierarchy Guidelines” section in this chapter

Rule No.	Description	Label	Rule
OPC.R.1®	Avoid small zigzag patterns for OPC friendly layouts (Figure 3.6.3 and 3.6.4). It is recommended that any edge of length $< 1.0 \times$ minimum width cannot have another adjacent edge of length $< 1.0 \times$ minimum width. The OPC layers: OD, PO, VTL_N, VTL_P, VTH_N, VTH_P, NP, PP, CO, M1, Vx, Mx, My and MD (2XTM).		
OPC.R.2g	Avoid small jogs (Figure 3.6.3). It is recommended that you use greater than, or equal to, half of the minimum width of each layer for each segment of a jog.		
OPC.R.3®	Recommended 45-degree edge length of all layers	A	$\geq$ 0.5



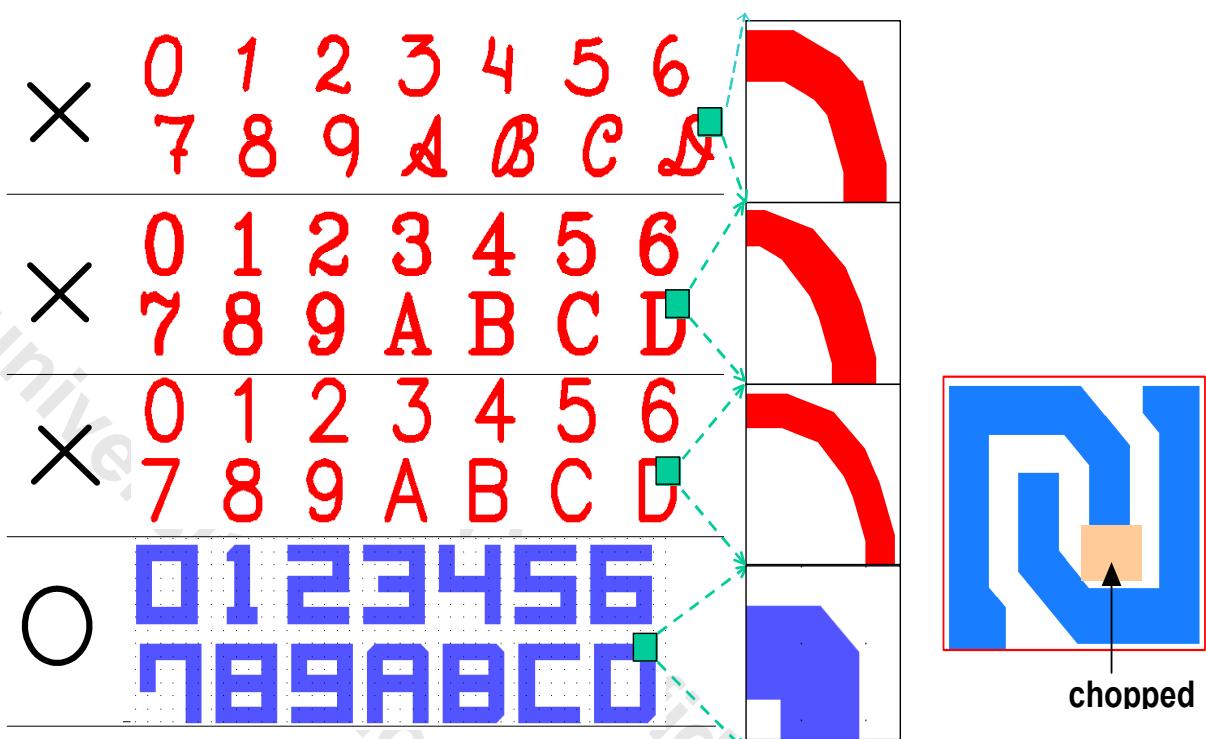


Figure 3.6.2 Logo Geometry Example

Worse performance in the simulation of contour for the layout with small jog/zigzag.

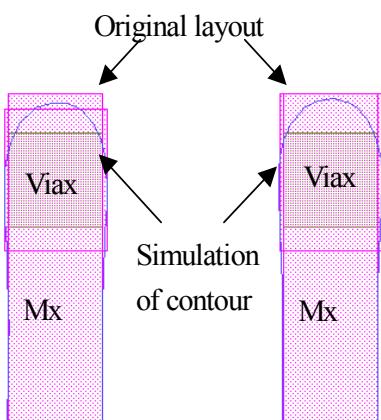


Figure 3.6.3 Simulation contour for the layout with and without small jog/zigzag. The simulation is Mx line and not well treated due to small jog/zigzag, and cause smaller Vias overlap.

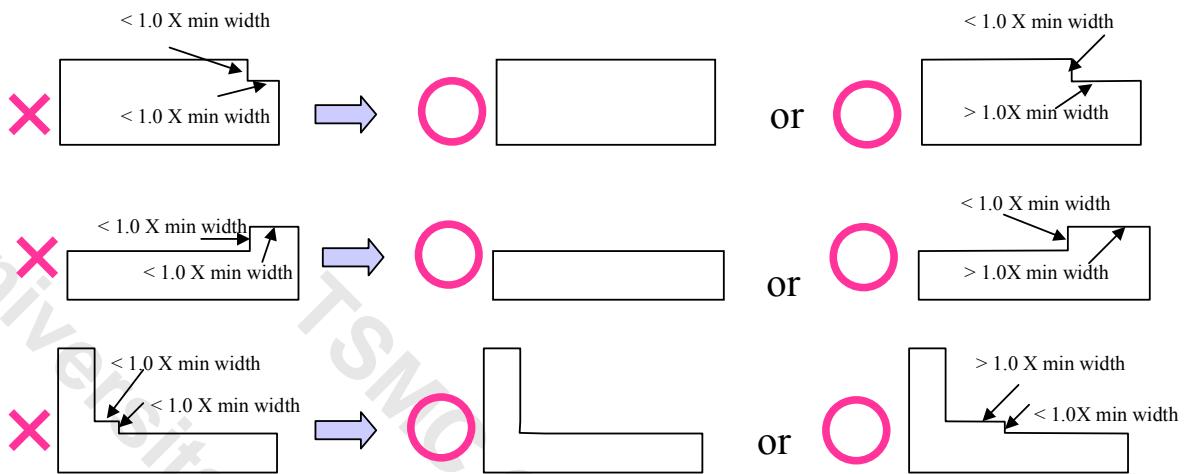


Figure 3.6.4 Avoid small zigzag

## 3.7 Design Hierarchy Guidelines

The style of the cell hierarchy in a design can significantly affect the following:

- OPC and mask-making cycle time
- Run time and memory usage of physical verification.

Following are the recommended practices:

- **Re-use design blocks as much as possible.**

Do not create two different cells for the same device.

- **Whenever possible, avoid using *L*, *U*, or *ring* shapes.**

For inevitable *ring* structures such as seal rings and power rings, use cells for holding each ring segment instead of drawing the whole ring at once. The same method applies to the *L* and *U* shapes.

- **Put everything as low in the cell hierarchy as possible.** Here are some examples:

- o Put all shapes required for defining a device or circuit into the same cell. An inverter cell, for example, should include NW, OD, PO, NP, and PP, as well as CO and M1 (for pins).
- o Avoid drawing a large shape to cover a whole circuit.
- o Place texts at the lowermost cell where devices can be formed.
- o For layout patches/revisions/ECOs, avoid changing device properties or metal connections at upper cells in the design hierarchy.
- o Draw within the cell the shapes required in TSMC's logic operations.

Please consider all independent layers used in each rule logic operations and derived layer logic operations. For example, LDN.EX.1 applies to NP and OD2; therefore, NP should reside in the same cell as OD2.

- **Make certain each cell is DRC clean in a bottom-up construction of the cell hierarchy.**

For example, when placing a contact in a cell, place M1 in that cell as well, with the required amount of M1.

- **Keep dummy fill geometry in a separate hierarchy from the main patterns and reduce the count of flattened dummy fill geometry as much as possible.**

## 4 Layout Rules and Recommendations

This chapter provides the following general layout information:

- 4.1 Layout Rule Conventions
- 4.2 Special Geometries Used in Physical Design Rules
- 4.3 Definition of Layout Geometrical Terminology
- 4.4 Minimum Pitches
- 4.5 CLN90 (Logic) Layout Rules and Guidelines
- 4.6 CMN90 (MIXED SIGNAL, RF) Layout Rules and guidelines

### 4.1 Layout Rule Conventions

Layout rules follow these conventions:

- Unless otherwise specified, all rules are of minimum dimension.
- The basic unit of measure is  $\mu\text{m}$ ; the basic unit of area is  $\mu\text{m}^2$ .
- Process, product, and reliability yields are expected to be improved when designs are relaxed from minimum dimensions. Minimum dimensions showed only to be used to shrink the chip size or to improve the circuit performance.
- Design rules requiring exact dimensions (“=” in the rule tables) are not to be relaxed.
- Guideline is grouped by a separate table.
- DFM recommendations and guidelines are designated by a registered symbol ® or “g” after the rule number.
- A registered symbol “<sup>U</sup>” is marked after the rule number as the rule is not checked by DRC.
- Bracket usage in the rules should be noted carefully:
  - o Parentheses ( ) are used for explanation.
  - o Square brackets [ ] are used for certain conditions.
  - o Curved brackets { } are used to indicate that an operation is performed.

## 4.2 Special Geometries Used in Physical Design Rules

The following definitions are used in the physical design rules:

### 4.2.1 Derived Geometries

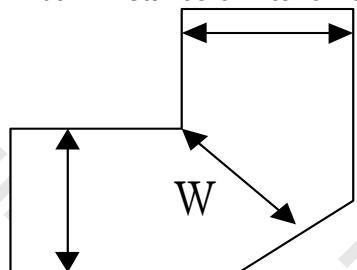
Term	Definition
ACTIVE	N+ ACTIVE OR P+ ACTIVE
ALLOD	OD OR DOD
Butted_STRAP	STRAP TOUCH ACTIVE
FIELD	NOT OD
FIELD PO	PO NOT OD
GATE	PO AND OD
N+ ACTIVE	(NP AND OD) NOT NW
N+OD	NP AND OD
NW STRAP	(NP AND OD) AND NW
NW1V	NW NOT OD2
NW2V	NW AND OD2
NWROD	(NW INTERACT NWDMY) INTERACT RPO
NWRSTI	(NW INTERACT NWDMY) NOT INTERACT RPO
PW	NOT NW
OD2	OD_18, OD_25, OD_33
P+ ACTIVE	(PP AND OD) AND NW
P+OD	PP AND OD
PW STRAP	(PP AND OD) NOT NW
STRAP	NW STRAP OR PW STRAP

### 4.2.2 Special Definition

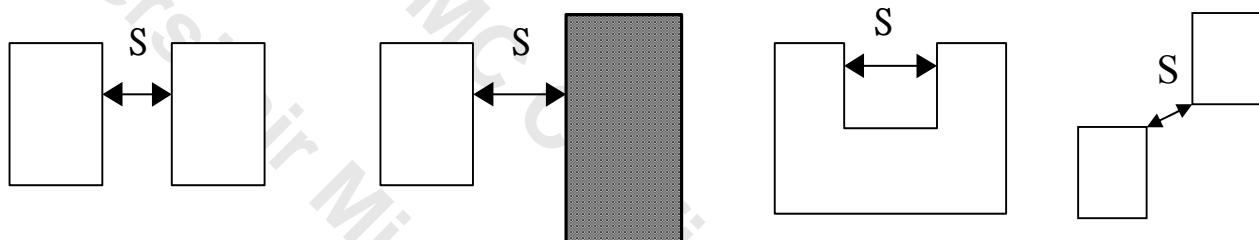
Term	Definition
NW	N-WELL
RW	PW inside DNW
MOS	Transistor structure consisting of a source, a drain, and a gate.
NMOS	N type MOS
PMOS	P type MOS
DOD	Dummy OD
DPO	Dummy PO
DMx	Dummy Metal
DMx_O	OPC dummy metal. The rules of DMx_O are the same as real metal, Mx.
DMD	Dummy MD
Chip edge	“Chip” doesn’t include seal ring and assembly isolation
Assembly isolation	The region between the seal ring and chip edge
CUP	Wire bond pad design for Circuit Under Pad

## 4.3 Definition of Layout Geometrical Terminology

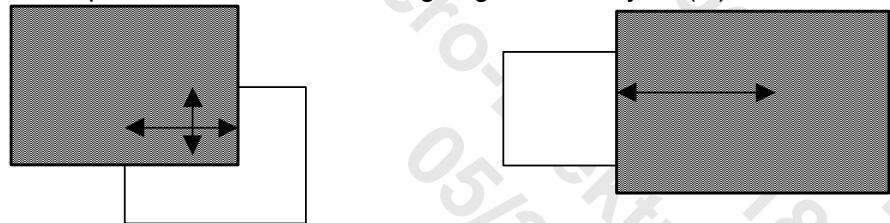
Width: Distance of interior-facing edge for single layer. (W)



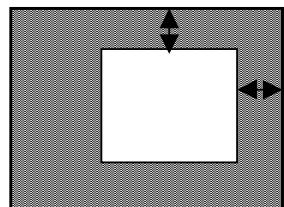
Space: Distance of exterior-facing edge for one or two layer (S)



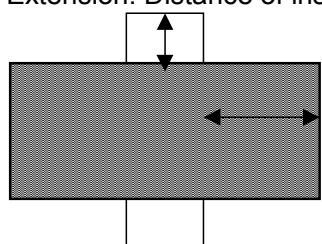
Overlap: Distance of interior-facing edge for two layers (O)



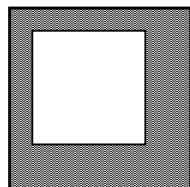
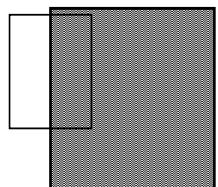
Enclosure: Distance of inside edge to outside edge (Fully inside) (EN)



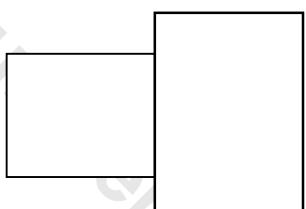
Extension: Distance of inside edge to outside edge (EX)



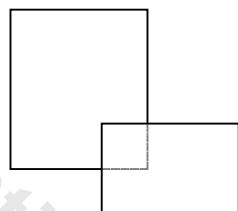
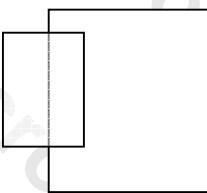
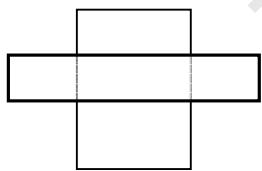
Interact with:



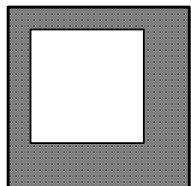
Butted



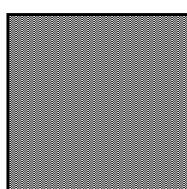
Cut:



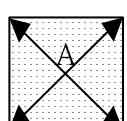
Inside:



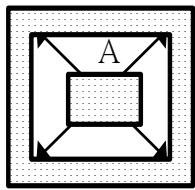
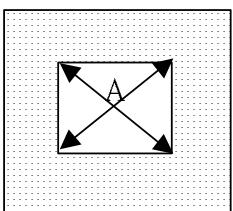
Outside:



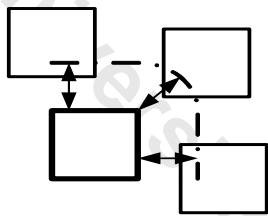
AREA (A):



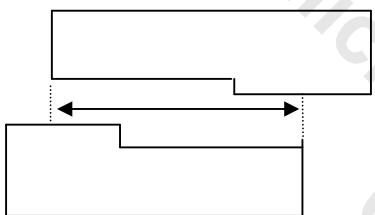
ENCLOSED Area (A):



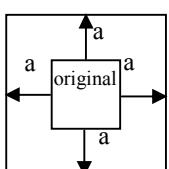
3-Neighboring:



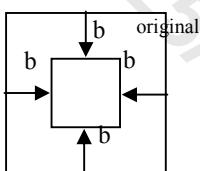
Parallel run length:



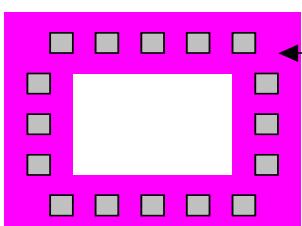
Size up a



Size down b

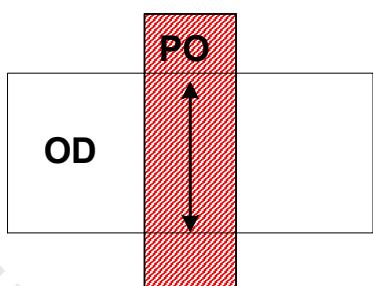


Guard ring

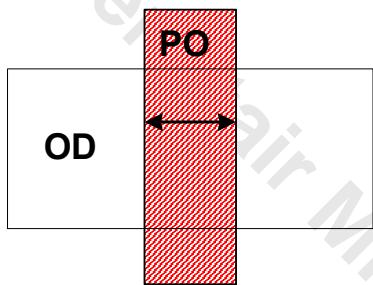


Ring-type OD and M1 with CO as  
many as possible

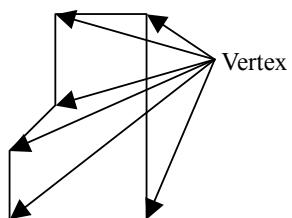
Channel width



Channel length



Vertex: Polygon whose edge form an angle



## 4.4 Minimum Pitches

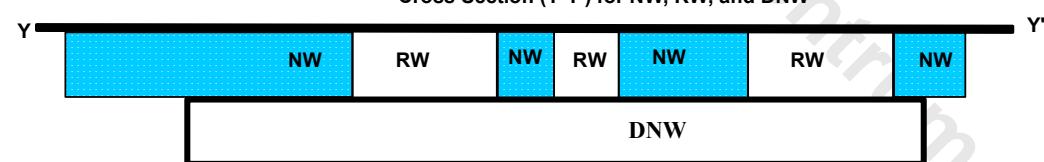
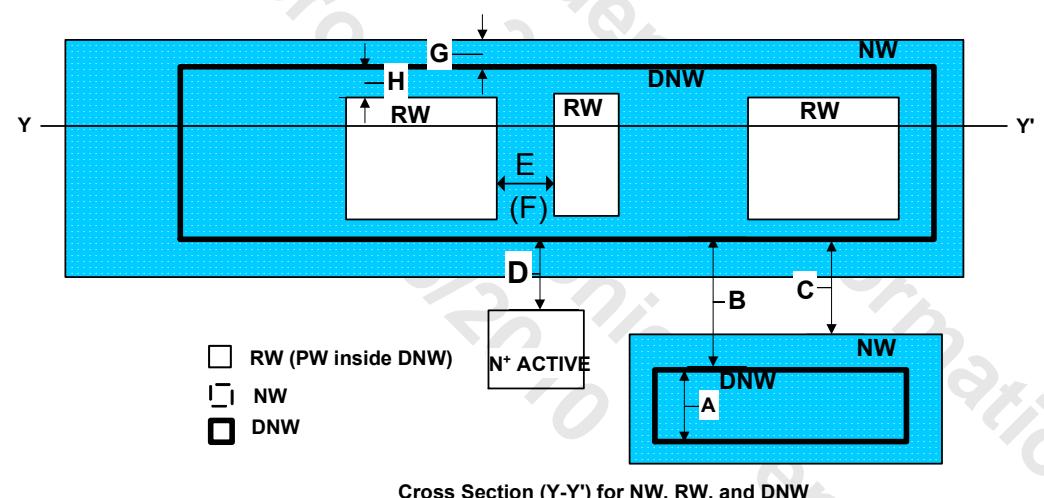
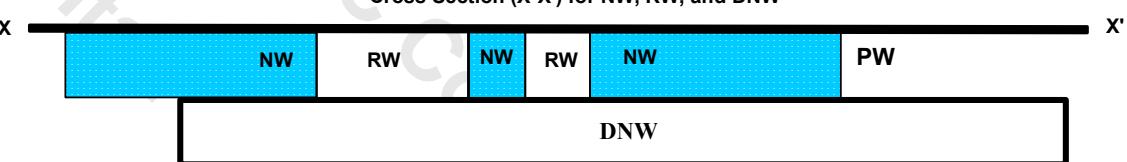
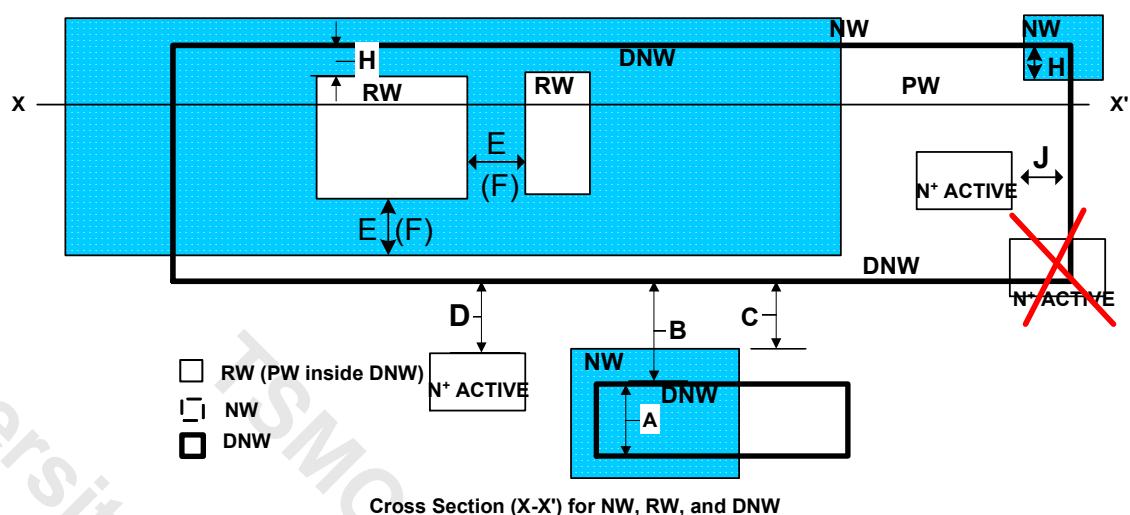
Layer	CLN90G/LP/HS (Unit: $\mu\text{m}$ )
OD interconnect pitch	0.25 (W/S=0.11/0.14)
OD interconnect width	0.11
OD transistor pitch	0.26 (W/S=0.12/0.14)
PO interconnect pitch (on STI)	0.24 (W/S=0.10/0.14)
PO interconnect width	0.10
PO transistor pitch (on OD)	0.25 (W/S=0.10/0.15)
Minimum length of a transistor	0.10
Minimum width of a transistor	0.12
N+/P+ spacing	0.44
M1 pitch	0.24 (W/S=0.12/0.12)
Mx pitch ( $x=2\sim 7$ )	0.28 (W/S=0.14/0.14)
Mn pitch ( $n=8\sim 9$ ) for 3XTM	0.84 (W/S=0.42/0.42)
My pitch ( $y=8\sim 9$ ) for 2XTM	0.56 (W/S=0.28/0.28)
Mu pitch	4.0 (W/S=2.0/2.0)
CTM pitch	2.8 (W/S=2.0/0.8)
CBM pitch	4.8 (W/S=2.8/2.0)
CO $\geq 3$ neighboring pitch	0.28 (W/S=0.12/0.16)
CO pitch	0.26 (W/S=0.12/0.14)
VIAx $\geq 3$ neighboring pitch ( $x=1\sim 6$ )	0.30 (W/S=0.13/0.17)
VIAx pitch ( $x=1\sim 6$ )	0.28 (W/S=0.13/0.15)
VIAN $\geq 3$ neighboring pitch ( $n=7,8$ ) for 3XTM	0.90 (W/S=0.36/0.54)
VIAN pitch ( $n=7,8$ ) for 3XTM	0.70 (W/S=0.36/0.34)
VIAy $\geq 3$ neighboring pitch ( $y=7,8$ ) for 2XTM	0.63 (W/S=0.26/0.37)
VIAy pitch ( $y=7,8$ ) for 2XTM	0.56 (W/S=0.26/0.30)

## 4.5 CLN90 (Logic) Layout Rules and Guidelines

### 4.5.1 Deep N-Well (DNW) Layout Rules (MASK ID:119) [Optional]

Rule No.	Description	Label		Rule
DNW.W.1	Width	A	$\geq$	3
DNW.S.1	Space	B	$\leq$	4.8
DNW.S.2	Space to NW with different potential	C	$\geq$	3.3
DNW.S.3	Space to N+ACTIVE (DNW cut N+ACTIVE is not allowed)	D	$\geq$	1.82
DNW.S.4	RW space to {RW OR PW} with different potential	E	$\geq$	1.0
DNW.S.5	{RW OR PW} space to {RW interact with OD2} with different potential	F	$\geq$	1.2
DNW.EN.1®	Recommended enclosure by NW for better noise isolation (Except SBDDMY region)	G	$\geq$	1.5
DNW.EN.2	Enclosure of N+ACTIVE	J	$\geq$	0.62
DNW.O.1	Overlap of NW	H	$\geq$	0.4
DNW.R.3	Keep {NW interact with same DNW} and PW in reverse bias			
DNW.R.4 <sup>U</sup>	(1) DNW and {NW interact with same DNW} must bias at same potential. (2) {NWs interact with same DNW} must bias at same potential			
Guideline	Description			
DNW.R.5g	Recommend not using floating RW unless necessary to avoid unstable device performance. DRC can flag RW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.			

## DNW

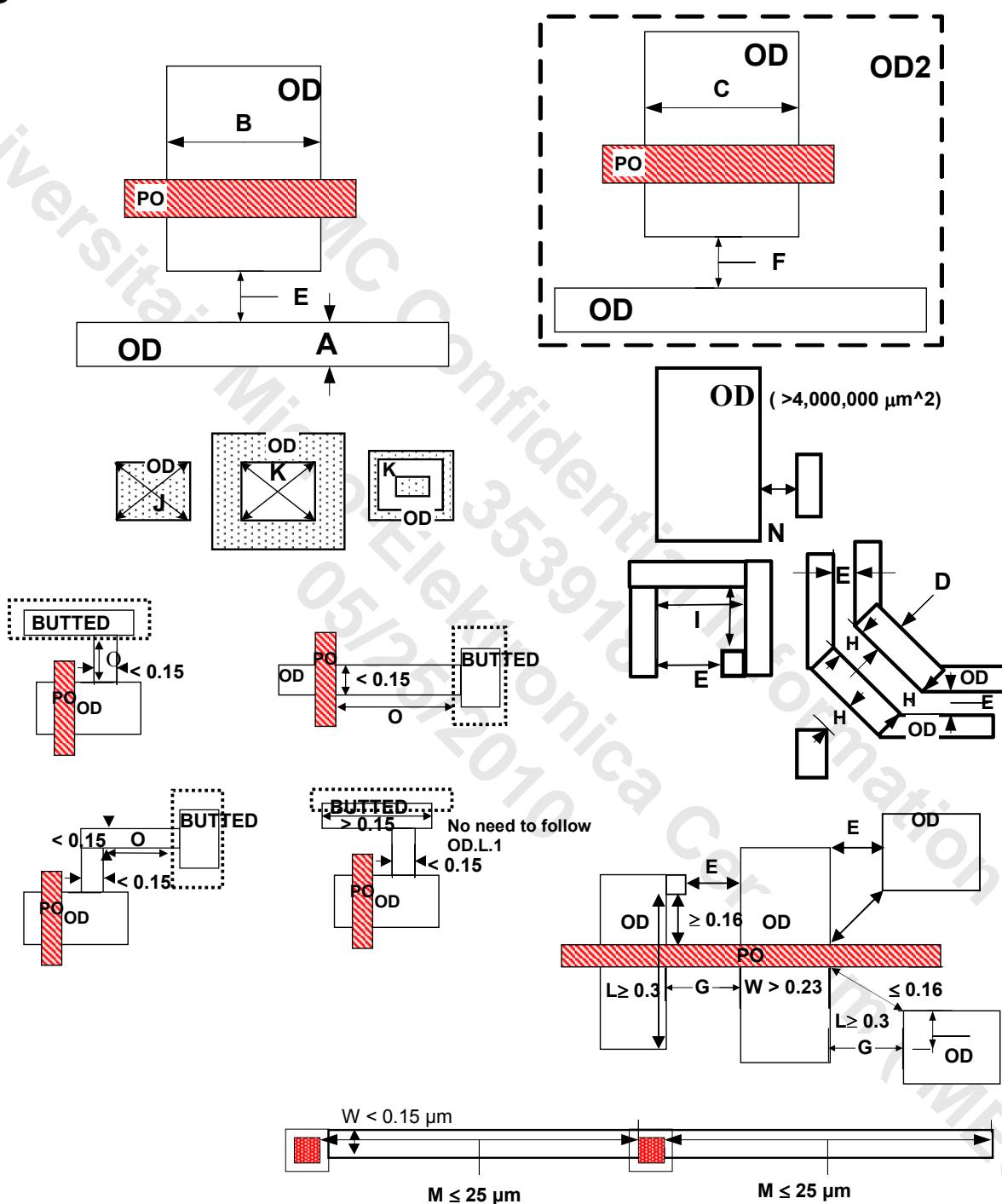


## 4.5.2 Gate Oxide and Diffusion (OD) Layout Rules (Mask ID: 120)

Rule No.	Description	Label		Rule
OD.W.1	Width	A	$\geq$	0.11
OD.W.2	Width of MOS ( $\leq 1.2V$ ) [for core device]	B	$\geq$	0.12
OD.W.2®	Recommended width of MOS ( $\leq 1.2V$ ) [for core device] for stable $I_{sat}$ (avoid corner rounding effect)	B	$\geq$	0.2
OD.W.3	Width of MOS ( $> 1.2V$ to $\leq 3.3V$ ) [for I/O device]	C	$\geq$	0.4
OD.W.4	Width of 45 degree OD Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)	D	$\geq$	0.18
OD.S.1	Space	E	$\geq$	0.14
OD.S.1®	Recommended minimum OD space to reduce short possibility caused by particle	E	$\geq$	0.18
OD.S.2	Space of {OD AND OD2} *It is recommended to avoid using minimum OD space, 0.14um, at OD interact with OD2 layout style for low leakage concern.	F	$\geq$	0.18
OD.S.3	Space between two ODs with a parallel length ( $L$ ) $\geq 0.3 \mu m$ and at least one of the corresponding OD regions has width ( $W$ ) $> 0.23 \mu m$ : (a) if crossed by a common PO, or (b) if PO is crossing one of the ODs. Rule applies up to the other OD with a space $\leq 0.16 \mu m$ away from the gate.	G	$\geq$	0.16
OD.S.4	Space to 45-degree OD	H	$\geq$	0.18
OD.S.5	Space between two segments of a U-shape or an O-shape OD (notch only)	I	$\geq$	0.2
OD.S.6®	Recommended space to OD [ OD area $> 4,000,000 \mu m^2$ ]	N	$\geq$	0.35
OD.A.1	Area	J	$\geq$	0.060
OD.A.2	Enclosed area	K	$\geq$	0.085
OD.L.1	Maximum length of {ACTIVE (source) [width $< 0.15 \mu m$ ] interacts with butted STRAP}	O	$\leq$	0.5
OD.L.2	Maximum OD length [OD width is $< 0.15 \mu m$ ] between two contacts as well as between one contact and the OD line end	M	$\leq$	25
OD.DN.1	{OD OR DOD} density across full chip		$\geq$	25%
			$\leq$	75%
OD.DN.2	{OD OR DOD} local density		$\geq$	20% in 150x150
			$\leq$	80% in 150x150 (outside OD2)
			$\leq$	90% in 150x150
OD.DN.3	{OD OR DOD} local density inside ODBLK		$\geq$	20% in 150x150
			$\leq$	80% in 150x150 (outside OD2)
			$\leq$	90% in 150x150
OD.R.1	OD must be fully covered by {NP OR PP} except for DOD/LOGO/NW resistor within OD/SBDDMY region.			
DOD.R.1*	DOD is a must. DOD CAD layer (TSMC default, 6;1) must be different from OD's. Please refer to section 6.1.			
Guideline	Description			
OD.L.2g <sup>U</sup>	Recommended to limit the maximum interconnect OD length (M) as short as possible to avoid Rs variation by salicidation.			

**Table Notes:**

- \* In order to meet the extremely tight requirement in terms of process control for STI etch, polish as well as channel length definition (inter-level dielectric (ILD) planariation), you must fill the DOD globally and uniformly even if the originally drawn OD already satisfies the required OD density rule (OD.DN.1~OD.DN.3). It is recommended to manually add DOD uniformly inside regions covered by the ODBLK layer, to gain better process window and electrical performance.

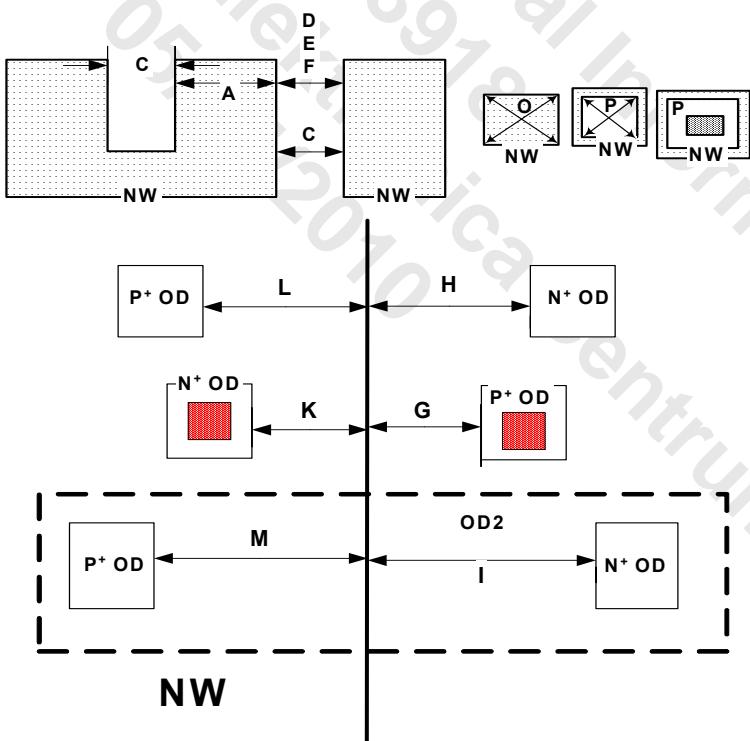
**OD**

## 4.5.3 N-Well (NW) Layout Rules

Rule No.	Description	Label		Rule
NW.W.1	Width	A	$\geq$	0.62
NW.S.1	Space	C	$\geq$	0.62
NW.S.2	Space of two NW1V with different potentials (*)	D	$\geq$	1.00
NW.S.3	NW1V space to NW2V with different potentials	E	$\geq$	1.20
NW.S.4	Space of two NW2V with different potentials (*)	F	$\geq$	1.20
NW.S.5	Space to PW STRAP	G	$\geq$	0.17
NW.S.6	Space to N+ ACTIVE	H	$\geq$	0.22
NW.S.7	Space to {N+ ACTIVE interact with OD2}	I	$\geq$	0.31
NW.EN.1	Enclosure of NW STRAP	K	$\geq$	0.17
NW.EN.2	Enclosure of P+ ACTIVE	L	$\geq$	0.22
NW.EN.3	Enclosure of {P+ ACTIVE interact with OD2}	M	$\geq$	0.31
NW.A.1	Area	O	$\geq$	1.55
NW.A.2	Enclosed area	P	$\geq$	1.55
Guideline	Description			
NW.R.1g	Recommend not using floating well unless necessary to avoid unstable device performance. DRC can flag both NW is not with CO in NPOD and PW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.			

(\*) DRC implementation is on different nets.

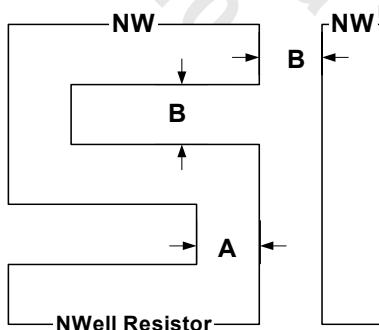
### NW

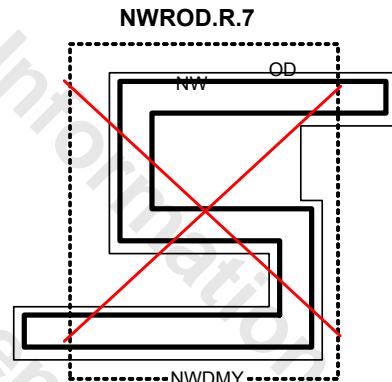
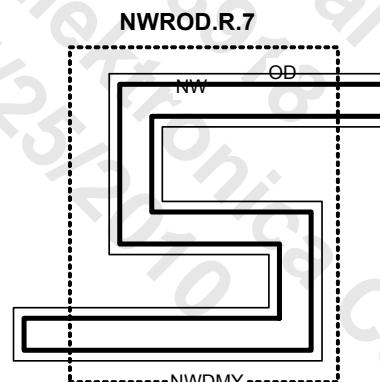
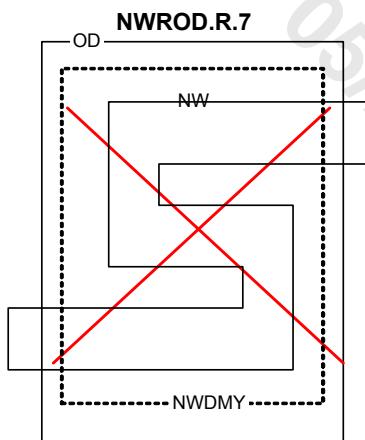
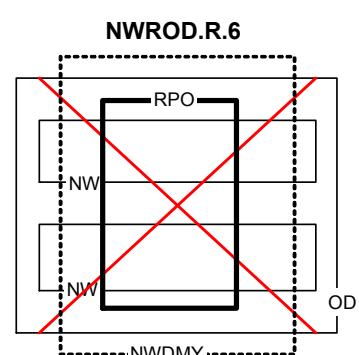
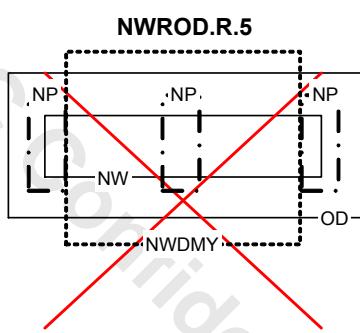
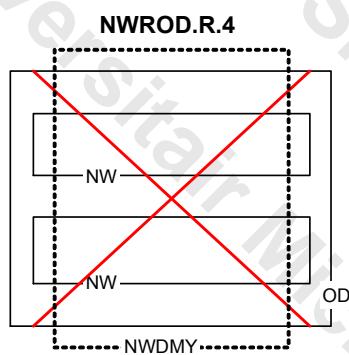
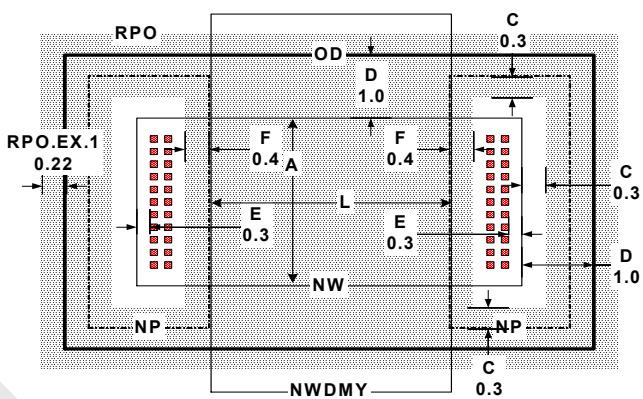


## 4.5.4 N-Well Resistor Within OD (NWROD) Layout Rules

Rule No.	Description	Label		Rule
NWROD.W.1	Width	A	$\geq$	1.8
NWROD.S.1	Space to NWROD or to NW	B	$\geq$	1.2
NWROD.S.2	Space to RPO	C	$\leq$	0.3
NWROD.EN.1	Enclosure by OD	D	$\geq$	1.0
NWROD.EN.2	Enclosure of CO	E	$\geq$	0.3
NWROD.O.1	RPO overlap of NP. Use exact value (0.4um) on sides touching NWDMY.	F	$\geq$	0.4
NWROD.O.2	{OD AND NWDMY} overlap of {NP, PP, VTH_N, VTH_P, VTL_N, or VTL_P } (all implant layers except NW) is not allowed.			
NWROD.R.1®	Recommend resistor length (L) $\geq$ 20um, and square number (length (L) / width (A)) $\geq$ 5 for SPICE simulation accuracy. DRC can not check square number.			
NWROD.R.4	Only one NW in NWROD is allowed in one OD.			
NWROD.R.5	Only two NPs in NWROD is allowed in one OD.			
NWROD.R.6	Only two RPO holes(Sailcide) in NWROD are allowed in same OD			
NWROD.R.7	For U-shape or S-shape NWROD, both OD and NW must be U-shape or S-shape and the OD edge must be parallel to the NW edge. DRC can only flag the pattern without OD space while 2 edges of NW [NW space or notch $\leq$ 5 um] parallel length $>$ 0 um.			
Guideline	Description			
NWROD.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.			

### NWROD



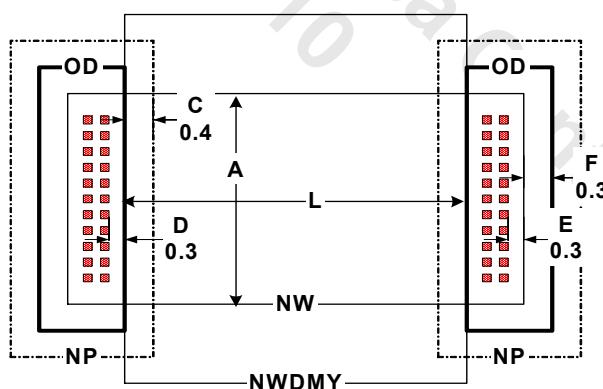
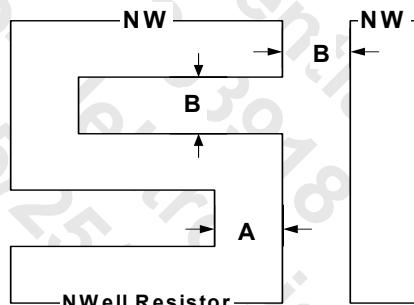


The layout is uncheckable

## 4.5.5 N-Well Resistor Under STI (NWRSTI) Layout Rules

Rule No.	Description	Label		Rule
NWRSTI.W.1	Width	A	$\geq$	1.8
NWRSTI.S.1	Space to NWRSTI or to NW	B	$\geq$	1.2
NWRSTI.EN.1	NP enclosure of OD	C	$\geq$	0.4
NWRSTI.EN.2	OD enclosure of CO	D	$\geq$	0.3
NWRSTI.EN.3	Enclosure of CO	E	$\geq$	0.3
NWRSTI.EX.1	OD extension on NWRSTI	F	$\geq$	0.3
NWRSTI.O.1	{NP interact with NWDMY} overlap of {PP, VTH_P, or VTL_P } (all p-type implant layers) is not allowed			
NWRSTI.R.1®	Recommend resistor length (L) $\geq$ 20um, and square number (length (L) / width (A)) $\geq$ 5 for SPICE simulation accuracy. DRC can not check square number.			
Guideline	Description			
NWRSTI.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.			

### NWRSTI

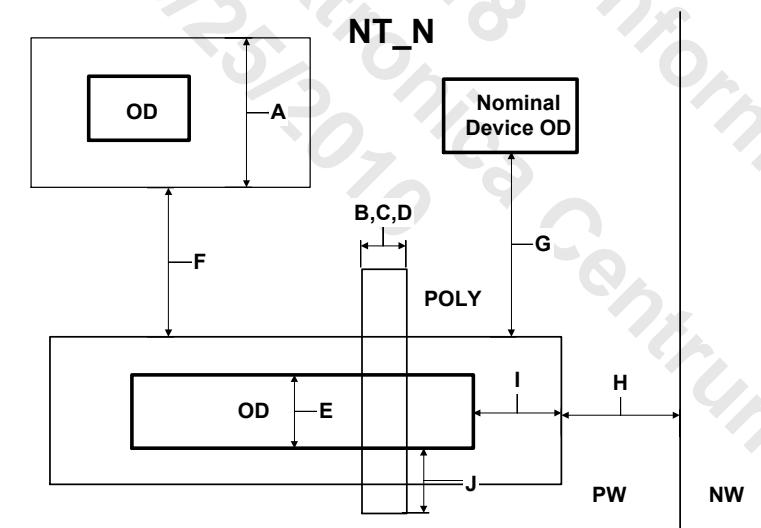


## 4.5.6 Native Device (NT\_N) Layout Rules

### NT\_N, Native NMOS Blocked Implant Definition

This layer is used to block NW and PW implant. If you use native NMOS devices in a circuit design, use this drawn layer with NW to generate PW.

Rule No.	Description	Label		Rule
NT_N.W.1	Width	A	$\geq$	0.62
NT_N.W.2	Channel length of 1.0V or 1.2V native device	B	$\geq$	0.20
NT_N.W.2.1	Channel length of 1.2V LP native device [channel width $\geq$ 1.2um]	B	$\geq$	0.33
NT_N.W.3	Channel length of 2.5V or 3.3V native device	C	$\geq$	1.20
NT_N.W.4	Channel length of 1.8V native device	D	$\geq$	0.8
NT_N.W.5	Channel width	E	$\geq$	0.5
NT_N.S.1	Space	F	$\geq$	0.62
NT_N.S.2	Space to [ACTIVE outside NT_N]	G	$\geq$	0.38
NT_N.S.3	Space to NW	H	$\geq$	1.20
NT_N.EN.1	Enclosure range of N+OD If the layout will be shrunk to be N80, you need to plot =0.285.	I	$\geq$	0.26
NT_N.EN.1			$\leq$	0.285
NT_N.EX.1	PO extension on {OD inside NT_N} (PO endcap)	J	$\geq$	0.35
NT_N.R.1	Overlap of {NW OR DNW} is not allowed			
NT_N.R.2	P+ gate is not allowed in NT_N			
NT_N.R.3	Only one OD region is allowed in NT_N <ul style="list-style-type: none"> <li>● Except NMOS capacitors with the same potential.</li> <li>● You have to draw a NCap_NTN layer to cover the NMOS capacitors. The NCap_NTN enclosure of OD have to be <math>\geq</math> 0um.</li> <li>● DRC also flags NCap_NTN and OD, which is outside of the NCap_NTN, in the same NT_N.</li> </ul>			



## 4.5.7 Thick Oxide (OD2) Layout Rules (Mask ID: 132)

Define thick oxide area of 1.8V, 2.5V, or 3.3V I/O transistors.

The OD\_33 layer (CAD layer: 15) is used for 3.3V gate oxide area.

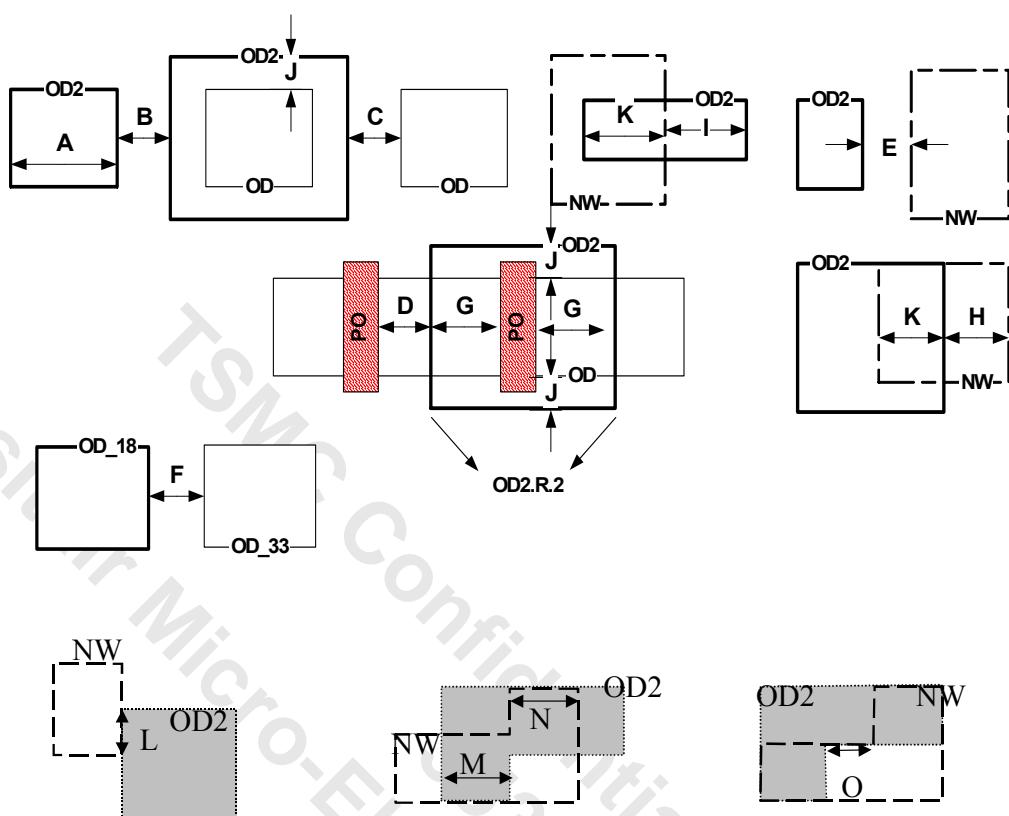
The OD\_25 layer (CAD layer: 41) is used for 2.5V gate oxide area.

The OD\_18 layer (CAD layer: 16) is used for 1.8V gate oxide area.

OD2 refers to any thick oxide device, for example, OD2 = OD\_18, OD\_25, OD\_33

Triple gate oxide is only for 1.0V/1.8V/3.3V of N90G process.

Rule No.	Description	Label		Rule
OD2.W.1	Width	A	$\geq$	0.62
OD2.W.2®	Width of {OD2 OR (NW OR NT_N)} to avoid small pattern in mask making	L	$\geq$	0.62
OD2.S.1	Space	B	$\geq$	0.62
OD2.S.2	Space to {ACTIVE OR GATE}	C	$\geq$	0.27
OD2.S.3	Space to 1.0V or 1.2V GATE	D	$\geq$	0.34
OD2.S.4	Space to NW. Space = 0 is allowed.	E	$\geq$	0.62
OD2.S.5	OD_33 space to OD_18. Space = 0 is allowed. OD_33 overlap of OD_18 is not allowed.	F	$\geq$	0.62
OD2.S.5®	Space of {NW NOT OD2} to avoid small pattern in mask making	M	$\geq$	0.62
OD2.S.6®	Space of {NW AND OD2} to avoid small pattern in mask making	O	$\geq$	0.62
OD2.S.7®	Space of {OD2 NOT (NW OR NT_N)} to avoid small pattern in mask making	N	$\geq$	0.62
OD2.EN.1	Enclosure of 1.8V, 2.5V, or 3.3V Gate in S/D direction	G	$\geq$	0.34
OD2.EX.1	NW extension on OD2. Extension = 0 is allowed.	H	$\geq$	0.62
OD2.EX.2	Extension on NW. Extension = 0 is allowed.	I	$\geq$	0.62
OD2.EX.3	Extension on {ACTIVE OR Gate}	J	$\geq$	0.27
OD2.O.1	Overlap of NW. Overlap = 0 is allowed.	K	$\geq$	0.62
OD2.R.1	OD_33 and OD_25 cannot be used on same die. OD_18 and OD_25 cannot be used on same die.			
OD2.R.2 <sup>U</sup>	If the OD is shared by core and IO, the OD must be at same potential.			

**OD2**

## 4.5.8 Poly (PO) Layout Rules (Mask ID: 130)

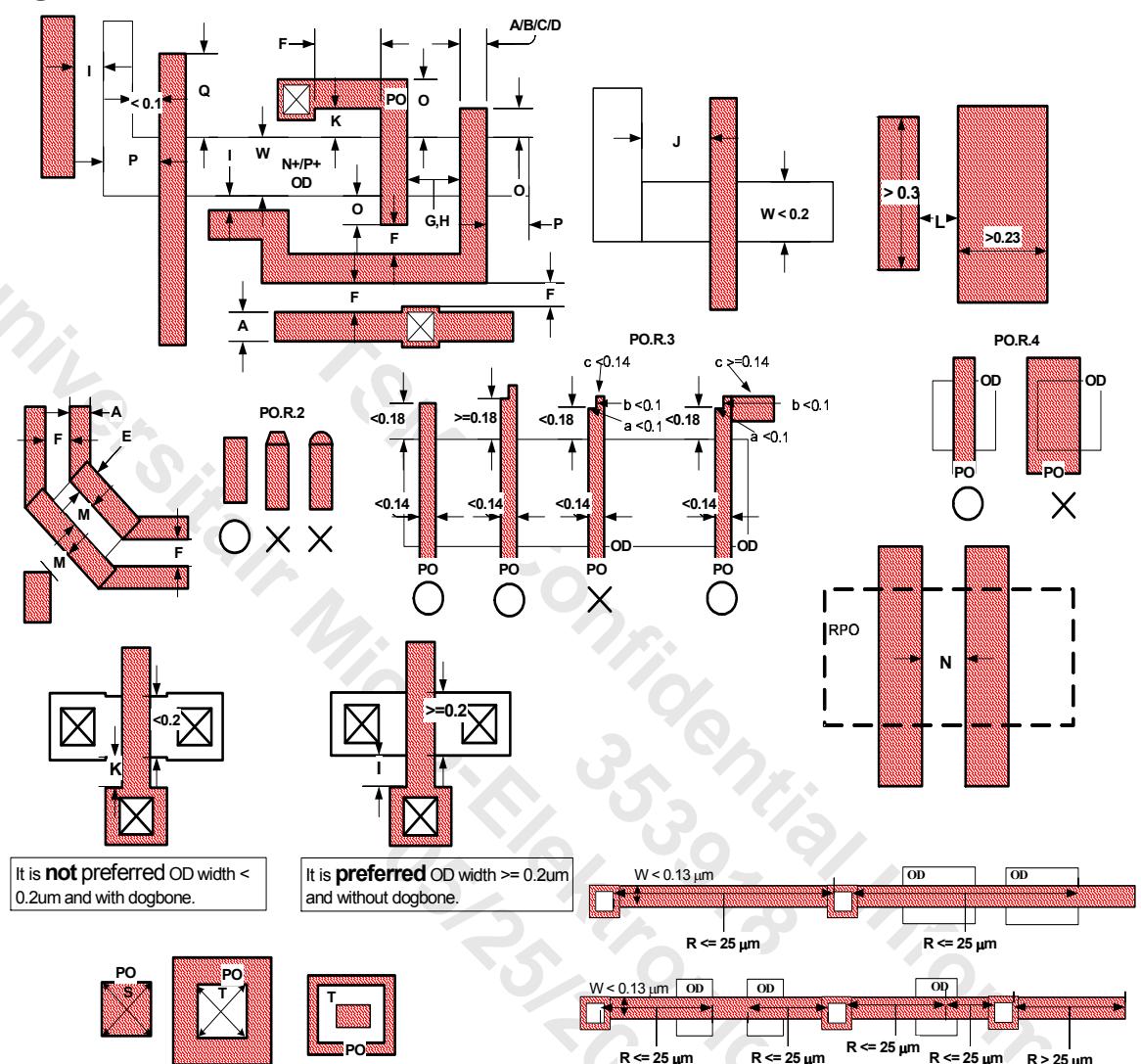
Please refer to section: 10.1.2 “ Guidelines for Optimal Electrical Model and Silicon Correlation” for more device layout guidelines.

Rule No.	Description	Label		Rule
PO.W.1	Width	A	$\geq$	0.10
PO.W.2	Channel length of 2.5V MOS	B	$\geq$	0.28
PO.W.3	Channel length of 3.3 V MOS	C	$\geq$	0.38
PO.W.4	Channel length of 1.8 V MOS	D	$\geq$	0.20
PO.W.5	Width of 45-degree FIELD PO Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)	E	$\geq$	0.19
PO.S.1	Space	F	$\geq$	0.14
PO.S.1®	Recommended minimum interconnect PO space to reduce the short possibility caused by particle	F	$\geq$	0.18
PO.S.2	GATE space in the same OD	G	$\geq$	0.15
PO.S.2®	Recommended GATE space in the same OD to avoid Isat variation	G	$\geq$	0.2
PO.S.3	{GATE inside OD2} space in the same OD	H	$\geq$	0.25
PO.S.4	FIELD PO space to OD	I	$\geq$	0.05
PO.S.5	Space to L-shape OD when PO and OD are in the same MOS [channel width (W) < 0.2 $\mu$ m]	J	$\geq$	0.10
PO.S.5®	Recommended space to L-shape OD when PO and OD are in the same MOS [channel width (W) $\geq$ 0.2 $\mu$ m and < 0.5 $\mu$ m] for stable Isat (avoid corner rounding effect)	J	$\geq$	0.10
PO.S.6	L-shape PO space to OD when PO and OD are in the same MOS [channel width (W) < 0.2 $\mu$ m].	K	$\geq$	0.10
PO.S.6®	Recommended L-shape PO space to OD when PO and OD are in the same MOS [channel width (W) $\geq$ 0.2 $\mu$ m and < 0.5 $\mu$ m] for stable Isat (avoid corner rounding effect)	K	$\geq$	0.10
PO.S.7	Space if at least one PO width is > 0.23 $\mu$ m, and the PO parallel run length is > 0.3 $\mu$ m.	L	$\geq$	0.18
PO.S.8	Space to 45-degree FIELD PO	M	$\geq$	0.19
PO.S.9	Space of {PO AND RPO}	N	$\geq$	0.25
PO.EX.1	Extension on OD (end-cap)	O	$\geq$	0.16
PO.EX.2	OD extension on PO	P	$\geq$	0.15
PO.EX.2®	Recommended OD extension on PO (full and symmetrical contact placement are recommended at both source and drain side) to avoid Isat degradation, especially for the device width > 2 $\mu$ m.	P	$\geq$	0.23
PO.EX.3	Extension on OD (end-cap) when the PO space to L-shape OD (in the same MOS) is < 0.1 $\mu$ m, and the channel width (W) is $\geq$ 0.2 $\mu$ m.	Q	$\geq$	0.18
PO.L.1	Maximum PO length between two contacts without gate, as well as the length from any point inside PO gate to nearest CO, when the PO width is < 0.13 $\mu$ m except RTMOM region (RTMOMDMY, CAD layer:155;21).	R	$\leq$	25
PO.A.1	Area	S	$\geq$	0.06
PO.A.2	Enclosed area	T	$\geq$	0.11
PO.DN.1	{PO OR DPO} density across full chip		$\geq$	14 %
PO.DN.2	{OD OR DOD OR PO OR DPO} local density		$\leq$	50%
			$\geq$	0.1%

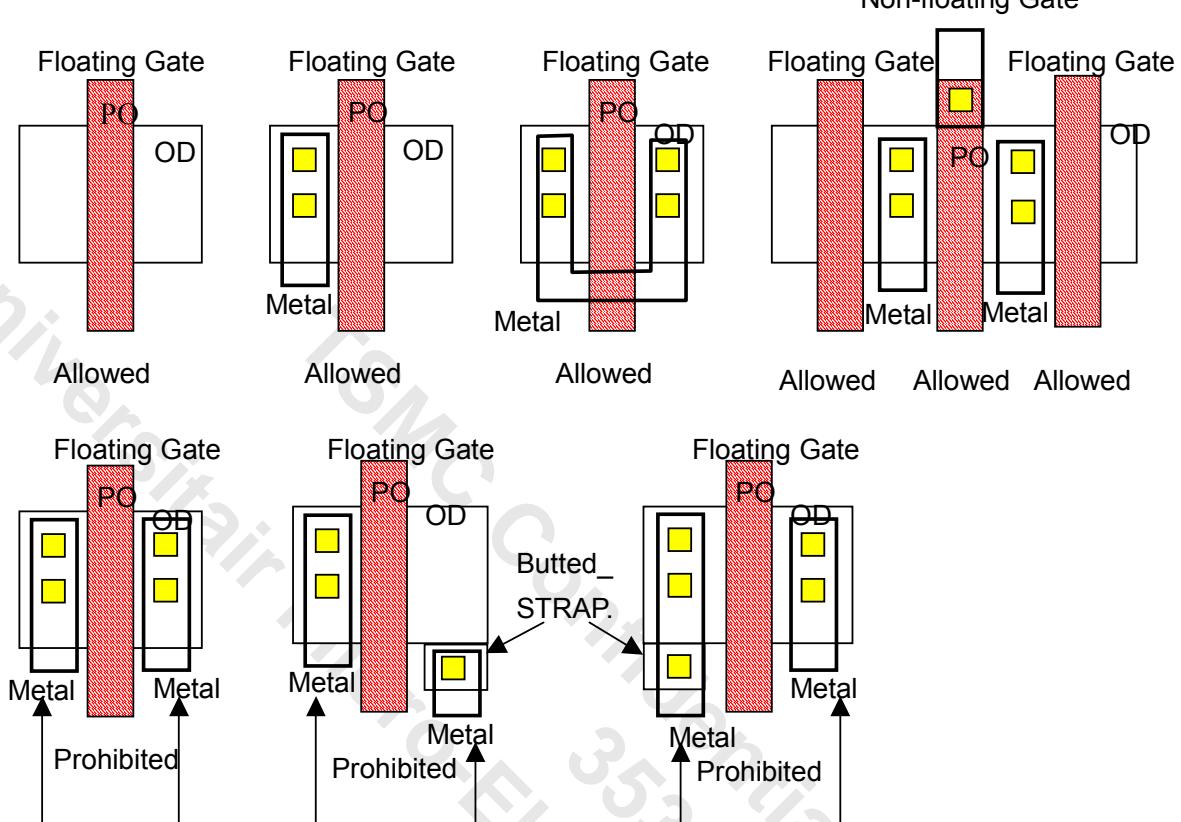
Rule No.	Description	Label	Rule
	<ol style="list-style-type: none"> <li>PO.DN.2 rules are checked over any 20 μm x 20 μm area. (stepping in 10 μm increments).</li> <li>For PO.DN.2 rules, the following regions can be excluded: <ul style="list-style-type: none"> <li>(CB sizing 2) for high speed/RF products</li> <li>ODBLK/POBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default</li> <li>Chip corner stress relief area if seal ring and stress relief pattern added by TSMC.</li> </ul> </li> <li>Even in areas covered by {ODBLK OR POBLK}, this pattern density that follows the PO.DN.2 rules is recommended.</li> </ol>		
PO.R.1	GATE must be a rectangle orthogonal to grid. (Bent GATE is not allowed).		
PO.R.2 <sup>U</sup>	PO line-end must be rectangular. Other shapes are not allowed.		
PO.R.3	No cut-out corner of any size in PO at PO end-cap [PO end-cap < 0.18 μm and channel length < 0.14 μm].		
PO.R.4	PO intersecting OD must form two or more diffusions except LOGO and RTMOM region (RTMOMDMY, CAD layer:155;21)		
PO.R.8	<p>It is prohibited for floating gate if the effective source/drain is not connected together.</p> <p>Floating gate in the DRC:</p> <ol style="list-style-type: none"> <li>Gate without Poly CO</li> <li>Gate with Poly CO but not connect to MOS OD, STRAP or PAD.</li> <li>It is not a floating gate if the Gate is connected to OD by Butted CO in SRAM bit cell.</li> </ol> <p>The effective source/drain in DRC: Source/drain is connected to different {MOSOD NOT PO}, STRAP, Gate, or PAD.</p> <p>This rule is only checked in whole chip, not in IP level.</p>		
DPO.R.1	DPO is a must. DPO CAD layer (TSMC default, 17;1) must be a different layer from the PO CAD layer. Please refer to section 6.2.		
Guideline	Description		
PO.L.1g <sup>U</sup>	Recommend to limit the maximum interconnect PO length(R) as short as possible to avoid Rs variation by salicidation		

**Table Notes:**

\* Good Poly uniformity is the key to meet the PO CD as well as circuit performance requirement. You must fill the DPO globally and uniformly even if the original drawn poly already satisfies the required poly density rule (PO.DN.1). The designer may wish to add dummy poly to improve the stability of the poly line dimension on silicon. It is recommended to manually add DPO uniformly inside regions covered by the dummy fill blocking layer POBLK, to gain better process window and electrical performance.

**PO**

## PO.R.8



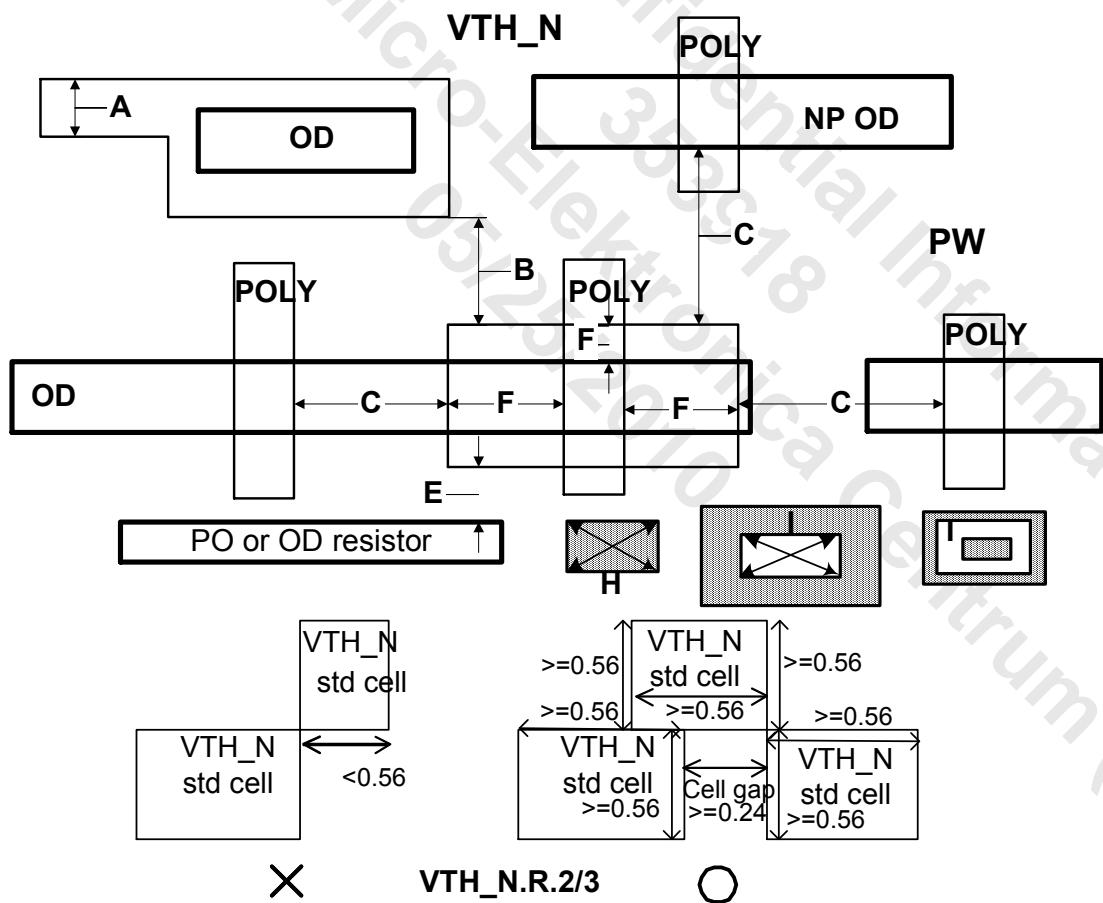
Source/drain is connected to different {MOS OD NOT PO}, STRAP, Gate, or PAD.

## 4.5.9 High Vt NMOS (VTH\_N) Layout Rules (Mask ID: 128)

### VTH\_N, 1.0V or 1.2V high Vt NMOS Implant Definition

VTH\_N is only used for 1.0V or 1.2V core devices. It is not allowed in 1.8V, 2.5V, and 3.3V I/O devices.

Rule No.	Description	Label		Rule
VTH_N.W.1	Width	A	$\geq$	0.4
VTH_N.S.1	Space	B	$\geq$	0.24
VTH_N.S.2	Space to gate	C	$\geq$	0.22
VTH_N.S.3	Space to unsilicided PO/OD	E	$\geq$	0.22
VTH_N.EN.1	Enclosure of gate	F	$\geq$	0.22
VTH_N.A.1	Area	H	$\geq$	0.4
VTH_N.A.2	Enclosed area	I	$\geq$	0.4
VTH_N.R.1	Overlap of P+ACTIVE, VTL_N, NT_N, or OD2 is not allowed.			
VTH_N.R.2	Point touch of corners of std library cells are allowed. [width $\geq$ 0.56 $\mu\text{m}$ ]			
VTH_N.R.3	One track overlap=0.28 $\mu\text{m}$ of std library cells are allowed. [width $\geq$ 0.56 $\mu\text{m}$ ]			

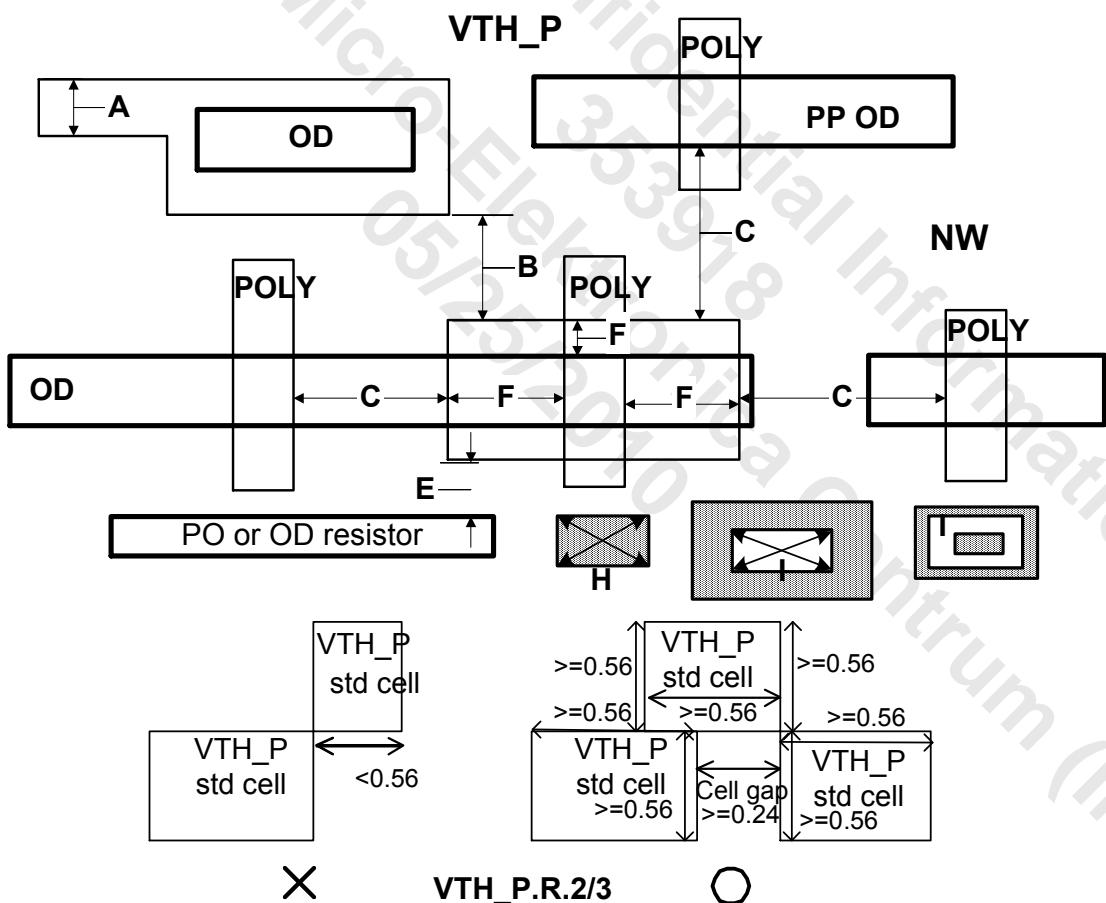


## 4.5.10 High Vt PMOS (VTH\_P) Layout Rules [G/LP(Mask ID: 127), GT(Mask ID: 125)]

### 1.0V or 1.2V High Vt PMOS Implant Definition

VTH\_P is only used for 1.0V or 1.2 V core devices. It is not allowed in 1.8V, 2.5V, or 3.3V I/O devices.

Rule No.	Description	Label		Rule
VTH_P.W.1	Width	A	$\geq$	0.40
VTH_P.S.1	Space	B	$\leq$	0.24
VTH_P.S.2	Space to gate	C	$\leq$	0.22
VTH_P.S.3	Space to unsilicided PO/OD	E	$\leq$	0.22
VTH_P.EN.1	Enclosure of gate	F	$\leq$	0.22
VTH_P.A.1	Area	H	$\leq$	0.40
VTH_P.A.2	Enclosed area	I	$\leq$	0.40
VTH_P.R.1	Overlap of N+ACTIVE, VTL_P, NT_N, or OD2 is not allowed.			
VTH_P.R.2	Point touch of corners of std library cells are allowed. [width $\geq$ 0.56 $\mu$ m]			
VTH_P.R.3	One track overlap=0.28 $\mu$ m of std library cells are allowed. [width $\geq$ 0.56 $\mu$ m]			



## 4.5.11 Low Vt NMOS (VTL\_N) Layout Rules [G(Mask ID: 118)/ GT]

G process (1.0V core device) uses VTL\_N mask to process LVT device.

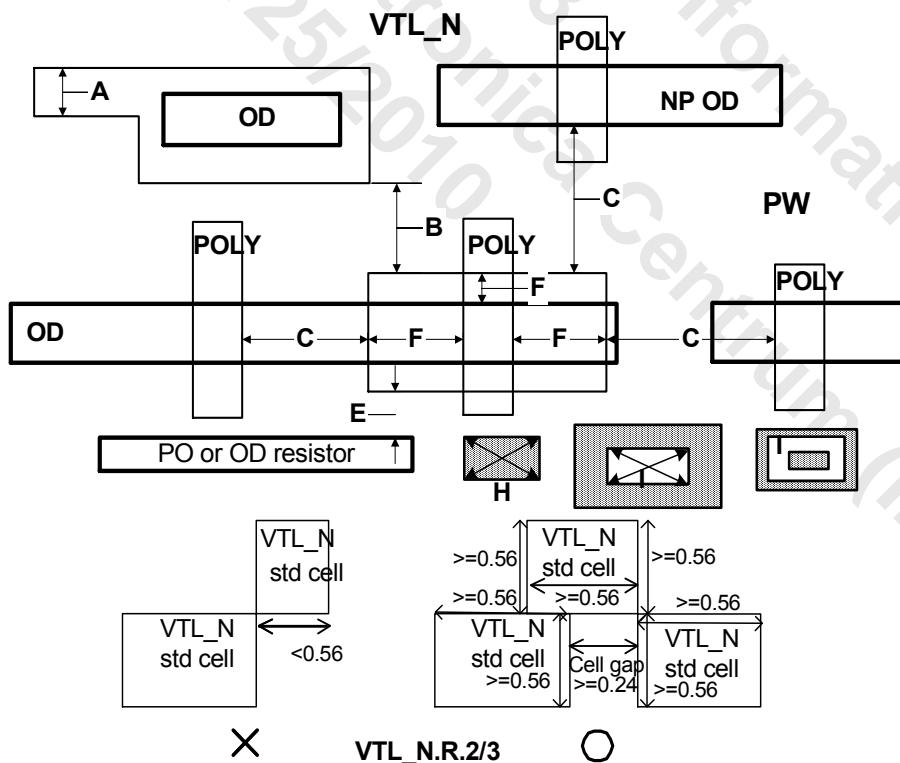
GT process (1.2V core device) uses logic operation by shrinking PO gate dimension to process LVT device.

You must provide VTL\_N to TSMC to performance logic operation during mask making.

VTL\_N is not allowed in 1.8V, 2.5V, and 3.3V I/O devices.

Core	Technology	
	G (1.0V)	GT (1.2V)
VTL_N (mask ID: 118) implant	Yes	No
GDS layer name (number) to tape out VTL_N mask	VTL_N (12)	No
Logical operation to push PO gate dimension	No	Yes
GDS layer name (number) in PO logical operation to recognize low Vt device	No	VTL_N (12)

Rule No.	Description	Label	Rule
VTL_N.W.1	Width	A	$\geq 0.40$
VTL_N.S.1	Space	B	$\geq 0.24$
VTL_N.S.2	Space to gate	C	$\geq 0.22$
VTL_N.S.3	Space to unsilicidized PO/OD	E	$\geq 0.22$
VTL_N.EN.1	Enclosure of gate	F	$\geq 0.22$
VTL_N.A.1	Area	H	$\geq 0.40$
VTL_N.A.2	Enclosed area	I	$\geq 0.40$
VTL_N.R.1	Overlap of P+ACTIVE, VTH_N, NT_N, or OD2 is not allowed.		
VTL_N.R.2	Point touch of corners of std library cells are allowed. [width $\geq 0.56 \mu\text{m}$ ]		
VTL_N.R.3	One track overlap=0.28 $\mu\text{m}$ of std library cells are allowed. [width $\geq 0.56 \mu\text{m}$ ]		



## 4.5.12 Low Vt PMOS (VTL\_P) Layout Rules [G(Mask ID: 117)/ GT]

G process (1.0V core device) uses VTL\_P mask to process LVT device.

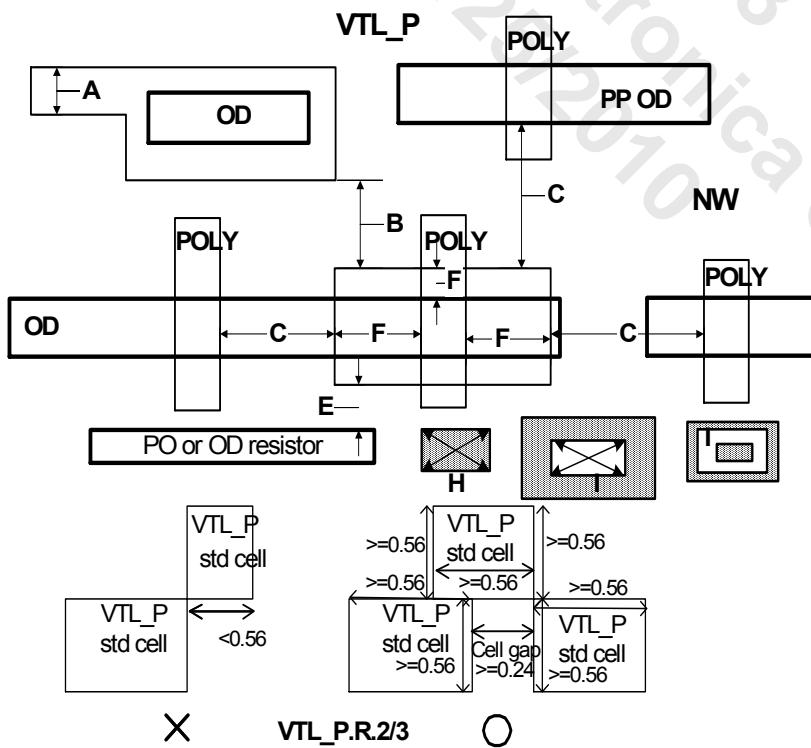
GT process (1.2V core device) uses logic operation by shrinking PO gate dimension to process LVT device.

You must provide VTL\_P to TSMC to performance logic operation during mask making.

VTL\_P is not allowed in 1.8V, 2.5V, and 3.3V I/O devices.

Core	Technology	
	G (1.0V)	GT (1.2V)
VTL_P(mask ID:117) implant	Yes	No
GDS layer name (number) to tape out VTL_P mask	VTL_P (13)	No
Logical operation to push PO gate dimension	No	Yes
GDS layer name (number) in PO logical operation to recognize low Vt device	No	VTL_P (13)

Rule No.	Description	Label		Rule
VTL_P.W.1	Width	A	$\geq$	0.40
VTL_P.S.1	Space	B	$\geq$	0.24
VTL_P.S.2	Space to gate	C	$\geq$	0.22
VTL_P.S.3	Space to unsilicided PO/OD	E	$\geq$	0.22
VTL_P.EN.1	Enclosure of gate	F	$\geq$	0.22
VTL_P.A.1	Area	H	$\geq$	0.40
VTL_P.A.2	Enclosed area	I	$\geq$	0.40
VTL_P.R.1	Overlap of N+ACTIVE, VTH_P, NT_N, or OD2 is not allowed.			
VTL_P.R.2	Point touch of corners of std library cells are allowed. [width $\geq$ 0.56 $\mu$ m]			
VTL_P.R.3	One track overlap=0.28 $\mu$ m of std library cells are allowed. [width $\geq$ 0.56 $\mu$ m]			



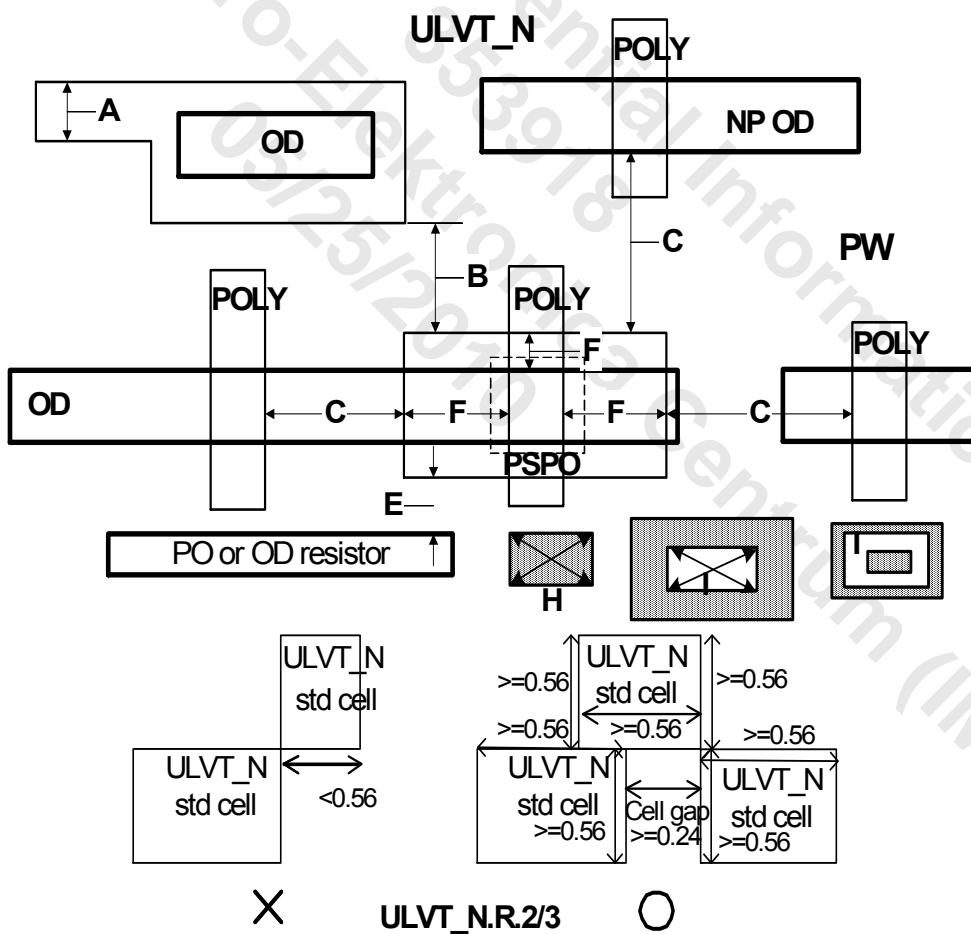
## 4.5.13 Ultra Low Vt NMOS (ULVT\_N) Layout Rules (Mask ID: 11R)

### ULVT\_N (CAD layer: 151;0), ultra low Vt NMOS Implant Definition

ULVT\_N is only used for core devices for N90LP/N85LP. It is not allowed in I/O devices (1.8/2.5V/3.3V).

ULVT\_N is only used for core devices for N80GC, please refer to T-N80-CL-DR-008.

Rule No.	Description	Label	Rule
ULVT_N.W.1	Width	A	$\geq$ 0.40
ULVT_N.S.1	Space	B	$\geq$ 0.24
ULVT_N.S.2	Space to gate	C	$\geq$ 0.22
ULVT_N.S.3	Space to unsilicided PO/OD	E	$\geq$ 0.22
ULVT_N.EN.1	Enclosure of gate	F	$\geq$ 0.22
ULVT_N.A.1	Area	H	$\geq$ 0.40
ULVT_N.A.2	Enclosed area	I	$\geq$ 0.40
ULVT_N.R.1	Overlap of P+ACTIVE, VTH_N, NT_N, or OD2 is not allowed.		
ULVT_N.R.2	Point touch of corners of standard library cells are allowed. [width $\geq$ 0.56 $\mu\text{m}$ ]		
ULVT_N.R.3	One track overlap=0.28 $\mu\text{m}$ of standard library cells are allowed. [width $\geq$ 0.56 $\mu\text{m}$ ]		
ULVT_N.R.4	{ULVT_N AND GATE} must inside PSPO		



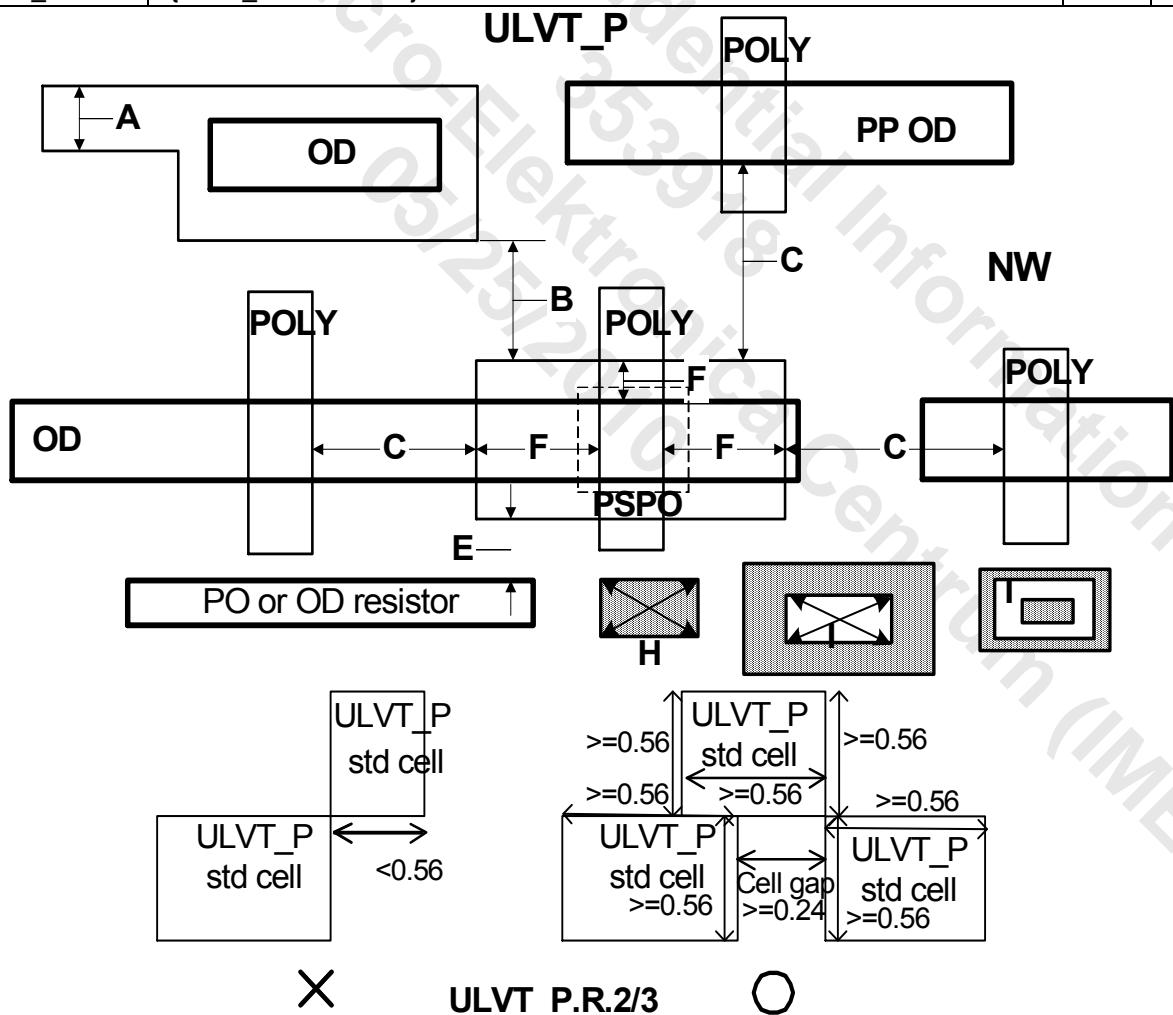
## 4.5.14 Ultra Low Vt PMOS (ULVT\_P) Layout Rules (Mask ID: 11Q)

### ULVT\_P (CAD layer: 152;0), ultra low Vt PMOS Implant Definition

ULVT\_P is only used for core devices N90LP/N85LP. It is not allowed in I/O devices (1.8/2.5V/3.3V).

ULVT\_P is only used for core devices for N80GC, please refer to T-N80-CL-DR-008.

Rule No.	Description	Label	Rule
ULVT_P.W.1	Width	A	$\geq$ 0.40
ULVT_P.S.1	Space	B	$\geq$ 0.24
ULVT_P.S.2	Space to gate	C	$\geq$ 0.22
ULVT_P.S.3	Space to unsilicidized PO/OD	E	$\geq$ 0.22
ULVT_P.EN.1	Enclosure of gate	F	$\geq$ 0.22
ULVT_P.A.1	Area	H	$\geq$ 0.40
ULVT_P.A.2	Enclosed area	I	$\geq$ 0.40
ULVT_P.R.1	Overlap of N+ACTIVE, VTH_P, NT_N, or OD2 is not allowed.		
ULVT_P.R.2	Point touch of corners of std library cells are allowed. [width $\geq$ 0.56 $\mu$ m]		
ULVT_P.R.3	One track overlap=0.28 $\mu$ m of std library cells are allowed. [width $\geq$ 0.56 $\mu$ m]		
ULVT_P.R.4	{ULVT_P AND GATE} must inside PSPO		

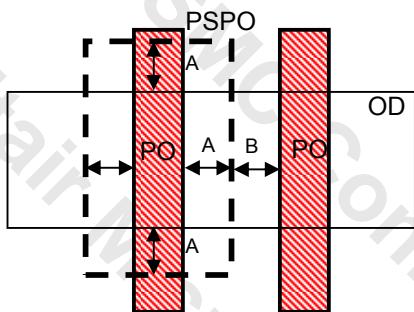


## 4.5.15 PSPO Layout Rules for LP Low Vt

PSPO: You must provide this layer (CAD layer: 17;51) to generate poly logical operation in LP low Vt process.  
If Your LP low Vt design follows G/GT low Vt rule, you can merge VTL\_N/VTL\_P as PSPO directly.

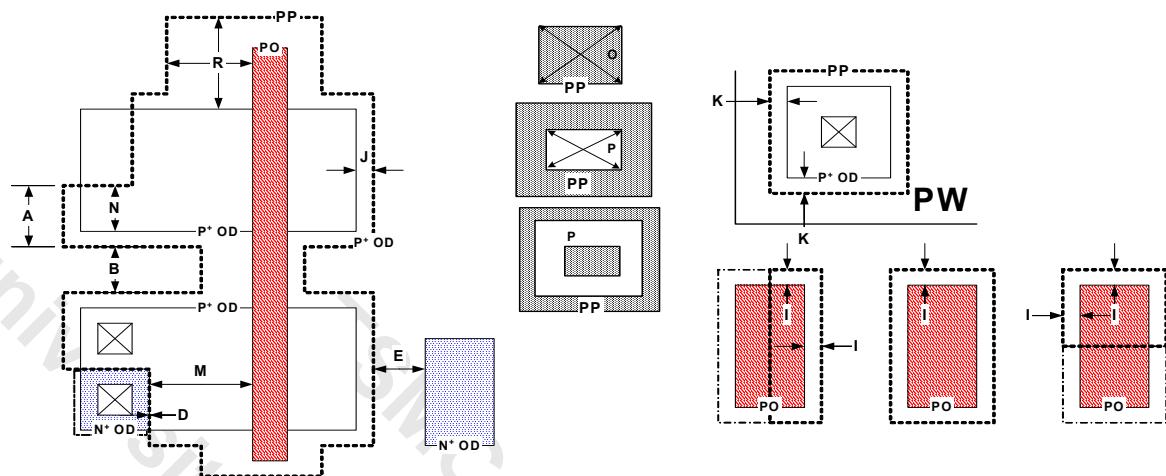
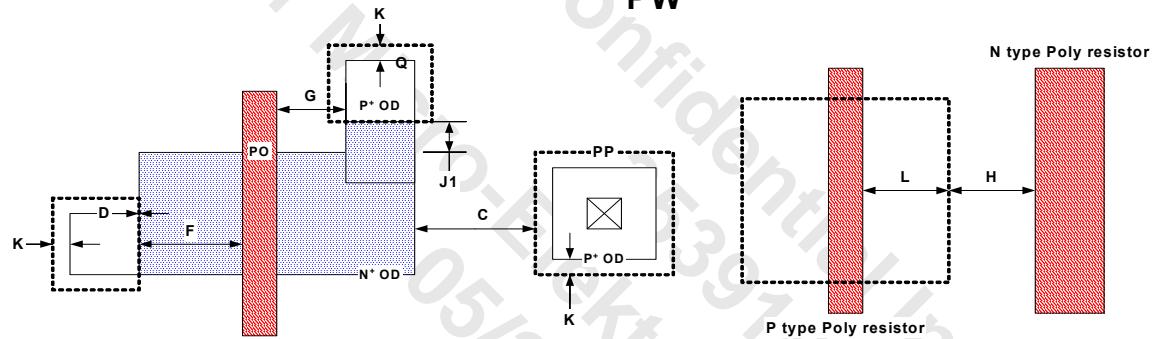
Rule No.	Description	Label		Rule
PSPO.EN.1	Enclosure of gate	A	$\leq$	0.05
PSPO.S.1	Space to gate	B	$\geq$	0.05
PSPO.R.1	Overlap of VTH_N, VTH_P, NT_N, or OD2 is not allowed.			

### PSPO



## 4.5.16 P+ Source/Drain Ion Implantation (PP) Layout Rules (Mask ID: 197)

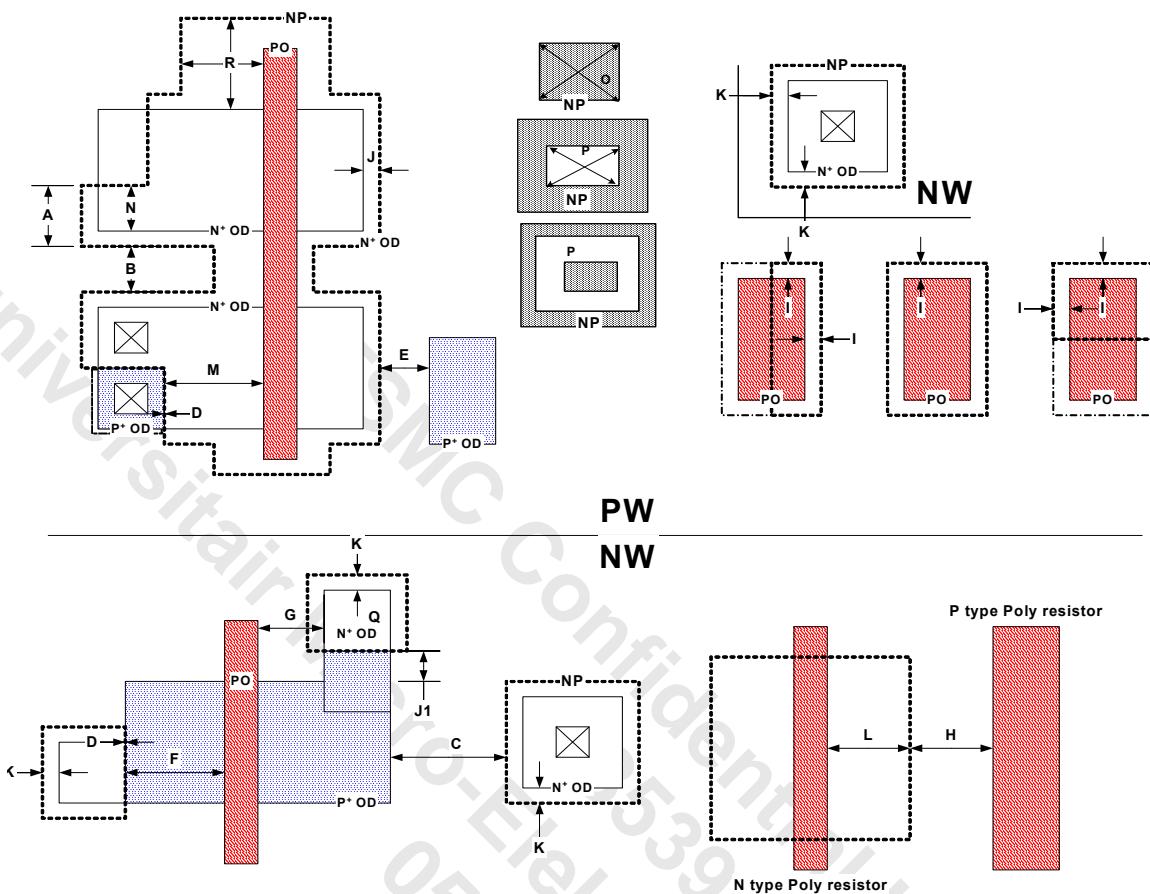
Rule No.	Description	Label		Rule
PP.W.1	Width	A	$\geq$	0.24
PP.S.1	Space	B	$\geq$	0.24
PP.S.2	Space to N+ACTIVE (non-butted)	C	$\geq$	0.13
PP.S.3	Space to {N+ACTIVE OR NW STRAP} (butted)	D	=	0.00
PP.S.4	Space to NW STRAP (non-butted)	E	$\geq$	0.02
PP.S.5	{PP edge on OD} space to NMOS GATE	F	$\geq$	0.32
PP.S.6	Butted PW STRAP space to PO in the same OD [the butted N+ ACTIVE extending $0 < J1 < 0.22 \mu\text{m}$ ]	G	$\geq$	0.32
PP.S.7	Space to N-type unsilicided OD/PO	H	$\geq$	0.20
PP.EN.1	{NP OR PP} enclosure of PO (except DPO/LOGO)	I	$\geq$	0.20
PP.EX.1	Extension on P+ACTIVE (except SBDDMY region)	J	$\geq$	0.13
PP.EX.2	Extension on PW STRAP	K	$\geq$	0.02
PP.EX.3	Extension on P-type unsilicided OD/PO	L	$\geq$	0.20
PP.EX.4	{PP edge on OD} extension on PMOS GATE	M	$\geq$	0.32
PP.O.1	Overlap of OD	N	$\geq$	0.13
PP.A.1	Area	O	$\geq$	0.122
PP.A.2	Enclosed area	P	$\geq$	0.122
PP.A.3	Area of butted PW STRAP	Q	$\geq$	0.04
PP.R.1	PP must fully cover {PMOS GATE SIZING $0.22 \mu\text{m}$ }	R	$\geq$	0.22
PP.R.2	Overlap of NP is not allowed.			
PP.R.3	OD must be fully covered by {NP OR PP} (except DOD/SBDDMY region).			

**PP****NW  
PW**

## 4.5.17 N+ Source/Drain Ion Implantation (NP) Rules (Mask ID: 198)

Rule No.	Description	Label		Rule
NP.W.1	Width	A	$\geq$	0.24
NP.S.1	Space	B	$\geq$	0.24
NP.S.2	Space to P+ACTIVE (non-butted)	C	$\geq$	0.13
NP.S.3	Space to {P+ACTIVE OR PW STRAP} (butted)	D	=	0.00
NP.S.4	Space to PW STRAP (non-butted)	E	$\geq$	0.02
NP.S.5	{NP edge on OD} space to PMOS GATE	F	$\geq$	0.32
NP.S.6	Butted NW STRAP space to PO in the same OD [the butted P+ ACTIVE extending $0 < J1 < 0.22 \mu\text{m}$ ]	G	$\geq$	0.32
NP.S.7	Space to P-type unsilicided OD/PO	H	$\geq$	0.20
NP.EN.1	{NP OR PP} enclosure of PO (except DPO/LOGO)	I	$\geq$	0.20
NP.EX.1	Extension on N+ACTIVE	J	$\geq$	0.13
NP.EX.2	Extension on NW STRAP	K	$\geq$	0.02
NP.EX.3	Extension on N-type unsilicided OD/PO	L	$\geq$	0.20
NP.EX.4	{NP edge on OD} extension on NMOS GATE	M	$\geq$	0.32
NP.O.1	Overlap of OD	N	$\geq$	0.13
NP.A.1	Area	O	$\geq$	0.122
NP.A.2	Enclosed area	P	$\geq$	0.122
NP.A.3	Area of butted NW STRAP	Q	$\geq$	0.04
NP.R.1	NP must fully cover {NMOS GATE SIZING 0.22 $\mu\text{m}$ }.	R	$\geq$	0.22
NP.R.2	Overlap of PP is not allowed.			
NP.R.3	OD must be fully covered by {NP OR PP} (except DOD and SBDDMY region).			

NP



## 4.5.18 Layout Rules for LDD Mask Logical Operations

### N1V/N2V/P1V/P2V(/N3V/P3V for TGO) and VTC\_N/VTL\_N/VTL\_P

As a default, TSMC generates some masking layers from drawn layers by logical operations. By default, these include N1V/N2V/P1V/P2V (/N3V/P3V for TGO) and VTC\_N/VTL\_N/VTL\_P masks. The following rules and recommendations (Fig. 1-Fig. 6) are defined to avoid small patterns during mask making.

**Warning:**



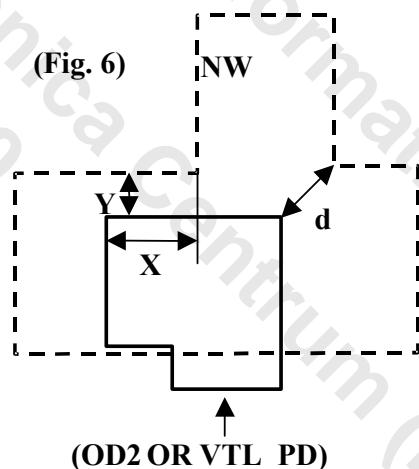
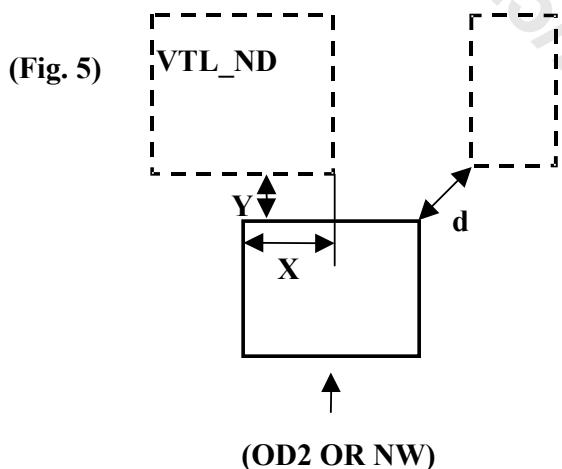
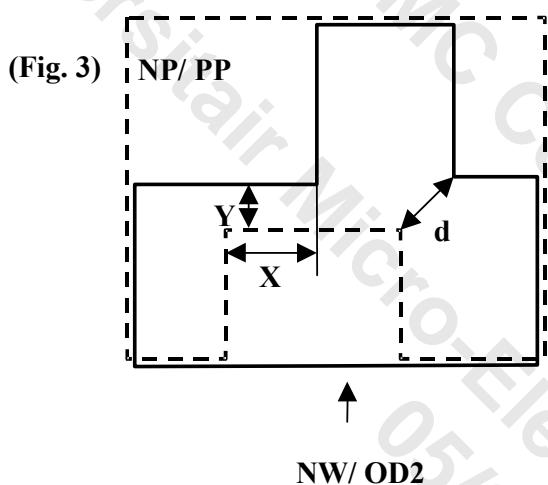
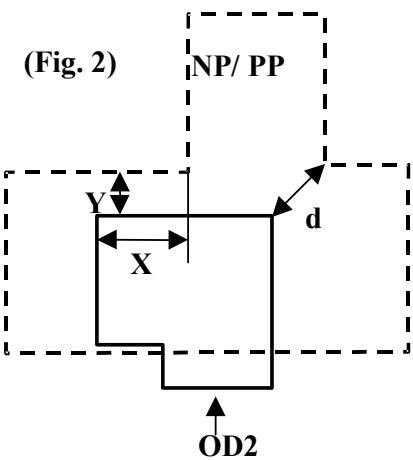
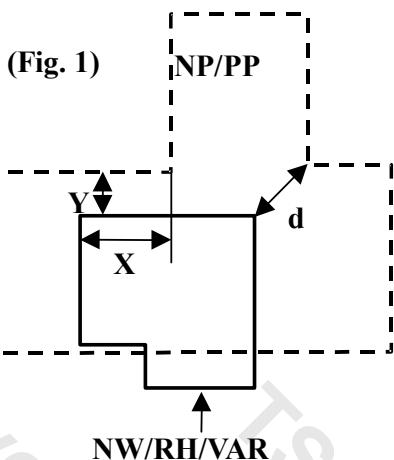
If the rules is not followed, the mask making cycle time will be seriously impacted.

The following are special requirements.

<b>D ≥ 0.24 μm</b>	The minimum extension/clearance between two corners of two layers
<b>X/Y (the extension/clearance between two edges of two layers in an X/Y)</b>	If either dimension X or Y < 0.24 μm (including 0, 2 edges aligned), the other dimension must be ≥ 0.24 μm.
<b>VTL_ND (VTL_N SIZING – 0.06)</b>	VTL_N is sized down by 0.06 μm.
<b>VTL_PD (VTL_P SIZING – 0.06)</b>	VTL_P is sized down by 0.06 μm.

Rule No.	Description			Rule
LDN.EX.1	NP extension on NW	Fig.1	≥	0.24
LDN.EX.2	NP extension on OD2	Fig.2	≥	0.24
LDN.EX.3	NP extension on RH	Fig.1	≥	0.24
LDN.EX.4	NP extension on VAR	Fig.1	≥	0.24
LDN.O.1	NP overlap of OD2	Fig.3	≥	0.24
LDP.EX.1	PP extension on OD2	Fig.2	≥	0.24
LDP.EX.2	PP extension on RH	Fig.1	≥	0.24
LDP.EX.3	PP extension on VAR	Fig.1	≥	0.24
LDP.O.1	PP overlap of NW	Fig.3	≥	0.24
LDP.O.2	PP overlap of OD2	Fig.3	≥	0.24
VT.S.1	VTL_ND space to {OD2 OR NW}	Fig.5	≥	0.24
VT.EX.2	NW extension on {OD2 OR VTL_PD}	Fig.6	≥	0.24

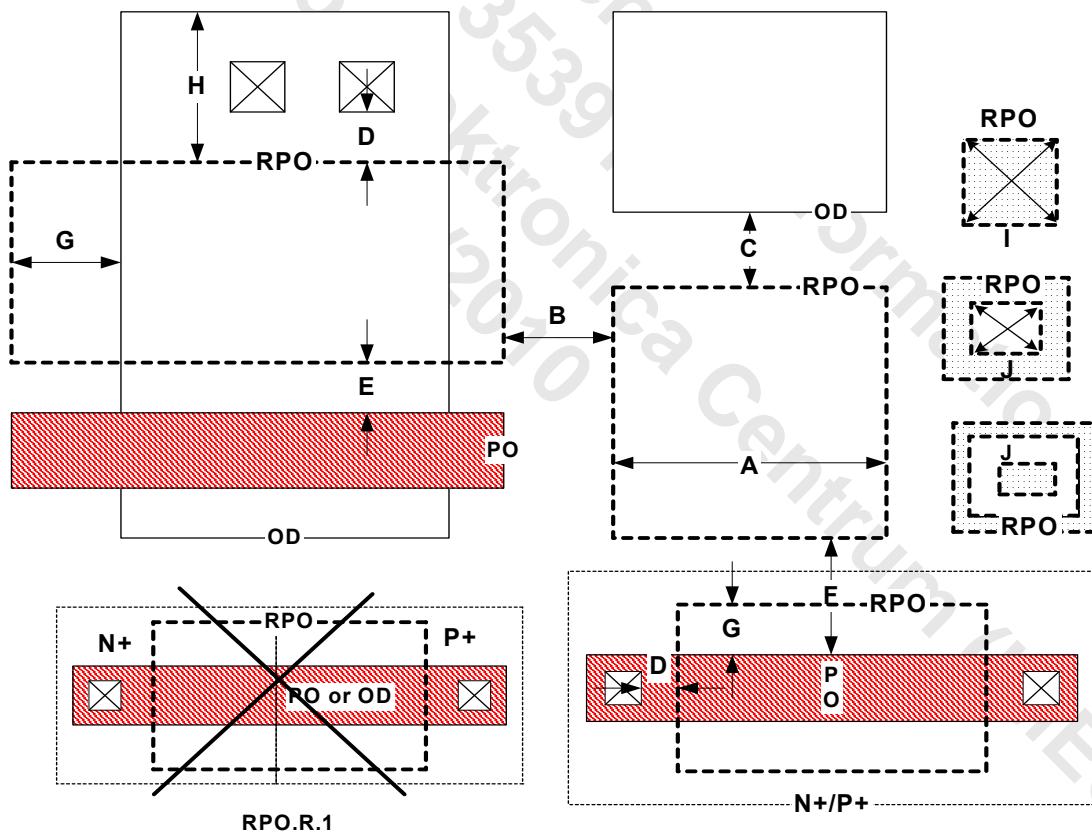
In DRC deck, we use proper sizing to reduce DRC false error.



## 4.5.19 Resist Protection Oxide (RPO) Layout Rules (Mask ID: 155)

Rule No.	Description	Label		Rule
RPO.W.1	Width	A	$\geq$	0.43
RPO.S.1	Space	B	$\geq$	0.43
RPO.S.2	Space to OD	C	$\geq$	0.22
RPO.S.3	Space to CO (overlap of CO is not allowed.)	D	$\geq$	0.22
RPO.S.4	Space to GATE (overlap of GATE is not allowed except ESD circuit.)	E	$\geq$	0.38
RPO.S.5	Space to PO	F	$\geq$	0.30
RPO.EX.1	Extension on unsilicided OD/PO	G	$\geq$	0.22
RPO.EX.2	OD extension on RPO	H	$\geq$	0.22
RPO.EX.3	Extension on unsilicided OD/PO [RPO both width and length >10 µm]	G	$\geq$	0.30
RPO.A.1	Area	I	$\geq$	1.00
RPO.A.2	Enclosed area	J	$\geq$	1.00
RPO.R.1	Butted NP/PP on unsilicided OD/PO is not allowed.			

### RPO



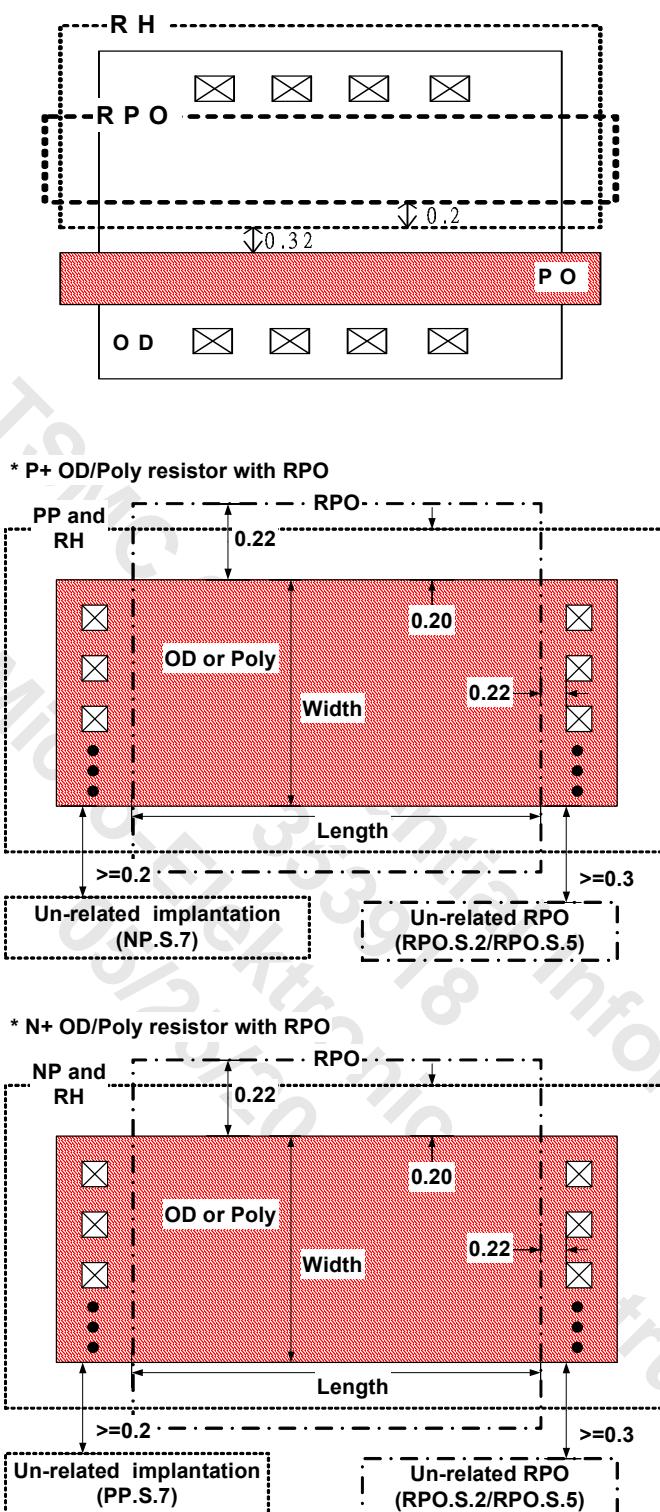
## 4.5.20 OD and Poly Resistor Guidelines

RH layer is required for OD and poly resistors. RH layer is a dummy layer that blocks NLDD or PLDD implants in the logic operations that generate N1V, N2V, P1V, and P2V.

Unsilicided OD resistor: {RH AND (RPO AND OD)}

Unsilicided PO resistor: {RH AND (RPO AND PO)}

<b>Guidelines for Dimensions</b>		
<b>RES.2g</b>	<b>Minimum width(W), length(L) and square number (L/W) for unsilicided OD/PO resistor in SPICE:</b>	Width $\geq 0.4 \mu\text{m}$ (Checked by DRC) Length $\geq 0.8 \mu\text{m}$ (Checked by DRC) Square number $\geq 1$ (Not checked by DRC)
<b>RES.10g</b>	<b>For unsilicided OD/PO resistor</b>	RH enclosure of unsilicided OD/PO resistor $\geq 0.2 \mu\text{m}$
<b>Other Guidelines</b>		
<b>RES.8g</b>	<b>For unsilicided OD resistor in the source or drain of MOS</b>	RH space to Gate $\geq 0.32 \mu\text{m}$ in source or drain direction.
<b>RES.9g</b>		RH extension on {RPO AND OD} $\geq 0.20 \mu\text{m}$
<b>RES.13g</b>	<b>For unsilicided PO resistor</b>	{RPO AND PO} must be fully covered by RH (except BJT or ESD circuits)
<b>RES.14g</b>	<b>For unsilicided OD resistor</b>	{RPO AND OD} must be fully covered by RH (except BJT or ESD circuits)
<b>RES.16g<sup>U</sup></b>	Recommended to use rectangle shape resistor for the SPICE simulation accuracy	
<b>Rules</b>		
<b>RES.8</b>	<b>For unsilicided OD/PO resistor</b>	RH space to Gate $\geq 0.22 \mu\text{m}$ (Overlap is not allowed.)
<b>RES.11</b>	<b>For unsilicided PO resistor</b>	RPO intersecting (PO AND RH) must form two or more POs (except BJT or ESD circuits)
<b>RES.12</b>	<b>For unsilicided OD resistor</b>	RPO intersecting (OD AND RH) must form two or more ODs (except BJT or ESD circuits)



**The Following table describes the resistance performance and variation with sampled width/length:**

1. The data is an example based on CLN90G SPICE model: T-N90-LO-SP-002 (V1.4) with the bias condition of 0.01V. Make sure to refer the most updated SPICE model version of each different technology to design your resistor.
2. It contains one typical case (TT) and two corner cases, slow (SS) and fast (FF).

Resistor	W (μm)	L (μm)	SQ (L/W)	TT (ohm)	SS (ohm)	FF (ohm)	TT/SS Diff	TT/FF Diff
<b>Unsilicided N+OD resistor</b>	2.0	4.0	2.0	196.9	237.0	157.9	20.38%	-19.78%
	1.0	2.0	2.0	207.6	260.1	157.8	25.26%	-24.00%
	0.7	1.4	2.0	216.7	280.1	157.7	29.23%	-27.25%
	0.4	0.8	2.0	239.5	332.1	157.4	38.64%	-34.28%
	2.0	10.0	5.0	479.7	569.2	393.5	18.64%	-17.97%
	1.0	5.0	5.0	494.6	604.7	391.9	22.25%	-20.77%
	0.7	3.5	5.0	507.4	636.1	390.5	25.36%	-23.05%
	0.4	2.0	5.0	539.8	719.7	387.1	33.31%	-28.29%
<b>Unsilicided P+OD resistor</b>	2.0	4.0	2.0	339.5	439.2	241.7	29.35%	-28.82%
	1.0	2.0	2.0	374.3	497.9	254.6	33.04%	-31.98%
	0.7	1.4	2.0	404.3	548.9	265.7	35.77%	-34.28%
	0.4	0.8	2.0	480.1	679.1	293.6	41.43%	-38.86%
	2.0	10.0	5.0	804.3	1026.6	586.4	27.65%	-27.09%
	1.0	5.0	5.0	846.2	1101.4	600.8	30.16%	-29.00%
	0.7	3.5	5.0	882.5	1166.8	613.2	32.21%	-30.52%
	0.4	2.0	5.0	974.9	1336.3	644.2	37.07%	-33.92%
<b>Unsilicided N+PO resistor</b>	2.0	4.0	2.0	204.5	249.8	160.4	22.15%	-21.60%
	1.0	2.0	2.0	230.8	296.0	168.6	28.22%	-26.96%
	0.7	1.4	2.0	254.4	338.0	176.0	32.84%	-30.85%
	0.4	0.8	2.0	319.3	457.2	196.1	43.19%	-38.58%
	2.0	10.0	5.0	488.5	582.0	397.8	19.13%	-18.58%
	1.0	5.0	5.0	531.9	654.8	415.7	23.12%	-21.84%
	0.7	3.5	5.0	571.8	723.4	477.9	26.50%	-16.43%
	0.4	2.0	5.0	686.2	929.8	486.3	35.51%	-29.13%
<b>Unsilicided P+PO resistor</b>	2.0	4.0	2.0	924.8	1120.4	734.3	21.15%	-20.60%
	1.0	2.0	2.0	1048.4	1323.5	785.8	26.24%	-25.04%
	0.7	1.4	2.0	1157.0	1504.6	830.6	30.05%	-28.21%
	0.4	0.8	2.0	1441.5	1995.6	945.6	38.44%	-34.41%
	2.0	10.0	5.0	2182.0	2593.0	1783.7	18.84%	-18.25%
	1.0	5.0	5.0	2360.9	2892.6	1860.5	22.52%	-21.19%
	0.7	3.5	5.0	2520.9	3167.2	1927.9	25.64%	-23.52%
	0.4	2.0	5.0	2953.7	3948.9	2103.8	33.69%	-28.77%

## 4.5.21 MOS Varactor Layout Rules (VAR)

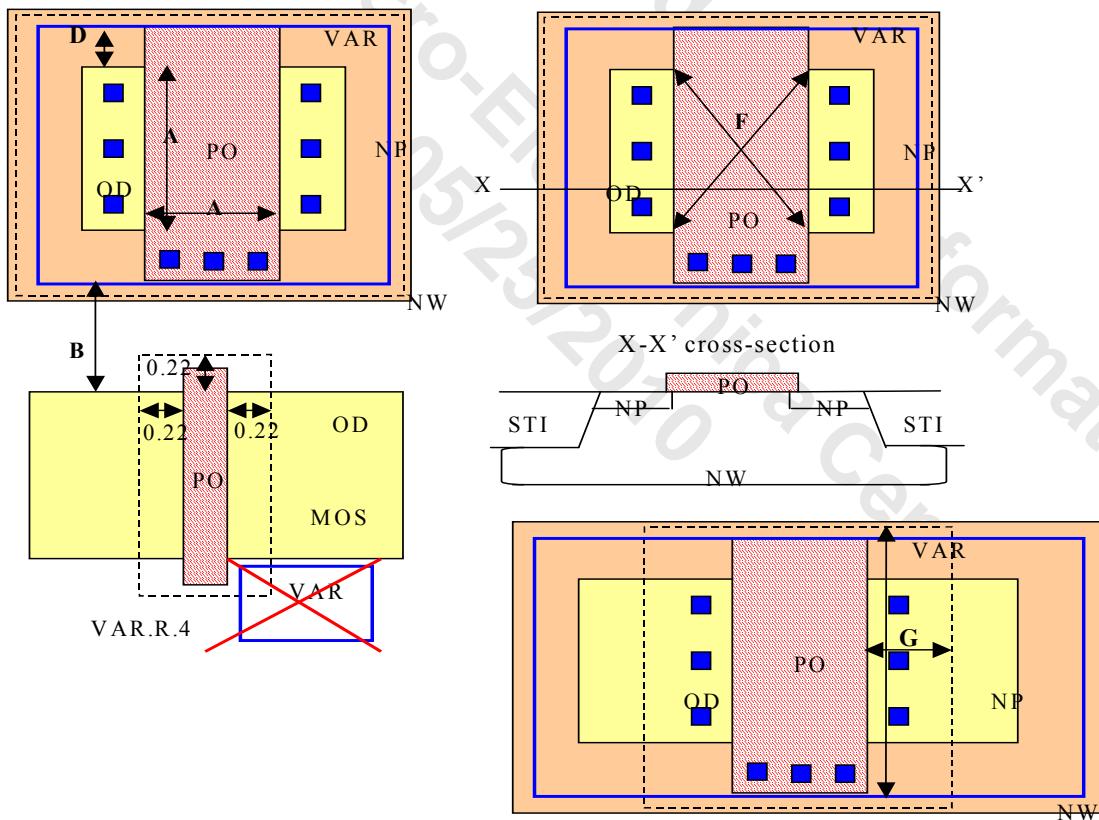
MOS varactor provides NMOS in NW capacitor structure for core and I/O region.

VAR: You must provide this layer (CAD layer: 143) to generate LDD logical operation, if the MOS varactor is used.

Rule No.	Description	Label	Rule
VAR.W.1	Width of {gate AND VAR}.	A	$\geq$ 0.4
VAR.S.1	Space to ACTIVE	B	$\geq$ 0.13
VAR.EN.1	Enclosure of OD	D	$\geq$ 0.22
VAR.A.1®	Recommended area of {gate AND VAR} for SPICE simulation accuracy. In SPICE model, $0.4\mu\text{m} \times 1.6\mu\text{m}$ is used for minimum area of {gate AND VAR}.	F	$\geq$ 0.64
VAR.R.1	VAR layer must be drawn to fully cover the varactor devices.		
VAR.R.2	Overlap of VTL_N, VTL_P, VTH_N, VTH_P, NT_N, PSPO, PW, or RPO is not allowed.		
VAR.R.3	PP overlap of {gate AND VAR} is not allowed.		
VAR.R.4	Overlap to {(PO AND ACTIVE) SIZING 0.22 $\mu\text{m}$ } is not allowed		
VAR.R.5	NP must fully cover {{{(VAR AND GATE) sizing 0.19) AND OD) sizing 0.13}}	G	

**Table note:** Due to the intrinsic gate leakage, you need to do SPICE simulation carefully while large area of MOS varactor is designed in the thin oxide area.

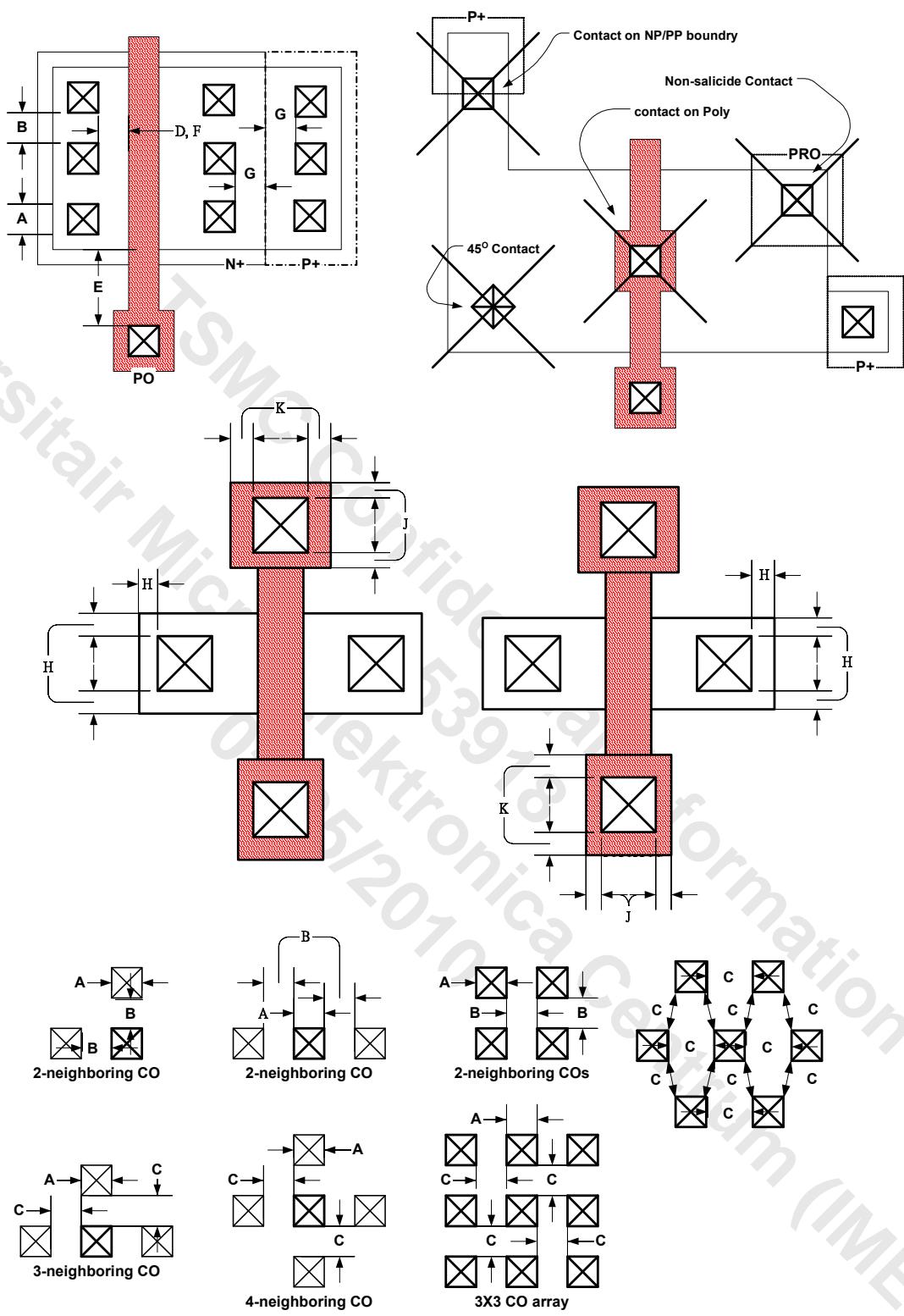
### VAR



## 4.5.22 Contact (CO) Layout Rules (Mask ID: 156)

Rule No.	Description	Label		Rule
CO.W.1	Width (square) (maximum = minimum )	A	=	0.12
CO.W.2	Width of CO bar. CO bar is only allowed in seal ring.		=	0.12
CO.S.1	Space	B	$\geq$	0.14
CO.S.2	Space to 3-neighboring CO (< 0.18 $\mu\text{m}$ distance)	C	$\geq$	0.16
CO.S.3	{CO inside OD} space to GATE (Overlap of GATE is not allowed) [space can be $\geq 0.058 \mu\text{m}$ inside SRAM word line decoder covered by layer 186;4]	D	$\geq$	0.07
CO.S.4	{CO inside PO} space to OD	E	$\geq$	0.10
CO.S.5	{CO inside OD} space to 1.8V, 2.5V, or 3.3V GATE	F	$\geq$	0.11
CO.S.6	Space to butted PP/NP edge on OD (overlap of NP/PP boundary on OD is not allowed.) (Except SBDDMY region)	G	$\geq$	0.06
CO.EN.1	Enclosure by OD	H	$\geq$	0.04
CO.EN.1®	Recommended enclosure by OD to avoid high Rc	H	$\geq$	0.07
CO.EN.2	Enclosure by PO	J	$\geq$	0.02
CO.EN.3	Enclosure by PO [at least two opposite sides]	K	$\geq$	0.05
CO.EN.3®	Recommended enclosure by PO [at least two opposite sides] to avoid high Rc	K	$\geq$	0.07
CO.R.2	Overlap of RPO is not allowed.			
CO.R.3	45-degree rotated CO is not allowed.			
CO.R.4	CO must be fully covered by M1 and {OD OR PO}.			
Guideline	Description			
CO.S.6g	Recommended to put contacts at both source side and butted well pickup side to avoid high Rs. DRC can flag if the STRAP is butted on source, one of STRAP and source is without CO.			
CO.R.1g <sup>U</sup>	Recommended to put {CO inside PO} space to GATE as close as possible to avoid high Rs.			
CO.R.5g	Recommend using redundant CO wherever layout allows to avoid high Rc. 1. Recommended to use double CO or more on the resistor connection. 2. Double CO on Poly gate to reduce the probability of high Rc 3. Recommend putting multiple and symmetrical source/drain CO for SPICE simulation accuracy, especially for the device width >2 $\mu\text{m}$ 4. If it is hard to increase the CO to gate spacing (CO.S.3®) for the large transistor, limit the number of source/drain CO: to have the necessary CO number for the current, and then distribute the CO evenly on the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle) 5. DRC can flag single CO.			

CO

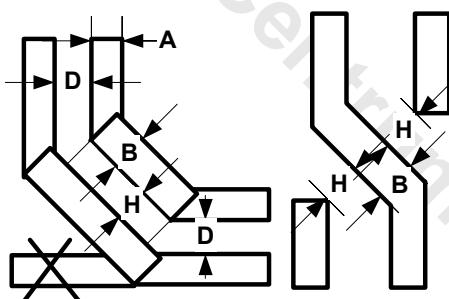
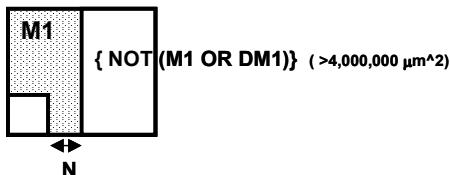
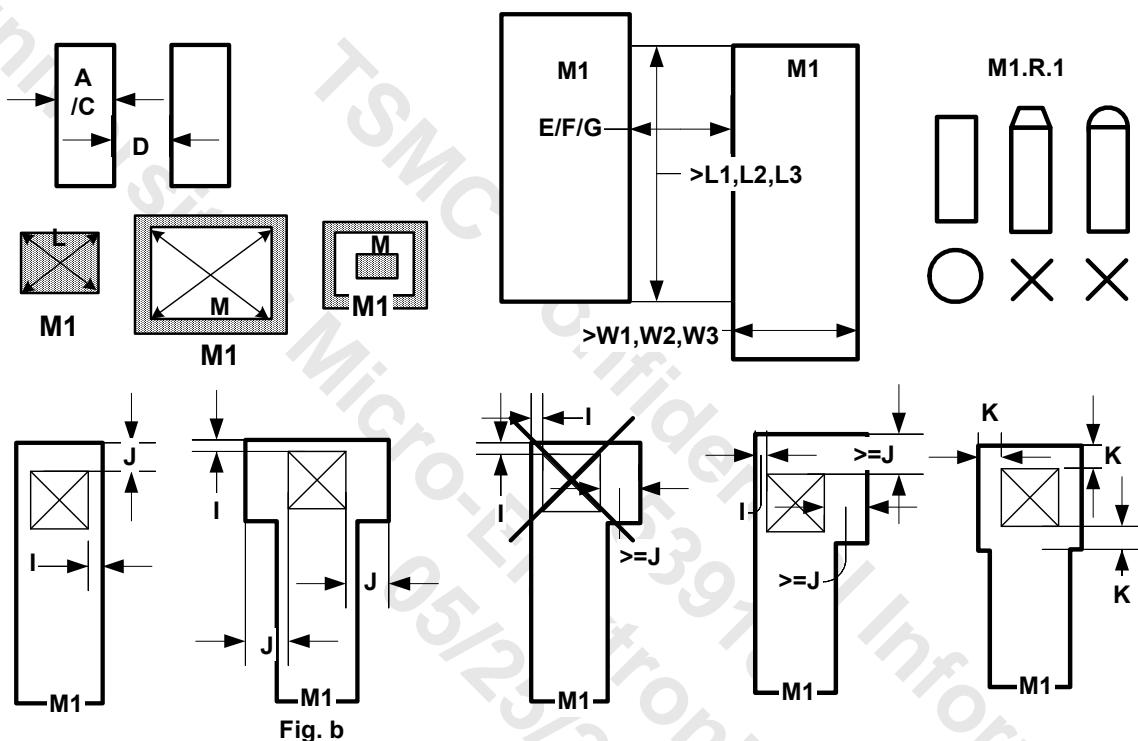


## 4.5.23 Metal-1 (M1) Layout Rules (Mask ID: 360)

Rule No.	Description	Label		Rule
M1.W.1	Width	A	$\geq$	0.12
M1.W.2	Width of 45-degree bent M1 Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)	B	$\geq$	0.19
M1.W.3	Maximum width	C	$\leq$	12.00
M1.S.1	Space	D	$\geq$	0.12
M1.S.2	Space [at least one metal line width > 0.3 $\mu\text{m}$ (W1) and the parallel metal run length > 0.52 $\mu\text{m}$ (L1)]	E	$\geq$	0.17
M1.S.3	Space [at least one metal line width > 1.5 $\mu\text{m}$ (W2) and the parallel metal run length > 1.5 $\mu\text{m}$ (L2)]	F	$\geq$	0.50
M1.S.4	Space [at least one metal line width > 4.5 $\mu\text{m}$ (W3) and the parallel metal run length > 4.5 $\mu\text{m}$ (L3)]	G	$\geq$	1.50
	Note: When M1 width > 9um is used, please take care of the M1.DN.2 rule by using larger space. For example, if two M1 with width 12um and space 1.5um, it will get 92.5% density violation on M1.DN.2; either enlarger the M1 space (like 2um) or reduce the M1 width (like 9um) to meet M1.DN.2.			
M1.S.5	Space to 45-degree bent M1	H	$\geq$	0.19
M1.S.6®	Recommended space between two non-M1 regions [ one of the non-M1 area > 4,000,000 $\mu\text{m}^2$ . Non-M1 region is defined as { NOT (M1 OR DM1)} e.g. enlarge the metal width $\geq$ 0.35 for the guard ring design.	N	$\geq$	0.35
M1.EN.0	Enclosure of CO is defined by either {M1.EN.1 and M1.EN.2} or M1.EN.3.			
M1.EN.1	Enclosure of CO	I	$\geq$	0.00
M1.EN.2	Enclosure of CO [at least two opposite sides]	J	$\geq$	0.05
M1.EN.2®	Recommended enclosure of CO [at least two opposite sides] to avoid high Rc	J	$\geq$	0.07
M1.EN.3	Enclosure of CO	K	$\geq$	0.025
M1.EN.3®	Recommended M1 [width >0.6um] enclosure of CO to avoid high Rc	K	$\geq$	0.07
M1.A.1	Area	L	$\geq$	0.058
M1.A.2	Enclosed area	M	$\geq$	0.2
M1.R.1 <sup>U</sup>	M1 line-end must be rectangular. Other shapes are not allowed.			
	For the following M1.DN.1, M1.DN.2, M1.DN.3, M1.DN.3®, and DM1.R.1, please refer to the "Dummy Metal Rules" section in Chapter 6 for the details.			
M1.DN.1	Metal density range in whole chip		$\geq$	15% in 50x50
			$\leq$	70% in 100x100
M1.DN.2	Maximum metal density over any 20 $\mu\text{m}$ x 20 $\mu\text{m}$ area (checked by stepping in 10 $\mu\text{m}$ increments).		$\leq$	90%
M1.DN.3	Metal density range within DMxEXCL		$\geq$	15% in 50x50
			$\leq$	70% in 100x100
M1.DN.3®	Metal density range within DMxEXCL over any 10 $\mu\text{m}$ x 10 $\mu\text{m}$ area with 3 $\mu\text{m}$ x 3 $\mu\text{m}$ open area (checked by stepping in 5 $\mu\text{m}$ increments) for CMP uniformity.		$\geq$	20%
DM1.R.1	DM1 is a must. The DM1 CAD layer (TSMC default, 31;1 for DM1) must be different from the M1 CAD layer.			

**Table Notes:**

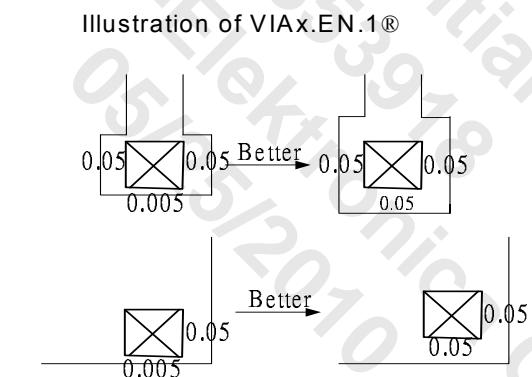
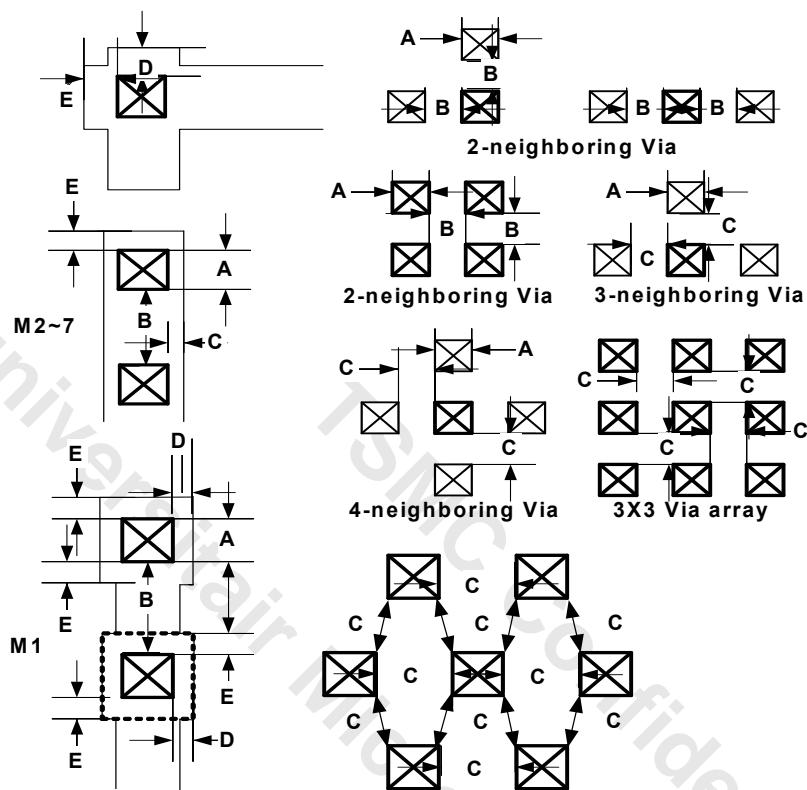
- To improve the metal CMP process window, you must fill the DMx globally and uniformly even if the originally drawn M1 has already met the density rule (M1.DN.1/M1.DN.2/M1.DN.3). For sensitive areas with auto-fill operations blocked by the DM1EXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.
- During IP/marco design, it is important to put certain density margin to avoid the possibility of high density violations (M1.DN.1, M1.DN.2, M1.DN.3) during placement. It may have unexpected violation during the IP/marco placement due to the environment, even if the IP/marco already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.



## 4.5.24 VIAx Layout Rules (Mask ID: 378, 379, 373, 374, 375, 376)

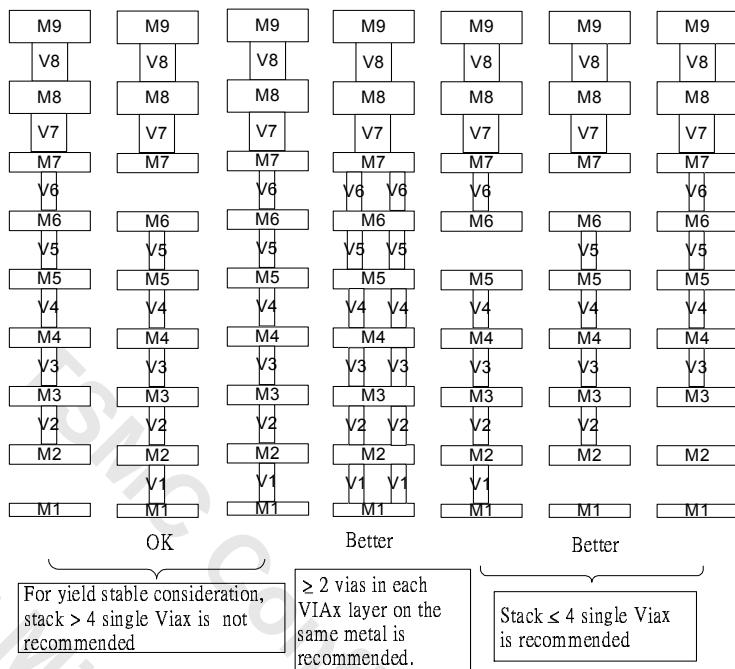
For the application of metal/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label	Rule
VIAx.W.1	Width (square) (maximum = minimum)	A	= 0.13
VIAx.W.2	Width of VIAx bar. VIAx bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a must if VIAx bar is used.		= 0.13
VIAx.S.1	Space	B	$\geq$ 0.15
VIAx.S.2	Space to 3-neighboring VIAx (< 0.19 $\mu\text{m}$ distance)	C	$\geq$ 0.17
VIAx.EN.0	Enclosure by Mx or M1 is defined by either {VIAx.EN.1and VIAx.EN.2} or VIAx.EN.3.		
VIAx.EN.0®	Recommended enclosure by Mx or M1 is defined by either VIAx.EN.1® or VIAx.EN.2®.		
VIAx.EN.1	Enclosure by Mx or M1	D	$\geq$ 0.005
VIAx.EN.1®	Recommended enclosure by Mx or M1 [VIA1 count $\leq$ 2 in the region of (M1 AND M2) or VIAx count $\leq$ 2 in the region of (Mx and Mx+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	D	$\geq$ 0.05
VIAx.EN.2	Enclosure by Mx or M1 [at least two opposite sides]	E	$\geq$ 0.05
VIAx.EN.2®	Recommended enclosure by Mx or M1 [at least two opposite sides] [VIA1 count $\leq$ 2 in the region of (M1 AND M2) or VIAx count $\leq$ 2 in the region of (Mx and Mx+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	E	$\geq$ 0.08
VIAx.EN.3	Enclosure by Mx or M1 [all sides]	D	$\geq$ 0.04
VIAx.R.1	45-degree rotated VIAx is not allowed.		
VIAx.R.2	At least two VIAx with space $\leq$ 0.29 (S1), or at least four VIAx with space $\leq$ 0.57 $\mu\text{m}$ (S1'), or at least nine VIAx with space $\leq$ 0.77 $\mu\text{m}$ (S1'') are required to connect Mx and Mx+1 when one of these two metals has width and length (W1) $>$ 0.42 $\mu\text{m}$ .		
VIAx.R.3	At least four VIAx with space $\leq$ 0.29 (S2), or at least nine VIAx with space $\leq$ 0.77 $\mu\text{m}$ (S2') are required to connect Mx and Mx+1 when one of these two metals has width and length (W2) $>$ 1.14 $\mu\text{m}$ .		
VIAx.R.4	At least two VIAx must be used for a connection that is $\leq$ 1 $\mu\text{m}$ (D) away from a metal plate (either Mx or Mx+1) with length $>$ 0.7 $\mu\text{m}$ (L) and width $>$ 0.7 $\mu\text{m}$ (W). (It is allowed to use one VIAx for a connection that is $>$ 1 $\mu\text{m}$ (D) away from a metal plate (either Mx or Mx+1) with length $>$ 0.7 $\mu\text{m}$ (L) and width $>$ 0.7 $\mu\text{m}$ (W).)		
VIAx.R.5	At least two VIAx must be used for a connection that is $\leq$ 2 $\mu\text{m}$ (D) away from a metal plate (either Mx or Mx+1) with length $>$ 2 $\mu\text{m}$ (L) and width $>$ 2 $\mu\text{m}$ (W). (It is allowed to use one VIAx for a connection that is $>$ 2 $\mu\text{m}$ (D) away from a metal plate (either Mx or Mx+1) with length $>$ 2 $\mu\text{m}$ (L) and width $>$ 2 $\mu\text{m}$ (W).)		
VIAx.R.6	At least two VIAx must be used for a connection that is $\leq$ 5 $\mu\text{m}$ (D) away from a metal plate (either Mx or Mx+1) with length $>$ 10 $\mu\text{m}$ (L) and width $>$ 3 $\mu\text{m}$ (W). (It is allowed to use one VIAx for a connection that is $>$ 5 $\mu\text{m}$ (D) away from a metal plate (either Mx or Mx+1) with length $>$ 10 $\mu\text{m}$ (L) and width $>$ 3 $\mu\text{m}$ (W).)		
VIAx.R.7	VIAx must be fully covered by Mx and Mx+1.		
VIAx.R.8®	Maximum consecutive stacked VIAx layer, which has only one via for each VIAx layer to avoid high Rc. (Example: VIA1~VIA4, VIA2~VIA5, VIA3~VIA6. This rule does not apply to top via. It is allowed to stack from VIA3 to VIA8 because VIA7 and VIA8 are top via.)	$\leq$	4
VIAx.R.11	Single VIAx is not allowed in "H-shape" Mx+1 when all of the following conditions come into existence: 1) The Mx+1 has "H-shape" interact with two metal holes: both two metal hole length (L2) $\leq$ 5um and two metal hole area $\leq$ 5um <sup>2</sup> 2) The VIAx overlaps on the center metal bar of this "H-shape" Mx+1 3) The length (L) of the center metal bar $\leq$ 1um and the width of metal bar is $\leq$ 0.42um.		
<b>Guideline</b>	<b>Description</b>		
VIAx.R.9g	Recommend using redundant vias to avoid high Rc wherever layout allows. Please refer to the "Via Layout Recommendations" section in Chapter 4. DRC can flag single via.		

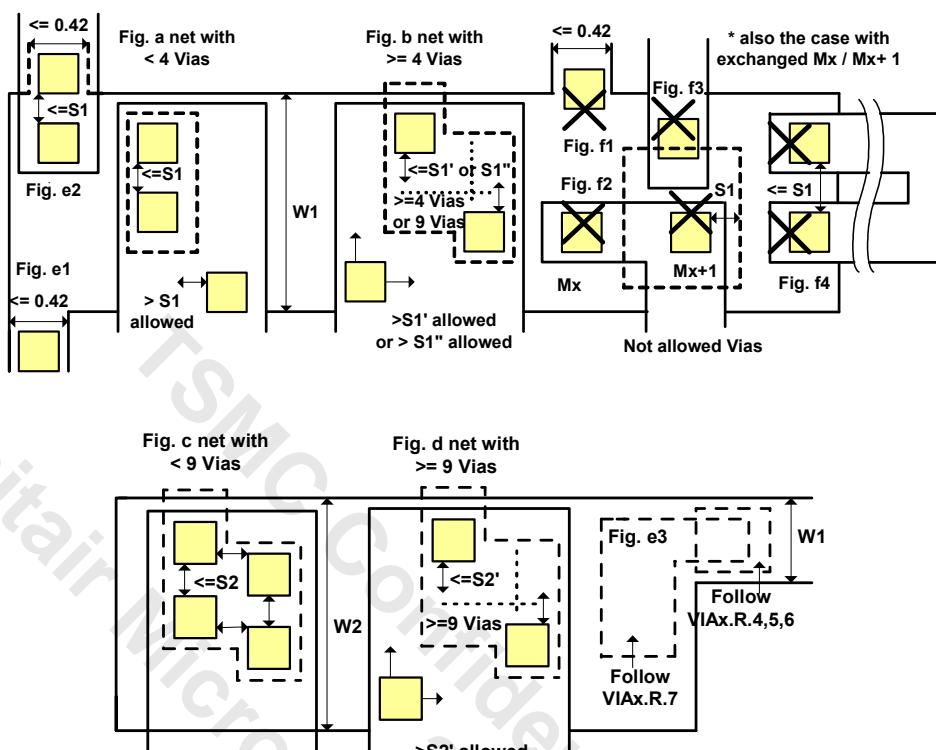


From the EM spec, at least two vias are needed. It is strongly suggested to use  $\geq$  two vias in each VIAx layer for stacked via structures.

Illustration of VIAx.R.8®



## Illustration of VIAx.R.2, VIAx.R.3 Rules



Rule VIAx.R.2 $0.42 \mu\text{m} < W1 \leq 1.14 \mu\text{m}$		Rule VIAx.R.3 $W2 \mu\text{m} > 1.14 \mu\text{m}$		Fig. d ≥ 9 vias	
Fig. a < 4 vias	Fig. b		Fig. c <9 vias		
	≥ 4 vias	≥ 9 vias			
S1 = 0.29 μm	S1' = 0.57 μm	S1'' = 0.77 μm	S2 = 0.29 μm	S2' = 0.77 μm	

**Fig a.** At least two vias with spacing  $\leq 0.29 \mu\text{m}$  inside the same overlapped metal region ( $M_x$  AND  $M_{x+1}$ ).

**Fig. b** At least four vias with spacing  $\leq 0.57 \mu\text{m}$ , or at least nine vias with spacing  $\leq 0.77 \mu\text{m}$

**Fig. c.** At least four vias with spacing  $\leq 0.29 \mu\text{m}$  inside the same overlapped metal region ( $M_x$  AND  $M_{x+1}$ ).

**Fig. d** At least nine vias with spacing  $\leq 0.77 \mu\text{m}$ .

**Fig. e1** A single via is allowed inside metal of width  $\leq 0.42 \mu\text{m}$ . However, it is a violation if the via is located on the boundary between metal segments of width  $\leq 0.42 \mu\text{m}$  and width  $> 0.42 \mu\text{m}$  as shown in fig f1.

**Fig. e2** A via or vias located on  $\leq W_1$  ( $W_2$ ) metal but near  $> W_1$  ( $W_2$ ) metal can be counted in for the rule.

**Fig. e3** A via or vias located on  $\leq W_1$  ( $W_2$ ) metal but near  $> W_1$  ( $W_2$ ) metal can be counted in for the rule.

**Fig. e3** Indicates the rules that the areas within the vias should follow.

*Layout violation examples:*

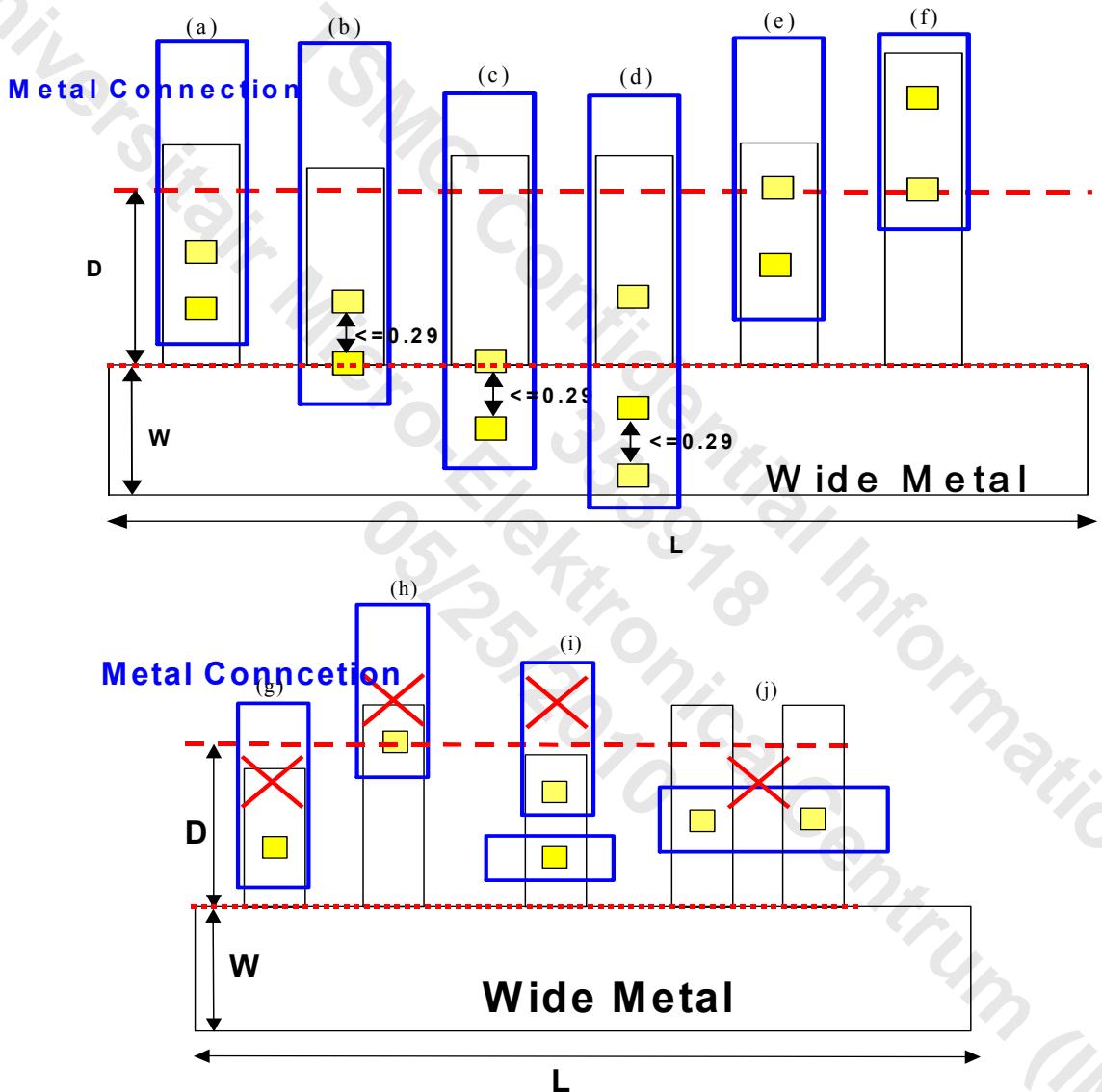
**Fig. f2.** Two vias with spacing  $> 0.29 \mu\text{m}$ .

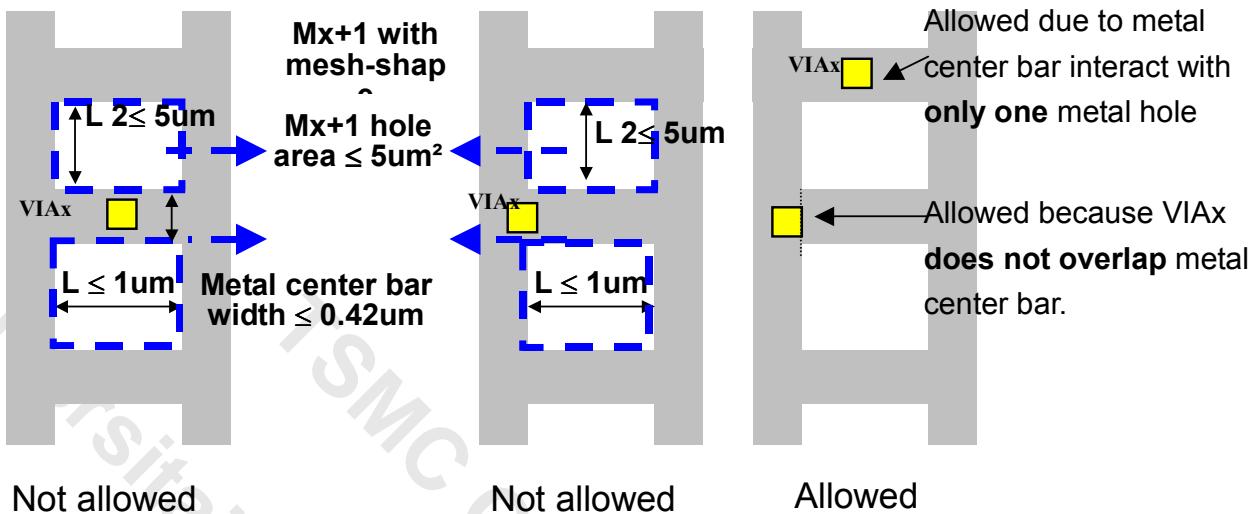
**Fig. f3/f4.** Two vias with spacing  $\leq 0.29 \mu\text{m}$  on the same net but not inside the same overlapped metal region ( $M_x$  AND  $M_{x+1}$ ).

## Illustration of VIAx.R.4/VIAx.R.5/VIAx.R.6 Rules

Rule No	VIAx.R.4	VIAx.R.5	VIAx.R.6
Wide Metal	M <sub>x</sub> or M <sub>x+1</sub>	M <sub>x</sub> or M <sub>x+1</sub>	M <sub>x</sub> or M <sub>x+1</sub>
Metal connection	M <sub>x+1</sub> or M <sub>x</sub>	M <sub>x+1</sub> or M <sub>x</sub>	M <sub>x+1</sub> or M <sub>x</sub>
W	> 0.7 $\mu$ m	> 2 $\mu$ m	> 3 $\mu$ m
L	> 0.7 $\mu$ m	> 2 $\mu$ m	> 10 $\mu$ m
D	$\leq$ 1 $\mu$ m	$\leq$ 2 $\mu$ m	$\leq$ 5 $\mu$ m

(a) ~ (f) is ok but (g) ~ (j) is not allowed



**Illustration of VIAx.R.11 Rules**

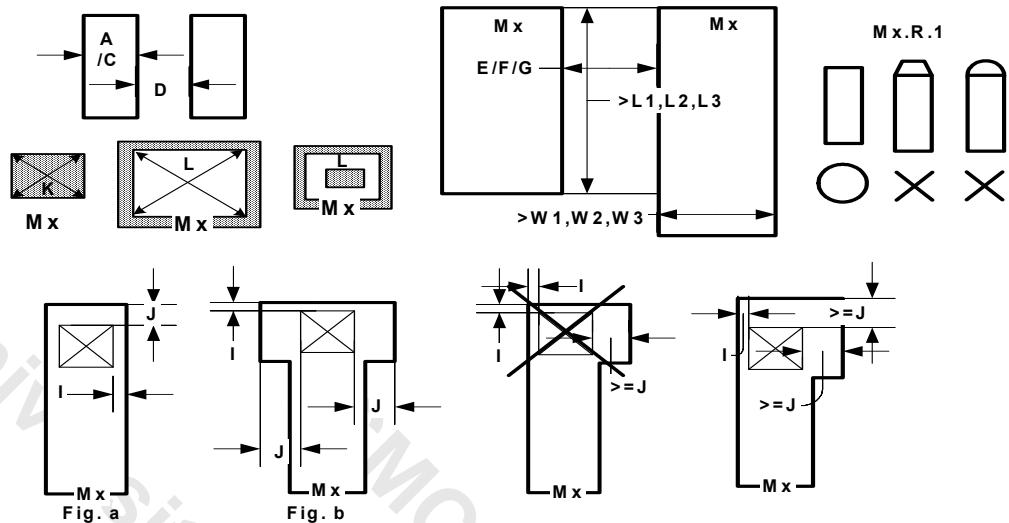
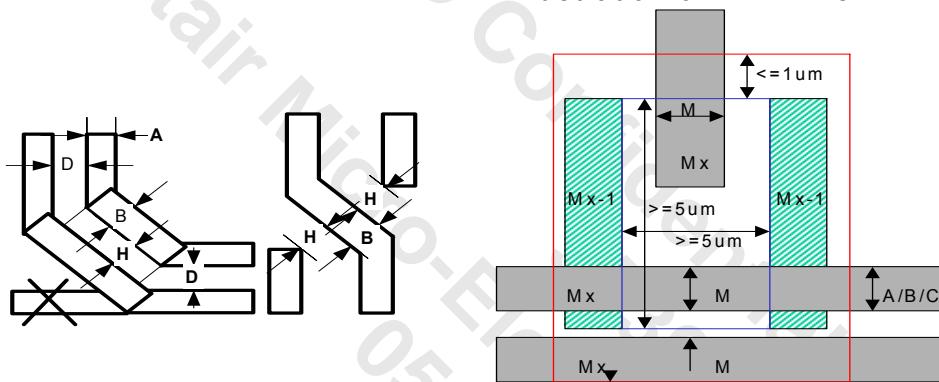
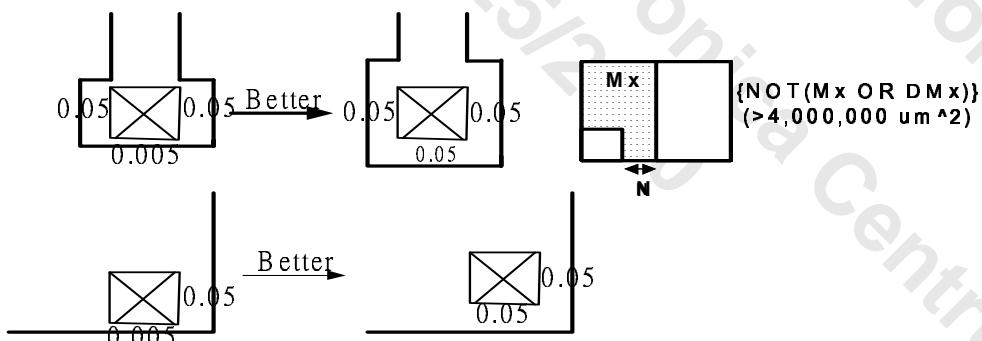
## 4.5.25 Mx Layout Rules (Mask ID: 380, 381, 384, 385, 386, 387)

For the application of metal/vias stacking sequence and associated mask id, please refer to section 2.5.

Rule No.	Description	Label	Rule
Mx.W.1	Width	A	$\geq 0.14$
Mx.W.2	Width of 45-degree bent Mx Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)	B	$\geq 0.19$
Mx.W.3	Maximum width	C	$\leq 12.00$
Mx.W.4®	Recommended Mx width [Mx on (((Mx-1 OR DMx-1) with space $\geq 5 \times 5 \mu\text{m}$ ) sizing 1)] for CMP uniformity	M	$\geq 0.16$
Mx.S.1	Space	D	$\geq 0.14$
Mx.S.2	Space [at least one metal line width $> 0.21 \mu\text{m}$ (W1) and the parallel metal run length $> 0.52 \mu\text{m}$ (L1)]	E	$\geq 0.19$
Mx.S.3	Space [at least one metal line width $> 1.5 \mu\text{m}$ (W2) and the parallel metal run length $> 1.5 \mu\text{m}$ (L2)]	F	$\geq 0.50$
Mx.S.4	Space [at least one metal line width $> 4.5 \mu\text{m}$ (W3) and the parallel metal run length $> 4.5 \mu\text{m}$ (L3)]	G	$\geq 1.50$
	Note: When Mx width $> 9\mu\text{m}$ is used, please take care of the Mx.DN.2 rule by using larger space. For example, if two Mx with width 12um and space 1.5um, it will get 92.5% density violation on Mx.DN.2; either enlarger the Mx space (like 2um) or reduce the Mx width (like 9um) to meet Mx.DN.2.		
Mx.S.5	Space to 45-degree bent Mx	H	$\geq 0.19$
Mx.S.6®	Recommended space between two non-Mx regions [ one of the non-Mx area $> 4,000,000 \mu\text{m}^2$ ]. Non-Mx region is defined as { NOT (Mx OR DMx) }. e.g. enlarge the metal width $\geq 0.35$ for guard ring design.	N	$\geq 0.35$
Mx.EN.0	Enclosure of VIAx-1 is defined by either {Mx.EN.1 and Mx.EN.2} or Mx.EN.3.		
Mx.EN.0®	Recommended enclosure of VIAx-1 is defined by either Mx.EN.1® or Mx.EN.2®.		
Mx.EN.1	Enclosure of VIAx-1	I	$\geq 0.005$
Mx.EN.1®	Recommended enclosure of VIAx-1 [VIAx-1 count $\leq 2$ in the region of (Mx-1 AND Mx)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	I	$\geq 0.05$
Mx.EN.2	Enclosure of VIAx-1 [at least two opposite sides]	J	$\geq 0.05$
Mx.EN.2®	Recommended enclosure of VIAx-1 [at least two opposite sides] [VIAx-1 count $\leq 2$ in the region of (Mx-1 AND Mx)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	J	$\geq 0.08$
Mx.EN.3	Enclosure of VIAx-1 [all sides].	I	$\geq 0.04$
Mx.A.1	Area	K	$\geq 0.07$
Mx.A.2	Enclosed area	L	$\geq 0.20$
Mx.R.1 <sup>U</sup>	Mx line-end must be rectangular. Other shapes are not allowed.		
	For the following Mx.DN.1, Mx.DN.2, Mx.DN.3, Mx.DN.3®, and DMx.R.1, please refer to the "Dummy Metal Rules" in Chapter 9 for the details.		
Mx.DN.1	Metal density range in whole chip		$\geq 15\%$ in 50x50
			$\leq 70\%$ in 100 x100

Rule No.	Description	Label	Rule
Mx.DN.2	Maximum metal density over any 20 $\mu\text{m}$ x 20 $\mu\text{m}$ area (checked by stepping in 10 $\mu\text{m}$ increments).		$\leq$ 90%
Mx.DN.3	Metal density range within DMxEXCL		$\geq$ 15% in 50x50
			$\leq$ 70% in 100x100
Mx.DN.3®	Metal density range within DMxEXCL over any 10 $\mu\text{m}$ x 10 $\mu\text{m}$ area with 3 $\mu\text{m}$ x 3 $\mu\text{m}$ open area (checked by stepping in 5 $\mu\text{m}$ increments) for CMP uniformity.		$\geq$ 20%
Mx.DN.4®	It is not recommended to have local density $> 70\%$ of all 3 consecutive metal (Mx, Mx+1 and Mx+2) over any 50um x 50um (stepping 25um) for CMP uniformity, i.e. it is preferred to have for either one of Mx, Mx+1, or Mx+2 to have a local density $\leq 70\%$ . 1. The metal layers include M1/Mx and dummy metals. 2. The check does not include chip corner stress relief pattern and seal ring.		
DMx.R.1*	DMx is a must. The DMx CAD layer (TSMC default, 32;1 for DM2) must be different from the Mx CAD layer.		
Guideline	Description		
Mx.R.2g <sup>U</sup>	For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance and the possibility of metal short. Please refer to section 10.1.1 and TSMC Reference Flow.		

- **Table Notes:** To improve the metal CMP process window, you must fill the DMx globally and uniformly even if the originally drawn Mx has already met the density rule (Mx.DN.1/Mx.DN.2/Mx.DN.3). For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.
- During IP/marco design, it is important to put certain density margin to avoid the possibility of high density violations (Mx.DN.1, Mx.DN.2, Mx.DN.3) during placement. It may have unexpected violation during the IP/marco placement due to the environment, even if the IP/marco already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.

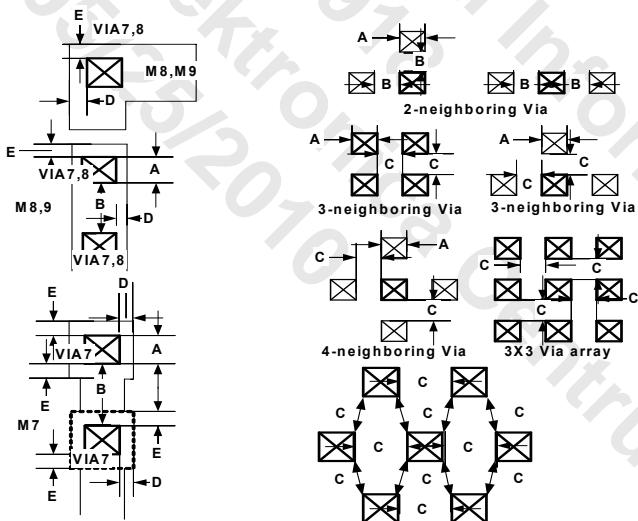
Illustration of  $M_x.W.4^{\circledR}$ Illustration of  $M_x.EN.1^{\circledR}$ 

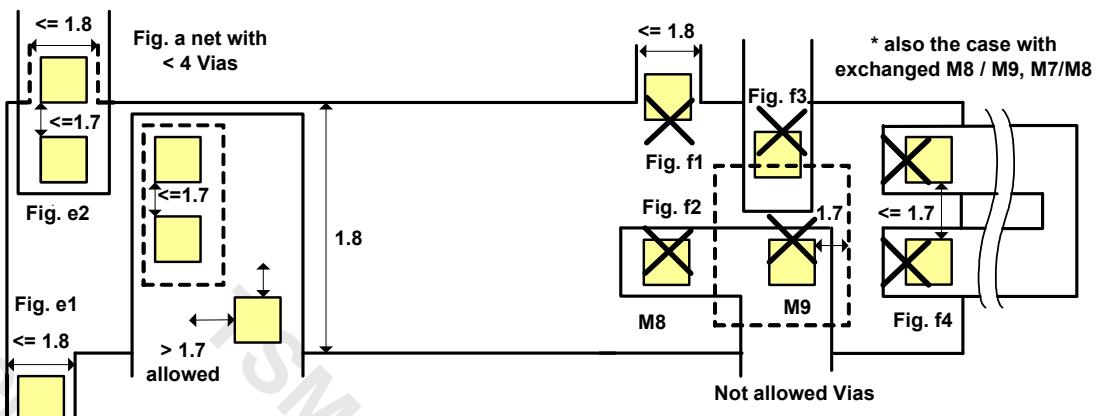
## 4.5.26 VIA<sub>n</sub> Layout Rules (Mask ID: 379, 373, 374, 375, 376, 377, 372) (3XTM)

For the application of metal/vias stacking sequence and associated mask id, please refer to section 2.5.

VIA<sub>n</sub> and VIA<sub>y</sub> can not be used on the same die.

Rule No.	Description	Label		Rule
VIA <sub>n</sub> .W.1	Width (square)(maximum = minimum)	A	=	0.36
VIA <sub>n</sub> .W.2	Width of VIA <sub>n</sub> bar. VIA <sub>n</sub> bar is only allowed in seal ring and fuse protection ring.		=	0.28
VIA <sub>n</sub> .S.1	Space	B	$\geq$	0.34
VIA <sub>n</sub> .S.2	Space to 3-neighboring VIA <sub>n</sub> (<0.56 $\mu$ m distance)	C	$\geq$	0.54
VIA <sub>n</sub> .EN.1	Enclosure by M <sub>x</sub> or M <sub>n</sub>	D	$\geq$	0.03
VIA <sub>n</sub> .EN.2	Enclosure by M <sub>x</sub> or M <sub>n</sub> [at least two opposite sides]	E	$\geq$	0.08
VIA <sub>n</sub> .R.1	45-degree rotated VIA <sub>n</sub> is not allowed.			
VIA <sub>n</sub> .R.2	At least two VIA <sub>n</sub> with spacing $\leq$ 1.7 $\mu$ m are required to connect M <sub>n</sub> and M <sub>n+1</sub> when one of these metals has a width and length > 1.8 $\mu$ m.			
VIA <sub>n</sub> .R.3	At least two VIA <sub>n</sub> must be used for a connection that is $\leq$ 5 $\mu$ m (D) away from a metal plate (either M <sub>n</sub> or M <sub>n+1</sub> ) with length > 10 $\mu$ m (L) and width > 3 $\mu$ m (W). (It is allowed to use one VIA <sub>n</sub> for a connection that is > 5 $\mu$ m (D) away from a metal plate (either M <sub>n</sub> or M <sub>n+1</sub> ) with length > 10 $\mu$ m (L) and width > 3 $\mu$ m (W)).			
VIA <sub>n</sub> .R.4	VIA <sub>n</sub> must be fully covered by M <sub>n</sub> and M <sub>n+1</sub> .			
Guideline	Description			
VIA <sub>n</sub> .R.5g	Recommend using redundant vias to avoid high R <sub>c</sub> wherever layout allows. DRC can flag single via.			



**Illustration of VIAn.R.2 Rule**

**Fig. a** At least two vias with spacing  $\leq 1.7$  μm inside the same overlapped metal region (M7 AND M8) or (M8 AND M9).

**Fig. e1** A single via is allowed inside metal of width  $\leq 1.8$  μm. However, it is a violation if the via is located on the boundary between a metal segment of width  $\leq 1.8$  μm and a segment of width  $> 1.8$  μm as in Fig. f1.

**Fig. e2** A via or vias that are located on  $\leq 1.8$  metal but near  $> 1.8$  metal can be counted in for the rule.

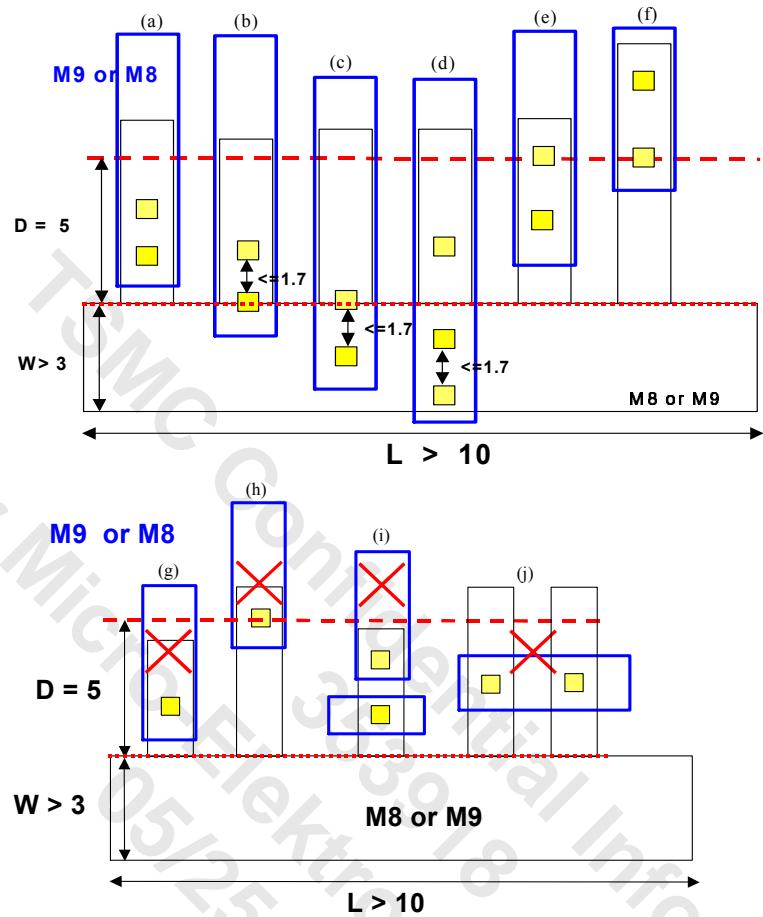
*Violated layout examples:*

**Fig. f2** Two vias with spacing  $> 1.7$  μm.

**Fig. f3/f4** Two vias with spacing  $\leq 1.7$  μm on the same net but not inside the same overlapped metal region (M7 AND M8) or (M8 AND M9).

## Illustration of VIAn.R.3 Rule

(a) ~ (f) is ok but (g) ~ (j) is not allowed



## 4.5.27 Mn Layout Rules (Mask ID: 381, 384, 385, 386, 387, 388, 389) (3XTM)

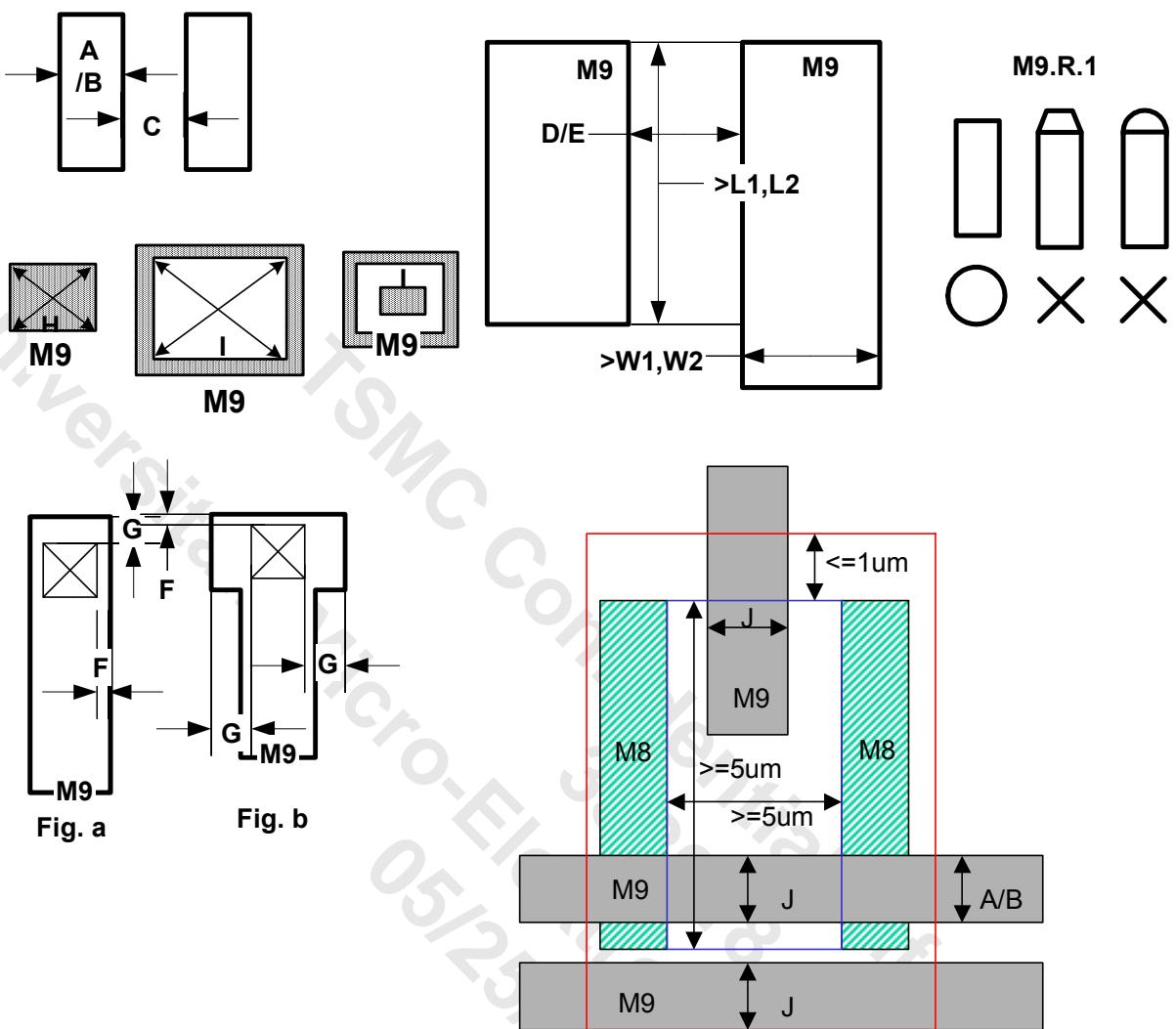
For the application of metal/vias stacking sequence and associated mask id, please refer to section 2.5.

Mn and My can not be used on the same die.

Rule No.	Description	Label	Rule
Mn.W.1	Width	A	$\geq$ 0.42
Mn.W.2	Maximum width [except bond pad]	B	$\leq$ 12.00
Mn.W.3®	Recommended Mn width [Mn on (((Mn-1 OR DMn-1) with space $\geq$ 5x5μm) sizing 1)] for CMP uniformity	J	$\geq$ 0.44
Mn.S.1	Space	C	$\geq$ 0.42
Mn.S.2	Space [at least one metal line width > 1.5 μm (W1) and the parallel metal run length > 1.5 μm (L1)]	D	$\geq$ 0.50
Mn.S.3	Space [at least one metal line width > 4.5 μm (W2) and the parallel metal run length > 4.5 μm (L2)]	E	$\geq$ 1.50
	Note: When Mn width > 9um is used, please take care of the Mn.DN.2 rule by using larger space. For example, if two Mn with width 12um and space 1.5um, it will get 92.5% density violation on Mn.DN.2; either enlarger the Mn space (like 2um) or reduce the Mn width (like 9um) to meet Mn.DN.2.		
Mn.EN.1	Enclosure of VIAn-1	F	$\geq$ 0.03
Mn.EN.2	Enclosure of VIAn-1 [at least two opposite sides]	G	$\geq$ 0.08
Mn.A.1	Area	H	$\geq$ 0.565
Mn.A.2	Enclosed area	I	$\geq$ 0.565
Mn.R.1 <sup>U</sup>	Mn line-end must be rectangular. Other shapes are not allowed.		
	For the following Mn.DN.1, Mn.DN.2, Mn.DN.3, and DMn.R.1, please refer to the "Dummy Metal Rules" in Chapter 9 for the details.		
Mn.DN.1	Mn density range in whole chip Bond pad is excluded from 80% density check.		$\geq$ 20% in 50x50 $\leq$ 80% in 100x100
Mn.DN.2	Maximum metal density over any 20um x 20um area (checked by stepping in 10um increments). Bond pad is excluded from 90% density check.		$\leq$ 90%
Mn.DN.3	Metal density range within DMnEXCL		$\geq$ 20% in 50x50 $\leq$ 80% in 100x100
Mn.R.1 <sup>U</sup>	Mn line-end must be rectangular. Other shapes are not allowed.		
DMn.R.1	DMn is a must. The DMn CAD layer (TSMC default, 38;1 for DM8) must be different from the Mn CAD layer.		

### Table Notes:

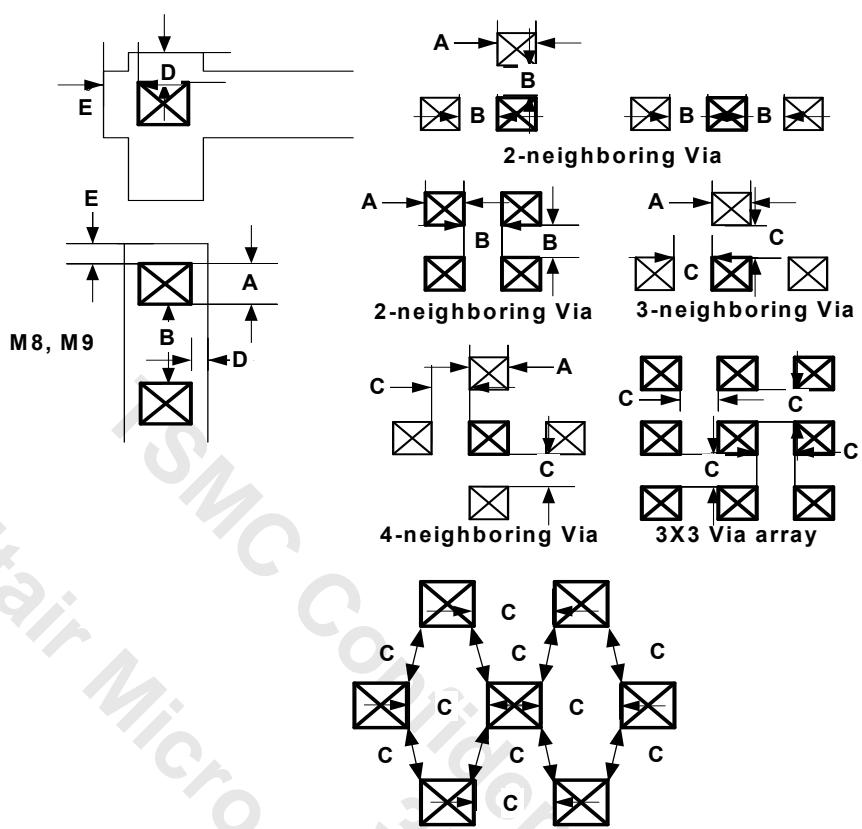
- For RF/Mixed-signal applications, some metal rules are different from Logic rules. Please refer to RF/Mixed-signal design rules for details.
- To improve the metal CMP process window, you must fill the DMn globally and uniformly even if the originally drawn Mn has already met the density rule (Mn.DN.1/Mn.DN.2/Mn.DN.3). For sensitive areas with auto-fill operations blocked by the DMxEXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.
- During IP/marco design, it is important to put certain density margin to avoid the possibility of high density violations (Mn.DN.1, Mn.DN.2, Mn.DN.3) during placement. It may have unexpected violation during the IP/marco placement due to the environment, even if the IP/marco alerady pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.



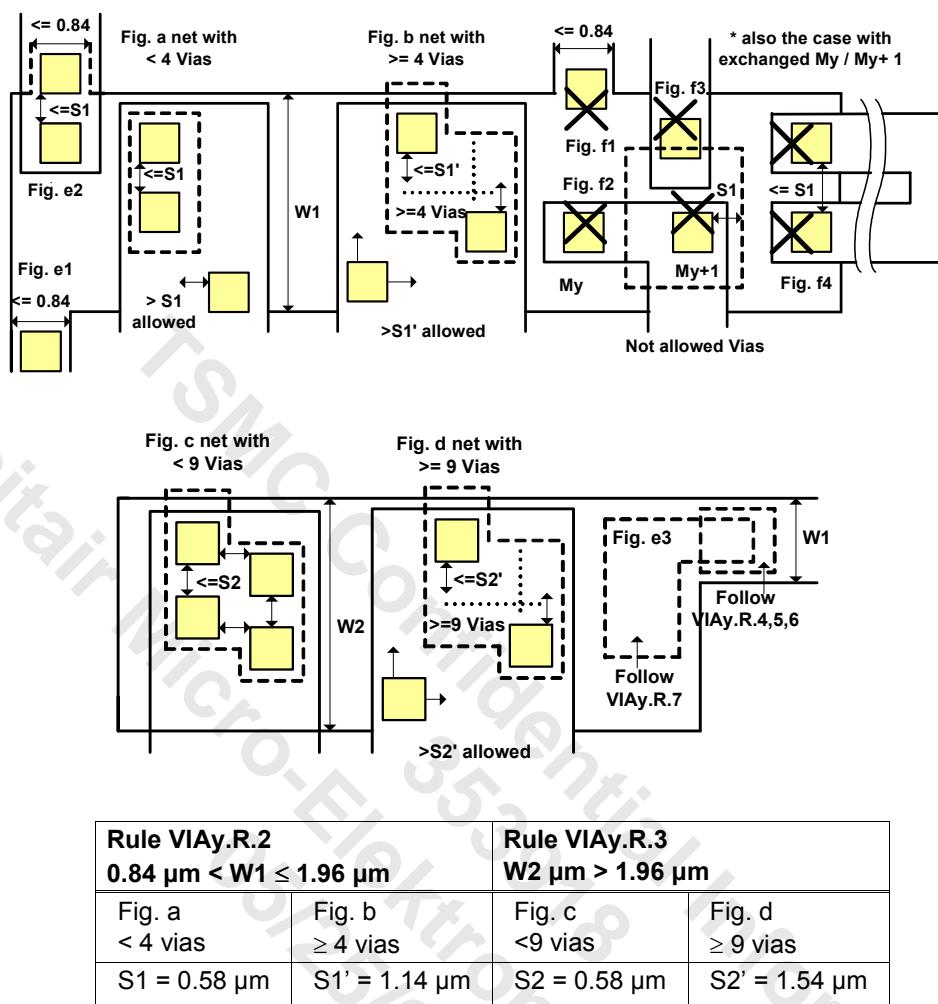
## 4.5.28 VIAy Layout Rules (Mask ID: 379, 373, 374, 375, 376, 377, 372) (2XTM)

For the application of metal/vias stacking sequence and associated mask id, please refer to section 2.5.  
VIAn and VIAy can not be used on the same die.

Rule No.	Description	Label		Rule
VIAy.W.1	Width (square)	A	=	0.26
VIAy.W.2	Width of VIAy bar. VIAy bar is only allowed in seal-ring and fuse protection ring.		=	0.13
VIAy.S.1	Space	B	$\geq$	0.30
VIAy.S.2	Space to 3-neighboring VIAy (< 0.39 $\mu\text{m}$ distance)	C	$\geq$	0.37
VIAy.EN.0®	Recommended enclosure by Mx or My is defined by either VIAy.EN.1® or VIAy.EN.2®.			
VIAy.EN.1	Enclosure by Mx or My	D	$\geq$	0.01
VIAy.EN.1®	Recommended enclosure by Mx or My [VIAy count $\leq 2$ in the region of (Mx AND My+1) or VIAy count $\leq 2$ in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	D	$\geq$	0.05
VIAy.EN.2	Enclosure by Mx or My [at least two opposite sides]	E	$\geq$	0.05
VIAy.EN.2®	Recommended enclosure by Mx or My [at least two opposite sides] [VIAy count $\leq 2$ in the region of (Mx AND My+1) or VIAy count $\leq 2$ in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	E	$\geq$	0.08
VIAy.R.1	45-degree rotated VIAy is not allowed.			
VIAy.R.2	At least two VIAy with space $\leq 0.58$ (S1), or at least four VIAy with space $\leq 1.14 \mu\text{m}$ (S1') are required to connect My and My+1 when one of these two metals has width and length ( $W_1$ ) $> 0.84 \mu\text{m}$ .			
VIAy.R.3	At least four VIAy with space $\leq 0.58$ (S2), or at least nine VIAy with space $\leq 1.54 \mu\text{m}$ (S2') are required to connect My and My+1 when one of these two metals has width and length ( $W_2$ ) $> 1.96 \mu\text{m}$ .			
VIAy.R.4	At least two VIAy must be used for a connection that is $\leq 1 \mu\text{m}$ (D) away from a metal plate (either My or My+1) with length $> 0.7 \mu\text{m}$ (L) and width $> 0.7 \mu\text{m}$ (W). (It is allowed to use one VIAy for a connection that is $> 1 \mu\text{m}$ (D) away from a metal plate (either My or My+1) with length $> 0.7 \mu\text{m}$ (L) and width $> 0.7 \mu\text{m}$ (W).)			
VIAy.R.5	At least two VIAy must be used for a connection that is $\leq 2 \mu\text{m}$ (D) away from a metal plate (either My or My+1) with length $> 2 \mu\text{m}$ (L) and width $> 2 \mu\text{m}$ (W). (It is allowed to use one VIAy for a connection that is $> 2 \mu\text{m}$ (D) away from a metal plate (either My or My+1) with length $> 2 \mu\text{m}$ (L) and width $> 2 \mu\text{m}$ (W).)			
VIAy.R.6	At least two VIAy must be used for a connection that is $\leq 5 \mu\text{m}$ (D) away from a metal plate (either My or My+1) with length $> 10 \mu\text{m}$ (L) and width $> 3 \mu\text{m}$ (W). (It is allowed to use one VIAy for a connection that is $> 5 \mu\text{m}$ (D) away from a metal plate (either My or My+1) with length $> 10 \mu\text{m}$ (L) and width $> 3 \mu\text{m}$ (W)).			
VIAy.R.7	VIAy must be fully covered by My and My+1.			
<b>Guideline</b>	<b>Description</b>			
VIAy.R.9g	For the small space, recommend using redundant vias to avoid high Rc wherever layout allows. Please refer to the "Via Layout Recommendations" in the section 4.5.31. DRC can flag single via.			



## Illustration of VIAy.R.2, VIAy.R.3 Rules



**Fig. a.** At least two vias with spacing  $\leq 0.58 \mu\text{m}$  inside the same overlapped metal region (My AND My+1).

**Fig. b** At least four vias with spacing  $\leq 1.14 \mu\text{m}$ .

**Fig. c.** At least four vias with spacing  $\leq 0.58 \mu\text{m}$  inside the same overlapped metal region (My AND My+1).

**Fig. d** At least nine vias with spacing  $\leq 1.54 \mu\text{m}$ .

**Fig. e1**A single via is allowed inside metal of width  $\leq 0.84 \mu\text{m}$ . However, it is a violation if the via is located on the boundary between metal segments of width  $\leq 0.84 \mu\text{m}$  and width  $> 0.84 \mu\text{m}$  as shown in fig f1.

**Fig. e2**A via or vias located on  $\leq W1$  (W2) metal but near  $> W1$  (W2) metal can be counted in for the rule.

**Fig. e3**A via or vias located on  $\leq W1$  (W2) metal but near  $> W1$  (W2) metal can be counted in for the rule.

**Fig. e3**Indicates the rules that the areas within the vias should follow.

*Layout violation examples:*

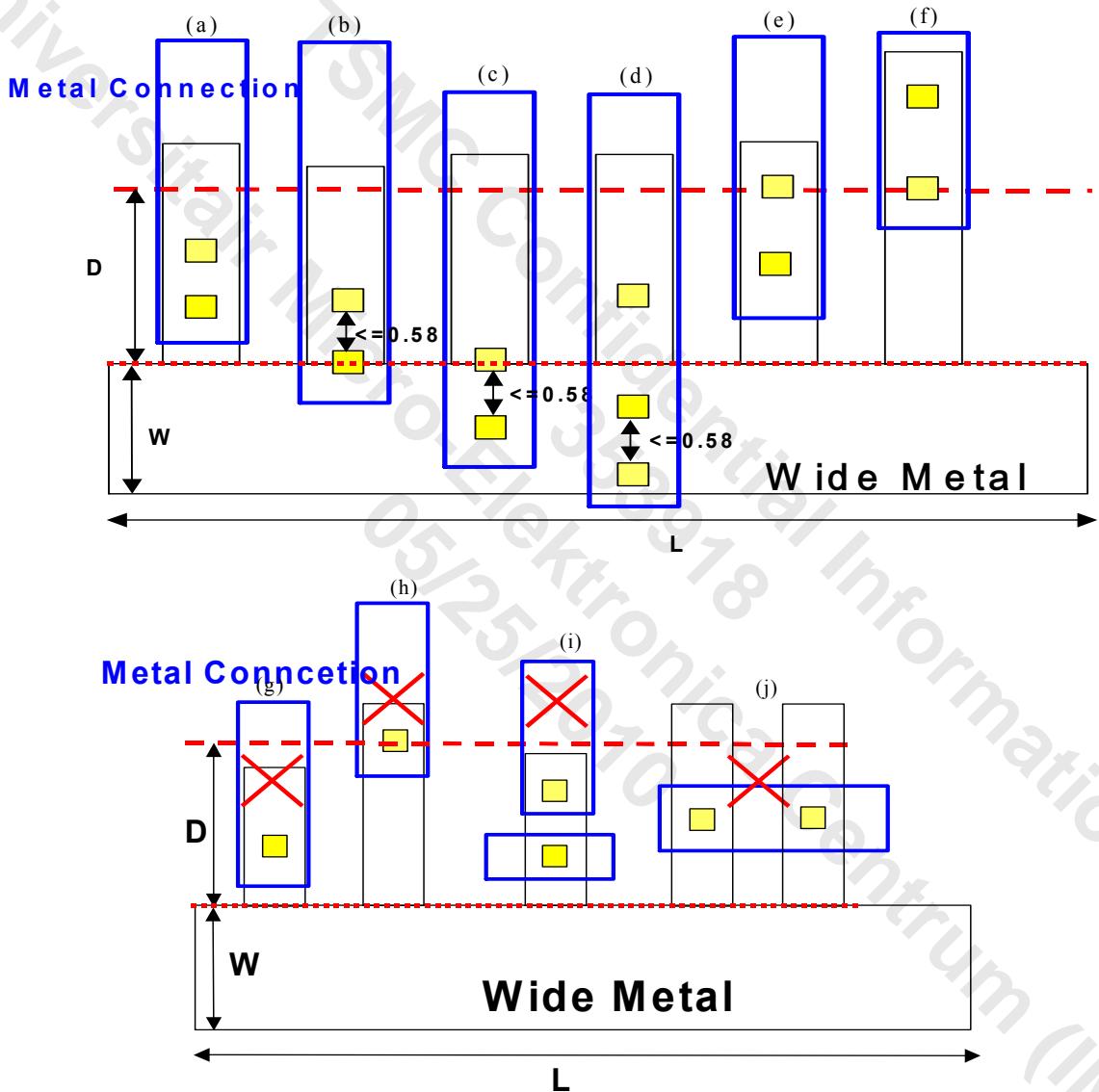
**Fig. f2.**Two vias with spacing  $> 0.58 \mu\text{m}$ .

**Fig. f3/f4.** Two vias with spacing  $\leq 0.58 \mu\text{m}$  on the same net but not inside the same overlapped metal region (My AND My+1).

## Illustration of VIAy.R.4/VIAy.R.5/VIAy.R.6 Rules

Rule No	VIAy.R.4	VIAy.R.5	VIAy.R.6
Wide Metal	My or My+1	My or My+1	My or My+1
Metal connection	My+1 or My	My+1 or My	My+1 or My
W	> 0.7 $\mu\text{m}$	> 2 $\mu\text{m}$	> 3 $\mu\text{m}$
L	> 0.7 $\mu\text{m}$	> 2 $\mu\text{m}$	> 10 $\mu\text{m}$
D	$\leq 1 \mu\text{m}$	$\leq 2 \mu\text{m}$	$\leq 5 \mu\text{m}$

(a) ~ (f) is ok but (g) ~ (j) is not allowed



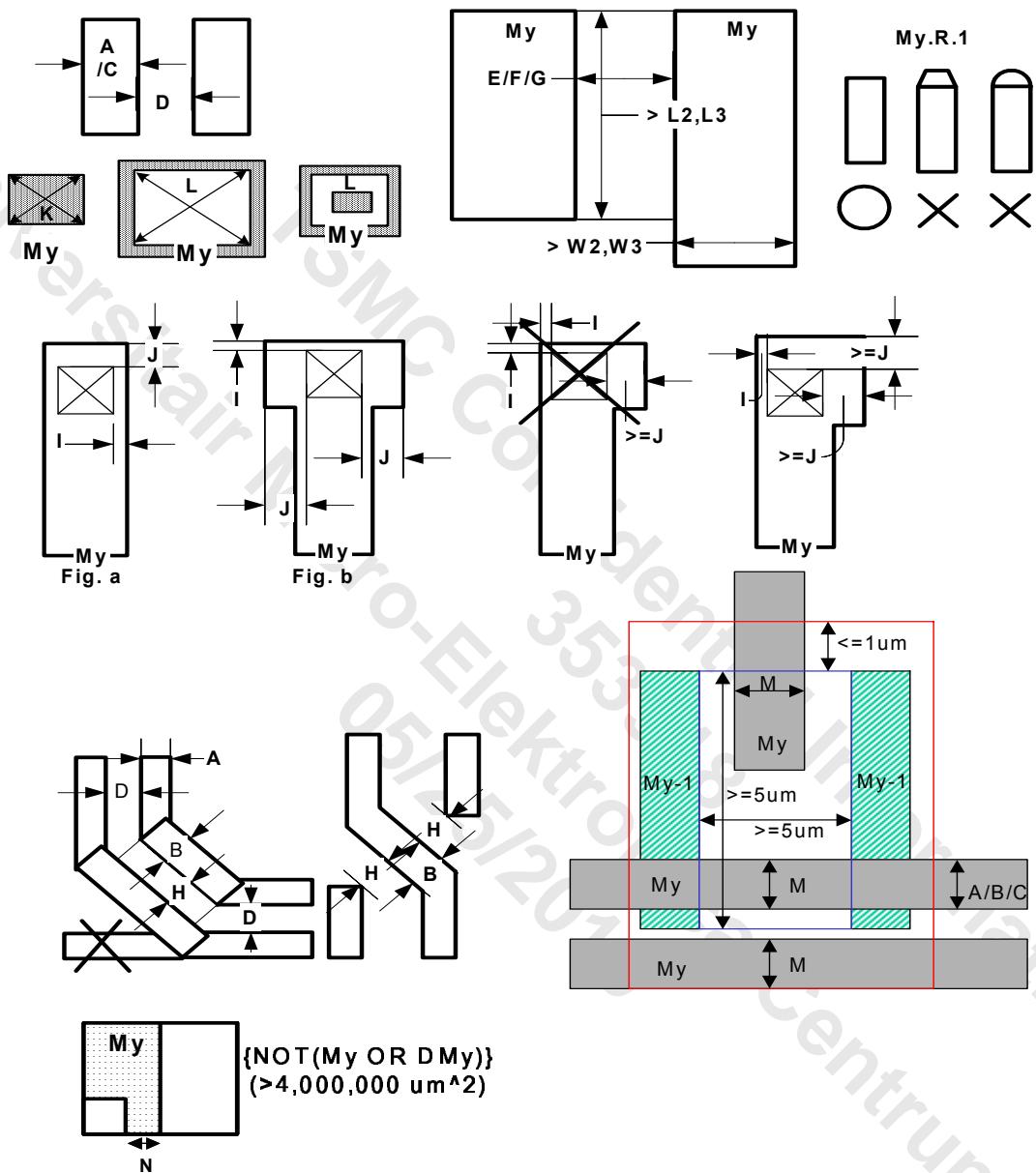
## 4.5.29 My Layout Rules (Mask ID: 381, 384, 385, 386, 387, 388, 389) (2XTM)

For the application of metal/vias stacking sequence and associated mask id, please refer to section 2.5.

Mn and My can not be used on the same die

Rule No.	Description	Label		Rule
My.W.1	Width	A	$\geq$	0.28
My.W.2	Width of 45-degree bent My Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)	B	$\geq$	0.39
My.W.3	Maximum width	C	$\leq$	12.00
My.W.4®	Recommended My width [My on (((My-1 OR DMy-1) with space $\geq$ 5x5μm) sizing 1)] for CMP uniformity	M	$\geq$	0.3
My.S.1	Space	D	$\geq$	0.28
My.S.3	Space [at least one metal line width > 1.5 μm (W2) and the parallel metal run length > 1.5 μm (L2)]	F	$\geq$	0.50
My.S.4	Space [at least one metal line width > 4.5 μm (W3) and the parallel metal run length > 4.5 μm (L3)]	G	$\geq$	1.50
	Note: When My width > 9um is used, please take care of the My.DN.2 rule by using larger space. For example, if two My with width 12um and space 1.5um, it will get 92.5% density violation on My.DN.2; either enlarger the My space (like 2um) or reduce the My width (like 9um) to meet My.DN.2.			
My.S.5	Space to 45-degree bent My	H	$\geq$	0.39
My.S.6®	Recommended space between two non-Mx regions [ one of the non-My area > 4,000,000μm <sup>2</sup> ]. Non-My region is defined as { NOT (My OR DMy) }. e.g. enlarge the metal width $\geq$ 0.35 for guard ring design.	N	$\geq$	0.35
My.EN.0®	Recommended enclosure of VIAy-1 is defined by either My.EN.1® or My.EN.2®.			
My.EN.1	Enclosure of VIAy-1	I	$\geq$	0.01
My.EN.1®	Recommended enclosure of VIAy-1 [VIAy-1 count $\leq=2$ in the region of (Mx AND My) or VIAy count $\leq=2$ in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	I	$\geq$	0.05
My.EN.2	Enclosure of VIAy-1 [at least two opposite sides]	J	$\geq$	0.05
My.EN.2®	Recommended enclosure of VIAy-1 [at least two opposite sides] [VIAy-1 count $\leq=2$ in the region of (Mx AND My) or VIAy count $\leq=2$ in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	J	$\geq$	0.08
My.A.1	Area	K	$\geq$	0.14
My.A.2	Enclosed area	L	$\geq$	0.49
	For the following My.DN.1, My.DN.2, My.DN.3, and DMy.R.1, please refer to the "Dummy Metal Rules" in Chapter 9 for the details.			
My.DN.1	Metal density range in the whole chip.		$\geq$	20% in 50x50
			$\leq$	80% in 100x100
My.DN.2	Maximum metal density over any 20 μm x 20 μm area (checked by stepping in 10 μm increments).		$\leq$	90%
My.DN.3	Metal density range within DMyEXCL		$\geq$	20% in 50x50
			$\leq$	80% in 100x100
My.R.1 <sup>U</sup>	My line-end must be rectangular. Other shapes are not allowed.			
DMy.R.1	DMy is a must. The DMy CAD layer (TSMC default, 38;1 for DM8) must be different from the My CAD layer.			

Guideline	Description		
My.R.2g <sup>U</sup>	For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance and the possibility of metal short. Please refer to section 10.1.1 and TSMC Reference Flow.		



## 4.5.30 MOM Layout Rules

- MOM is a fringe Metal-Oxide-Metal capacitor. It is based on the capacitance between parallel metal lines separated by the inter-level dielectric. The device does not require any additional masks.
- Although any kind of metal combination, M1/Mx/My/Mn/Mu/AP, is allowed to build a MOM element in terms of process, TSMC only provides a specific MOM SPICE model and the associated PDK cell named RTMOM which is covered by RTMOMDMY (CAD layer: 155;21) (see section 4.5.30.1)

	Non-RTMOM structure			RTMOM structure		
	SPICE	PDK	Process	SPICE	PDK	Process
M1	X	X	O	O	O	O
Mx	X	X	O	O	O	O
My/Mn/Mu/AP	X	X	O	X	X	O

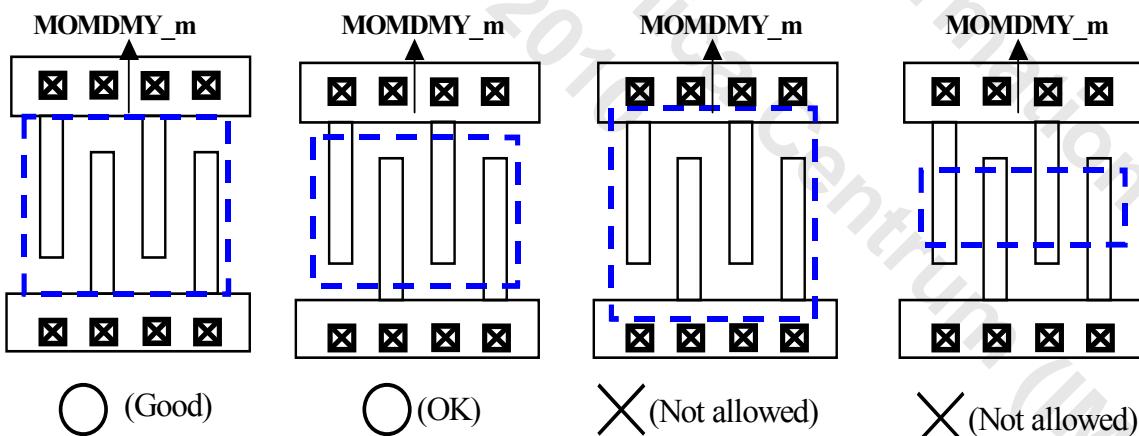
O: available X: not available

\*Mu is the ultra thick metal (34K Å) for the interconnection and inductor in the MS/RF process.

- MOMDMY\_m (m=1~9/AP) is a dummy layer for DRC/LVS to recognize the MOM region.

Layer name	CAD layer	Description	Non-RTMOM structure	RTMOM structure
MOMDMY_1	155;1	M1 MOM region	O	O
MOMDMY_2	155;2	M2 MOM region	O	O for Mx
MOMDMY_3	155;3	M3 MOM region	O	O for Mx
MOMDMY_4	155;4	M4 MOM region	O	O for Mx
MOMDMY_5	155;5	M5 MOM region	O	O for Mx
MOMDMY_6	155;6	M6 MOM region	O	O for Mx
MOMDMY_7	155;7	M7 MOM region	O	O for Mx
MOMDMY_8	155;8	M8 MOM region	O	
MOMDMY_9	155;9	M9 MOM region	O	
MOMDMY_AP	155;20	AP MOM region	O	

- In order to have a good DRC check, you need to draw the MOMDMY\_n carefully. The following examples are for your reference.

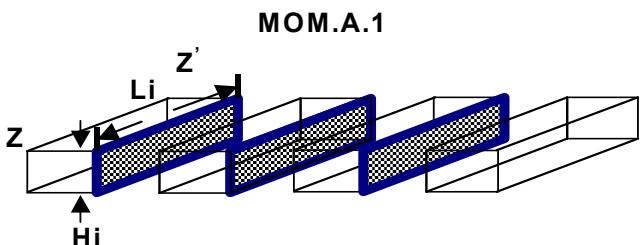
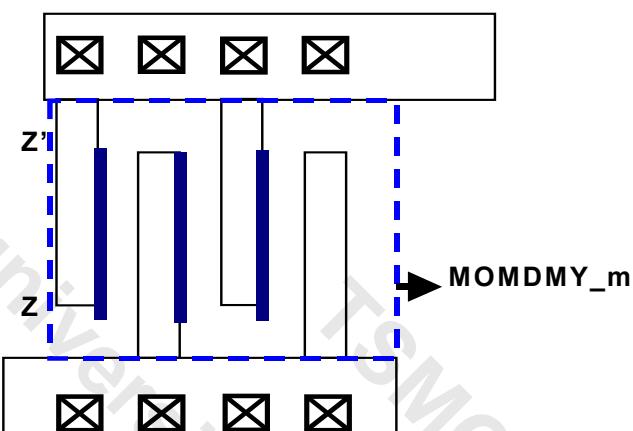


- You need to pay attention to meet the metal local density rule above/under the MOM element. Therefore, if you want to design a RF MOM circuit with a large area, it is recommended to connect several smaller MOM elements. And each element should be surrounded with dummy metals.
- The Multi-X Couple layout is recommended for large pair capacitors design to improve the matching performance (see section 4.5.30.1).
- Use symmetrical dummy metals around the matched pairs instead of automatically generated dummy metals.
- Carefully design wire access to capacitor terminals, and consider access to external metal lines to ensure an optimal symmetry of the device environment.
- The MOM PDK cell in TSMC is without Via.

Rule No.	Description	Label		Rule
	<b>Definition of MOM without Via</b> Count of {VIAM inside (Mm AND MOMDMY_m) AND (Mm+1 AND MOMDMY_m+1)} ≤ 4, (m=1~9/AP)			
MOM.A.1**	Maximum sidewall area of total metals in MOM without Via. For the definition of the sidewall area of total metals, please refer to the figure 4.5.30.1.	A	≤	2.77E8
	<b>Definition of MOM with Via</b> Count of {VIAM inside (Mm AND MOMDMY_m) AND (Mm+1 AND MOMDMY_m+1)} > 4, (m=1~9/AP)			
MOM.S.3	Space of Metal (M1/Mx) in MOM with Via [excluding the region of metal line end]	B	≥	0.14
MOM.S.4	Space of VIAx in MOM with Via in different net	C	≥	0.15
MOM.A.2**	Maximum sidewall area of {total metals+ total Vias} in MOM with Via. For the definition of the sidewall area of {total metals+ total Vias}, please refer to the figure 4.5.30.2.	D	≤	2.00E6

\*\*The rule value of MOM.A.1 and MOM.A.2 is based on the 3.3V operation voltage. If your layout violates these two rules and you don't apply 3.3V on the MOM application, please refer to the following table to waive the rules.

N90	Applied voltage				
	3.3V	2.5V	1.8V	1.2V	1.0V
MOM without Via	2.77E8	4.66E8	7.35E8	1.09E9	1.24E9
MOM with Via	2.00E6	3.37E6	5.31E6	7.86E6	8.95E6

**MOM without Via**

**A= Total metal sidewall area**

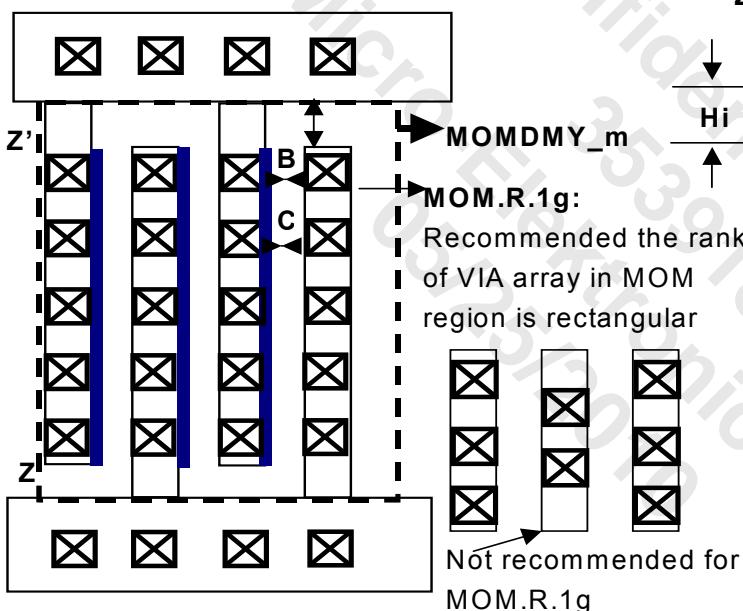
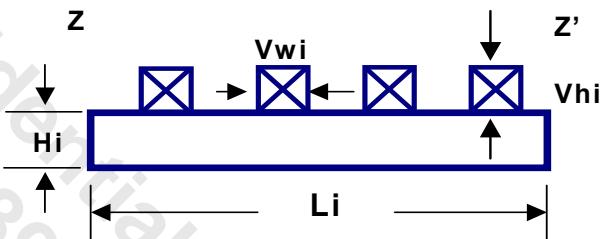
$$= \sum_{i=1}^n H_i \times L_i$$

**L<sub>i</sub>= finger length**

**H<sub>i</sub>= metal thickness**

**n=total metal finger number-1**

Figure 4.5.28.1

**MOM with Via****MOM.A.2**

**D= Via total sidewall area + Metal total sidewall area**

$$= \sum_{i=1}^n V_{wi} \times V_{hi} \times m + \sum_{i=1}^n H_i \times L_i$$

**V<sub>wi</sub>= via width**

**V<sub>hi</sub>= via height**

**H<sub>i</sub>= metal thickness**

**L<sub>i</sub>= metal length**

**m= total via number per finger**

**n= total metal finger number-1**

Figure 4.5.28.2

**Metal thickness and Via height (Å)**

M1	Mx	Mn	My	Mu	AP
2400	3100	8500	5600	34000	14500
	VIAx	VIAN	VIAy	VIAu	RV
	3200	7150	4500	7150	8000

## 4.5.30.1 RTMOM (Rotated Metal Oxide Metal) Capacitor Guidelines

This section lists the guidelines for TSMC offered RTMOM. The offered RTMOM is a fringe Metal-Oxide-Metal capacitor. It is based on the capacitor between parallel metal lines separated by the inter-level dielectric. The device does not require any additional mask..

1. Although any kind of metal combination, M1/Mx/My/Mz/Mr/Mu/AP, is allowed to build a MOM element in terms of process, TSMC only provides a specific MOM SPICE model and the associated PDK cell named RTMOM which is covered by MOMDMY (CAD layer: 155;21). (The TSMC offered PDK RTMOM is implemented by “Mx” or “Mx/M1”, at least three layers are required).

	Non-RTMOM structure			RTMOM structure		
	SPICE	PDK	Process	SPICE	PDK	Process
M1	X	X	O	O	O	O
Mx	X	X	O	O	O	O
My/Mn/Mu/AP	X	X	O	X	X	O

O: available X: not available

2. The poly-shielded layer is adopted to avoid RF performance degradation.
3. In order to avoid the OD density violation, RTMOM PDK provides an option of floating OD in OD2 under the poly-shielded pattern.
4. The Multi-X Couple layout is recommended for large-pair capacitor design, which can improve the matching performance. The Parallel and Multi-X Couple layout for match pairs is illustrated in Figure 4.5.30.1.1 and Figure 4.5.30.1.2.
  - The unit cell C1 and the unit cell C2 of the Multi-X Couple RTMOM are placed in an array with alternate pattern placement in each row and each column.
  - If the total capacitance  $C > 400\text{fF}$  is required, it is recommended to use Multi-X Couple layout type with unit cell  $< 200\text{fF}$ , to improve the matching performance. It is not recommended to use  $2 \times 200\text{fF}$  Parallel RTMOM design.

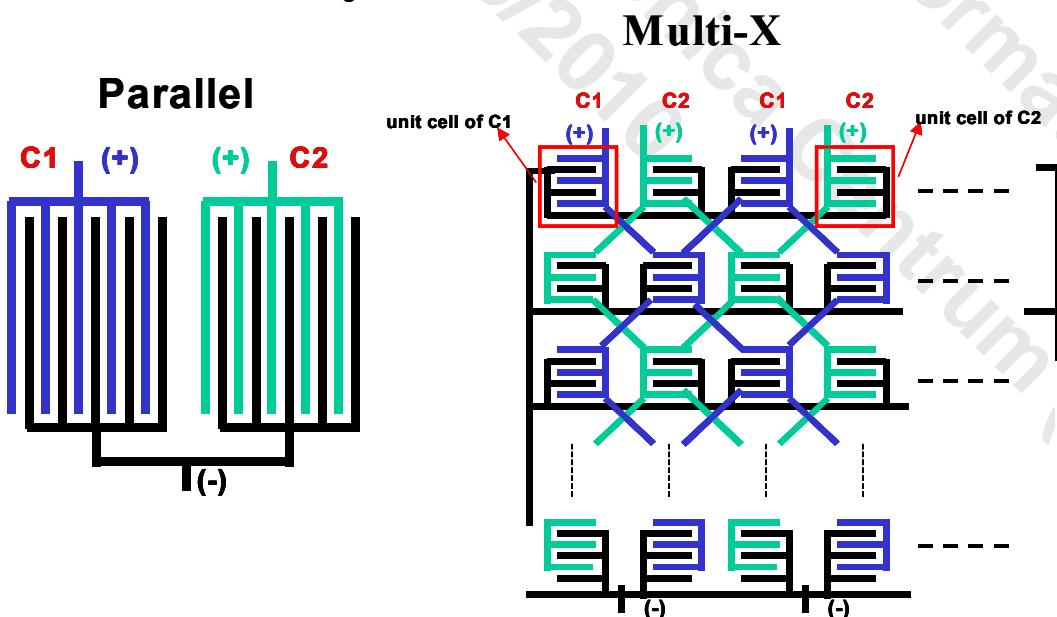


Figure 4.5.30.1.1

Figure 4.5.30.1.2

5. In order to make sure the SPICE simulation accuracy, and avoid the density rule violation, the following guidelines are recommended.

- The dummy metal exclusive layers (DMxEXCL) are adopted under RTMOM to avoid dummy pattern insertion. It is not recommended to place below/above the RTMOM any dummy metal patterns or routing. If dummy metal or routing (not generated by PDK itself) are added into the region below/above the RTMOM generated by PDK, the resulting extra parasitic and model inaccuracy must be taken into consideration by designers.
- If the metal density rule is violated due to the large area of RTMOM, parallel connected small RTMOMs array with dummy metals between individual RTMOM is recommended, as shown in Figure 4.5.30.1.3.

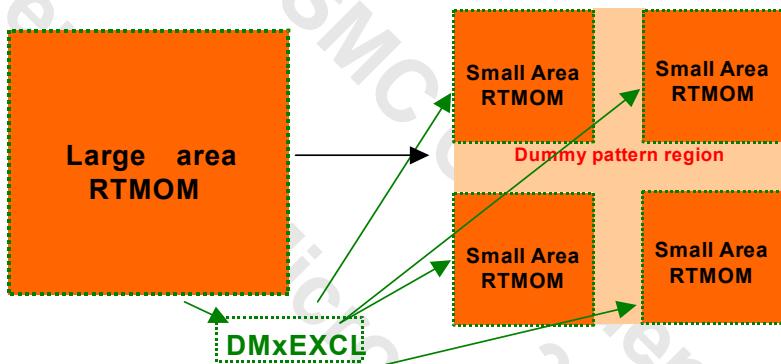


Figure 4.5.30.1.3

## 4.5.31 Via Layout Recommendations

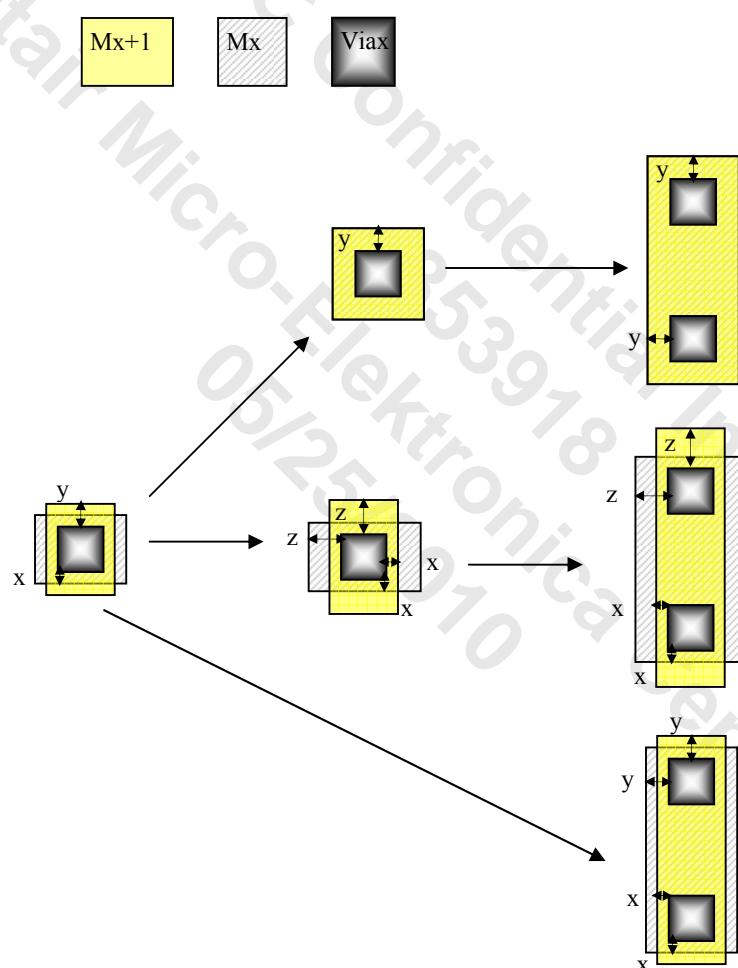
For better yield and reliability, use of a commercial auto router or TSMC utility is recommended to add redundant vias and bigger metal enclosures wherever the layout allows. Please refer to the most updated “T-N90-LO-DR-001-X4, TSMC 90NM DFM LAYOUT ENHANCEMENT UTILITY”. You can download the document from TSMC-Online (Design Portal—Reference Flow) for the reference of redundant vias insertion at auto router.

**Annotation:**

x: value of minimum extension rule (5 nm) (VIAx.EN.1 and Mx.EN.1) or (5 nm) (VIAY.EN.1 and MY.EN.1)

y: value of recommended extension (50 nm) (VIAx.EN.1® and Mx.EN.1®) or (50 nm) (VIAY.EN.1® and MY.EN.1®), same as line-end extension rule (VIAx.EN.2 and Mx.EN.2) or (VIAY.EN.2 and MY.EN.2).

z: value of recommended line-end extension value (80 nm) (VIAx.EN.2® and Mx.EN.2®) or (80 nm) (VIAY.EN.2® and MY.EN.2®).



## 4.5.32 Product Labels and Logo Rules

**1. Use any of the following product labels:**

- o Copyright and year
- o Company logo
- o Part number
- o Mask level names
- o Other similar labels

**2. Make sure there is a dummy layer LOGO (CAD layer no. 158) to do DRC for product labels.**

Product labels must be fully covered by LOGO dummy layer.

**3. Form the product labels for the CO/Via layer by using squares with minimum width.**

A big CO/Via polygon for a character (or a numeral) is not allowed.

**4. Don't use minimum rules for the product labels, except for CO/Vias.**

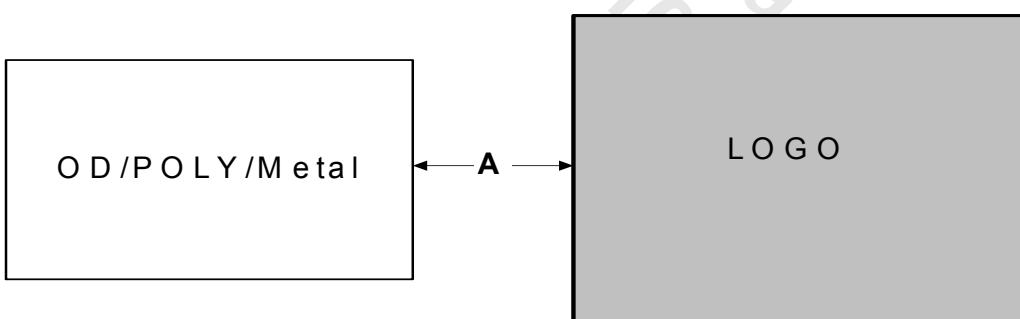
It is best to have greater than, or equal to, 1  $\mu\text{m}$  of width and space. If the minimum width and space is greater than 1  $\mu\text{m}$  in the rule (for example, 30K thick metal) please use at least the minimum width and space.

**5. To protect the product labels, do not use a dummy OD/Poly/Metal in the LOGO demarcated regions.**

For process uniformity, keep the LOGO layer and the corresponding product labels at least 10  $\mu\text{m}$  distant from the OD/PO/Metal geometry. Add dummy fill in this 10  $\mu\text{m}$  border region. (The TSMC dummy pattern utility will insert dummy pattern geometry in the 10  $\mu\text{m}$  LOGO border region to minimize the process impact on the circuit OD/PO/Metal geometry that is near the LOGO.)

**6. To protect the product labels and process uniformity consideration, do not use circuits in the LOGO demarcated regions.**

Rule No.	Description	Label		Rule
LOGO.S.1	Space to OD, PO, or Metals (non-dummy patterns)	A	$\geq$	10
LOGO.O.1	Overlap of CB, CBD, FW, PM, UBM, DOD, DPO, or DMx is not allowed.			
LOGO.R.1 <sup>U</sup>	A circuit in the LOGO is not allowed.			
LOGO.R.2	The rules of PO.EX.1, PO.EX.2, PO.EX.2®, PO.EX.3, PO.R.1, and PO.R.4 can be exempted from DRC in LOGO area.			



## 4.5.33 SRAM Rules

Rule No.	Description			
SRAM.W.1	(Width of SRM) interact with OD. The SRM edge should be aligned to the boundary of the cell array, which may include storage, strapping, and dummy edge cells.	A	$\geq$	0.62
SRAM.EX.1	(SRM extension on NW) interact with OD. Extension = 0 is allowed.	B	$\geq$	0.62
SRAM.R.1 <sup>U</sup>	<b>Customer-designed SRAM bit cell:</b> Review by TSMC's R&D and PE before use a customer-designed SRAM bit cell. It is recommended to use the standard TSMC SRAM cells including core, edge, and strap cells. If non-standard cells are used, TSMC requires you to submit a layout at least one month before tape-out for TSMC to review and approve the use of SRAM cells.			
SRAM.R.2 <sup>U</sup>	<b>Logic SPICE model:</b> Don't use TSMC logic SPICE model to design SRAM unless the layout strictly follows the logic design rule for designing SRAM. TSMC's R&D and PE must review the SRAM layout.			
SRAM.R.3 <sup>U</sup>	<b>Redundancy:</b> If the accumulated SRAM density is greater than 4.0M bits, redundancy is needed. The accumulated SRAM density is normalized density of <b>0.999um<sup>2</sup></b> cell size. Please refer to the most current version of the TSMC Embedded SRAM Redundancy Implementation Rule ( <i>T-000-CL-RP-002</i> ).			
SRAM.R.4 <sup>U</sup>	<b>SRAM cell implant:</b> TSMC provides the following V <sub>t</sub> implants in SRAM cells (see the table 4.5.33.1, table 4.5.33.2 and table 4.5.33.3): <b>Cell implant for NMOS (VTC_N):</b> You must provide a special layer SRM. The VTC_N layer is derived from logical operations using "SRM" marker layer.			
SRAM.R.5 <sup>U</sup>	<b>Array delay-tracking bit cells:</b> This kind of bit cell should be embedded inside an array. If a delay-tracking cell is to be placed outside an array, it should be fully surrounded by dummy bit cells.			
SRAM.R.6 <sup>U</sup>	<b>Dummy layouts for embedded SRAM:</b> To minimize proximity and loading effects during processing, you must add dummy layouts to provide a similar surrounding for every cell. To add dummy layouts, please refer to SRAM cell layout documents for guidelines and GDS examples. These documents provide instructions for adding dummy layouts in both columns and rows, at array edges, and at the connection/tap in-between arrays.			
SRAM.R.7 <sup>U</sup>	<b>SRAMDMDY (186;4):</b> Can only use in the word-line decoder of TSMC SRAM(0.999um <sup>2</sup> and 1.15um <sup>2</sup> ). This layer is only to waive CO.S.3 and G.1. And it must be reviewed by TSMC's R&D and PE even if you uses TSMC cell.			
SRAM.R.12	SRAMDMDY (186;4) overlap SRAMDMDY (186;0) is not allowed.			
SRAM.R.13	SRM must fully cover GATE.			
Guidelines	Description			
SRAM.R.8g <sup>U</sup>	<b>SRAM device length/width:</b> To avoid Pass Gate (PG) leakage impact on SRAM cell electrical performance, the PG gate length should be $\geq 0.11 \mu\text{m}$ . The PG gate width should be $\geq 0.12 \mu\text{m}$ . The minimum enclosed OD area is $0.59 \mu\text{m} \times 1.02 \mu\text{m}$ (STD HD $1.27 \mu\text{m}^2$ SRAM cell). Consult with TSMC regarding the SRAM cell's electrical performance and the suppression of accumulated pass-gate leakage on a bit line.			
SRAM.R.9g <sup>U</sup>	<b>Sense-amp and decoder redundancy:</b> In addition to bit-row and/or bit-column redundancy design, redundancy in peripheral array elements, such as sense amplifiers and decoders, is recommended. Architectural efficiency can minimize the added overhead area entailed by this additional redundancy. Peripheral element redundancy is especially important for high-density memory blocks.			
SRAM.R.10g <sup>U</sup>	<b>Bit cell orientation:</b> It is recommended to place the bit cells of related SRAM blocks in the same orientation. The overall Poly CD uniformity improvement is 0.5nm. The vertical and horizontal poly CD may have 2nm difference in the worse case as the poly orientation is different.			
SRAM.R.11.g <sup>U</sup>	<b>Guardring:</b> It is recommended to have an additional VSS (PW) guardring around the memory circuit block.			
SRAM.R.14g <sup>U</sup>	Avoid placing SRAM at the chip corner and chip edge. (Please refer Figure 8.5.7 in Chapter 8)			

**Table 4.5.33.1 90nm TSMC SRAM Cells Mask Requirement Summary**

Process Type	N90G		N90GT		N90LP		
SRAM Rule	UHD	DP	UHD	DP	UHD	HD	DP
Cell Size	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.15um <sup>2</sup>	1.99um <sup>2</sup>
NMOS VT	std VT+ VTC_N		std VT+*HVT_N+VTC_N			std VT+VTC_N+HVT_N	
PMOS VT	std VT		std VT+*HVT_P			std VT+HVT_P	

\*In N90GT cells, HVT\_N/HVT\_P masks are automatically generated by logical operations from SRM & N-Well layers.

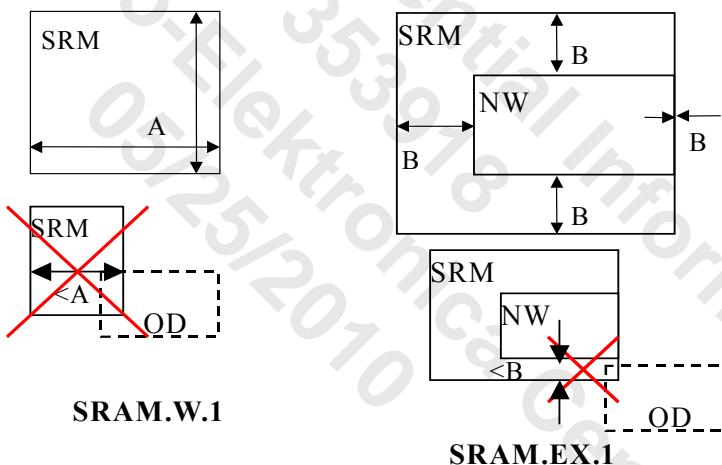
**Table 4.5.33.2 85nm TSMC SRAM Cells Mask Requirement Summary**

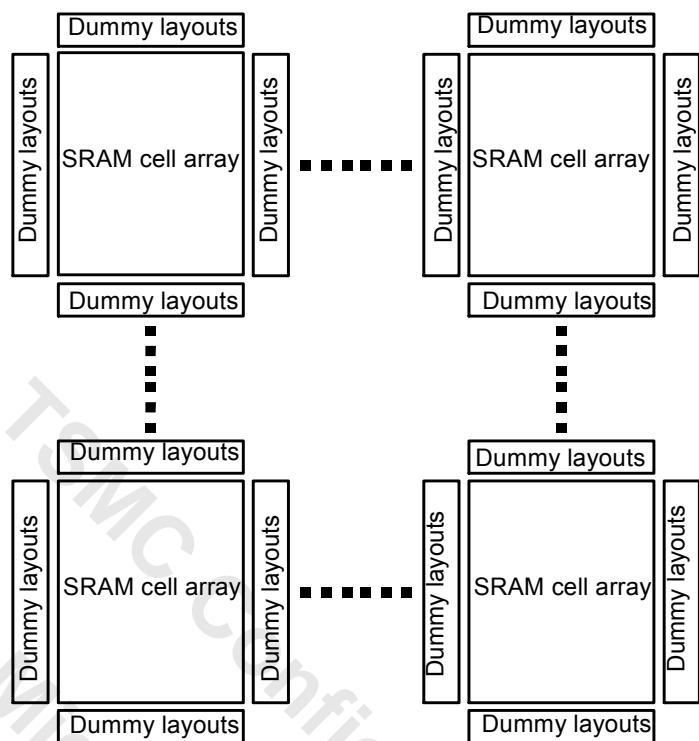
Process Type	N85G		N85LP		
SRAM Rule	UHD	DP	UHD	SP	DP
Cell Size	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.15um <sup>2</sup>	1.99um <sup>2</sup>
NMOS VT	std VT+ VTC_N			std VT+VTC_N+HVT_N	
PMOS VT	std VT			std VT+HVT_P	

**Table 4.5.33.3 80nm TSMC SRAM Cells Mask Requirement Summary**

Process Type	N80GC		N80GT		N80HS		N80LP
SRAM Rule	UHD	DP	UHD	DP	UHD	DP	SP
Cell Size	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	1.15um <sup>2</sup>
NMOS VT	std VT+ VTC_N			std VT+VTC_N+*HVT_N		std VT+ VTC_N	
PMOS VT	std VT		std VT+*HVT_P			std VT+*HVT_P	

\*In N80GT/HS cells, HVT\_N/HVT\_P masks are automatically generated by logical operations from SRM & N-Well layers.





## 4.5.34 Metal Fuse Layout Rules

Please refer to Document no.: T-N90-LO-DR-003 for Cu fuse and T-000-CL-DR-005 for AP fuse.

## 4.5.35 Chip Corner Stress Relief Pattern (CSR) Layout Rules

### 4.5.35.1 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns

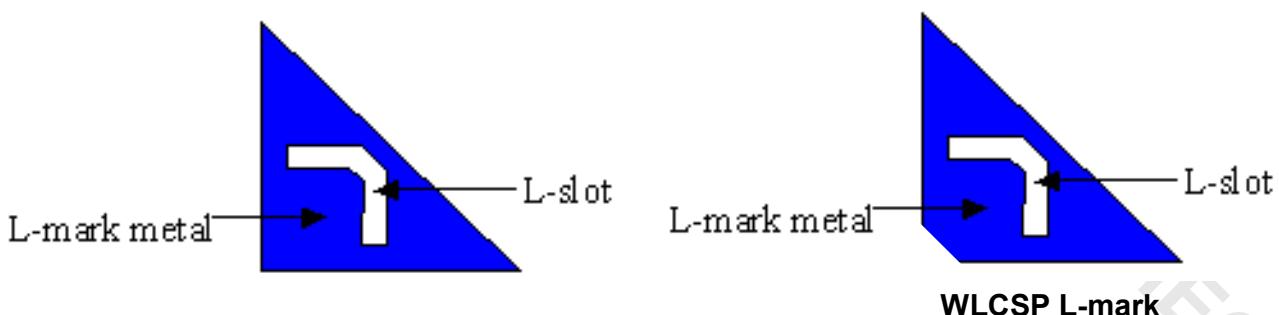
- The chip corner stress relief pattern can reduce the impact of damage induced by thermal stress during packaging and field applications.
- You can request TSMC to add the CSR pattern and the seal ring, and only CSR.R.1 in the following table must be met. If you want to add the CSR patterns and the seal ring by yourself, then you can use TSMC-offered sample GDS file (attached in this document) by following the CSR rules of this section (except CSR.R.1), and the seal ring rules.
- Standard seal ring structures:
  - Sample GDS file for 3XTM L-mark seal-ring corner: N90SR\_3XTM\_L-mark\_8KX8K\_20051110.gds
  - Sample GDS file for 3XTM big seal-ring corner: N90SR\_3XTM\_BIG\_8KX8K\_20051110.gds
  - Sample GDS file for 3XTM small seal-ring corner: N90SR\_3XTM\_SML\_1KX1K\_20051110.gds
  - Sample GDS file for 2XTM L-mark seal-ring corner: N90SR\_2XTM\_L-mark\_8KX8K\_20051110.gds
  - Sample GDS file for 2XTM big seal-ring corner: N90SR\_2XTM\_BIG\_8KX8K\_20051110.gds
  - Sample GDS file for 2XTM small seal-ring corner: N90SR\_2XTM\_SML\_1KX1K\_20051110.gds
  - For UTM sealring, please refer to section 4.6.10, the chip corner stress relief pattern (CSR) and seal ring rules for UTM.
- TSMC offers new sealring structures in WLCSP.
  - Sample GDS file for 3XTM L-mark seal-ring corner: N90SR\_3XTM\_L-mark\_20091022\_WLCSP.gds
  - Sample GDS file for 2XTM L-mark seal-ring corner: N90SR\_2XTM\_L-mark\_20091022\_WLCSP.gds
  - For UTM sealring, please refer to section 4.6.10, the chip corner stress relief pattern (CSR) and seal ring rules for UTM.
- Mask combination CB (mask ID: 107)/ AP (mask ID: 307)/ CB (mask ID: 107) is not allowed for WLCSP process.
- An alignment mark (L-mark) is drawn at each chip corner in the L-mark seal-ring corner. You can use this L-mark for the laser alignment of ID number verification or the metal fuse cutting purpose. If these L-marks can not meet your testing house requirement, you can find the L-mark rules in the metal fuse design rule document.
- It is recommended to use L-mark seal ring.
  - L-mark sealring is recommended to be used for new tapeouts.
  - Existing products is to use previous CSR structures (Big/Small or L-mark).
  - Whatever kind of sealring you use, please take care of the option of the dummy filling. If you use L-mark sealring, please also use L-mark sealring option in the dummy-filling utility to make sure that dummy filling can be filled correctly.

- The Reference coordinates of L-mark:** You can calculate the coordinates of L-mark by yourself, or follow the coordinates of the below table.

(Chip_X, Chip_Y) are the dimensions of the chip (without sealring and assembly isolation)			
L-Mark Coordinates ( $\mu\text{m}$ )	Coordinate A	Coordinate B	Coordinate C
	<p>Sealring+Assembly</p> <p>Chip_Y (0,0)</p> <p>Chip_X</p> <p>L1</p> <p>L2</p> <p>L3</p> <p>L4</p>	<p>Sealring+Assembly</p> <p>Chip_Y</p> <p>Chip_X</p> <p>L1</p> <p>L2</p> <p>L3</p> <p>L4</p>	<p>Sealring+Assembly</p> <p>Chip_Y</p> <p>Chip_X</p> <p>L1</p> <p>L2</p> <p>L3</p> <p>L4</p>
	(0, 0) is at the center of the chip	(0, 0) is at bottom-left of the chip with sealring (10um) and assembly isolation (10um)	(0, 0) is at bottom-left of the chip without sealring (10um) and assembly isolation (10um)
<b>L1</b>	(-0.5X+14.25, -0.5Y+14.25)	(34.25, 34.25)	(14.25, 14.25)
<b>L2</b>	(-0.5X+14.25, 0.5Y-14.25)	(34.25, Y+5.75)	(14.25, Y-14.25)
<b>L3</b>	(0.5X-14.25, 0.5Y-14.25)	(X+5.75, Y+5.75)	(X-14.25, Y-14.25)
<b>L4</b>	(0.5X-14.25, -0.5Y+14.25)	(X+5.75, 34.25)	(X-14.25, 14.25)

- L-mark metal:** a solid metal (top Cu metal) with an L shaped hole in LMARK.
- L-mark metal in CSR:** L-mark metal in a CSR pattern.
- L-slot:** L shaped hole in an L-mark metal
- L-mark metal layer:** Only one top Cu metal is required for L-mark metal, and AP for L-mark metal is not allowed.

	Without Cu RDL (MD)								With Cu RDL (MD)							
	1P3M	1P4M	1P5M	1P6M	1P7M	1P8M	1P9M	1P3M	1P4M	1P5M	1P6M	1P7M	1P8M	1P9M		
L-mark metal layer	M3	M4	M5	M6	M7	M8	M9	MD	MD	MD	MD	MD	MD	MD	MD	MD



## General Information

Chip-corner stress relief pattern and seal ring structures are based on the 1P9M process :

- The square CO/Via must follow each layer's width rule.
- For more than two top-metal layers (Mn or My) with generic top-metal thickness, the Via (VIAn-1 or VIAy-1) below the thick metal (Mn or My) must follow CSR.S.3, CSR.EN.3, and the VIAn or VIAy rules.
- Please be careful with the non-generic logical operation, CAD bias, and shrinkage effects on the drawn dimensions of a stress relief pattern and seal ring.
- CSRDMY is a dummy marker layer aligned to the boundary of the stress relief pattern for DRC.

### For a flip-chip product without AP-MD

- The CBD (mask code 107) layout is same as the CB layout.
- Please draw the AP (mask code 307) layer on the seal ring as shown in this chapter, in the "Chip Corner Stress Relief Pattern" section and in the "Seal Ring Rules" section.
- Don't draw the UBM (mask code 020) layout on the chip-corner stress relief pattern, seal ring, and assembly isolation structures. No UBM metal is allowed in these regions.

### For a product with AP-MD

- The CB-VD (mask code 306) and CB2 (mask code 107) layout is same as the CB layout.
- Please draw the AP-MD (mask code 309) layer on the seal ring.
- Don't draw the UBM (mask code 020) layout on the chip-corner stress relief pattern, seal ring, and assembly isolation structures. No UBM metal is allowed in these regions.

**Layer usage due to different metal combination:**

	One thick metal (Mn or My) without Cu RDL (MD)						One thick metal (Mn or My) with Cu RDL (MD)					
	1P3M	1P4M	1P5M	1P6M	1P7M	1P8M	1P3M	1P4M	1P5M	1P6M	1P7M	1P8M
M1	31	31	31	31	31	31	31	31	31	31	31	31
VIA1	51	51	51	51	51	51	51	51	51	51	51	51
M2	32	32	32	32	32	32	32	32	32	32	32	32
VIA2	58*	52	52	52	52	52	57*	52	52	52	52	52
M3	39*	33	33	33	33	33	38*	33	33	33	33	33
VIA3		58*	53	53	53	53		57*	53	53	53	53
M4		39*	34	34	34	34		38*	34	34	34	34
VIA4			58*	54	54	54			57*	54	54	54
M5				39*	35	35			38*	35	35	35
VIA5					58*	55				57*	55	55
M6					39*	36				38*	36	36
VIA6						58*	56				57*	56
M7						39*	37				38*	37
VIA7							58*					57
M8							39*					38
VIAD								167	167	167	167	167
MD								168	168	168	168	168

	Two thick metal (Mn or My) without Cu RDL (MD)						Two thick metal (Mn or My) with Cu RDL (MD)					
	1P4M	1P5M	1P6M	1P7M	1P8M	1P9M	1P4M	1P5M	1P6M	1P7M	1P8M	1P9M
M1	31	31	31	31	31	31	31	31	31	31	31	31
VIA1	51	51	51	51	51	51	51	51	51	51	51	51
M2	32	32	32	32	32	32	32	32	32	32	32	32
VIA2	57*	52	52	52	52	52	57*	52	52	52	52	52
M3	38*	33	33	33	33	33	38*	33	33	33	33	33
VIA3	58*	57*	53	53	53	53	57*	57*	53	53	53	53
M4	39*	38*	34	34	34	34	38*	38*	34	34	34	34
VIA4		58*	57*	54	54	54		57*	57*	54	54	54
M5		39*	38*	35	35	35		38*	38*	35	35	35
VIA5			58*	57*	55	55			57*	57*	55	55
M6			39*	38*	36	36			38*	38*	36	36
VIA6				58*	57*	56				57*	57*	56
M7				39*	38*	37				38*	38*	37
VIA7					58*	57					57*	57
M8						39*	38				38*	38
VIA8							58					57*
M9							39					38*
VIAD								167	167	167	167	167
MD								168	168	168	168	168

- Based on the different metal combination, please extract the above the layer number.

\* Please transfer the above CAD layers to the correct layer number in your definition.

## 4.5.35.2 Chip Corner Stress Relief Pattern (CSR) Layout Rules

Rule No.	Description	Label	Rule
CSR.R.1	Empty areas in four chip corners must be reserved and no layout is allowed inside if you request TSMC to add a chip corner stress relief pattern (CSR) and a seal ring. Fig. a shows the <i>big seal-ring corner</i> . Fig. b shows the <i>small seal-ring corner</i> . Fig. C shows the <i>L-mark seal-ring corner</i> .		


**Warning:**

Violation of the CSR.R.1 rule may result in a serious layout mistake, and, therefore, many masks might need corrections. Please review the mask data after TSMC adds the stress relief pattern and seal ring.

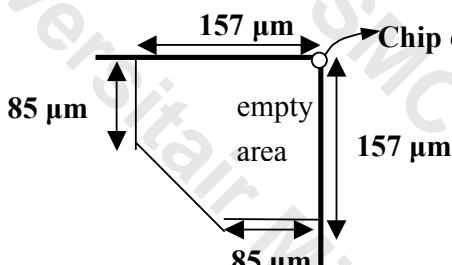


Fig.a Big seal-ring corner

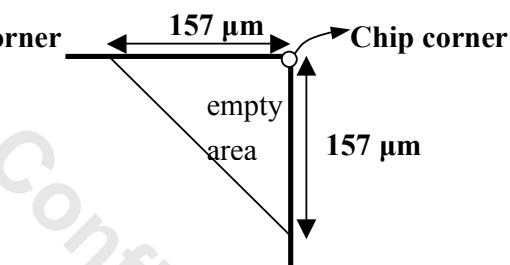


Fig.b Small seal-ring corner

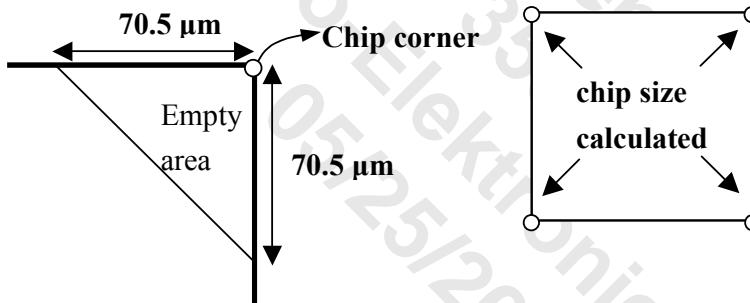


Fig.c L-mark seal-ring corner

**Rules that apply to customer-added stress relief patterns and seal rings:**

CSR.R.2	The CSR structure must include M9/M8 (top metal), VIA8/VIA7 (top via), M7, VIA6. . . . , VIA1, M1, CO, PP, and OD layers. CSR is a fence type structure formed by crossed 1.5 μm metals with CO/Via located at the metal crossing. Therefore, fully overlapped vias and metals of all levels (except top vias) are formed.			
CSR.S.1	CO space	A1	$\geq$	0.320
CSR.EN.1 <sup>U</sup>	CO enclosure by metal [crossing area]	B1	$\geq$	0.190
CSR.S.2	VIAx space at the same level	A2	$\geq$	0.290
CSR.EN.2 <sup>U</sup>	VIAx enclosure by metal [crossing area]	B2	$\geq$	0.175
CSR.S.3	VIAx or VIAy space	A3	$\geq$	0.400
CSR.EN.3 <sup>U</sup>	VIAx or VIAy enclosure by metal [crossing area]	B3	$\geq$	0.190
CSR.R.3 <sup>U</sup>	(CO/VIAx, VIAx/VIAy) number at the metal crossing area	D	$\geq$	(9, 4)
CSR.W.1	Width of L-slot	a	=	10
CSR.L.1	Length of L-slot	b	$\geq$	20
			$\leq$	25

Rule No.	Description	Label		Rule
CSR.EN.4	L-mark metal in CSR enclosure of L-slot [in the direction of the L-slot length] (Except WLCSP sealring region)	c	$\geq$	4
			$\leq$	6
CSR.EN.4.1	L-mark metal in CSR enclosure of L-slot [in the direction of the L-slot length] for WLCSP sealring region	c	$\geq$	4
			$\leq$	7
CSR.EN.5	L-mark metal in CSR enclosure of L-slot [perpendicular to the direction of the L-slot length] (Except WLCSP sealring region)	c'	$\geq$	28
			$\leq$	29
CSR.EN.5.1	Metal layers of sealring corners can only exist isosceles triangle for WLCSP sealring region. An empty isosceles triangle area must exist butted to the WLCSP sealring outside corner.			
	Minimum length of isosceles triangle		$\geq$	18.5
	Maximum length of isosceles triangle		$\leq$	19.5
CSR.W.2	Width of 45 degree corner of L-slot	d	$\geq$	6
			$\leq$	8
CSR.W.3	Width of Via ring (CO/VIAx/VIA <sub>n</sub> /VIAy) around CSR pattern and L-slot	e	=	0.12/0.13/0.28/ 0.13
CSR.EN.6	Metal enclosure of (CO, VIAx, VIA <sub>n</sub> , VIAy ) around L-slot	f	$\geq$	0.52
CSR.EN.7	Metal enclosure by L-mark metal in CSR around the L-slot	g	$\geq$	0.25

### 4.5.35.3 Chip Corner Stress Relief (CSR) Pattern

#### 4.5.35.3.1 Big Seal-ring Corner and Small Seal-ring Corner

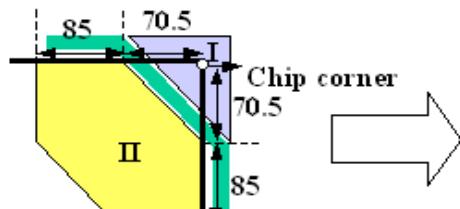


Fig. 1a, big seal-ring corner

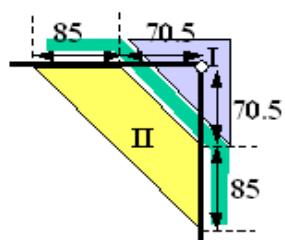


Fig. 1b, small seal-ring corner

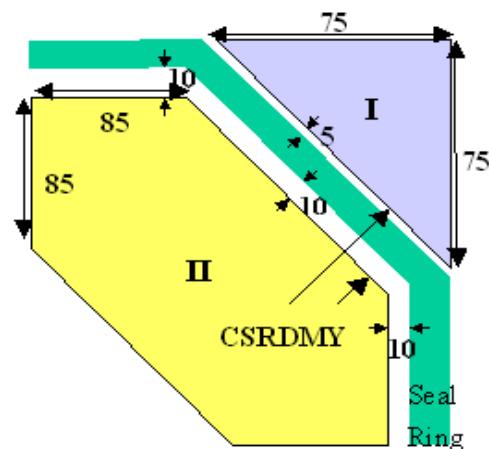
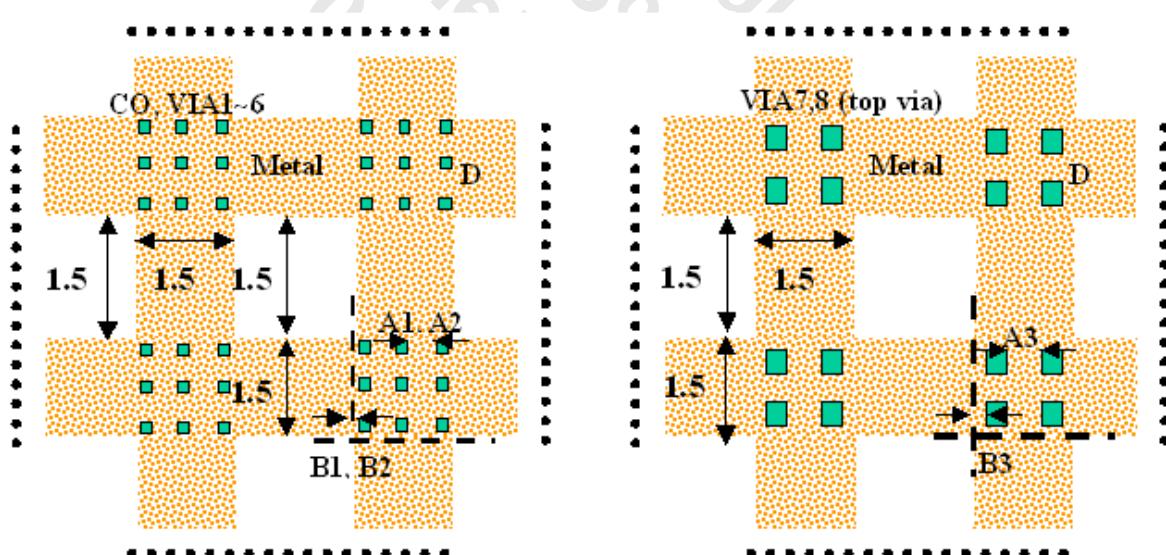


Fig. 1c

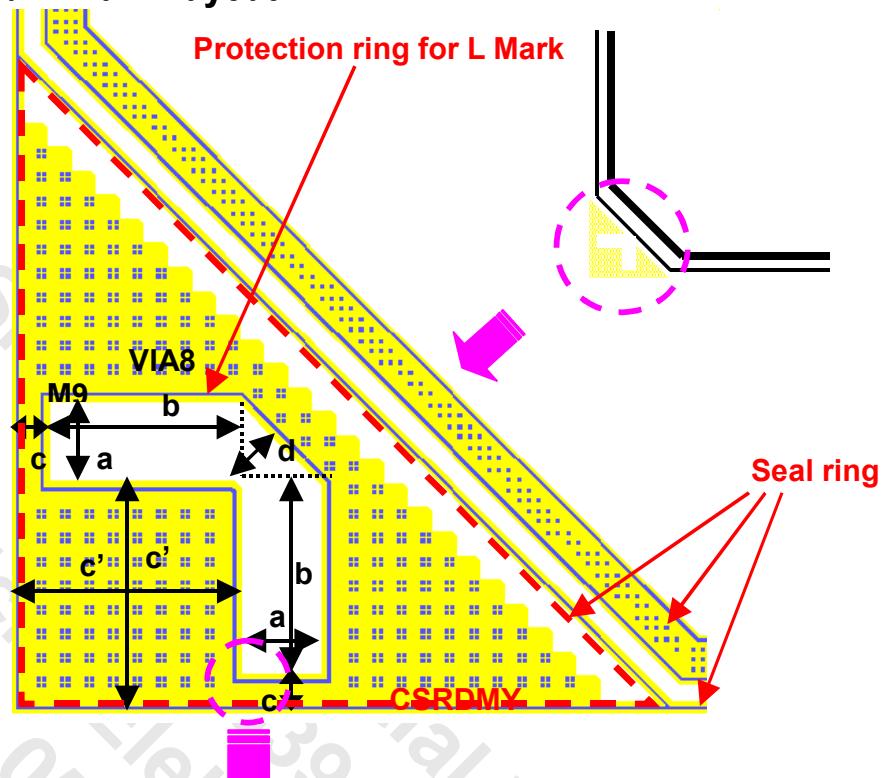
Within region I and II, designer must add a dummy pattern for chip corner stress relief, shown with the following examples.



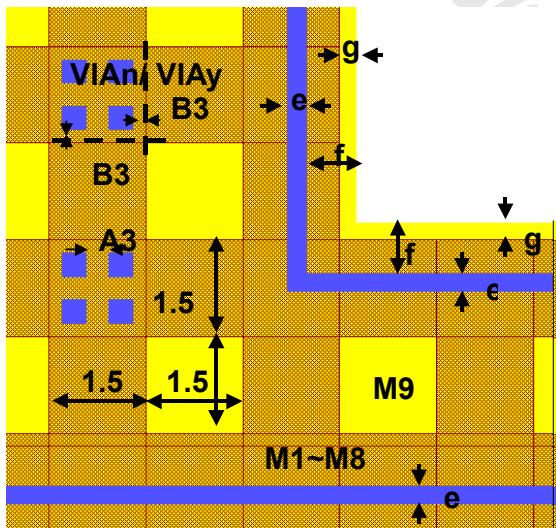
Connected to PP/OD

#### 4.5.35.3.2 L-mark Seal-ring Corner

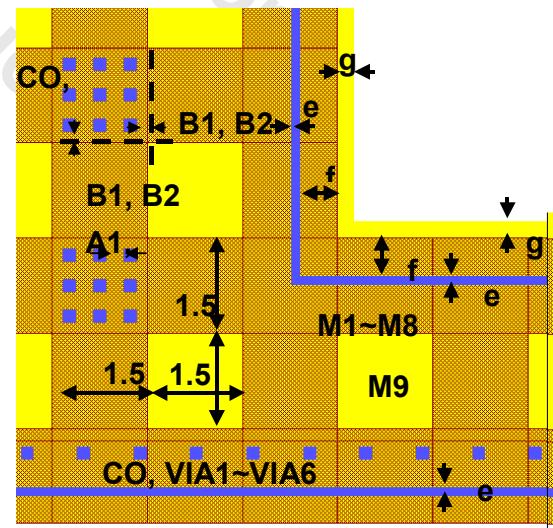
Top view and L-mark Layout



VIAN/ VIAy and metal Layout

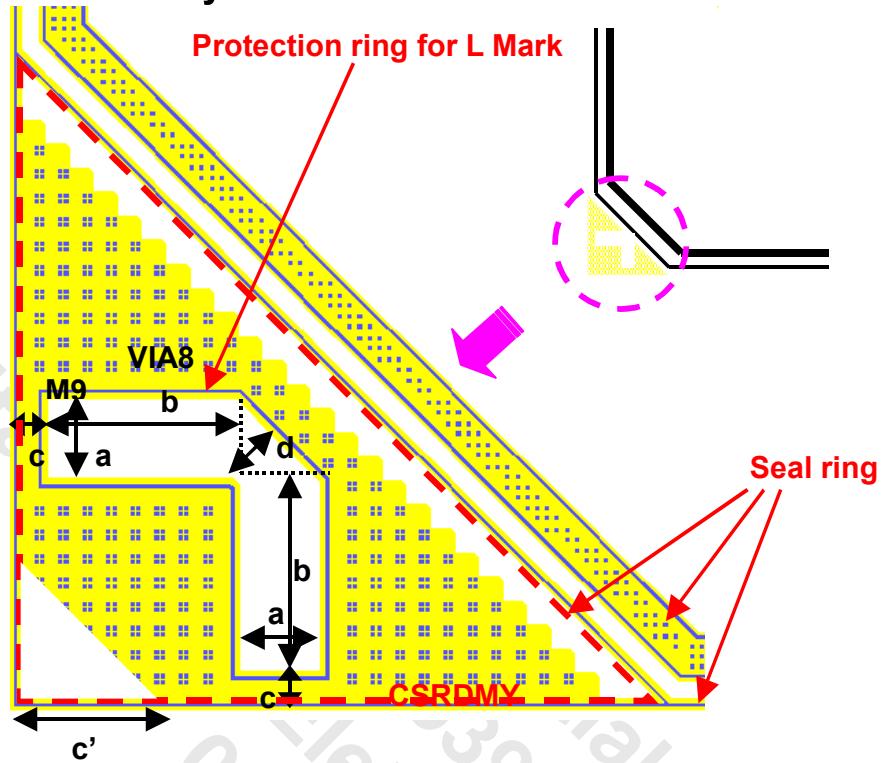


CO/VIA1/VIAx and Metal Layout



#### 4.5.35.3.3 L-mark Seal-ring Corner for WLCSP

##### Top view and L-mark Layout



## 4.5.36 Seal Ring Layout Rules

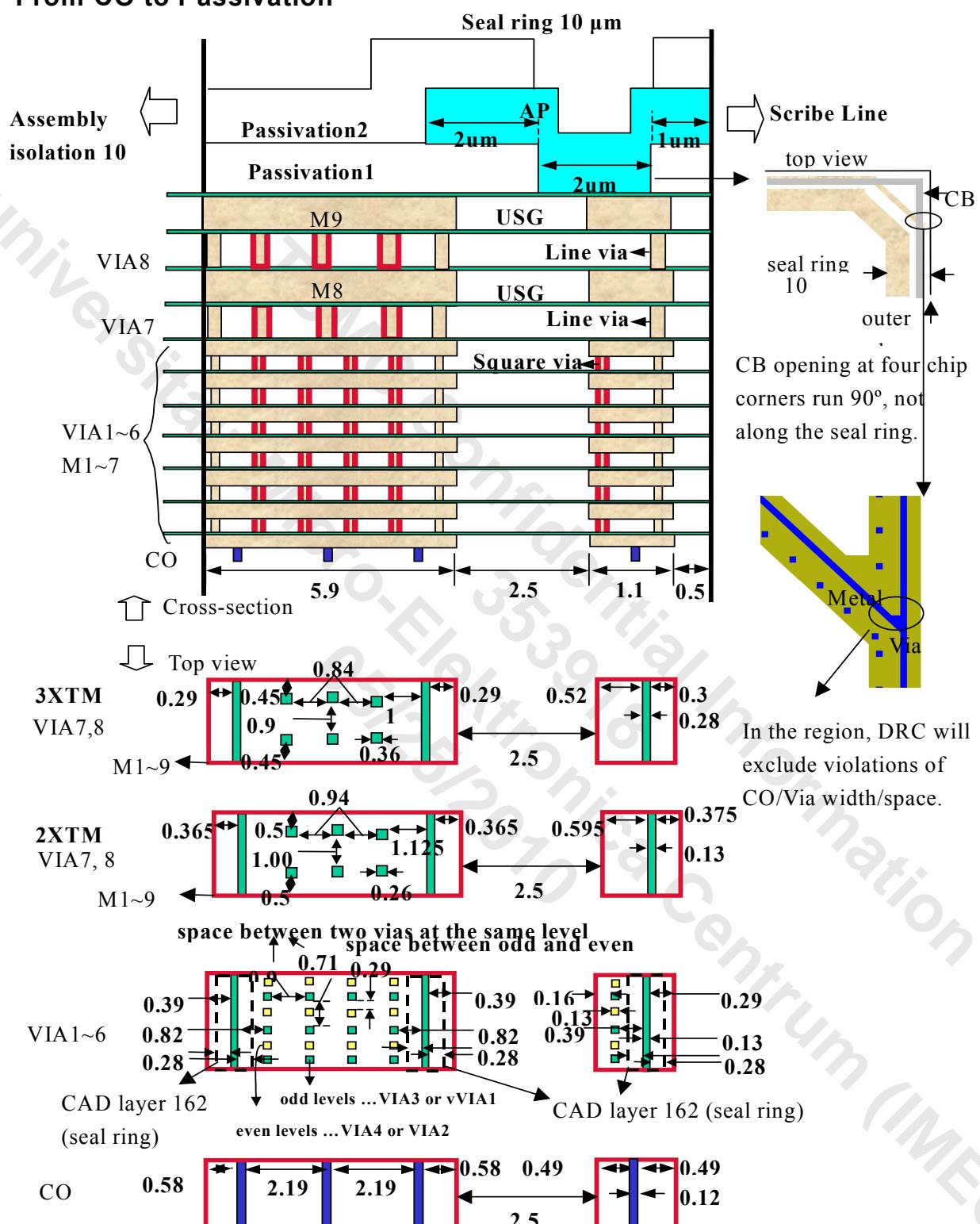
Please follow exactly the schematic diagram in Figure a. for a seal ring layout—as in the GDS example. Currently, DRC can't fully check the seal-ring layout dimensions. If you want to use dimensions other than those shown in Figure a., please consult with TSMC.

If TSMC adds a seal ring, TSMC will also add an assembly isolation and a seal ring structure at the same time. An AI pad (AP) can be generated by logic operation only for a non-flip-chip product.

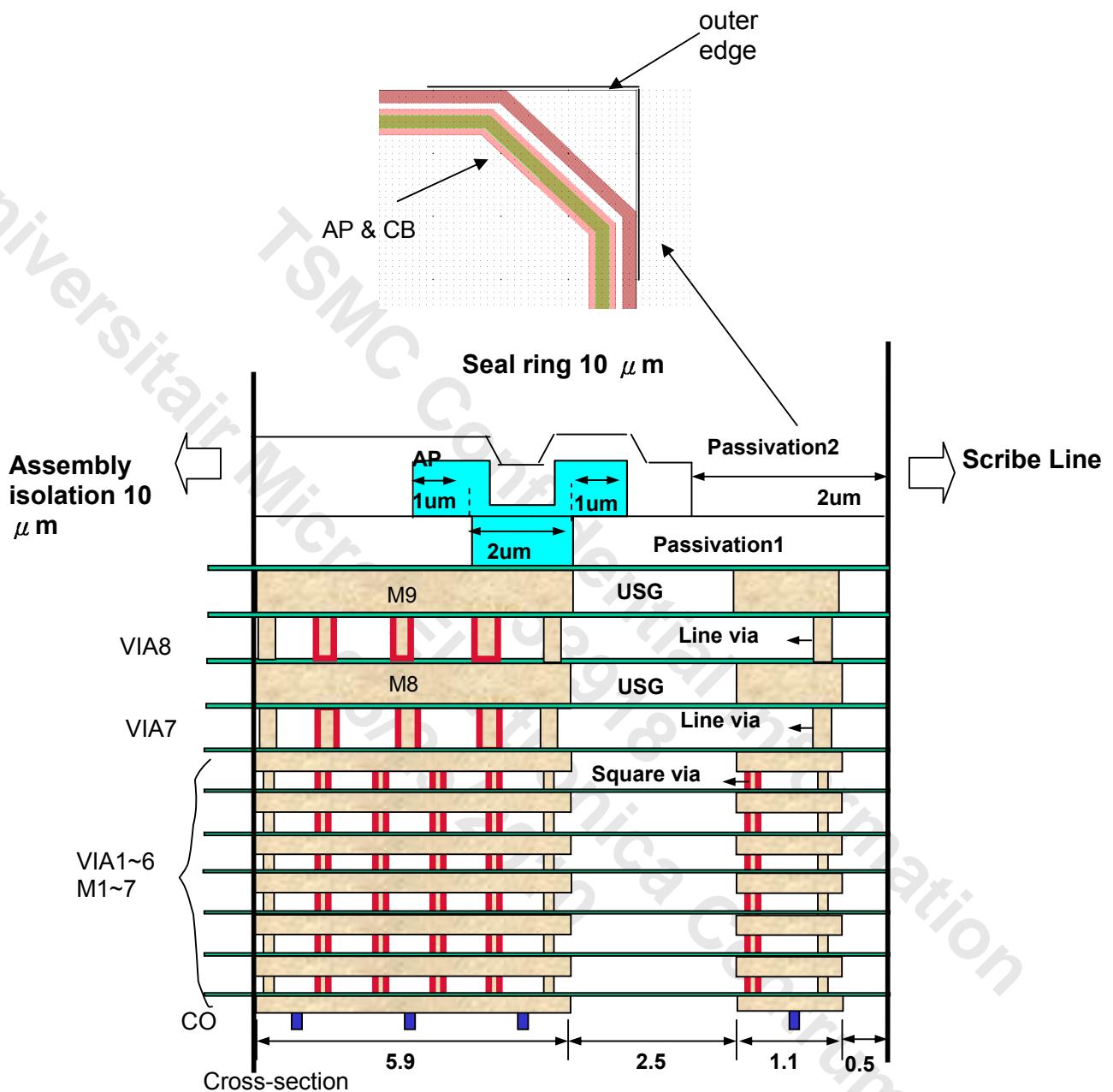
Rule No.	Description	Rule
SR.S.1	<p>Width of Assembly isolation. Only M1~Mtop and CDU allowed in assembly isolation region. [For non-WLCSP seal ring] (1) Connect circuit to seal ring through M1~Mtop if needed. (2) Connect circuit to seal ring through AP is not allowed.</p> <p>[For WLCSP seal ring] (1) Connect circuit to seal ring through M1~Mtop if needed. (2) For connecting circuit to seal ring through AP, it is only allowed connecting to the most inner seal ring (AP overlaps with CB2 is not allowed).</p>	$\geq$ 10
SR.S.1.1	It is not allowed to use AP-MD to connect circuit and seal ring for Flip Chip to avoid the encroachment of AP-MD by UBM etch process. (Except WLCSP sealing region)	
SR.R.1	SEALRING layer is a must if either you add sealring by themselves or metal fuse is used.	
SR.EN.1	(OD interact seal ring) enclosure of metal with the outer edge of seal ring.	$\geq$ 0.5
CO.W.2	Width of CO bar. CO bar is only allowed in seal ring.	= 0.12
VIAx.W.2	<p>Width of VIAx bar. VIAx bar is only allowed in seal ring and fuse protection ring. SEALRING layer (CAD layer: 162 for both seal-ring and fuse protection ring) is a must to cover VIAx bar if VIAx bar is used. For the seal ring layout, please refer to the Figure a of next page or GDS example. For the layout of fuse protection ring, please refer to the N90 fuse rule (T-N90-LO-DR-003).</p>	= 0.13
VIAN.W.2	Width of VIAx bar. VIAx bar is only allowed in seal ring and fuse protection ring.	= 0.28
VIAy.W.2	Width of VIAx bar. VIAx bar is only allowed in seal ring and fuse protection ring.	= 0.13

## Cross-sectional view of seal ring

From CO to Passivation

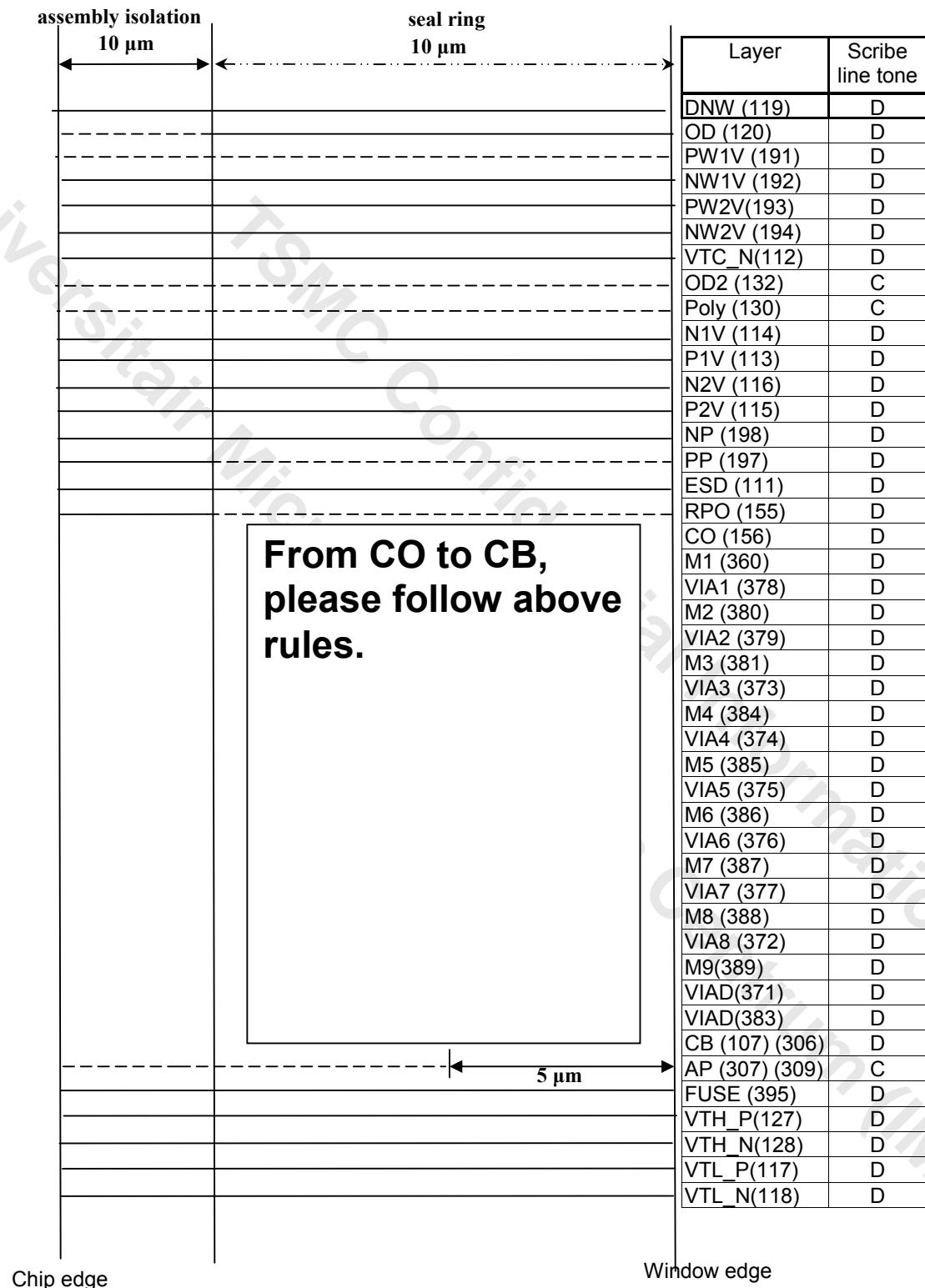


## Cross-sectional view of WLCSP seal ring From CO to Passivation



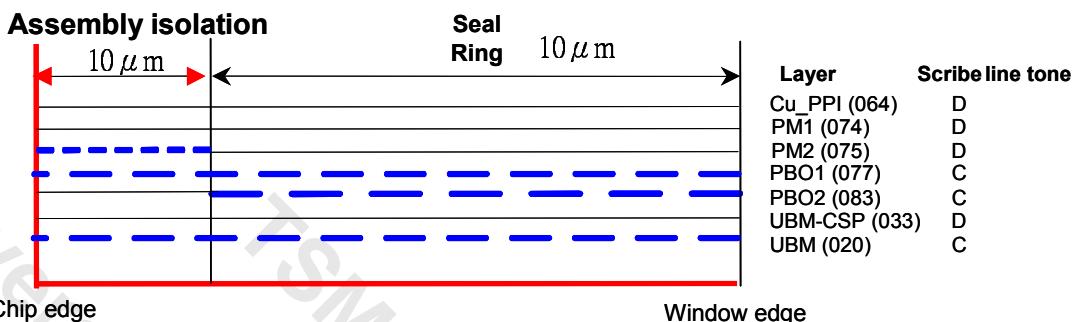
## For other layers

--- : Digitized area is clear on      --- : Digitized area is dark on



## For WLCSP layers

— : Digitized area is clear on mask. — : Digitized area is dark on mask.



Remark: Please refer the layout of PM1 to draw PM1.

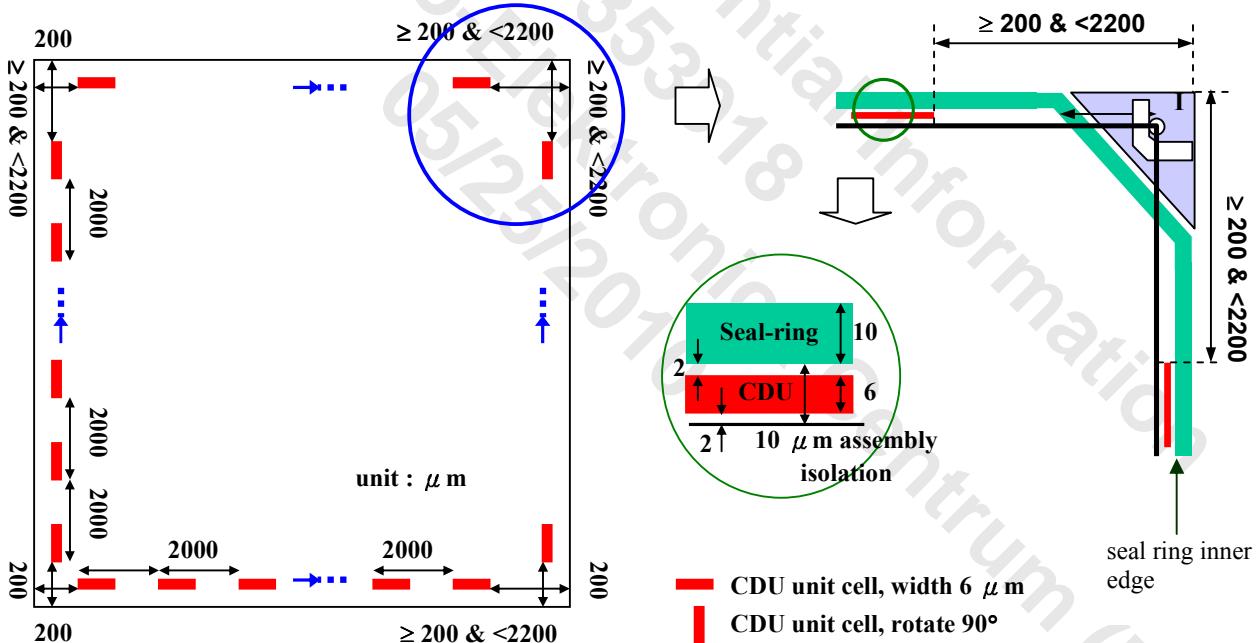
## 4.5.37 CDU (Critical Dimension Uniformity) Rules

- CD uniformity:** It is suggested that you add a CDU pattern in a 10 µm assembly isolation beside a seal ring. The CDU must include OD/Poly/CO/M1 with isolated/dense pitches for different proximity monitoring. If you request that TSMC add a chip corner stress relief pattern and seal ring, TSMC will add CDU.
- Customer-added CDU:** If you add the stress relief pattern, seal ring, and CDU by yourself, you need to know the following:
  - GDS example: **same as seal-ring GDS**
  - You need a dummy layer CDUDMY (CAD layer:165) to align to the CDU cell edge.
  - The DRC will only check the CDU rules in the 2 following rules.

Rule No.	Description
CDU.R.1	CDUDMY must be inside the assembly isolation, beside the seal ring.
CDU.R.2	OD/Poly/CO/M1 must be inside the CDUDMY.

- CDU Clearance:** The assembly isolation must be equal to, or greater than, 10 µm. If the assembly isolation is less than 10 µm, the space is not enough for CDU.

**Example:** A CDU cell that is 6 µm wide is placed in a chip from the left to the right and from the bottom to the top. This occurs every 2000 µm. The space from the left-bottom edge to the short edge of the first CDU cell is 200 µm. The space from the short edge of the last CDU cell to the top-right edge is greater than, or equal to 200 µm and less than 2200 µm. The space from the CDU long edge to the seal ring inner edge is 2 µm.



## 4.5.38 Antenna Effect Prevention (A) Layout Rules

A protection OD means diode, STRAP, source, drain and so on.

Rule No.	Description		Ratio	
	<b>Prevention without protection OD (A.R.1~6, A.R.10~11)</b>		In OD2 (GATE AND OD2)	Not in OD2 (GATE NOT OD2)
A.R.1	Drawn ratio of the poly top area to the active poly gate area that is connected directly to it	≤	250	250
A.R.2	Drawn ratio of the poly sidewall area to the active poly gate area that is connected directly to it	≤	500	500
A.R.3	Drawn ratio of the poly contact area to the active poly gate area that is connected directly to it	≤	10	10
A.R.4	Single-layer drawn ratio of a via area to the active poly gate area that is connected directly to it	≤	20	20
A.R.6	Ratio of cumulative metal top area (from M1 to M9) to an active poly gate area	≤	1000(1.8V IO) 5000(except 1.8V IO)	5000
A.R.10	Drawn ratio of RV area to the active poly gate area that is connected directly to it	≤	20	200
A.R.11	Drawn ratio of AP-MD sidewall area to the active poly gate area that is connected directly to it	≤	1000	2000
	<b>Prevention with protection OD (A.R.7~8, A.R.12~13)</b>			
A. R.7	Drawn ratio of cumulative via area (from Via1 to Via8) to the active poly gate area, with a protection OD	≤	OD area x 210 + 900, for cumulative layers	
A.R.8	Drawn ratio of the cumulative metal top area (from M1 to Last Metal-1) to the active poly gate area, with a protection OD	≤	OD area x 456 + 43000 , for cumulative layers	
		≤	OD area x 8000 + 50000 for last metal alone	
A.R.12	Drawn ratio of RV area to the active poly gate area with a protection OD	≤	OD area x 83 + 400	
A.R.13	Drawn ratio of AP-MD sidewall area to the active poly gate area with a protection OD	≤	OD area x 8000 + 30000	

### Table Notes:

- It is recommended to have OD connection to the poly gate through metal lines for all devices.
- All N+ OD and P+ OD areas connected to metal or via do contribute to the OD area. (Including source or drain diffusion of MOSFET and Strap areas)
- If a large OD is needed, it is recommended to have one big diffusion area with multiple contacts. Avoid covering the entire diode area with metal.
- Gate poly thickness is 1500 angstrom (Å) for both core and I/O gates.
- For all of the protection ODs in the same net, if the summation of their areas is larger than  $0.06 \mu\text{m}^2$ , they can be treated as effective protection ODs against plasma charging.
- In order to avoid the antenna ratio mismatch between the paired devices, metal lines need to be as symmetry as possible.
- The transistors in mismatch sensitive configurations shall be tied to an active region by M1 to prevent process-induced damage.
- When an error is detected at DRC, antenna ratio can be reduced by the following suggestion; connect the node to a protection OD, connect the gate to the highest metal level as close to the gate as possible, or connect the node to the output of the driver with a lower metal level.
- DRC implementation for calculations of metal to gate area ratio in cumulative antenna rules,
  - “Cumulated Ratio” of A.R.4 and A.R.6 rules is defined as:  
 $\text{Area (Mx(n))/Area(GATE(n))} + \text{Area(Mx-1(n-1))/Area(GATE(n-1))} + \dots + \text{Area(M1(1))/Area(GATE(1))}$ 
    - Where GATE(n) is the total GATE area in a particular net constructed by the incremental connections up to current n<sup>th</sup> stage.
    - Mx(n) is the whole area of metal x (x = 1~ top) in the same net.
  - Definition of the protection OD for antenna rules:  
 Total area of (OD NOT POLY) INTERACT CONTACT on the same net
- Failure Criterion  
 Tailing percentage of 20% changes in gate current in Log-normal distribution (which is expressed with the following equation) is less than 5%.

$$\Delta Ig (\%) \equiv \left| \frac{Ig(n) - Ig(n-1)}{Ig(n-1)} \right| \times 100\%$$

### 4.5.37.1 Poly Antenna Ratio

The definition of the **poly top area antenna ratio** for each layer is:

$$\text{ratio} = (L_p \times L_d + L_{pe} \times W_{pe}) / (W_d \times L_d)$$

The definition of the **poly sidewall area antenna ratio** for each layer is:

$$\text{ratio} = 2 \times [(L_{pe} + W_{pe} + L_p) \times t] / (W_d \times L_d)$$

- L<sub>p</sub>: length of field poly connected to gate
- W<sub>p</sub>: width of field poly connected to gate
- L<sub>pe</sub>: length of field poly extension connected to gate
- W<sub>pe</sub>: width of field poly extension connected to gate
- t: poly thickness
- W<sub>d</sub>: transistor channel width
- L<sub>d</sub>: transistor channel length

### 4.5.37.2 M1-M9 Antenna Ratio

The definition of the M1-M9 antenna ratio for each layer is:

$$\text{ratio} = (W_m \times L_m) / (W_d \times L_d)$$

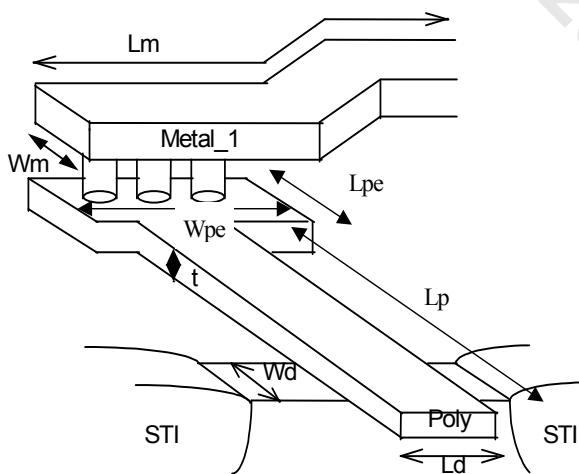
- L<sub>m</sub>: length of metal line connected to gate
- W<sub>m</sub>: width of metal line connected to gate
- W<sub>d</sub>: transistor channel width
- L<sub>d</sub>: transistor channel length

### 4.5.37.3 CO Via1 – Via8 Antenna Ratio

The definition of CO, VIA1-VIA8 antenna ratio is:

$$\text{ratio} = \{\text{total contact (via) area}\} / W_d \times L_d$$

- W<sub>d</sub>: transistor channel width
- L<sub>d</sub>: transistor channel length



#### 4.5.37.4 AP-MD Antenna Ratio

The definition of the AP-MD antenna ratio is:

$$\text{ratio} = 2 \times [(W_m + L_m) \times t_1] / (W_d \times L_d)$$

L<sub>m</sub>: length of metal line connected to gate

W<sub>m</sub>: width of metal line connected to gate

t<sub>1</sub>: thickness of metal line connected to gate

W<sub>d</sub>: transistor channel width

L<sub>d</sub>: transistor channel length

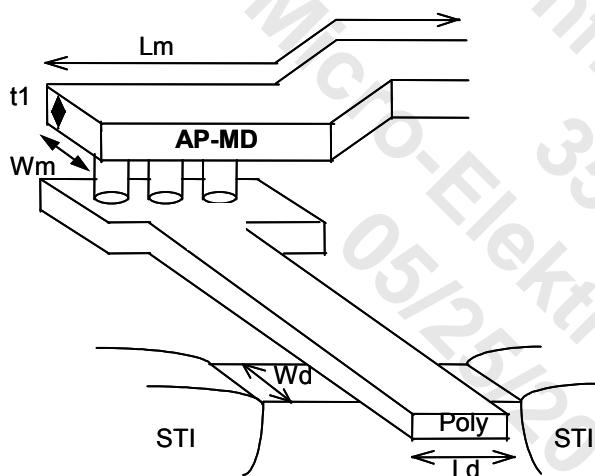
#### 4.5.37.5 RV (Passivation-1 VIA Hole) Antenna Ratio

The definition of RV antenna ratio is:

$$\text{ratio} = \{\text{total RV area}\} / (W_d \times L_d)$$

W<sub>d</sub>: transistor channel width

L<sub>d</sub>: transistor channel length



## 4.6 CMN90 (Mixed Singnal, RF) Layout Rules and Guidelines

### 4.6.1 Capacitor Top Metal (CTM) Layout Rules (Mask ID: 182)

The MiM capacitance is defined by the CTM and CBM area. Individual CTM or CBM (i.e. dummy CTM or CBM) is not allowed. It is important to define the correct CAD layer name for the different capacitor application in the following table.

Special Layer Name	TSMC Default CAD Layer	Description
CTMDMY	148;110	Dummy layer for defined MiM capacitor 1.0fF/um <sup>2</sup> . Its size is equal to the CBM layer size up by 10 µm per side.
CTMDMY	148;115	Dummy layer for defined MiM capacitor 1.5fF/um <sup>2</sup> . Its size is equal to the CBM layer size up by 10 µm per side.
CTMDMY	148;120	Dummy layer for defined MiM capacitor 2.0fF/um <sup>2</sup> . Its size is equal to the CBM layer size up by 10 µm per side
CTMDMY	148	Dummy layer for defined MiM capacitor region. Use for DRC. Its size is equal to the CBM layer size up by 10 µm per side

Rule No.	Description	Label		Rule
CTM.W.1	Width	A	$\geq$	2.0
CTM.W.1®	Recommended width for SPICE simulation accuracy.	A	$\geq$	4.0
CTM.W.2	Maximum length and width For example, 10 µm x 101 µm CTM is not allowed.	A1	$\leq$	100.0
CTM.S.1	Space	B	$\geq$	0.80
CTM.R.4	CTM must be an orthogonal rectangle. L shape and polygon are not allowed.			

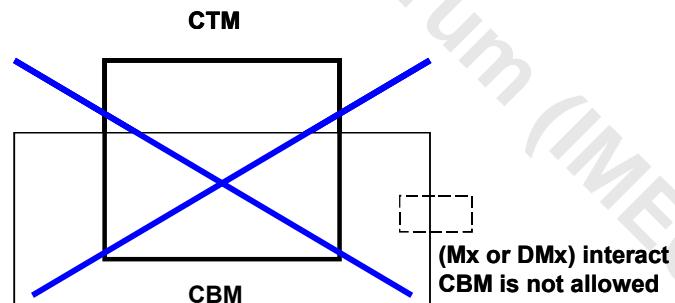
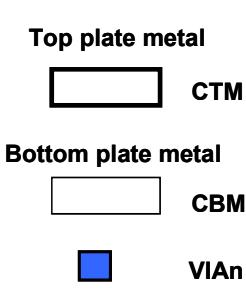
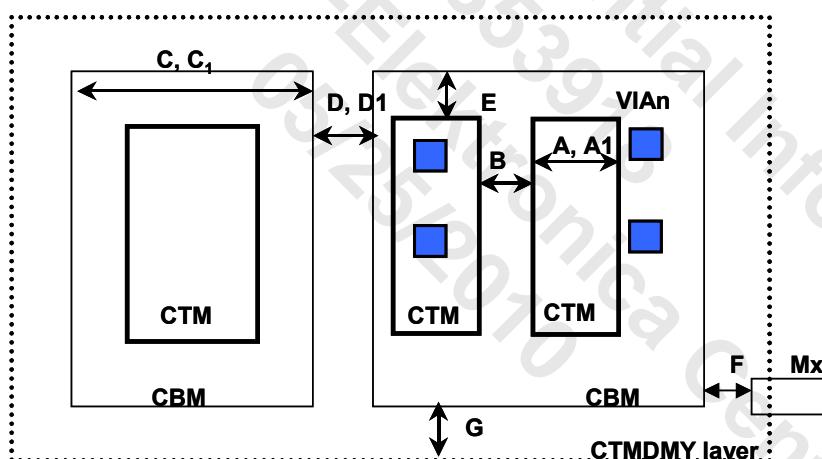
## 4.6.2 Capacitor Bottom Metal (CBM) Layout Rules (Mask ID: 183)

Rule No.	Description	Label		Rule
CBM.W.1	Width	C	$\geq$	2.8
CBM.W.2	Maximum length and width For example, 10 $\mu\text{m}$ x 211 $\mu\text{m}$ CBM is not allowed.	$C_1$	$\leq$	210
CBM.S.1.1	Space of CBM inside a CTMDMY* [area $\leq 40,000 \mu\text{m}^2$ ]	D	$\geq$	2.0
CBM.S.1.2	Space of CBM inside a CTMDMY* [area $> 40,000 \mu\text{m}^2$ ]	D1	$\geq$	2.6
CBM.S.2	Space to top Mx	F	$\geq$	0.5
CBM.EN.1	Enclosure of CTM (CTM must be fully inside CBM. CTM cut a CBM is not allowed).	E	$\geq$	0.4
CBM.EN.2	CTMDMY* is equal to CBM layer sizing up 10 $\mu\text{m}$ for each side. DRC checking layer (CTMDMY, GDS layer 148) is needed to specify the MiM capacitor region; special Mn and Vn design rules will be defined inside this area.	G	=	10.0
CBM.R.2	The CBM interacts with the (Mx or DMx) of the last Mx layer below CBM is not allowed. For example, (M4 or DM4) can not interact with CBM if the MiM is placed between M4 & M5.			
Mx.DN.5	It is not allowed to have local density $< 15\%$ of all 3 consecutive metal (Mx, Mx+1 and Mx+2) under ((CBM SIZING 25) SIZING -25) whose size is $\geq 200\text{um} \times 200\text{um}$			
Mx.R.3g <sup>U</sup>	It's recommended to use 1) PDK cell with metal shielding option, 2) Don't put a lot of MIM together, 3) To design small MIM region to meet Mx.DN.1 and Mx.DN.4®.			

Note: When an array type MiM capacitor is designed, it is strongly recommended to use a common CBM plate.

\*: DRC will auto size up CBM by 10 $\mu\text{m}$  to check the CTMDMY associated rules.

### CTM and CBM



## 4.6.3 Recommendations for the circuit under MIM

This section lists the design recommendations for the circuit under MIM.

- The MIM spice model include RF and BB (baseband) model. The user guidelines of the model are listed at table 4.6.3.1 and table 4.6.3.2:
- The model has two types:
  - Three terminal model (3T): the terminals are CTM, CBM and ground. Two kinds of MIM scheme are supported:
    - RF and BB model for MIM with metal shielding layers.
    - RF and BB model for MIM without metal shielding layers.
  - Two terminal model (2T): the terminals are only CTM and CBM.
- For the model accuracy consideration, the model type of MIM device is defined by the start and end layers. Between the start and end layer regions, user cannot put any metal routing or dummy metal. It is a must to draw the dummy blocking layer, DMxEXCL, in the MIM device. Please refer to Table 4.6.3.2. The size of DMxEXCL is equal to the size of CBM region.

**Table 4.6.3.1 MIM DUT model type**

Model type <sup>a</sup>			Spice name <sup>b</sup>		Start layer <sup>c</sup>	End layer <sup>d</sup>
3T <sup>e</sup>	w/i shield <sup>f</sup>	RF <sup>g</sup>	Type-a <sup>g</sup>	mimcap_um_sin_rf <sup>g</sup>	Mtop-4 <sup>g</sup>	Mn or UTM <sup>g</sup>
		BB <sup>g</sup>	Type-b <sup>g</sup>	NA <sup>g</sup>	Mtop-4 <sup>g</sup>	CTM <sup>g</sup>
	w/o shield <sup>f</sup>	RF <sup>g</sup>	Type-c <sup>g</sup>	mimcap_woum_sin_rf <sup>g</sup>	Substrate <sup>g</sup>	Mn or UTM <sup>g</sup>
		BB <sup>g</sup>	Type-d <sup>g</sup>	mimcap_sin_3t <sup>g</sup>	Substrate <sup>g</sup>	CTM <sup>g</sup>
2T <sup>e</sup>			Type-e <sup>g</sup>	mimcap_sin <sup>g</sup>	CBM <sup>g</sup>	CTM <sup>g</sup>

Table 4.6.3.2 Dummy blocking layer, DMxEXCL, range for different MIM type

Layer	DMxEXCL layer	Type-a	Type-b	Type-c	Type-d	Type-e
		RF-3T-w/i-shield	BB-3T-w/i-shield	RF-3T-w/o-shield	BB-3T-w/o-shield	BB-2T
M9	(150;9)	v		v		
M8	(150;8)	v		v		
M7	(150;7)	v	v	v	v	
M6	(150;6)	v	v	v	v	
M5	(150;5)	v	v	v	v	
M4	(150;4)			v	v	
M3	(150;3)			v	v	
M2	(150;2)			v	v	
M1	(150;1)			v	v	
Poly	(150;21)			v	v	
OD	(150;20)			v	v	

Note: 1.“v” marks mean it must have this dummy DMxEXCL layer.

2. MIM is placed between M7 and M8 as an example.

In the five MIM model types:

Type-a. In the RF 3T with shield MIM type, the model construct from shield metal layer (Mtop-4) and end at Mn or UTM layer (1P9M). Under the shield metal layer, it allows metal routing and devices pass through the MIM region.

Type-b. In the BB 3T with shield MIM type, the model construct from shield metal layer (Mtop-4) and end at CTM layer. Under the shield metal layer, it allows metal routing and devices pass through the MIM region. Above the CTM and shield metal layers, the metal routing can be used.

Type-c. In the RF 3T without shield MIM type, the model construct from substrate and end at Mn or UTM layer (1P9M). Between the start and end layer region, it is not allowed to put any metal routing or dummy metal. If you want to add dummy metal layers, it can select other 4 MIM model types, or use smaller size of MIM devices.

Type-d. In the BB 3T without shield MIM type, the model construct from substrate and end at CTM layer. Between the start and end layer region, it is not allowed to put any metal routing or dummy metal. Above the CTM layer, the metal routing can be used.

Type-e. In the 2T MIM type, the model construct from CBM and end at CTM layer. Under the CBM layer, it allows metal routing and devices pass through the MIM region. Above the CTM layer, the metal routing can be used.

## 4.6.4 VIA<sub>n</sub> Layout Rule for MIM Capacitor and UTM

In this section, VIA<sub>n</sub> layer is the top VIA (size=0.36um) above CTM or CBM capacitors. Except to follow the VIA<sub>n</sub> rules in the section 4.5, you also need to meet the following specific rules are related to the MIM or UTM connection.

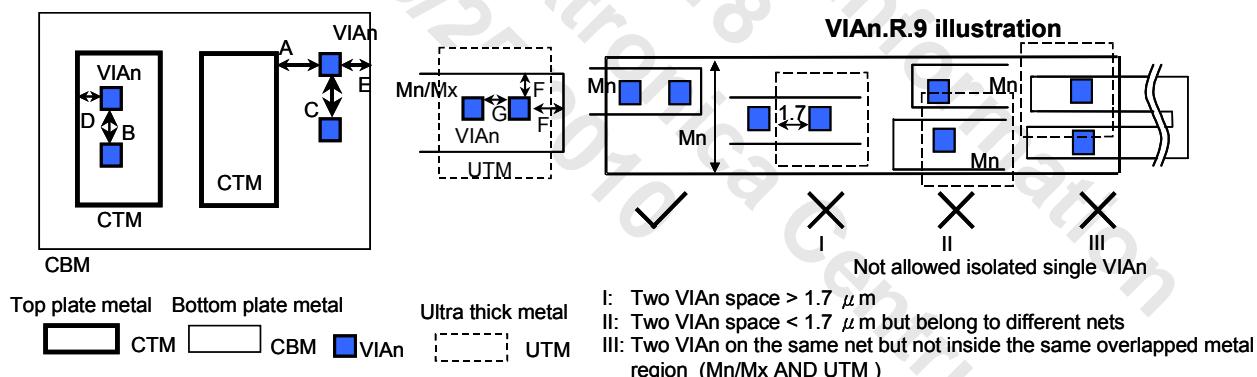
### 4.6.4.1 VIA<sub>n</sub> Layout Rule for CTM/CBM

Rule No.	Description	Label		Rule
VIA <sub>n</sub> .S.3	[VIA <sub>n</sub> inside CBM but outside CTM] space to CTM	A	$\geq$	0.30
VIA <sub>n</sub> .S.4	Space of VIA <sub>n</sub> inside CTM.	B	$\geq$	0.54
VIA <sub>n</sub> .S.5	Space of VIA <sub>n</sub> inside CBM	C	$\geq$	0.54
VIA <sub>n</sub> .EN.3	Enclosure by CTM (cut is not allowed)	D	$\geq$	0.24
VIA <sub>n</sub> .R.7	At least two VIA <sub>n</sub> are required to connected to either a CTM or a CBM. Single VIA <sub>n</sub> in a CTM or in a [CBM NOT CTM] or connect to (the top M <sub>x</sub> layer inside CTMDMY*) is not allowed.			
Guideline	Description			
VIA <sub>n</sub> .R.8g <sup>U</sup>	For MIM applications, put as many VIA <sub>n</sub> as possible for both CTM and CBM connections.			

\*: DRC will auto size up CBM by 10μm to check the CTMDMY associated rules.

### 4.6.4.2 VIA<sub>n</sub> Layout Rule for UTM

Rule No.	Description	Label		Rule
VIA <sub>n</sub> .EN.5	[VIA <sub>n</sub> inside UTM] enclosure by [M <sub>n</sub> or M <sub>x</sub> ]	F	$\geq$	0.08
VIA <sub>n</sub> .R.9	At least two [VIA <sub>n</sub> under UTM], with space (G) $\leq$ 1.7 μm, are required to connect [M <sub>x</sub> or M <sub>n</sub> ] and UTM. One via for UTM or connect to (the top M <sub>x</sub> layer inside CTMDMY) is not allowed.	G	$\leq$	1.7



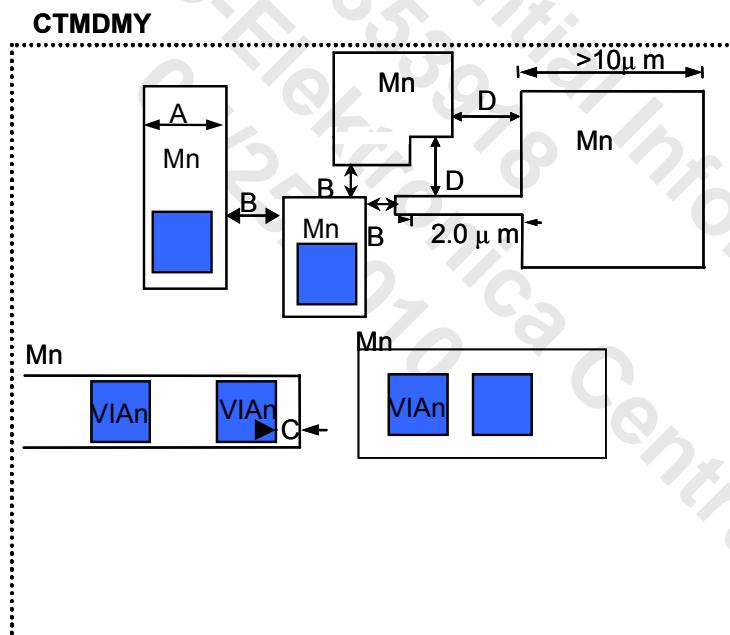
## 4.6.5 Mn Layout Rule for MIM Capacitor

Mn layer means the first metal layer above the MIM capacitor and connect to CTM or CBM. Except to follow the Mn (3XTM) rules in the section 4.5, you also need to meet the following specific rules which are related to the MIM.

Rule No.	Description	Label	Rule
Mn.W.4	Width of Mn [1st metal above MIM capacitor connect to CTM or CBM] inside CTMDMY*.	A	$\geq$ 0.84
Mn.S.4	Space of Mn [1st metal above MIM capacitor connect to CTM or CBM] inside CTMDMY*.	B	$\geq$ 0.84
Mn.S.5	Inside the CTMDMY* region, Mn space to wide Mn (both Mn line width and length > 10 $\mu m$ ), or wide Mn branch (a small piece of Mn is connected to wide Mn within 2.0 $\mu m$ range from the wide Mn).	D	$\geq$ 1.2
Mn.EN.3	Mn [1st metal above MIM capacitor connect to CTM or CBM] enclosure of [VIAn inside CTMDMY] inside CTMDMY*.	C	$\geq$ 0.1
Mn.DN.5	Mn [1st metal above MIM capacitor connect to CTM or CBM] density range inside a CTMDMY* [the overlapped area of {checking window AND CTMDMY} $\geq$ 2500 $\mu m^2$ ] Note: TSMC PDK cells have taken this rule into layout consideration. If you do not use TSMC PDK cells, please pay attention on the Mn layout while you design the MM_RF device.		$\geq$ 50% by 200x200 $\leq$ 80% by 100x100

\*: DRC will auto size up CBM by 10 $\mu m$  to check the CTMDMY associated rules.

### Rules for Mn and VIAn inside a CTMDMY



## 4.6.6 Antenna Effect Prevention Design Rules for MIM Capacitor

### 4.6.6.1 MIM structures With the Antenna effect:

The antenna effect should be taken into consideration for your MIM capacitor design. The layout style of the MIM capacitor routing will impact its immunity to the antenna effect during fab process. Antenna rules are defined separately for the following metallization options:

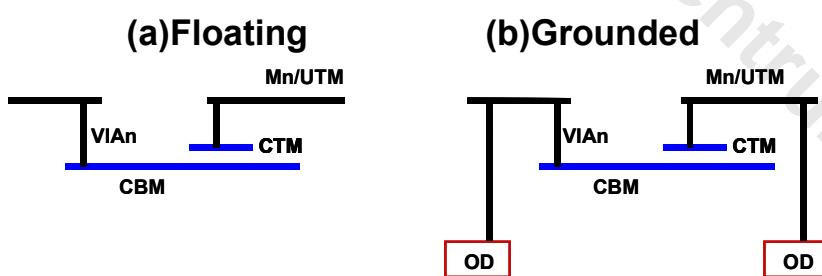
**Table 4.6.6.1 Metallization Options for Metal Layers above MIM**

Metallization Options	Metal Layers above MIM				
	1 <sup>st</sup> Mn	2 <sup>nd</sup> Mn	UTM	Cu-MD	AP-MD
A	V				
B			V		
C	V	V			
D	V		V		
E	V			V	
F	V				V
G			V		V
H	V	V			V
I	V		V		V

Note: In this table, Cu-MD is the Cu RDL and AP-MD is the AP-RDL.

#### 4.6.6.1.1 Terminology

- “**Floating**” defines as below:  
CTM or CBM node is not connected to any OD or poly gate region.
- “**Grounded**” defines as below:  
CTM or CBM node is connected to OD region.
- “**Balanced structures**” defines as below:  
Both CTM and CBM nodes are floating or connected to ground (including protection diode) through the same metal path (i.e. Mn, UTM or AP-MD) after MIM structure is formed. Please refer to Fig 4.6.6.1.1.



**Fig.4.6.6.1.1 Examples of balanced structures**

- “Unbalanced structures” defines as below:

- If only one node of the MIM capacitor is connected to OD, but the other node is not connected to OD at the same metal layer. Please refer to Fig 4.6.6.1.2.
- If one node of the MIM capacitor is connected to GATE. Please refer to Fig 4.6.6.1.2.

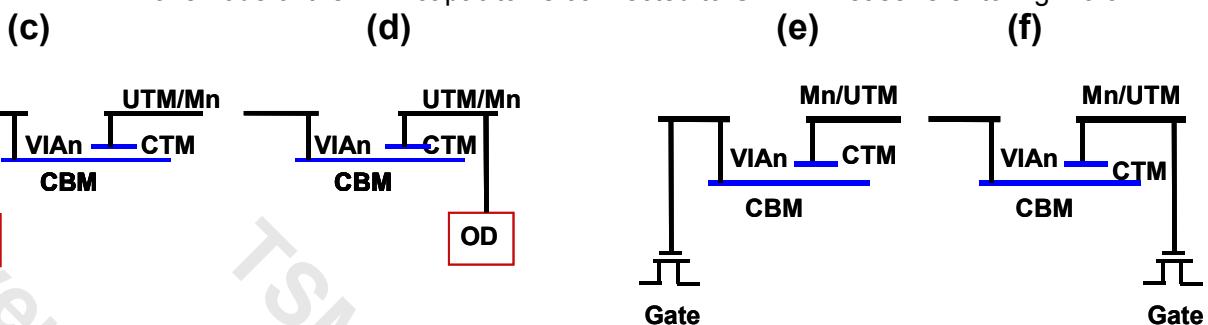


Fig. 4.6.6.1.2 Examples of unbalanced structures

#### 4.6.6.1.2 MIM Structure Recognition Methodology

Below tables are for clear definition of balanced & unbalanced MIM structure.

A, B: Two terminals of MIM

All structure = balanced (float) + balanced (OD) + unbalanced

Unbalanced (A-OD): Unbalanced structure. Terminal A connected to OD and terminal B not connected to OD.

Unbalanced (B-OD): Unbalanced structure. Terminal B connected to OD and terminal A not connected to OD.

Table 4.6.6.1.2.1 One metal layer above MIM

1st A, B	Structure
Both A, B floating	Balanced (float)
Both A, B connect to OD	Balanced (OD)
Others	Unbalanced

Table 4.6.6.1.2.2 Two metal layers above MIM (2<sup>nd</sup> metal is Mn/UTM)

1st A, B	2nd A, B	Structure
Balanced (float)	Balanced (float)	Balanced
Balanced (float)	Balanced (OD)	Balanced
Balanced (OD)	All structures	Balanced
Other combinations		Unbalanced

Table 4.6.6.1.2.3 Two metal layers above MIM (2<sup>nd</sup> metal is AP-MD)

1st A, B	2nd A, B	Structure
Balanced (float)	Balanced (float)	Balanced
All structures	Balanced (OD)	Balanced
Balanced (OD)	All structures	Balanced
Other combinations		Unbalanced

Table 4.6.6.1.2.4 Three metal layers above MIM (3<sup>rd</sup> metal is AP-MD)

1st A, B	2nd A, B	3rd A, B	Structure
Balanced (float)	Balanced (float)	Balanced (float)	Balanced
Balanced (OD)	All structures	All structures	Balanced
All structures	Balanced (OD)	All structures	Balanced
All structures	All structures	Balanced (OD)	Balanced
Unbalanced (A-OD)	Unbalanced (B-OD)	All structures	Balanced
Unbalanced (A-OD)	All structures	Unbalanced (B-OD)	Balanced
All structures	Unbalanced (A-OD)	Unbalanced (B-OD)	Balanced
Other combinations			Unbalanced

#### 4.6.6.1.3 Check Methods:

- If there is only one Metal (Mn or UTM) above the MIM capacitor:

Refer to Fig. 4.6.6.1.1 and Fig. 4.6.6.1.2 to check MIM structure is balanced or unbalanced.

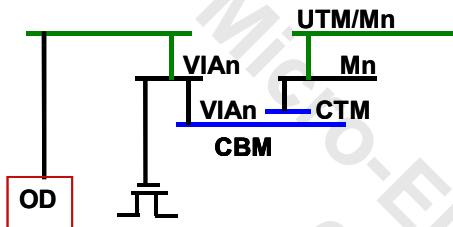
- If there are at least two Metal layers (Table 4.6.6.1 option C~I) above the MIM capacitor:

1. Each metal layers above MIM capacitor must follow the antenna rule. (Please refer to section 4.6.6.2).
2. DRC first check the 1<sup>st</sup> metal layer right above the MIM capacitor. It is the same as only one Metal above the MIM capacitor.
3. Then DRC following check the 2<sup>nd</sup> metal layer above the MIM capacitor:

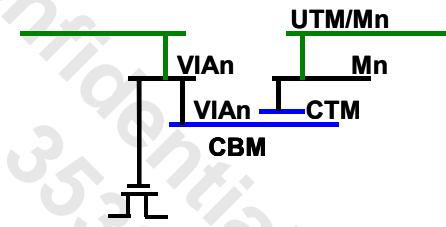
3-1. If the 1<sup>st</sup> metal layer above the MIM capacitor is balanced, it only needs to check the 2<sup>nd</sup> metal scheme.

3-2. If the 1<sup>st</sup> metal layer above the MIM capacitor is unbalanced, it needs to check the all metal schemes above MIM capacitor as below, then to judge whether the 2<sup>nd</sup> metal layer is balanced or unbalanced.

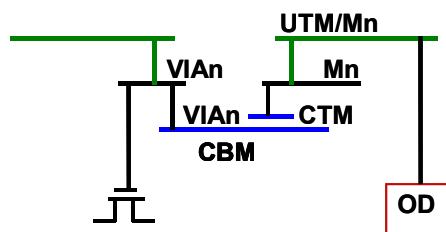
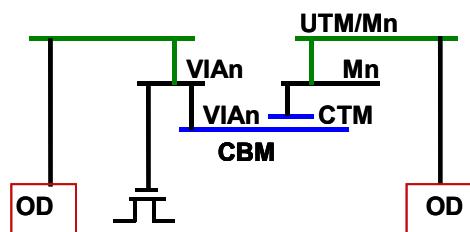
(g)Unbalanced



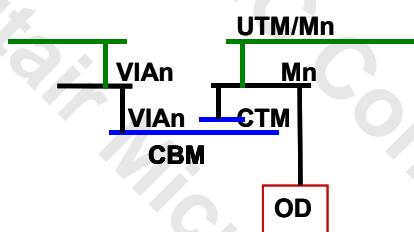
(h)Unbalanced



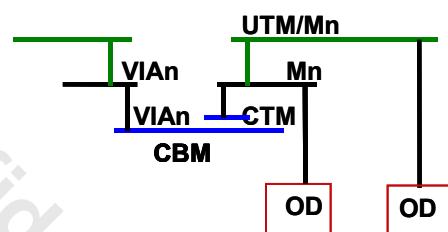
(i)Unbalanced

(j)Unbalanced  
(not allowed in 2.0fF/um2 MIM)

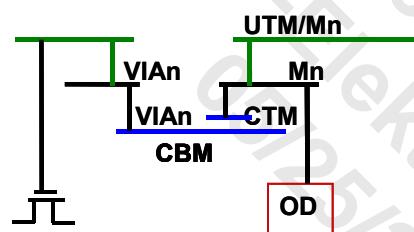
(k)Unbalanced



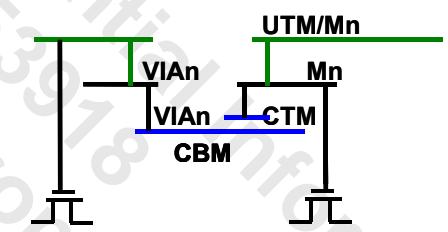
(l)Unbalanced



(m)Unbalanced

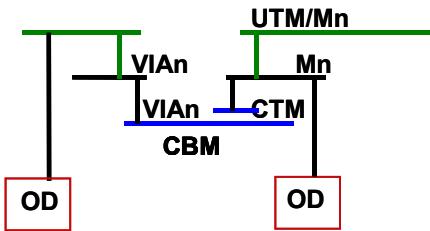


(n)Unbalanced



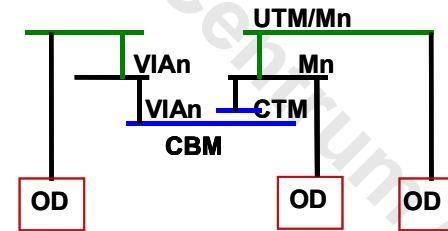
(o)Unbalanced

(not allowed in 2.0fF/um2 MIM)



(p)Unbalanced

(not allowed in 2.0fF/um2 MIM)



## 4.6.6.2 Antenna Effect Prevention Layout Rules

The following antenna rules for the metal and via layers above CTM and CBM can cover all the film schemes in the Table 4.6.6.1.

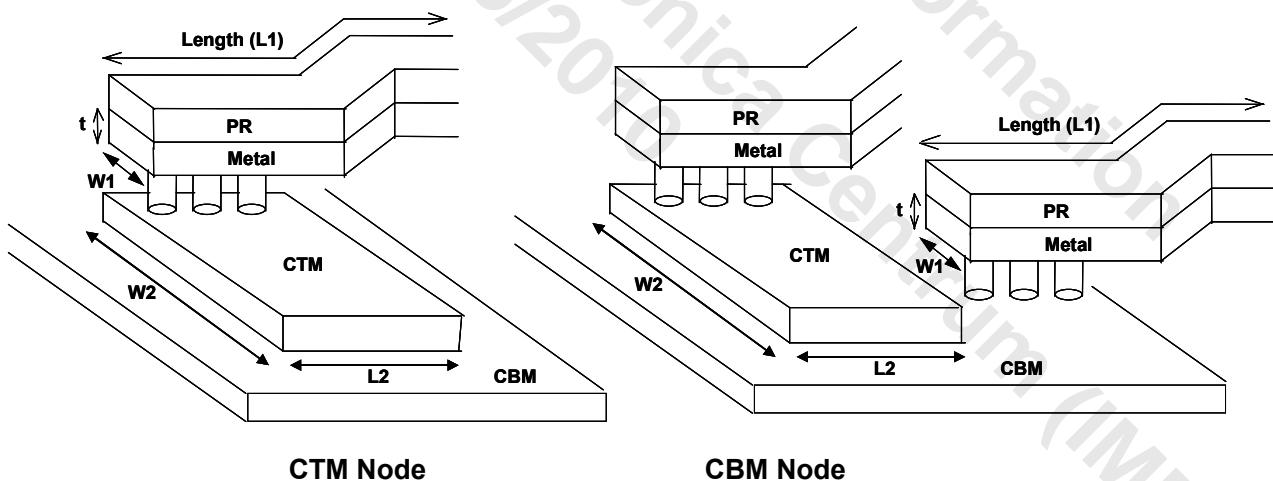
Rule No.	Description	Antenna Ratio	
		CTM Node	CBM Node
A.R.MIM.1	Maximum ratio of the cumulative metal top area and AP-MD sidewall area to the MIM capacitor for <b>balanced structure</b> when both <b>CTM</b> and <b>CBM</b> are floating or grounded.	≤	1000 1000
Both A.R.MIM.2 and A.R.MIM.3 must be followed simultaneously for the following conditions: (1) Both CTM/CBM are connected to gate. (2) One of CTM/CBM connects to gate and the other is floating.			
A.R.MIM.2	Maximum ratio of the cumulative metal top area and AP-MD sidewall area to the MIM capacitor for <b>unbalanced structure</b> where <b>CTM</b> is connected to OD, and <b>CBM</b> is floating or connected to gate.	≤	1000 5
A.R.MIM.3	Maximum ratio of the cumulative metal top area and AP-MD sidewall area to the MIM capacitor for <b>unbalanced structure</b> where <b>CBM</b> is connected to OD, and <b>CTM</b> is floating or connected to gate.	≤	5 1000
Both A.R.MIM.4 and A.R.MIM.5 must be followed simultaneously for the following conditions: (1) Both CTM/CBM are connected to gate. (2) One of CTM/CBM connects to gate and the other is floating.			
A.R.MIM.4	Maximum counts of the cumulative both VIA and RV to the same connection to MIM capacitor for <b>unbalanced structure</b> when <b>CTM</b> is connected to OD and <b>CBM</b> is floating or connected to gate.	≤	NA 50
A.R.MIM.5	Maximum counts of the cumulative both VIA and RV to the same connection to MIM capacitor for <b>unbalanced structure</b> when <b>CBM</b> is connected to OD and <b>CTM</b> is floating or connected to gate.	≤	50 NA
A.R.MIM.8 <sup>U</sup>	It is strong suggested to use a protection OD		
A.R.MIM.9	For 2.0fF/um <sup>2</sup> MIM, the <b>unbalance structure</b> is not allowed.		

Note: You do not need to concern the VIA/VR associated rules for the balanced structures.

### 4.6.6.3 Definition of Antenna Ratio

Different antenna ratio formulas are defined for Cu and AP-MD due to the process differences.

Metal Layer	MIM node	Drawn Ratio Formula	Definition
Cu Antenna (Mn, UTM, MD)	CTM node	$(L1 \times W1) / (W2 \times L2)$	L1: metal length connected to CTM W1: metal width connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	$(L1 \times W1) / (W2 \times L2)$	L1: metal length connected to CBM W1: metal width connected to CBM W2: connected CTM width L2: connected CTM length
VIA Antenna	CTM node	$\{ \text{total VIA area} \} / (W2 \times L2)$	total VIA area connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	$\{ \text{total VIA area} \} / (W2 \times L2)$	total VIA area connected to CBM W2: connected CTM width L2: connected CTM length
AP-MD Antenna	CTM node	$2 [(L1 + W1) \times t] / (W2 \times L2)$	L1: metal length connected to CTM W1: metal width connected to CTM t : metal thickness of AP-MD W2: connected CTM width L2: connected CTM length
	CBM node	$2 [(L1 + W1) \times t] / (W2 \times L2)$	L1: metal length connected to CBM W1: metal width connected to CBM t : metal thickness of AP-MD W2: connected CTM width L2: connected CTM length
RV Antenna	CTM node	$\{ \text{total RV area} \} / (W2 \times L2)$	total RV area connected to CTM W2: connected CTM width L2: connected CTM length
	CBM node	$\{ \text{total RV area} \} / (W2 \times L2)$	total RV area connected to CBM W2: connected CTM width L2: connected CTM length



## 4.6.7 Ultra Thick Metal (UTM) Layout Rules

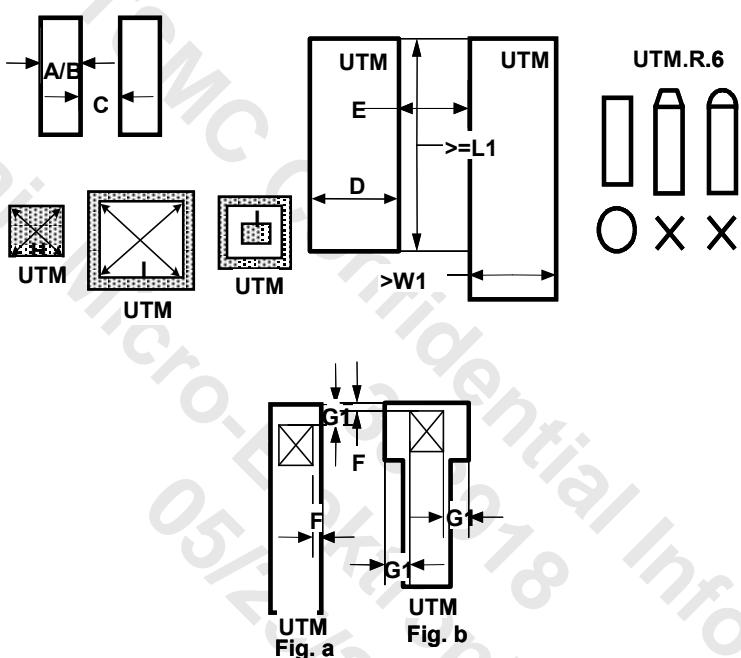
UTM (34KÅ) and Mn (8.5 KÅ) can not co-exist on the same metal layer.

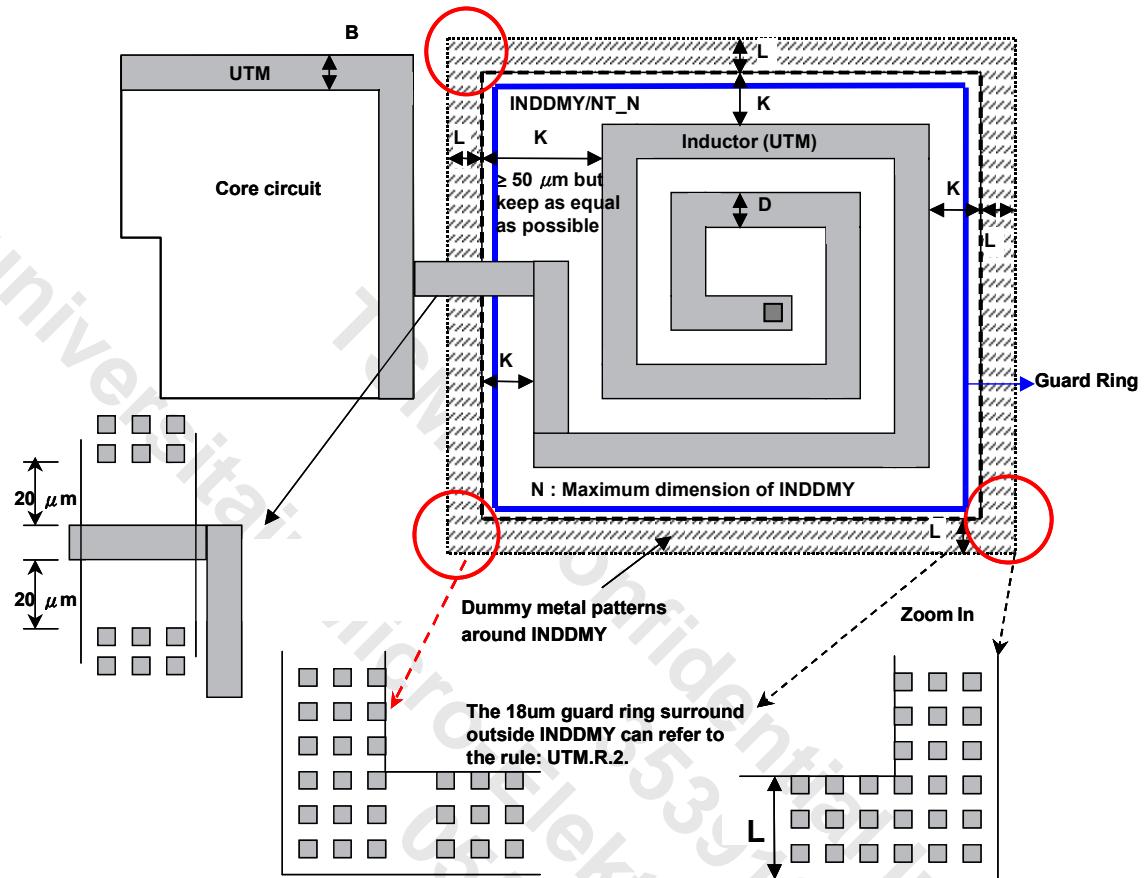
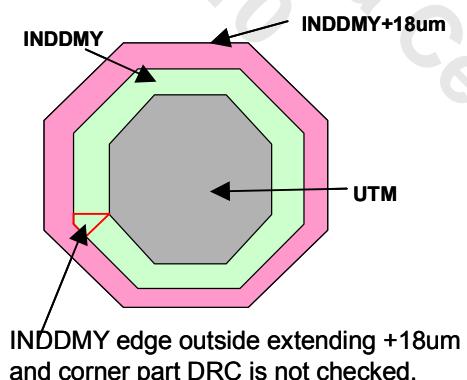
Cu RDL (Cu-MD) above UTM layer is not allowed. However, Al RDL (AP-MD) is allowed.

Rule No.	Description	Label	Rule
UTM.W.1	Width	A	$\geq$ 2.00
UTM.W.2	Maximum width (except bond pad and INDDMY)	B	$\leq$ 12.00
UTM.W.3	Maximum width inside INDDMY.	D	$\leq$ 30
UTM.W.4	Maximum width and length of an INDDMY region (for example: 590x601 µm is not allowed)	N	600.0
UTM.S.1	Space	C	$\geq$ 2.00
UTM.S.2	Space inside INDDMY [at least one UTM width $\geq$ 12µm (w1) and the parallel length $\geq$ 12 µm (L1)]	E	$\geq$ 3.0
UTM.EN.1	Enclosure of VIA <sub>n</sub>	F	$\geq$ 0.30
UTM.EN.2	Enclosure of VIA <sub>n</sub> [at least two opposite sides]	G <sub>1</sub>	$\geq$ 0.40
UTM.EN.3®	Recommended INDDMY enclosure of UTM (inductor) for SPICE simulation accuracy.	K	$\geq$ 50.0
UTM.A.1	Area	H	$\geq$ 9
UTM.A.2	Enclosed area	I	$\geq$ 9
UTM.DN.1	UTM density range over any 100µm x 100µm area (checked by stepping in 50um increments). The following region would be excluded during DRC: ----Bond pad (defined by CB or CBD) ----Chip corner stress relief area and seal ring ----FW/LMARK/LOGO/(INDDMY SIZING 18) This rule is only applied while the width of {checking window NOT excluded region} $\geq$ 25µm		$\geq$ 20% $\leq$ 80%
UTM.DN.2	UTM density over the whole chip (include INDDMY)		$\geq$ 20% $\leq$ 70%
UTM.DN.3	M1, Mx, Mn metal density over the whole chip (include INDDMY)		$\geq$ 20%
UTM.DN.4	UTM [connect to CTM or CBM] density range inside a CTMDMY* [the overlapped area of {checking window AND CTMDMY} $\geq$ 2500µm <sup>2</sup> ]		$\geq$ 50% by 200x200 $\leq$ 80% by 100x100
UTM.DN.5®	Maximum density of INDDMY over the whole chip		$\leq$ 5%
UTM.R.2	At least a region of width (L) $\geq$ 18 um with dummy metal (M1/Mx/Mn/UTM) is required to surround outside the INDDMY. In this region, it's only allowed to have the dummy metal patterns and the related inductor metal routing. The DRC deck will use {(INDDMY edge outside extending +18um) NOT INDDMY} to define this region. This region needs to follow: <ul style="list-style-type: none"><li>o It is not allowed to have metal routing except (a) UTM inductor or (b) the metal underneath Vn connected to UTM inductor inside INDDMY or (c) M1 for guard ring of UTM inductor only.</li><li>o It is not allowed to have VIA<sub>x</sub> or VIA<sub>n</sub> (the layer underneath Mn).</li><li>o It is not allowed to have a 9um*9um open area without any metal or dummy metal except the 20 um extension region next to "inductor pin-out port". ("inductor pin-out port" is define as picture)</li></ul>		
UTM.R.3	Any active device, passive device, interconnect metal line, dummy metal and VIA <sub>x</sub> is not allowed inside an INDDMY region except for the inductor structure itself (include VIA <sub>n</sub> , under layer metal connect to the inductor, IND guard ring inside INDDMY and OD, PO.....layers).		

UTM.R.6 <sup>U</sup>	UTM line-end must be rectangular. Other shapes are not allowed.		
UTM.R.8	At least four VIA <sub>n</sub> are required inside INDDMY to connect the (M <sub>n</sub> or M <sub>x</sub> ) with an inductor. (Put as many VIA <sub>n</sub> as possible for RF applications)		
<b>Guidelines</b>	<b>Description</b>		
UTM.R.1g <sup>U</sup>	Keep placing the INDDMY separately and uniformly cross over a chip		
UTM.R.9g <sup>U</sup>	For inductor devices offered in TSMC's SPICE model, a native substrate layer is created under the inductor coil to minimize eddy currents. This layer is specified by NT_N with the exact shape as the INDDMY layer. This NT_N drawn layer adds no process cost and no extra mask and is included in TSMC's PDK and its associated sample layout document.		

\*: DRC will auto size up CBM by 10µm to check the CTMDMY associated rules.



**Inductor:****Illustration UTM.R.2**

## 4.6.8 Metal Density Rules Summary for MIM/UTM

You have to follow the section 4.5 and chapter 9 to meet the logic metal density rules. The summary of MIM and UTM metal density rules are as the following:

Rule No.	Description	Label	Rule
Mn.DN.5	Mn [1 <sup>st</sup> metal above MIM capacitor connect to CTM or CBM] density range inside a CTMDMY* [the overlapped area of {checking window AND CTMDMY} $\geq 2500\mu\text{m}^2$ ]	$\wedge$	50% by 200x200
		$\vee\!\! \wedge$	80% by 100x100
UTM.DN.1	UTM density range over any 100 $\mu\text{m}$ x 100 $\mu\text{m}$ area (checked by stepping in 50 $\mu\text{m}$ increments). <ul style="list-style-type: none"> <li>The following region would be excluded during DRC.               <ul style="list-style-type: none"> <li>Bond pad (define by CB or CBD)</li> <li>Chip corner stress relief area and seal ring</li> <li>FW/LMARK/LOGO/(INDDMY SIZING 18)</li> </ul> </li> <li>This rule is only applied while the width of (checking window NOT excluded region) <math>\geq 25\mu\text{m}</math></li> </ul>	$\wedge$	20%
UTM.DN.2	UTM metal density over the whole chip (include INDDMY)	$\wedge$	20%
UTM.DN.3	M1,Mx, Mn metal density over the whole chip (include INDDMY)	$\wedge$	20%
UTM.DN.4	UTM [connect to CTM or CBM] density range inside a CTMDMY* [the overlapped area of {checking window AND CTMDMY} $\geq 2500\mu\text{m}^2$ ]	$\wedge$	50% by 200x200
		$\vee\!\! \wedge$	80% by 100x100
UTM.DN.5®	Maximum density of INDDMY over the whole chip	$\leq$	5%

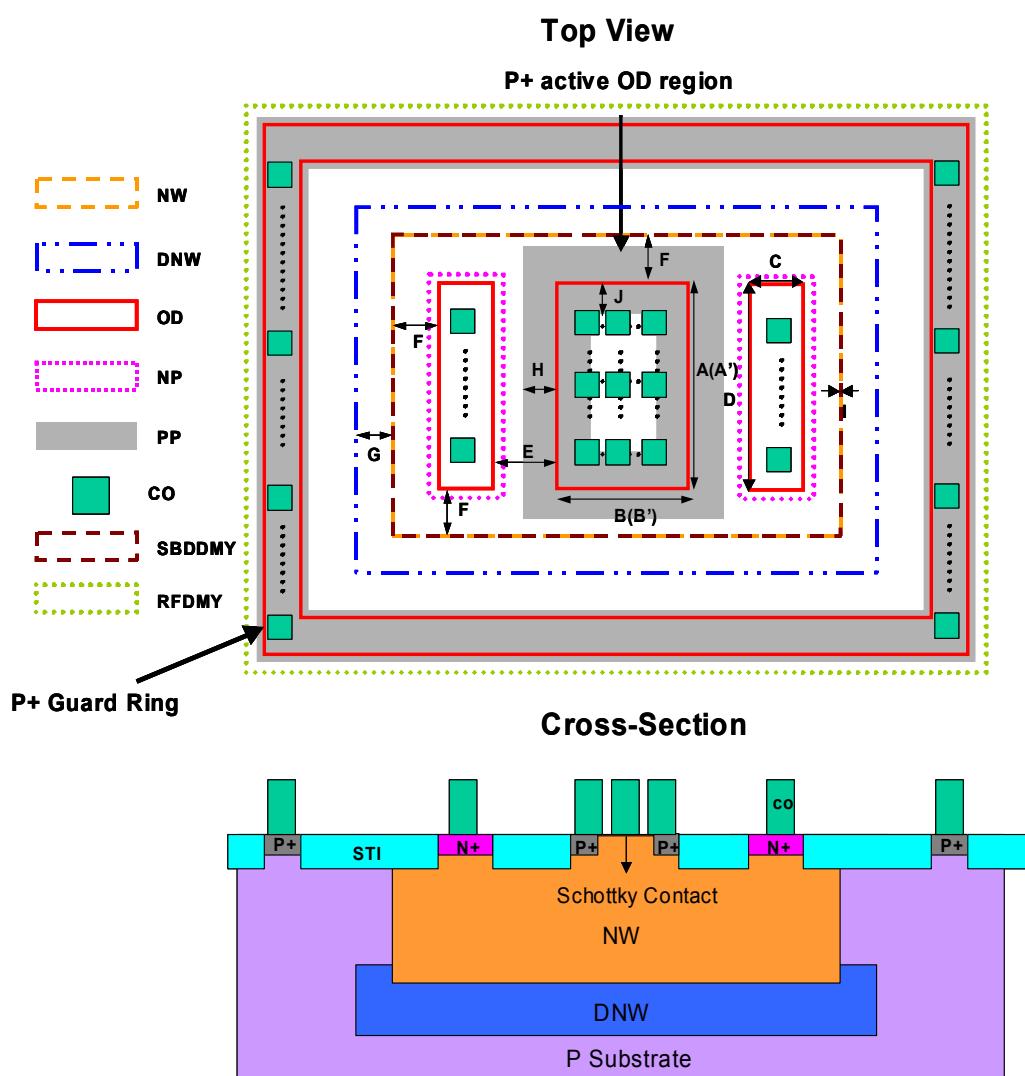
\*: DRC will auto size up CBM by 10 $\mu\text{m}$  to check the CTMDMY associated rules.

## 4.6.9 Schottky Barrier Diode (SBD) Layout Rules

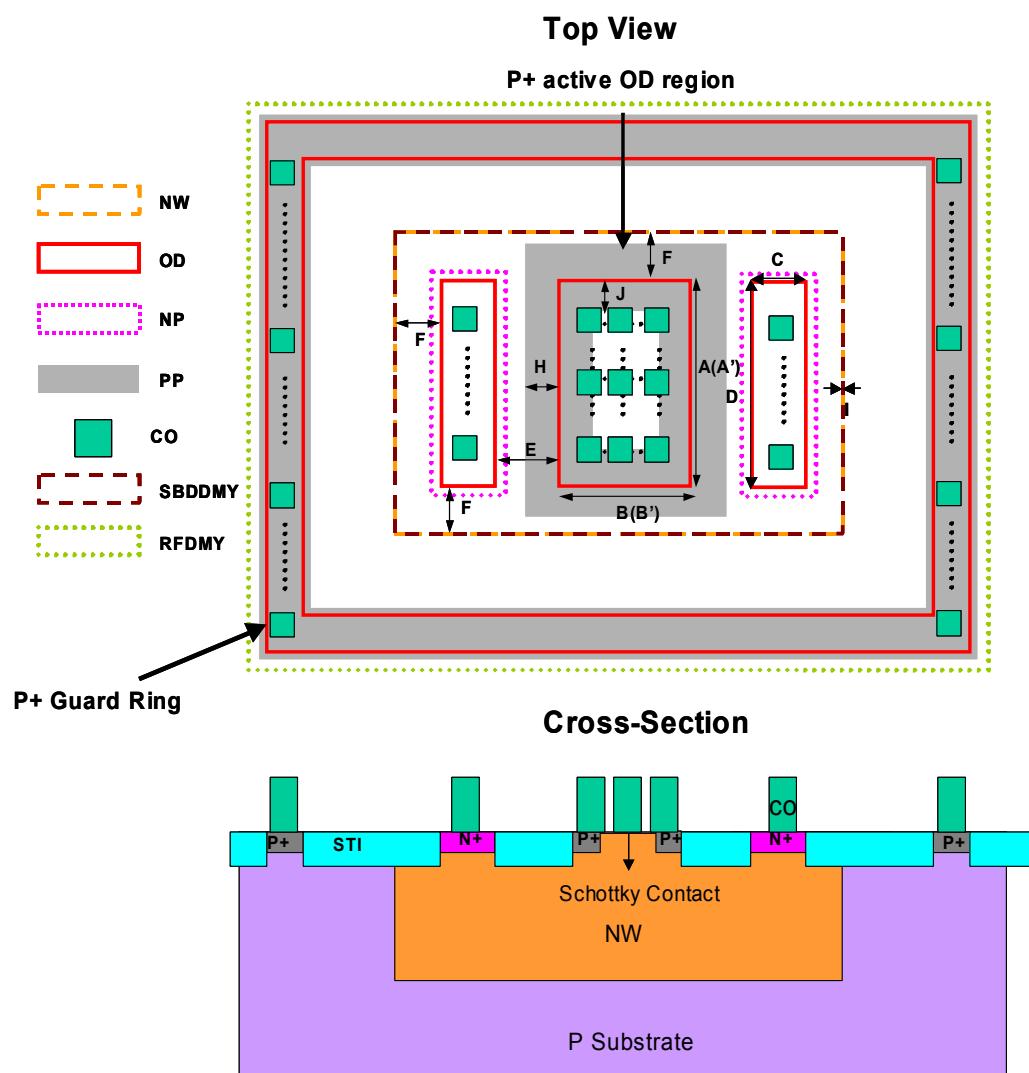
Dummy layer SBDDMY is must in logic operation for 1.2V PLDD mask making.

SBD is only offered for N90LP RF device.

Rule No.	Description	Label		Rule
SBD.W.1	Minimum width of an OD region to define the width of the P+ active OD region of the SBD.	A	$\approx$	1
SBD.W.1.1	Maximum width of an OD region to define the width of the P+ active OD region of the SBD.	A'	$\leq$	16
SBD.W.2	Minimum length of an OD region to define the length of the P+ active OD region of the SBD.	B	$\approx$	0.5
SBD.W.2.1	Maximum length of an OD region to define the length of the P+ active OD region of the SBD.	B'	$\leq$	4
SBD.W.3	Minimum and Maximum length of an OD region to define the length of the NP OD region of the SBD.	C	=	0.2
SBD.W.4	The width of NP OD region of the SBD must be equal to P+ active OD region of the SBD.	D		
SBD.S.1	Space between P+ active OD region and NP OD region of the SBD.	E	=	0.32
SBD.E.1	Minimum and maximum extension from NW edge to an OD region used for the SBD.	F	=	0.700
SBD.E.1.1	Minimum extension of DNW beyond NW for a better noise isolation, as shown in Fig. 4.6.9.1	G	$\approx$	0.6
SBD.E.2	Minimum and maximum extension of a PP region beyond an enclosed P+ active OD region of the SBD.	H	=	0.13
SBD.E.3	Maximum and Minimum extension of "SBDDMY" beyond NW.	I	=	0
SBD.O.1	Minimum and maximum overlap from a PP edge to a P+ active OD region of the SBD.	J	=	0.13
SBD.R.1	The P+ active OD region of the SBD must be located between the NP OD regions. The NP OD region must be located parallel with the width of the P+ active OD region at left and right sides.			
SBD.R.2	Maximum Finger Number (N) of the P+ active OD region of the SBD should be $\leq 16$ , as shown in Fig. 4.6.9.3			
SBD.R.3	Each NW of SBD should be surrounded by the P+ Guard Ring (P+ pickup ring).			
SBD.R.4	Use "RFDMY" to fully cover SBD and P+ Guard Ring for LVS to recognize RF Device.			
SBD.R.5	PP for SBD must be a rectangle ring. PP rectangle ring must surround OD. Other shape is not allowed.			
SBD.R.7® <sup>U</sup>	Recommend: Use CO as many as possible on the SBD connection for spice simulation accuracy.			



**Fig. 4.6.9.1. SBD with DNW (single finger (N=1))**



**Fig. 4.6.9.2. SBD without DNW (single finger (N=1))**

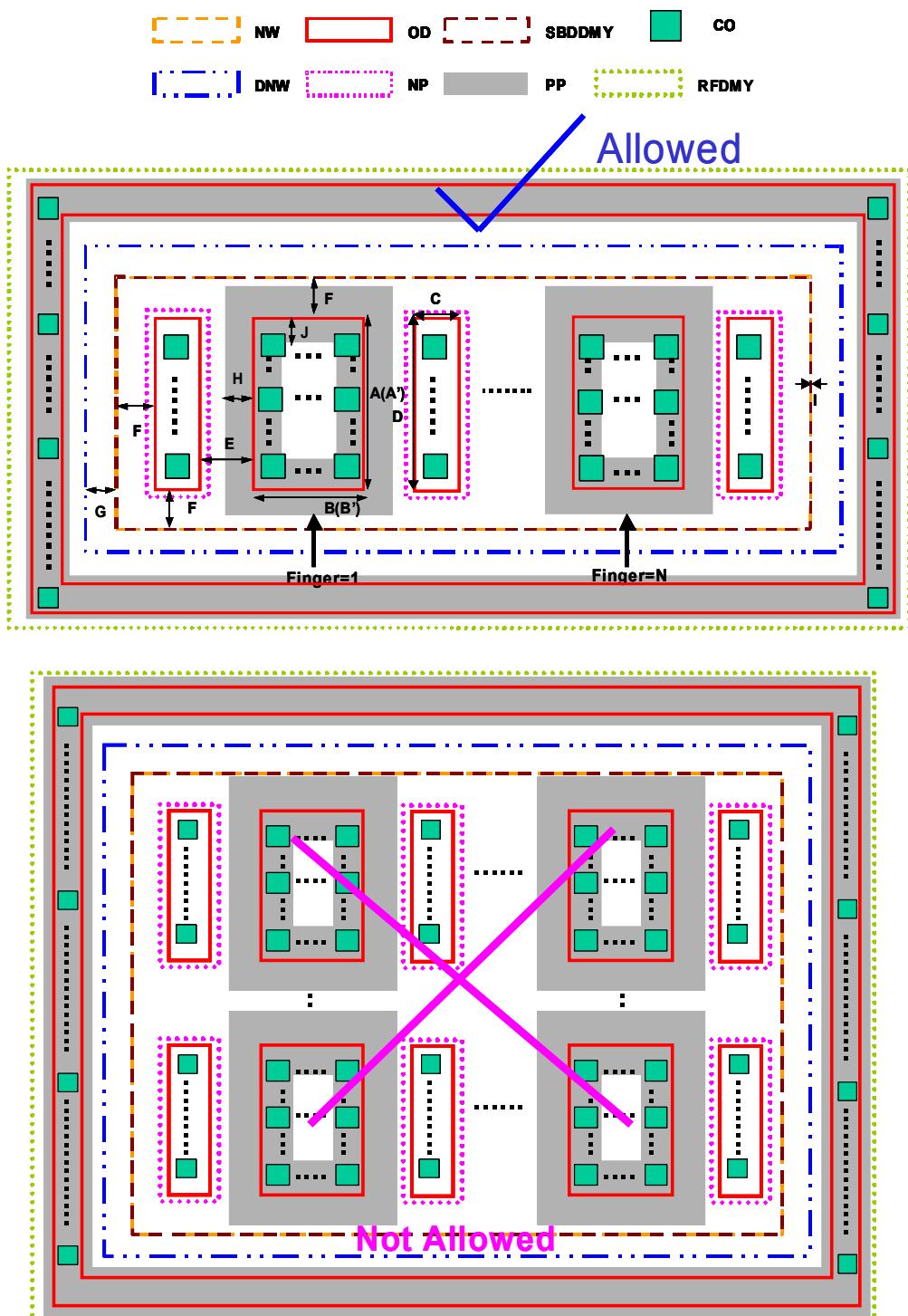
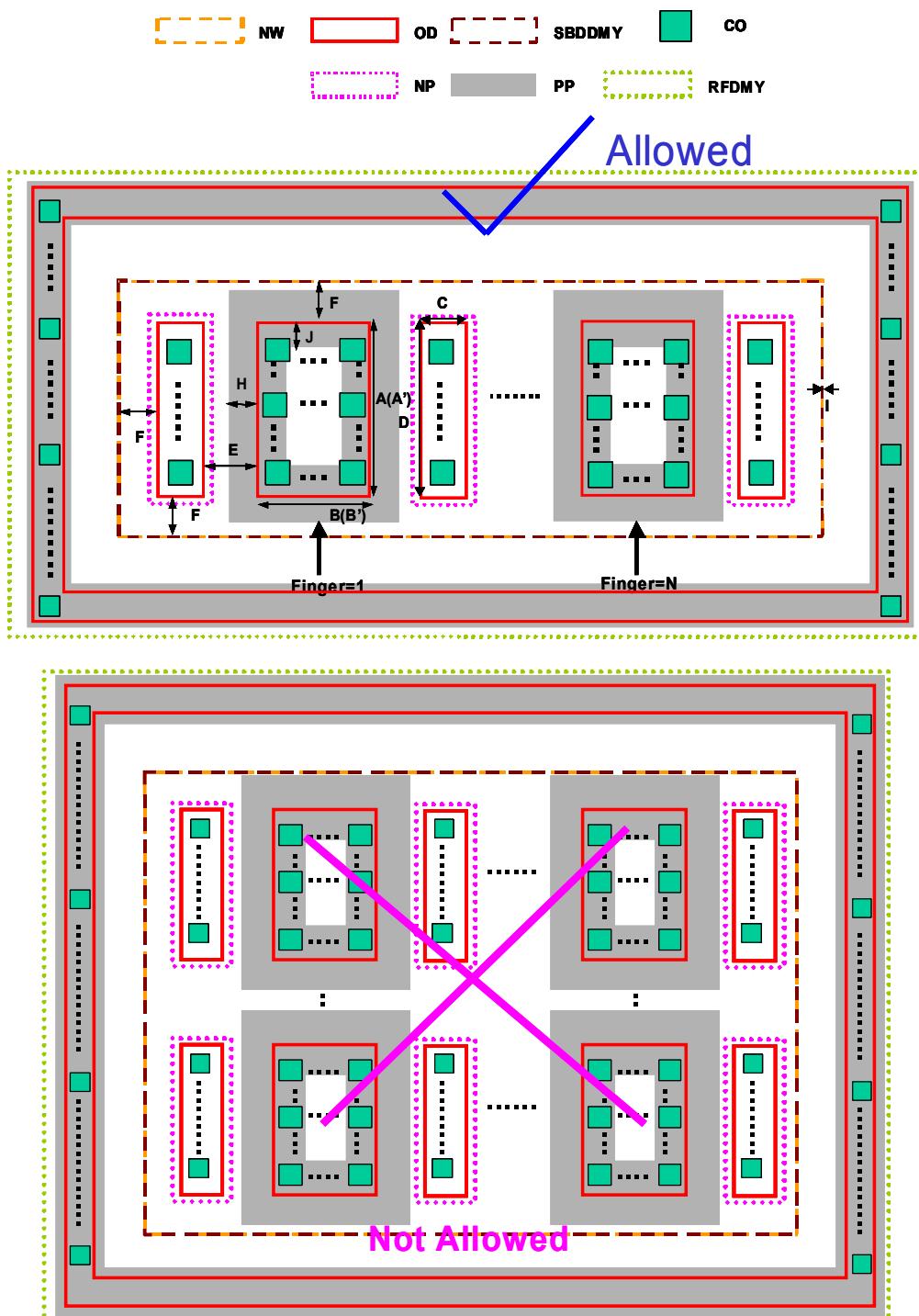


Fig. 4.6.9.3. SBD with DNW (multi-finger (N>1)).

Fig. 4.6.9.4 SBD without DNW (multi-finger ( $N > 1$ ))

## 4.6.10 The Chip Corner Stress Relief Pattern (CSR) and Seal Ring Rules for UTM

### 4.6.10.1 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns:

Below CSR rules only apply to a UTM design. MIM and other CSR rules of TSMC's standard layers please refer to section 4.5

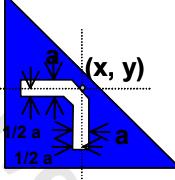
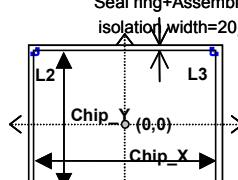
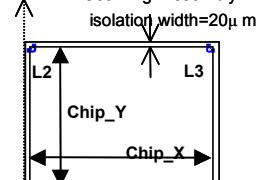
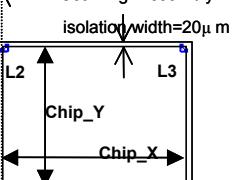
The chip corner stress relief pattern can reduce the impact of damage induced by thermal stress during packaging and field applications.

You can request TSMC to add the CSR pattern and the seal ring, and only CSR.R.1 in the following table must be met. If you want to add the CSR patterns and the seal ring by yourself, then you can use TSMC-offered sample GDS file (attached in this document) by following the CSR rules of this section (except CSR.R.1), and the seal ring rules.

- o *Sample GDS file for 3XTM L-mark seal-ring corner: N90SR\_3XTM\_L-mark\_UTM\_20080407.gds*
- o *Sample GDS file for 3XTM L-mark seal-ring corner of WLCSP: N90SR\_3XTM\_L-mark\_UTM\_20091023\_WLCSP.gds*

An alignment mark (L-mark) is drawn at each chip corner in the L-mark seal-ring corner. You can use this L-mark for the laser alignment of ID number verification or the metal fuse cutting purpose. If these L-marks can not meet your testing house requirement, you can find the L-mark rules in the following N90 fuse design rule document.

**The Reference coordinates of L-mark:** You can calculate the coordinates of L-mark by yourself, or follow the coordinates of the below table.

(Chip_X, Chip_Y)are the dimensions of thechip (without sealring and assembly isolation)			
L-Mark Coordinates ( $\mu\text{m}$ )	Coordinate A	Coordinate B	Coordinate C
	<p>Seal ring+Assembly isolation width=20<math>\mu\text{m}</math></p> 	<p>Seal ring+Assembly isolation width=20<math>\mu\text{m}</math></p> 	<p>Seal ring+Assembly isolation width=20<math>\mu\text{m}</math></p> 
(0, 0) is at the center of the chip		(0, 0) is at bottom-left of the chip with sealring (10 $\mu\text{m}$ ) and assembly isolation (10 $\mu\text{m}$ )	(0, 0) is at bottom-left of the chip without sealring (10 $\mu\text{m}$ ) and assembly isolation (10 $\mu\text{m}$ )
L1	(-0.5X+14.25,-0.5Y+14.25)	(34.25, 34.25)	(14.25, 14.25)
L2	(-0.5X+14.25, 0.5Y+14.25)	(34.25, Y+5.75)	(14.25, Y-14.25)
L3	(0.5X-14.25, 0.5Y+14.25)	(X+5.75, Y+5.75)	(X-14.25, Y-14.25)
L4	(0.5X-14.25,-0.5Y+14.25)	(X+5.75, 34.25)	(X-14.25, 14.25)

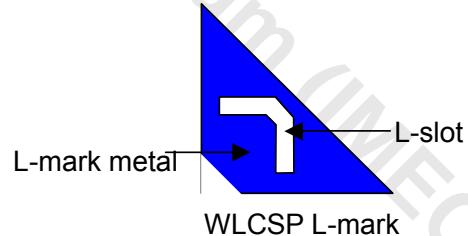
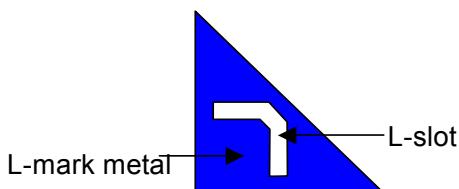
**L-mark metal:** a solid metal (top Cu metal) with an L shaped hole in LMARK.

**L-mark metal in CSR:** L-mark metal in a CSR pattern.

**L-slot:** L shaped hole in an L-mark metal

**L-mark metal layer:** Only one top Cu metal is required for L-mark metal, and AP for L-mark metal is not allowed. This seal ring is available only for UTM process without Cu RDL(MD). UTM layer CAD layer is the same as top metal like M9.

	Without Cu RDL (MD) -- for UTM process						
	1P3M	1P4M	1P5M	1P6M	1P7M	1P8M	1P9M
L-mark metal layer	M3	M4	M5	M6	M7	M8	M9



**General Information**

Chip-corner stress relief pattern and seal ring structures are based on the 1P9M process (M9 is UTM):

- The square CO/Via must follow each layer's width rule.
- For more than two top-metal layers (Mn+Mn or Mn+UTM) with generic top-metal thickness, the VIAx or VIAy below the thick metal (Mn or UTM) must follow CSR.S.3, CSR.EN.3, and the VIAx or VIAy rules.
- Please be careful with the non-generic logical operation, CAD bias, and shrinkage effects on the drawn dimensions of a stress relief pattern and seal ring.
- CSRDMY is a dummy mark layer aligned to the boundary of the stress relief pattern for DRC.

**For a flip-chip product without AP-MD**

- The CBD (mask code 107) layout is same as the CB layout.
- Please draw the AP (mask code 307) layer on the seal ring as shown in this chapter, in the "Chip Corner Stress Relief Pattern" section and in the "Seal Ring Rules" section.
- Don't draw the UBM (mask code 020) layout on the chip-corner stress relief pattern, seal ring, and assembly isolation structures. No UBM metal is allowed in these regions.

**For a product with AP-MD**

- The CB-VD (mask code 306) and CB2 (mask code 107) layout is same as the CB layout.
- Please draw the AP-MD (mask code 309) layer on the seal ring.
- Don't draw the UBM (mask code 020) layout on the chip-corner stress relief pattern, seal ring, and assembly isolation structures. No UBM metal is allowed in these regions.

#### 4.4.9.2 Chip Corner Stress Relief Pattern (CSR) Layout Rules:

Rule No.	Description	Label		Rule
CSR.R.1	Empty areas in four chip corners must be reserved and no layout is allowed inside if you request TSMC to add a chip corner stress relief pattern, seal ring... Fig. a shows the L-mark seal-ring corner.			


**Warning:**

TSMC add seal ring	
L-mark seal-ring corner	Developing

You need to add seal ring if you want to use L-mark seal-ring corner.

Violation of the CSR.R.1 rule may result in a serious layout mistake, and, therefore, many masks might need corrections. Please review the mask data after TSMC adds the stress relief pattern and seal ring.

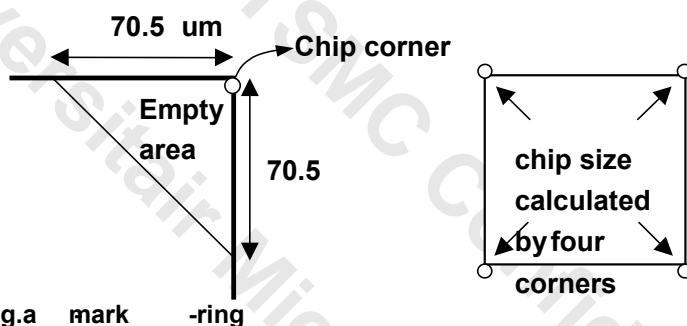


Fig.a mark -ring

**For customer-added stress relief patterns, seal rings, please refer to the following rules.**

CSR.R.2	The user must add a CSR in all four of the chip corners. The CSR should fill the four chip-corner areas as shown in Fig.a			
CSR.R.3	The CSR structure must include UTM9 (ultra thick metal)/ V8ind (inductor via)/ M8 (thick top metal) / VIA7 (top via)/M7/VIA6...VIA1/M1/CO/PP/OD layers. CSR is a fence type structure formed by crossed 1.5 $\mu\text{m}$ Mx-1 metal strips with CO/Via located at the metal crossing. Therefore, fully overlapped vias and metals of all levels are formed.			
CSR.S.1	CO space	A1	$\geq$	0.320
CSR.EN.1 <sup>U</sup>	CO enclosure by metal [crossing area]	B1	$\geq$	0.190
CSR.S.2	VIA1~VIA6 space at the same level	A2	$\geq$	0.290
CSR.EN.2 <sup>U</sup>	VIA1~VIA6 enclosure by metal [crossing area]	B2	$\geq$	0.175
CSR.S.3	VIA7 and V8 space	A3	$\geq$	0.400
CSR.EN.3 <sup>U</sup>	VIA7 and V8 enclosure by metal [crossing area]	B3	$\geq$	0.190
CSR.R.4	CO~VIA6/VIA7~V8ind number at the metal crossing area	D	$\geq$	(9, 4)
CSR.W.1	Width of L-slot	a	=	10
CSR.L.1	Length of L-slot	b	$\geq$	20
		b	$\leq$	25
CSR.EN.4	L-mark metal in CSR enclosure of L-slot [in the direction of the L-slot length]	c	$\geq$	4
		c	$\leq$	6
CSR.EN.5	L-mark metal in CSR enclosure of L-slot [perpendicular to the direction of the L-slot length] (Except WLCSP sealring region)	c'	$\geq$	27
		c'	$\leq$	29
CSR.EN.5.1	Metal layers of sealring corners can only exist isosceles triangle for WLCSP sealring region. An empty isosceles triangle area must exist butted to the WLCSP sealring outside corner.			
	Minimum length of isosceles triangle		$\geq$	15.5
	Maximum length of isosceles triangle		$\leq$	16.5
CSR.W.2	Width of 45 degree corner of L-slot	d	$\geq$	6
		d	$\leq$	8

Rule No.	Description	Label		Rule
CSR.W.3	Width of Via ring (CO/VIAx/VIA <sub>n</sub> /VIAy) around CSR pattern and L-slot	e	=	0.12/0.13/ 0.28/0.13
CSR.EN.6	Metal enclosure of (CO, VIAx, VIA <sub>n</sub> , VIAy ) around L-slot	f	≥	0.52
CSR.EN.7	Metal enclosure by L-mark metal in CSR around the L-slot	g	>	0.25

**General Information:**

Chip corner stress relief pattern and seal ring structures are based on the 1P9M (M9 is UTM) process:

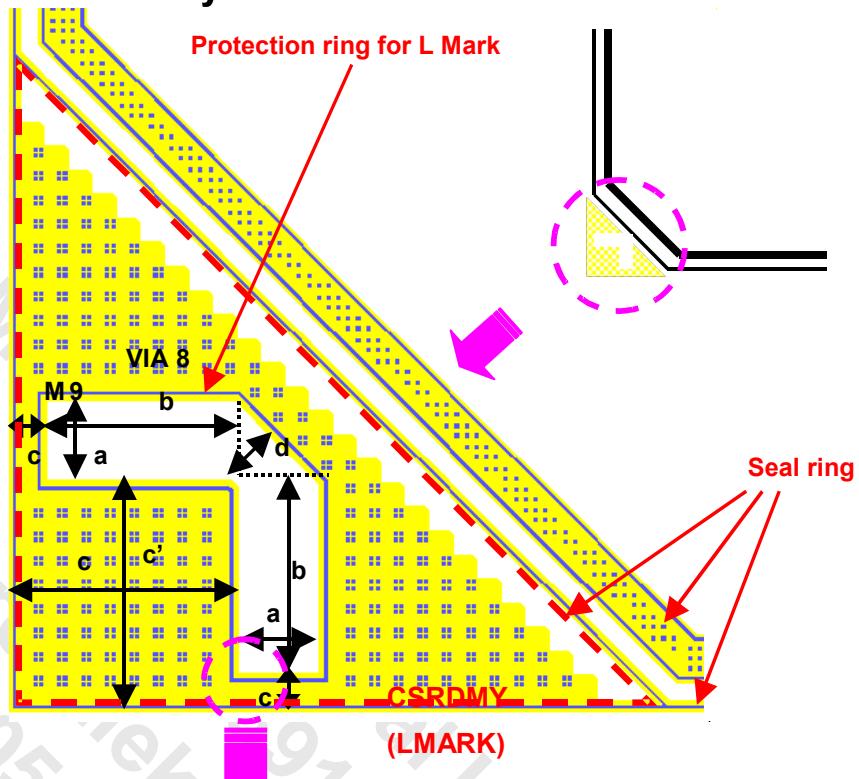
1. Square CO/Via must follow each layer's width rule.
2. Only one ultra thick (34 KÅ) top metal layer (UTM) can be used.
3. Please be careful with the non-generic logical operation, CAD bias, and shrinkage effects on the drawn dimensions of a stress relief pattern and seal ring..
4. CSRDMY is a dummy layer aligned to the boundary of stress relief pattern region I/II, for DRC.
5. For 1P8M process with M8 is UTM, please skip M7, VIA6 layers.
6. For 1P7M process with M7 is UTM, please skip M7, M6, VIA6,VIA5 layers.
7. For 1P6M process with M6 is UTM, please skip M7, M6, M5,VIA6, VIA5, VIA4 layers.
8. For 1P5M process with M5 is UTM, please skip M7, M6, M5, M4,VIA6, VIA5, VIA4, VIA3 layers.
9. For 1P4M process with M4 is UTM, please skip M7, M6, M5, M4, M3, VIA6, VIA5, VIA4, VIA3, VIA2 layers.
10. If you use low-K metal directly with UTM, Please also need skip M8,V7 layers.

**For flip-chip products**

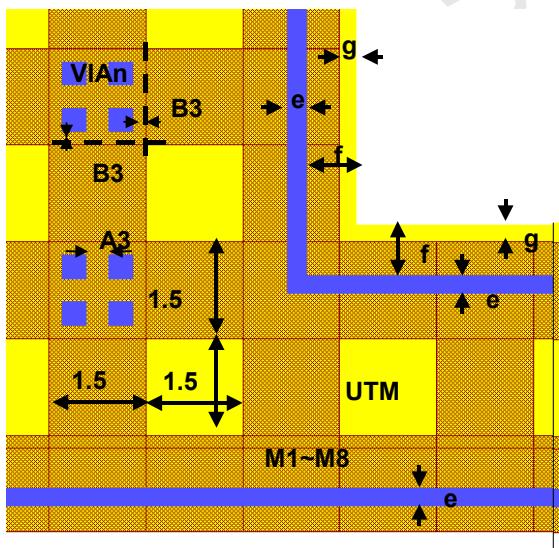
1. Don't draw a UBM (mask code 020) layout on the chip corner stress relief pattern, seal ring, and assembly isolation structures. No UBM metal is allowed in these regions.
2. Please draw PM (mask code 009 layer) on the seal ring and assembly isolation regions. No Polyimide is allowed in the seal ring and assembly isolation regions.
3. Please draw AP (mask 307 layer) on the seal ring as shown in this chapter's sections: "Chip Corner Stress Relief Pattern" and "Seal Ring Rules."

#### 4.6.10.1.1 L-mark Seal-ring Corner

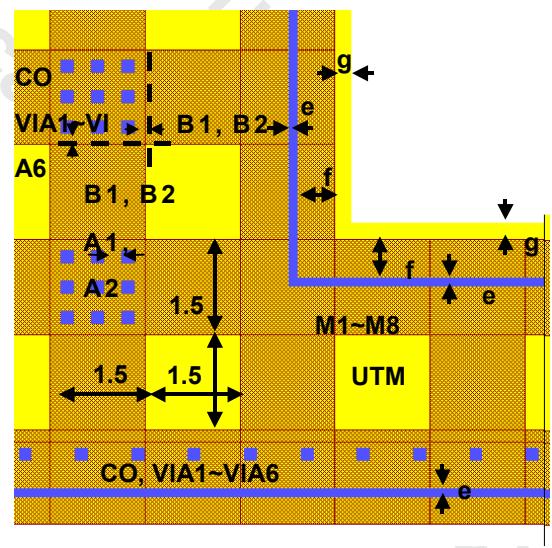
**Top view and L-mark Layout**



**VIAx and metal Layout**

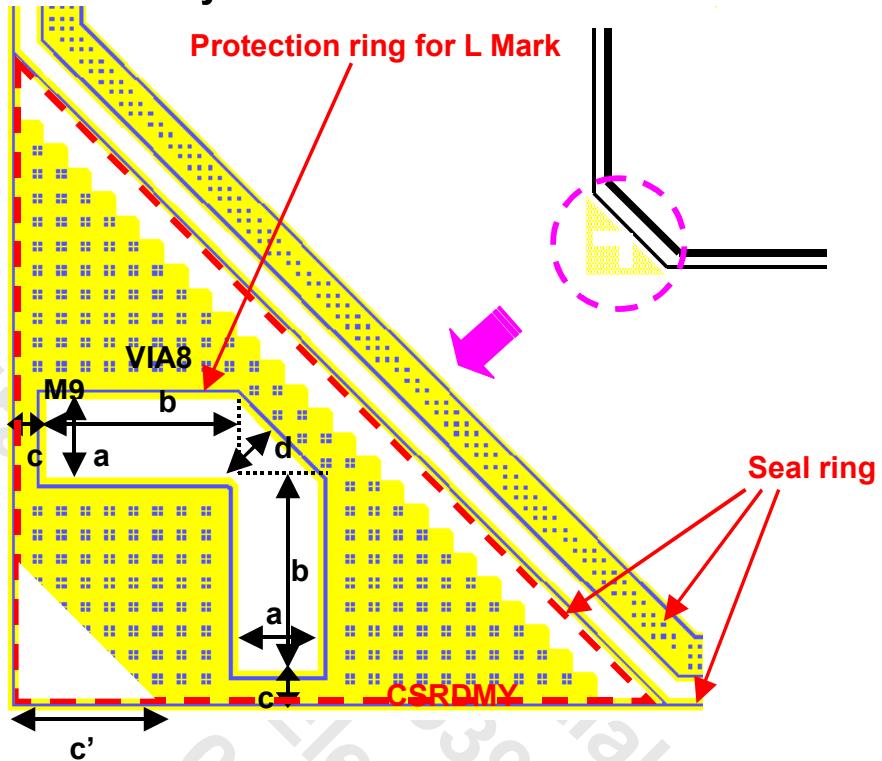


**CO/VIA1/VIAx and Metal Layout**



#### 4.6.10.1.2 L-mark Seal-ring Corner for WLCSP

##### Top view and L-mark Layout



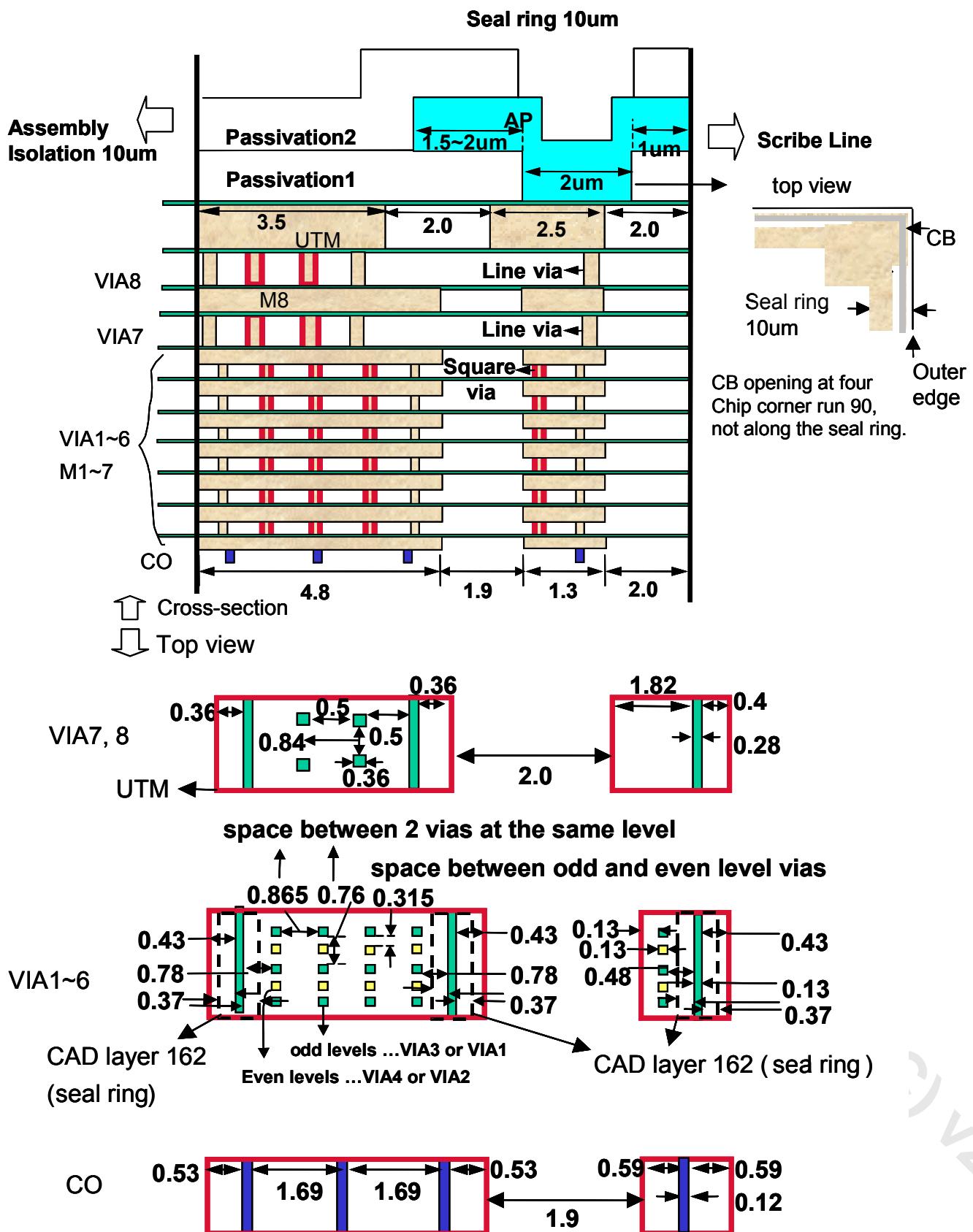
#### 4.6.10.2 Seal Ring Layout Rules for UTM:

Please follow exactly the schematic diagram in the figure in this section (as in the GDS example) for a seal ring layout. Currently, DRC can't fully check these dimensions. If you want to use dimensions other than those shown in the figure in this section, please consult with TSMC.

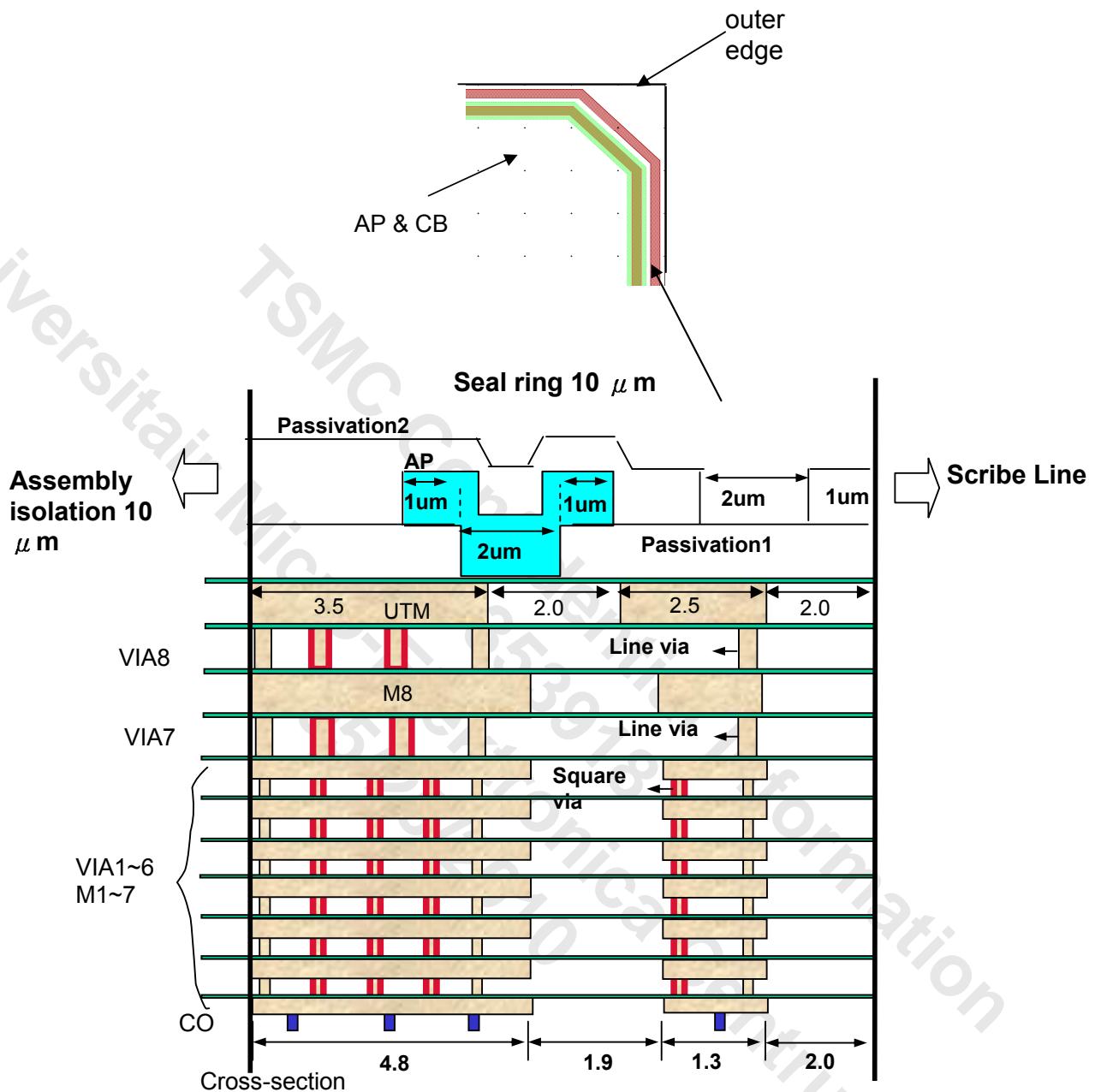
Assembly isolation depends on the capability of an assembly house. If TSMC adds a seal ring, TSMC will also add assembly isolation and a seal ring structure at the same time. TM8 layout is similar to M1/Mx in seal ring region. An AlCu pad (AP)/Polyimide(PM) can be generated by logic operation only for a non-flip-chip product.

Rule No.	Description		Rule
SR.EN.1	(OD interact seal ring) enclosure of metal with the outer edge of seal ring.	≥	2.0

## Cross-sectional view of seal ring From CO to Passivation



## Cross-sectional view of WLCSP seal ring



## 2. For other layers

— : Digitized area is clear on mask

— : Digitized area is dark on mask

**assembly isolation**

10 µm

**seal ring**

10 µm

Chip edge

Window edge

**From CO to CB,  
please follow above  
rules.**

5 µm

Layer	Scribe line tone
DNW (119)	D
OD (120)	D
PW1V (191)	D
NW1V (192)	D
PW2V(193)	D
NW2V (194)	D
VTC_N(112)	D
OD2 (132)	C
Poly (130)	C
N1V (114)	D
P1V (113)	D
N2V (116)	D
P2V (115)	D
NP (198)	D
PP (197)	D
ESD (111)	D
RPO (155)	D
CO (156)	D
M1 (360)	D
VIA1 (378)	D
M2 (380)	D
VIA2 (379)	D
M3 (381)	D
VIA3 (373)	D
M4 (384)	D
VIA4 (374)	D
M5 (385)	D
VIA5 (375)	D
M6 (386)	D
VIA6 (376)	D
M7 (387)	D
VIA7 (377)	D
M8 (388)	D
VIA8 (372)	D
M9 or UTM(389)	D
CB (107)	D
AP (307)	C
FUSE (395)	D
VTUH_P(217)	D
VTUH_N(218)	D
VTH_P(127)	D
VTH_N(128)	D
VTL_P(117)	D
VTL_N(118)	D
CTM (182)	C
CBM (183)	C

# 5 Wire Bond, Flip Chip and Interconnection Design Rules



Need to perform package qualification for change in wafer technology, wafer passivation scheme, die size, package type, package size and package material.

TSMC offers two kinds of AP-MD thickness; 14.5KÅ of AP-MD and 28KÅ of ultra thick AP-MD.

For lead-free bump design rule, please consult with tsmc.

This chapter provides the following general layout information:

- 5.1 Layout rules for wire Bond
- 5.2 Layout rules for EU/HL flip chip
- 5.3 Mechanical and thermal guidelines for FCBGA

## 5.1 Layout Rules for Wire Bond

### 5.1.1 Recommendations for Wire Bond

1. **Pad geometry selection:**
  - a. Three wire bond geometries are provided: (1) Single in-line; (2) Staggered; and (3) Tri-tiers.
  - b. Since the variable IO cells might be used on the same chip, different pad geometries on one chip are also allowed. In addition, to meet the pad geometry rules, a space between different pad geometries is also needed. Please refer to the rule of **CB.S.3**.
2. **Pad pitch and width:**
  - a. Whenever possible, use a larger pad pitch and size.
  - b. It's recommended to use a single pad size on one chip. If you use different pad sizes on one chip, you have to optimize the bonding conditions. You should consult your assembly house carefully.
3. **Polyimide (PM, mask 009):** By default, the PM mask is a reverse tone of the CB mask (or derived from the CB layer by logical operation). **Polyimide** is not a standard offer in N90 and N80. TSMC's dual passivation can cover all the mechanical related package reliability requirements. If you have a special need for polyimide, please contact TSMC.
4. **Dummy wire bond pads:**

**QFP packages:** Please add two dummy bond pads on each chip corner to form the double bond pads (Fig 5.1.2.2.1) for wire sweep protection during mold encapsulation of packaging.
5. **Lead-free packaging with Polyimide coated wafers:** For the lead-free reliability test requirement (260°C reflow temperature of pre-condition test), it's recommended to use a "Green" grade molding compound to prevent PM/molding compound interface de-lamination.
6. **For the N90/ N85 and N80, TSMC allows the use of AP-MD above Mtop as an additional interconnection layer.** It can provide low metal sheet resistance ( $R_s$ ) and reduce IR drop. Please refer to the design rules in the section 5.1.2.6.
7. **Test guideline** "Minimum power bus pin numbers per power design is need if  $I_{op} > 1000mA$ . " to improve over killed issues and throughput in testing. Minimum power pin number design is as below (M is the power pin number):

$$M_{min} = \frac{10 * I_{op}}{VDD_{nom} - VDD_{min}}$$

where  $VDD_{nom} = \frac{VDD_{max} + VDD_{min}}{2}$

$VDD_{max}$  : the maximum allowable operating VDD

$VDD_{min}$  : the minimum allowable operating VDD

$I_{op}$  : the current consumption of a nominal rating power supply VDD

### 5.1.1.1 Recommendations for Circuit Under Pad (CUP)

1. **Circuit under pad:** Metal routing, resistor, de-coupling capacitor, diode, well pickup, IO or ESD circuit are allowed to be placed under pad. However, analog circuit, SRAM, and sensitive circuits should not be placed under the CUP structure. You must consult TSMC if other devices are required to be placed under pad.
2. **Optimizing the wire bonding parameters on the first CUP product:** The bonding condition of CUP is different from the traditional fully stacked pad (non-CUP). It's recommended that the user optimize the bonding conditions on the first CUP product by using the following steps:
  - a. Study the bonding conditions first. Use DOE (Design Of Experiment) to optimize the bonding parameters (golden wire, time, power, bonding force, ...), and use the wire pull and ball shear test to find the process window.
  - b. IMC (Inter Metallurgic Compound) coverage check and a cratered test are also recommended.
3. **Control the junction temperature ( $T_j$ ) of High Temperature Operation Life (HTOL) test:  $T_j < 140^\circ\text{C}$ .**
4. **It's allowed to draw CUP pads and non-CUP pads on the same chip:** Please follow the steps below on your first product:
  - a. Use the same pad opening size for CUP and non-CUP pads, or as similar size as possible.
  - b. WBDMY must be drawn on CUP pads for DRC purposes.
  - c. Optimize the bonding condition by following item 2 above. Both CUP and non-CUP must be taken into consideration.
5. **For RF pad application:**
  - a. The CUP pad design can be used for RF pad application.
  - b. No circuits, metal routing, or dummy metal layers are allowed within the pad region as defined by WBDMY.
  - c. You should apply DMxEXCL (CAD layer: 150;x, x=1~8) in each metal layer under the CUP pad region to prevent any dummy metal from being generated within the RF pad region. The region of DMxEXCL is illustrated in section 5.1.2.3.2.

## 5.1.2 Wire Bond Rules

### 5.1.2.1 Mask Information

Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Type		Description
						WB1	WB2	
1	CB	107	C	43	-	1	0	Pass-1 pad opening for wire bond
2	CB-VD	306	C	Derived	RV, CB, FW_AP	0	1	Pass-1 VIA hole for wire bond
3	AP	307	D	Derived	CB	1	0	Al metal pad for wire bond
4	AP-MD	309	D	42	-	0	1	AP RDL for wire bond
5	FW_Cu	395	C	95; 0	-	*	*	Top metal Cu fuse window
6	FW_AP	30A	C	95; 20	-	0	*	AP fuse window
7	CB	107	C	43	-	1	0	Pass-2 pad opening for wire bond (same mask with Pass-1 mask)
8	CB2	308	C	86	-	0	1	Pass-2 pad opening for AP RDL
9	PM	009	D	Derived	CB, FW_Cu, FW_AP, LMARK	*	*	Polyimide window for wire bond (for C013 FSG only)
<b>WB1</b>		<b>Wire Bond without AP RDL (AP-MD)</b>						
<b>WB2</b>		<b>Wire Bond with AP RDL (AP-MD)</b>						

The definition of legends (0, 1, and \*):

0 : Does not use the mask

1 : Must use the mask

\* : Optional mask

## 5.1.2.2 Passivation Layer Open Rules

- The 80 µm tri-tier pitch is only for BGA packages.

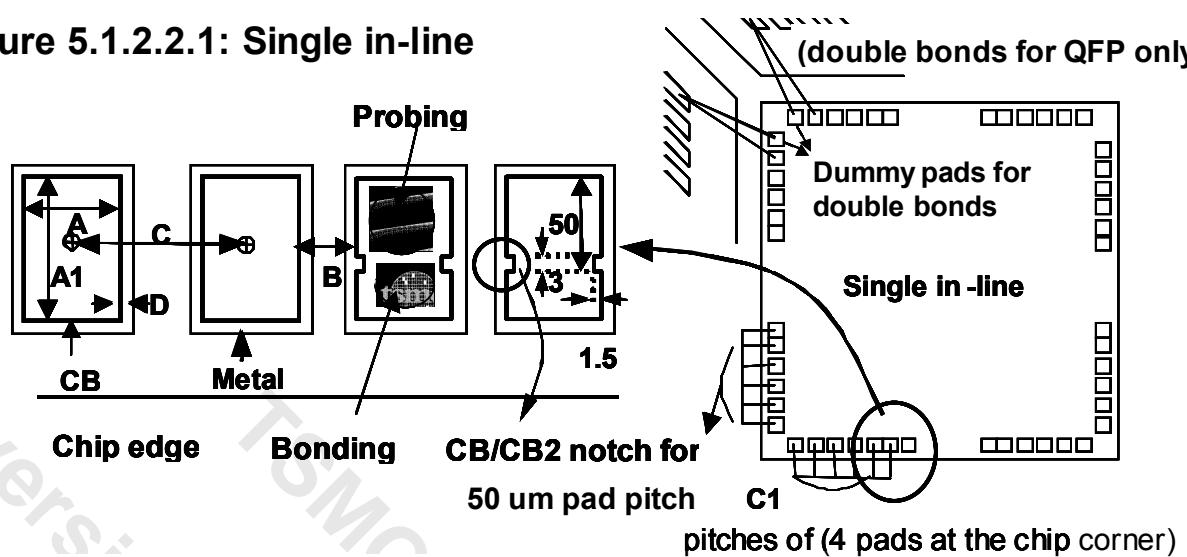
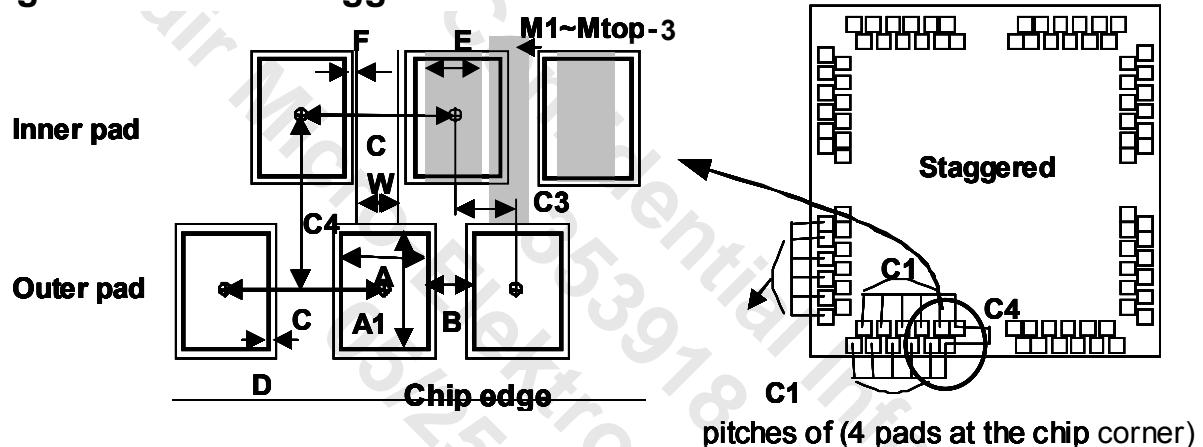
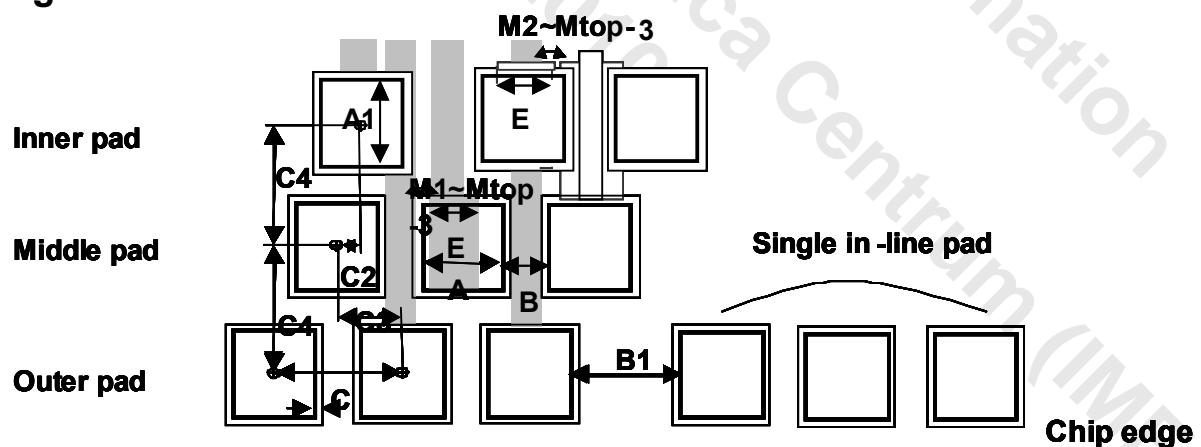
### Passivation window (CB/CB2)

Rule No.	Description	Label	Rule
#CB.W.1	Width of CB/CB2	A	≥ Table 5.1.2.2.1
#CB.W.2	Length of CB/CB2 (the edge perpendicular to nearby chip edge)	A1	≥ Table 5.1.2.2.1
CB.W.3	Width of pad metal under Mtop-2 within the CB/CB2 region Staggered: M1, M2~Mtop-3 under inner pad Tri-tier: M1, M2~Mtop-3 under middle pad M2~Mtop-3 under inner pad N90 CUP pad is excluded.	E	≥ Table 5.1.2.2.1
CB.W.4 <sup>u</sup>	Recommended total width of all metal layers connecting with bond pad.	W	≥ 10
#CB.S.1	Space of two CB/CB2	B	≥ Table 5.1.2.2.1
CB.S.2	Space of metal pad geometries, or space of metal pad to metal line DRC check metal pad by the following definitions: (1) {Mx AND [CB sizing 3]}, or (2) {AP-MD AND [CB2 sizing 3]}, or (3) {Mtop AND [CB sizing 3]} for N90 CUP pad	F	≥ 2.5
#CB.S.3	Space of the different pad geometries [(Single to Stagger), (Single to Tri-tier) or (Stagger to Tri-tier)]	B1	≥ 15
#CB.P.1 <sup>u</sup>	Pitch of (4 pads at the chip corner) Note: To start from the corners, the first four pitches must be larger than the pitch in the regularly repeating pad center area.	C1	≥ Table 5.1.2.2.1
#CB.P.2 <sup>u</sup>	Pitch of x-direction (inner and middle pad of Tri-Tier)	C2	≥ 13 ≤ 40
#CB.P.3 <sup>u</sup>	Pitch of x-direction [(inner and outer pad of Staggered) or (middle and outer pad of Tri-Tier)]	C3	≥ Table 5.1.2.2.1
#CB.P.4 <sup>u</sup>	Pitch of y-direction (between inner-middle-outer pad) Staggered: inner-outer pad Tri-Tier: middle-outer pad, and inner-middle pad	C4	≥ Table 5.1.2.2.1
CB.EN.1	CB enclosure by Mx and Mtop and CB2 enclose by AP-MD in pad regions Except, Staggered: M1, M2~Mtop-3 under inner pad Tri-Tier: M1, M2~Mtop-3 under middle and inner pad N90 CUP pad: M1~Mtop-1	D	≥ 1.5
#CB.R.1	For pad pitch < 55µm, one pair of notches on each pad CB/CB2 is required, to be the reference point for probing and bonding. Please refer to Figure 5.1 for the size and location.		

Table 5.1.2.2.1 Rule Summary of item A~E

Pitch(C)	A	A1	B	C1	C3	C4	E
≥50 single in-line	44	80	6	80			
≥55 single in-line	49	66	6	80			
≥60 staggered	53	66	7	100	30	96	20
≥70 staggered (Recommended)	58	72	12	100	35	102	45
≥80 staggered (Recommended)	65	75	15	108	40	115	50
≥80 tri-tier (BGA only)	65	75	15	108	40	115	50

This pad geometry can allow tighter pitch (< 55µm), but it needs the CB notch pairs to separate the probing and bonding locations (CB.R.1).

**Figure 5.1.2.2.1: Single in-line****Figure 5.1.2.2.2: Staggered****Figure 5.1.2.2.3: Tri-Tier**

## 5.1.2.3 Pad Structure Rules

### 5.1.2.3.1 Full Stacking Rules

- The mechanical properties of the low-k material in the Cu process require a careful design of the structure under the wire bond pad to provide mechanical integrity. Any violation, including structure or rule, may induce yield or reliability problems during testing and assembly.
- CB2 rules are applied for AP-MD process only.

#### Metal/Via/Passivation Window (CB and CB2) Rules

Rule No.	Description	Label		Rule
<b>Common items (for Single In-Line/ Staggered/ Tri-Tier)</b>				
CB.EN.1	CB enclosure by Mx/Mtop and CB2 enclosure by AP-MD in pad regions Except, Staggered: M1~Mtop-3 under inner pad Tri-Tier: M1~Mtop-3 under middle and inner pad	D	$\geq$	1.5
CB.R.5	1. Pad structure must be at least AP-MD/Mtop/ VIAtop...VIA1/M1. 2. AP-MD/Mtop pad metal is solid and without slots. 3. Parallel slots should be distributed over Mtop-1 ~M1 pad. Odd and even level slots orthogonal to each other, with via located on metal crossings, are recommended. Keep current flow direction parallel to metal in bond pad, as much as possible, to reduce resistance. 4. <sup>u</sup> Fully stacked vias of all levels (except VIAtop) and fully stacked metal of odd (even) levels are recommended. 5. Slot geometry in bond pad is rectangular. 6. {RV interact CB/CB2} is prohibited.			
CB.R.6	CB/CB2/ pad metal corners should turn 45°. Length of 45° edge.	U, V	$\geq$	2
			$\leq$	3

For more than one thick metal layer with top metal thickness, these thick metal layers are named ML. VIA layers below the thick metal are named VIAL.

Rule No.	Description	Label		Rule
CBVIAx.W.2	Width of VIAx	G	=	Table 5.1.2.3.1.1
CBVIAx.S.3	Space of two VIAx	H	$\geq$	Table 5.1.2.3.1.1
CBVIAx.EN.4	VIAx enclosure by Mx	I	$\geq$	0.05
CBVIAT.W.3	Width of VIAtop and width of VIAL	Ga	=	Table 5.1.2.3.1.1
CBVIAT.S.4	Space of two VIAtop and space of two VIAL	Ha	$\geq$	Table 5.1.2.3.1.1
CBVIAT.EN.2	VIAtop enclosure by Mtop-1/MT, and VIAL enclosure by Mtop-1/ML, and the lowest VIAL enclosure by the uppermost Mx.	Ia	$\geq$	Table 5.1.2.3.1.1
CBVIAx.R.3	Ratio of total exposure area of {VIA hole inside (CB or CB2)} to (CB or CB2) area Except: VIA1, VIA2 ~VIAtop-2 under inter row pad of Staggered VIA1, VIA2 ~VIAtop-2 under inter/middle row pad of Tri-tier	J		Table 5.1.2.3.1.1
CBVIAx.R.3.1	Ratio of total exposure area of {VIA1, VIA2~VIAtop-2 inside (CB or CB2)} to (CB or CB2) area (In the inter row pad of staggered and the inter/middle row pad of Tri-tier)	J1	$\geq$	Table 5.1.2.3.1.1
CBVIAx.R.4	VIAx/VIAtop/VIAL number at square metal crossing region with width equal to CBMx.W.2 in pad area (for orthogonal slot)	K	$\geq$	Table 5.1.2.3.1.1
CBMx.W.2	Width (Space of slots) of M1~Mtop-1 in pad area	L	=	1.5
CBMx.W.3	Width of M1~Mtop-1 pad ring (except 45° corners)	N	=	5
CBMx.S.2	Space (Width of slots) of M1~Mtop-1 in pad area	M	=	1
CBMx.S.3	Space (Width of 1 <sup>st</sup> slot) between M1~Mtop-1 ring and the nearest metal in pad area	P	$\geq$	1
			$\leq$	3.5

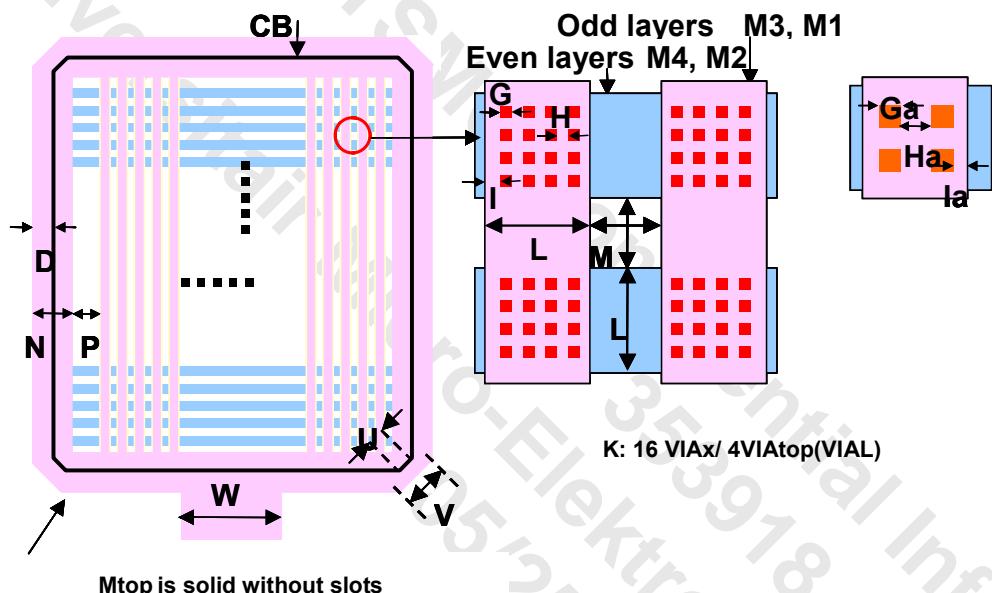
Table 5.1.2.3.1.1 Rule Summary of Item G~K

Technology	G	H	Ga	Ha	Ia	J	J1	K
CN90 (TM: Mn)	0.13	0.22	0.36	0.54	0.12	2.4 %	2%	16 / 4 ea
CN90 (2XTM: My)	0.13	0.22	0.26	0.54	0.12	2.4%	2%	16 / 4 ea

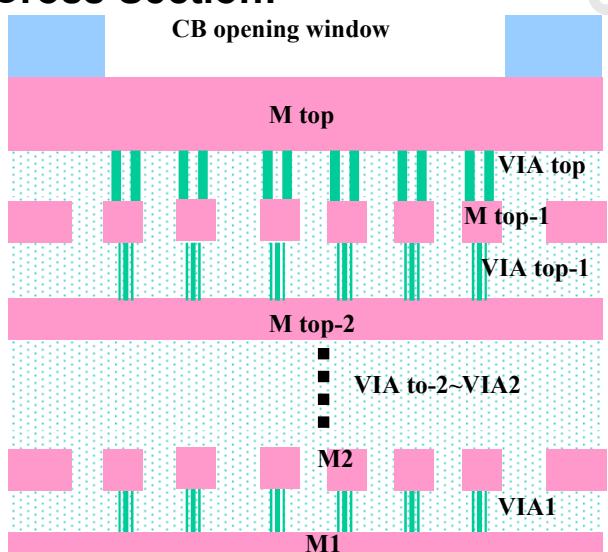
## Fully Stacking Pad Structure Schematic Diagram:

### Top View:

\*M1~Mtop-1 slot: Orthogonal slots between odd and even layers are recommended, for parallel slots, even layers are identical to odd layers.



### Cross Section:



### 5.1.2.3.2 CUP (Circuit Under Pad) Structure Rules

- The mechanical properties of the low-k material in the Cu process require a careful design of the structure under the wire bond pad to provide mechanical integrity. Any violation, including structure or rule, may induce yield or reliability problems during testing and assembly.

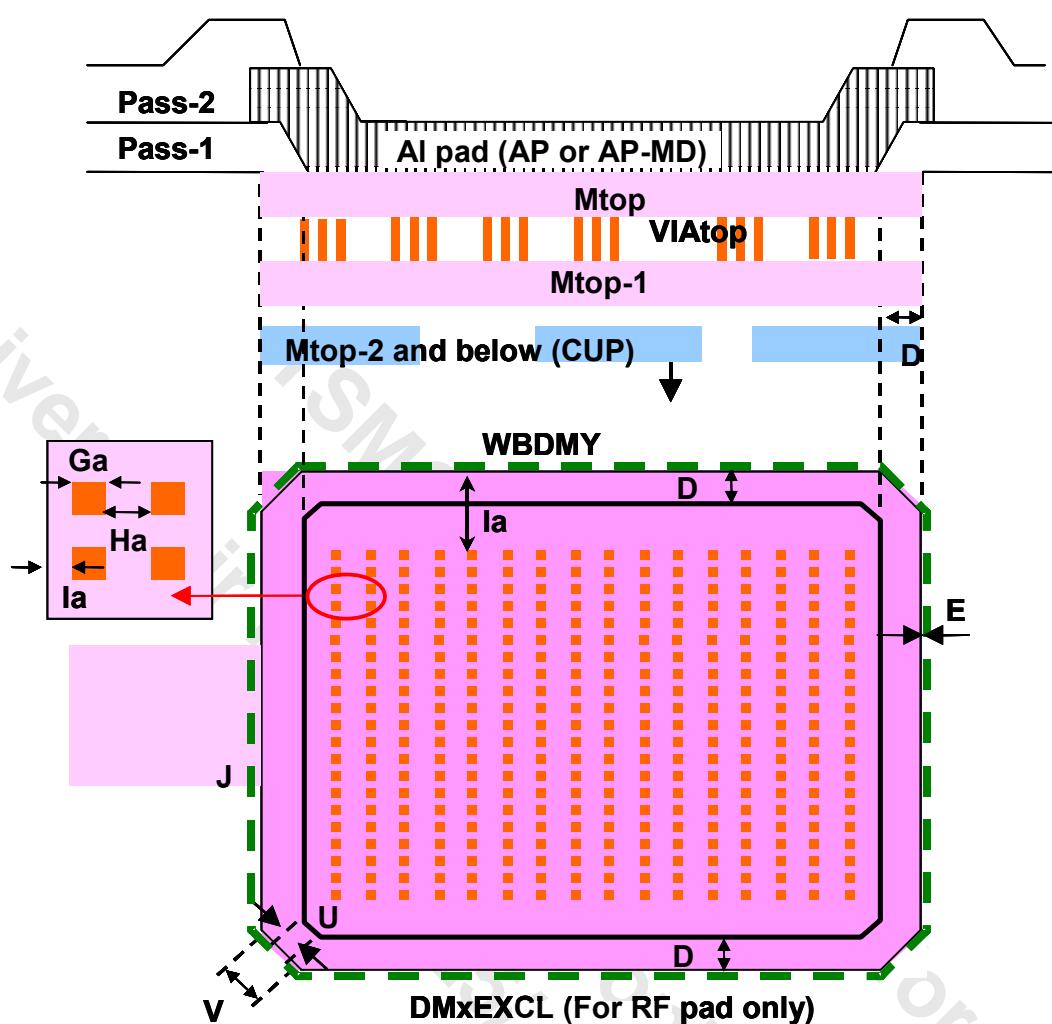
#### Metal/Via/Passivation Opening Rules for CB (without AP-MD) and CB/CB2 (with AP-MD):

Rule No.	Description	Label	Rule
CUPCB.EN.6	CB enclosure by Mtop, or CB2 enclosure by AP-MD [except circuit connection side]	D	$\geq$ 1.5
CUPCB.EN.7	Dummy layer WBDMY (wire bond pad region, N90 CAD layer is 183;0) is required for DRC purposes to cover the CUP pad area. WBDMY enclosure of metal pad (maximum = minimum) Metal pad: {(Mtop, Mtop-1) AND [CB sizing 3]}	E	= 0
CUPCB.R.7	CUP pad structure includes one level of solid Al pad (AP or AP-MD) and two levels of solid Cu metal (Mtop and Mtop-1) to form a bond pad. <ol style="list-style-type: none"> <li>Al pad (AP) is derived from the CB layer for no AP-MD process. For AP-MD process, Al pad (AP-MD) is required to be drawn by you.</li> <li>At least one Cu thick top metal is required for a CUP pad.</li> </ol>		
CUPCB.R.8 <sup>u</sup>	The AP-MD, Mtop, or Mtop-1 portion of the circuit connection side of the CUP pad structure are allowed to act for signal dispersion purposes.		
CUPCB.R.9	CB/CB2/AP-MD/Mtop/Mtop-1 solid pad corners should turn 45°. Length of 45° edge	U, V	2~3
CUPVIAT.W.1	Width of VIAtop	Ga	= Table 5.1.2.3.2.1
CUPVIAT.S.1	Space of two VIAtop	Ha	$\geq$ Table 5.1.2.3.2.1
CUPVIAT.EN.1	VIAtop enclosure by Mtop/ Mtop-1	Ia	$\geq$ Table 5.1.2.3.2.1
CUPVIAT.DN.1	Ratio of total exposure VIAtop area to CB/CB2 area within CB/CB2 region	J	$\geq$ Table 5.1.2.3.2.1
CUPVIAT.DN.2	Minimum via density over any 10x10 um CB area (checked by stepping in 5 um increments)	J1	$\geq$ Table 5.1.2.3.2.1

Table 5.1.2.3.2.1 Rule summary of VIAtop

Type	Mtop	Ga	Ha	Ia	J	J1
CN90	Mn or UTM	0.36	0.54	0.09	10%	10%
	My	0.26	0.37	0.05	12%	12%

## CUP WIRE BOND PAD STRUCTURE

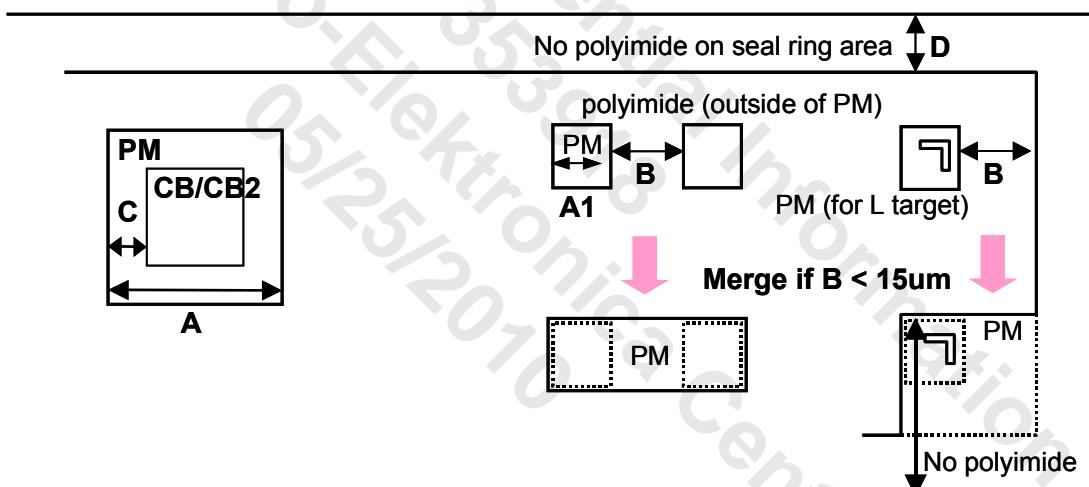


### 5.1.2.4 Polyimide (PM) Rules for Wire Bond

- Polyimide is not a standard offer in N90/ N85 and N80. TSMC's dual passivation can cover all the mechanical related package reliability requirements. If you have special need for polyimide, please contact TSMC.
- The rules are based on TSMC process capability. If you want to implement polyimide layer at the assembly house, please consult their rules.
- By default, the PM mask is generated by logic operation from CB (or CB2 for AP-MD) with the reverse tone of CB mask.
- The following rules must be followed if you draw the polyimide layout.

Rule No.	Description	Label		Rule
<b>Common items (for Single In-Line/ Staggered/ Tri-Tier)</b>				
PM.W.1	Width (Interact with CB/CB2 region)	A	$\wedge$	86
PM.W.2	Width (Not interact with CB/CB2/sealring region)	A1	$\wedge$	30
PM.S.1	Space of two PM, or space of PM to chip edge. Merge if space is less than 15 $\mu$ m.	B	$\wedge$	15
PM.EN.1	Enclosure of CB/CB2	C	$\wedge$	5
PM.R.3	Polyimide is prohibited over seal ring area	D		

**PM:**



### 5.1.2.5 Wire Bond Non-shrinkable Rules for the N85

- For design with a wire bond pad pitch below 53um (53um is before 94% shrink, and 50um is after 94% shrink), please consult your probe-card vendor in advance. Make sure that your probe-card vendor is able to provide such small pitch of wire bond pad.
- All of design rules for wire bond are shrinkable.** Please follow the related rules of the reference document.

### 5.1.2.6 Wire Bond Non-shrinkable Rules for the N80

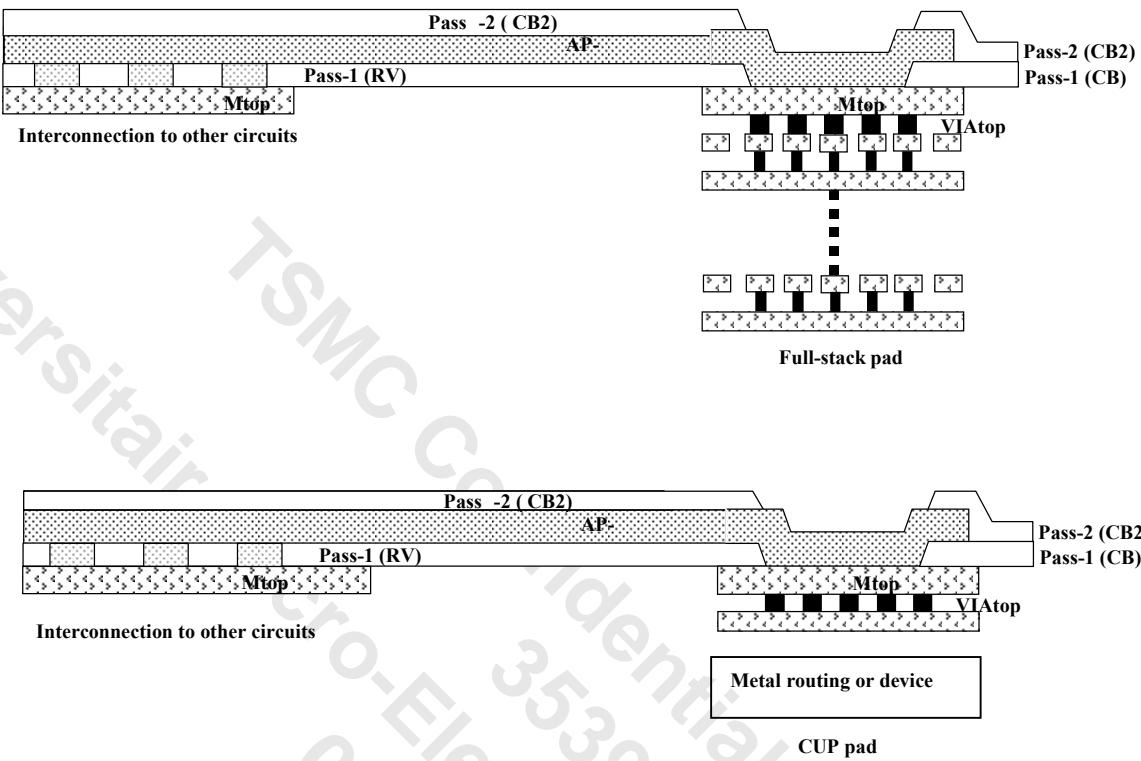
- The layout dimensions of the following items needs to be sized up before 90% shrinkage.

Rule No	Description	Rule		
		Pitch $\geq 50\mu\text{m}^{\ddagger}$ Single in-line	Pitch $\geq 55\mu\text{m}^{\ddagger}$ Single in-line	Pitch $\geq 60\mu\text{m}$ Stagger
#CB.W.1	Width	$\geq$	48.4	53
#CB.W.2	Length of (the edge perpendicular to nearby chip edge)	$\geq$	88	66 <sup>†</sup>
#CB.S.1	Space	$\geq$	6.6	6.6
#CB.P.1 <sup>u</sup>	Pitch of (4 pitches at each chip corner)	$\geq$	88	110

- Table notes:**<sup>†</sup> These rules are shrinkable.
- <sup>‡</sup> The pitch is real pad pitch after 90% shrinkage.

### 5.1.2.7 RV and AP-MD Layout Rules for Wire Bond

For N90/N85 and N80, TSMC allows the use of AP-MD above Mtop as an additional interconnection layer.

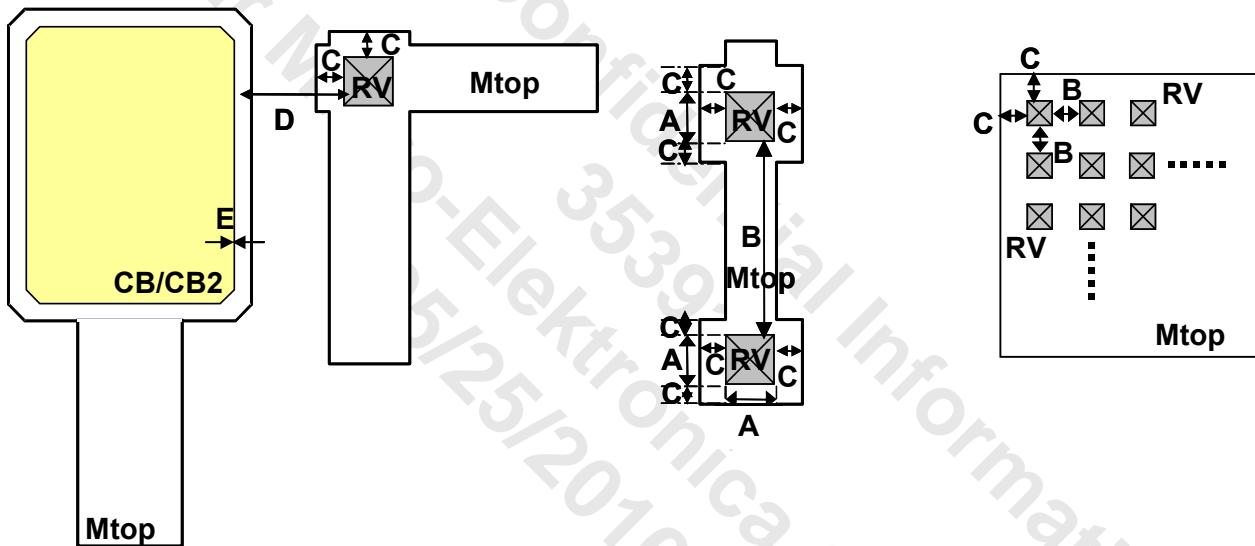


### 5.1.2.7.1 RV Layout Rules (CB VIA hole)

- CB-VD mask (306) is generated by the logical operation of CB (CAD layer: 76) and RV (CAD layer: 85).
- You must consider the RV counts to provide enough current for ESD requirements. Therefore, it's recommended to make as many RV holes as possible.

Rule No.	Description	Label		Rule
RV.W.1	Width (Square) (maximum =minimum) {Not inside seal ring}	A	=	3
RV.S.1	Space	B	$\geq$	3
RV.S.3	Space to CB/CB2/FW/FW(AP) [Overlap is prohibited]	D	$\geq$	6
RV.EN.1	Enclosure by Mtop {Not inside seal ring}	C	$\geq$	1.5
RV.R.1	A 45-degree rotated RV is prohibited. (Except WLCSP seal ring region)			
RV.R.2	{CB inside CB2} enclosure by CB2 (CB and CB2 must draw same size and identical shape)	E	=	0

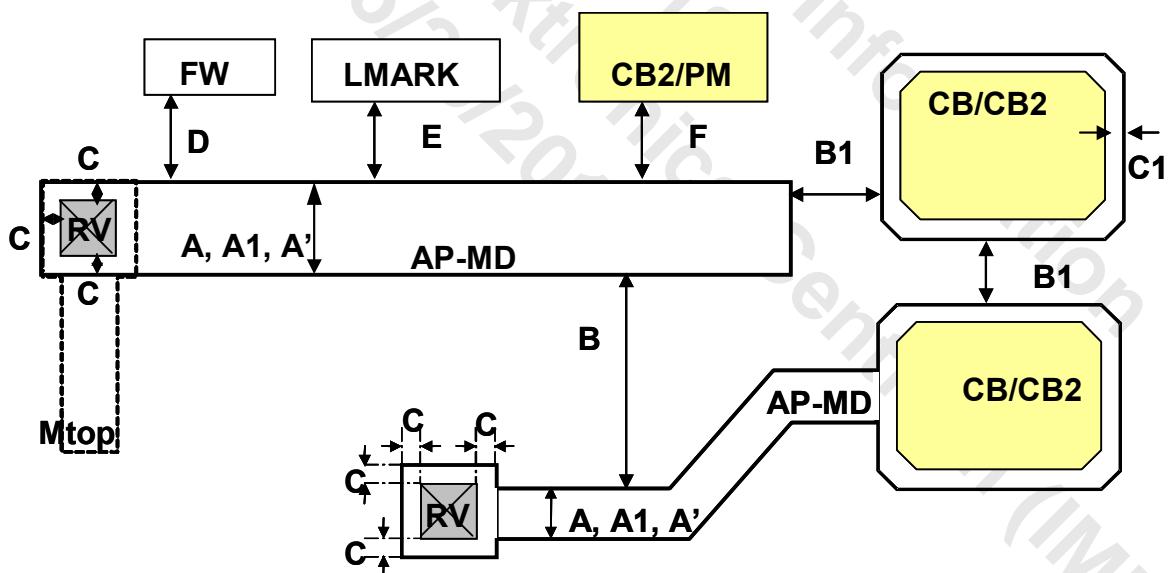
### RV:



### 5.1.2.7.2 AP-MD Layout Rules

Rule No.	Description	Label		Rule
AP.W.1	Width {Interconnection only} {Not inside FW(AP) or seal ring}	A	$\geq$	3
AP.W.2	Maximum width {Interconnection only} {Not inside CB or CB2}	A1	$\leq$	35
AP.W.2 <sup>U</sup>	Recommended total width of BUS line [Connect with bond pad]	A'	$\geq$	10
AP.S.1	Space	B	$\geq$	2
AP.S.1.1	{AP AND [CB2 sizing 3]} space to {AP AND [CB2 sizing 3]}, or space to AP routing (Except spacing in the same polygon)	B1	$\geq$	2.5
AP.S.2	Space to FW_CU/FW_AP [(Overlap FW_CU)/ (Cut FW_AP) is prohibited]	D	$\geq$	5
AP.S.3	Space to LMARK [Overlap is prohibited, except seal-ring]	E	$\geq$	5
AP.S.4	Space to CB2/PM [Overlap is prohibited, except bond pad region and seal ring]	F	$\geq$	3.5
AP.EN.1	Enclosure of RV {Not inside seal ring}	C	$\geq$	1.5
AP.EN.2	Enclosure of CB/CB2	C1	$\geq$	1.5
AP.DN.1	AP density across full chip		$\geq$	10%
			$\leq$	70%
AP.R.1 <sup>U</sup>	Maximum chip size for wire bond using AP-MD routing. Need to add polyimide layer for wirebond using AP-MD routing for die size $\geq= 100\text{mm}^2$ .		$\leq$	100 mm <sup>2</sup>

### AP-MD:



## 5.2 Layout Rules for EU/HL Flip Chip

### 5.2.1 Recommendations for EU/HL Flip Chip

#### 5.2.1.1 General Layout Recommendations

**1. Ground-up (Area-array I/O):** *Ground-up* refers to the interconnect layout style of a flip chip design in which the I/O cell and solder bump pads are distributed within the chip core (not placed in a ring outside the core) to take advantage of a minimum routing distance and chip size. Therefore, there is no redistribution layer required for a flip chip product with ground-up design.

The ground-up layout style is also known as an *area-array I/O* because the I/O circuits must be arranged in an array to minimize the distance between the I/O and the metal pads. The following information should be noted regarding the ground-up design at TSMC:

- The wafer process flow of ground-up (area-array I/O) products at TSMC's fab is identical to that of the wire bond products.
- Because the I/O circuits are no longer restricted to the periphery of the chip, there are things to be aware of to ensure good ESD and latch-up performance. For details, please refer to "I/O ESD protection circuit design and layout guideline" in the appropriate logic design rule manual.

**2. Die size and bump pad pitch selection:** Please take assembly process capability and packaging type into consideration. In the early design stage, it is very important to consider the bump pitch rules in your chip layout in conjunction with the substrate layout at the same time, especially for the small bump pitch design below 160um pitch. Please consult with your assembly house for the substrate information and process capability first. TSMC recommends following Table 5.2.1 to determine the proper bump pitch, UBM size and bump materials.

Table 5.2.1 Die size to bump pitch, UBM width and bump material selection

Chip Area ( $\text{mm}^2$ )	$A \leq 100$	$100 < A \leq 225$	$225 < A \leq 400$	$A > 400$
Min. Bump Pitch (um)	150	160	180	200
Min. UBM (um)	80	85	90	100
Bump Composition*	EU, HL	EU, HL	EU	EU

\* EU: eutectic, HL: high lead. For lead free application, please refer to LF design rule.



**\* Warning:** For design with a bump pitch below 160um, please consult your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.

#### 3. Required bumping and testing flow:

- TSMC's standard backend process for flip chip products is:

PM or passivation opening (fuse window [if applicable] etch)  $\Rightarrow$  WAT  $\Rightarrow$  (Fab out)  $\Rightarrow$  Solder bumping  $\Rightarrow$  Die sort (CP1)  $\Rightarrow$  Laser repair [if applicable]  $\Rightarrow$  Die sort (CP2) [if applicable]  $\Rightarrow$  Flip chip assembly  $\Rightarrow$  Final test (FT)

As a result, "die sort before bumping" is prohibited. Please contact TSMC for further technical support if needed.

- TSMC only allows HL/EU bump products at 150°C test. If you need higher baking temperature, please consult with TSMC.

Note: TSMC products' qual pass HTS/150°C 1000hrs reliability test.

**4. Mask making:** The below masks can't be generated by logical operation for flip chip design. You should provide the mask drawings in the tape-out GDSII file.

- o CB/CBD (mask107)
- o CB-VD (mask 306, for AP-MD only)
- o AP (mask 307)
- o AP-MD (mask 309, for AP-MD only)
- o CB2 (mask: 308, for AP-MD only)
- o PM (mask 009)
- o UBM (mask 020)

**5. Bumping and UBM (Under Bump Metallurgy) masks:** For bumping in TSMC, the UBM mask is needed for tape-out. For bumping in third-party bump houses, a UBM mask is not needed for tape-out to TSMC. Please consult with bump houses for their detailed UBM rules.

**6. Polyimide (PM):**

- o Polyimide is not a standard offering in N90 and N80. TSMC's dual passivation can cover all the mechanical related package reliability requirements. If you have a special need for polyimide, please contact TSMC.
- o If you don't use TSMC bump service, the PM layer should be implemented at your bump house, not at TSMC. This is to prevent the unpredictable compatibility problem that might happen between the PM and the bumping process.

**7. Backside grinding:** Wafer backside grinding is not recommended before bumping because of concerns about wafer breakage incurred in the bumping process. Therefore, backside grinding is allowed to a minimum 736.6um (29 mils) for 12" wafers.

**8. Alpha particle sensitive area:** Bumps on the top of the alpha particle sensitive circuit, like SRAM, are not recommended, except when ultra low alpha particle materials (Solder bump, under-fill, pre-solder bump...) are used. TSMC bump line uses ultra low alpha particle material. If the bumping is not done at TSMC, please consult with your bumping house about the alpha particle emission rate data and make sure your assembly house uses ultra low alpha particle materials. Please refer to the rules of UBM.R.4g and UBM.S.4® in the section 5.2.2.

**9. Dummy bumps:** Bumps that are farther away from the center of a die are generally more susceptible to higher mechanical stress. Dummy bumps that are distributed over the chip and that follow regular design rules are recommended for improving mechanical and thermal performance.

**10. Layout under bump:** Device placement and routing under bump pads is allowed.

**11. Orientation identifier:** For a chip with a perfectly symmetrical bump array, an orientation or a "marker" bump is recommended to create asymmetry and to avoid pick-and-place issues during flip chip assembly processes.

**12. Polyimide (PM)/CBD/CB2 window opening:**

Whenever possible, use a larger PM, CBD, or CB2 opening.

**13. For N90/ N85 and N80,** TSMC allows the use of AP-MD above Mtop as a redistribution layer (Wire-bond to Flip-chip, please refer to section 5.2.1.2) or an additional interconnection layer. This can provide low metal sheet resistance (Rs) and reduce IR drop.

**14. If you are going to design a new product with LF application, or you are going to migrate your current product from EU/HL to LF package, you have to follow the most updated LF design rule. There are several design rules which are tighter than the EU/HL, and are the key to have successful package reliability qualification.**

### 5.2.1.2 Recommendations for Redistribution Metal

1. **Redistribution layer:** *Redistribution* refers to the rearrangement from the traditional peripheral **wire bond pad** to the **solder bump pad array** by an additional interconnection metal, termed a redistribution layer, which is on the top of the original top metal (Mtop). A redistribution layer is used to convert a product from a wire bond to a flip chip package.

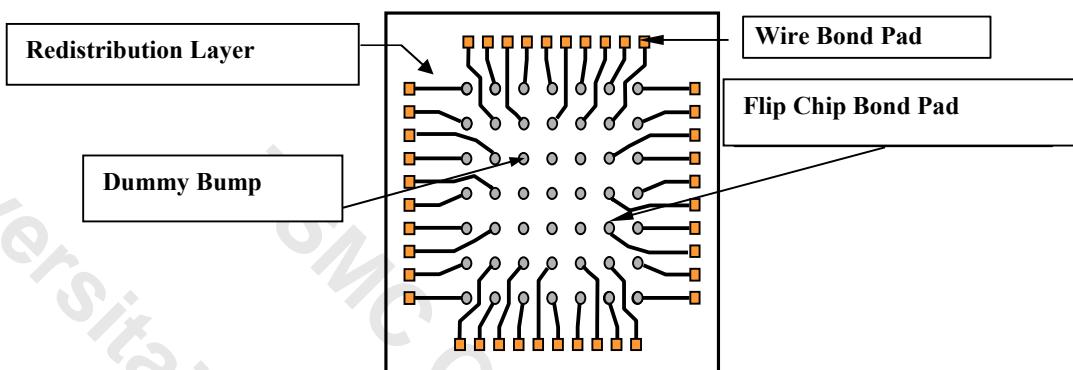


Figure 5.2.1.2 Schematic diagram of bump pad redistribution

2. **Interconnection for a solder bump of a flip chip package:** Two kinds of interconnection are offered for those who want to design the interconnection for a solder bump of a flip chip package.
  - a. **RDL (redistribution before passivation):**  
This interconnection style uses additional via (VIAD) and metal (MD) layers above the original top metal (Mtop). The VIAD and MD design rules and processes (film thickness and mask grade) are identical to the original ones of VIA<sub>top</sub> and M<sub>top</sub>.
  - b. **PPI (redistribution after passivation1 and passivation2):**  
This kind of process uses CB as a via hole to connect M<sub>top</sub> and PPI. Using the AP layer as PPI metal layer. (mask name: AP-MD, mask\_ID:309).
3. **I/O ESD protection recommendations:**
  - a. **Recommended minimum bus line width is 10μm.** The bus line width definition is the total width of all metal lines connecting with the same bump pad.
  - b. **Recommended maximum BUS line resistance from V<sub>dd</sub> pad or V<sub>ss</sub> pad to any I/O pad is 3Ω.**
  - c. **Recommended minimum counts of VIAD connecting to bump pad:** 300 each
  - d. **Recommended minimum counts of RV connecting to bump pad:** 9 each
4. Please refer to the “I/O ESD Protection Guideline” section in the corresponding design rule manual.

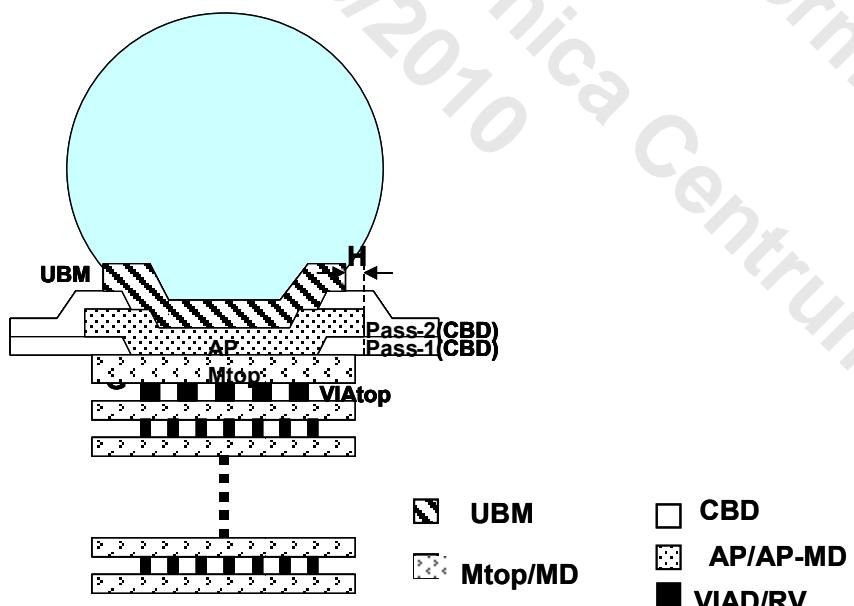
## 5.2.2 Under Bump Metallurgy (UBM) Rules

For lead-free bump design rule, please consult with tsmc.

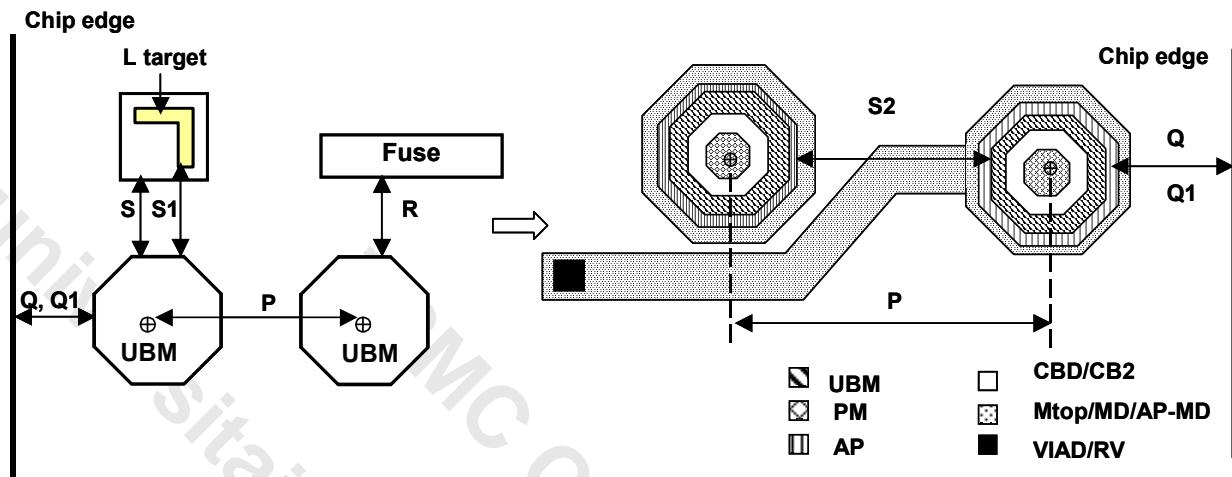
Rule No.	Description	Label	Rule																																
UBM.P.1	Pitch	P	≤ 150																																
UBM.S.1	Space to metal fuse protection ring	R	≤ 50																																
UBM.S.3	Space to L target	S1	≤ 80																																
UBM.S.4®	Space of two UBM (Maximum) It is recommended not to have isolated bumps, or avoid unnecessarily spare regions.	S2	≤ 400																																
UBM.EN.1	Enclosure by chip edge	Q	≤ 80																																
UBM.EN.1®	Recommended enclosure by chip edge (Maximum)	Q1	≤ 300																																
UBM.EN.2	Enclosure by AP/AP-MD	H	≤ 2																																
UBM.A.1® <sup>u</sup>	Area (without UBM in the chip center, for test inking requirement. Not necessary for inkless sorting)		≤ 750x750																																
UBM.DN.1	Density across full chip Dummy UBM is required if the UBM density is less than 10%. The dummy pattern should be as uniform as possible over the chip.		≤ 10%																																
UBM.DN.3	Maximum density of the non UBM sizing up area of whole chip for preventing isolated bump—the DRC will check this by: 1. Area density of whole chip NOT {UBM sizing + 200um} 2. Only one polygon is allowed after sizing up to prevent iso bump		≤ 20%																																
UBM.R.1 <sup>u</sup>	Shape of UBM/CBD/ PM/CB2 for bump: equilateral octagon is minimum requirement, and circle shape is recommended. Only single size bump/UBM is allowed.																																		
UBM.R.2 <sup>u</sup>	Dummy UBM that follow rules are required to improve mechanical strength and thermal dissipation.																																		
UBM.R.3	Bump ball (includes active bump and dummy bump) structure must include the layers (at least) in the below table. UBM pattern not for bump (for example, seal ring, part ID, fuse window, L target window, text mark or logo) is forbidden. <table border="1"> <thead> <tr> <th>Technology</th><th>Mtop</th><th>MD</th><th>CBD</th><th>AP</th><th>CB2</th><th>PM*</th><th>UBM</th></tr> </thead> <tbody> <tr> <td>N90</td><td>✓</td><td></td><td>✓</td><td>✓</td><td></td><td>✓</td><td>✓</td></tr> <tr> <td>N90 With Cu-MD</td><td></td><td>✓</td><td>✓</td><td>✓</td><td></td><td>✓</td><td>✓</td></tr> <tr> <td>N90 With AP-MD</td><td></td><td></td><td></td><td>✓</td><td>✓</td><td>✓</td><td>✓</td></tr> </tbody> </table> *: If you use polyimide in your design, the bump ball structure must include the PM layer as well.	Technology	Mtop	MD	CBD	AP	CB2	PM*	UBM	N90	✓		✓	✓		✓	✓	N90 With Cu-MD		✓	✓	✓		✓	✓	N90 With AP-MD				✓	✓	✓	✓		
Technology	Mtop	MD	CBD	AP	CB2	PM*	UBM																												
N90	✓		✓	✓		✓	✓																												
N90 With Cu-MD		✓	✓	✓		✓	✓																												
N90 With AP-MD				✓	✓	✓	✓																												
UBM.R.5	<b>Note: This rule is the difference between EU/HL and LF. Please refer to the most updated LF design rule to have a successful package design, no matter it is a new LF product or it is a migrate from EU/HL to LF.</b>  A minimum number of chip corner dummy bumps is required according to the chip size; these dummy bumps must be the ones that are nearest to chip corner among all bumps. Please refer to Figure 5.2.2.1 and Table 5.2.2. DRC checks the chip corner dummy bump by the following conditions: 1. The DRC deck defines a "UBM bounding box" for the whole chip by forming a smallest rectangle that contains all UBM bump pads. (Figure 5.2.2.1.) 2. At the corner of the "UBM bounding box", a "corner bump check zone" is then determined according to the chip size. (Table 5.2.2																																		

Rule No.	Description	Label		Rule
	defines the leg dimension of the corner bump zone.) 3. Check how many "chip corner bumps" interact with the "corner bump check zone" 4. Check whether the "chip corner bumps" are dummy bumps. 5. Dummy bump definition: Without Al RDL: Top metal of bump pad structure does not connect to any top VIA. With Al RDL: AP-MD of bump pad structure does not connect to any RV or CBD.			
UBM.R.6® <sup>u</sup>	Recommended size ratio of UBM/Pre-Solder Bump SRO (=C/N) and BGA SRO/Board Pad (=T/O). <b>Ratio=1.05 is preferred.</b> <b>SRO: Solder Resist Opening</b>		≤	0.95
			≥	1.05

Rule No.	Description	Label		Rule
UBM.R.4g <sup>u</sup>	It is recommended not to put any bump on the top of SRAM, analog, sensitive circuits, and the matching pairs. <ul style="list-style-type: none"><li>o The circuits should be located at a minimum distance of 60 µm from the bump pad's PM or CBD edge.</li><li>o It is also recommended to consider UBM.S.4® at the same time.</li><li>o If bump over SRAM, analog, or sensitive circuit areas is needed, it is recommended to use the ultra-low alpha particle materials in the bump and assembly processes (solder bump, under-fill, pre-solder bump...) to avoid a high Soft Error Rate (SER).</li><li>o TSMC uses ultra-low alpha particle materials in the solder bump process.</li></ul> If you could not meet UBM.S.4® and UBM.R.4g at the same time, you can consult TSMC for the layout suggestions.			
UBM.R.5g <sup>u</sup>	It is recommended not to place the IO bump pads in the 2 <sup>nd</sup> and 3 <sup>rd</sup> row in the bump array corner, but put Vss, Vdd, or dummy bump pads.			



## UBM: Top View



## Schematic diagram for UBM.R.5.

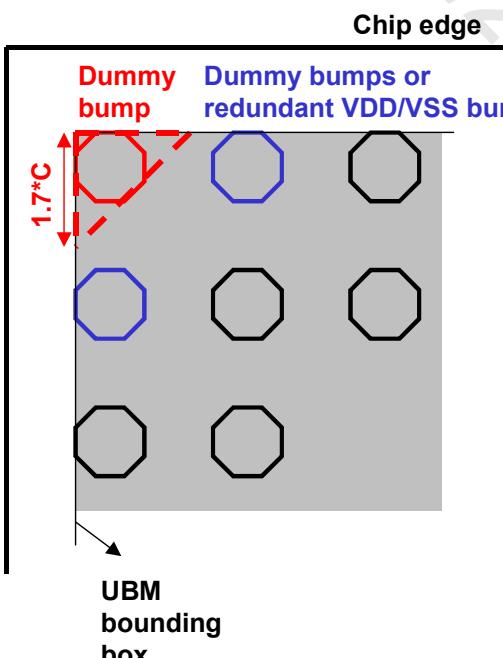
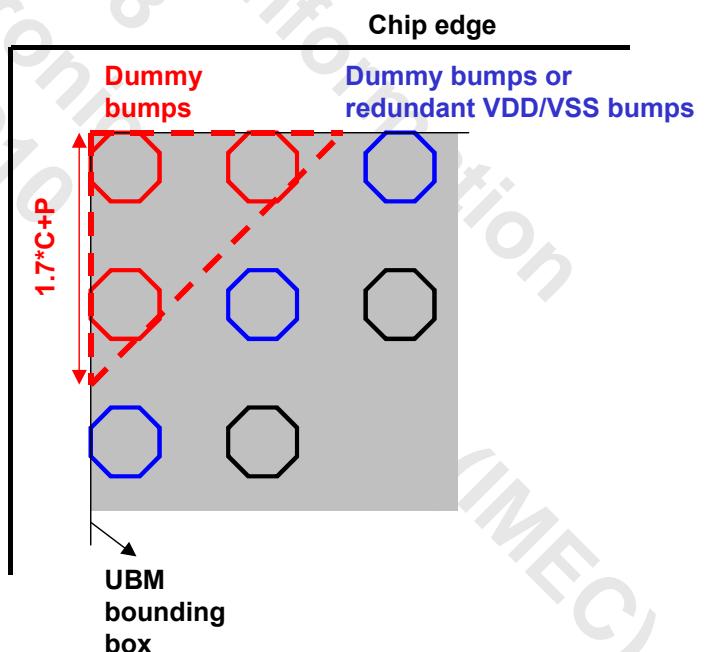
Area $\leq$ 225Area $>$ 225

Figure 5.2.2.1 Schematic diagram for UBM.R.5

Table 5.2.2. Area of active bump exclusion zone and dummy bump counts.

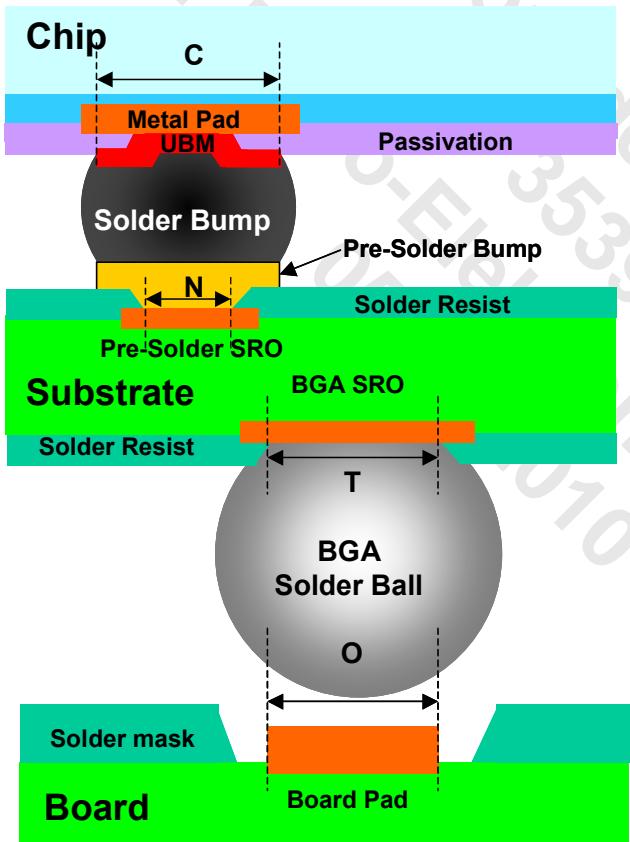
(1) Main node (Layout = On-Si)

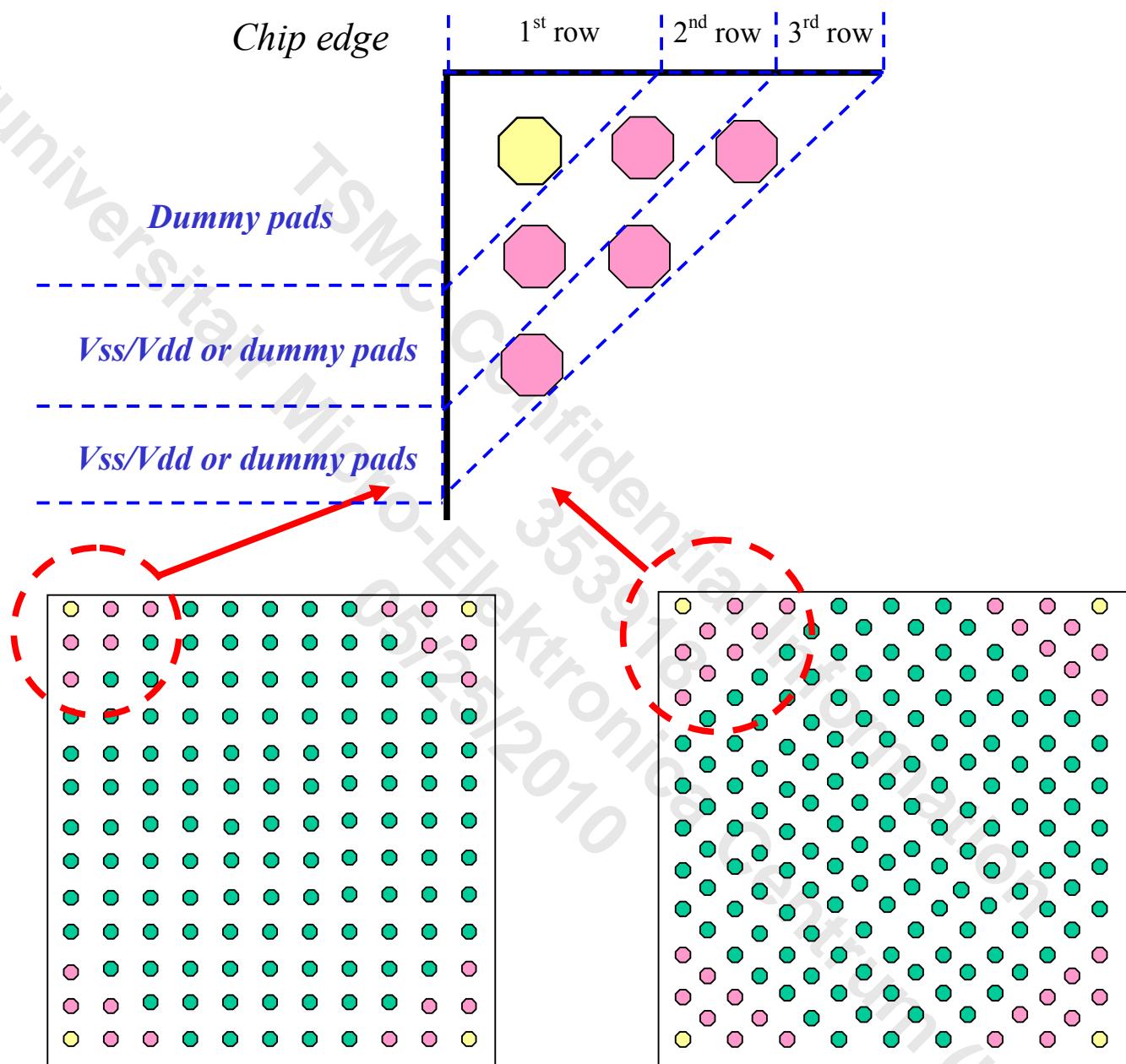
Design Dimension = On Silicon Dimension ( $\mu\text{m}$ )	Chip size ( $\text{mm}^2$ )	Area $\leq 225$	Area $> 225$
	Leg dimension of corner bump check zone	1.7*C	1.7*C+P
	Minimum dummy bump count	1	3

(2) Half node (111% blow up from main node (half node On-Si=100%; Layout=111%)

Design Dimension ( $\mu\text{m}$ )	Chip size ( $\text{mm}^2$ )	Area $\leq 278$	Area $> 278$	
	On Silicon Dimension ( $\mu\text{m}$ )	Chip size ( $\text{mm}^2$ )	Area $\leq 225$	Area $> 225$
	Leg dimension of corner bump check zone	1.7*C	1.7*C+P	
	Minimum dummy bump count	1	3	

C: UBM width; P: min. UBM pitch according to the chip size

**Schematic diagram for UBM.R.6®**

**Schematic diagram for UBM.R.5g<sup>U</sup>**

## 5.2.3 Flip Chip Rules

### 5.2.3.1 Mask Information:

- For the N90/ N85 and N80, TSMC allows to use of AP-MD and Cu-MD above Mtop as an additional interconnection layer.
- 
- Ground-up (with CBD) and AP-MD for redistribution layer (with RV) can be used on the same chip but need to confirm MT (mask tape-out) form about the mask and CAD layer information:
  - Ground-up: CB-VD mask (306) is derived from CBD (CAD layer: 169;0) by logic operation.
  - AP-MD redistribution: CB-VD mask (306) is derived from RV (CAD layer: 85;0) by logic operation.

#### Mask Information and CAD Layers

Sequence	Mask Name	Mask ID	Digitized Area (Dark or Clear)	CAD Layer	Reference Layer in Logical Operation	Type			Description
						FC1	FC2	FC3	
1	VIAD	371	C	167	-	0	1	0	Via hole between MD and Mtop
2	Cu-MD	383	D	168	-	0	1	0	Redistribution metal for flip chip
3	CBD	107	C	169	-	1	1	0	Pass-1 pad opening for flip chip
4	CB-VD	306	C	Derived	RV, CBD, FW_AP	0	0	1	Pass-1 VIA hole for flip chip
5	AP	307	D	42	-	1	1	0	Al metal pad for flip chip
6	AP-MD	309	D	42	-	0	0	1	AP RDL for flip chip
7	FW_Cu	395	C	95 ; 0	-	*	*	*	Top metal Cu fuse window
8	FW_AP	30A	C	95; 20	-	0	0	*	AP fuse window
9	CBD	107	C	169	-	1	1	0	Pass-2 pad opening for flip chip (same mask with Pass-1 mask)
10	CB2	308	C	86	-	0	0	1	Pass-2 pad opening for AP RDL
11	PM	009	D	5	-	*	*	*	Polyimide window for flip chip (for C013 FSG only)
12	UBM	020	D	170	-	1	1	1	Under bump metallurgy for flip chip
<b>FC1</b>		Flip chip without RDL							
<b>FC2</b>		Flip chip with Cu RDL (Cu-MD)							
<b>FC3</b>		Flip chip with AP RDL (AP-MD)							
<b>The definition of legends (0, 1, and *):</b> 0 : Does not use the mask 1 : Must use the mask * : Optional mask									

### 5.2.3.2 Bump Pad Structure Rules

- The following bump pad rules are used for the TSMC bumping process. If you do not use TSMC bump service, please consult your bumping house regarding these rules.
- Ground-up (with CBD) and AP-MD for redistribution layer (with RV) can be used on the same chip.

#### Bump Rules for Dual Passivation Schemes

Rule No.	Description	Label		Rule
BP.W.4	Width of CBD/CB2 under UBM area	A	$\geq$	40 (without PM)
BP.W.5				50 (with PM)
BP.W.6	Width of UBM (CBD width and PM width must conform to the following table)	C	=	Table 5.2.3.2.1
BP.EN.5	CBD/CB2 enclosure by UBM Without AP RDL, CBD not interact UBM is not allowed (except sealring, FW_AP, L-target). With AP RDL, CB2 not interact UBM is not allowed (except sealring, FW_AP, L-target).	E	$\geq$	10
BP.EN.6	PM enclosure by CBD/CB2	F	$\geq$	10
BP.EN.7	CBD enclosure by Mtop/MD	G	$\geq$	2
BP.R.1	CB2 on AP-MD for interconnection is prohibited [except UBM and sealring]			
UBM.EN.2	UBM enclosure by AP/AP-MD	H	$\geq$	2
BP.R.2®	Recommended bump pitch selection according to chip size.		$\geq$	Table 5.2.3.2.2*
UBM.R.7®	Recommended UBM width selection according to chip size.		$\geq$	Table 5.2.3.2.2*

Table 5.2.3.2.1 Bumping Pad Dimensions (Unit in  $\mu\text{m}$ )

P	Bump pitch	150-175*	175-200			200-225			$\geq 225$		
C	UBM width	80**	80**	85	90	90	100	108	100	108	
A	CBD/CB2 (without PM)	40-60	40-60	40-65	40-70	40-70	40-80	40-88	40-80	40-88	
	CBD/CB2 (with PM)	50-60	50-60	50-65	50-70	50-70	50-80	50-88	50-80	50-88	
B	PM	30-40	30-40	30-45	30-50	30-50	30-60	30-68	30-60	30-68	
Z	Bump height	80	80	85	90	90	90	100	90	100	90
X	Bump diameter <sup>†</sup>	105	105	109	117	117	123	129	127	134	123
									129	127	134
									145		

<sup>†</sup> Bump diameter depends on bump height for reference use

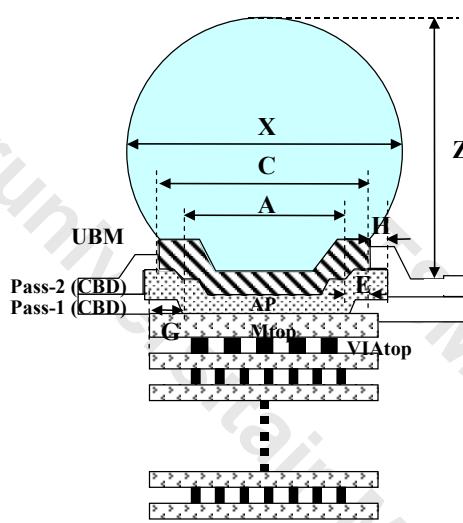
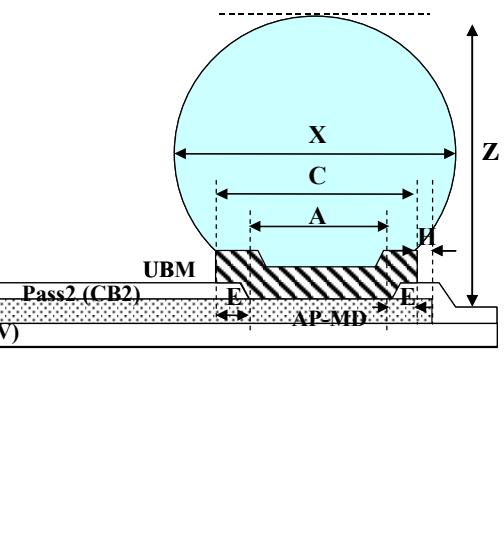
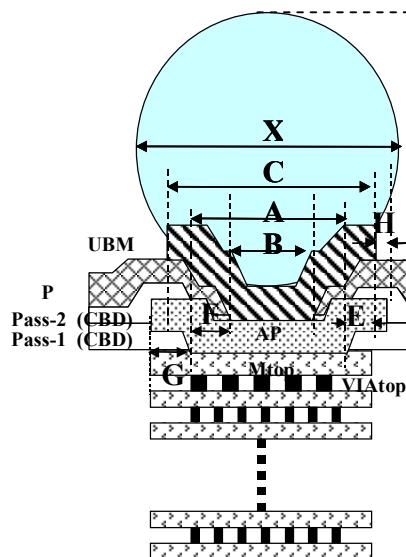
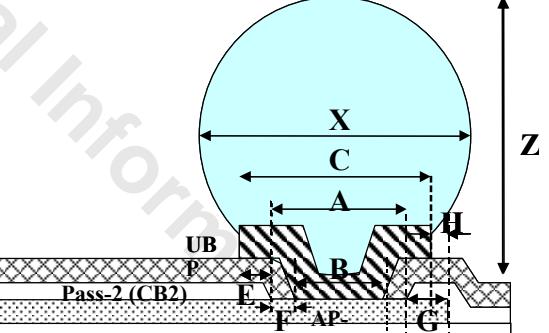
**Warning:** For design with a bump pitch below 160um, please consult your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.



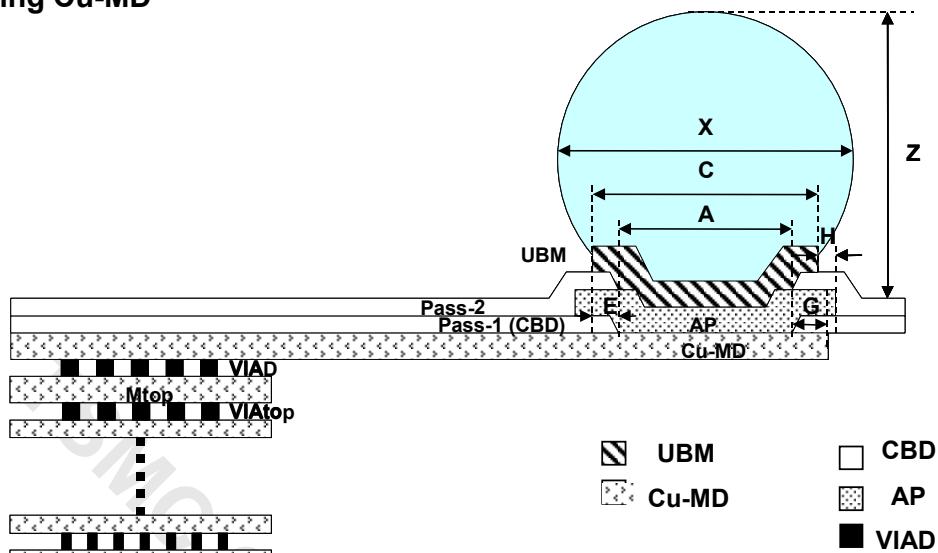
Table 5.2.3.2.2 Die size to bump pitch, UBM width and bump material selection

Chip Area ( $\text{mm}^2$ )	$\text{Area} \leq 100$	$100 < \text{Area} \leq 225$	$225 < \text{Area} \leq 400$	$\text{Area} > 400$
Min. Bump Pitch ( $\mu\text{m}$ )	150	160	180	200
Min. UBM ( $\mu\text{m}$ )	80	85	90	100
Bump Composition*	EU, HL	EU, HL	EU	EU

\* EU: eutectic, HL: high lead. For lead free application, please refer to LF design rule.

**Pass-1+Pass-2 for ground-up****Pass-1 (RV)+Pass-2 for using AP-MD****Pass-1+Pass-2+PM for ground-up****Pass-1 (RV)+Pass-2+ PM for using AP-MD**

## Pass-1+Pass-2 for using Cu-MD

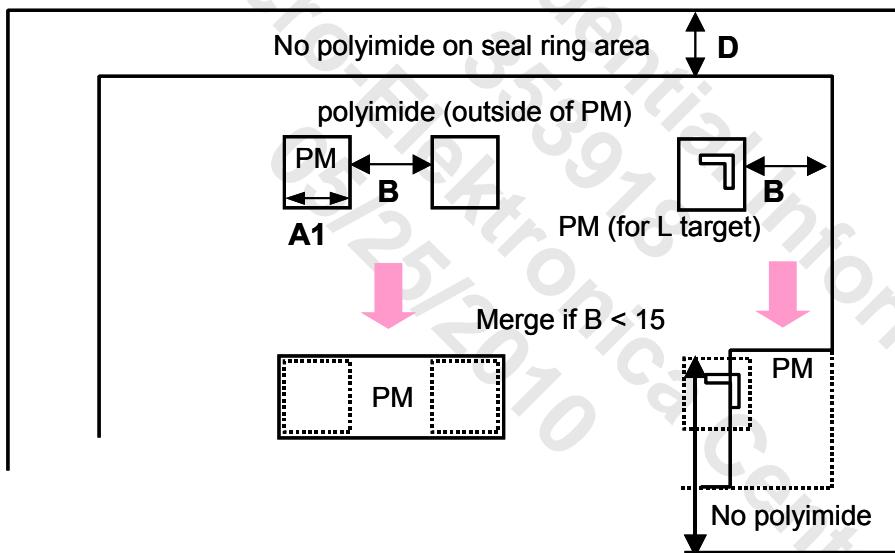


### 5.2.3.3 Polyimide (PM) Rules for EU/HL Flip Chip

- Polyimide is optional for the N90/ N85 and N80. TSMC's dual passivation can cover all the mechanical related package reliability requirements. If you have a special need for polyimide, please contact TSMC.
- Polyimide is must for LF application and rules are different from this section. Please refer to the most updated LF design rule.
- The rules are based on TSMC process capability. If you do not use TSMC bumping service, please consult your bumping house regarding these rules, and the PM layer should be implemented at your bump house, not at TSMC. This is to prevent the unpredictable compatibility problem that might happen between PM and bumping process.
- PM is a drawn layer for flip chip design. It cannot be generated by logic operation. You need to define the CAD layer in the tape-out information.

Rule No.	Description	Label		Rule
PM.W.2	Width (Not interact with CBD/CB2/sealring region)	A1	$\geq$	30
PM.S.1	Space of two PM, or space of PM to chip edge. Merge if space is less than 15 $\mu$ m.	B	$\geq$	15
PM.R.3	Polyimide is prohibited over the seal ring area.	D		

**PM:**



### 5.2.3.4 Flip Chip Non-shrinkable Rules for the N85

- The bumping rules for flip-chip design are critical on the bumping ball formation.** Customers must meet the non-shrinkable rules before 94% linear shrink.
- The bump height and diameter would decrease due to UBM shrinking.** Customers must evaluate this bump height change by themselves.



\* **Warning:** For the design with a bump pitch 150~175um (after shrink), please consult with your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.

Rule No	Description		Rule	Rule
			Die size < 15mmx15mm	Die size ≥ 15mmx15mm
UBM.P.1	Pitch	≤	170	191
UBM.S.1	Space to metal fuse protection ring	≤	53.2	53.2
UBM.S.3	Space to L target	≤	85.1	85.1
UBM.EN.1	Enclosure by chip edge	≤	85	85
UBM.EN.2	Enclosure by AP	≤	2.1	2.1
BP.W.4	Width of CBD/CB2	≥	43 (without PM)	43 (without PM)
BP.W.6	Width of UBM	≤	85	85
	CBD/CB2 enclosure by UBM Without AP RDL, CBD not interact UBM is not allowed (except sealring, FW_AP, L-target). With AP RDL, CB2 not interact UBM is not allowed (except sealring, FW_AP, L-target).	≥	10.6	10.6
BP.EN.5				

### 5.2.3.5 Flip Chip Non-shrinkable Rules for the N80

- The layout dimensions of the following items need to be sized up before 90% shrinkage.

Rule No	Description		Rule
UBM.P.1	Pitch	≥	165
UBM.S.1	Space to metal fuse protection ring	≥	55
UBM.S.3	Space to L target	≥	88
UBM.EN.1	Enclosure by chip edge	≥	88
UBM.EN.2	Enclosure by AP	≥	2.2
BP.W.4	Width of CBD/CB2	≥	44 (without PM) 55 (with PM)
BP.W.5	Width of PM under UBM area.	≥	33
BP.W.6	Width of UBM	≥	88
BP.EN.5	CBD/CB2 enclosure by UBM Without AP RDL, CBD not interact UBM is not allowed (except sealring, FW_AP, L-target). With AP RDL, CB2 not interact UBM is not allowed (except sealring, FW_AP, L-target).	≥	11.0



\* **Warning:** For design with a bump pitch below 160um (rule UBM.P.1, after shrinkage), please consult your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.

## 5.2.3.6 Redistribution Metal Layout Rules

- Users can use the metal layer before passivation (Cu-MD), or after passivation1 (AP-MD) as the redistribution metal. The thicknesses of the metal layer are listed in the following table.

Redistribution Metal	Before/After passivation	Before	After
	Metal layer	Cu-MD	AP-MD
	Metal type	Cu	Al
	Thickness (Å)	8.5K	14.5K 28K

### 5.2.3.6.1 General guidelines of MD Layout Rules for Cu process (Redistribution Metal Before Passivation)

- Please refer to the “I/O ESD Protection Guideline” section in the corresponding design rule manual.
  - The recommended minimum BUS line width is 10µm. (BUS line width = total width of all metal layers connecting with bump pad)
  - The recommended maximum resistance of the BUS line from V<sub>dd</sub> or V<sub>ss</sub> pads to any I/O pad is 3Ω.
  - The recommended minimum counts of VIAD connecting to a bump pad is 300.
  - The recommended minimum counts of RV connecting to bump pad is 9.

### 5.2.3.6.2 MD and VIAD Rules

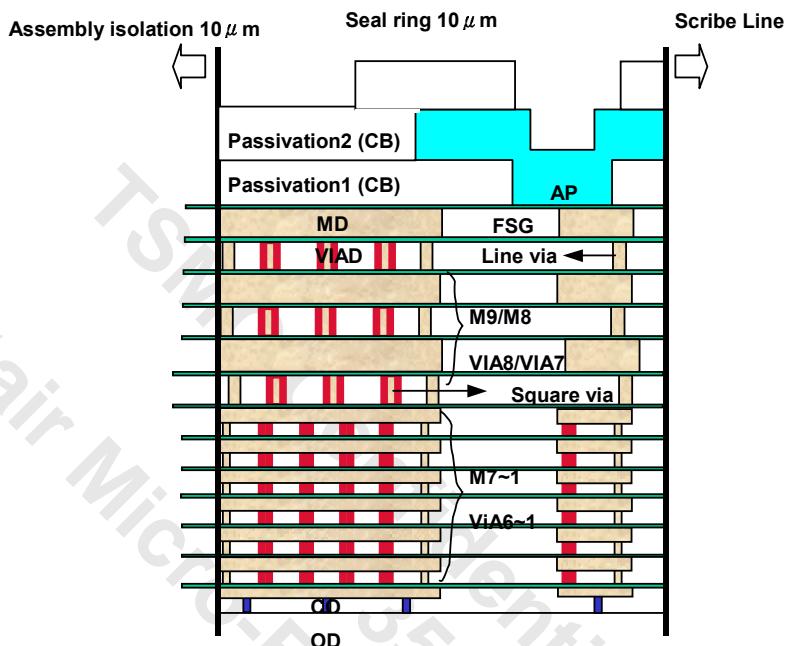
- MD and VIAD must follow the Mtop (Mn) and VIAtop(VIAn) rules of each logic design rule manual.
- VIAD is the via hole between two thick metals (Mtop and MD). The rule of VIAD enclosure by Mtop must follow the rule of Mtop (Mn) enclosure of VIAtop (VIAn).
- For the seal ring, antenna, current density, stress relief, and metal slot rules of VIAD and MD, please refer to the corresponding rule items in the section 4.5.

Rule section in the “Layout Rule Description” chapter of each logical Design Rule Manual		
VIAtop rule	Mtop rule	Other metal rule
Large Via Rule (VIAn)	Thick Metal Rule (Mn)	<ul style="list-style-type: none"> <li>Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9,D)</li> <li>Current Density (EM) Specification</li> <li>Chip Corner Stress Relief Pattern (CSR)</li> <li>Seal-Ring Rule</li> <li>Antenna Effect Prevention Design Rule</li> </ul>

### 5.2.3.6.3 Seal Ring Structure Using MD layer

- MD and VIAD layout within seal ring are the same as the Mtop and VIAtop layer.

**CN90 seal ring cross-section:**



## 5.2.3.7 RV and AP-MD Layout Rules (Redistribution AL Metal After Passivation 1)

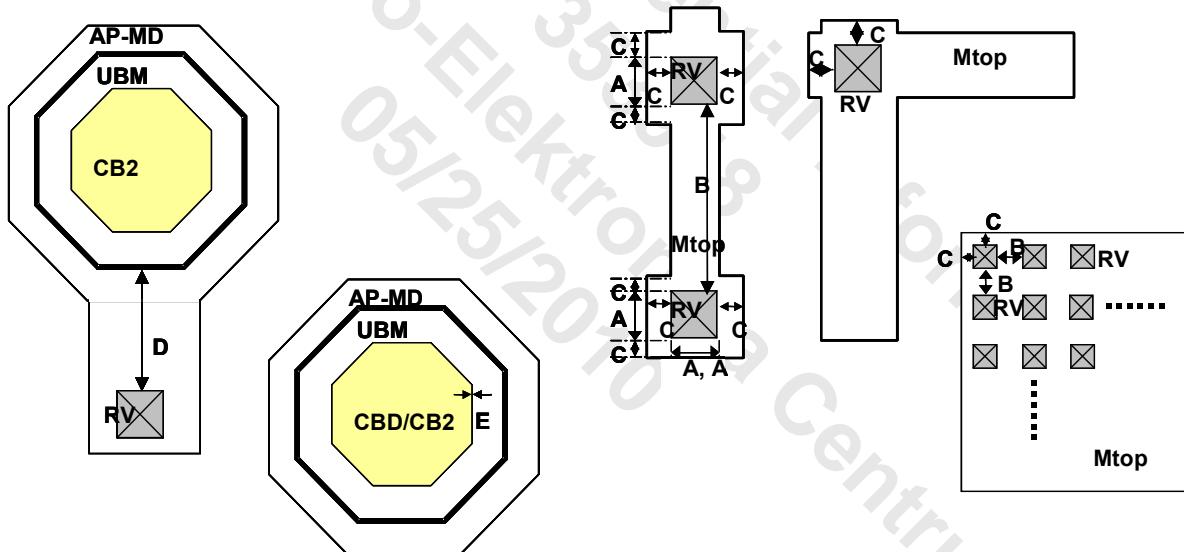
- CB-VD mask (306) is generated by the logical operation of CBD (CAD layer: 169) or RV (CAD layer: 85).

### 5.2.3.7.1 RV Layout Rules (Passivation-1 VIA Hole)

- You must consider that RV counts can provide enough current for ESD requirements. Therefore, it is recommended to make as many RV holes as possible.

Rule No.	Description	Label		Rule
RV.W.1	Width (Square) (maximum =minimum) {Not inside seal ring}	A	=	3
RV.S.1	Space	B	$\geq$	3
RV.S.2	Space to UBM [Overlap is prohibited]	D	$\geq$	0
RV.EN.1	Enclosure by Mtop {Not inside seal ring}	C	$\geq$	1.5
RV.R.1	A 45-degree rotated RV is prohibited (Except WLCSP seal ring region)			
RV.R.3	{CBD inside CB2} enclosure by CB2 (For ground-up design, CBD and CB2 must draw same size, and identical shape.)	E	=	0

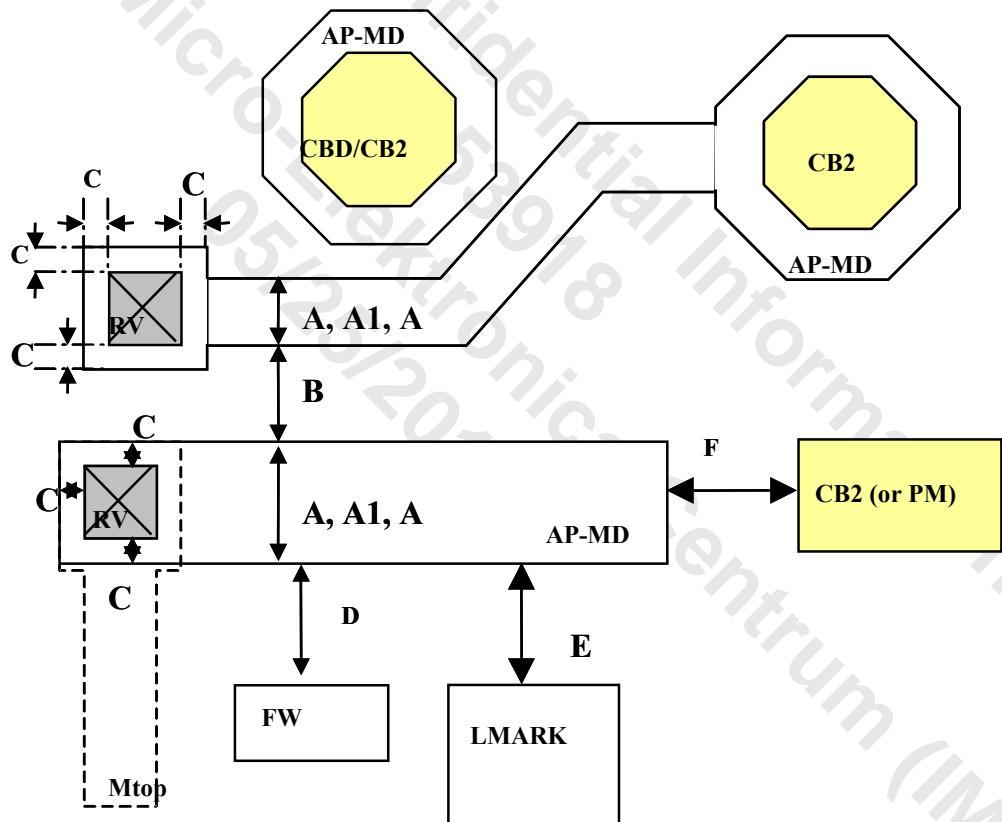
**RV:**



### 5.2.3.7.2 AP-MD Layout Rules

Rule No.	Description	Label		Rule
AP.W.1	Width {Interconnection only} {Not inside FW(AP) or seal ring}	A	$\geq$	3
AP.W.2	Maximum width {Interconnection only} {Not inside UBM, CB or CB2}	A1	$\leq$	35
AP.W.2® <sup>U</sup>	Recommended total width of BUS line [Connect with bump pad]	A'	$\approx$	10
AP.S.1	Space	B	$\approx$	2
AP.S.2	Space to FW_CU/FW_AP [(Overlap FW_CU)/ (Cut FW_AP) is prohibited]	D	$\approx$	5
AP.S.3	Space to LMARK [Overlap is prohibited, except seal-ring]	E	$\geq$	5
AP.S.4	Space to CB2/PM [Overlap is prohibited, except UBM region and seal ring]	F	$\geq$	3.5
AP.EN.1	Enclosure of RV {Not inside seal ring}	C	$\geq$	1.5
AP.DN.1	AP density across full chip		$\approx$	10%
			$\leq$	70%

#### AP-MD:



### 5.2.3.7.3 Seal Ring Structure Using AP-MD layer

- PM in N90/N85/N80 is optional.
- PM is prohibited to cover the seal ring.
- The seal ring structure is the same as section 4.5.

### 5.2.3.7.4 Antenna Effect Prevention (A) Layout Rules for RV and AP-MD

The antenna rules of RV and AP-MD for flip chip are the same as those for wire bond. Please refer to section 5.1.2.6.3 for the associated rules.

## 5.3 Mechanical and Thermal Guidelines for FCBGA

1. FCBGA (Flip Chip Ball Grid Array) package is used for high performance devices with high I/O counts, high power, advanced silicon technology, and sophisticated circuit design. Large die size coupled with high power makes FCBGA susceptible to reliability concerns associated with thermal behavior. Special attention is also needed when dealing with mechanical behavior on low-k devices. Through appropriate package designs from thermal and mechanical behavior perspectives, the FCBGA reliability issue can be significantly improved.
  2. If the product has the following features, the mechanical and thermal behavior must be taken into consideration in the chip design:
    1. Higher power device
    2. Larger die size
    3. Die with low K dielectric material
  3. The thermal and mechanical guidelines for FCBGA are to reduce product and package reliability issues during packaging technology development. Through thermal and mechanical analytical and experimental assessment, TSMC can provide the following information and suggestions within the guidelines:
    - i. Substrate thermal conductivity impact.
    - ii. Heat spreader thickness effect.
    - iii. Package thermal budget assessment.
    - iv. Die size consideration related to thermal solution design.
    - v. Die/substrate warpage with given underfill selection.
    - vi. Critical stresses on low k layer with given underfill selection.
    - vii. Packaging materials recommendations such as the selection of underfill and thermal interface material (TIM) with given die and package design.
4. Selected examples based on package design and/or packaging material selection, are shown below to articulate the effect of each attribute.
- i. Mechanical attributes and effect on low-K stress
    1. The selection of adequate underfill material can reduce low-K or bump stress.
    2. The smaller die size to the package introduces the lower stress in low-K and bump.
    3. Increasing the SRO size defined by the solder resist (down UBM/SRO size ratio) has a great and positive effect on bump reliability and impacts slightly the reliability of low-K. Keep UBM/SRO size ratio closed to 1.0 could balance the stress in low-K and bump.
    4. The selection of adequate heat spreader thickness can reduce low-K or bump stress.

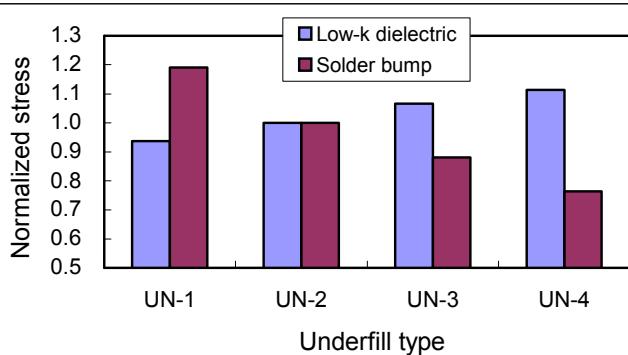


Fig. 5.3.1 Low-K/bump stress vs. underfill

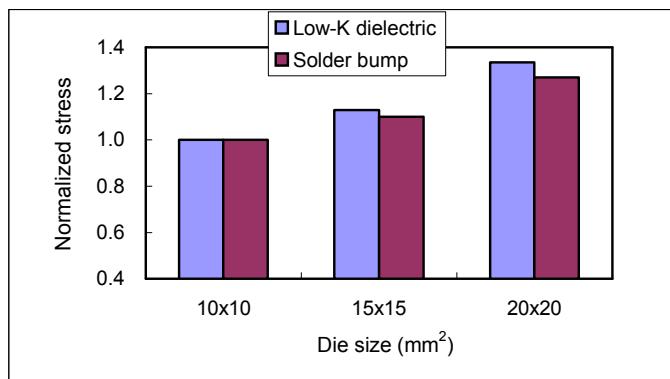


Fig. 5.3.2 Low-K/bump stress vs. die size

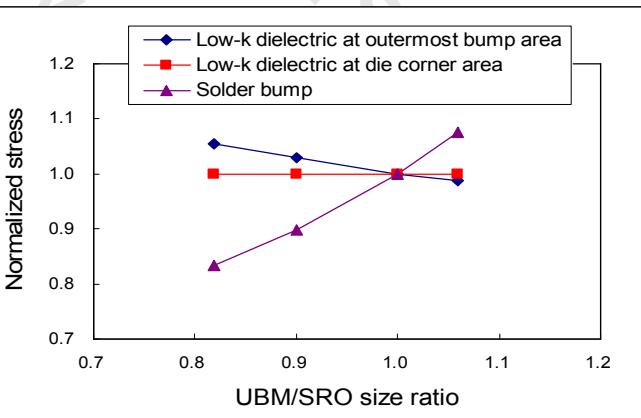


Fig. 5.3.3 Low-K/bump stress vs. UBM/SRO size ratio

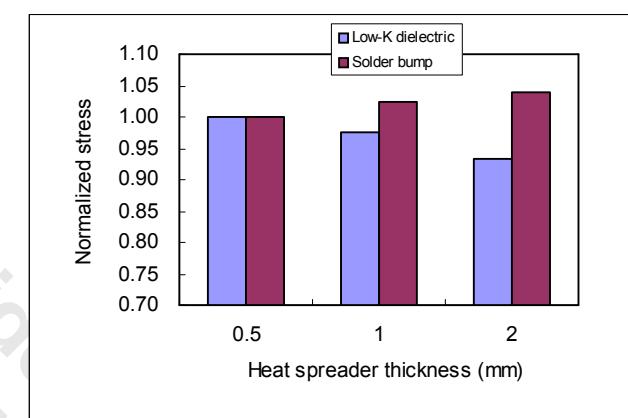


Fig. 5.3.4 Low-K/bump stress vs. heat spreader thickness

## ii. Thermal attributes and impact on thermal performance

- The effect of the die size on a given system thermal performance ( $R_{ja}$ ) and package thermal performance ( $R_{jc}$ ) is significant.
- The effect of heat spreader thickness on device thermal performance is shown below. A thickness heat spreader will improve the thermal performance. It is suggested when heat spreader thickness exceeds 0.5 mm, the thermal design is adequate.

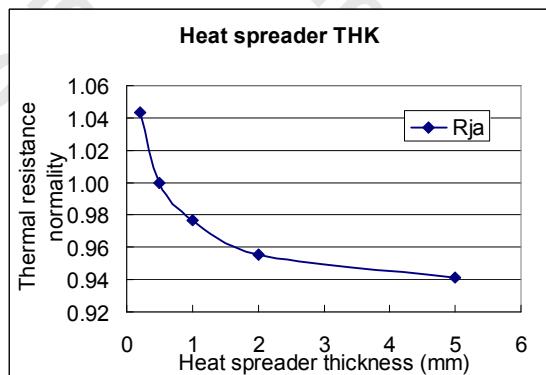
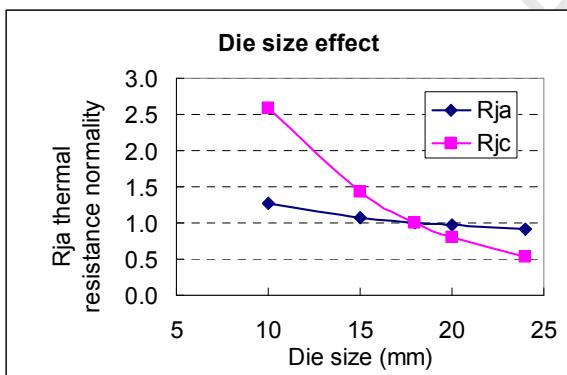


Fig. 5.3.5 Device thermal performances vs. die size and heat spreader thickness

For further information about the mechanical and thermal guidelines, please contact your account manager or Backend Marketing for assistance.

# 6 N85 Design Information

This chapter provides the following general layout information:

- 6.1 Overview
- 6.2 Non-shrinkable layout rules for logic
- 6.3 Design flow for tape-out

## 6.1 Overview

This document provides all the rules and reference information for the design and layout of integration circuits using TSMC 85 nm CMOS LOGIC/MS 1P9M (single poly, 9 metal layers), salicide, Cu technology.

- **CLN85 offers G/LP process.** – 94% shrinkage from CLN90 layout dimensions.
  - **CLN85G:** Provides CLN90G general purpose products with 94% linear shrinkage for the die area saving purpose. CLN85G offers dual-gate oxide process for 1.0V core and, 1.8V, 2.5V, or 3.3V I/O devices, and triple-gate oxide process for 1.0V core, 1.8V and 3.3V I/O device.
  - **CLN85LP:** Provides CLN90LP low power products with 94% linear shrinkage for the die area saving purpose. CLN85LP offers dual-gate oxide process for 1.2V core and, 2.5V or 3.3V I/O devices.
- **CMN85 offers G/LP with extra process steps for mixed-signal (MS) process. It includes metal-insulator-metal (MIM) capacitor in G/LP process and ultra thick metal (UTM; 34KA) for inductor in LP. Only mixed-signal (base band) SPICE model is supported, and no RF SPICE model is supported.** – 94% shrinkage from CMN90 layout dimensions.
  - **CMN85G for MS:** Provides CMN90G general purpose products with 94% linear shrinkage for the die area saving purpose. CMN85G offers dual-gate oxide process for 1.0V core and, 2.5V, or 3.3V I/O devices.
  - **CMN85LP for MS:** Provides CMN90LP low power products with 94% linear shrinkage for the die area saving purpose. CMN85LP offers dual-gate oxide process for 1.2V core and, 2.5V, or 3.3V I/O devices.
- **Customers must complete all GDS and DRC related efforts in N90 level,** i.e. follow N90 design rules and CLN85 non-shrinkable rules to tape out. TSMC will shrink the GDS to CLN85 while mask making.

### 6.1.1 General Logic Design Specifications

- **The drawn dimension in N85 tape-out need to follow N90 rules and the non-shrinkable rules of this document, then TSMC will have a 94% linear shrinkage during mask making.**
- **Designers must assess the shrinkage impact** on critical circuits, such as PLL, analog and IO circuits.
- **Seal ring and chip corner stress relief pattern (CSR) are shrinkable.** If you want to draw your own seal ring and CSR, you need to follow the N90 seal ring and CSR rules.

### 6.1.2 SRAM Design Specifications

- **N85 SRAM cells in different process:**

Process Type	N85G		N85LP		
	UHD	DP	UHD	SP	DP
SRAM <sup>†</sup>	UHD	DP	UHD	SP	DP
Cell Size (N90 drawn dimension)	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.15um <sup>2</sup>	1.99um <sup>2</sup>

<sup>†</sup> UHD: Ultra High Density; DP: Dual Port; SP: Single Port

## 6.2 Non-shrinkable Layout Rules

### 6.2.1 Pad Rule for Wire Bond

- All of design rules for wire bond are shrinkable. Please follow the related rules of the reference document.
- For design with a wire bond pad pitch below 53um (53um is before 94% shrink, and 50um is after 94% shrink), please consult your probe-card vendor in advance. Make sure that your probe-card vendor is able to provide such small pitch of wire bond pad.

### 6.2.2 Flip Chip Bump Rules

- The bumping rules for flip-chip design are critical on the bumping ball formation. Customers must meet the non-shrinkable rules before 94% linear shrink.
- The bump height and diameter would decrease due to UBM shrinking. Customers must evaluate this bump height change by themselves.

 \* **Warning:** For the design with a bump pitch 150~175um (after shrink), please consult with your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.

#### 6.2.2.1 Non-shrinkable Rules:

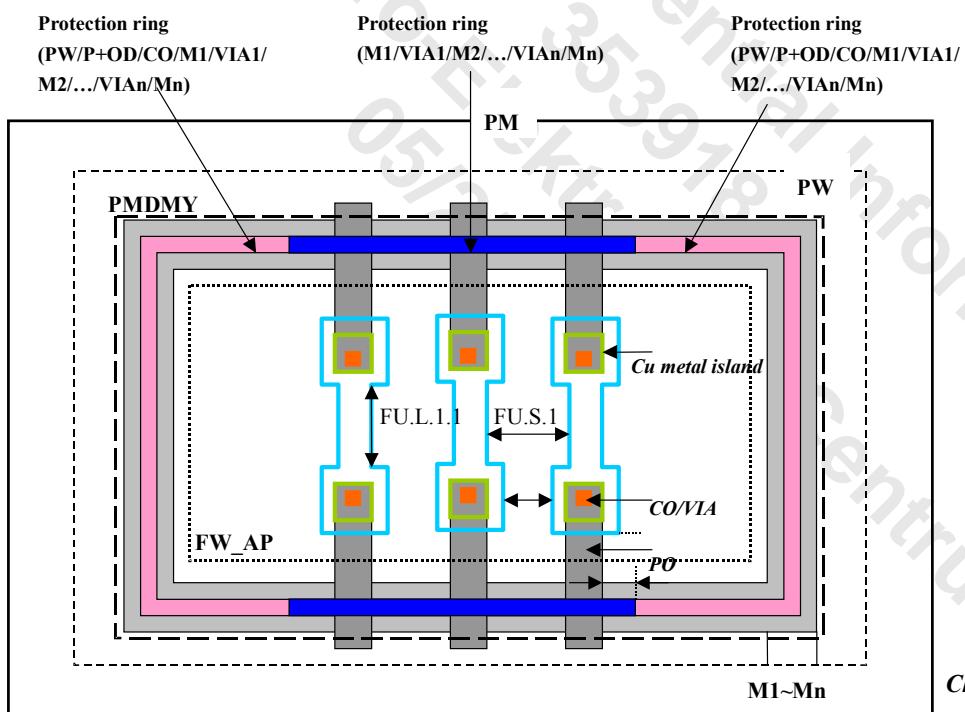
Rule No	Description		Rule	Rule
			Die size < 15mmx15mm	Die size ≥ 15mmx15mm
UBM.P.1	Pitch	≥	170	191
UBM.S.1	Space to metal fuse protection ring	≥	53.2	53.2
UBM.S.3	Space to L target	≥	85.1	85.1
UBM.EN.1	Enclosure by chip edge	≥	85	85
UBM.EN.2	Enclosure by AP	≥	2.1	2.1
BP.W.4	Width of CBD/CB2	≥	43 (without PM)	43 (without PM)
BP.W.6	Width of UBM	≥	85	85
BP.EN.5	CBD/CB2 enclosure by UBM Without AP RDL, CBD not interact UBM is not allowed (except sealring, FW_AP, L-target). With AP RDL, CB2 not interact UBM is not allowed (except sealring, FW_AP, L-target).	≥	10.6	10.6

## 6.2.3 AP Metal Fuse Rules

- Reference document: *T-000-CL-DR-005 TSMC AI FUSE (AP FUSE) DESIGN RULE FOR CU PROCESS*
- “Long-length AP fuse” can allow 94% shrinking.
- “Short-length AP fuse” is non-shrinkable. Please follow the rules in the following table.
- L-mark is non-shrinkable. Please follow the rules in the following table.

### 6.2.3.1 Non-shrinkable Rules:

Rule No.	Description	Rule
FUL.1.1	Length of AP fuse between dog bone ( <b>Short-length AP fuse only</b> )	≥ 6.36
FUS.1	Space of AP fuse ( <b>Short-length AP fuse only</b> )	≥ 4.03
LW.W.1	Minimum width of L-slot (11 µm is recommended)	≥ 10.6
	Maximum width of L-slot	≤ 21.2
LWL.1	Minimum length of L-slot (33 µm is recommended)	≥ 31.8
	Maximum length of L-slot	≤ 53
LW.EN.1	LMARK enclosure of L-slot [in the direction of the L-slot length]	≥ 12.72
LW.EN.2	LMARK enclosure of L-slot [perpendicular to the direction of the L-slot length]	≥ 31.8



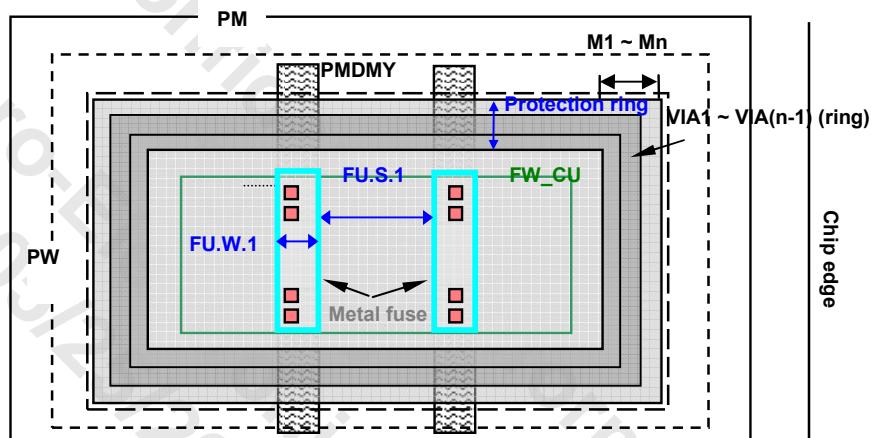
## 6.2.4 Top Metal Fuse Rules

- Reference document: *T-N90-LO-DR-003 TSMC 90 NM LOGIC TOP METAL FUSE DESIGN RULE*
- “Dog bone” fuse is not recommended. If you want to use this fuse structure, you need to do 106% size up on all dimensions in CLN90 fuse DRM (Doc. No.: *T-N90-LO-DR-003*).
- The following non-shrinkable rules are defined for “straight line” fuse only.

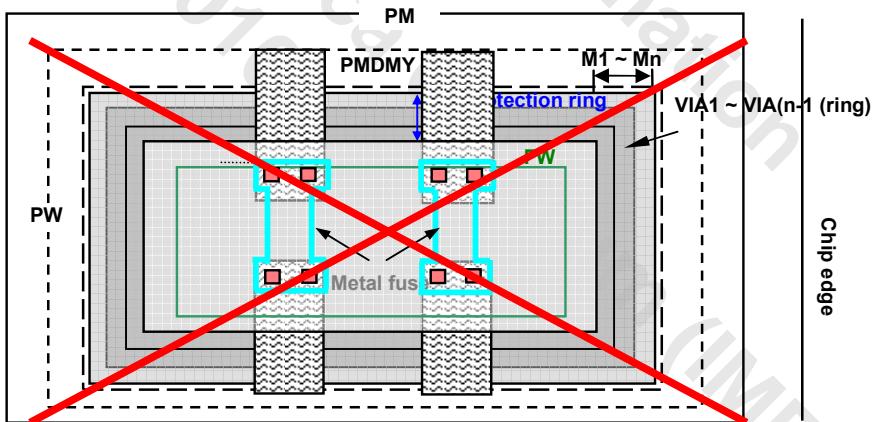
### 6.2.4.1 Non-shrinkable Rules: (For straight line fuse)

Rule No.	Description	Rule
FU.W.1	Width of metal fuse	= 0.85
FU.S.1	Space of metal fuse	$\geq$ 4.24
LW.W.1	Minimum width of L-mark (11 $\mu\text{m}$ is recommended)	$\geq$ 10.6
	Maximum width of L-mark	$\leq$ 21.2
LW.L.1	Minimum length of L-mark (33 $\mu\text{m}$ is recommended)	$\geq$ 31.8
	Maximum length of L-mark	$\leq$ 53
LW.EN.1	LMARK enclosure of L-mark [in the direction of the L-mark length]	$\geq$ 12.72
LW.EN.2	LMARK enclosure of L-mark [perpendicular to the direction of the L-mark length]	$\geq$ 31.8

“Straight line” fuse:  
(Recommended)



“Dog bone” fuse:  
(Not recommended)



## 6.3 Design Flow For Tape-Out

The N85 process is shrank from the N90 process, and the design rules are almost the same. Follow the four steps below, and it's easy to translate the existing N90 design to N85 process.

Use the correct tech files in N85.

Check the DRC violations with the non-shrinkable rules, and modify the layout if there is any violation.

Add ".option scale=0.94" in the spice simulation.

Add the scaling factor in RC extraction in LPE flow.

Most of the IP in N90 process can be used in N85 process without any modification, for example, the standard cell, the standard IO, and the SRAM certified in N85 process. The circuit performance in the chip should be close in N90 process and N85 process, except the ESD performance and the analog circuits. In the same standard IO library, the ESD performance in N85 process should be different from the ESD performance in N90 process due to the smaller discharge area. The analog circuit should be verified with the spice model card in N85 process to make sure the design margin is enough in N85 silicon.

It's recommended to perform the full-chip timing/leakage simulation and characterization to ensure the chip functionality and the robustness in N85 (with enough design margin)

This chapter contains the following topics:

- 6.3.1 N85 technology files and usage
- 6.3.2 Analog IP design
- 6.3.3 Legacy IP porting
- 6.3.4 Chip integration

## 6.3.1 N85 Technology files and usage

tsmc offers technology files for the digital and analog design. Please contact CE and FAE to get the latest version.

Categories	Tools	Input layout dimension	Output data dimension
Spice model			
DRC	Calibre	N90	N90
	Hercules	N90	N90
LVS/LPE	Calibre	N90	N90
	Hercules	N90	N90
RCX	Assura	N90	N90
	Star-RCXT	N90	N85
	Calibre-xRC	N90	N85
	Fire&Ice QX/QRC	N90	N85
DFM Enhancer utility	Assura RCX	N90	N85
	Dummy metal	N90	N90
	Dummy PO/OD	N90	N90
	Double VIA	N90	N90
PDK		N90	N90/N85

### 6.3.1.1 Spice model and simulation

Using the N85 spice model card in the spice simulation, the option “.option scale=0.94” must be added in the spice netlist to make the spice simulator to scale the device as the correct silicon size. Since the spice netlist in the half-node process is kept as the spice netlist in the full-node process, the scaling option is used to make the spice simulator to scale the device as the real silicon size in the half-node process. The spice model is customized for such approach, so that the user must not scale the spice netlist as the silicon dimension in the half-node process.

The following table shows the simulation behaviors when the spice simulator, Hspice and Spectre, reads the scaling option:

	Geometric parameters	W	L	PD	PS	AD	AS	SA	SB
MOS	0.94	0.94	0.94	0.94	0.8836	0.8836	0.94	0.94	
	NRS	NRD	SCA	SCB	SCC				
DIO	Electrical parameters	1	1	1	1	1			
	Geometric parameters	AREA							
BJT	No parameter	No impact because only fixed layout/models are provided							
Design Cap & Resistor	Geometric parameters	No impact because they are modeled as macro (sub-circuit). Scaling factor is set in SPICE model header.							
Parasitic R, C	Parasitic values	No impact because no geometric parameters							

Design input:

Pre-layout or post-layout spice netlist:

Pre-layout: N90 netlist

Post-layout: LPE netlist in N90 device dimension and N85 parasitic.

Insert the ".option scale=0.94" in the netlist.

Design output:

Meet timing or not?

Tsmc offering:

N85 Spice model

### 6.3.1.2 DRC

There are few non-shrinkable rules in the half-node process, so that the design must be verified with the correct DRC deck in the half-node process. The layout is drawn in the full-node process environment, and the DRC tool will verify the layout with the half-node design rules in the half-node DRC deck. The DRC reports shows the DRC violations, if any, in the full-node environment, too.

Design input: Layout (GDSII) in N90 dimension

Design output: DRC violation or not?

Tsmc offering:

N85 DRC deck with the shrinkable and non-shrinkable rules

Antenna and package rules including the wire-bond pad and flip-flop RDL

### 6.3.1.3 Dummy Insertion

The dummy PO/OD/Metal rules in N85 are equivalent to the dummy PO/OD/Metal rules in N90, so that the dummy insertion utilities in N90 can be used in N85 design directly.

Design input: Layout (GDSII) in N90 dimension

Design output: Final layout with dummy PO, OD, Metal insertion in N90 dimension

tsmc offering:

N90 DM/DPO/DOD insertion utility

N90 DFM enhancer

### 6.3.1.4 LVS/LPE

Use the LVS deck for the half-node process to verify the layout in the full-node dimension and the spice netlist in the full-node dimension. For the LPE extraction, use the LVS/LPE combo deck to extract the layout as the database for the RC extraction tool. The NRS/NRD for the device is different in the full-node process and in the half-node process, so that the resistance table in the half-node LVS/LPE combo deck is different from the LVS/LPE combo deck in the full-node process.

Design input:

Layout (GDSII) in N90 dimension

Spice netlist in N90 dimension

Design output:

LVS matched or not?

LPE database for the RC extraction

tsmc offerings:

N85 LVS/LPE combo deck

### 6.3.1.5 RCX

The scaling in the device is modeled in the spice simulation with the scaling option, and the scaling in the metal/VIA is handled in the RC extraction. One scaling option must be specified in the RC extraction script to scale the metal/VIA of the design in the RC extractor, and one option must be specified in the RC extraction script to prevent the devices be scaled. Only metal/VIA is scaled in the RC extraction, and the devices are scaled in the spice simulation.

Design input:

Layout (GDSII) in N90 dimension

LPE database in N90 dimension

Design output:

Parasitic R/C in N85

LPE spice netlist with N90 device dimension and N85 parasitic

tsmc offerings:

N85 RC extraction technology files

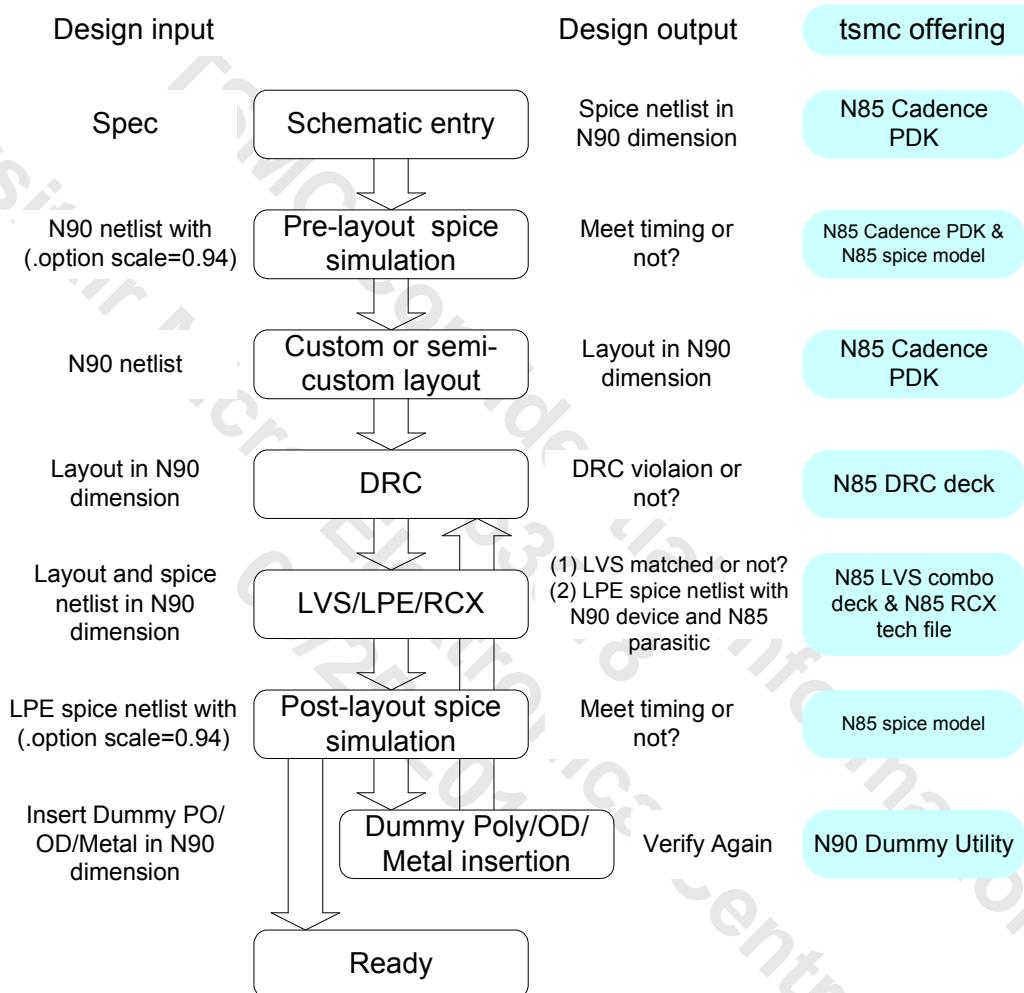
User's setting:

LVS Tools	Hercules	Calibre	Assura LVS
RCX Tools	Star-RCXT	Calibre-xRC	Assura RCX
Interconnect scaling	(In Star-RCXT command file) <b>magnification_factor: 0.94</b> <b>magnify_device_params: NO</b> (For cross-reference in output netlist) <b>XREF: YES</b>	(In Calibre-xRC run script) <b>setenv PEX_FMT_NO_MAGNIFY ON</b>  (In xRC rule file) <b>PEX MAGNIFY 0.94</b>	<b>capgen -c -scale 0.94</b> To generate a N85 deck

## 6.3.2 Analog IP design

The design flow is almost the same as the design flow in the full node process. Just add the “.option scale=0.94” in the spice netlist for the spice simulation, and use the correct tech files in the design. The details, such as Spice simulation, DRC, LVS, and RCX, can be referred to details in the previous section.

Here is the basic flow for N85 process, and it can be used in applying 94% shrinkage from an existing N90 design or developing a new N85 design.



Once the IP is verified in the post-layout spice simulation with the correct tech files and the correct usage, the IP can be put in the test chip and verified in the N85 shuttle.

There is one notice about N85 design:

N90 SRAM bit cell can be directly shrunk to N85. Designers need to assess 6% shrink impact on SRAM macro performance. For self-owned SRAM cell, please contact TSMC to perform a mandatory bit cell review.

### 6.3.3 Legacy IP porting

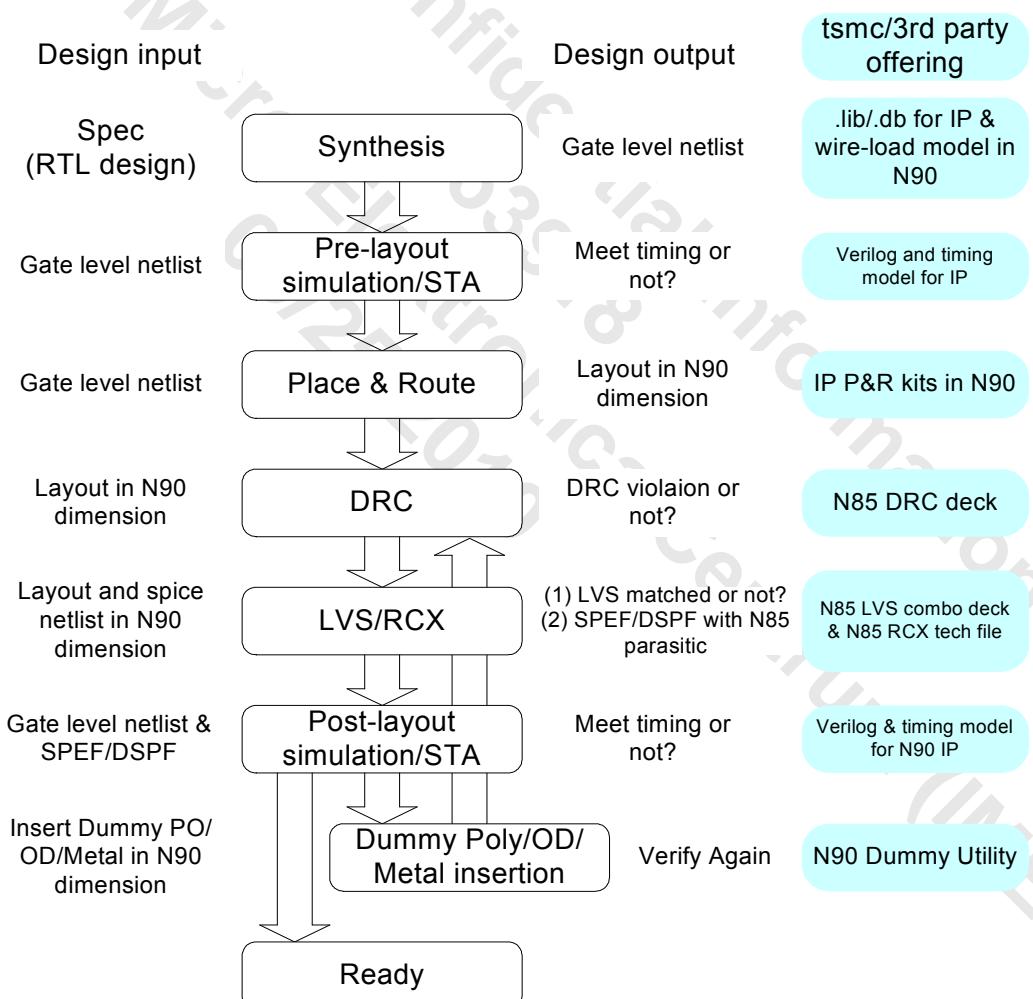
For most of the IP design, the circuits can be shrunk directly. If there is no DRC violation related to the non-shrinkable rules, the IP can be shrunk; if there are DRC violations related to the non-shrinkable rules, the layout of such IP should be modified to avoid the DRC violations. The IP should be simulated with the spice model in the half-node process, so that the timing can be analyzed before the tapeout.

### 6.3.4 Chip integration

#### 6.3.4.1 Introduction

The design flow is almost the same as the design flow in the full node process. If the design kits are ready for the half-node process, such as the .lib or .db, use these half-node design kits in the design; if the design kits are not ready for the half-node process, such as the .lib or .db, use the design kits in the full-node process with additional margins.

Here is the basic flow for N85 process. It can be used in applying 94% shrinkage from an existing N90 design or developing a new N85 design. There is no timing design kit for N85 process, so that the design kits in N90 is used in the static timing analysis and the post-layout verilog simulation.



### 6.3.4.2 Synthesis

If there are design kits for the half-node process, such as .lib or .db, use these design kits in the synthesis to compile the RTL code and the timing constraints into the gate level netlist; if there is no design kit for the half-node process, such as .lib or .db, use the design kits in the full-node process in the synthesis to compile the RTL code and the timing constraints, with additional reasonable timing margins, into the gate level netlist.

Design input: RTL and timing constraint

Design output: Gate level netlist

Current environment:

N90 standard IO library

N90 3<sup>rd</sup> party IP & Library, such as standard cell, SRAM

N90 wire load model for interconnect RC estimation

Reasonable timing margin

### 6.3.4.3 Simulation/STA

If there are design kits for the half-node process, such as .lib or .db, use these design kits in the STA and the verilog simulation; if there is no design kit for the half-node process, such as .lib or .db, use the design kits in the full-node process in the STA and the verilog simulation with additional timing margins.

Design input:

For pre layout simulation/STA: Gate level netlist

For post layout simulation/STA: Gate level netlist or SPEF or DSPF with N85 parasitic

Design output:

Meet timing or not?

Pass simulation/STA or not?

Current environment:

N90 timing kits in IP and Library

Reasonable timing margin

### 6.3.4.4 Place and Route

If there are physical design kits in the half-node process, such as the lef or the Milkyway FRAM view, use these design kits in the place/route. If there is no physical design kit in the half-node process, such as the lef or the Milkyway FRAM view, using the physical design kits in the full-node process is fine since the layout dimension is the same in the full-node process and in the half-node process. Additional timing margins are necessary when using the physical design kits in the full-node process.

Design input: Gate level netlist and floorplan in N90 dimension

Design output: Layout in N90 dimension

Current environment:

N90 P&R kit

LEF or Milkyway FRAM in N90 dimension

Electrical/timing model in N90 dimension

P&R tech file and RCX files for implementation

Reasonable timing margin is necessary

### 6.3.4.5 Dummy Insertion

The dummy PO/OD/Metal rules in N85 are equivalent to the dummy PO/OD/Metal rules in N90, so that the dummy insertion utilities in N90 can be used in N85 design directly.

Design input: Layout (GDSII) in N90 dimension

Design output: Final layout with dummy PO, OD, Metal insertion in N90 dimension

Tsmc offering:

N90 DM/DPO/DOD insertion utility

N90 DFM enhancer

### 6.3.4.6 DRC

The DRC deck in the half-node process is used to verify the layout in the half-node process, so is the Antenna deck/bond pad deck in the half-node process.

Design input: Layout (GDSII) in N90 dimension

Design output: DRC violation or not?

Tsmc offering:

N85 DRC deck

Antenna and package rules including the wire-bond pad and flip-flop RDL

### 6.3.4.7 LVS/RCX

The LVS deck in the half-node process is used to verify the layout vs the schematic. For the RC extraction, use the RC tech file in the half-node process to get the RC in the half-node process.

Design input:

Layout (GDSII, DEF, and Milkyway) in N90 dimension

Spice netlist in N90 dimension

Design output:

LVS matched or not?

SPEF or DSPF gate level netlist with N85 parasitic

tsmc offering:

N85 LVS deck

N85 RCX technology file for sign-off

The configurations can be referred to section 1.2.4.

### 6.3.4.8 IR/EM Analysis

If there are design kits for the half-node process, such as .lib or .db, use these design kits in the power calculation, and use the RC tech file in the half-node process to analyze the IR/EM behavior in the design; if there is no design kit for the half-node process, such as .lib or .db, use the design kits in the full-node process to calculate the power consumption, and use the RC tech file in the full-node process to analyze the IR/EM behavior in the design with the tighten signoff criteria.

Design input: P&R layout database (DEF or Milkyway) in N90 dimension

Design output:

Chip power analysis in N90 dimension

Chip IR/EM analysis result in N90 dimension

Current environment:

N90 library kits with N90 timing, power views

N85 EM rules

Reasonable IR drop margin

### 6.3.4.9 Package

Since the minimum pad or bump pitch of the assembly house is usually described in the silicon dimension, the LVS pin coordinates in the half-node process has to be scaled as 94% to derive the package pin locations for the assembly house.

Design input: Chip LVS I/O pin location file in N90 drawn dimension

Design output: Package pin location file in N85 silicon dimension

tsmc offering: Pad, bump, and RDL design rules

Customer's setting:

Notice that minimum pad or bump pitch of assembly house is usually described in silicon dimension.

Scale chip LVS pin text coordinates by 0.94 in spreadsheet to derive package pin locations for assembly house.

# 7 N80 Design Information

This chapter provides the following general layout information:

- 7.1 Overview
- 7.2 Non-shrinkable layout rules for logic
- 7.3 Core decoupling capacitor (OD\_DECAP) layout rules (for CLN80HS only) (Mask ID: 135)
- 7.4 Non-shrinkable layout rules for CTM (Mask ID: 182) and CBM (Mask ID: 183) of MIM
- 7.5 Design flow for tape-out

## 7.1 Overview

This chapter provides all the rules and reference information for the design and layout of integration circuits using TSMC 80 nm CMOS LOGIC 1P9M (single poly, 9 metal layers), salicide, Cu technology.

- **CLN80 offers GC/GT/HS/LP process** – 90% shrinkage from CLN90 layout dimensions.
    - **CLN80GC**: provides CLN90G products with 90% shrinkage for die area saving purpose. CLN80GC offers dual-gate oxide process for 1.0V core and, 2.5V or 3.3V I/O devices.
    - **CLN80GT**: provides CLN90GT products with 90% shrinkage for die area saving purpose. CLN80GT offers dual-gate oxide process for 1.2V core and, 1.8V or 2.5V I/O devices.
    - **CLN80HS**: provides CLN90GT product with 90% shrinkage for high-speed performance requirement by aggressive device design. CLN80HS offers dual gate oxide processes for 1.05V core and, 1.8V or 2.5V I/O devices.
    - **CLN80LP**: provides CLN90LP products with 90% shrinkage for die area saving purpose. CLN80LP offers dual-gate oxide process for 1.2V core and 2.5V I/O devices.
  - **CMN80 offers GC with extra process steps for mixed-signal (MS) process. It includes metal-insulator-metal (MIM) capacitor** – 90% shrinkage from CMN90 layout dimensions.
    - **CMN80GC for MS**: Provides CMN90G products with 90% shrinkage for die area saving purpose. CMN80GC offers dual-gate oxide process for 1.0V core and, 2.5V or 3.3V I/O devices.
  - **TSMC offers one kind of inter-layer metal (Mx) and two kinds of top-layer metal (Mn/ My)**:
    - Mx: Inter-layer Metal, W/S=0.14μm/0.14μm.
    - Mn (3XTM): top metal pitch is four times of Mx pitch (W/S=0.42μm/0.42μm).
    - My (2XTM): top metal pitch is two times of Mx pitch (W/S=0.28μm/0.28μm).
  - **TSMC N80 generation does not support UTM inductor devices**.
  - **You must complete all GDS and DRC related efforts in N90 level**, i.e. follow N90 design rules and N80 non-shrinkable rules to tape out. TSMC will shrink the GDS to N80 while mask making.
  - **Native device relative rules are non-shrinkable** – Native device of 1.0V, 1.05V, 1.2V, 1.8V 2.5V or 3.3V must be sized up 110%<sup>a</sup>.
- <sup>a</sup> sized up 110%: Use a size-up factor of 1.10x, together with grid-size of 5 nm, to minimize the risk of data truncation or grid snapping.
- **Low-Vt device is not allowed on CLN80GT/ LP**.
  - **Capacitor and Varactor for CLN80HS**:
    - A second choice is provided for the Core(1.05V) MOS capacitor by using OD\_DECAP (mask ID: 135, CAD layer:118) for low leakage performance requirement. Please refer to section 3.3: OD\_DECAP rules.
    - Core decoupling capacitor device (OD\_DECAP) is not allowed to use for the transistor purpose.
    - Varactor outside OD2 in CLN80HS is not allowed due to no SPICE model.

## 7.1.1 General Design Specifications

- The drawn dimension in N80 tape-out needs to follow N90 rules and the non-shrinkable rules of this chapter, then TSMC will have a 90% linear shrinkage during mask making.
- Designers must assess the shrinkage impact on critical circuits, such as PLL, analog and IO circuits.
- Seal ring and chip corner stress relief pattern (CSR) are shrinkable. If you want to draw your own seal ring and CSR, you need to follow the N90 seal ring and CSR rules in chapter 4.
- Designers may consider a direct 110% size-up at the N90 level to maintain the circuit performance (for example: matching circuits, current-driving at IO circuits).
- Dummy OD/PO/Mx (DOD/DPO/DMx) patterns and rules are shrinkable.
  - DOD / DPO / DMx are must for the N80 process.
  - You can keep the original N90 dummy patterns, as long as the DOD/DPO/DMx rules can be met after re-tuning the real circuits.
  - You must re-fill the dummy patterns, if the DOD/DPO/DMx rules could not be met after re-tuning the real circuits.
  - It is recommended to use TSMC auto-fill utilities. (DOD and DPO utility no.: T-N80-CL-DR-001-C2; DMx utility no.; T-N90-LO-DR-001-C3)
- Designers may consider a direct 110% size-up at the N90 level to maintain the circuit performance (for example: matching circuits, current-driving at I/O circuits) in N80 technology.
- It's recommended to use 1 nm design grid on 110% size-up IP layout to minimize the device layout mismatch due to data truncation or grid snapping. It may occur 5nm layout mismatch when snapping the design grid to 5nm on 110% size-up circuit. You should pay attention on the performance impact on the size-up circuits, especially on OD and PO layout. Please refer to the "110% Size-up" section 7.5.3 for details. You could also consult with the TSMC Design Support Department about the size-up procedure.
- For newly developed IP, a compatible design for N90 and N80 is recommended. Please consider the following guidelines besides non-shrinkable rules
  - 10nm design grid for critical device layout for both device parameters and device coordinates. Thus, avoid the device mismatch caused by grid snapping (no matter for 110% size-up or direct shrink flow).
  - Avoid using 45° lines. If 45° shape is necessary, use 10nm grid for both endpoints of 45° lines. Thus, avoid skewed lines no matter for size-up or direct shrink flow.
  - Add dummy blockage for DM/DPO/DOD on critical timing area. Thus, for size-up flow, it will help for designer to rip-up N90 dummy and re-insert N80 dummy by TSMC utility.

## 7.1.2 SRAM Design Specifications

- You can prepare SRAM by
  1. Consult with 3<sup>rd</sup> party vendors; or
  2. Use TSMC's silicon proven SRAM bit cellsto build the configuration; or
  3. Use self-own SRAM cell. Please contact TSMC to perform a mandatory bit cell review.
- The following SRAM cells are silicon proven in TSMC.

Process Type	N80GC		N80GT		N80HS		N80LP
SRAM <sup>†</sup>	UHD	DP	UHD	DP	UHD	DP	SP
Cell Size (N90 drawn dimension)	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	0.999um <sup>2</sup>	1.99um <sup>2</sup>	1.15um <sup>2</sup>

- Five special layers are critical to SRAM usage in the N80 process.
  - Mask making purpose.
    1. Layer "SRM" (CAD layer 50) is necessary for cell implant mask generation.
    2. Layer "DPSRM" (CAD layer 74;0) of dual port SRAM cell is essential for mask making purpose.
    3. Layer "SRAMDMY\_PE" (CAD layer 186;1) is required for LVS and mask making purpose. It will define the pass-gate transistors.
  - DRC purpose
    4. Layer "SRAMDMY" (CAD layer 186;0) is needed for DRC purpose only. It will define the SRAM regions (including only SRAM cells/arrays).
    5. Layer "SRAMDMY" (CAD layer 186;4) is required for DRC purpose only. It will define the word decoder of TSMC SRAM (0.999um<sup>2</sup> and 1.15um<sup>2</sup>). This layer is only to waive CO.S.3 and G.1.
- Please follow SRAM rules and recommendations in the chapter 4.

## 7.2 Non-shrinkable Layout Rules for Logic

### 7.2.1 Purpose:

A set of non-shrinkable rules are defined to meet the below requirements:

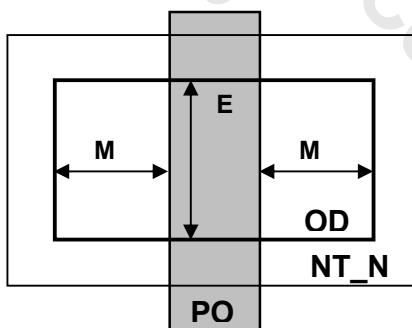
1. The limitation of the silicon process step, testing probing, laser repair and assembly.
2. Prevent DRC false errors from 110% size up steps.
3. Except the non-shrinkable rules in the following section, other rules (please refer to chapter 4) are shrinkable.

#### 7.2.1.1 Non-shrinkable Rules

In the following table, the “x” in  $M_x$ , refer to 2,3,4,5,6 and 7; the “n” in  $M_n$ , refer to 8 and 9.

Rule No	Description		Rule
DNW.S.1	DNW space to DNW	$\geq$	5.28
DNW.S.2	DNW space to NW	$\geq$	3.63
NT_N.W.2	Channel length of core native device (CLN80GT)	$\geq$	0.22
NT_N.W.2.2	Channel length of core native device (CLN80HS/GC)	$\geq$	0.50
NT_N.W.2.3	Channel length of core native device [CLN80HS with limited E and M] [( $0.5 < E \leq 1.0 \mu m$ , $M \leq 0.79 \mu m$ ) OR ( $E=0.5$ )]	$\geq$	0.30
NT_N.W.3	Channel length of 2.5V or 3.3V native device	$\geq$	1.32
NT_N.W.4	Channel length of 1.8V native device	$\geq$	0.88
NT_N.S.2	NT_N space to [ACTIVE outside NT_N]	$\geq$	0.415
NT_N.S.3	NT_N space to NW	$\geq$	1.32
NT_N.EN.1	NT_N enclosure of N+OD (maximum = minimum)	$=$	0.285
NT_N.EX.1	PO extension on {OD inside NT_N} (PO endcap)	$\geq$	0.385
OD.A.2	OD enclosed area	$\geq$	0.102
PO.W.2	Channel length of 2.5V MOS	$\geq$	0.31
PO.W.3	Channel length of 3.3V MOS	$\geq$	0.415
PO.W.4	Channel length of 1.8 V MOS	$\geq$	0.22
VAR.R.6	VAR outside OD2 is not allowed (CLN80HS)		

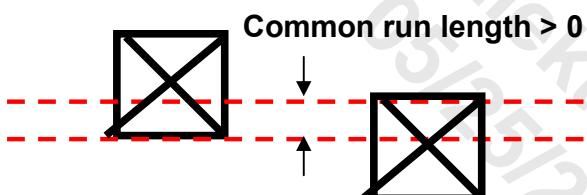
#### Illustration of NT\_N.W.2.3:



### 7.2.1.2 Recommended Non-shrinkable Rule

Rule No	Description		Rule
OD.W.4®	Width of 45 degree bent OD	≥	0.195
OD.S.4®	OD space to 45 degree OD	≥	0.195
PO.W.5®	Width of 45-degree FIELD PO	≥	0.205
PO.S.8®	PO space to 45-degree FIELD PO	≥	0.205
PO.EX.1®	PO extension on OD (end-cap)	≥	0.175
CO.S.3®	{CO inside OD} space to GATE (Overlap of GATE is not allowed) [space can be ≥ 0.058 µm inside SRAM word line decoder covered by layer 186;4]	≥	0.075
M1.W.2®	Width of 45-degree bent M1	≥	0.205
M1.S.5®	M1 space to 45-degree bent M1	≥	0.205
VIAx.S.3®	Two adjacent VIAx space between different net if the common run length > 0 µm	≥	0.17
Mx.W.2®	Width of 45-degree bent Mx	≥	0.205
Mx.S.5®	Mx space to 45-degree bent Mx	≥	0.205

#### Illustration of VIAx.S.3®



### 7.2.1.3 Stress Migration and Wide Metal Spacing Rules Adjustment

- The rules listing in the below table are adjusted to avoid DRC false alarm on 110% size-up circuits.
- Except 110% size-up circuits, other circuits have to follow the stress migration and wide metal spacing rules in chapter 4. However, the following rules will be met automatically as long as rules in Chapter 4 are met.

Rule No	Description		Rule
M1.S.2	Space [at least one M1 line width > <b>0.33μm(W1)</b> and the parallel M1 run length > <b>0.575μm(L1)</b> ]	≥	0.17
M1.S.2.1	Space [at least one M1 line width > <b>0.3μm(W1)</b> and the parallel M1 run length > <b>0.8μm(L1)</b> ]	≥	0.130
M1.S.3	Space [at least one M1 line width > <b>1.65μm(W2)</b> and the parallel M1 run length > <b>1.65μm(L2)</b> ]	≥	0.5
M1.S.4	Space [at least one M1 line width > <b>4.95μm(W3)</b> and the parallel M1 run length > <b>4.95μm(L3)</b> ]	≥	1.5
VIAx.R.2	At least two VIAx with space ≤ <b>0.32μm(S1)</b> , or at least four VIAx with space ≤ <b>0.63μm(S1')</b> , or at least nine VIAx with space < <b>0.85μm(S1'')</b> are required to connect M <sub>x</sub> and M <sub>x+1</sub> when one of these two metals has width and length (W1) > <b>0.47μm</b> .		
VIAx.R.3	At least four VIAx with space ≤ <b>0.32μm(S2)</b> , or at least nine VIAx with space ≤ <b>0.85μm(S2')</b> are required to connect M <sub>x</sub> and M <sub>x+1</sub> when one of these two metals has width and length (W2) > <b>1.26μm</b> .		
VIAx.R.4	At least two VIAx must be used for a connection that is ≤ <b>1.0μm(D)</b> away from a metal plate (either M <sub>x</sub> or M <sub>x+1</sub> ) with length > <b>0.77μm(L)</b> and width > <b>0.77μm(W)</b> . (It is allowed to use one VIAx for a connection that is > <b>1.0μm (D)</b> away from a metal plate (either M <sub>x</sub> or M <sub>x+1</sub> ) with length > <b>0.77μm(L)</b> and width > <b>0.77μm(W)</b> .)		
VIAx.R.5	At least two VIAx must be used for a connection that is ≤ <b>2.0μm(D)</b> away from a metal plate (either M <sub>x</sub> or M <sub>x+1</sub> ) with length > <b>2.2μm(L)</b> and width > <b>2.2μm(W)</b> . (It is allowed to use one VIAx for a connection that is > <b>2.0μm(D)</b> away from a metal plate (either M <sub>x</sub> or M <sub>x+1</sub> ) with length > <b>2.2μm(L)</b> and width > <b>2.2μm(W)</b> .)		
VIAx.R.6	At least two VIAx must be used for a connection that is ≤ <b>5.0μm(D)</b> away from a metal plate (either M <sub>x</sub> or M <sub>x+1</sub> ) with length > <b>11μm(L)</b> and width > <b>3.3μm(W)</b> . (It is allowed to use one VIAx for a connection that is > <b>5.0μm(D)</b> away from a metal plate (either M <sub>x</sub> or M <sub>x+1</sub> ) with length > <b>11μm(L)</b> and width > <b>3.3μm(W)</b> ).		
Mx.S.2	Space [at least one M <sub>x</sub> line width > <b>0.24μm(W1)</b> and the parallel M <sub>x</sub> run length > <b>0.575μm(L1)</b> ]	≥	0.19
Mx.S.2.1	Space [at least one M <sub>x</sub> line width > <b>0.21μm(W1)</b> and the parallel M <sub>x</sub> run length > <b>0.8μm(L1)</b> ]	≥	0.150
Mx.S.3	Space [at least one M <sub>x</sub> line width > <b>1.65μm(W2)</b> and the parallel M <sub>x</sub> run length > <b>1.65μm(L2)</b> ]	≥	0.50
Mx.S.4	Space [at least one M <sub>x</sub> line width > <b>4.95μm(W3)</b> and the parallel M <sub>x</sub> run length > <b>4.95μm(L3)</b> ]	≥	1.50
VIAN.R.2	At least two VIA <sub>n</sub> with spacing ≤ <b>1.87μm</b> are required to connect M <sub>n</sub> and M <sub>n+1</sub> when one of these metals has a width and length > <b>1.98μm</b> .		
VIAN.R.3	At least two VIA <sub>n</sub> must be used for a connection that is ≤ <b>5.0μm(D)</b> away		

Rule No	Description		Rule
	from a metal plate (either Mn or Mn+1) with length > <b>11µm(L)</b> and width > <b>3.3µm(W)</b> . (It is allowed to use one VIA <sub>n</sub> for a connection that is > <b>5.0µm(D)</b> away from a metal plate (either Mn or Mn+1) with length > <b>11µm(L)</b> and width > <b>3.3µm(W)</b> ).		
Mn.S.2	Space [at least one Mn line width > <b>1.65µm(W1)</b> and the parallel Mn run length > <b>1.65µm(L1)</b> ]	≥	0.50
Mn.S.3	Space [at least one Mn line width > <b>4.95µm(W2)</b> and the parallel Mn run length > <b>4.95µm(L2)</b> ]	≥	1.50
My.S.3	Space [at least one metal line width > <b>1.65µm (W2)</b> and the parallel metal run length > <b>1.65µm (L2)</b> ]		0.50
My.S.4	Space [at least one metal line width > <b>4.95µm (W3)</b> and the parallel metal run length > <b>4.95µm (L3)</b> ]		1.50
VIAy.R.2	At least two VIA <sub>y</sub> with space ≤ <b>0.64µm</b> (S1), or at least four VIA <sub>y</sub> with space ≤ <b>1.26µm</b> (S1') are required to connect My and My+1 when one of these two metals has width and length (W1) > <b>0.93µm</b> .		
VIAy.R.3	At least four VIA <sub>y</sub> with space ≤ <b>0.64µm</b> (S2), or at least nine VIA <sub>y</sub> with space ≤ <b>1.7µm</b> (S2') are required to connect My and My+1 when one of these two metals has width and length (W2) > <b>2.16µm</b> .		
VIAy.R.4	At least two VIA <sub>y</sub> must be used for a connection that is ≤ <b>1µm</b> (D) away from a metal plate (either My or My+1) with length > <b>0.77µm</b> (L) and width > <b>0.77µm</b> (W). (It is allowed to use one VIA <sub>y</sub> for a connection that is > <b>1µm</b> (D) away from a metal plate (either My or My+1) with length > <b>0.77µm</b> (L) and width > <b>0.77µm</b> (W).)		
VIAy.R.5	At least two VIA <sub>y</sub> must be used for a connection that is ≤ <b>2µm</b> (D) away from a metal plate (either My or My+1) with length > <b>2.2µm</b> (L) and width > <b>2.2µm</b> (W). (It is allowed to use one VIA <sub>y</sub> for a connection that is > <b>2µm</b> (D) away from a metal plate (either My or My+1) with length > <b>2.2µm</b> (L) and width > <b>2.2µm</b> (W).)		
VIAy.R.6	At least two VIA <sub>y</sub> must be used for a connection that is ≤ <b>5µm</b> (D) away from a metal plate (either My or My+1) with length > <b>11µm</b> (L) and width > <b>3.3µm</b> (W). (It is allowed to use one VIA <sub>y</sub> for a connection that is > <b>5µm</b> (D) away from a metal plate (either My or My+1) with length > <b>11µm</b> (L) and width > <b>3.3µm</b> (W)).		

## 7.2.2 Pad Rule for Wire Bond

- Please refer to the wire bond, flip chip and interconnection design rules in chapter 5, except the rules listing in the following table.
- Since the pad rule is limited by testing and assembly capability, you has to check the layout dimension before 90% linear shrink.
- Single in-line and Staggered pad rule is non-shrinkable. The design rules Tri-tiers pad structure are shrinkable.

### 7.2.2.1 Non-shrinkable Rules:

Rule No	Description	Rule		
		Pitch $\geq 50\mu\text{m}^{\ddagger}$ Single in-line	Pitch $\geq 55\mu\text{m}^{\ddagger}$ Single in-line	Pitch $\geq 60\mu\text{m}$ Stagger
#CB.W.1	Width	$\geq$ 48.4	53	58
#CB.W.2	Length of (the edge perpendicular to nearby chip edge)	$\geq$ 88	66 <sup>†</sup>	66 <sup>†</sup>
#CB.S.1	Space	$\geq$ 6.6	6.6	7.7
#CB.P.1 <sup>u</sup>	Pitch of (4 pitches at each chip corner)	$\geq$ 88	88	110

• **Table notes:**<sup>†</sup> These rules are shrinkable.

• <sup>‡</sup>The pitch is real pad pitch after 90% shrinkage.

## 7.2.3 Flip Chip Bump Rules

- Please refer to the wire bond, flip chip and interconnection design rules in chapter 5, except the rules listing in the following table.
- The bumping rules for flip-chip design are critical on the bumping ball formation. You must meet the non-shrinkable rules before 90% linear shrink.
- The bump height and diameter would decrease due to UBM shrinking. You must evaluate this bump height change carefully.



\* **Warning:** For the design with a bump pitch 150~175um (after shrink), please consult with your assembly house in advance. Make sure that your assembly house is able to provide such substrates and the associated service for your smaller bump pitch design.

### 7.2.3.1 Non-shrinkable Rules:

Rule No	Description		Rule
UBM.P.1	Pitch	≥	165
UBM.S.1	Space to metal fuse protection ring	≥	55
UBM.S.3	Space to L target	≥	88
UBM.EN.1	Enclosure by chip edge	≥	88
UBM.EN.2	Enclosure by AP	≥	2.2
BP.W.4	Width of CBD/CB2	≥	44 (without PM) 55 (with PM)
BP.W.5	Width of PM under UBM area.	≥	33
BP.W.6	Width of UBM	≥	88
BP.EN.5	CBD/CB2 enclosure by UBM Without AP RDL, CBD not interact UBM is not allowed (except sealring, FW_AP, L-target). With AP RDL, CB2 not interact UBM is not allowed (except sealring, FW_AP, L-target).	≥	11.0

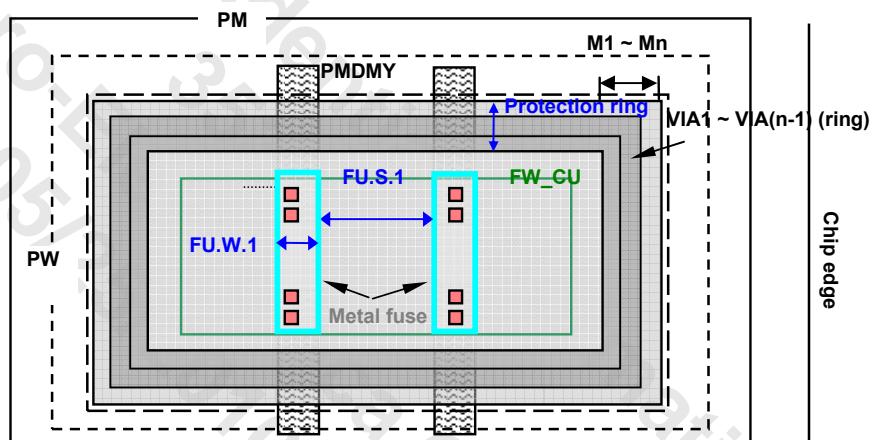
## 7.2.4 Top Metal Fuse Rules

- Reference document: *T-N90-LO-DR-003 TSMC 90 NM LOGIC TOP METAL FUSE DESIGN RULE*
- “Dog bone” fuse is not recommended. If you want to use this fuse structure, you need to do 110% size up on all dimensions in CLN90 fuse DRM (Doc. No.: *T-N90-LO-DR-003*).
- The following non-shrinkable rules are defined for “straight line” fuse only.

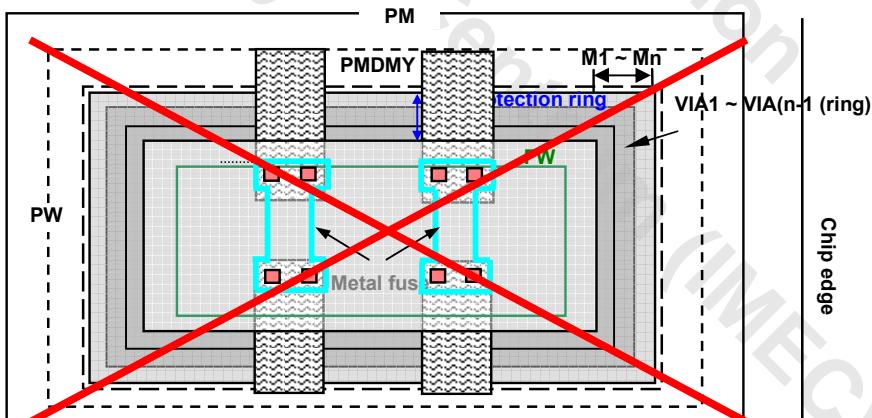
### 7.2.4.1 Non-shrinkable Rules: (For straight line fuse)

Rule No.	Description	Rule
FU.W.1	Width of metal fuse	= 0.88
FU.S.1	Space of metal fuse	$\wedge$ 4.4
LW.W.1	Minimum width of L-mark (11 $\mu\text{m}$ is recommended)	$\wedge$ 11
	Maximum width of L-mark	$\vee$ 22
LW.L.1	Minimum length of L-mark (33 $\mu\text{m}$ is recommended)	$\wedge$ 33
	Maximum length of L-mark	$\vee$ 55
LW.EN.1	LMARK enclosure of L-mark [in the direction of the L-mark length]	$\wedge$ 13.2
LW.EN.2	LMARK enclosure of L-mark [perpendicular to the direction of the L-mark length]	$\wedge$ 33

“Straight line” fuse:  
(Recommended)



“Dog bone” fuse:  
(Not recommended)

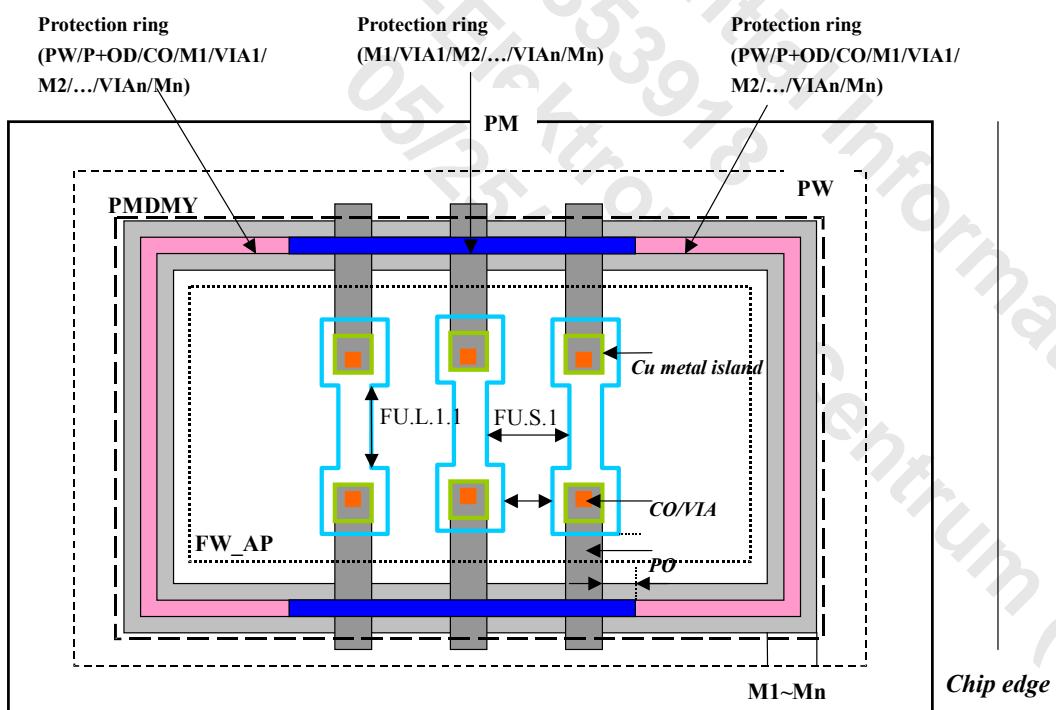


## 7.2.5 AP Metal Fuse Rules

- Reference document: *T-000-CL-DR-005 TSMC AI FUSE (AP FUSE) DESIGN RULE FOR CU PROCESS*
- “Long-length AP fuse” can allow 90% shrinking.
- “Short-length AP fuse” is non-shrinkable. Please follow the rules in the following table.
- L-mark is non-shrinkable. Please follow the rules in the following table.

### 7.2.5.1 Non-shrinkable Rules:

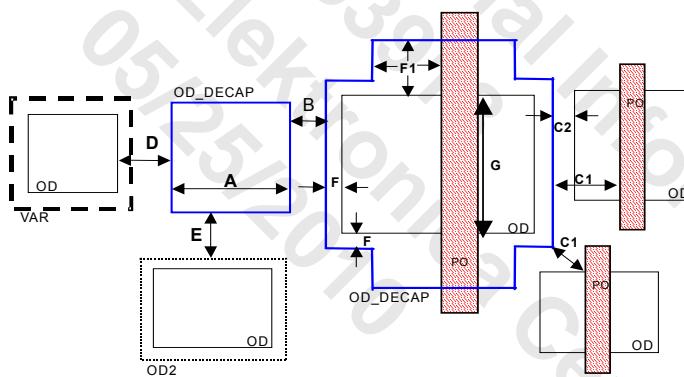
Rule No.	Description		Rule
FUL.1.1	Length of AP fuse between dog bone ( <b>Short-length AP fuse only</b> )	$\geq$	6.6
FUS.1	Space of AP fuse ( <b>Short-length AP fuse only</b> )	$\geq$	4.18
LW.W.1	Minimum width of L-slot (11 $\mu\text{m}$ is recommended)	$\geq$	11
	Maximum width of L-slot	$\leq$	22
LWL.1	Minimum length of L-slot (33 $\mu\text{m}$ is recommended)	$\geq$	33
	Maximum length of L-slot	$\leq$	55
LW.EN.1	LMARK enclosure of L-slot [in the direction of the L-slot length]	$\geq$	13.2
LW.EN.2	LMARK enclosure of L-slot [perpendicular to the direction of the L-slot length]	$\geq$	33



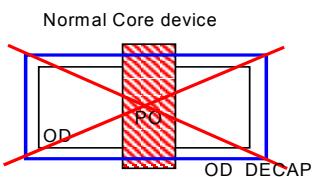
## 7.3 Core Decoupling Capacitor (OD\_DECAP) Layout Rules (For CLN80HS only) (Mask ID: 135)

- A second choice is provided for the Core (1.05V) MOS capacitor by using OD\_DECAP for lower leakage performance requirement.
- It's used for the N/PMOS decoupling capacitor only (N+OD/PO/PW, P+OD/PO/NW).

Rule No.	Description	Label		Rule
OD_DECAP.W.1	Width	A	$\geq$	0.47
OD_DECAP.W.2	Channel width in OD_DECAP	G	$\geq$	0.52
OD_DECAP.S.1	Space	B	$\geq$	0.47
OD_DECAP.S.2	Space to GATE	C1	$\geq$	0.22
OD_DECAP.S.3	Space to OD	C2	$\geq$	0.07
OD_DECAP.S.4	Space to {VAR AND OD} (Overlap is not allowed)	D	$\geq$	0.27
OD_DECAP.S.5	Space to OD2 (Overlap is not allowed)	E	$\geq$	0.47
OD_DECAP.EN.1	Enclosure of OD	F	$\geq$	0.07
OD_DECAP.R.1	OD_DECAP must fully cover {GATE SIZING 0.22 $\mu$ m}	F1	$\geq$	0.22
OD_DECAP.R.2 <sup>U</sup>	Overlap of normal core device is not allowed.			
OD_DECAP.R.3	OD_DECAP cut OD is not allowed			

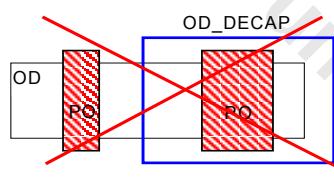


OD\_DECAP.R.2:



Not allow

OD\_DECAP.R.3:



Not allow

## 7.4 Non-shrinkable Layout Rules for CTM (Mask ID: 182) and CBM (Mask ID: 183) of MiM

- Besides the non-shrinkable and seal ring rules in CLN80GC, the table 7.4.1 is the non-shrinkable rules for the CTM & CBM layers of MiM capacitors on CMN80GC technology.

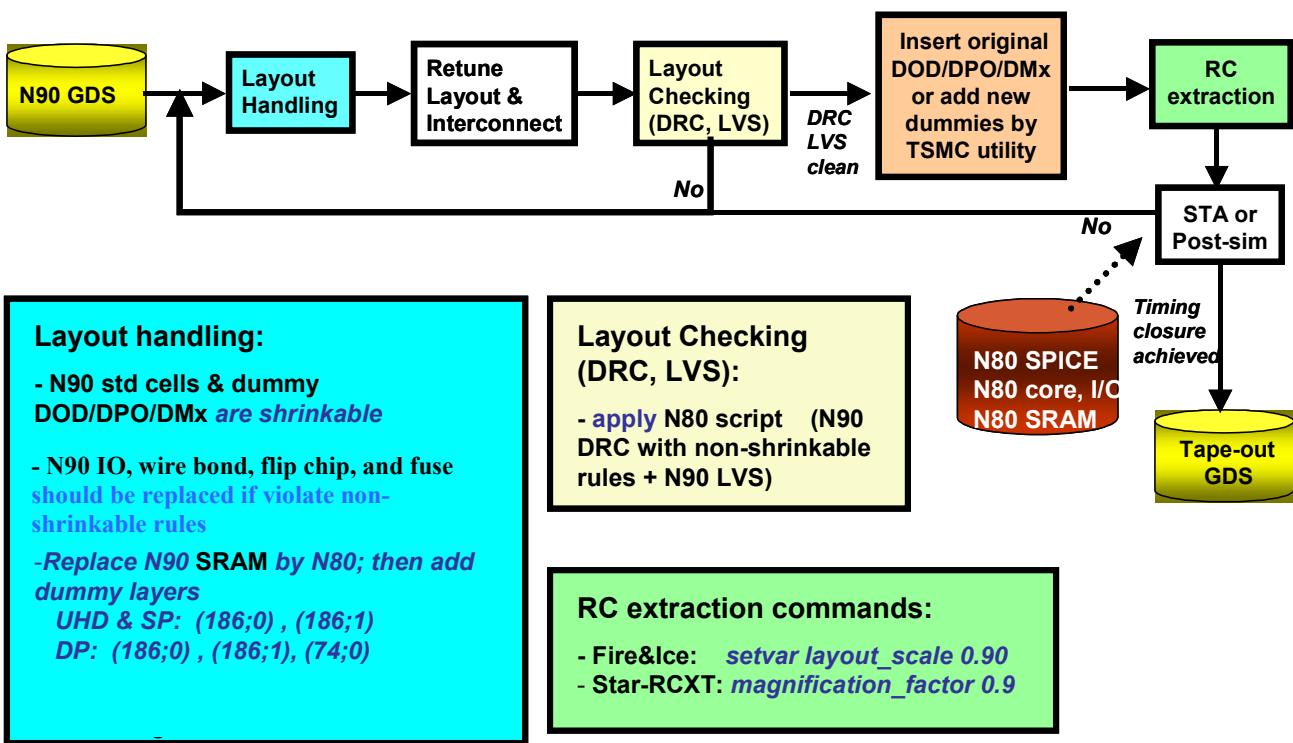
**Table 7.4.1 CMN80GC non-shrinkable rule for the CTM and CBM of MiM capacitors**

Rule no.	Description	Rule
CTM.S.1	Space	$\geq$ 0.88
CBM.S.1.1	Space of CBM inside a CTMDMY[Area < 44,000 $\mu\text{m}^2$ ]	$\geq$ 2.2
CBM.S.1.2	Space of CBM inside a CTMDMY[Area $\geq$ 44,000 $\mu\text{m}^2$ ]	$\geq$ 2.86
CBM.EN.1	Enclosure of CTM	$\geq$ 0.44
VIA.n.S.3	[VIA inside CBM but outside CTM] space to CTM	$\geq$ 0.33
VIA.n.EN.3	Enclosure by CTM	$\geq$ 0.26
VIA.n.EN.4	Enclosure by CBM	$\geq$ 0.22
Mn.S.4	Space of Mn[1st metal above MIM capacitor connect to CTM or CBM] inside CTMDMY	$\geq$ 0.92

## 7.5 Design Flow For Tape-Out

### 7.5.1 How to shrink the existing N90 design

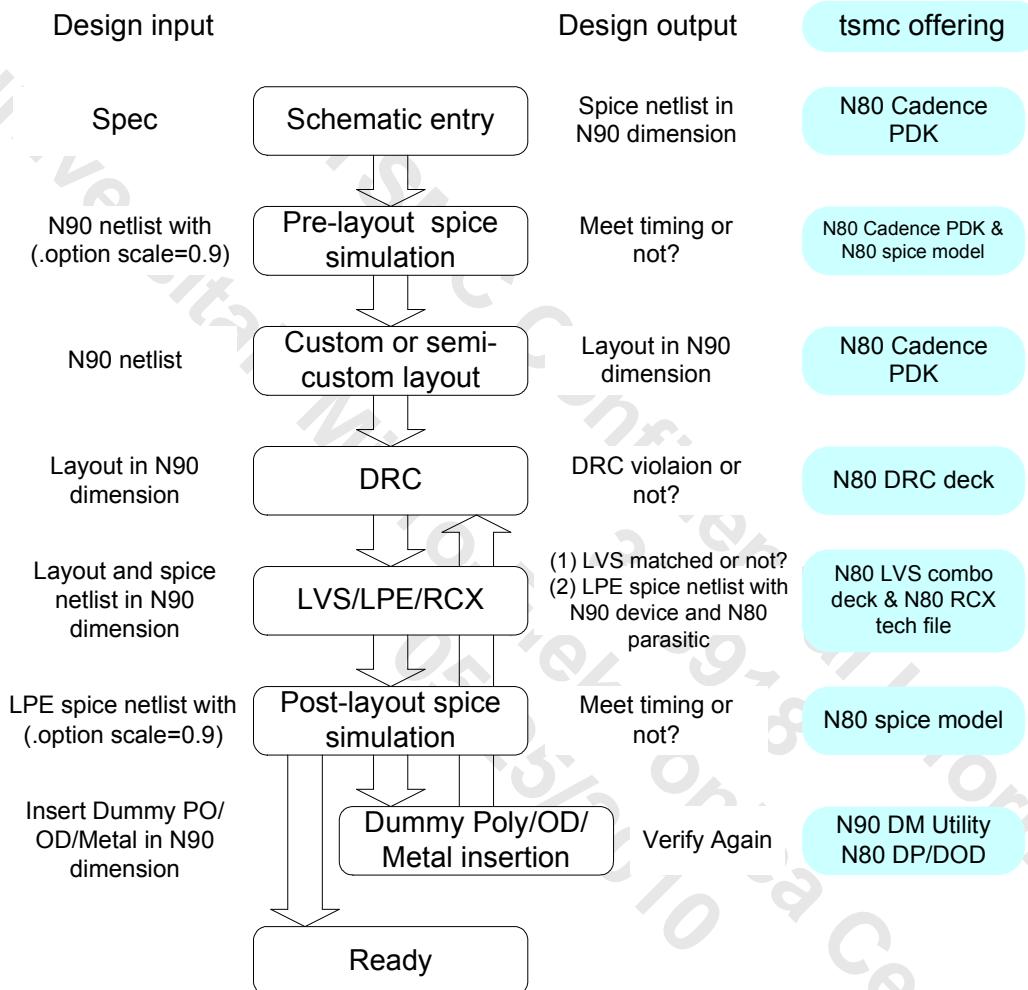
- **Designers must evaluate the following items when applying 90% shrinkage from an existing N90 design:**
  - Perform full-chip timing, leakage simulation and characterization to ensure chip functionality and robustness (with enough design margin).
  - Assess the BEOL RC delay impact, because the resistance of via-hole and sheet resistance (Rs) of metal line is higher in N80 as compared to N90.
  - Do not use low Vt devices in the design. They are not offered in N80 technology.
- **SRAM replacement:**
  - Designers must replace the N90 SRAM cell with a N80 one. It is also essential to replace the dummy, strapping, boundary, and twist cells with N80 leaf-cells.
    - Replace N90 SRAM by N80; then add dummy layers
      - UHD & SP: (186;0), (186;1) / DP: (186;0), (186;1), (74;0)
  - You have to confirm with the designers of the fuse IP about the necessary of fuse IP replacement.
- **110% size-up:** Designers may consider 110% size-up at the N90 level on the analog circuits (for example: matching circuits, current-driving at I/O circuits) to maintain the circuit performance.
- **It's recommended to use 1 nm design grid on 110% size-up IP layout to minimize the device layout mismatch due to the data truncation or grid snapping.** It may occur 5nm layout mismatch when snapping to 5nm design grid on the 110% size-up circuit. You should pay attention on the performance impact on the size-up circuits, especially on OD and PO layout. Please refer to the "110% Size-up" section 7.5.3 for the details. You could also consult with the TSMC Design Service about the size-up procedure.
- **The layouts for N80 must follow non-shrinkable rules.** (Please refer to section 7.2 "Non-shrinkable Layout Rules".)
- **Dummy OD/PO/Mx (DOD/DPO/DMx) patterns and rules are shrinkable.**
  - You can keep the original N90 dummy patterns, as long as the DOD/DPO/DMx rules can be met after re-tuning the real circuits.
  - You must re-fill the dummy patterns, if the DOD/DPO/DMx rules could not be met after re-tuning the real circuits.
  - It is recommended to use TSMC auto-fill utilities. (DOD and DPO utility no.: T-N80-CL-DR-001-C2; DMx utility no.; T-N90-LO-DR-001-C3)

**Figure 7.5.1.1 Shrink an existing N90 design to N80**

## 7.5.2 Analog IP design

### 7.5.2.1 Introduction

Here is the basic flow for N80 process, and it can be used in applying 90% shrinkage from an existing N90 design or developing a new N80 design.



## 7.5.2.2 Spice simulation

Design input:

- Pre-layout or post-layout spice netlist:
  - Pre-layout: N90 netlist
  - Post-layout: LPE netlist in N90 device dimension and N80 parasitic.
- Insert the ".option scale=0.9" in the netlist.

Design output:

- Meet timing or not?

tsmc offering:

- N80 Spice model

Geometric Shrink Factor Impact:

The scaling option in Hspice and Spectre will modify the parameters in device, and here is the table about the behavior in the simulator:

	Geometric parameters	W	L	PD	PS	AD	AS
		0.9	0.9	0.9	0.9	0.81	0.81
MOS	Electrical parameters	NRS	NRD				
		1	1				
DIO	Geometric parameters	AREA					
		0.81					
BJT	No parameter	No impact because only fixed layout/models are provided					
Design Cap & Resistor	Geometric parameters	No impact because they are modeled as macro (sub-circuit). Scaling factor is set in SPICE model header.					
Parasitic R, C	Parasitic values	No impact because no geometric parameters					

- **TSMC provides N80 logic and SRAM models, which designers can use to do pre-sim and post-sim for the circuits.**
- **Outline for both existing N90 design migration and new N80 design**

1. At pre-sim stage, scale=0.9 must be added in the net-list if the device size is in N90 dimension.
2. At post-sim stage, LPE will extract device size based on layout dimension and RC extractor will take care of parasitic extraction scaling. The device size is still in N90 dimension but parasitic is extracted based on 90% shrunk layout. As a result, scale=0.9 should be added in net-list for N80 simulation since it only impacts MOS, DIO geometry but not on parasitics). With this flow, pre-sim and post-sim environments are the same. Thus, it's easier for design integration and LVS back-annotation for debugging.

- **Simulation Syntax for scaling (HSPICE only):**

The following is an example for MOS and DIODE lib.

```
.option post tnom=25 ingold=2 numdgt=6 scale=0.9
```

- For the part of resistors and varactors, scale factor is put in spice model header. It is suitable for both pre-layout and post-layout simulation. Please refer to the example below.

```
***** Macro Model Resistor & Capacitor (or Varactor) *****
```

```
.LIB scale_option_res
.param scale_res= 0.9
.ENDL scale_option_res
```

```
.LIB scale_option_cap
.param scale_cap=0.9
.ENDL scale_option_cap
```

```
.LIB scale_option_cap25
.param scale_cap25=0.9
.ENDL scale_option_cap25
```

- There are also flags in SPICE model header for contact to poly gate resistance estimation in pre-layout stage.

```
***** Contact-to-poly parasitics *****
```

```
.LIB CCO_pre_simu
.param ccoflag=1
.ENDL CCO_pre_simu
```

```
.LIB CCO_pre_simu_hvt
.param ccoflag_hvt=1
.ENDL CCO_pre_simu_hvt
```

```
.LIB CCO_pre_simu_25
.param ccoflag_25=1
.ENDL CCO_pre_simu_25
```

```
.LIB CCO_pre_simu_na
.param ccoflag_na=1
.ENDL CCO_pre_simu_na
```

```
.LIB CCO_pre_simu_na25
.param ccoflag_na25=1
.ENDL CCO_pre_simu_na25
```

- BJT model is not a scalable model, so users can't specify "area" in the net-list. The model is calibrated based on a shrunk size (N80) and will not be affected by scale option

### 7.5.2.3 DRC

Design input: Layout(GDSII) in N90 dimension

Design output: DRC violation or not?

tsmc offering:

- N80 DRC deck
- Antenna and package rules including the wire-bond pad and flip-flop RDL

Customer's setting:

- Chip level: turn on the “FULL\_CHIP” switch
- IP level: turn off the “FULL\_CHIP” switch

### 7.5.2.4 LVS/LPE/RCX

Design input:

- Layout(GDSII) in N90 dimension
- Spice netlist in N90 dimension

Design output:

- LVS matched or not?
- LPE spice netlist with N90 device dimension and N80 parasitic

tsmc offerings:

- N80 LVS/LPE combo deck
- N80 RC extraction technology files

Customer's setting:

LVS Tools	Hercules	Calibre	Assura LVS
RCX Tools	Star-RCXT	Calibre-xRC	Assura RCX
Interconnect scaling	(In Star-RCXT command file) <i>magnification_factor: 0.9</i> <i>magnify_device_params: NO</i> (For cross-reference in output netlist) <i>XREF: YES</i>	(In Calibre-xRC run script) <i>setenv PEX_FMT_NO_MAGNIFY ON</i>  (In xRC rule file) <i>PEX MAGNIFY 0.9</i>	<i>capgen -c -scale 0.9</i> To generate a N80 deck

### 7.5.3 110% size-up

- For the size-up circuits, it's recommended to snap the design grid size to 1nm to minimize the device layout mismatch risk due to the data truncation or grid snapping.
- If you snap the design grid size to 5nm in the size-up circuits, the device layout may occur 5nm mismatch. You should pay attention to the performance impact on the size-up circuits, especially on OD and PO layout. Please refer to the mismatch impact ratio in the following table.

The impact ratio by the different design grid size after snapping						
Design grid size	Mismatch caused by grid snapping	OD/PO layout dimension				
		0.1um	0.11um	0.12um	0.13um	0.14um
5nm	5nm	0%	4.17%	3.85%	3.57%	3.33%
1nm	1nm	0%	0.46%	0.42%	0.39%	0.36%

- 110% size-up procedure:

**Prepare N90 IP:** Given N90 layout GDSII, which is clean on N90 DRC/LVS check.

**Stream-in:** Stream into layout editor database with precision 0.1nm (adding 1 more digit for database precision)

**Size-up 110%:** Size up layout by 110% in layout database

**Size-down CO/VIA:** Size down all CO/VIA layers to make CO/VIA size to be the same as before size-up. Thus, CO/VIA sizes comply with DRC.

**Flatten and merge polygons:** Flatten and merge polygons for avoiding gaps or jogs happening after grid snapping.

**Stream-out:** If you have the critical devices in the size-up circuits, please stream out and snap all co-ordinates to 1nm design grid.

**Run N80 DRC/LVS check:** Check the size-up circuits by 1nm grid size in DRC command file<sup>†</sup>. If there are any DRC violations, modify layout to fix these violations.

<sup>†</sup> Fill the cell name of size-up circuits behind the 1nm grid check variable in DRC command file. (Don't need to fill the cell name, if you snap to 5nm design grid). The variable of cell selection for 1nm grid check is listed below:

**CellsFor1nmGrid "cell1 name" "cell2 name" "cell3 name"...**

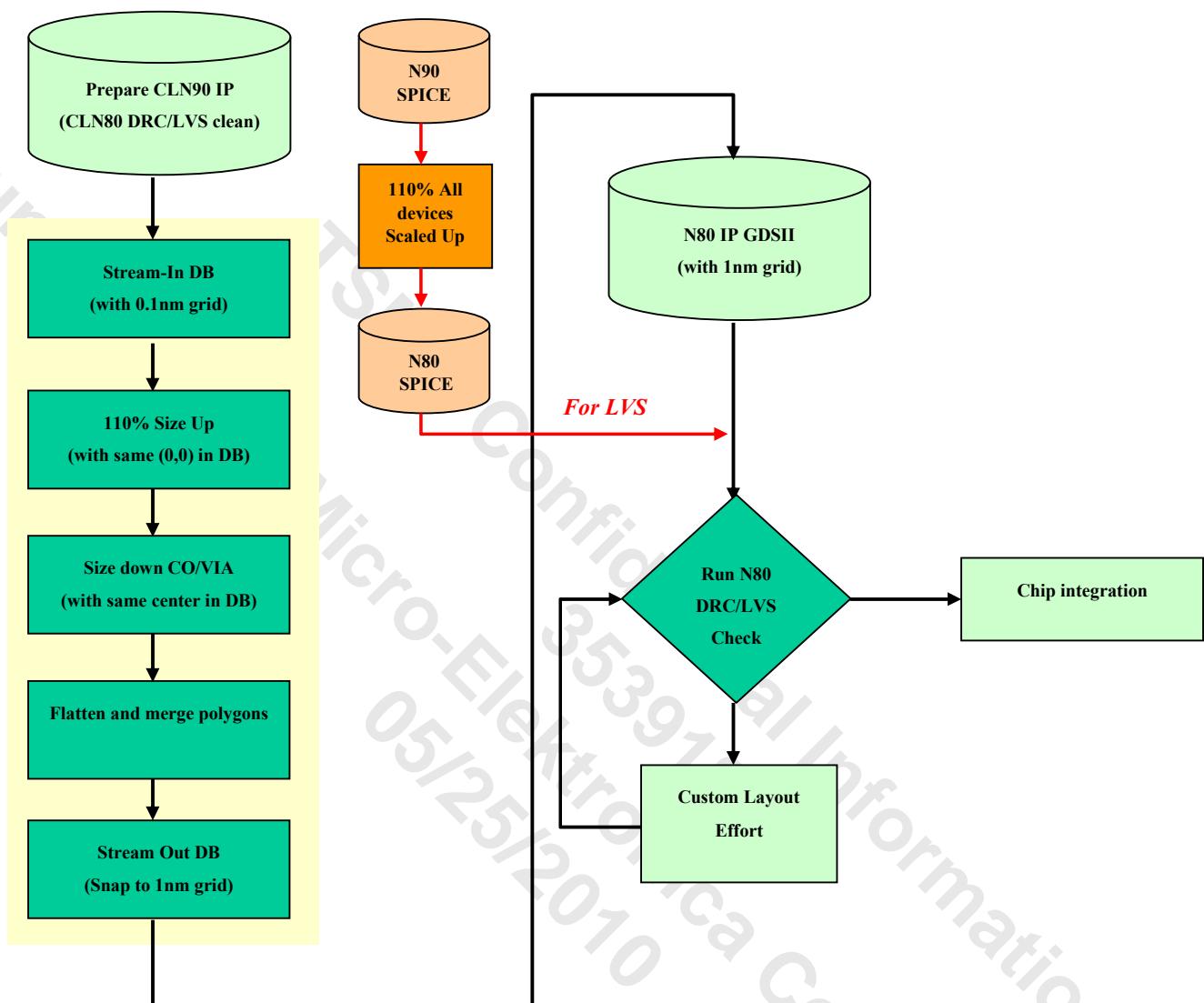
- Chip integration for size-up and direct-shrink circuits:

**Direct-shrink part:** Circuits of direct-shrink part keeps 5nm design grid, same as N90 requirement.110%

**Size-up part:** Circuits of 110% size-up part use 1nm design grid.

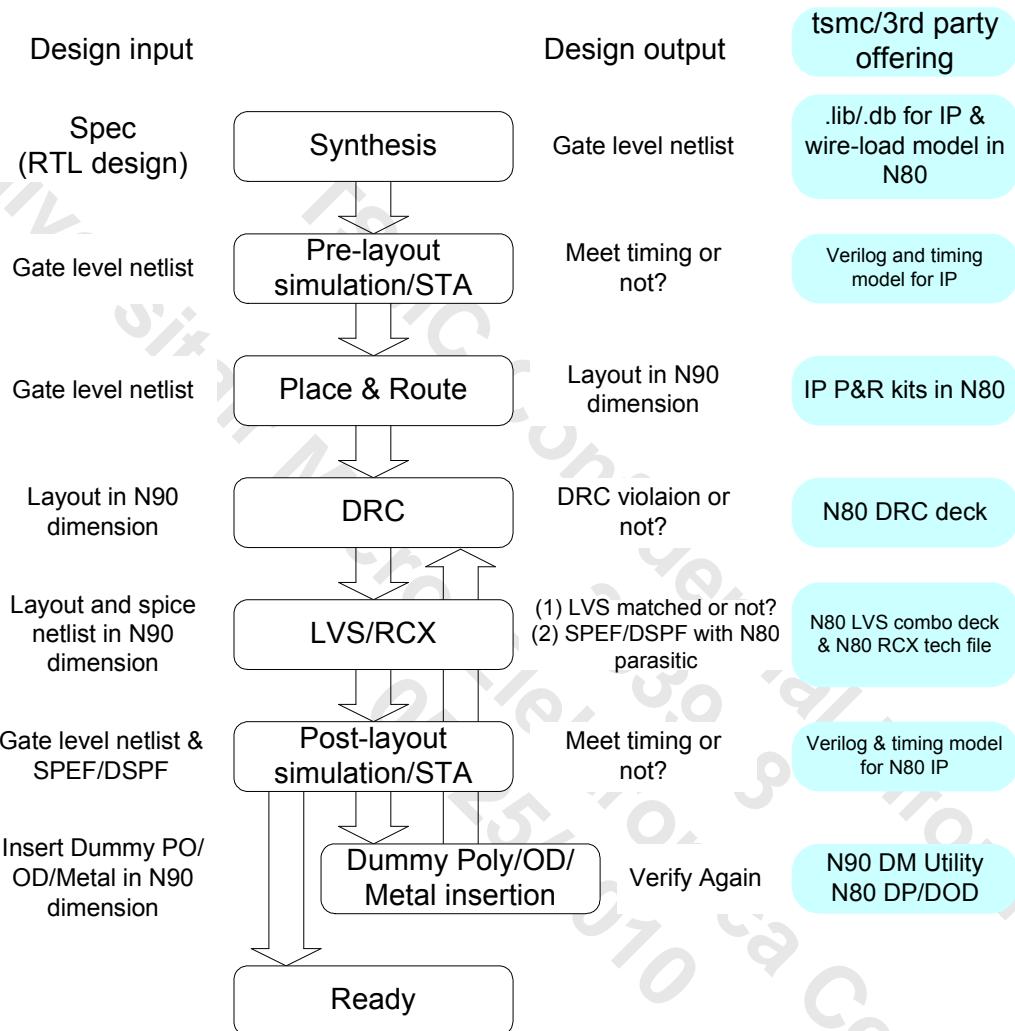
**Run N80 DRC/LVS check:** Please fill the cell name of 110% size-up circuits behind the 1nm grid check variable in DRC command file (Don't need to fill the cell name, if you use 5nm design grid in 110% size-up circuits). Then, 110% size-up circuits will be checked by 1nm grid size and the other direct shrink circuits will be checked by 5nm grid size. If there are any DRC violations, modify the layout to fix these violations.

- Please refer to Figure 7.5.3.1 for the 110% size-up flow chart

**Figure 7.5.3.1 Flow Chart of Size-up Procedure**

## 7.5.4 Digital IP and Chip integration

Here is the basic flow for N80 process. It can be used in applying 90% shrinkage from an existing N90 design or developing a new N80 design.



### 7.5.4.1 Synthesis

Design input: RTL and timing constraint

Design output: Gate level netlist

Current environment:

- N80 standard cell library
- N80 standard IO library
- N80 PLL
- N80 SRAM
- N80 3rd party IP & Library
- N80 wire load model for interconnect RC estimation
- Reasonable timing margin

## 7.5.4.2 Simulation/STA

Design input:

- For pre layout simulation/STA: Gate level netlist
- For post layout simulation/STA: Gate level netlist or SPEF or DSPF with N80 parasitic

Design output:

- Meet timing or not?
- Pass simulation/STA or not?

Current environment:

- N80 timing kits in IP and Library
- Reasonable timing margin

## 7.5.4.3 DRC

Design input: Layout (GDSII) in N90 dimension

Design output: DRC violation or not?

tsmc offering:

- N80 DRC deck
- Antenna and package rules including the wire-bond pad and flip-flop RDL

Customer's setting:

- Chip level: turn on the “FULL\_CHIP” switch
- IP level: turn off the “FULL\_CHIP” switch

## 7.5.4.4 LVS/RCX

Design input:

- Layout (GDSII, DEF, and Milkyway) in N90 dimension
- Spice netlist in N90 dimension

Design output:

- LVS matched or not?
- SPEF or DSPF gate level netlist with N80 parasitic

tsmc offering:

- N80 LVS deck
- N80 RCX technology file for sign-off

Customer's setting

LVS Tools	Hercules	Calibre	Assura LVS
RCX Tools	Star-RCXT	Calibre-xRC	Assura RCX
Interconnect scaling	(In Star-RCXT command file) <i>magnification_factor: 0.9</i> <i>magnify_device_params: NO</i> (For cross-reference in output netlist) <i>XREF: YES</i>	(In Calibre-xRC run script) <i>setenv PEX_FMT_NO_MAGNIFY ON</i>  (In xRC rule file) <i>PEX MAGNIFY 0.9</i>	<i>capgen -c -scale 0.9</i> To generate a N80 deck

## 7.5.4.5 Place and Route

Design input: Gate level netlist and floorplan in N90 dimension

Design output: Layout in N90 dimension

Current environment:

- CLN80 P&R kit
- LEF or Milkyway FRAM in N90 dimension
- Electrical/timing model in N80 dimension
- P&R tech file and RCX files for implementation
- Reasonable timing margin is necessary

<i>Cadence SOC Encounter</i>	<code>setShrinkFactor 0.9</code>
<i>Synopsys Astro</i>	<code>atTimingSetup atTimingSetupGoto "Parasitics" atCmdSetField "Parasitic Model Geometry Scaling" "0.9" atCmdSetParaModel</code>
<i>Synopsys Physical Compiler or IC Compiler</i>	<code>set_extraction_option -max_process_scale 0.9   -min_process_scale 0.9</code>
<i>Magma BlastFusion</i>	<p>During Volcano library preparation, layer list definition will depend on how many metal/via layers used in design</p> <pre>set l /LibraryName set Layers {M1 M2 M3 M4 M5 M6 M7 VIA1 VIA2 VIA3 VIA4 VIA5 VIA6} foreach layer \$Layers {     rule layer extraction \$layer \$l -scaling 0.9 } run prepare lib \$l -check_routability</pre>

## 7.5.4.6 IR/EM analysis

Design input: P&R layout database (DEF or Milkyway) in N90 dimension

Design output:

- Chip power analysis in N80 dimension
- Chip IR/EM analysis result in N80 dimension

Current environment:

- N80 library kits with CLN80 timing, power views
- N80 EM rules
- Reasonable IR drop margin

IR/EM Tools	Voltage Storm (Static)	Apache ( Static and Dynamic)
Input files	DEF file	LEF files DEF file
Layout scaling for chip analysis	In Vstorm command file <i>layout_scale 0.9</i>	In GSR file, <i>LEF_SCALE_FACTOR 0.9 {leffile1 leffile2}</i> <i>DEF_SCALE_FACTOR 0.9 {deffile}</i> Power pin/pad location file coordinates moved by users themselves
Library preparation	<b>In XTC command file</b> <i>setvar process_scale_factor 0.9</i>	In APL config file, either set <i>SIZE_SCALE 0.9</i> or put <i>.OPTION SCALE=0.9 in library spice file</i>

## 7.5.4.7 Package

Design input: Chip LVS I/O pin location file in N90 drawn dimension

Design output: Package pin location file in N80 silicon dimension

tsmc offering: Pad, bump, and RDL design rules

Customer's setting:

Notice that minimum pad or bump pitch of assembly house is usually described in silicon dimension.

Scale chip LVS pin text coordinates by 0.9 in spreadsheet to derive package pin locations for assembly house.

# 8 Layout Rules, Recommendations, and Guidelines for Analog Circuits

This chapter provides information about the following topics:

- 8.1 User guides
- 8.2 Layout rules for the WPE (well proximity effect)
- 8.3 Layout guidelines for LOD (length of the OD region) effect
- 8.4 Layout rules, recommendations, and guidelines for the analog design
- 8.5 Layout rules and guidelines for device placement
- 8.6 Burn-in guidelines for analog circuits

## 8.1 User Guides

1. Use these rules, recommendations, and guidelines to achieve better analog device performance and matching. In analog circuits, good device matching provides good performance margin and production yield.
2. The examples of analog circuits:
  - **Operational Amplifier:** includes differential input pair, bias circuit, and current mirror.
  - **DAC:** includes constant current source, amplifier using external Rset to adjust full range current and bias circuit.
  - **ADC:** includes comparator, amplifier, sample/hold switches, switching capacitor, and reference voltage resistor ladder.
  - **PLL:** includes VCO (delay stage) and charge pump (current mirror, buffer/opamp).
  - **Bandgap:** includes BJT, current mirror, bias circuit, differential amplifier, and ratioed resistor.
  - **LNA and mixer.**
  - **Sense amplifiers in memories.**
  - **Matching pair** includes active and passive device.
3. If you have any concerns about your circuit regarding the following rules, recommendations, and guidelines, TSMC DRC deck can help you to flag the violations. Analog DRC deck is bundled in the TSMC logic DRC deck. The following two methods can specify the region to run the analog part. Please also refer to the user guide in the DRC deck.
  - **Dummy layer:**
    - RRuleAnalog (CAD layer: 182;3): for the layout rules, recommendations and guidelines of the analog designs.
  - **Cell selection based on the following variable:**
    - CellsForRRuleAnalog: only check the cells in the variable.
    - ExclCellsForRRuleAnalog: don't check the cells in the variable.
4. A registered symbol “m” is marked as the rules, recommendations and guidelines of the analog designs.

## 8.2 Layout Rules for the WPE (Well Proximity Effect)

NMOS or PMOS very close to the well edge will exhibit a difference in threshold and Id from that of the device located remotely from the well edge.

For the sensitive circuit, e.g. constant current source or differential input pair, which needs precise device parameter control like  $\Delta V_t < 5\text{mV}$  and  $\Delta I_d < 2\%$ , please follow the subsequent four layout rules for WPE.

Rule No.	Device	Dimension
PO.S.11m	Gate space to (OD2 OR (NW OR NT_N)) in Core NMOS	$\geq$ 1.2
PO.EN.1m	Gate enclosure by (NW NOT NT_N) in Core PMOS	$\geq$ 1.0
PO.EN.2m	Gate enclosure by (OD2 NOT (NW OR NT_N)) in IO NMOS.	$\geq$ 2
PO.EN.3m	Gate enclosure by ((NW AND OD2) NOT NT_N) in IO PMOS	$\geq$ 2

1. The OD2 layout will change the Well pattern on mask due to logic operation. Therefore, not only NW layout but also OD2 layout will impact WPE effect. Please refer to the figure 8.2.1 and logic operation of the above four recommendations.
2. For dimensions smaller than the above rules, the  $V_t$  of a MOS device is raised as well as degrading the  $I_d$ . This effect increases with the reduction of the space or enclosure dimensions.
3. The WPE phenomenon occurs to every MOS: standard  $V_t$ , high  $V_t$ , low  $V_t$ , thin oxide MOS and thick oxide MOS.
4. If the above dimension is impossible to comply with in the critical circuit requiring tight matching in threshold voltage or  $I_d$ , identical layouts with identical well enclosure dimension should be kept. (Figure 8.2.3)
5. If the distance between gate and well is the same, the WPE impact from the poly end cap direction is smaller than that from the source/drain direction.
6. SPICE model has included the WPE effect. Users need to input SC in the netlist to activate these new features. During post-simulation LPE will automatically extract the SC from layout, and add the extracted SC to the netlist, then activate the model properly. (SC is the distance between gate to Well edge, please refer to the Appendix in the SPICE document). Not only NW layout but also OD2 layout will impact WPE calculation. Please refer to the 4 WPE recommendations in this section and the Figure 8.2.1.

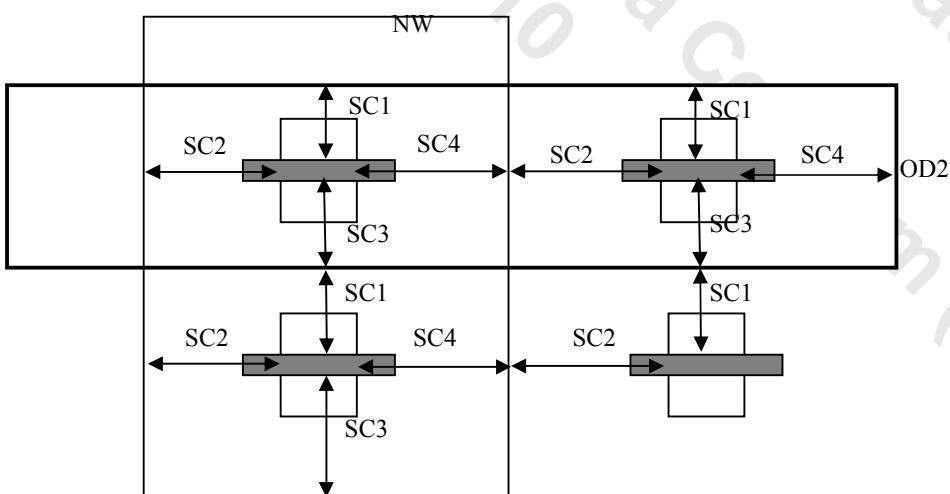
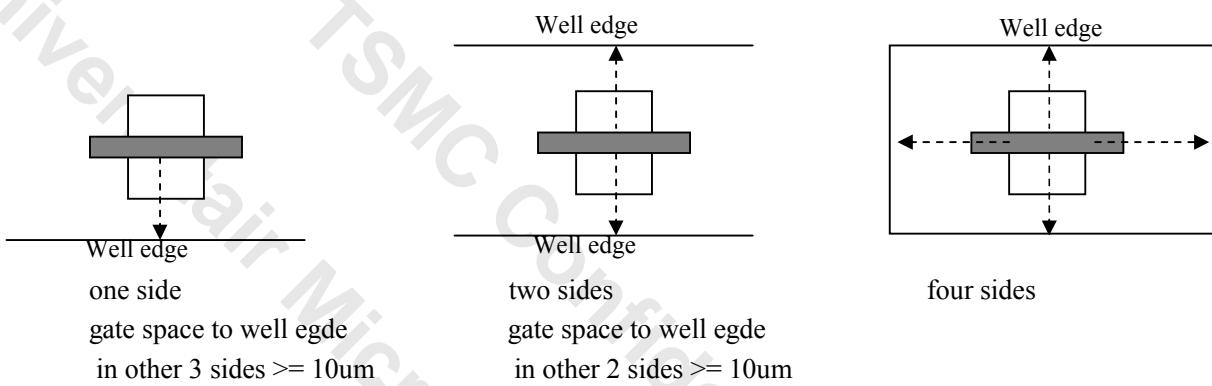


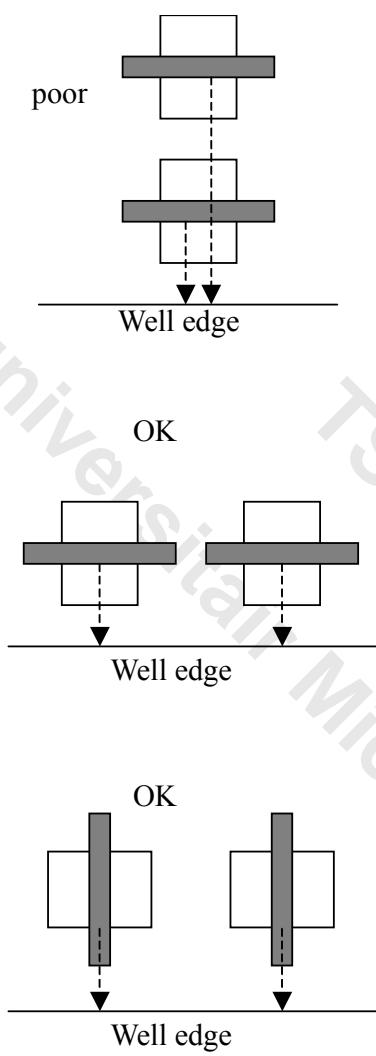
Figure 8.2.1 Both NW layout and OD2 layout are related to WPE

7. The detailed information regarding the device parameter impact by the WPE from one side, by the WPE from two sides, or by the WPE from four sides is as the following.

	Core N/PMOS		IO N/PMOS	
	$\Delta V_t < 5\text{mV}$	$\Delta I_d < 2\%$	$\Delta V_t < 5\text{mV}$	$\Delta I_d < 2\%$
1 side	$\geq 1.0\mu\text{m}$	$\geq 1.2\mu\text{m} / \geq 1.0\mu\text{m}$	$\geq 2.0\mu\text{m}$	$\geq 0.8\mu\text{m}$
2 sides	$\geq 1.5\mu\text{m}$	$\geq 2.\mu\text{m} / \geq 1.5\mu\text{m}$	$\geq 3.0\mu\text{m} / \geq 2.5\mu\text{m}$	$\geq 1.0\mu\text{m} / \geq 1.2\mu\text{m}$
4 sides	$\geq 2.0\mu\text{m}$	$\geq 2.5\mu\text{m}$	$\geq 4.5\mu\text{m} / \geq 3.5\mu\text{m}$	$\geq 1.5\mu\text{m}$



**Figure 8.2.2 One/two/four side for WPE**



For example, to meet  $\Delta V_t < 5\text{mV}$  in core N/PMOS,  
please keep gate space to well edge  $\geq 2.0\mu m$  in 4 sides.

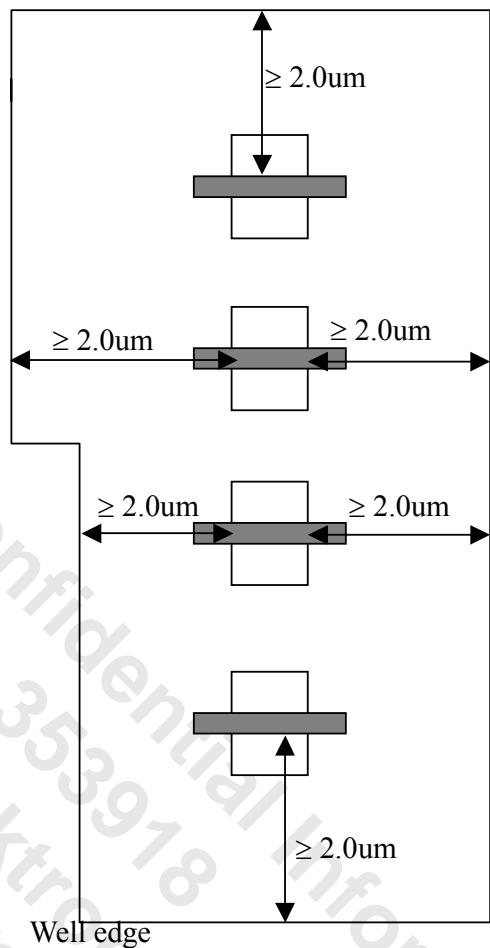


Figure 8.2.3 Device Placement for Matching Pairs

## 8.3 Layout Guidelines for LOD (Length of the OD region) Effect

### 8.3.1 What is LOD?

1. The device performance ( $V_t$  or  $I_d$ ) will be impacted by the LOD effect. It is due to the different mechanical stress induced by the different OD length.
2. The SPICE model has included the LOD effect. Users need to input SA and SB in the netlist to activate these new features. (SA and SB are the distance between the gate and the OD edge). (Figure 8.3.1)

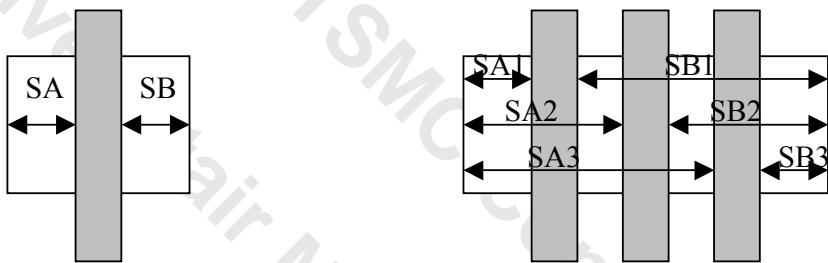


Figure 8.3.1 Example of SA and SB

### 8.3.2 Id change due to different SA

1. The drain current of the NMOS device will increase as the SA (or SB) increases, and the PMOS will decrease. Please refer to the figure 8.3.2.

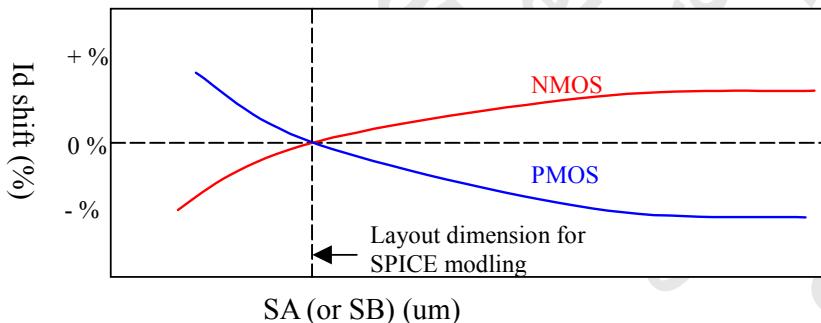


Figure 8.3.2 Id shift (%) due to different SA in NMOS/PMOS

2. Based on item 1, the NMOS  $I_d$  of a multi-finger device is higher than that of a series of single gate. Please refer to the figure 8.3.3.

	SB	$I_d$ of NMOS	$I_d$ of PMOS
Multi-finger device	larger	larger	smaller
Single-gate device	smaller	smaller	larger

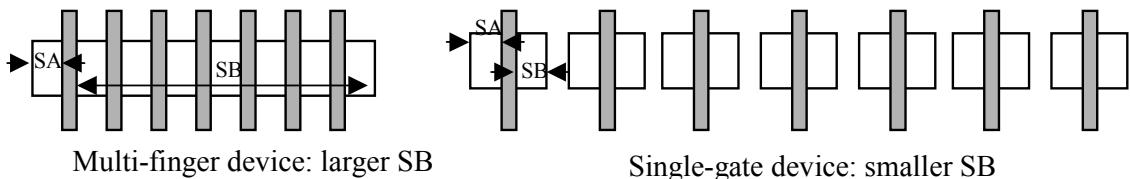


Figure 8.3.3 Id difference between multi-finger device and single-gate device in NMOS/PMOS

### 8.3.3 How to have a precise LOD Simulation

#### 1. For pre-sim cases

- PDK: Every MOS device in PDK has a layout view. So, when you use TSMC PDK to do design, the corresponding Pcell layouts are also ready. TSMC PDK includes a Skill code which can estimate the SA and SB values from the corresponding Pcell before real layouts. The pre-sim netlist will include the accurate SA and SB parameters.
- If you do not use PDK cell, you need to estimate the SA and SB first, and put them into the netlists as transistor instance parameters.

SA and SB are  $0.63\mu m$  for core device and  $0.82\mu m$  for IO devices in the layout of test structures for TSMC's SPICE model generation. If you copy the above dimensions during layout design, the LPE will not do any LOD correction.

#### 2. For post-sim cases (layouts are ready), designers need to use the TSMC LPE deck to extract the SA and SB directly from layouts. The LPE will automatically add the extracted SA and SB to the netlists and thus the simulators will then activate the models properly.

#### 3. Avoid the irregular OD layout due to model accuracy concerns. (Figure 8.3.4)

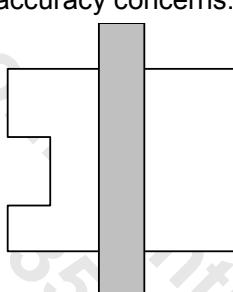
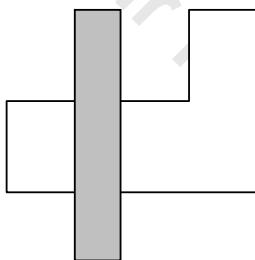


Figure 8.3.4 Irregular OD

## 8.4 Layout Rules, Recommendations, and Guidelines for the Analog Designs

### 8.4.1 General Guidelines

Guideline No.	Description
AN.R.1mg <sup>U</sup>	If possible, use devices with large widths. Do not use minimum widths and lengths for performance-critical device. Using current source device as an example, a designer should refer to the device I-V curve to check at which W/L range, the drain saturation current reaches a constant level.
AN.R.2mg <sup>U</sup>	Use larger areas for transistors, resistors, and capacitor devices for better mismatch.. Refer to the square root area model ( $1/\sqrt{WL}$ ) (Figure 8.4.1). However, figure 8.4.1 is not always suitable for every kind of MOS. Please contact TSMC to access the detail mismatch characterization report.
AN.R.33mg <sup>U</sup>	It is recommended to adopt all the advisory number of the DFM Action-Required Rules, and also adopt all the parametric/systematic related DFM Recommendations/Guidelines.
AN.R.34mg <sup>U</sup>	Prefer simple shapes (rectangles) of OD and Poly.
AN.R.35mg <sup>U</sup>	Avoid OD routing (Prefer using metals and Co) to limit the number of corner OD (risk of OD rounding), and to limit the number of narrow OD connections (risk of OD Rs variation)

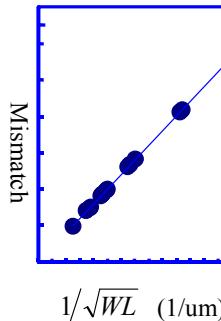


Figure 8.4.1 square root area model

## 8.4.2 MOS Recommendations and Guidelines

Recommendation No.	Description			Recommended	Min. Rule
PO.EX.1m®	Recommended PO extension on OD (end-cap)	G	$\geq$	0.18	0.16
PO.S.5m®	Recommended PO space to L-shape OD when PO and OD are in the same MOS for SPICE simulation accuracy	E1	$\geq$	0.1 (all dimensions)	0.1 (channel width < 0.2)
PO.S.6m®	Recommended L-shape PO space to OD when PO and OD are in the same MOS for SPICE simulation accuracy	E	$\geq$	0.1 (all dimensions)	0.1 (channel width < 0.2)
Guideline No.	Description				
PO.EX.2m <sup>g<sup>U</sup></sup>	For current mirror devices using common OD, please pay attention to LOD effect (please refer to section 8.3), eg. when using common OD, please follow the following items: 1) Keep the same SA/SB 2) Enlarger extension (F1) to put dummy gate at both source/drain sides with the same gate width, length, pitch and count, as possible.				
AN.R.44mg <sup>U</sup>	It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS device is enough to build up charge to the steady state, it is recommended to use <10 times of minimum channel length at the high operation frequency range. The operating frequency shall be below $0.2 * gm / Cgate$ , where gm is the transconductance of the transistor and Cgate is the gate-oxide capacitor.				

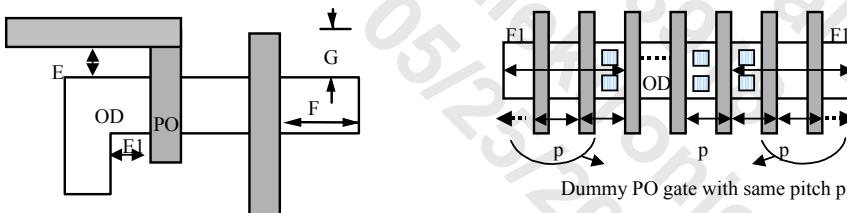


Figure 8.4.2 Analog Circuit Layout

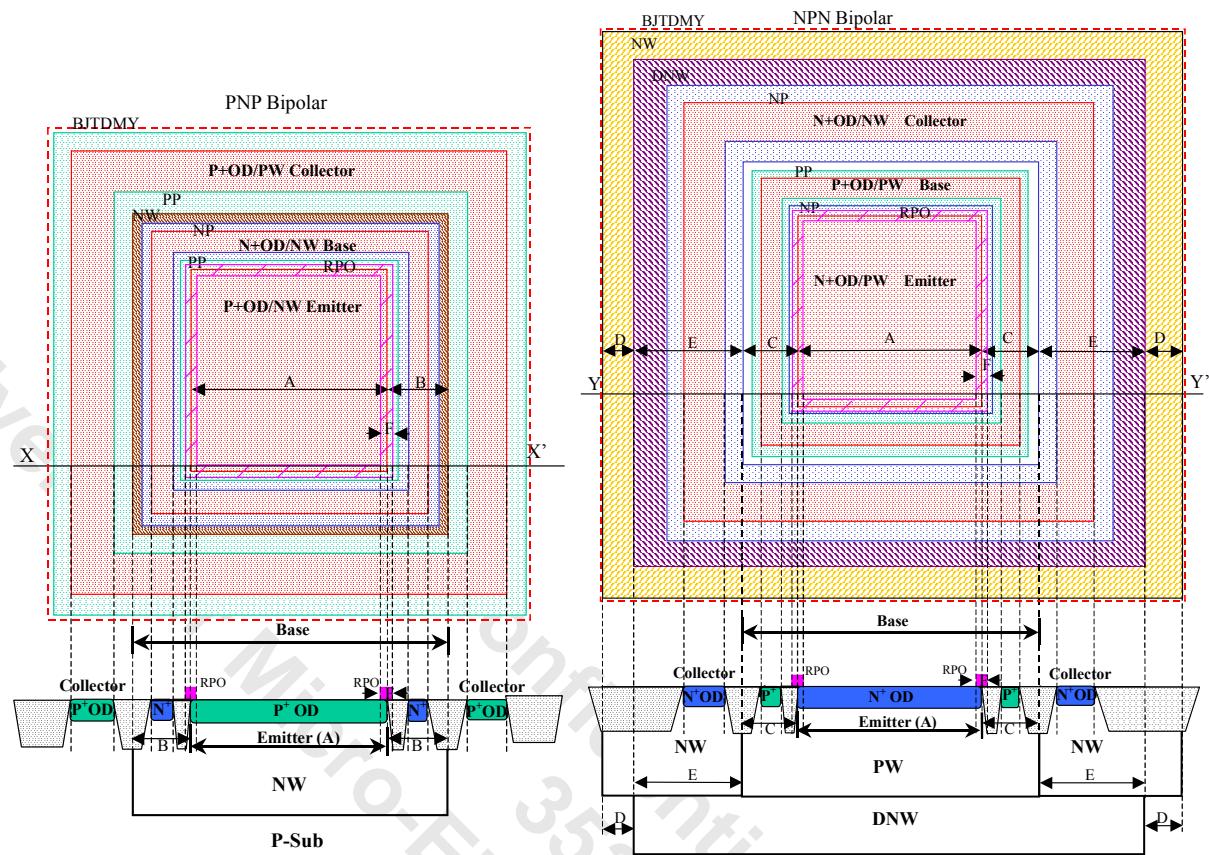
## 8.4.3 Bipolar Transistor (BJT) Rules and Recommendations

1. Two kinds of vertical bipolar are provided, PNP bipolar (P+/NW/PSUB) and NPN bipolar (N+/PW/DNW).
2. SPICE and PDK offer 3 kinds of emitter size and base size:

	PNP10 and NPN10	PNP5 and NPN5	PNP2 and NPN2
Emitter size	10x10	5x5	2x2
Base size	16x16	11x11	8x8

3. In order to have precise SPICE simulation prediction, it is strongly recommended that users should apply the standard TSMC bipolar layouts in their designs. Please refer to the bipolar sample GDS in SPICE sample layout document (T-N90-CL-SP-034) or PDK. DRC will also check the following rules and recommendations.
4. The entire device needs to be covered with a BJTD MY (CAD layer: 110) which is used for DRC and LVS checks.

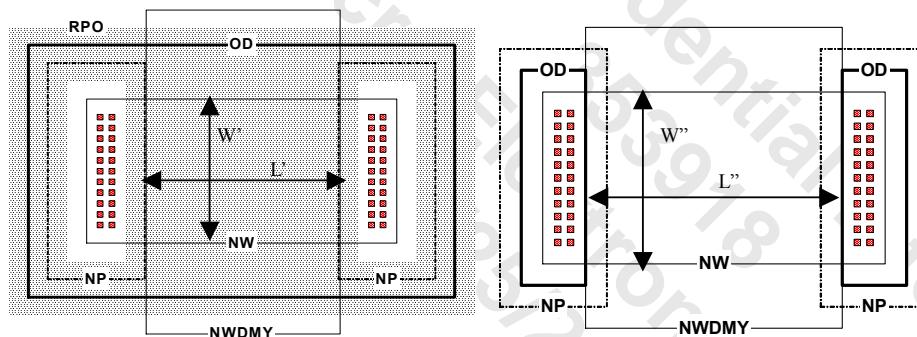
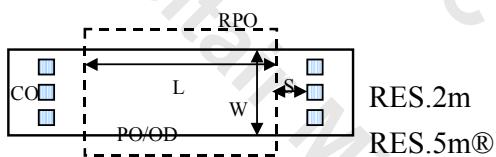
Rule No.	Description	Label		Rule
BJT.R.1	RPO needs to cover 0.3um on the Emitter OD edge for both OD and STI sides, i.e. RPO= ((Emitter OD sizing 0.3) NOT (Emitter OD sizing -0.3))	F		
Recommendation No.	Description	Label		Rule
BJT.R.2®	OD (Emitter size) is 2µm x 2µm, 5µm x 5µm, 10µm x 10µm,	A	=	
BJT.R.3®	NW enclosure of P+OD (Emitter OD) for PNP bipolar (no check corner to corner)	B	=	3.0
BJT.R.4®	NW space to N+OD (Emitter OD) for NPN bipolar (no check corner to corner)	C	=	3.0
BJT.R.5®	NW enclosure of DNW for NPN bipolar	D	>	1.5
BJT.R.6®	DNW enclosure of PW for NPN bipolar (no check corner to corner)	E	=	5.5
BJT.R.7®	BJTD MY overlap of NT_N, PO, VTH_N, VTH_P, VTLN, VTL_P, RH, VAR, and SRM is not recommended.			



**Figure 8.4.3 Layout and cross-section of a vertical PNP and NPN bipolar device**

## 8.4.4 Resistor Rules

Rule No.	Description
RES.2m	Width (W) $\geq 0.4\mu m$ , length (L) $\geq 0.8\mu m$ , and square number (L/W) $\geq 1$ for unsilicided OD/PO resistor. DRC can't check the square number.
RES.5m®	Recommened CO space to unsilicided OD/PO resistor = 0.22 (S).
NWROD.R.1m	Width (W') $\geq 1.8\mu m$ , length (L') $\geq 20\mu m$ , and square number (L'/W') $\geq 5$ for NW resistor within OD. DRC can't check the square number.
NWRSTI.R.1m	Width (W'') $\geq 1.8\mu m$ , length (L'') $\geq 20\mu m$ , and square number (L''/W'') $\geq 5$ for NW resistor under STI. DRC can't check the square number.



NW resistor within OD  
NWROD.R.1m

NW resistor under STI  
NWRSTI.R.1m

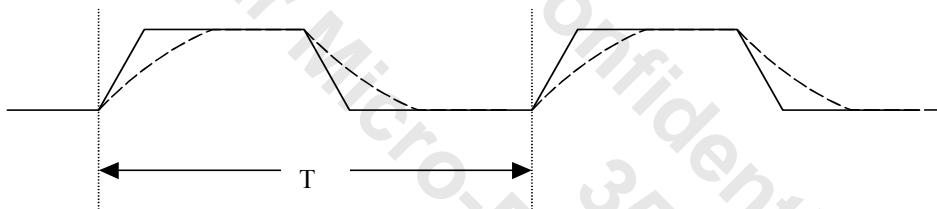
Figure 8.4.4 Resistor layout

## 8.4.5 Capacitor Guidelines

Guideline No.	Description
AN.R.36mg <sup>U</sup>	It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS capacitor (excluding varactor) is enough to build up charge to the steady state, it is recommended to use proper channel length at the high operation frequency range. The operating frequency shall be below $0.2 * gm / C_{gate}$ , where $gm$ is the transconductance of the transistor and $C_{gate}$ is the gate-oxide capacitance.
AN.R.37mg <sup>U</sup>	Varactor (NMOS capacitor in NW) is the best choice as MOS capacitor. And the NW should have a P-type guard ring tied to ground.

### 8.4.5.1 Design Guidelines for Capacitor Connections -- for the Estimation of Minimum Metal Width and Minimum Via Number

— Ideal current curve  
--- Real current curve



**Figure 8.4.5 Transient peak current**

For the estimation of minimum metal line width and the minimum number of vias connecting to capacitor terminals, we assume that the charging up or discharge time is a quarter of clock period  $T$ .

In calculation:

$\Delta t = T/4$  to charge up to VDD or discharge from VDD to ground.

$$T = 1/f, f \text{ is the clock frequency.}$$

The current to charge or discharge capacitor is

$$I_{max} = C \cdot \frac{dV}{dt} = C \cdot V_{DD} / (4f) = 4f \cdot V_{DD} \cdot C$$

$C$  is the capacitance extracted from layout

$f$  (is the clock frequency) and  $V_{DD}$  are provided by designer.

The minimum metal line width is

$$W(\text{metal width in } \mu\text{m}) = I_{max} / J_{max}, \text{ where } J_{max} = \text{EM current density for metal line per } \mu\text{m.}$$

The minimum number of via is

$$N(\text{Via number}) = I_{max} / J_{via}, \text{ } J_{via} = \text{EM current density for each Via.}$$

Both  $J_{max}$  and  $J_{via}$  are provided by process specifications to avoid EM (electro migration).

## 8.5 Layout Rules and Guidelines for Device Placement

### 8.5.1 General Rules and Guidelines

Rule No.	Description
AN.R.3m <sup>U</sup>	<p>You need to insert the dummy patterns in the empty area, even if the OD, PO, and metal density have already met the density rules. Insert the dummy patterns properly.</p> <p>The recommended steps for this AN.R.3m are:</p> <ol style="list-style-type: none"><li>1<sup>st</sup> Insert identical geometric dummy cells manually to minimize the proximity effect (Figure 8.5.1)</li><li>2<sup>nd</sup> Use TSMC's utility to fill dummy patterns on the rest of the empty space.</li><li>3<sup>rd</sup> In TSMC's utility, RRuleAnalog (CAD layer: 182;3) layer can't avoid DOD, DPO, or DMx insertion in the region. Please use ODBLK, POBLK, or DMxEXCL layer to cover your analog circuit, which will exclude DOD, DPO or DMx insertion during the chip level.</li><li>4<sup>th</sup> Do electrical or silicon characterization.</li></ol>
Guideline No.	<b>Description</b>
AN.R.4mg <sup>U</sup>	Avoid any sparse poly gate. Please refer to the item 3 in the section 10.1.2.1.1

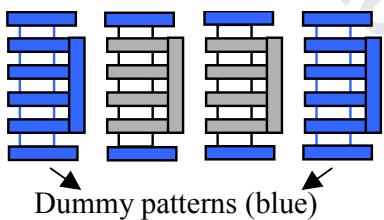


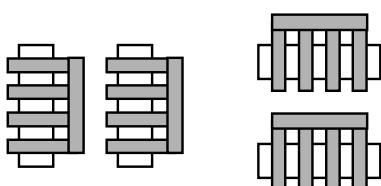
Figure 8.5.1 Example of manual DOD, DPO, or unit cell

## 8.5.2 Matching Rules and Guidelines

Rule No.	Description
AN.R.5m <sup>U</sup>	Make certain that the areas and shapes of matching pairs are identical. Do not use matching pairs with different proximities (iso/dense), nor with different widths, direction and areas, and different shapes of equal areas.
AN.R.38m <sup>U</sup>	Make certain that the local pattern density of, and nearby, the matching pair should be identical as much as possible. Use enough dummy cells surrounding the matching pair is highly recommended.
AN.R.6m <sup>U</sup>	Elements of the matching pair should have the same orientation (Figure 8.5.2).
AN.R.7m <sup>U</sup>	Avoid routing metal over a matching pair. M1 is the most critical. If it is unavoidable, then use identical routing metal with same potential, over the matching pair. (Figure 8.5.3).
Guideline No.	Description
AN.R.8mg <sup>U</sup>	Place the matching devices close together and, if possible, use "common-centroid" or "inter-digitated" placement for better matching. "Common-centroid" architecture is recommended for those devices that cannot be placed close together (Figure 8.5.4).
AN.R.9mg <sup>U</sup>	Regardless of any device dimensions of matching pairs with consistent resistance concerns, use the symmetrical number of contacts (please refer to the CO.R.5g ) and the same CO to PO gate space. (Figure 8.5.9). The layout of interconnection routing should be symmetrical with respect to each branch.
AN.R.10mg <sup>U</sup>	Pay attention to the associated routing layout, as well as the associated pattern density, of the matching pair, to minimize the Rs difference. (Figure 8.5.5)
AN.R.11mg <sup>U</sup>	Pay attention to the matching topology of the resistor layout (Figure 8.5.6)
AN.R.12mg <sup>U</sup>	The PO gate must connect to a protection diode by M1 to reduce the antenna effects in current mirror and matching pairs.
AN.R.39.mg <sup>U</sup>	In order to avoid the drift of electrical parameter matching, it is important to maintain identical DC bias on the each matching-transistor (NMOS or PMOS) at all operation conditions (eg, standby conditions). If the DC bias is not identical, please evaluate the impact of matching performance.

Better matching layout : same orientation

PO gates are all along x-direction (or y-direction)



Poor matching layout : different orientation

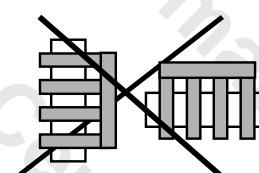
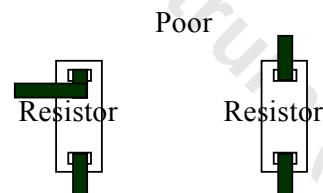
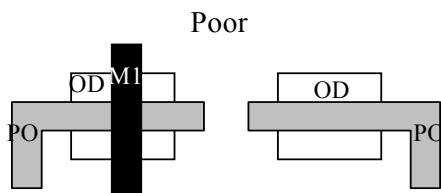


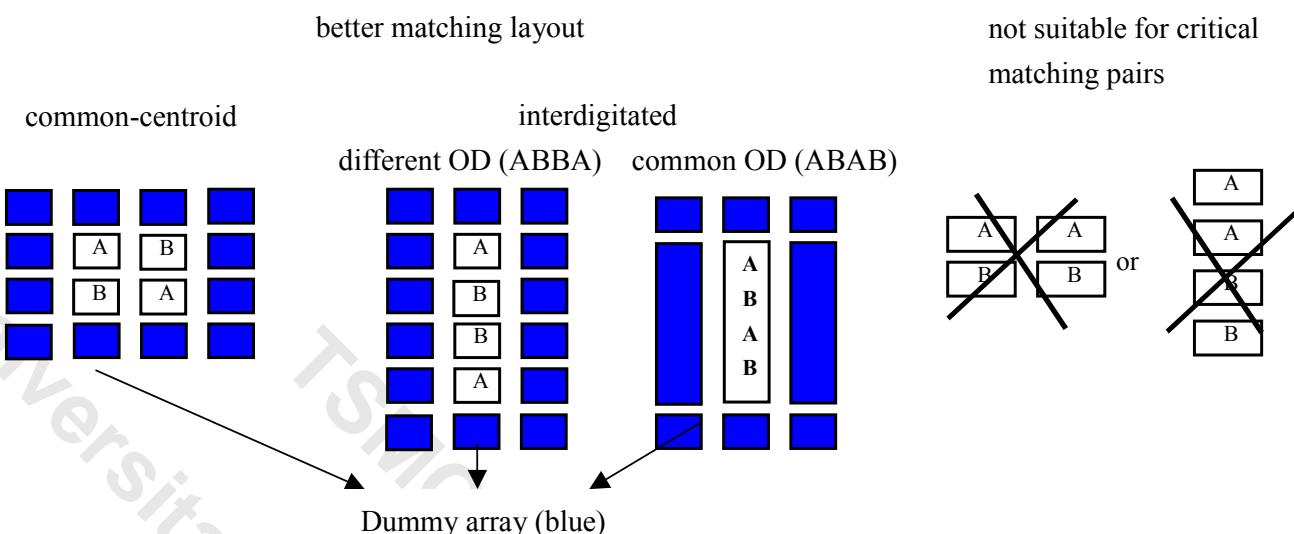
Figure 8.5.2 Example of same or different orientation for matching pairs



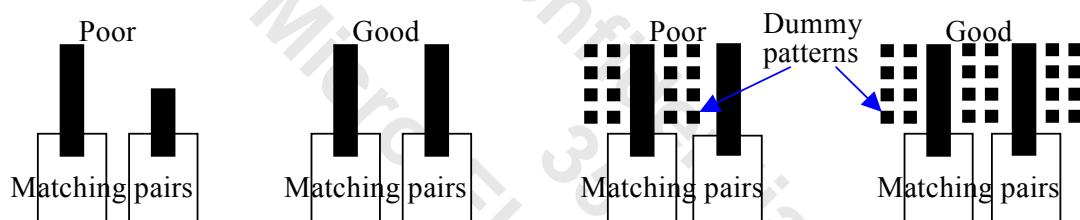
M1 over MOS affecting Vt

M1 over resistor affecting resistance

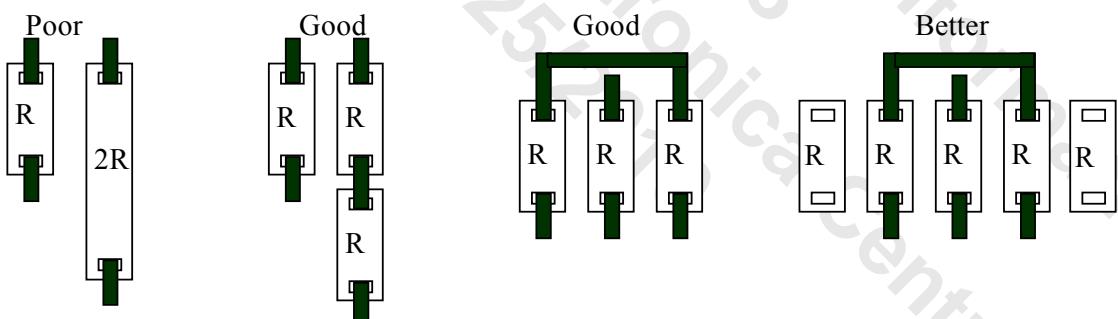
Figure 8.5.3 Example of routing metal over a matching pair



**Figure 8.5.4 Example of common-centroid or inter-digitated layout for matching pairs**



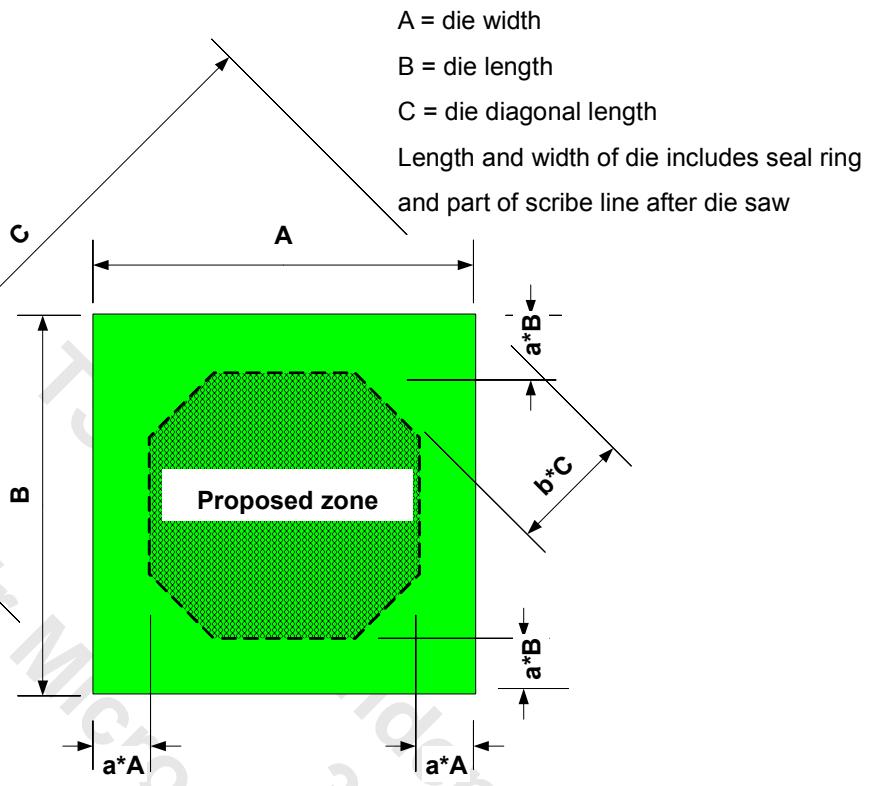
**Figure 8.5.5 Example of the associated routing layout of the matching pair**



**Figure 8.5.6 Example of matching topology of resistor layout for matching pairs**

### 8.5.3 Electrical Performance Rules and Guidelines

Rule No.	Description
AN.R.13m <sup>U</sup>	Avoid placing the matching pairs or performance-critical devices at the chip corner and chip edge. (Figure 8.5.7)
Guideline No.	Description
AN.R.14mg <sup>U</sup>	Avoid using silicided-OD connected between well strap and the MOS source node (butted junction) in analog, matching and performance-critical devices. (Figure 8.5.8)
AN.R.15mg <sup>U</sup>	Optimize the CO number at both source and drain sides of performance-critical devices. (Figure 8.5.9)
AN.R.16mg <sup>U</sup>	Do not use maximum latch-up rule near narrow ravine between wells. (Figure 8.5.10)
AN.R.17mg	Place unsilicided PO resistor on an N-well for better noise immunity. A P+ PO resistor is recommended for overall performance.
AN.R.18mg <sup>U</sup>	Do not use single via for high current or resistance sensitive wire. (Figure 8.5.11)
AN.R.19mg	Use thick oxide (OD2) MOS varactor and capacitor to reduce gate oxide leakage. DRC can not check capacitor.
AN.R.20mg <sup>U</sup>	CB and CBD are not recommended to put on the top of matching pairs or performance-critical devices.
AN.R.40.mg <sup>U</sup>	For the matching sensitive circuits with DC bias at low Vgs regions; the layout style effects (such as LOD, WPE and device orientation) should be carefully reviewed.



For the bottom/upper die in a stacked-die wirebond PBGA package

- 1) a: away from die edge  $\geq 10\%$  of the chip edge length
- 2) b: away from die corner  $\geq 15\%$  of the chip diagonal dimension

For a single-die wirebond PBGA package

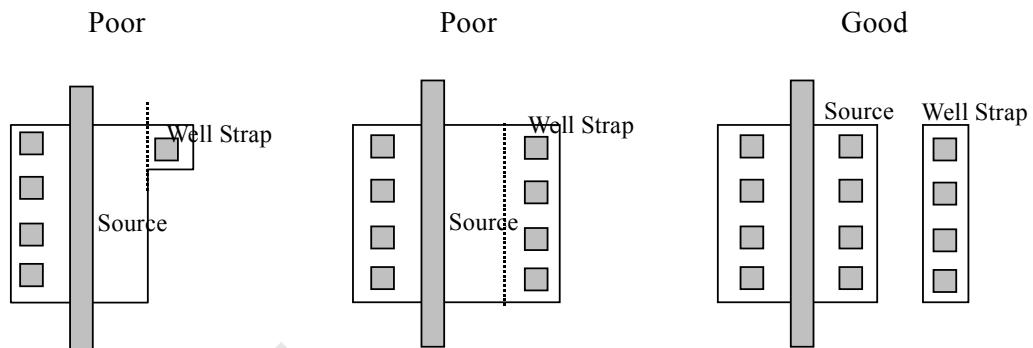
- 1) a: away from die edge  $\geq 3\%$  of the chip edge length
- 2) b: away from die corner  $\geq 5\%$  of the chip diagonal dimension

For a single-die flip chip PBGA package

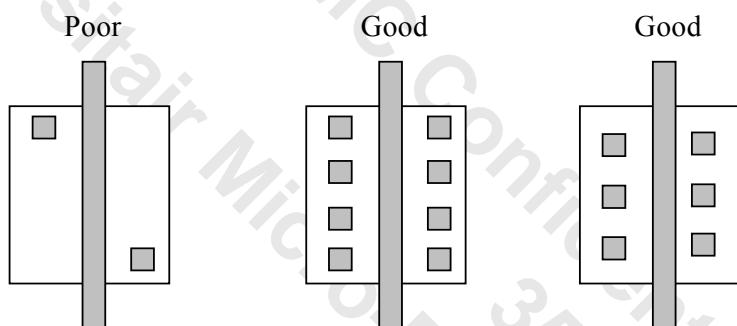
- 1) a: away from die edge  $\geq 1\%$  of the chip edge length
- 2) b: away from die corner  $\geq 3\%$  of the chip diagonal dimension

The above numbers may be changed by several factors, e.g. die size, die thickness, package type, package material, package size, and circuit design margin, please contact TSMC for more details.

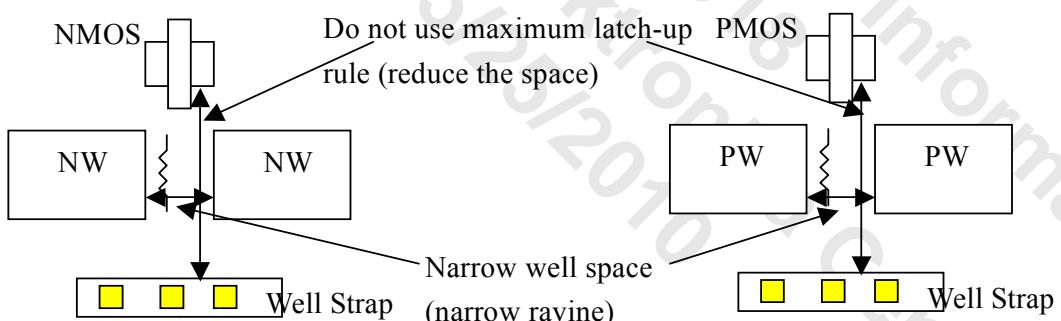
**Figure 8.5.7 The proposed zone for matching pairs or performance-critical devices**



**Figure 8.5.8 Example of avoiding using silicided-OD connected between well strap and the MOS source node**



**Figure 8.5.9 Optimize CO number at both source and drain sides**



**Figure 8.5.10 Example of maximum latch-up rule near narrow ravine between wells**



**Figure 8.5.11 Example of not using single via for high current or resistance sensitive wire**

## 8.5.4 Noise

### 8.5.4.1 Power and Ground

Guideline No.	Description
AN.R.21mg <sup>U</sup>	For the low noise circuit, a P-Well ring, which is tied to VSS, is recommended to surround all PMOS devices in each analog circuit block.
AN.R.22mg <sup>U</sup>	For the low noise circuit, a N-Well ring, which is tied to VDD, is recommended to surround all NMOS devices in each analog circuit block.
AN.R.23mg <sup>U</sup>	Putting NMOS in RW (PW in DNW) is a good practice of isolating critical circuit from substrate noise (Figure 8.5.12). Make sure every NW connected to DNW must have the same potential (refer to DNW.R.4).
AN.R.24mg <sup>U</sup>	Use NT_N layer (width >1um), as a high resistance region, to isolate two high frequency circuits, to reduce the noise or signal coupling from substrate (Figure 8.5.13). <ul style="list-style-type: none"> <li>■ minimize the signal lines crossing the high resistance NT_N region</li> <li>■ maximize the distance between metal lines from the substrate above the NT_N region (use upper level metal).</li> </ul>
AN.R.25mg <sup>U</sup>	Use separate power supplies and ground buses for the noisy and sensitive circuit, and also for the analog and digital circuits.
AN.R.26mg <sup>U</sup>	Keep enough distance between the noisy and sensitive areas.
AN.R.27mg <sup>U</sup>	Use a wide guard ring to stabilize substrate and well potential.
AN.R.28mg <sup>U</sup>	If transistors within sensitive circuit must be tied together with source and body, do not tie them in the local area by shorter metal line. (Figure 8.5.14)

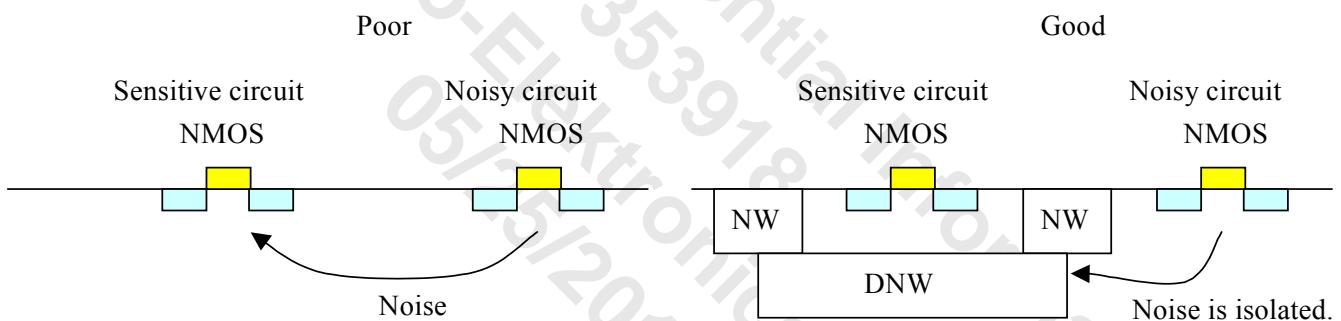
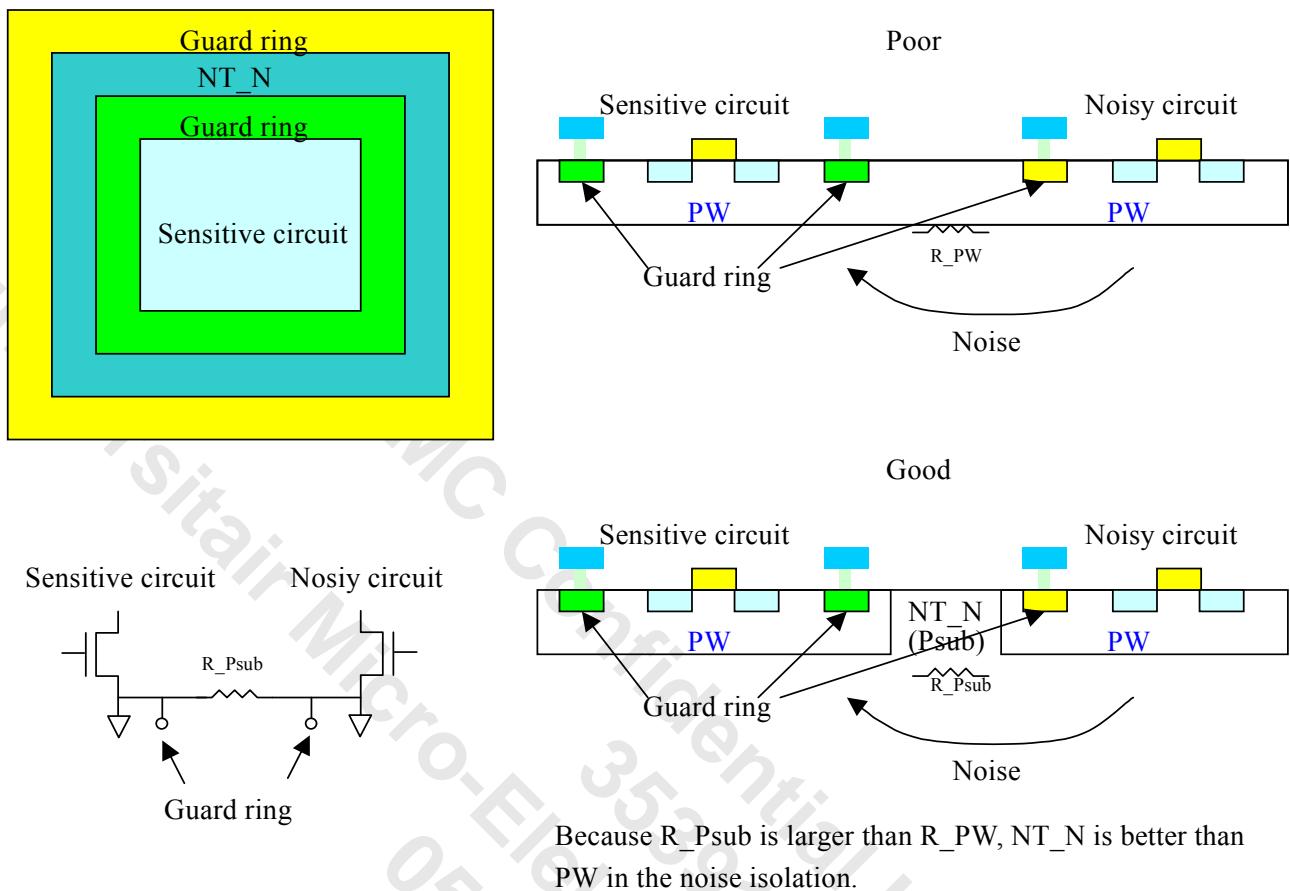
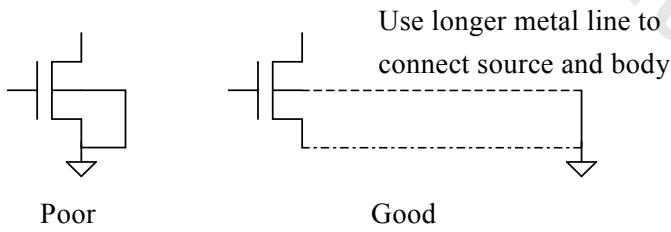


Figure 8.5.12 Example of NMOS in RW



**Figure 8.5.13 Example of NT\_N layer as a high resistance region**



**Figure 8.5.14 Example of transistors within sensitive circuit tied together with source and body**

### 8.5.4.2 Signal

Guideline No.	Description
AN.R.29mg <sup>U</sup>	Keep high frequency signal in high level metal layer.
AN.R.30mg <sup>U</sup>	Use metal shield for victim line that is noise sensitive.
AN.R.31mg <sup>U</sup>	Use metal and poly shield for attacker line that travels through long distance.
AN.R.32mg <sup>U</sup>	Prevent feedback path through chip seal ring between critical input and output. Use additional guard ring to isolate the coupling. (Figure 8.5.15)

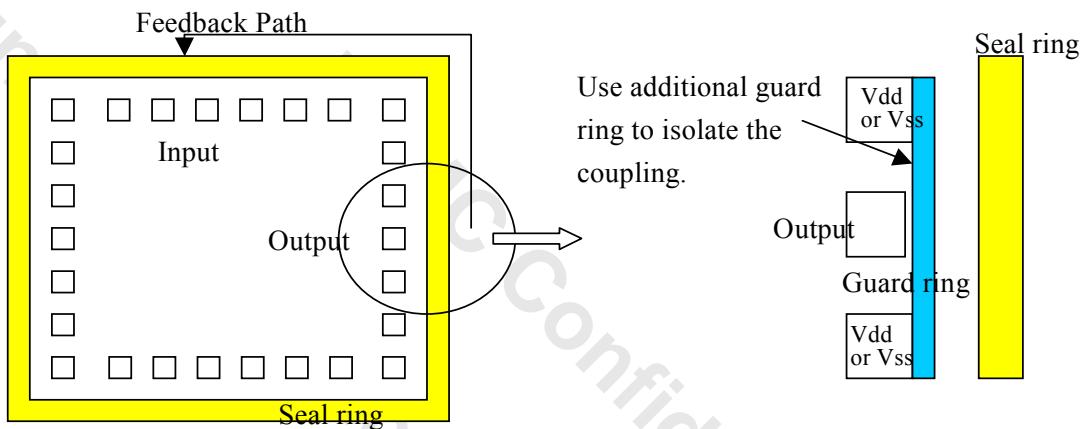


Figure 8.5.15 Example of prevention from feedback path through chip seal ring

## 8.6 Burn-in Guidelines for Analog Circuits

Guideline No.	Description
AN.R.41mg <sup>U</sup>	For the sensitive circuit, e.g. differential input pair, which needs precise device mismatching parameter control such as $\Delta V_t$ and $\Delta I_{sat}$ , it must avoid unbalanced DC bias stress during burn-in period. For example, $V_A=Vdd$ or GND & $V_B=1/2Vdd$ , which causes current supplied from current source flowing differently on the differential input pair ( $I_A \neq I_B$ ). This will make differential pair matching become worse after burn-in stress. (Figure 8.6.1)
AN.R.42mg <sup>U</sup>	Be sure that the analog circuit operates at normal operational condition during burn-in. For example, avoid P1 floating (when R is external) and make it be biased at the normal condition during burn-in. (Figure 8.6.2)
AN.R.43mg <sup>U</sup>	With the protection diode connection in the sensitive circuit to reduce plasma induced damage during wafer processing.

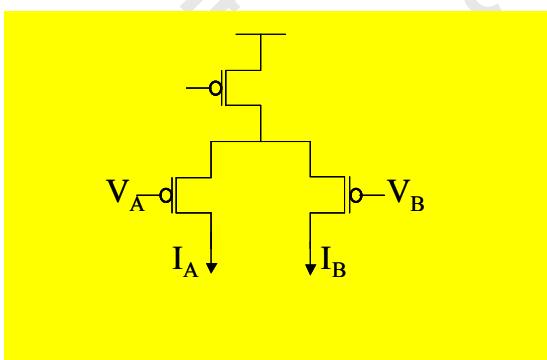


Figure 8.6.1 Example of differential input pair

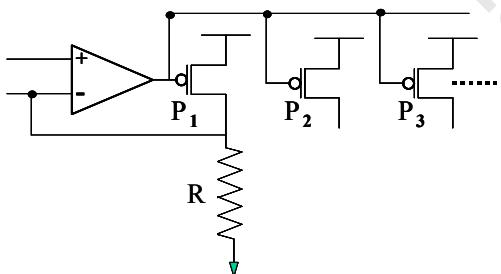


Figure 8.6.2 Example of analog circuit

# 9 Dummy Pattern Rule and Filling Guideline

This chapter contains the following topics:

- 9.1 Dummy OD rules
- 9.2 Dummy poly rules
- 9.3 Dummy metal rules
- 9.4 Dummy pattern fill usage summary

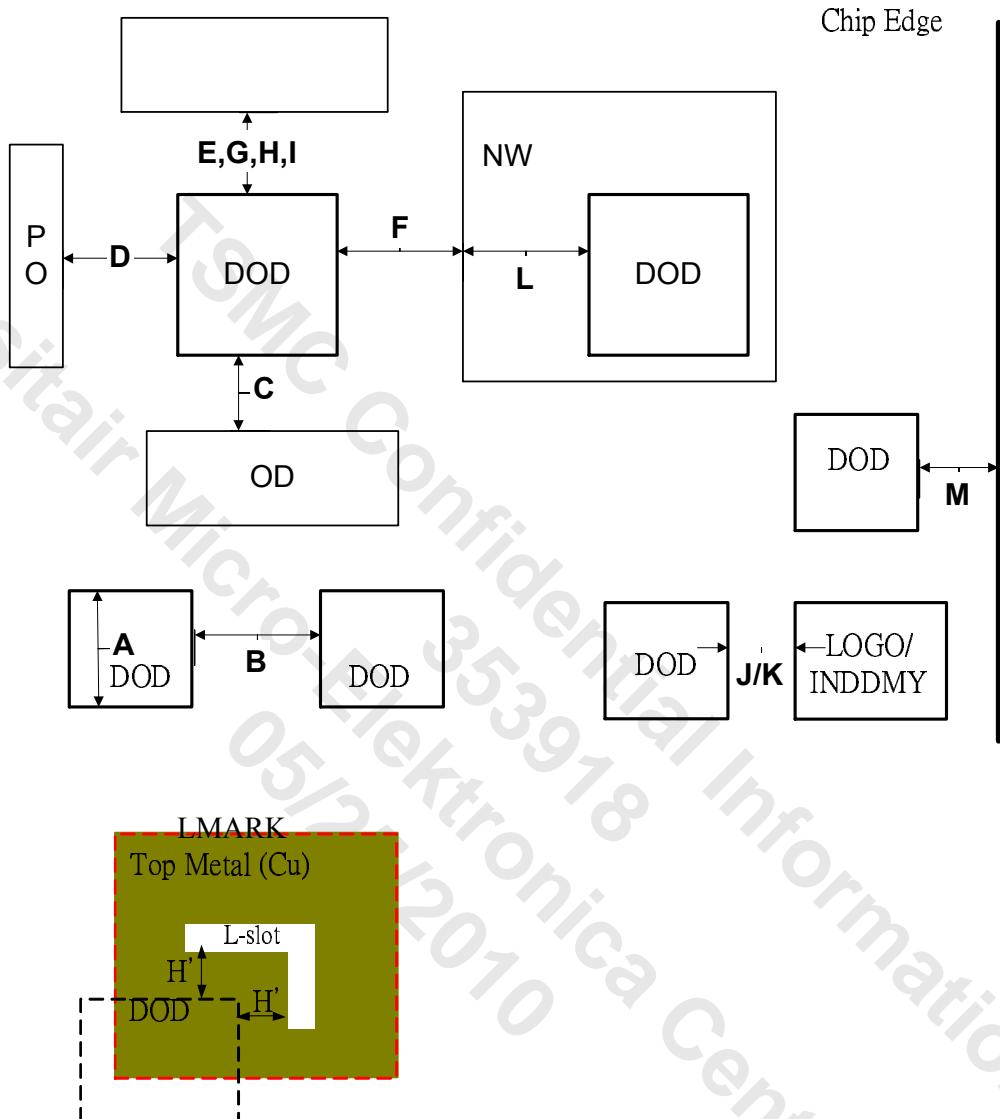
## 9.1 Dummy OD (DOD) Rules

1. In order to meet the extremely tight requirement in terms of process control for STI etch, polish as well as channel length definition (inter-level dielectric (ILD) planarization), you must fill the DOD globally and uniformly even if the originally drawn OD already satisfies the required OD density rule (OD.DN.1~OD.DN.3).
2. It is recommended to use TSMC's auto-fill utilities (documents: T-N90-LO-DR-001-C2 and T-N90-LO-DR-001-H2).  
It is important to perform the utility on the whole chip GDS. It is dangerous to perform the utility only on the local density violation blocks in terms of the process requirement.
3. It is recommended to use filler cells with OD/PO to fill a large empty area in the standard-cell-based block during the P&R stage. Current TSMC DOD/DPO utility is difficult to insert DOD shapes into a standard-cell placed area. For the better PO and OD CD control requirement, it is suggested to layout both OD and PO into filler cell (treat OD/PO as dummy filling, need to follow OD/PO and related rules, and use the GDS layer of OD/PO).
4. Evaluate the impact on OD masks carefully when any one of the following layouts is revised:
  - o PO/ DPO (poly and dummy poly)
  - o NW/ ODBLK/NWDMY/ FW/LMARK/ LOGO/ INDDMY
5. Use the dummy layer ODBLK properly. This layer (CAD layer no. 150;20) directs TSMC utility that the area covered should be blocked from DOD fill operations. ODBLK is for excluding DOD, not for excluding dummy Poly (DPO).
6. It is suggested to make sure that the ODBLK layer covers sensitive circuits, such as:
  - o Pad areas for high frequency signals
  - o SRAM sensitive functional blocks and bit cell arrays
  - o Analog/RF circuits (DAC/ADC, PLL, Inductor, MiM capacitor) and so on
7. It is recommended to manually add DOD uniformly inside regions covered by the ODBLK layer, to gain better process window and electrical performance.
8. Don't put DOD in areas covered by the following marker layers:
  - o Metal fuse (FW)/L target region (LMARK)
  - o Well resistor under STI (NWDMY)
  - o Inductor (INDDMY)
  - o LOGO
  - o Region of chip corner stress relief pattern, seal ring, and CDU patternTSMC's fill generation utility will not add DOD into these regions, as these layers are well defined. The ODBLK covered areas should not cover or overlap the above areas for DRC reasons.
9. Please refer to the "Dummy Pattern Fill Usage Summary" section in this chapter for additional information.
10. Please consult with TSMC first before you use your own DOD rules.

Rule No.	Description	Label		Rule
DOD.W.1	Width	A	$\geq$	0.5
DOD.S.1	Space	B	$\geq$	0.4
DOD.S.2	Space to OD (Overlap is not allowed)	C	$\geq$	0.6
DOD.S.3	Space to PO (Overlap is not allowed)	D	$\geq$	0.6
DOD.S.5	Space to NW	F	$\geq$	0.6
DOD.S.6	Space to FW (Overlap is not allowed)	G	$\geq$	1.2
DOD.S.7.0	Space to LMARK or L-slot is defined by either DOD.S.7 or DOD.S.7.1.			
DOD.S.7	Space to LMARK (Overlap is not allowed)	H	$\geq$	1.2
DOD.S.7.1	Space to L-slot (Overlap is not allowed)	H'	$\geq$	5.0
DOD.S.8	Space to NWDMY (Overlap is not allowed)	I	$\leq$	0.6
DOD.S.9	Space to LOGO (Overlap is not allowed)	J	$\geq$	0.0
DOD.S.10	Space to INDDMY (Overlap is not allowed)	K	$\geq$	1.2
DOD.EN.1	Enclosure by NW (fully outside is allowed)	L	$\geq$	0.6
DOD.EN.2	Enclosure by chip edge	M	$\geq$	0.6
OD.DN.1	{OD OR DOD} density across full chip		$\leq$	25%
			$\leq$	75%
OD.DN.2	{OD OR DOD} local density		$\geq$	20%
			$\leq$	80% (outside OD2)
			$\leq$	90%
OD.DN.3	{OD OR DOD} local density inside ODBLK		$\geq$	20%
			$\leq$	80% (outside OD2)
			$\leq$	90%
	<ol style="list-style-type: none"> <li>OD.DN.2 and OD.DN.3 are checked over any 150 <math>\mu\text{m}</math> x 150 <math>\mu\text{m}</math> window (stepping in 75 <math>\mu\text{m}</math> increments).</li> <li>(outside OD2) means the overlapped width between the checking window and OD2 layer is smaller than 37.5 <math>\mu\text{m}</math>.</li> <li>For OD.DN.2/OD.DN.3, the following regions can be excluded: <ul style="list-style-type: none"> <li>(CB sizing 2) for high speed/RF products for 20% rule.</li> <li>NWDMY/FW/LMARK/LOGO/INDDMY for 20% rule</li> <li>Chip corner stress relief and seal ring, and assembly isolation for 20%/80%/90% rule</li> </ul> </li> <li>OD.DN.2 is applied while the width of ((checking window NOT the item 3) <math>\geq</math> 37.5um).</li> <li>OD.DN.3 must be followed for every defined ODBLK region. This rule is only applied while the width of ((checking window AND ODBLK) NOT item 3) <math>\geq</math> 37.5um.</li> </ol>			
DOD.R.1	DOD is a must. DOD CAD layer (TSMC default, 6;1) must be different from OD's.			
DOD.R.2	DOD inside chip corner stress relief area is not allowed [except seal ring and stress relief patterns drawn by you].			
DOD.R.3	Only square (or rectangular) and solid shapes are allowed.			
Guideline	Description			
DOD.S.2g <sup>U</sup>	Recommended space to OD (C = 0.6)			
DOD.S.4g <sup>U</sup>	Recommended space to ODBLK (E $\geq$ 0.6) (Overlap is not recommended)			

**DOD**

ODBLK/FW/LMARK/NWDMY



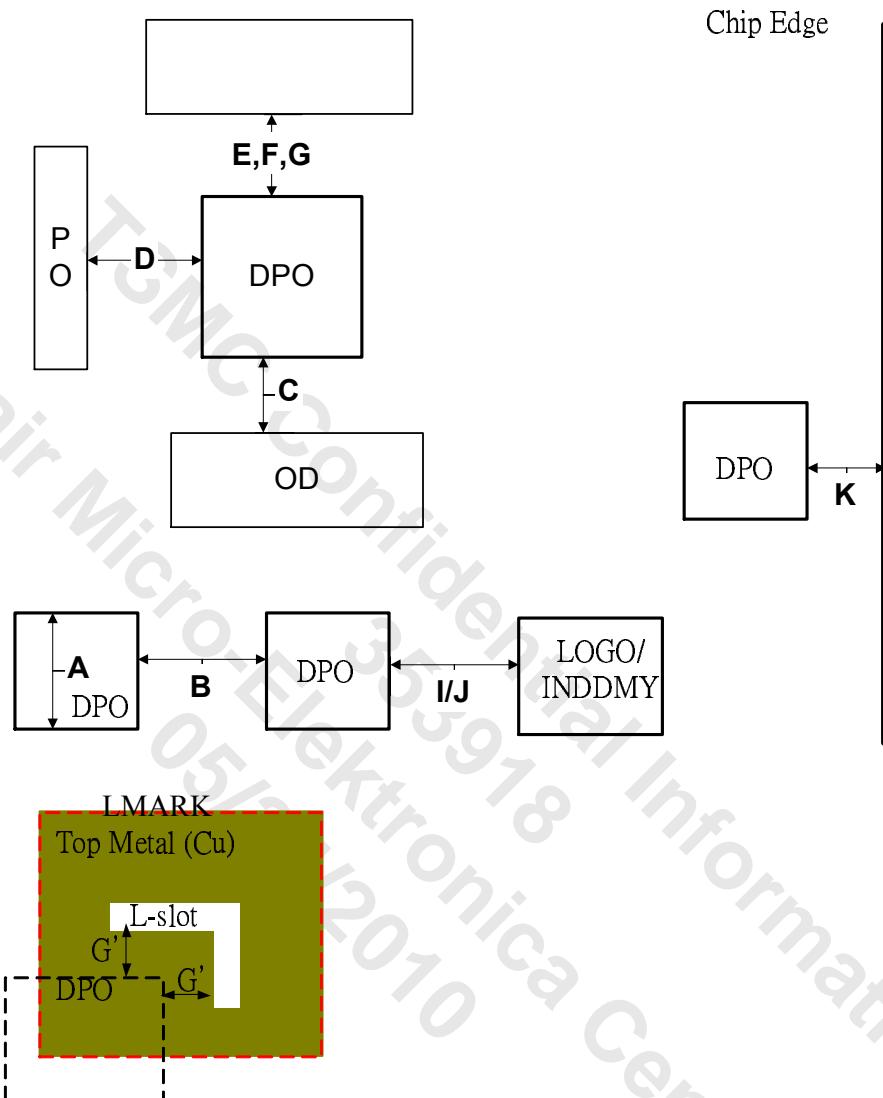
## 9.2 Dummy Poly (DPO) Rules

1. **Good Poly uniformity is the key to meet the PO CD as well as circuit performance requirement.** You must fill the DPO globally and uniformly even if the original drawn poly already satisfies the required poly density rule (PO.DN.1). The designer may wish to add dummy poly to improve the stability of the poly line dimension on silicon.
2. **It is recommended to use TSMC's auto-fill utilities** (documents *T-N90-LO-DR-001-C2* and *T-N90-LO-DR-001-H2*).
3. **It is recommended to use filler cells with OD/PO to fill a large empty area in the standard-cell-based block during the P&R stage.** Current TSMC DOD/DPO utility is difficult to insert DOD shapes into a standard-cell placed area. For the better PO and OD CD control requirement, it is suggested to layout both OD and PO into filler cell (treat OD/PO as dummy filling, need to follow OD/PO and related rules, and use the GDS layer of OD/PO).
4. **Evaluate the impact on the poly mask carefully** when there is DPO in the mask and any one of the following layouts is revised:
  - o OD/DOD
  - o POBLK/FW/LMARK/LOGO/INDDMY
5. **Use the dummy layer POBLK properly.** This layer (CAD layer no. 150;21) directs the TSMC utility that the area covered should be blocked from DPO fill operations. POBLK is for excluding DPO, not for excluding dummy OD (DOD).
6. **It is suggested to make sure that the POBLK layer covers sensitive circuits**, such as:
  - a. Pad areas for high frequency signals
  - b. SRAM sensitive functional blocks and bit cell arrays
  - c. Analog/RF circuits (DAC/ADC, PLL, Inductor, MiM capacitor) and so on
7. **It is recommended to manually add DPO uniformly inside regions covered by the dummy fill blocking layer POBLK**, to gain better process window and electrical performance.
8. **Don't put DPO in areas covered by the following marker layers** to avoid DRC problems.
  - o Metal fuse (FW)/L target region (LMARK)
  - o Inductor (INDDMY)
  - o LOGO
  - o Region of chip corner stress relief pattern, seal ring, and CDU patternTSMC's fill generation utility will not add DPO into these regions because these layers are well defined. The POBLK covered areas should not cover or overlap the above areas for DRC reasons.
9. **Please refer to the "Dummy Pattern Fill Usage Summary" section in this chapter for additional information.**
10. **Please consult with TSMC first before you use your own DPO rules.**

Rule No.	Description	Label		Rule
DPO.W.1	Width	A	$\geq$	0.4
DPO.S.1	Space	B	$\geq$	0.3
DPO.S.2	Space to OD (Overlap is not allowed)	C	$\geq$	0.2
DPO.S.3	Space to PO (Overlap is not allowed)	D	$\geq$	0.5
DPO.S.5	Space to FW (Overlap is not allowed)	F	$\geq$	1.2
DPO.S.6.0	Space to LMARK or L-slot is defined by either DPO.6 or DPO.6.1.			
DPO.S.6	Space to LMARK (Overlap is not allowed)	G	$\geq$	1.2
DPO.S.6.1	Space to L-slot (Overlap is not allowed)	G'	$\geq$	5.0
DPO.S.8	Space to LOGO (Overlap is not allowed)	I	$\geq$	0.0
DPO.S.9	Space to INDDMY (Overlap is not allowed)	J	$\geq$	1.2
DPO.EN.1	Enclosure by chip edge	K	$\geq$	0.6
PO.DN.1	{PO OR DPO} density across full chip		$\geq$	14%
			$\leq$	50%
PO.DN.2	{OD OR DOD OR PO OR DPO} local density		$\geq$	0.1%
	1. PO.DN.2 rules are checked over any 20 $\mu\text{m}$ x 20 $\mu\text{m}$ area. (stepping in 10 $\mu\text{m}$ increments). 2. For PO.DN.2 rules, the following regions can be excluded: o (CB sizing 2) for high speed/RF products o ODBLK/POBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default o Chip corner stress relief area if seal ring and stress relief pattern added by TSMC. 3. Even in areas covered by {ODBLK OR POBLK}, this pattern density that follows the PO.DN.2 rules is recommended. 4. The rule is applied while width of (checking window NOT item 2) $\geq$ 5um			
DPO.R.1	DPO is a must. DPO CAD layer (TSMC default, 17;1) must be a different layer from the PO CAD layer.			
DPO.R.2	DPO inside chip corner stress relief area is not allowed [except seal ring and stress relief patterns drawn by you].			
DPO.R.3	Only square (or rectangular) and solid shapes are allowed.			
Guideline	Description			
DPO.S.3g <sup>U</sup>	Recommended space to PO (D = 0.5).			
DPO.S.4g <sup>U</sup>	Recommended space to POBLK (E $\geq$ 0.4) (Overlap is not recommended)			
DPO.R.4g <sup>U</sup>	DPO cut DOD is not recommended			

**DPO**

## ODBLK/POBLK/FW/LMARK



## 9.3 Dummy Metal (DM) Rules

(DM<sub>x</sub>, x = 1,2,3,4,5,6,7,8,9,D)

1. To improve the metal CMP process window, **you must fill the dummy metal globally and uniformly** even if the originally drawn M<sub>x</sub> has already met the density rule (M<sub>x</sub>.DN.1/M<sub>x</sub>.DN.2/M<sub>x</sub>.DN.3).
2. **Use either the P&R dummy fill or the utility dummy fill as a method for inserting dummy metal.** Two methods are available for automated dummy metal insertion: commercial P&R tools and a utility from TSMC:
  - o The P&R dummy fill is better for dummy metal insertion at the chip level.
  - o The utility dummy fill is better for IP blocks, library cells, and full custom cells.
  - o Commercial P&R software inserts rectangular DM<sub>x</sub> geometry. TSMC also provides P&R settings for DM<sub>x</sub> insertion. Please refer to Reference Flow in *TSMC-Online*.
  - o The TSMC utility can insert square DM<sub>x</sub> uniformly within the original layout. (documents *T-N90-LO-DR-001-C3* and *T-N90-LO-DR-001-H3*)
  - o If you use TSMC's auto-fill utility to fill the DM<sub>x</sub> on the whole chip GDS, TSMC will waive the low local density violation (15% and 20% in M<sub>x</sub>.DN.1 and M<sub>x</sub>.DN.3). If you do not use TSMC's utility to perform the dummy metal generation, you must meet the local density rule (M<sub>x</sub>.DN.1/M<sub>x</sub>.DN.3).
3. In the TSMC utility, 2 kinds of dummy metal are generated, DM<sub>x</sub> and DM<sub>x</sub>\_O.
  - o DM<sub>x</sub>\_O: OPC dummy metal. The rules of DM<sub>x</sub>\_O are the same as real metal, M<sub>x</sub>.
    - o DM<sub>x</sub>\_O receives OPC. In the MT form, you need to combine DM<sub>x</sub>\_O into the real metal, like (M<sub>x</sub> OR DM<sub>x</sub>\_O).
    - o DM<sub>x</sub>\_O needs to meet all M<sub>x</sub> rules.
  - o The distinction between M<sub>x</sub>, DM<sub>x</sub>, and DM<sub>x</sub>\_O

	M <sub>x</sub>	DM <sub>x</sub>	DM <sub>x</sub> _O
GDS datatype	0	1	7
Do OPC modification on it	Yes	No	Yes
Refer to it during OPC	Yes	Yes	Yes
Follow M <sub>x</sub> rule	Yes	No	Yes

4. Use the dummy layer DM<sub>x</sub>EXCL properly. This layer directs TSMC's utility that the area covered should be blocked from DM fill operations. **All metal (geometry) beneath a customer-drawn blockage layer (DM<sub>x</sub>EXCL) must meet the density rule specified in M<sub>x</sub>.DN.3.**
5. **It is suggested to make sure that DM<sub>x</sub>EXCL is drawn over the following:**
  - o Sensitive circuits (such as SRAM sensitive function blocks and bit cell array) and analog circuits (such as DAV/ADC, and PLL)
  - o RF application circuits
  - o Pad areas for high frequency signals
  - o MIM capacitors for mixed-signal circuits

At a minimum, the first metal layer immediately beneath CBM is required. For example, if the capacitor is located between M8 and M7, then M7 under the CBM regions must be blocked.

For sensitive areas with auto-fill operations blocked by the DM<sub>x</sub>EXCL layer, careful manual uniform fill addition is still recommended so as to gain a better process window and electrical performance.

6. For DMxEXCL, use the GDS layer numbers 150;n (n = 1,2,3,4,5,6,7,8,9). For MD, use the GDS layer numbers (DMDEXCL) 150;15.
7. Revision of the following layers may necessitate re-filling of DMx. Because of this, **evaluate the impact on the metal layer mask carefully** when any one of the following layouts is revised:
  - o Mx and DMxEXCL layers. This layout revision impacts the Mx mask only.
  - o FW/LMARK/LOGO/INDDMY. This revision impacts all the metal layer masks.
  - o CBM (between Mx and Mx+1). This revision impacts the Mx mask only if there are no DM problems at the other metal layers. (CBM is a capacitor bottom-plate metal for an MIM capacitor in the MS/RF process.)
8. In order to have an accurate interconnect RC for timing and power analysis, it is important to extract RC after dummy metal insertion, and extract RC with density based metal thickness variation feature enabled.
9. **Don't put DMx in areas covered by the following marker layers:**
  - o Metal fuse (FW)/L target region (LMARK)
  - o MIM capacitor region (CBM)
  - o Inductor region (INDDMY SIZING 18)
  - o LOGO
  - o Regions of chip corner stress relief pattern, seal ring, and CDU pattern
 TSMC's fill generation utility will not add DMx into these regions because these layers are well defined. The DMxEXCL covered areas should not cover or overlap the above areas for DRC reasons.
10. Please refer to the “Dummy Pattern Fill Usage Summary” section in this chapter for additional information.
11. Please consult with TSMC first before you use your own DMx rules.

Rule No.	Description	Label		Rule
DMx.W.1	Width (minimum)	A	$\geq$	
DMx.W.2	Width (maximum) (checked by sizing down 1.5 $\mu\text{m}$ )	B	$\leq$	3.0
DMx.S.1	Space	C	$\geq$	
DMx.S.2	Space to Mx (Overlap is not allowed)	D	$\geq$	
DMx.S.3	Space to Mx (Overlap is not allowed) [Mx width > 4.5 $\mu\text{m}$ and the parallel metal run length > 4.5 $\mu\text{m}$ ]	E	$\geq$	1.5
DMx.S.4	Space to FW (Overlap is not allowed)	F	$\geq$	5.0
DMx.S.5.0	Space to LMARK or L-slot is defined by either DMx.5 or DMx.5.1.			
DMx.S.5	Space to LMARK (Overlap is not allowed)	G	$\geq$	5.0
DMx.S.5.1	Space to L-slot (Overlap is not allowed)	G'	$\geq$	5.0
DMx.S.7	Space to LOGO (Overlap is not allowed)	I	$\geq$	0.0
DMx.S.8	Space to INDDMY (Overlap is not allowed)	J	$\geq$	2.5
DMx.S.9	Space to CBM [CBM between Mx and Mx+1] (Overlap is not allowed)	K	$\geq$	1.5
DMx.EN.1	Enclosure by chip edge	L	$\geq$	2.5
DMx.A.1	Area (minimum)	M	$\geq$	
DMx.A.2	Area (maximum)	N	$\leq$	

Layer	Dimension				
	A	C	D	M	N
<b>M1 and Mx</b>	0.32	0.4	0.6	0.32	80
<b>Mn and MD (3XTM)</b>	0.6	0.8	0.6	0.60	160
<b>My and MD (2XTM)</b>	0.4	0.72	0.6	0.4	160
<b>UTM (ultra thick metal)</b>	3.0	3.0	3.0	9.00	600

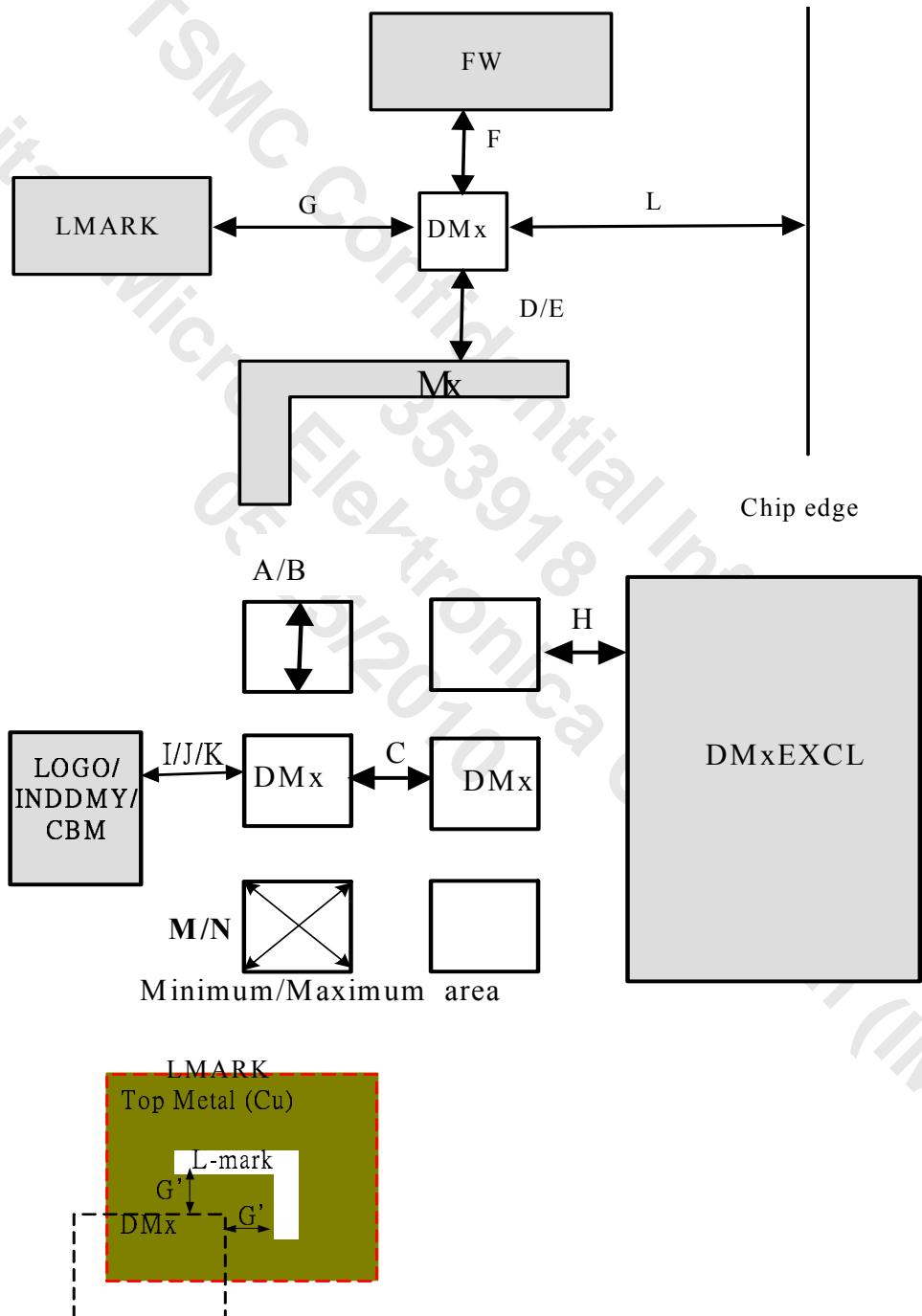
**Table Notes:**

UTM is ultra thick metal for interconnection and inductor in the MS/RF process.

Rule No.	Description		
Mx.DN.1	{Mx OR DMx} local density range in whole chip	≤ 15% in 50x50 (M1/Mx)	
		≤ 20% in 50x50 (Mn/ My/ MD)	
		≤ 20% in 100x100 (UTM)	
		≤ 70% in 100x100 (M1/Mx)	
		≤ 80% in 100x100 (Mn/ My/ MD/ UTM)	
Mx.DN.3	Metal local density range within DMxEXCL	≤ 15% in 50x50 (M1/Mx)	
		≤ 20% in 50x50 (Mn/ My/ MD)	
		≤ 20% in 100x100 (UTM)	
		≤ 70% in 100x100 (M1/Mx)	
		≤ 80% in 100x100 (Mn/ My/ MD/ UTM)	

	<ol style="list-style-type: none"> <li>1. <math>Mx.DN.1/Mx.DN.3 \geq 15\%/20\%</math> rule is checked over any <math>50 \mu m \times 50 \mu m</math> area (stepping in <math>25 \mu m</math> increments) for M1/Mx/Mn/My/MD and checked over any <math>100 \mu m \times 100 \mu m</math> area (stepping in <math>50 \mu m</math> increments) for UTM.</li> <li>2. <math>Mx.DN.1/Mx.DN.3 \leq 70\%/80\%</math> rule is checked over any <math>100 \mu m \times 100 \mu m</math> area (stepping in <math>50 \mu m</math> increments).</li> <li>3. <math>Mx.DN.1/Mx.DN.3</math> would exclude the following regions: <ul style="list-style-type: none"> <li>o FW/ LOGO/(INDDMY SIZING 18) for 15%/20% rules</li> <li>o LAMRK for 15%/20%/80% rules</li> <li>o Chip corner stress relief area and seal ring, and assembly isolation for 15% / 20% / 70% / 80% rule</li> <li>o CBM of MIM capacitor for 15%/20% rules. For example, if the capacitor is constructed between M8 and M7, then the M7 density check would exclude the CBM region.</li> </ul> </li> <li>4. <math>Mx.DN.1 \geq 15\%/20\%</math> rule is applied while the width of (checking window NOT item 3) <math>\geq 12.5 \mu m</math> for M1/Mx/Mn/My/MD and applied while the width of (checking window NOT item 3) <math>\geq 25 \mu m</math> for UTM.</li> <li>5. <math>Mx.DN.1 \leq 70\%/80\%</math> rule is applied while the width of (checking window NOT item 3) <math>\geq 25 \mu m</math>.</li> <li>6. <math>Mx.DN.3</math> must be followed for every defined DMxEXCL region.</li> <li>7. <math>Mx.DN.3 \geq 15\%/20\%</math> rule is only applied while the width of ((checking window AND DMxEXCL) NOT item 3) <math>\geq 12.5 \mu m</math> for M1/Mx/Mn/My/MD and applied while the width of (checking window NOT item 3) <math>\geq 25 \mu m</math> for UTM.</li> <li>8. <math>Mx.DN.3 \leq 70\%/80\%</math> rule is only applied while the width of ((checking window AND DMxEXCL) NOT item 3) <math>\geq 25 \mu m</math>.</li> <li>9. Bond pad is excluded from 80% density check.</li> </ol>		
Mx.DN.3®	<p>{Mx OR DMx} local density within DMxEXCL with <math>3 \mu m \times 3 \mu m</math> open area inside.</p> <ol style="list-style-type: none"> <li>1. Checked over any <math>10 \mu m \times 10 \mu m</math> area (stepping in <math>5 \mu m</math> increments)</li> <li>2. The open area is the region without metal or dummy metal.</li> <li>3. Mx.DN.3® will exclude the following regions: <ul style="list-style-type: none"> <li>o FW/LMARK/ LOGO/ (INDDMY SIZING 18)</li> <li>o CBM of MIM capacitor. For example, if the capacitor is constructed between M8 and M7, then the M7 density check would exclude the CBM region.</li> <li>o Chip corner stress relief area and seal ring</li> </ul> </li> <li>4. The rule is applied while width of (checking window NOT item 3) <math>\geq 2.5 \mu m</math></li> </ol>	$\geq$	20% (M1/Mx)
Mx.DN.2	Maximum metal density over any $20 \mu m \times 20 \mu m$ area (checked by stepping in $10 \mu m$ increments) Mn and My of bond pad and LMARK are excluded from 90% density check. The rule is applied while width of (checking window NOT Bond pad) $\geq 5 \mu m$	$\leq$	90% (M1/ Mx/ Mn/ My/ MD)
Mx.DN.4®	<p>It is not recommended to have local density <math>&gt; 70\%</math> of all 3 consecutive metal (Mx, Mx+1 and Mx+2) over any <math>50 \mu m \times 50 \mu m</math> (stepping <math>25 \mu m</math>), i.e. it is preferred to have for either one of Mx, Mx+1, or Mx+2 to have a local density <math>\leq 70\%</math>.</p> <ol style="list-style-type: none"> <li>1. The metal layers include M1/Mx and dummy metals.</li> <li>2. The check does not include chip corner stress relief pattern and seal ring.</li> </ol>		
DMx.R.1	DMx is a must. The DMx CAD layer (TSMC default, 31;1 for DM1) must be different from the Mx CAD layer.		
DMx.R.2	DMx inside chip corner stress relief area is not allowed [except seal ring and stress relief patterns drawn by you].		
DMx.R.3	Only square (or rectangular) and solid shapes are allowed.		
DMx_O.R.1	DMx_O INTERACT Mx is not allowed.		
<b>Guideline</b>	<b>Description</b>		

DMx.S.6g <sup>U</sup>	Recommended space to DMxEXCL ( $H \geq 0.6$ ) (Overlap is not recommended)		
DMx.W.1g <sup>U</sup>	Recommended DMx size (width x length) and space		
	<b>Rectangle (P&amp;R Fill) (follow the most update Reference flow)</b>		<b>Square (Utility Fill)</b>
	<b>Width x Length/Space</b>	<b>DMx to Mx space</b>	<b>Width x Length</b>
<b>M1 and Mx</b>	0.32x1~0.32x6/0.52	0.61	0.6x0.6~3x3
<b>Mn and MD</b>	0.6x1~0.6x10/1.08	1.17	1x1~3x3
<b>My and MD</b>	0.4x1~0.4x10/0.72	0.78	1x1~3x3
<b>UTM</b>	3x3~3x10/3	3	3x3

**DMx**

## 9.4 Dummy Pattern Fill Usage Summary

This section is divided into the following sections:

- Dummy pattern filling requirements
- Recommended flow for dummy pattern filling
- Blockage layer (ODBLK/POBLK/DMxEXCL) requirements and recommendations
- Dummy pattern filling guidelines
- Mask revision guidelines
- Dummy pattern re-fill evaluation flow chart

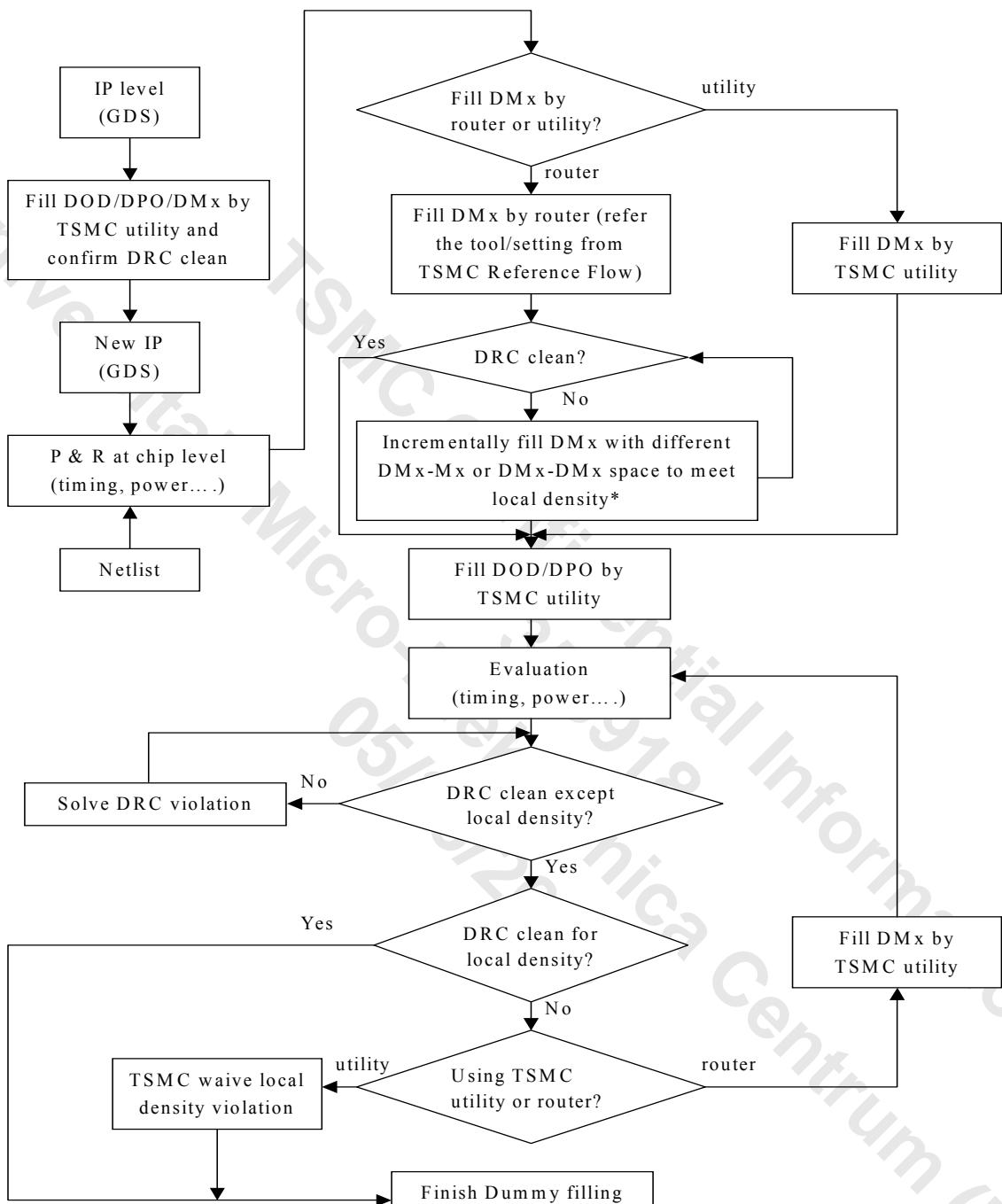
### 9.4.1 Dummy Pattern Filling Requirements

#### 1. OD/PO/Metal pattern density requirements

	Local Density Range	Window check size	Whole Chip Density Range
<b>OD</b>	20%~80% for Core region 20%~90% for I/O region	150 μm * 150 μm	25%~75%
<b>Poly</b>	NA	NA	14%~50%
<b>Metal</b>	≤ 90% for M1/Mx/Mn/My/MD	20 μm * 20 μm	NA
	15%~70% for M1/Mx 20%~80% for Mn/My/MD/UTM	50 μm * 50 μm for 15%/20% 100 μm * 100 μm for 70%/80%	NA

2. **DOD/DPO/DMx requirement:** The DOD/DPO/DMx must be filled, even if the local or chip density has already met the density rules (OD.DN.1/OD.DN.2/OD.DN.3/PO.DN.1/PO.DN.2/Mx.DN.1/Mx.DN.2/Mx.DN.3).
3. **Density requirement:** It is recommended that you use the TSMC auto-fill utility to generate dummy fill patterns.  
If you use TSMC's auto-fill utility to fill DOD and DMx, TSMC will waive the low density rule violations (OD.DN.2, OD.DN.3, Mx.DN.1, and Mx.DN.3). Both the local density rules and chip density rules must be met if TSMC's auto-fill utility is not used to generate the DOD/DPO/DMx fill.
4. **Tool recommendation:** It is recommended to fill dummy patterns using P&R dummy fill (for DMx only) with TSMC provided settings or using the TSMC's auto-fill utility.  
The TSMC auto-fill utility can fill patterns uniformly. It is structurally and hierarchically optimized to provide maximum yield and manufacturability improvement with minimum perturbation to the circuit.

## 9.4.2 Recommended Flow for Dummy Pattern Filling



\* If incrementally fill DMx is done many times, it still can't meet local density, please fill DMx by TSMC utility.

## 9.4.3 Blockage Layer (ODBLK/POBLK/DMxEXCL) Requirements and Recommendations

- Density requirement:** For any area covered by a blockage layer, it is especially critical to meet the local density rules.

Blockage layers specify sensitive regions (by recommendation or requirement), and P&R dummy fill(for DMx only) or the TSMC auto-fill utility does not fill dummy patterns for these regions. For details, please refer to the following sections in this chapter: "Dummy OD Rules," Dummy Poly Rules," and "Dummy Metal Rules."

Circuit	Blockage Layer		
	ODBLK	POBLK	DMxEXCL
RF application circuit	Must	Must	Must
Pad metal area for high frequency signals	Must	Must	Must
SRAM block and bit cell area	Recommended	Recommended	Must (M1 at least)
Analog block (ADC/DAC/PLL, and so on)	Must	Must	Recommended

- RF circuits:** Draw a blockage layer that covers the entire RF circuit. Designers should consider the signal coupling impact and keep a suitable distance between the RF circuits and the blockage layer edge.
- High frequency signal pads:** Draw blockage layers that are coincident with the outer edge of the metal pads.
- Other sensitive regions:** Draw a blockage layer that covers the other sensitive regions, including the SRAM function block and bit cell array, analog circuits (DAC/ADC/PLL), and so on.

- Areas excluded from certain dummy fill:** Don't put any dummy patterns into the following regions:

- Metal fuse (FW)/L target region (LMARK): DOD/DPO/DMx
- Well resistor under STI region (NWDMDY): DOD
- CBM region: DMx (if CBM between Mx+1 and Mx)
- INDDMY region: DOD/DPO/DMx
- LOGO region: DOD/DPO/DMx
- Seal ring /CDU /chip corner stress relief pattern region: DOD/DPO/DMx

The TSMC utility will not add dummy patterns into these regions unless the correct dummy layer is specified, or the correct option is turned on (for CBM and chip corner).

The ODBLK/POBLK/DMxEXCL covered areas should not cover or overlap the above areas for DRC reasons.

## 9.4.4 Dummy Pattern Filling Guidelines

### 1. Dummy pattern filled by P&R dummy fill (for DMx only) or TSMC's dummy fill utility.

Put all relevant layers (MUST and OPTION listed in the following table) into one GDS file. If the OPTION layers are not ready to tape out, draw the blockage layer to avoid dummy pattern fill. (For example, if FW is not ready to tape out when making an OD mask, draw FW into ODBLK to exclude DOD filling.)

Layer ID	Description	Dummy Pattern		
		DOD	DPO	DMx (x=1,2,3,4,5,6,7,8,9,D)
OD	Diffusion	MUST	MUST	
PO	Poly	MUST	MUST	
NW	N-well	MUST		
Mx	x=1,2,3,4,5,6,7,8,9,D			MUST
FW	Fuse window	OPTION	OPTION	OPTION
LMARK	L-mark	OPTION	OPTION	OPTION
CBM	Capacitor bottom metal			OPTION
NWDMY	N-Well resistor	OPTION		
INDDMY	Inductor dummy layer	OPTION	OPTION	OPTION
ODBLK	DOD blockage layer	OPTION		
POBLK	DPO blockage layer		OPTION	
DMxEXCL	DMx blockage layer			OPTION
LOGO	Product labels	OPTION	OPTION	OPTION

2. **Dummy pattern geometry (DOD/DPO/DMx) generated by P&R tool or TSMC utility:** You must place this fill geometry in a reserved layer (data type 1 as default).
3. **Dummy pattern generated by a non-TSMC utility:** If the auto-fill utility is not provided by TSMC, it must meet the DOD/DPO/DMx rule. Also, keep this fill geometry in a reserved layer (data type 1 as default).
4. **CAD layer usage:** If dummy patterns and active patterns have different GDS layers and data types (such as data type 0 and 1), the dummy patterns should follow the DOD/DPO/DMx rules.

If dummy geometry and active circuit geometry are placed on the same GDS layers and data types (such as data type 0), the dummy patterns should follow the appropriate OD/PO/Mx rules. Please note that placement of dummy geometry on the same CAD layer as circuit geometry will result in longer mask making cycle times.

## 9.4.5 Mask Revision Guidelines

When masks or layouts are revised, re-evaluate to modify the filled dummy patterns.

Layer ID	Dummy Pattern		
	DOD	DPO	DMx (x=1,2,3,4,5,6,7,8,9,D)
1 OD	○	✓	✗
2 PO	✓	○	✗
3 NW	✓	✗	✗
4 Mx (x=1,2,3,4,5,6,7,8,9,D)	✗	✗	○
5 FW	✓	✓	✓
6 LMARK	✓	✓	✓
7 CBM	✗	✗	✓
8 NWDMY	✓	✗	✗
9 INDDMY	✓	✓	✓
10 ODBLK	✓	✗	✗
11 POBLK	✗	✓	✗
12 DMxEXCL (x=1,2,3,4,5,6,7,8,9,D)	✗	✗	✓
13 LOGO	✓	✓	✓
14 DOD	○	✓	✗
15 DPO	✓	○	✗

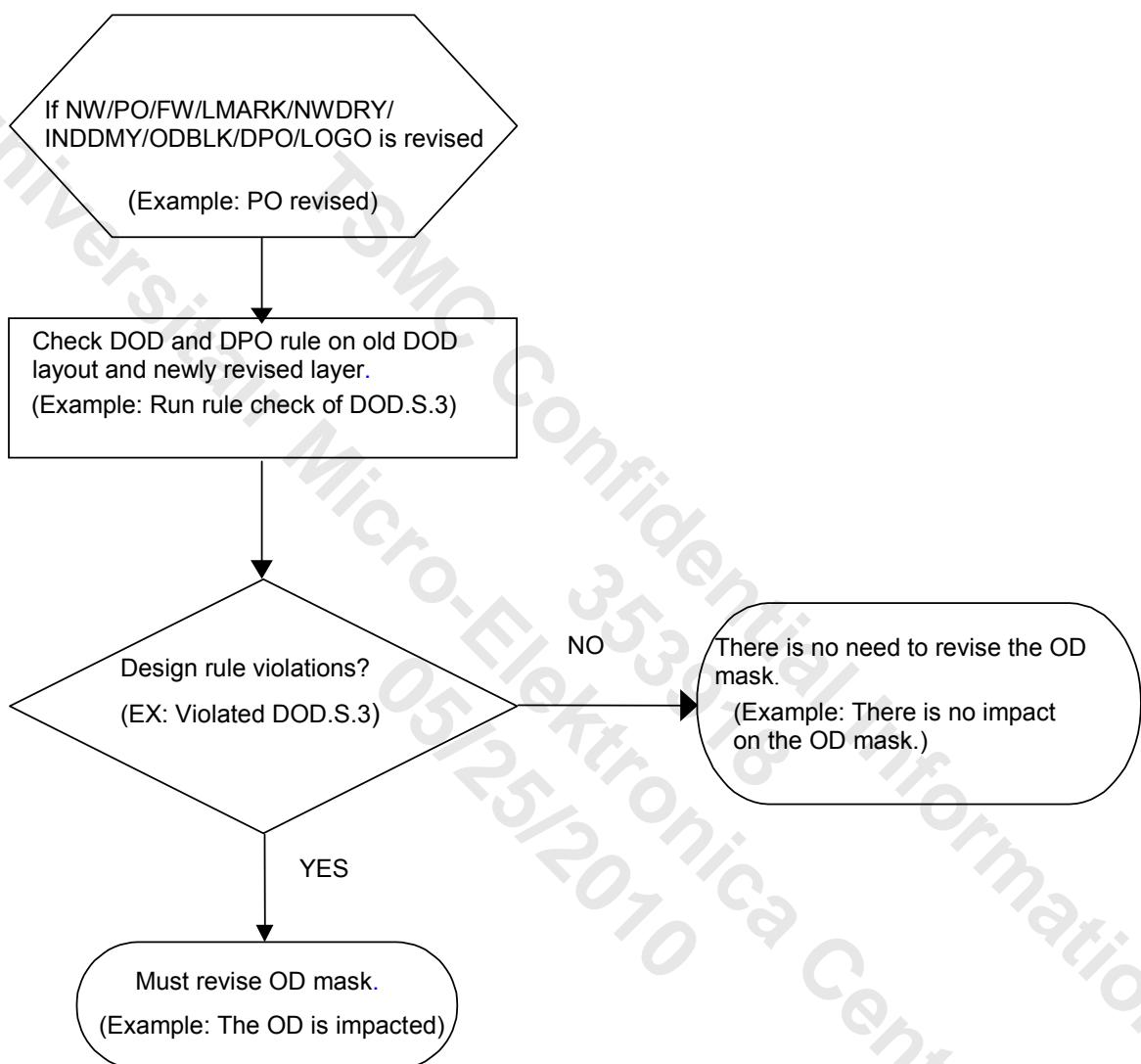
○ : Needs mask revision

✓ : Evaluate mask revision

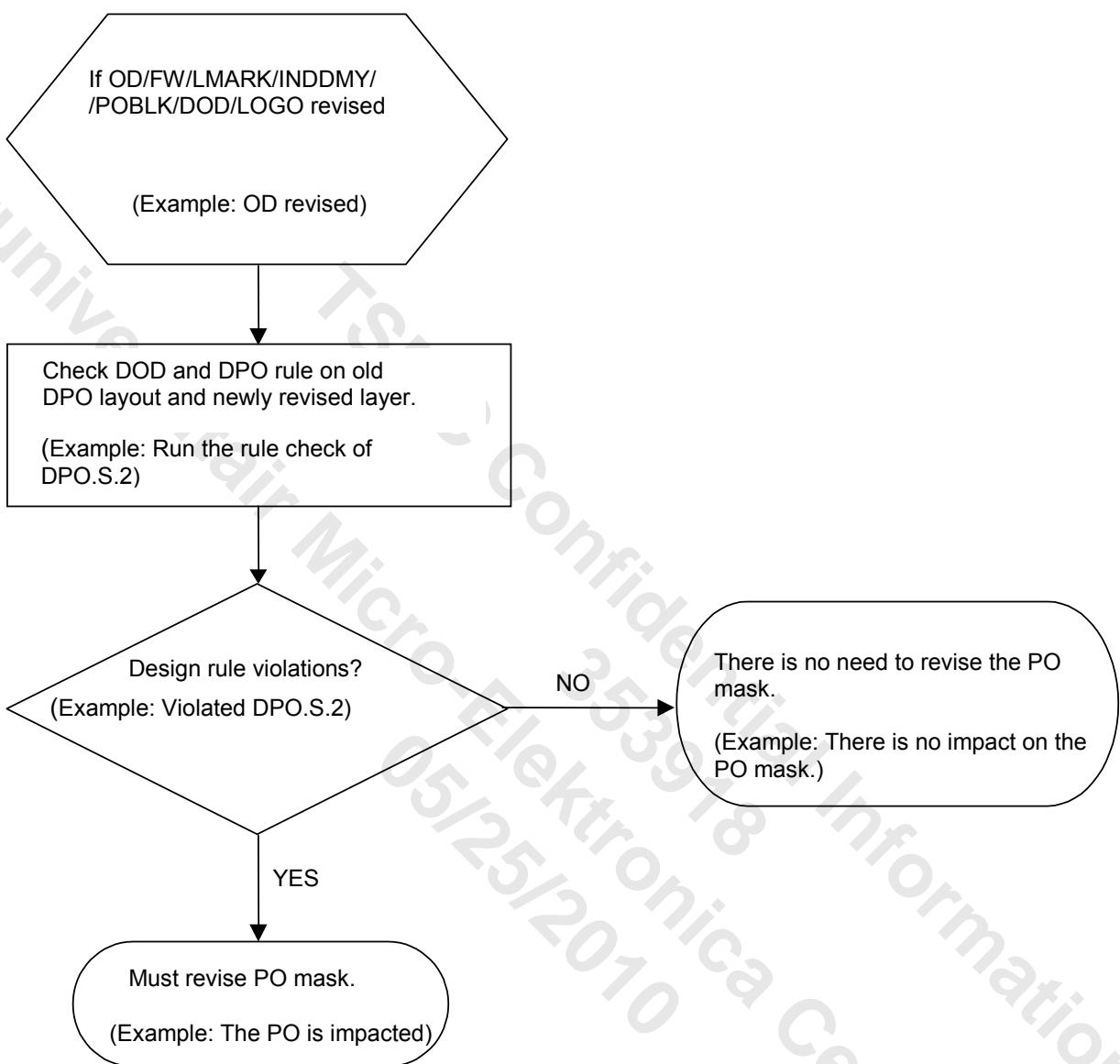
✗ : Doesn't need mask revision

## 9.4.6 Dummy Pattern Re-fill Evaluation Flow Chart

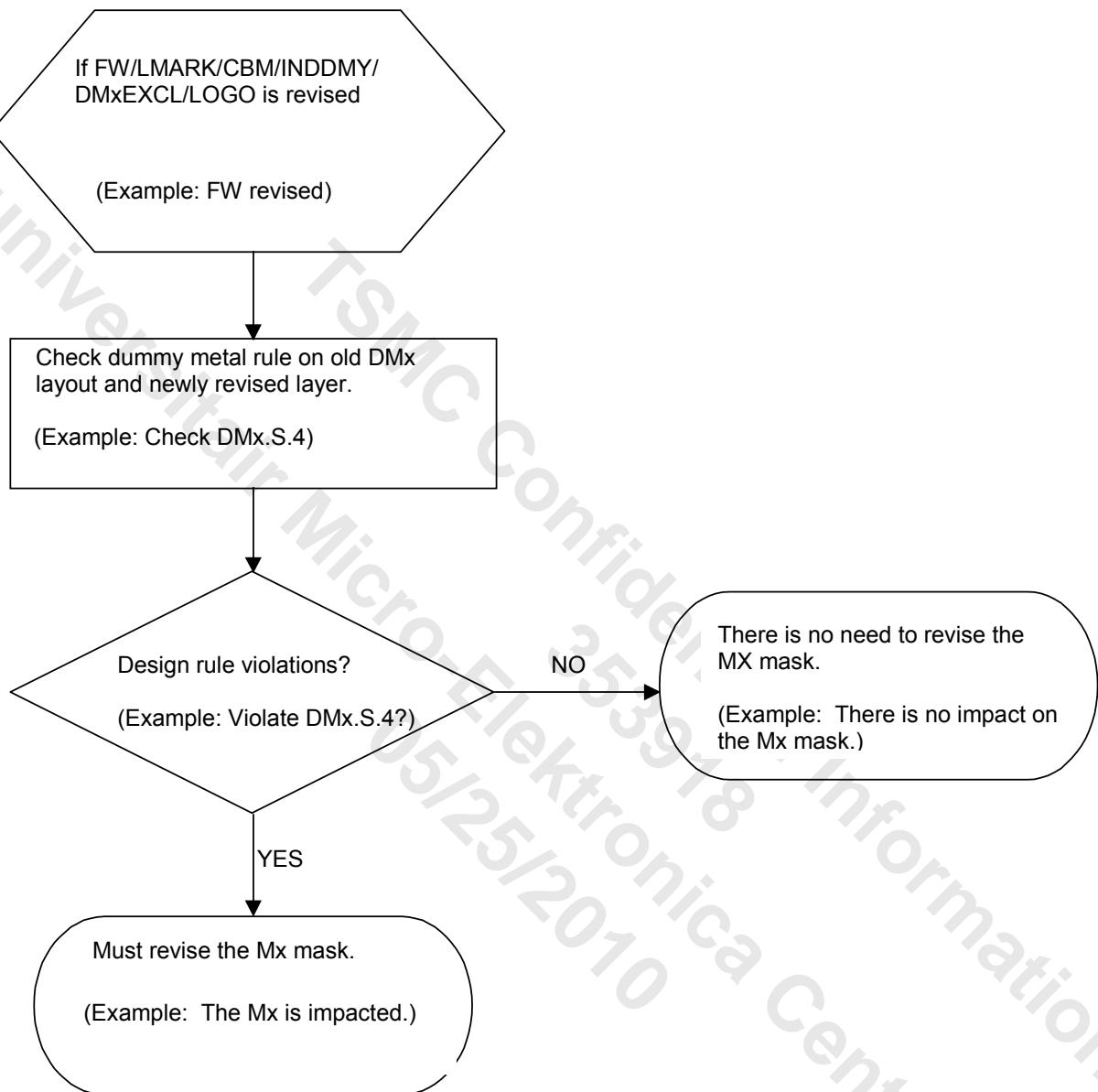
### OD Mask Revision Decision Flow



## PO Mask Revision Decision Flow



## Mx/My/Mn Mask Revision Flow



# 10 Design For Manufacturing (DFM)

This chapter provides information about the following topics:

- 10.1 Layout guidelines for yield enhancement
- 10.2 DFM recommendations and guidelines summary
- 10.3 Mechanical and thermal guidelines for FCBGA
- 10.4 MFU optimization kit

## 10.1 Layout Guidelines for Yield Enhancement

This section provides guidelines for layout optimization to minimize certain potential and unnecessary yield or timing loss under the condition that they introduce no area penalty.

For a given chip design, first and foremost, efforts should be made to achieve as small a die size as possible. The guidelines should not be used indiscriminately, which could result in unnecessarily large chip sizes.

This section is divided into the following topics:

- Layout tips for minimizing critical areas
- Guidelines for optimal electrical model and silicon correlation
- Guidelines for mask making efficiency

### 10.1.1 Layout Tips for Minimizing Critical Areas

Defects are variable in size and therefore follow a size distribution. A *critical area* of a given layout is an accumulative area that is susceptible to certain failures (shorts or opens) caused by defects of a certain size. For example, although the total occupied areas are the same in panels A and B of Figure 10.1.1, the wires in layout A are more vulnerable to defect-induced shorts because they have a larger critical area.

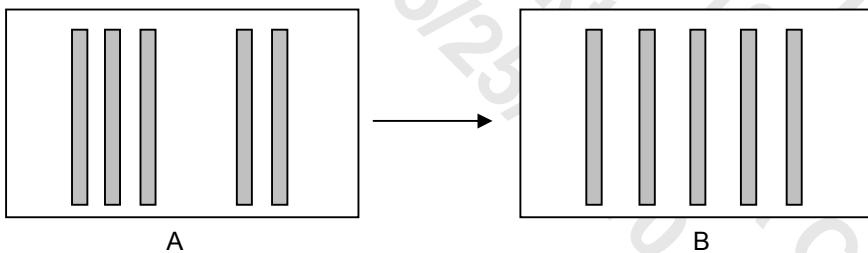


Figure 10.1.1 Layout Examples of Critical Areas

#### 1. Space out the wiring.

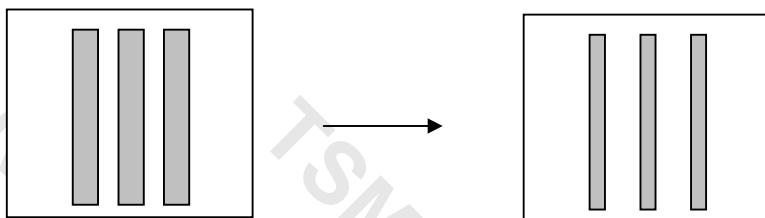
Spacing out the wiring, either using Wire Spreading at P&R stage or manually layout modification at cell level, to take advantage of an empty space can reduce the critical area. This practice has additional benefits:

- o It can reduce wire cross coupling.
- o It can reduce the possibility of pattern short.
- o It can evenly distribute the local pattern density, thereby creating less variation in wire Rs.

## 2. Reduce the probability of wiring shorts.

The critical area plays a role in the yield of a given design, but so does the rate of failure that corresponds to the critical area. Manufacturing experience indicates that a wiring short circuit is a more frequent problem than an open circuit.

- o Give priority to increasing wiring space for conductors of non-minimum wiring pitch, second only to wire resistance or EM considerations. Refer to Figure 10.1.2.



**Figure 10.1.2 Reduced Probability of Wiring Shorts**

- o For long and parallel metal or poly lines use a larger space.
- o Avoid the use of redundant wiring, except for reliability or performance considerations.
- o Draw wires in an orthogonal fashion.
- o Avoid leaving small jogs, especially in the corner areas where metal spacing is at a minimum.
- o Avoid using 45-degree turns, except for very wide metal buses, where the length of the 45-degree portion should be sufficiently large.

## 3. Reduce the risk of open silicided wire or high resistance silicided wire.

To avoid a potential silicide break related to an open circuit or high resistance in narrow lines of poly or OD:

- o Do not use a long narrow width poly conductor, if possible, as a means of local interconnection. The length of un-contacted narrow width poly should be kept to a minimum.
- o If possible, do not use a narrow width OD conductor as a means of interconnection.
- o Avoid a butted N+OD/P+OD interface in a narrow OD.
- o Use a sufficient number of contacts when a narrow OD strip is used for substrate tapping.

## 4. Reduce the probability of a contact or via open circuit.

Open and soft open (excessively high  $R_c$ ) of a single contact or via are usually a yield bottleneck, given their sheer number in a chip. While the manufacturer strives to bring down the failure rate as low as possible, a designer can contribute to further reduction of the probability.

Whenever possible, include redundant vias and contacts for the following benefits:

- o Reduces the probability of an open circuit
- o Reduces via and contacts resistance and potential variation.
- o Potentially increases via stress migration immunity

## 5. Reduce the probability of open vias in a single-via stack.

Whenever possible, use a larger than minimum sized island metal for stacking a single via. This reduces the risk of via resistance variation or open vias.

## 10.1.2 Guidelines for Optimal Electrical Model and Silicon Correlation

The following sections offer recommended practices to minimize the deviation of processed hardware from electrical models.

### 10.1.2.1 Transistors

1. **Avoid layout styles that may contribute to silicon-to-model deviation.**
  - o Avoid using narrow-width devices and short channel device if they require high precision, such as current source device.
- Due to critical dimension variations in channel length and channel width, the electrical properties of narrow-width devices and short channel devices vary more than those of larger devices.
- Poly or OD corner rounding may impact the device length or width critical dimension, primarily in narrow width devices ( $W < 0.2 \mu\text{m}$ ). These DFM Action-Required rules, PO.S.5® and PO.S.6®, should be followed to eliminate this effect while  $W > 0.2 \mu\text{m}$  and  $< 0.5 \mu\text{m}$ .
  - o Source or drain contacts should be placed symmetrically wherever possible. Avoid using single source or drain contacts on large width devices. Please refer to CO.R.5g.
  - o Use the recommendation from DFM recommendation CO.EN.1® regarding sufficient OD-to-contact overlap.  
The benefits of sufficient OD-to-contact overlap are less variation of contact resistance and the avoidance of potentially excessive drain or source leakage.
  - o Use uniform poly and OD densities across a design.  
The poly and OD densities in the neighboring area could affect the gate critical dimension. Although the post-layout insertion of dummy OD, or dummy poly, or both, may patch some empty spaces, it is best to avoid the problem with careful planning and space filling at the macro levels of layout design initially. Please refer to these rules in Chapter 9: "DOD Rule," "DPO Rule," "Dummy Pattern Fill Usage Summary" and also 10.1.2.1.1: "Improvement of poly CD uniformity."
2. **Be aware that thin oxide gate leakage of the 90nm process is higher than that of previous generations.** Its impact on the functionality of a circuit, which uses thin oxide transistors and/or capacitors and/or MOS varactors, must be taken into account by using a proper SPICE model that contains the leakage components.
3. **Pay attention to the leakage current for narrow-width devices with a low- $V_t$  option.**  
Please consult the SPICE model for detailed information.
4. **Pay attention to the unexpected leakage current from floating gate**  
Please tie unused input gates to the known potential. Thus, leakage current can be estimated accurately by circuit simulation. For example, avoid floating input gates in the spare cells (ECO cells).
5. **Device behavior is influenced by layout style possibly due to stress distribution induced by STI/OD edge.** Designer may need to take this length of OD (LOD) effect into consideration during device or cell level design.
6. **Avoid using asymmetrical or single source/drain CO placement on large device (CO.R.5g).**
7. **For PMOS device, if the NWELL is tied to the source used as an internal AC node, the NWELL total area junction capacitance should be included in the circuit simulation by adding the Well capacitance at the source node.**
8. **Take NWELL sheet resistance into consideration during simulation, to reflect the transient bias variation by adding the Well resistance between source node and substrate node.**

### 10.1.2.1.1 Improvement of poly CD uniformity

Further recommendation for improvement of poly CD uniformity (3-sigma) at small channel length:

1. **Uni-directional poly lines are suggested.** The overall CD uniformity improvement is 0.5nm. The vertical and horizontal poly CD may have 2nm difference in worse case as the poly orientation is different.
  2. **Avoid poly pitch <0.28um to improve CD uniformity.** 0.5nm CD improvement can be achieved. Please refer to DFM Action-Required rule PO.S.2®.
  3. **Reduce sparse poly gate count. Avoid to draw a PO gate (channel length  $\leq 0.12 \mu\text{m}$ ) > 1.0um away from nearby PO or dummy PO (S2, S3 in figure 10.1.3).** 0.5nm improvement can be achieved.
    - o **Insert dummy PO surrounding existing PO gate if this PO gate is the nearest one to cell edge and is > 0.5um away from cell edge.** (S1, S3 in figure 10.1.3)
    - o **Recommend to insert dummy PO (or PO) with same parallel run length as of the surrounded PO gate.**
- Hard macro cells are sometimes with placement blockages. However, this blockage would degrade DOD/DPO insertion performance and cause a wide open area.
  - IP designers have to own the responsibility of reducing isolated PO/OD by inserting dummy PO/OD inside the hard macro layout.
  - Either extend hard macro boundary to align with blockage area, or minimize the distance (recommended < 3um) from the blockage edge to the macro cell boundary. Also embed this blockage area in macro cell.
  - Have dummy patterns in the blockage area as default and being verified with library characterization process.
  - Avoid any open area  $\geq 10 \times 10 \mu\text{m}$  without any OD/PO patterns inside in the macro cell area.

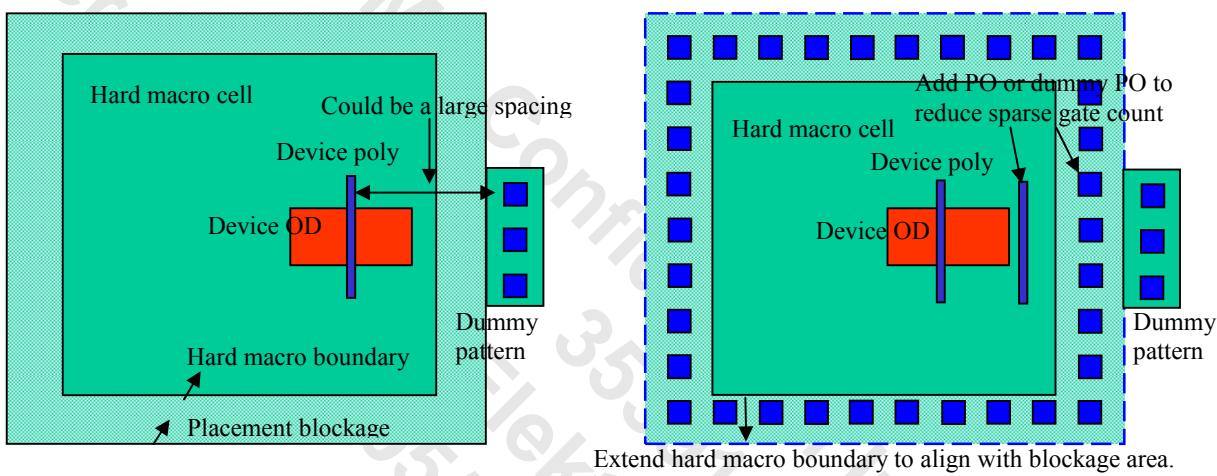
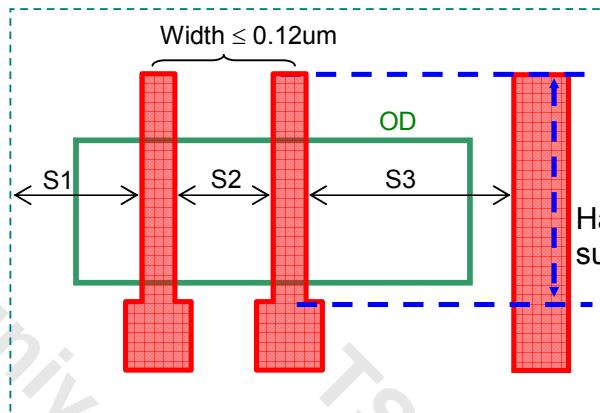


Figure 10.1.3 Reduce sparse poly count

- o Empty area in the standard cell array is not allowed. You needs to use patterned filler cell to insert the empty area of the standard cell array by P&R.
- It is requested to have OD and PO patterns in the filler cell, which provides better gate CD uniformity.
- Need to put dummy PO firstly on sides of both cell edges with <0.5um space to nearby cell edge. A space ( $\geq 0.1 \mu\text{m}$ ) to nearby cell edge is recommended.
- Need to follow the layout rules in DRM
- Use larger PO width in the filler cell. Width  $\geq 0.12\mu\text{m}$  is recommended.
- Put OD and PO uniformly across the whole filler cell. Maximized the length of the OD and PO as much as you can (to match the cell height). If the space was not enough, put PO first.
- Rectangular PO pattern is recommended in the filler cell.
- Dummy fillers of floating and fixed voltage are both acceptable from process point of view. However, the associated implant layers are must if the filler cell is connected to a fixed voltage.
- It is also recommended to put filler cell at the edges of standard cell arrays during P&R.

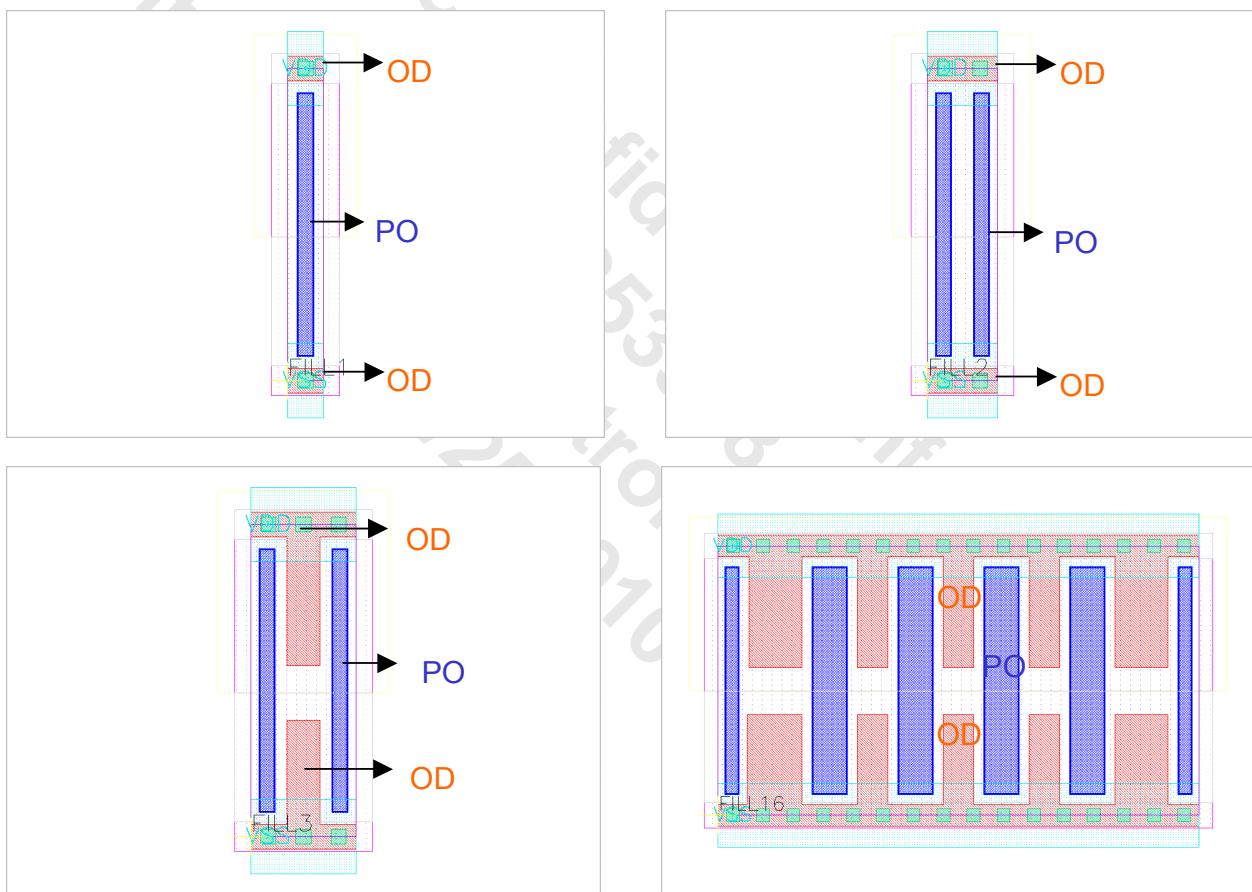
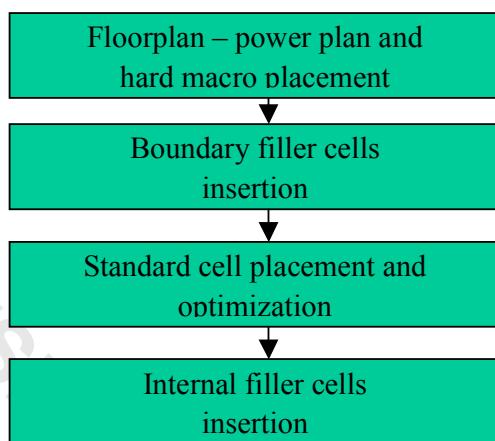


Figure 10.1.4 Example of filler cell

- Guidelines for P&R during filler cell insertion at P&R:

Flow:



Layout with filler cells  
Boundary filler cells

2.1.1.1 Before standard cell placement, inserting fillers on block boundary and macro boundary for occupying the placement locations.

Internal filler cells

2.1.1.2 After standard cell placement, using original filler insertion command.

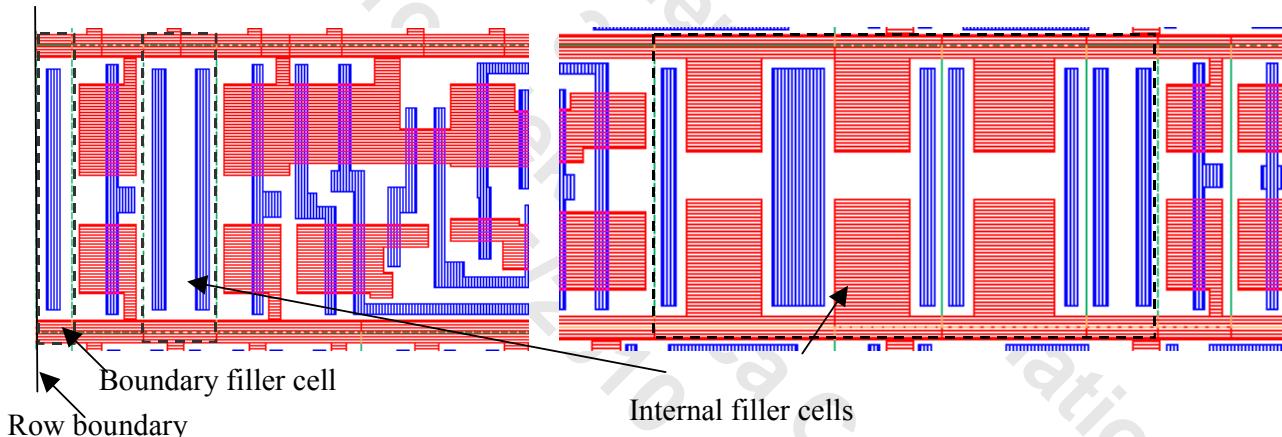


Figure 10.1.5 Layout with filler cells

## 10.1.2.2 Capacitors

**It is strongly recommended NOT to use thin oxide for a de-coupling capacitor with the gate directly tied to power(refer to ESD.12g).** It is recommended to connect the gate to power/ground through a resistor or other tie-up/tie-down circuitry. Please also be aware of the thin oxide gate leakage level.

## 10.1.2.3 Resistors

1. For SPICE simulation accuracy it is strongly recommended to put each OD/poly resistor in a dense area.
2. Avoid using small poly and OD width resistor that is critical in performance.
3. In order to have accurate interconnect RC for timing and power analysis, it is important to extract RC after dummy metal insertion and extract RC with density based metal thickness variation feature enabled.

## 10.1.3 Electrical Wiring

1. **Avoid using minimum-width poly or OD where resistance is critical to the circuit performance.**
2. During IP/marco design, it is important to put certain density margin to avoid the possibility of high density violations (Mx.DN.1, Mx.DN.2, Mx.DN.3) during placement. It may have unexpected violation during the IP/marco placement due to the environment, even if the IP/marco alerady pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.
3. **Wherever possible, use two or more narrower metal buses to replace a single bus that uses the maximum width.**
4. **Maintain uniform metal density to minimize wire sheet resistance variation and maximize the associated photo process window. Target the local density to the middle range of the specification, avoiding the two extreme ends.**
5. **Need dummy insertion in the library/IP/Macro blockage area:**
  - o Either extand hard macro boundary to align with blockage area or minimize the distance (recommended  $\leq 3\text{um}$ ) from the blockage edge to the macro cell boundary. Also embed this blockage region in macro cell.
  - o Have dummy patterns (DOD/DPO/DMx) in the blockage area as default and being verified with library characterization process.
  - o Need to re-define I/O pin for P&R at new marco cell boundary if you push out hard macro boundary to align with blockage area.
  - o Avoid any open area  $\geq 3 \times 3 \text{ um}$  without any metal patterns inside in the macro cell area (refer to Mx.DN.1®).

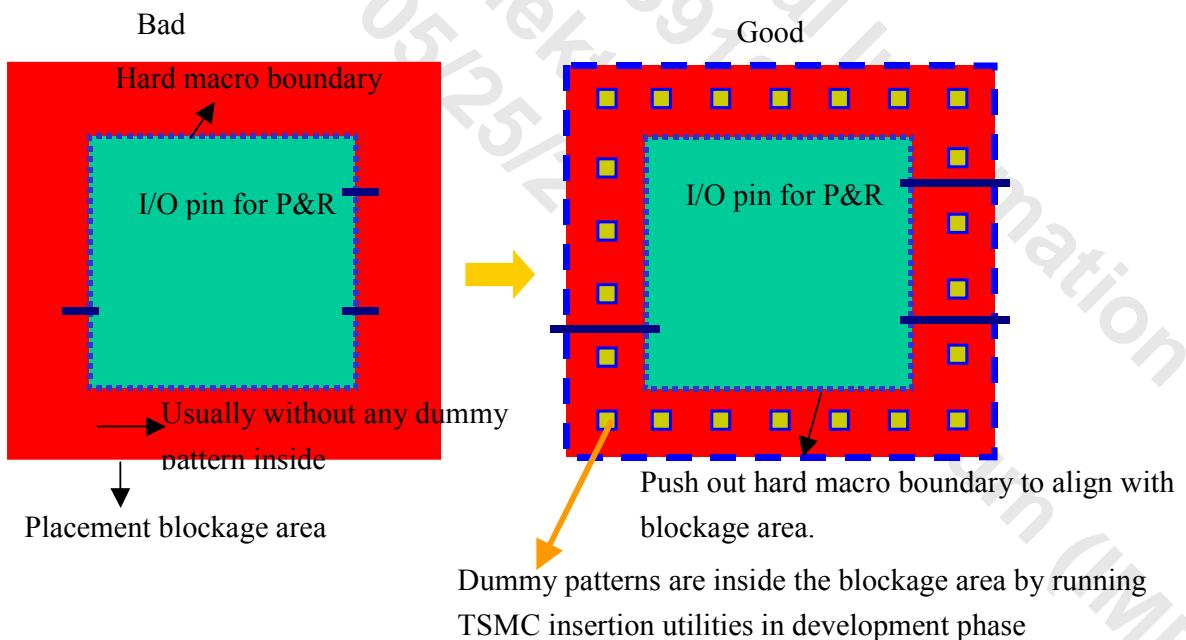


Figure 10.1.6 Dummy insertion for library/IP/Macro blockage area

## 10.1.4 Guidelines for Mask Making Efficiency

Please refer to these Chapter 3 sections:

- “Design Geometry Restrictions”
- “Design Hierarchy Guidelines”

## 10.1.5 Guidelines for Low Power Designs

For low power design methodologies, please refer to TSMC Reference Flow:

1. TSMC Reference Flow V6.0 includes:
  - Multiple voltage scaling island (dynamic power and leakage optimization)
  - Fine grain MTCMOS (leakage optimization)
  - TSMC low power library
2. TSMC Reference Flow V5.0 includes:
  - Single core voltage island (dynamic power and leakage optimization)
  - Back bias (leakage optimization)
3. TSMC Reference Flow V4.0 includes:
  - Multi-Vt (leakage optimization)

## 10.2 DFM Recommendations and Guidelines Summary

- Please use the following advisory/recommended dimensions and guidelines whenever possible, unless doing so impacts chip size or performance.
- DFM does not have to comply to the advisory/recommendation value completely. Any change even by one grid helps.
- By using DFM recommendations and guidelines, higher precision of models, better reliability, lower timing, process or yield variation may be expected.
- If your circuit has concern about the DFM Action-Required rules (10.2.1) and Recommendations (10.2.2), TSMC DRC deck can help you to flag the violations. DFM DRC deck is bundled in the TSMC logic DRC deck. The following 2 methods can specify the region to run DFM recommendations in DFM DRC deck. Please also refer to the “User Guide” in the DFM deck

### 1. Dummy layer:

- RRuleRequire(CAD layer: 182;1): for the DFM Action-Required Rules
- RRuleRecommend(CAD layer: 182;2): for the DFM Recommendations

### 2. Cell selection based on the following variables:

- CellsForRRuleRequired
- CellsForRRuleRecommended
- ExclCellsForRRuleRequired: only check the cells in the variable.
- ExclCellsForRRuleRecommended: don't check the cells in the variable.

### 10.2.1 Action-Required Rules

Using minimum dimension of the following rules may have influence on the electrical characteristics (e.g. Idsat) of a related device. It is required that either the concerned influence be taken into account in a circuit electrical design if a dimension is less than the advisory point, or the advisory value be used. DFM LPE in the LVS is provided for Action-Required Rules to get optimized device parameters and simulation result.

No.	Description		Advisory	Min. Rule
PO.S.2®	Recommended GATE space in the same OD to avoid Isat variation	≥	0.2	0.15
PO.EX.2®	Recommended OD extension on PO to avoid Isat degradation. • LPE model can support the simulation accuracy while channel width $\leq 2\mu\text{m}$ . • Full and symmetrical contact placement are recommended at both source and drain side, especially for the device width $> 2\mu\text{m}$ .	≥	0.23	0.15
PO.S.5®	Recommended PO space to L-shape OD when PO and OD are in the same MOS [channel width ( $W$ ) $\geq 0.2 \mu\text{m}$ and $< 0.5 \mu\text{m}$ ] for stable Isat (avoid corner rounding effect)	≥	0.1	0.05 (PO.S.4)
PO.S.6®	Recommended L-shape PO space to OD when PO and OD are in the same MOS [channel width ( $W$ ) $\geq 0.2 \mu\text{m}$ and $< 0.5 \mu\text{m}$ ] for stable Isat (avoid corner rounding effect)	≥	0.1	0.05 (PO.S.4)

## 10.2.2 Recommendations

Using minimum dimension of the following rules is okay. If a non-minimum recommendation is used, however, the variation of the related electrical parameter (e.g. contact or via  $R_c$ ) can be minimized and yield benefit may be expected. It is recommended that the DFM Recommendations be used wherever possible

No.	Description	Recommended	Min. Rule
OPC.R.1®	It is recommended that any edge of length $< 1.0 \times$ minimum width cannot have another adjacent edge of length $< 1.0 \times$ minimum width for OPC friendly layout.	-	-
OPC.R.3®	Recommended 45-degree edge length of all layers for OPC friendly layout.	$\geq 0.5$	-
DNW.EN.1®	Enclosure by NW for better noise isolation	$\geq 1.5$	-
OD.W.2®	Recommended width of MOS ( $< 1.2V$ ) [for core device] for stable $I_{sat}$ (avoid corner rounding effect)	$\geq 0.2$	0.12
OD.S.1®	Recommended minimum OD space to reduce short possibility cause by particle	$\geq 0.18$	0.14
OD.S.6®	Recommended space to OD [ OD area $> 4,000,000 \mu\text{m}^2$ ]	$\geq 0.35$	0.14
NWROD.R.1®	Recommend length $\geq 20\mu\text{m}$ , and square number (length/ width) $\geq 5$ in NW resistor within OD for SPICE simulation accuracy. DRC can not check square number.		
NWRSTI.R.1®	Recommend length $\geq 20\mu\text{m}$ , and square number (length / width) $\geq 5$ in NW resistor under STI for SPICE simulation accuracy. DRC can not check square number.		
OD2.W.2®	Width of {OD2 OR (NW OR NT_N)} to avoid small pattern in mask making	$\geq 0.62$	
OD2.S.5®	Space of {NW NOT OD2} to avoid small pattern in mask making	$\geq 0.62$	
OD2.S.6®	Space of {NW AND OD2} to avoid small pattern in mask making	$\geq 0.62$	
OD2.S.7®	Space of {OD2 NOT (NW OR NT_N)} to avoid small pattern in mask making	$\geq 0.62$	
PO.S.1®	Recommended minimum interconnect Poly space to reduce the short possibility caused by particle	$\geq 0.18$	0.14
VAR.A.1®	Recommended area of {gate AND VAR} for SPICE simulation accuracy. In SPICE model, $0.4\mu\text{m} \times 1.6\mu\text{m}$ is used for minimum area of {gate AND VAR}.	$\geq 0.64$	-
CO.EN.1®	Recommended CO enclosure by OD to avoid high $R_c$	$\geq 0.07$	0.04
CO.EN.3®	Recommended CO enclosure by PO [at least two opposite sides] to avoid high $R_c$	$\geq 0.07$	0.05
M1.S.6®	Recommended space between two non-M1 regions [ one of the non-M1 area $> 4,000,000\mu\text{m}^2$ . Non-M1 region is defined as { NOT (M1 OR DM1)} e.g. enlarge the metal width $\geq 0.35$ for the guard ring design. ]	$\geq 0.35$	
M1.EN.2®	Recommended M1 enclosure of CO [at least two opposite sides] to avoid high $R_c$	$\geq 0.07$	0.05
M1.EN.3®	Recommended M1 [width $>0.6\mu\text{m}$ ] enclosure of CO to avoid high $R_c$	$\geq 0.07$	0.025
M1.DN.3®	Metal density range within DM1EXCL over any $10 \mu\text{m} \times 10 \mu\text{m}$ area with $3 \mu\text{m} \times 3 \mu\text{m}$ open area (checked by stepping in $5 \mu\text{m}$ increments) for CMP uniformity. Please refer to the "Dummy Metal Rules" section in Chapter 9 for detail dummy metal rules.	$\geq 20\%$	

No.	Description	Recommended	Min. Rule
VIAx.EN.1®	Recommended VIAx enclosure by Mx or M1 [VIA1 count <=2 in the region of (M1 AND M2) or VIAx count <=2 in the region of (Mx and Mx+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥ 0.05	0.005
VIAx.EN.2®	Recommended VIAx enclosure by Mx or M1 [at least two opposite sides] [VIA1 count <=2 in the region of (M1 AND M2) or VIAx count <=2 in the region of (Mx and Mx+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥ 0.08	0.05
VIAx.R.8®	Maximum consecutive stacked VIAx layer, which has only one via for each VIAx layer, to avoid high Rc. (Example: VIA1~VIA4, VIA2~VIA5, VIA3~VIA6. This recommendation does not apply to top via. It is allowed to stack from VIA3 to VIA8 because VIA7 and VIA8 are top via.)	≤ 4	
Mx.W.4®	Recommended Mx width [Mx on (((Mx-1 OR DMx-1) with space ≥ 5x5μm) sizing 1)] for CMP uniformity	≥ 0.16	0.14
Mx.S.6®	Recommended space between two non-Mx regions [ one of the non-M1 area > 4,000,000μm^2. Non-Mx region is defined as { NOT (Mx OR DMx)} e.g. enlarge the metal width ≥ 0.35 for the guard ring design.	≥ 0.35	
Mx.EN.1®	Recommended Mx enclosure of VIAx-1 [VIAx-1 count <=2 in the region of (Mx-1 AND Mx)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥ 0.05	0.005
Mx.EN.2®	Recommended Mx enclosure of VIAx-1 [at least two opposite sides] [VIAx-1 count <=2 in the region of (Mx-1 AND Mx)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥ 0.08	0.05
Mx.DN.3®	Metal density range within DMxEXCL over any 10 μm x 10 μm area with 3 μm x 3 μm open area (checked by stepping in 5 μm increments) for CMP uniformity. Please refer to the "Dummy Metal Rules" section in Chapter 9 for details about dummy metal rules.	≥ 20%	-
Mx.DN.4®	It is not recommended to have local density > 70% of all 3 consecutive metal (Mx, Mx+1 and Mx+2) over any 50um x 50um (stepping 25) for CMP uniformity, i.e. it is allowed for either one of Mx, Mx+1, or Mx+2 to have a local density ≤ 70%. 1. The metal layers include M1/Mx and dummy metals. 2. The check does not include chip corner stress relief pattern and seal ring.		
Mn.W.3®	Recommended Mn width [Mn on (((Mn-1 OR DMn-1) with space ≥ 5x5μm) sizing 1)] for CMP uniformity	≥ 0.44	0.42
VIAy.EN.1®	Recommended enclosure by Mx or My [VIAy count <=2 in the region of (Mx AND My+1) or VIAy count <=2 in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥ 0.05	0.01
VIAy.EN.2®	Recommended enclosure by Mx or My [at least two opposite sides] [VIAy count <=2 in the region of (Mx AND My+1) or VIAy count <=2 in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥ 0.08	0.05
My.W.4®	Recommended My width [My on (((My-1 OR DMy-1) with space ≥ 5x5μm) sizing 1)] for CMP uniformity	≥ 0.3	0.28
My.S.6®	Recommended space between two non-Mx regions [ one of the non-My area > 4,000,000μm^2 ]. Non-My region is defined as { NOT (My OR DMy)} e.g. enlarge the metal width ≥ 0.35 for the guard ring design.	≥ 0.35	

No.	Description		Recommended	Min. Rule
My.EN.1®	Recommended enclosure of VIAy-1 [VIAy-1 count <=2 in the region of (Mx AND My) or VIAy count <=2 in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥	0.05	0.01
My.EN.2®	Recommended enclosure of VIAy-1 [at least two opposite sides] [VIAy-1 count <=2 in the region of (Mx AND My) or VIAy count <=2 in the region of (My AND My+1)] to avoid high Rc. Please refer to the "Via Layout Recommendations" in the section 4.5.31.	≥	0.08	0.05
CTM.W.1®	Recommended width for SPICE simulation accuracy.	≥	4	-
UTM.EN.3®	Recommended INDDMY enclosure of UTM (inductor) for SPICE simulation accuracy.	≥	50	-
UTM.DN.5®	Maximum density of INDDMY over the whole chip	≤	5%	-
CB.W.4® <sup>U</sup>	Recommended total width of all metal layers connecting with bond pad.	≥	10	-
AP.W.2® <sup>U</sup>	Recommended total width of BUS line [Connect with bond pad]	≥	10	-
UBM.S.4®	Space of two UBM (Maximum) It is recommended not to have isolated bumps, or avoid unnecessarily spare regions.	≤	400	-
UBM.EN.1®	Recommended enclosure by chip edge (Maximum)	≤	300	-
UBM.A.1® <sup>U</sup>	Area (without UBM in the chip center, for test inking requirement. Not necessary for inkless sorting)	≥	750x750	-
UBM.DN.1®	Recommendation for whole chip UBM density	≥	10%	
UBM.DN.3®	Recommendation for maximum density of whole chip NOT {UBM sizing + 200um}	≤	20%	
UBM.R.6® <sup>U</sup>	Recommended size ratio of UBM/Pre-Solder Bump SRO (=C/N) and BGA SRO/Board Pad (=T/O). <b>Ratio=1.05 is preferred.</b> <b>SRO: Solder Resist Opening</b>	≥	0.95	
BP.R.2®	Recommended bump pitch selection according to chip size.	≥	Table 5.2.3.2.2*	
UBM.R.7®	Recommended UBM width selection according to chip size.	≥	Table 5.2.3.2.2*	

VIAx.EN.0®: Recommended enclosure by Mx or M1 is defined by either VIAx.EN.1® or VIAx.EN.2®.

Mx.EN.0®: Recommended enclosure of VIAx-1 is defined by either Mx.EN.1® or Mx.EN.2®.

VIAy.EN.0®: Recommended enclosure by Mx or My is defined by either VIAy.EN.1® or VIAy.EN.2®.

My.EN.0®: Recommended enclosure of VIAy-1 is defined by either My.EN.1® or My.EN.2®.

Table 5.2.3.2.2 Die size to bump pitch, UBM width and bump material selection

Chip Area (mm <sup>2</sup> )	Area≤100	100<Area≤225	225<Area≤400	Area>400
Min. Bump Pitch (um)	150	160	180	200
Min. UBM (um)	80	85	90	100
Bump Composition*	EU, HL	EU, HL	EU	EU

\* EU: eutectic, HL: high lead. For lead free application, please refer to LF design rule.

## 10.2.3 Guidelines

The followings are guidelines regarding layout design practice, although they cannot be quantified. These guidelines should be observed to their maximum in any circuit designs.

No.	Description
OPC.R.2g	It is recommended that you use greater than, or equal to, half of the minimum width of each layer for each segment of a jog.
DNW.R.5g	Recommend not using floating RW unless necessary to avoid unstable device performance. DRC can flag RW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.
NW.R.1g	Recommended not to use floating well unless necessary to avoid unstable device performance. DRC can flag both NW is not with CO in NPOD and PW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.
NWROD.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.
NWRSTI.R.3g	Recommended to use rectangle shape resistor for the SPICE simulation accuracy. DRC can flag {NWDMY AND NW} is not a rectangle.
OD.L.2g <sup>U</sup>	Recommended to limit the maximum interconnect OD length as short as possible to avoid Rs variation by salicidation.
PO.L.1g <sup>U</sup>	Recommended to limit the maximum interconnect PO length as short as possible to avoid Rs variation by salicidation.
CO.S.6g	Recommended to put contacts at both source side and butted well pickup side to avoid high Rs. DRC can flag if the STRAP is butted on source, one of STRAP and source is without CO.
CO.R.1g <sup>U</sup>	Recommend to put {CO inside PO} space to GATE as close as possible to avoid high Rs
CO.R.5g	Recommend using redundant CO to avoid high Rc wherever layout allows 1. Recommended to use double CO or more on the resistor connection. 2. Double CO on Poly gate to reduce the probability of high Rc 3. Recommend putting multiple and symmetrical source/drain CO for SPICE simulation accuracy, especially for the device width >2 μm 4. If it is hard to increase the CO to gate spacing (CO.S.3®) for the large transistor, limit the number of source/drain CO: to have the necessary CO number for the current, and then distribute the CO evenly on the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle) 5. DRC can flag single CO.
VIAx.R.9g VIAy.R.9g	Recommend using redundant vias wherever layout allows to avoid high Rc. Please refer to the “Via Layout Recommendations” in the section 4.5.31. DRC can flag single via.
VIAN.R.5g	Recommend using redundant vias wherever layout allows to avoid high Rc. DRC can flag single via.
Mx.R.2g <sup>U</sup> My.R.2g <sup>U</sup>	For the small space, recommended to enlarge the metal space, by using Wire Spreading function of EDA tool, to reduce the wire capacitance and the possibility of metal short. Please refer to TSMC Reference flow.

No.	Description
VIA <sup>U</sup> An.R.8g <sup>U</sup>	For MIM applications, put as many VIA <sup>U</sup> as possible for both CTM and CBM connections.
UTM.R.1g <sup>U</sup>	Keep placing the INDDMY separately and uniformly cross over a chip
UTM.R.9g <sup>U</sup>	For inductor devices offered in TSMC's SPICE model, a native substrate layer is created under the inductor coil to minimize eddy currents. This layer is specified by NT_N with the exact shape as the INDDMY layer. This NT_N drawn layer adds no process cost and no extra mask and is included in TSMC's PDK and its associated sample layout document.
UBM.R.4g <sup>U</sup>	<p>It is recommended not to put any bump on the top of SRAM, analog, sensitive circuits, and the matching pairs.</p> <ul style="list-style-type: none"> <li>o The circuits should be located at a minimum distance of 60 µm from the bump pad's PM or CBD edge.</li> <li>o It is also recommended to consider UBM.S.4® at the same time.</li> <li>o If bump over SRAM, analog, or sensitive circuit areas is needed, it is recommended to use the ultra-low alpha particle materials in the bump and assembly processes (solder bump, under-fill, pre-solder bump...) to avoid a high Soft Error Rate (SER).</li> <li>o TSMC uses ultra-low alpha particle materials in the solder bump process.</li> </ul> <p>If you could not meet UBM.S.4® and UBM.R.4g at the same time, you can consult TSMC for the layout suggestions.</p>
UBM.R.5g <sup>U</sup>	It is recommended not to place the IO bump pads in the 2 <sup>nd</sup> and 3 <sup>rd</sup> row in the bump array corner, but put Vss, Vdd, or dummy bump pads.

## 10.2.4 Grouping Table of DFM Action-Required Rules, Recommendations and Guidelines

No.	1st priority to implement for yield and performance enhancement	Systematic			Defect	SPICE
		CMP	Litho/OPC	Others		
PO.S.2®			V	V		V
PO.EX.2®				V		V
PO.S.5®			V			V
PO.S.6®			V			V
OPC.R.1®			V			
OPC.R.3®			V			
DNW.EN.1®				V		
OD.W.2®						V
OD.S.1®					V	
OD.S.6®				V		
NWROD.R.1®						V
NWRSTI.R.1®						V
OD2.W.2®				V		
OD2.S.5®				V		
OD2.S.6®				V		
OD2.S.7®				V		
PO.S.1®					V	
VAR.A.1®						V
CO.EN.1®			V			V
CO.EN.3®			V			V
M1.S.6®				V		
M1.EN.2®	V		V			V
M1.EN.3®	V		V			V
M1.DN.3®		V				
VIAx.EN.1®	V		V			V
VIAx.EN.2®	V		V			V
VIAx.R.8®		V				
Mx.W.4®		V				
Mx.S.6®				V		
Mx.EN.1®	V		V			V
Mx.EN.2®	V		V			V
Mx.DN.3®		V				
Mx.DN.4®		V				
Mn.W.3®		V				
VIAy.EN.1®	V		V			V
VIAy.EN.2®	V		V			V
My.W.4®		V				
My.S.6®				V		
My.EN.1®	V		V			V
My.EN.2®	V		V			V
CTM.W.1®						V
UTM.EN.3®						V
UTM.DN.5®		V				
CB.W.4® <sup>U</sup>				V		
AP.W.2® <sup>U</sup>				V		

No.	1st priority to implement for yield and performance enhancement	Systematic			Defect	SPICE
		CMP	Litho/OPC	Others		
UBM.S.4®				v		
UBM.EN.1®				v		
UBM.A.1® <sup>U</sup>				v		
UBM.DN.1®				v		
UBM.DN.3®				v		
UBM.R.6® <sup>U</sup>				v		
BP.R.2®				v		
UBM.R.7®				v		
OPC.R.2g			v			
DNW.R.5g				v	v	
NW.R.1g				v	v	
NWROD.R.3g					v	
NWRSTI.R.3g					v	
OD.L.2g <sup>U</sup>				v		
POL.1g <sup>U</sup>				v		
CO.S.6g					v	
CO.R.1g <sup>U</sup>					v	
CO.R.5g	v				v	v
VIAx.R.9g	v				v	v
VIAy.R.9g	v				v	v
VIAx.R.5g	v				v	v
Mx.R.2g <sup>U</sup>				v	v	
My.R.2g <sup>U</sup>				v	v	
VIAx.R.8g <sup>U</sup>				v		
UTM.R.1g <sup>U</sup>				v		
UTM.R.9g <sup>U</sup>					v	
UBM.R.4g <sup>U</sup>				v		
UBM.R.5g <sup>U</sup>				v		

## 10.3 GDA die size optimization kit

- Gross Die Advisor (GDA) is to optimize die size x-y for both mask field allocation and gross die maximization.
- The function of GDA is based on user input die size, target gross die and TSMC generic fabrication condition to estimate gross die count, and recommend a list of the other die size combination (X / Y) with higher gross die and MFU>65% criterion. Based on GDA result, user can choose the best combination of die size and gross die to meet the project need in the early design phase.
- Use GDA function from TSMC on-line
  - TSMC On-line Directory: Home/Design Portal/Design Assistance/Die Size Planning

### 10.3.1 Recommended GDA criteria MFU>65%

- The benefits from GDA:
  - Simulate gross die count base on initial die size x-y at the early design stage.
  - Advise die size x-y for better gross die count and MFU>65% simultaneously.
- The MFU ratio is calculated by (die size+assembly isolation +sealring+ scribe-line Area) / (maximum scanner field size).

# 11 Layout Guidelines for Latch-Up and I/O ESD

This chapter consists of the following 2 Sections:

- 11.1 Layout rules and guidelines for latch-up prevention
- 11.2 I/O ESD protection circuit design and layout guideline

## 11.1 Layout Rules and Guidelines for Latch-up Prevention

### 11.1.1 Latch-up Introduction

Before latch-up, the parasitic components of an inverter can be modeled as the equivalent circuit in Figure 11.1.1. As the output signal is higher than  $V_{dd}+0.7V$  (overshooting), the bipolar VT2 turns on first. As the output signal is lower than  $-0.7V$  (undershooting), the bipolar LT2 turns on first. The collector of each BJT is connected to the base of the other transistor and can inject the minority carriers to the well to induce a potential difference between PW and Vss, or NW and Vdd, to forward the base to emitter junction of the other transistor (LT1 or VT1), resulting in the other transistor turning on. When both BJT's, which connect to  $V_{dd}$  (VT1) and  $V_{ss}$  (LT1), turn on, the injected minority carrier concentrations are increased higher than the doping concentrations of NW and PW (Figure 11.1.2). Subsequently, NW and PW disappear and a heavy conductivity region creates a low resistance path between  $V_{dd}$  and  $V_{ss}$  (please refer to JH Lee et. al, "The positive trigger lowering effect for latch-up," in IPFA, p. 85, 2004). This may induce a circuit malfunction, and destroy the device in the worst case.

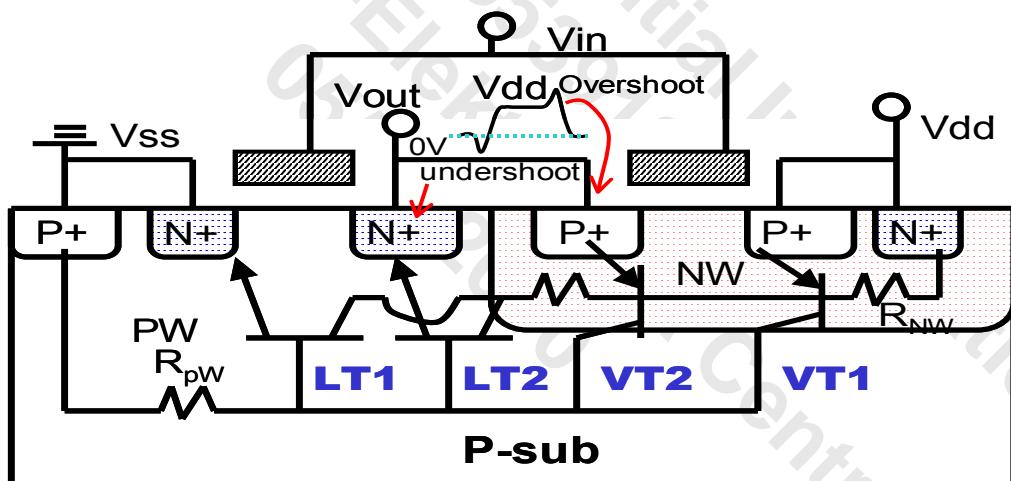
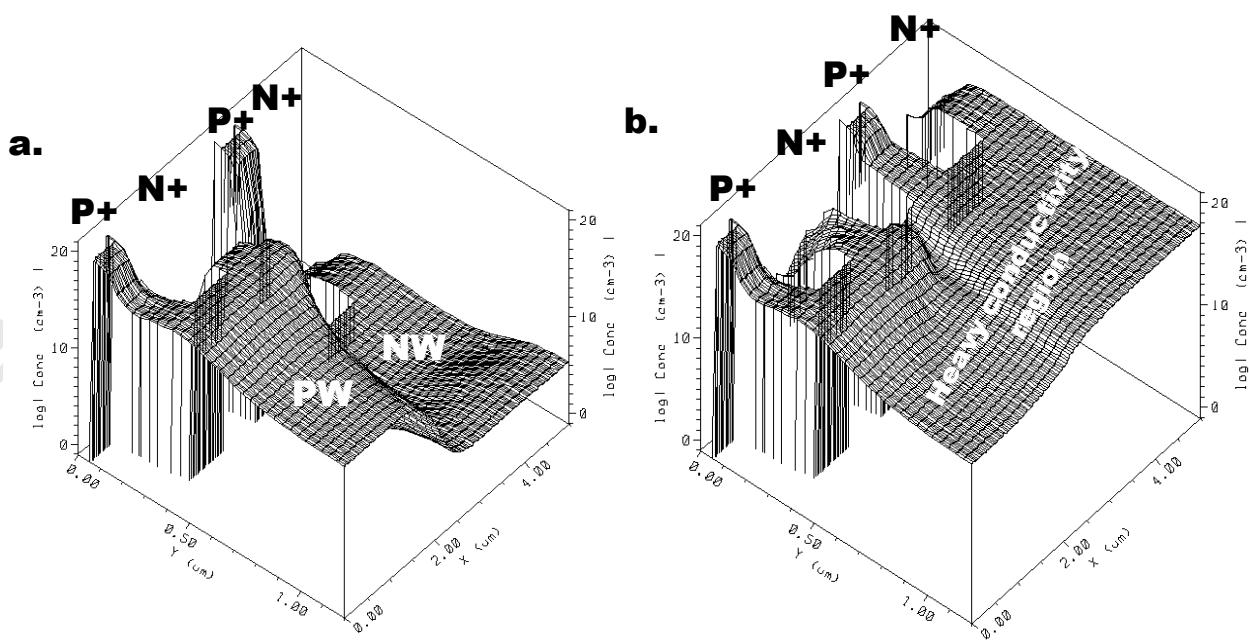
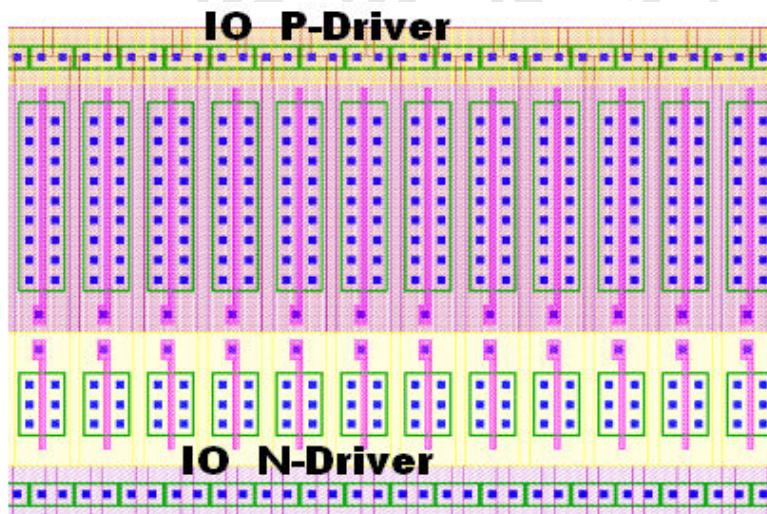


Fig. 11.1.1 Lump element model for an inverter before latch-up



**Fig. 11.1.2 Hole concerations (a) before latch-up, (b) after latch-up**

The latch-up trigger sources often come from the IO Pad, but both IO circuits and internal circuits might cause a latch-up if the layout does not follow the latch-up design rules. The following lists the latch-up failure cases caused by layout rule violations.



**Fig. 11.1.3 LUP.1g violation: (IO without guard-ring)**

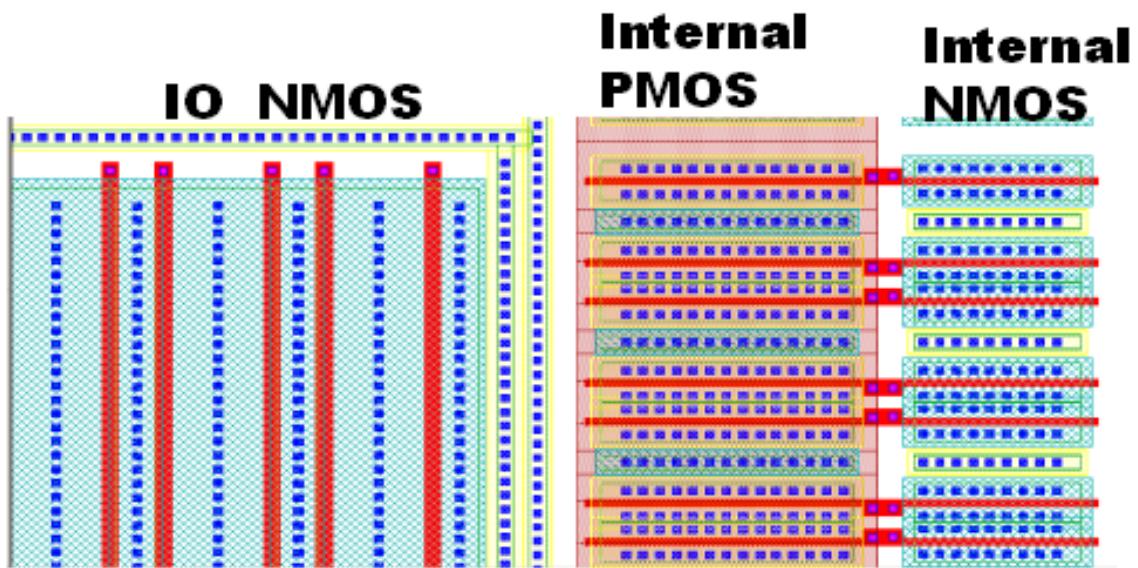


Fig. 11.1.4 LUP.2g violation:  
(Within 20um from IO, N/PMOS in the internal circuit without the guard-ring)

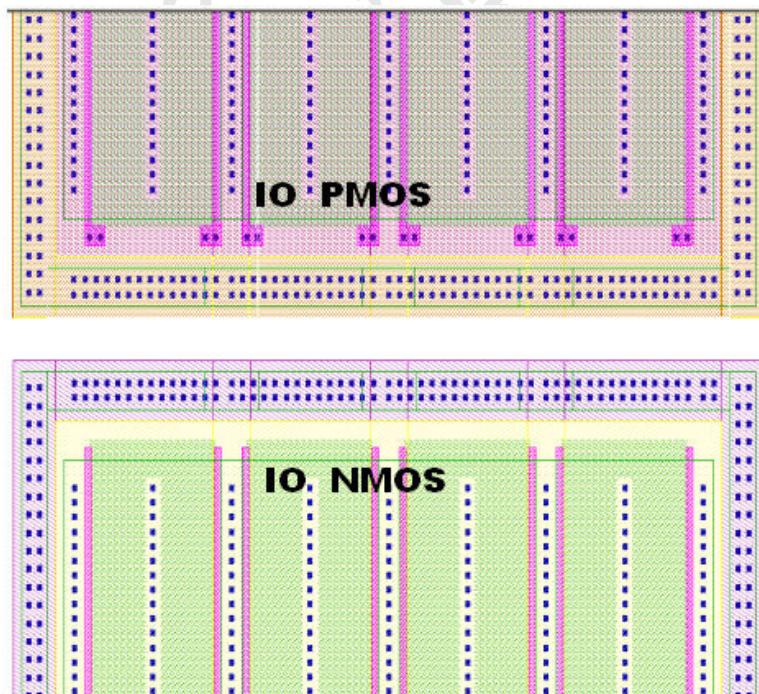


Fig. 11.1.5 LUP.3g violation: (too short IO N/PMOS space)

The following figure shows the latch-up failure if the layout does not violate any latch-up design rule. The displacement current ( $Cdv/dt$ ) may induce the internal circuit latch-up if the internal circuit is nearby the capacitors and is not separated by a P+ strap. Please separate the internal circuit and capacitor by a P+ strap to inhibit the displacement current to induce the latch-up.

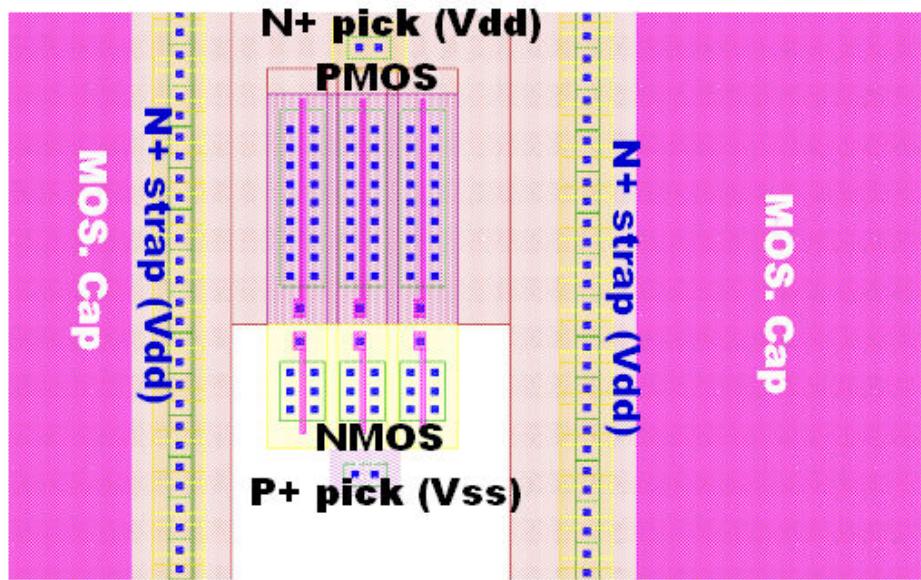


Fig. 11.1.6 LUP.8g violation, but DRC can not flag it:  
(Inverter and capacitor are not separated by P+ guard-ring)

## 11.1.2 Layout Rules and Guidelines for Latch-up Prevention

### 11.1.2.1 Special Definition in Latch-up Prevention

Term	Definition
I/O pads	Do not include Vdd pad and Vss pad.
Internal circuit	Include NMOS, PMOS, de-coupling capacitors and varactor that do not connect to an IO pad.
Guard-ring	Complete un-broken ring-type OD and M1 with CO as many as possible, connected to Vdd or Vss.
N+ guard-ring	Complete un-broken ring-type (NP AND OD) and M1 with CO as many as possible, connected to Vdd.
P+ guard-ring	Complete un-broken ring-type (PP AND OD) and M1 with CO as many as possible, connected to Vss.
NMOS cluster	A group of NMOSs
PMOS cluster	A group of PMOSs

DRC uses the two following methods to recognize the MOS and ACTIVE which connect to an I/O pad:

- 1) MOS/ ACTIVE in SDI
- 2) MOS/ ACTIVE connect to an I/O pad by metal

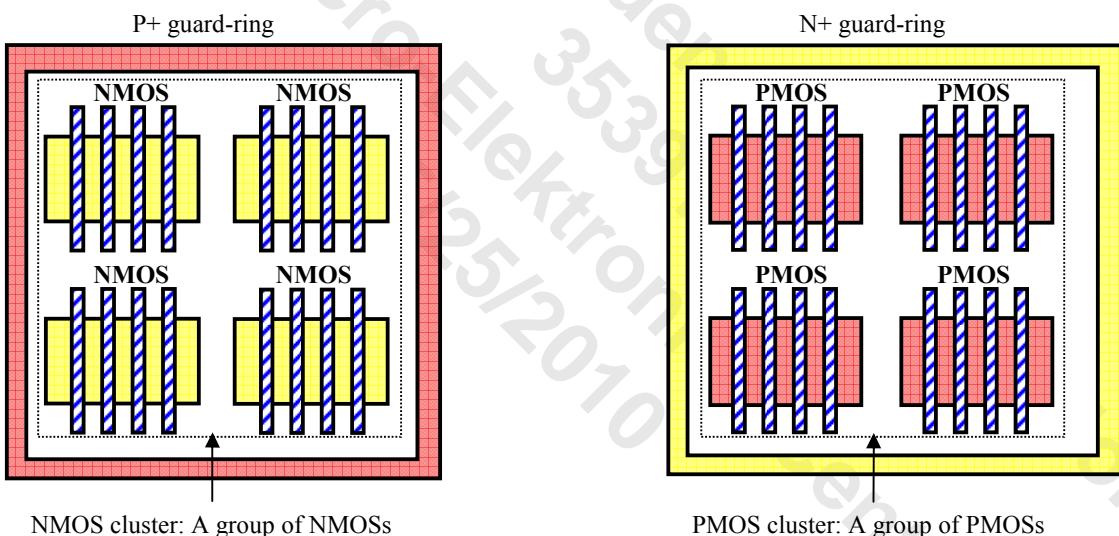


Fig. 11.1.7 Example of an NMOS cluster and a PMOS cluster

## 11.1.2.2 Latch-up Dummy Layers Summary

### 11.1.2.2.1 SDI Dummy Layer (CAD layer: 122)

SDI is a DRC layer but not for mask making. It is required to cover all the OD regions of the ESD related circuits (Regular IO, high voltage tolerant I/O, Power Clamp), including MOS and diode, that are connected to the pads. SDI is not necessary to cover the Well STRAP or ESD guard-ring.

### 11.1.2.2.2 LUPWDMDY Dummy Layer (CAD layer: 255;1)

LUPWDMDY is a dummy layer to waive these guidelines, LUP.1g, LUP.2g, LUP.3.1g, LUP.3.2g, LUP.3.3g, LUP.3.4g, LUP.4, LUP.5.1g, LUP.5.2g, LUP.5.3g, and LUP.5.4g.

- Condition:
  - It is not recommended to use this layer before silicon is proven at the package.
  - Please consult TSMC if you would like to follow it as rules and have DRC violations before tapeout.
- Usage:
  - Draw LUPWDMDY to fully cover MOS/ACTIVE OD/ Diode regions that are connected to I/O pads, including the source, gate, drain, and diode, but not necessarily to cover Well STRAP, guard-ring.
  - It is for DRC usage but not a tapeout required CAD layer.

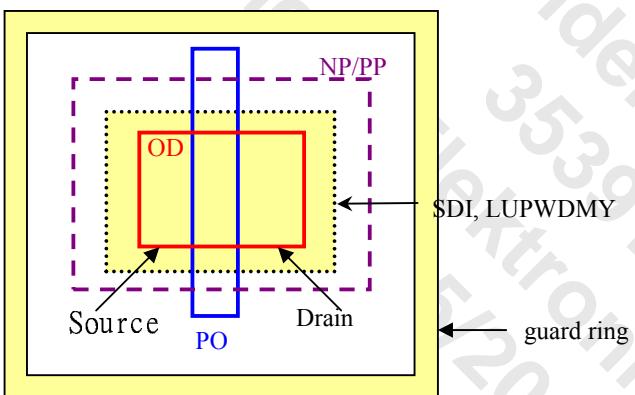


Fig. 11.1.8 Example of SDI/LUPWDMDY

## 11.1.2.3 DRC methodology for Latch-up Rules

### 11.1.2.3.1 DRC methodology for LUP.1

- DRC use the following features to find out the devices for LUP.1:
  1. The Active/MOS OD covered by SDI (122;0).
  2. The Active OD which is connected to (#1) I/O PAD. (#2)
  3. The following cases are excluded :
    - I. The Active OD is used for Resistor.
    - II. The Active/MOS OD is covered by LUPWDMY (255;1).
- #1: DRC use the following features to check the connectivity :
  1. Build-up the connection by Metal, Via, RV, AP, CB, CB2, and CBD
  2. By default, the connection is broken by resistors for Latch-Up rule checks.
  3. If the resistance of used resistors between PAD and the Active/MOS OD is lower than 200 ohm, the switch of "DISCONNECT\_AFTER\_RESISTOR" should be turned off to keep the connection after resistors.
- #2 : DRC use the following features to distinguish Power & I/O PAD :
  1. By default, DRC will recognize power PAD according to the connectivity of AP, CB, CB2, and CBD to STRAP.
  2. Check the PAD with "power text" to recognize power PAD.
    - I. Control by the switch of "DEFINE\_PAD\_BY\_TEXT". The switch is off by default.
    - II. Default power text name is "Vdd" "Vss" "aVdd" "aVss" ... (same as LVS)
  3. Check the PAD with "power dummy layer" to recognize power PAD.
    - I. VDDDMY(255;4): Dummy Layer for Power(Vdd) PAD
    - II. VSSDMY(255;5): Dummy Layer for Ground(Vss) PAD
  4. Except for recognized Power PAD, all the others are I/O PAD.
- The guard ring can not share for different type devices.

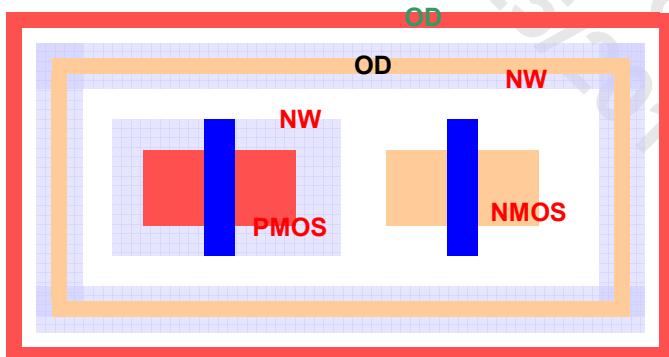


Fig. 11.1.9 example of illegal guard ring

### 11.1.2.3.2 DRC methodology for LUP.2

- DRC use the following features to find out the devices for LUP.2:
  - The MOS OD within 20um space from the Active/MOS OD for LUP.1 check
  - The following cases are excluded:
    - The MOS OD is floating without any contact over gate and S/D.
    - The MOS OD is covered by LUPWDMY (255;1)
    - The NMOS is inside DNW, and the NW over DNW is the same as the NW of relative PMOS which is 8um away from the NMOS.
    - The NMOS is inside DNW, and the NW over DNW is not the same as the NW of relative PMOS, but these two NWs are connected.

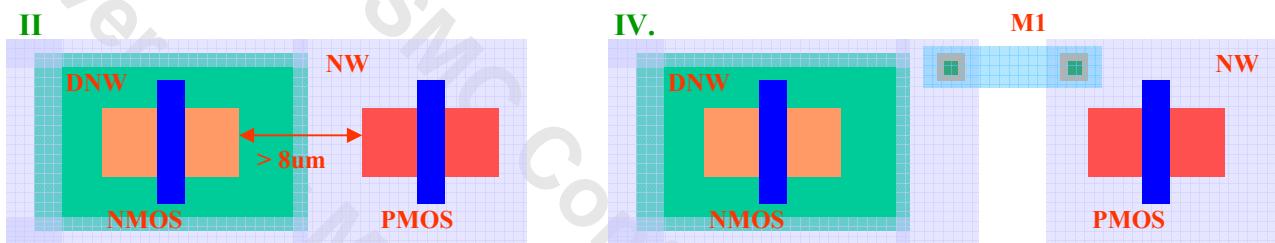


Fig. 11.1.10 example of LUP.2 III and IV

### 11.1.2.3.3 DRC methodology for LUP.3 group

- DRC use the following features to find out the devices for LUP.3 group:
  - Find out the MOS OD for LUP.1 check
  - The following cases are excluded:
    - The excluded case "I" and "II" in LUP.1.
    - The NMOS is inside DNW, and the NW over DNW is not the same as the NW of relative PMOS, but these two NWs are connected.

#### 11.1.2.3.4 DRC methodology for LUP.4

- DRC use the following features to check the guard-ring width.
  - Find out the Active/MOS OD for LUP.1 & LUP.2 check.
  - The devices should be placed inside a complete guard-ring with width  $\geq 0.2\mu m$ .

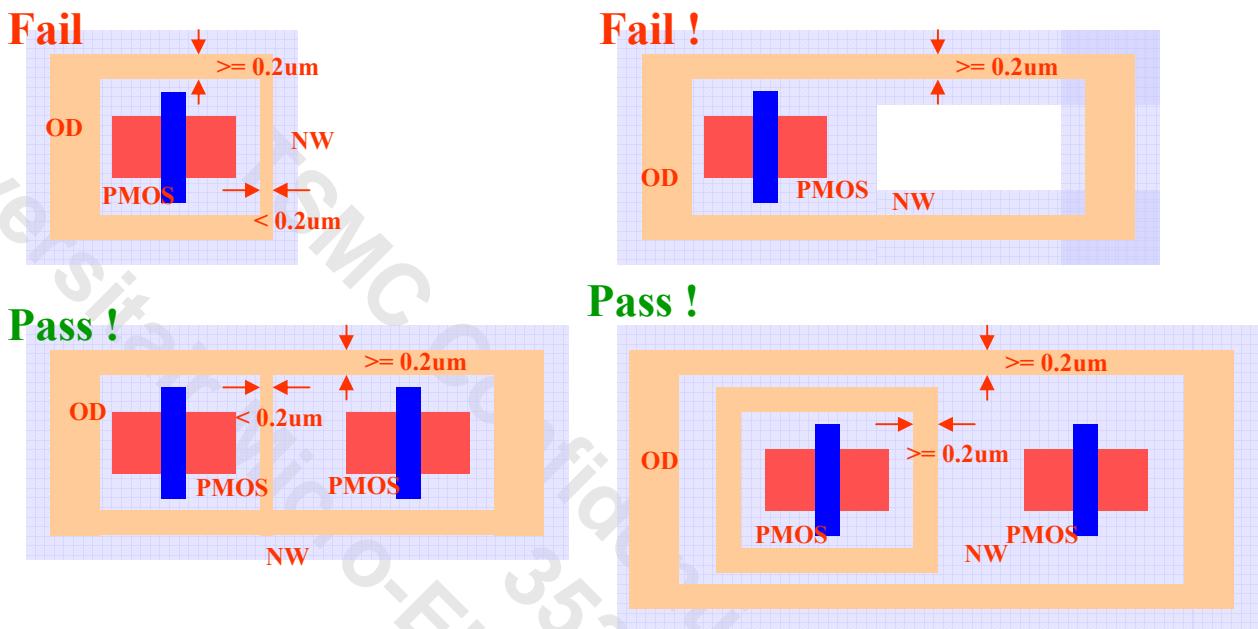


Fig. 11.1.11 example of LUP.4

#### 11.1.2.3.5 DRC methodology for LUP.5 group

- DRC use the following features to find out the devices for LUP.3 group:
  - Find out the MOS OD for LUP.1 & LUP.2 check.
  - The excluded cases are "I", "II", and "IV" in LUP.2.

## 11.1.2.4 Layout Rules and Guidelines for Latch-up Prevention

Table 11.1.1 Layout Rules and Guidelines for Latch-up Prevention

Rule No.	Description	Label		Dimension (um)
LUP.1g	<p>Any N+ACTIVE or an N+ACTIVE cluster connected to an I/O pad must be surrounded by a P+ guard-ring. (Figure 11.1.12)</p> <p>Any P+ACTIVE or a P+ACTIVE cluster connected to an I/O pad must be surrounded by a N+ guard-ring. (Figure 11.1.12)</p> <p>Please also refer to LUP.9g for further information.</p>			
LUP.2g	<p>Within 20um space from the MOS connected to an I/O pad, a P+ guard-ring is required to surround an NMOS or an NMOS cluster. And an N+ guard-ring is required to surround a PMOS or a PMOS cluster. (Figure 11.1.14)</p> <p>NMOS guard-ring are exempt from the following conditions (Figure 11.1.13):</p> <ol style="list-style-type: none"> <li>1) When the NMOS is enclosed by a DNW, and the NW of the checked PMOS [connected to an I/O pad and within 8um space from NMOS enclosed by a DNW] does not interact with the DNW.</li> <li>2) If the voltage (Va) of the NW INTERACT DNW is <math>\geq</math> the voltage (Vb) of the NW of the checked PMOS. However, DRC can only flag the different connection.</li> </ol>			
	<p>LUP.3.1g, LUP.3.2g, LUP.3.3g, LUP.3.4g, LUP.5.1g, LUP.5.2g, LUP.5.3g, LUP.5.4g are exempt from the following conditions (Figure 11.1.13):</p> <ol style="list-style-type: none"> <li>1) When the NMOS is enclosed by a DNW, and the NW of the checked PMOS does not interact with the DNW.</li> <li>2) If the voltage (Va) of the NW INTERACT DNW is <math>\geq</math> the voltage (Vb) of the NW of the checked PMOS. However, DRC can only flag the different connection.</li> <li>3) If there is a resistor between N/PMOS and IO pad.</li> </ol>			
LUP.3.1g	For the 1.2V, 1.05V or 1.0V N/PMOS which connects to an I/O pad, space between the NMOS and the PMOS. (Figure 11.1.12)	A	$\geq$	2
LUP.3.2g	<p>For the 1.8V N/PMOS which connects to an I/O pad directly, (Figure 11.1.12)</p> <ol style="list-style-type: none"> <li>1) space between the 1.8V NMOS and the 1.8V/1.2V/1.05V/1.0V PMOS</li> <li>2) space between the 1.8V PMOS and the 1.8V/1.2V/1.05V/1.0V NMOS</li> </ol>	A	$\geq$	2.3
LUP.3.3g	<p>For the 2.5V N/PMOS which connects to an I/O pad directly, (Figure 11.1.12)</p> <ol style="list-style-type: none"> <li>1) space between the 2.5V NMOS and the 2.5V/1.2V/1.05V /1.0V PMOS</li> <li>2) space between the 2.5V PMOS and the 2.5V/1.2V/1.05V /1.0V NMOS</li> </ol>	A	$\geq$	2.6
LUP.3.4g	<p>For the 3.3V N/PMOS which connects to an I/O pad directly, (Figure 11.1.12)</p> <ol style="list-style-type: none"> <li>1) space between the 3.3V NMOS and the 3.3V/1.2V/1.05V /1.0V PMOS</li> <li>2) space between the 3.3V PMOS and the 3.3V/1.2V/1.05V /1.0V NMOS</li> </ol>	A	$\geq$	5

Rule No.	Description	Label		Dimension (um)
LUP.4g	Width of the N+ guard-ring and P+ guard-ring for the ACTIVE connected to an I/O pad, and also MOS within 20um space from the MOS connected to an I/O pad. (e. g. width of guard-ring of LUP.1g and LUP.2g)	B	≥	0.2
LUP.5.1g	For the internal circuits within 20um space from 1.2V, 1.05V or 1.0V MOS which connects to an I/O pad, 1) space between the 1.2V, 1.05V or 1.0V NMOS connected to an I/O pad and the PMOS in the internal circuit (Figure 11.1.14) 2) space between the 1.2V, 1.05V or 1.0V PMOS connected to the I/O pad and the NMOS in the internal circuit (Figure 11.1.14)	C	≥	2
LUP.5.2g	For the internal circuits within 20um space from 1.8V MOS which connects to an I/O pad directly, 1) space between the 1.8V NMOS connected to an I/O pad and the PMOS in the internal circuit (Figure 11.1.14) 2) space between the 1.8V PMOS connected to the I/O pad and the NMOS in the internal circuit (Figure 11.1.14)	C	≥	2.3
LUP.5.3g	For the internal circuits within 20um space from 2.5V MOS which connects to an I/O pad directly, 1) space between the 2.5V NMOS connected to an I/O pad and the PMOS in the internal circuit (Figure 11.1.14) 2) space between the 2.5V PMOS connected to the I/O pad and the NMOS in the internal circuit (Figure 11.1.14)	C	≥	2.6
LUP.5.4g	For the internal circuits within 20um space from 3.3V MOS which connects to an I/O pad directly, 1) space between the 3.3V NMOS connected to an I/O pad and the PMOS in the internal circuit (Figure 11.1.14) 2) space between the 3.3V PMOS connected to the I/O pad and the NMOS in the internal circuit (Figure 11.1.14)	C	≥	5
LUP.6	1) Any point inside NMOS source/drain {(N+ACTIVE INTERACT PO) NOT PO} space to the nearest PW STRAP in the same PW. (Figure 11.1.15) 2) Any point inside PMOS source/drain {(P+ACTIVE INTERACT PO) NOT PO} space to the nearest NW STRAP in the same NW. (Figure 11.1.15) In SRAM bit cell region, the rule is relaxed from 30um to 40um.	D	≤	30
LUP.7g <sup>U</sup>	All the guard-rings and STRAPS should be connected to VDD/VSS with very low series resistance. Use as many contacts and vias as possible.			
LUP.8g <sup>U</sup>	A P+ guard-ring should separate a large capacitor and MOS.			
LUP.9g <sup>U</sup>	Additional one N+ STRAP and one P+ STRAP are required to be inserted between the P+ guard-ring and N+ guard-ring for LUP.1 (Figure 11.1.12). And the N+ STRAP should isolate the P+ STRAP and the P+ guard-ring. And the P+ STRAP should isolate the N+ STRAP and the N+ guard-ring.			

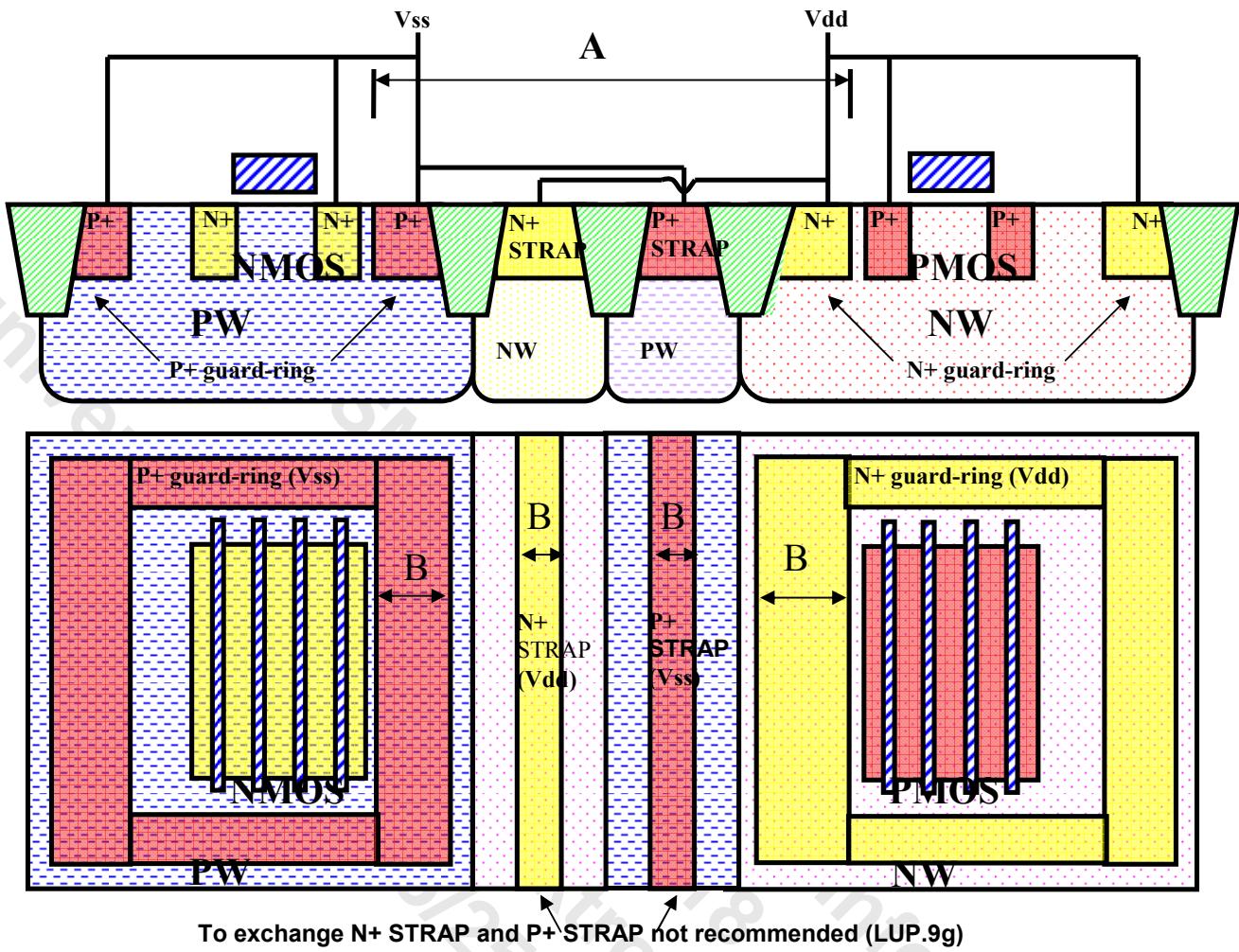
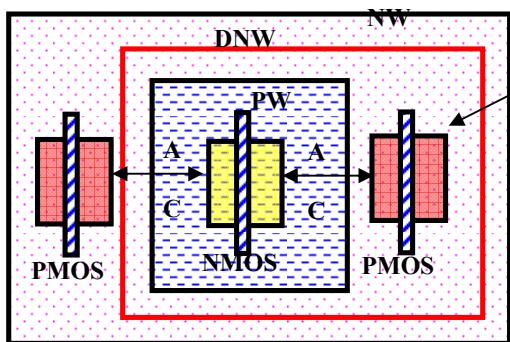
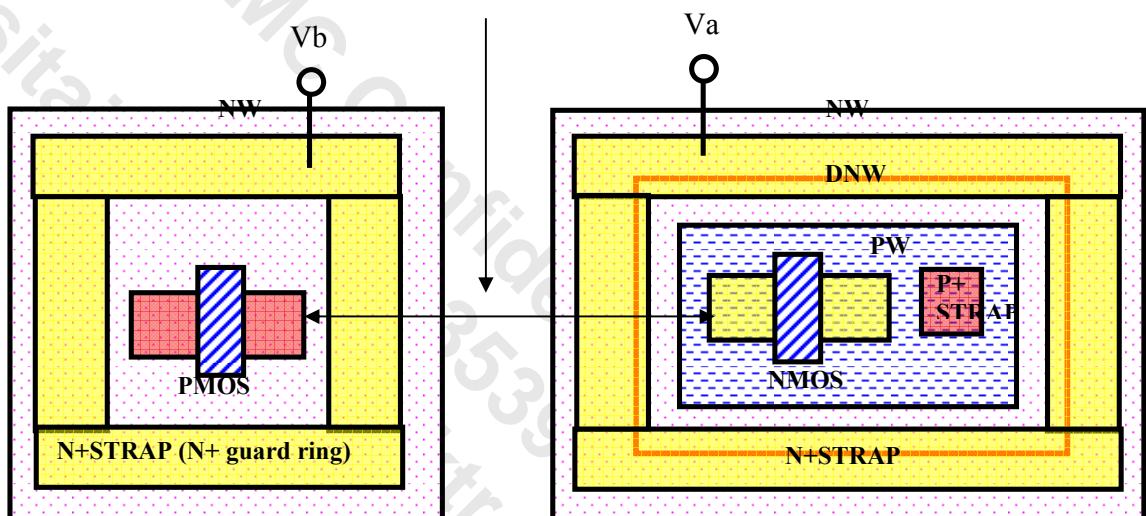


Figure 11.1.12

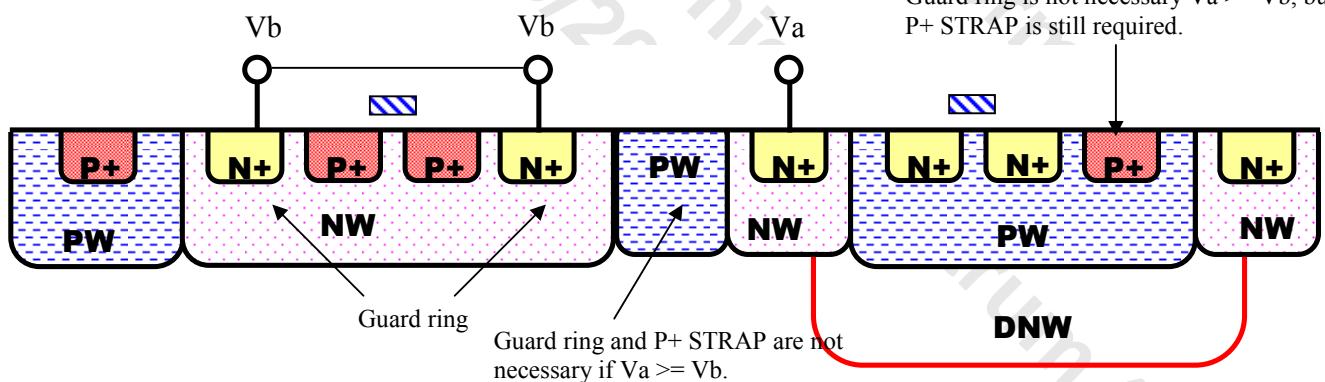
If the NW of the checked PMOS interacts with the DNW, the space needs to follow A or C.



If voltage  $V_a \geq V_b$ ,  
the space can be  $< A$  or  $< C$



Guard ring is not necessary  $V_a \geq V_b$ , but P+ STRAP is still required.



For LUP.2g, LUP.3.1g, LUP.3.2g, LUP.3.3g, LUP.3.4g, LUP.5.1g, LUP.5.2g, LUP.5.3g, LUP.5.4g, if voltage  $V_a \geq V_b$ , the above rules allow that the NMOS is enclosed by a DNW and the NW of the checked PMOS does not interact with the DNW. However, DRC can only flag the different connection.

**Figure 11.1.113**

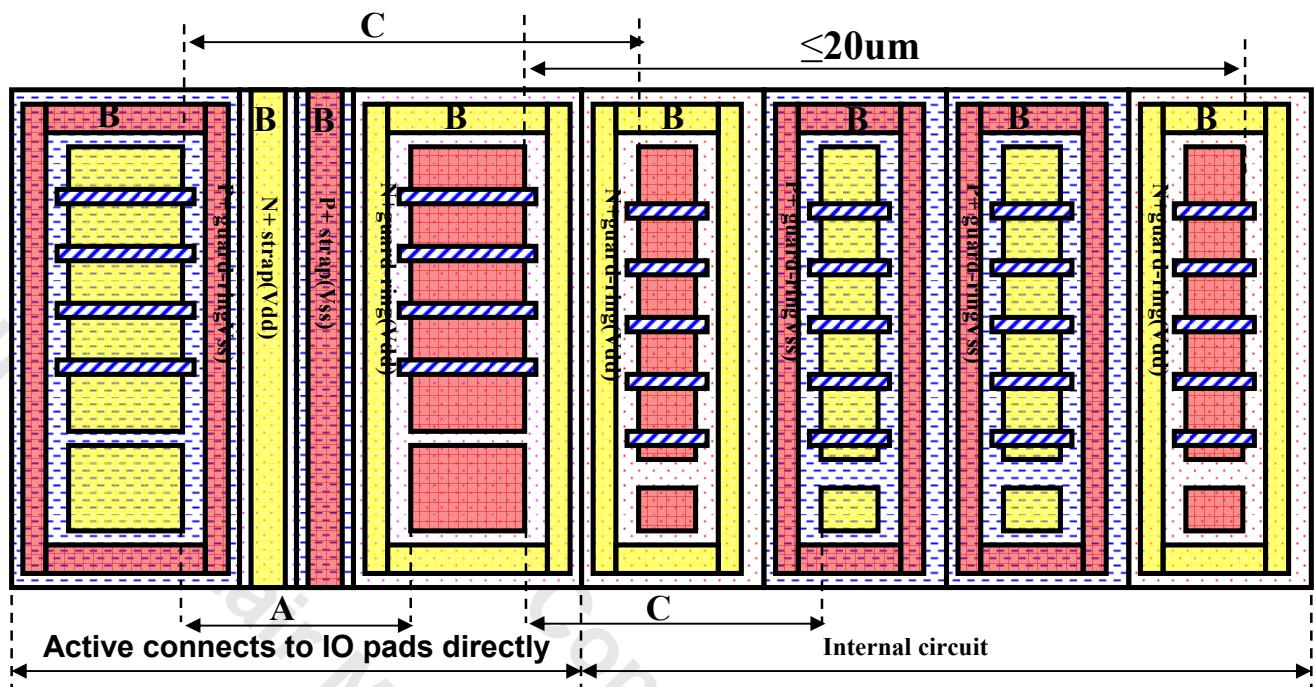


Figure 11.1.14

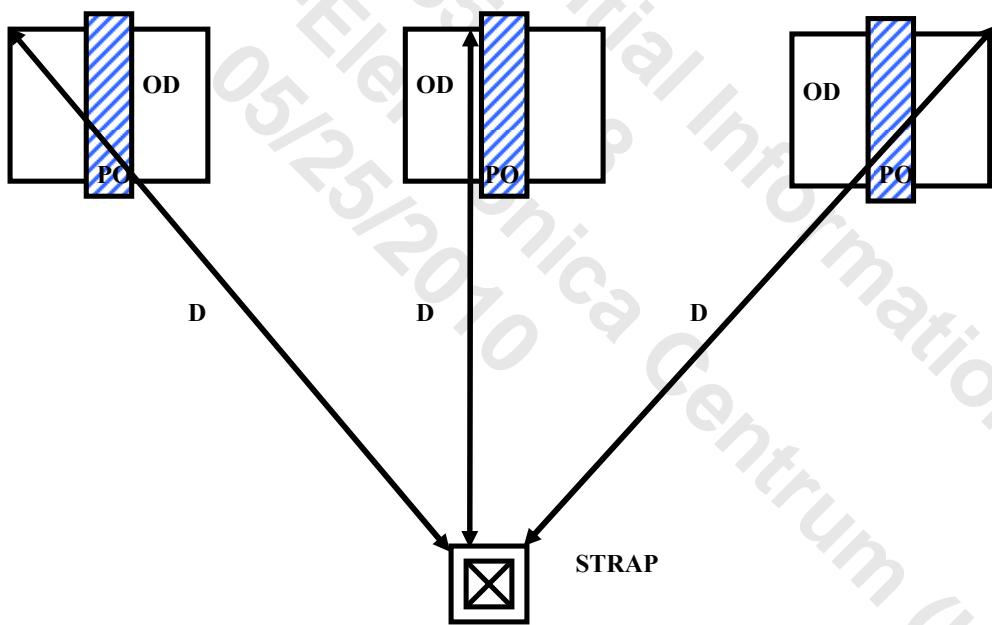


Figure 11.1.15

## 11.1.3 Test Specification and Requirements

TSMC Latch-Up testing is performed at room temperature and 125°C by complying the Latch-up test methodology defined by JEDEC JC-40.2. The test items include Input/Output over-voltage/ over-current test (Fig. 11.1.16) and supply over-voltage test (Fig. 11.1.17). It applies a stepped voltage/current to one pin per device with all other pins open except Vdd and Vss. Testing was started from Vdd/50mA (positive) or 0V/-50mA (negative), and the DUT was biased for 0.5 seconds. If the Icc current does not reach the predefined limit ( $I_{dd}=200\text{mA}$ ), then the voltage was increased by  $\pm 0.1\text{V}$  or  $\pm 50\text{mA}$  and the pin was tested again until  $\pm 1.5\text{Vdd}$  or  $\pm 200\text{mA}$  for Input/Output over-voltage/ over-current. The latch up test passed as the  $I_{dd} \leq \pm 200\text{mA}$  at 125°C.

### Notes:

1. DUT: Device under test.

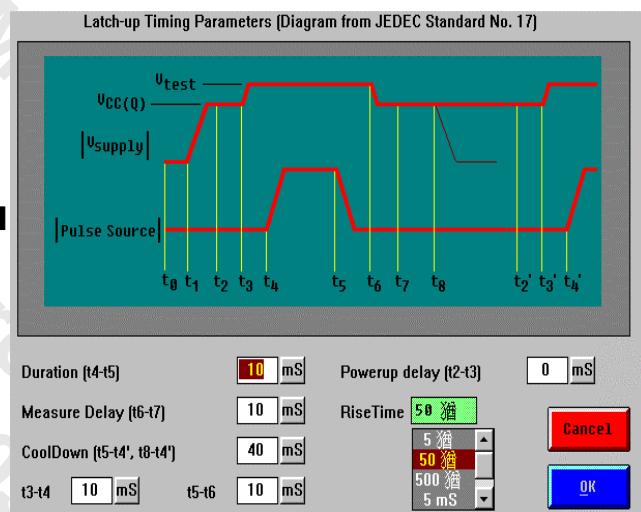
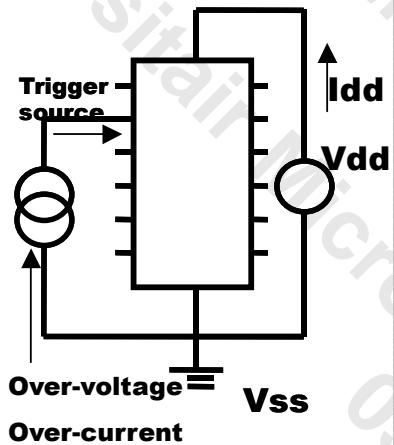


Fig. 11.1.16 Input/Output Over-Voltage/Current Test

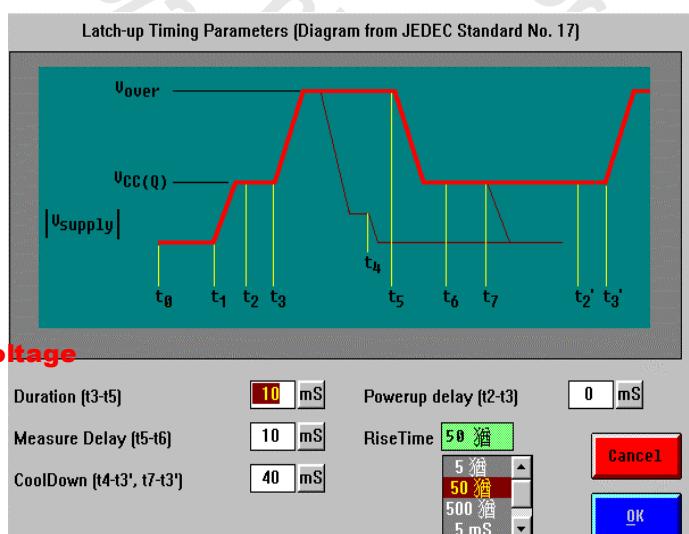
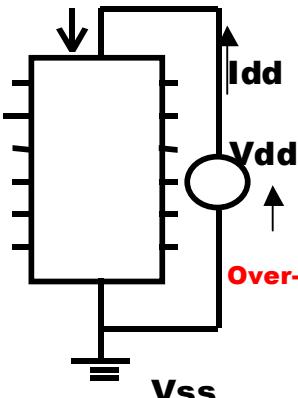


Fig. 11.1.17 Supply Over-voltage Test

## 11.2 I/O ESD Protection Circuit Design and Layout Guidelines

### 11.2.1 ESD introduction

During manufacturing, it is inevitable the IC will suffer various kinds of Electrostatic-Discharge (ESD) damage. Different environments, wafer during CMOS process, package, testing and human handling, will generate different kinds of ESD's. Currently, the charge device model (CDM), Human-Body mode (HBM) and Machine model (MM) are the most common models used to simulate the ESD events generated from various environments. The main difference between CDM and HBM is that CDM charges come from the substrate through the internal circuit to the pad, while the ESD's for HBM and MM come from the external environment to the pad. So, most ESD protection devices only can be used to protect HBM and MM, but cannot be used to protect the CDM since the ESD protection device is at the pad and there is no direct current path between the internal circuit and the ESD protection device.

The discharging behaviors for the three ESD models all can be simplified by the equivalent circuit in Figure 11.2.1 and expressed by the equation :

$$I_{ESD} = V_{ESD} \frac{e^{(-\alpha+\beta)t} - e^{-(\alpha+\beta)t}}{2\beta L_o} \quad (1). \text{ where } \alpha=R_o/(2L_o), \beta=\sqrt{(R_o C_o)^2 - 4L_o C_o}/(2L_o C_o)$$

For HBM, the  $R_o$ ,  $C_o$  and  $L_o$  is  $1.5K\Omega$ ,  $100pF$  and  $7.4\mu H$ , respectively. For MM, the  $R_o$ ,  $C_o$  and  $L_o$  is  $10\Omega$ ,  $200pF$  and  $7.4\mu H$ , respectively. Substituting the above vaules into eq. (1), the measured and theoretical current waveforms for HBM and MM are shown in Figure 11.2.2. For HBM, the rise time is  $<10nsec$ , the decay time is  $150nsec$  ( $R_o C_o=1.5K\Omega \times 100pF$ ) and the peak current is equal to  $V_{ESD}/R_o$ . The period for MM is nearly  $90nsec$  and the peak current for  $200V$  MM is nearly  $1.7A$ .

Figure 11.2.3 shows the CDM discharging current waveforms vs.  $L_o$  and  $R_o$  based on eq. (1) for  $500V$  CDM. The CDM period and peak current are varied with  $L_o$ ,  $C_o$ , and  $R_o$ . Compared with HBM and MM, the CDM has a shorter period and a larger peak current.

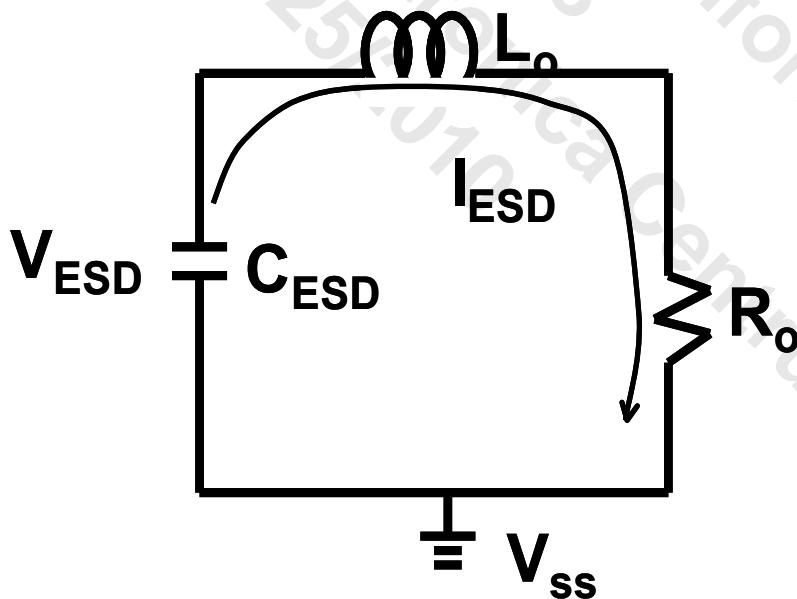


Fig. 11.2.1 The simplified equivalent circuit for ESD

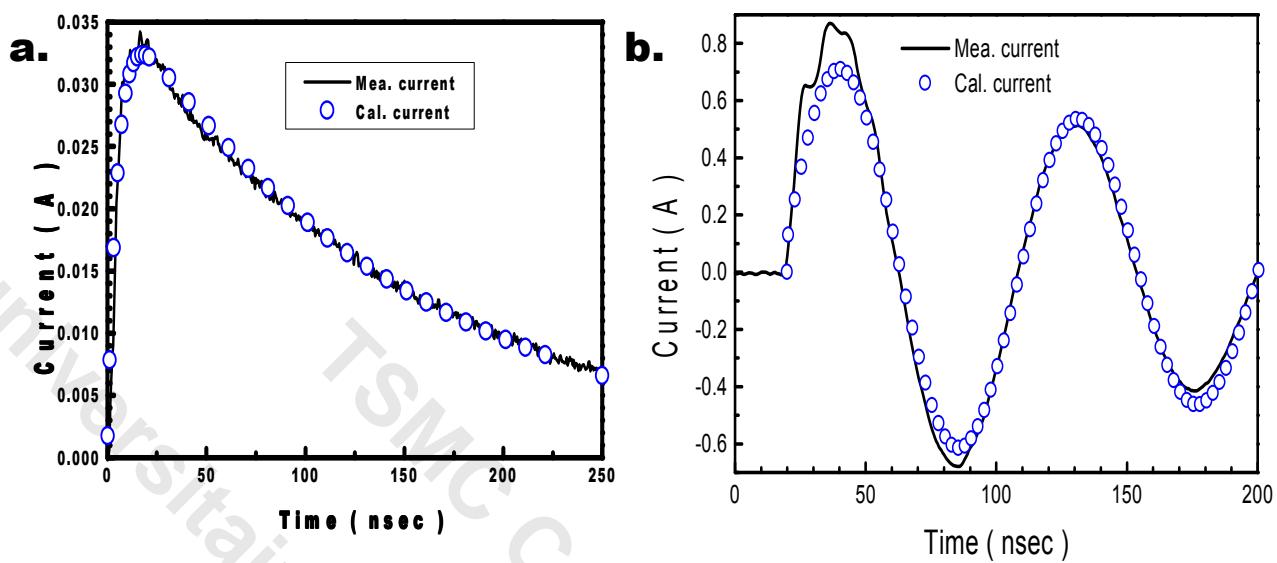


Fig. 11.2.2 The discharging current waveform for (a) HBM and (b) MM

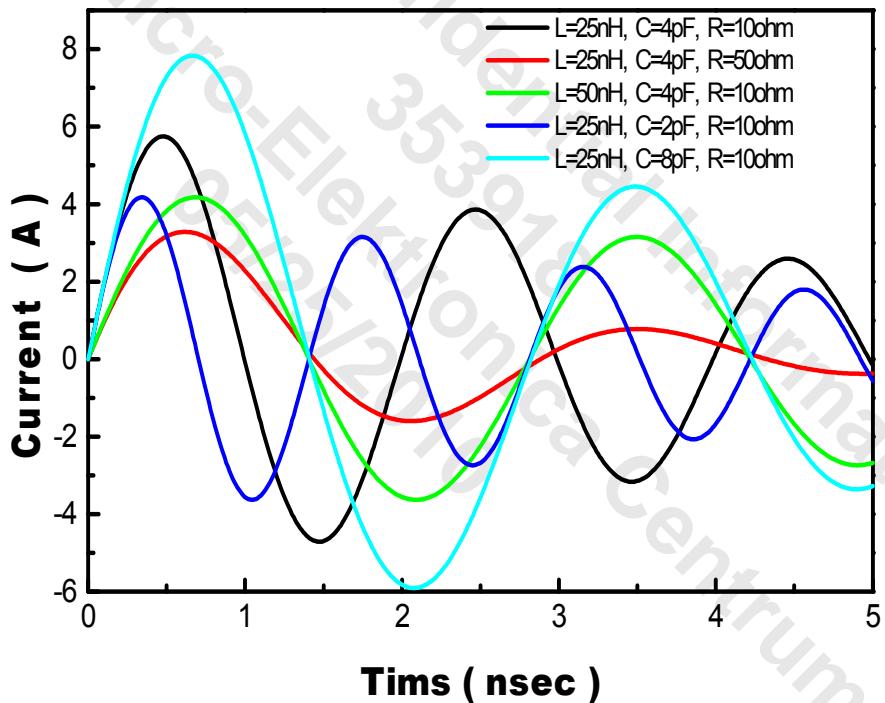


Fig. 11.2.3 The CDM discharging current waveforms vs.  $L_o$ ,  $R_o$ , and  $C_o$

Besides the above three models, another kind of ESD, which occurs during wire bonding, has been found. We call it ball-bonding ESD (BBE). The stress period of the BBE ( $\sim 20\text{nsec}$ ) is shorter than HBM and MM, but longer than CDM. The stress voltage ( $\sim 13\text{V}$ ) of BBE is much smaller than HBM, MM and CDM. The BBE came from the charged wire through the pad and device which connect the pad to the substrate. It might induce the reliability issue and degrade the device ESD performance if the ESD protection device is not robust enough or the pad is without the ESD protection device. (Please refer to JH Lee et. al, "The impact of ball-bonding induced voltage transient on sub-90nm CMOS technology," in IRPS, p. 97, 2007.)

Because the pad is the median used to interact with externals for an IC, all pads need ESD protection devices to protect the ESD coming from various environments to prevent internal circuit damage.

## 11.2.2 TSMC IO ESD layout style introduction

TSMC IO ESD protection scheme is the self-protection scheme that IO is the ESD protection device. No matter NMOS or PMOS, they all have the snapback phenomena. The snapback mechanism can be described as the following: As the applied voltage is higher than the device trigger voltage ( $V_{t1}$  in Fig. 11.2.4), a lot of holes are generated due to a drain junction occurrence Avalanche-breakdown. The hole current ( $I_{sub}$  in Fig. 11.2.4) flows through the substrate ( $R_{sub}$  in Fig. 11.2.4) and raises up the substrate potential ( $V_{sub}$  in Fig. 11.2.4), and eventually forward bias the p-n junction (D1 in Fig. 11.2.4) between the P-substrate and the source when the potential becomes higher than 0.7V. Subsequently, a lot of electrons are injected from the source and flow to the p-n junction between the P-substrate and the drain, which generates more electron-hole pairs due to impact-ionizations at the high electrical field of the drain junction. The resulting carrier transport mechanism causes a positive feedback effect to turn on the parasitic n-p-n bipolar transistor (npn in Fig. 11.2.4). As the parasitic n-p-n is turned on, it can sink a much higher current level than the initial Avalanche-breakdown current and goes into a stable snapback region as shown in Fig. 11.2.4.

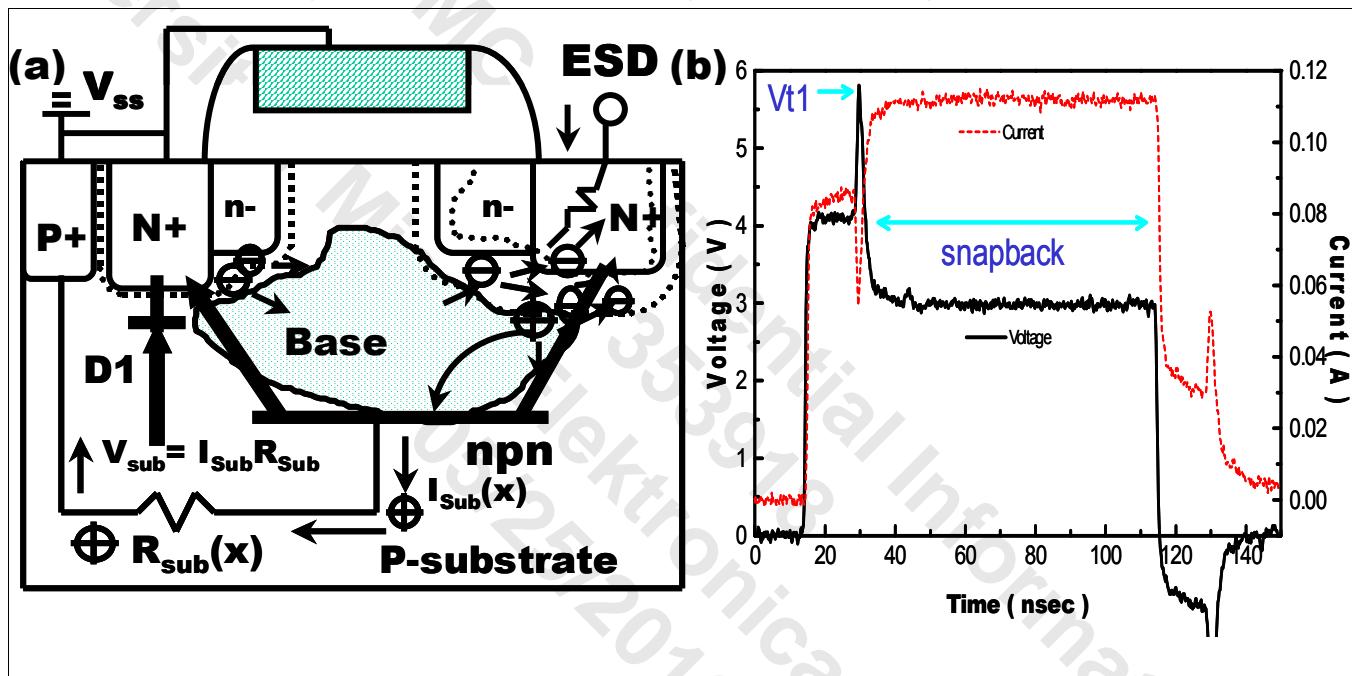


Fig. 11.2.4 (a) the parasitic components of a Grounded-gate NMOS (GGNMOS), (b). real time IV characteristics of a GGNMOS under 100 nsec TLP pulse

The RPO is the silicide blocking layer which is commonly used for an ESD protection device to forbid the silicide formation on the drain region. The RPO scheme might be not a good solution for IO design due to larger series resistance, but it can provide a stable ESD performance for an ESD protection device. So, the device ESD performance does not vary between technology generations or manufacturing fabs. Fig. 11.2.5 shows the high current IV characteristics of a RPO N+ OD resistor. The RPO N+ OD resistor has a saturation region. In the saturation region, the resistor becomes a high impedance resistor, so the increase in the applied voltage does not increase the stress current. From this characteristic, we can deduce that RPO can be used to clamp the current to prevent the current being localized in a given region. As a region enters the saturation point, it becomes a high impedance resistor. Then, the current of this region cannot be increased anymore. Subsequently, the current will be pushed to flow to other non-saturated regions and the current can distribute along the junction uniformly.

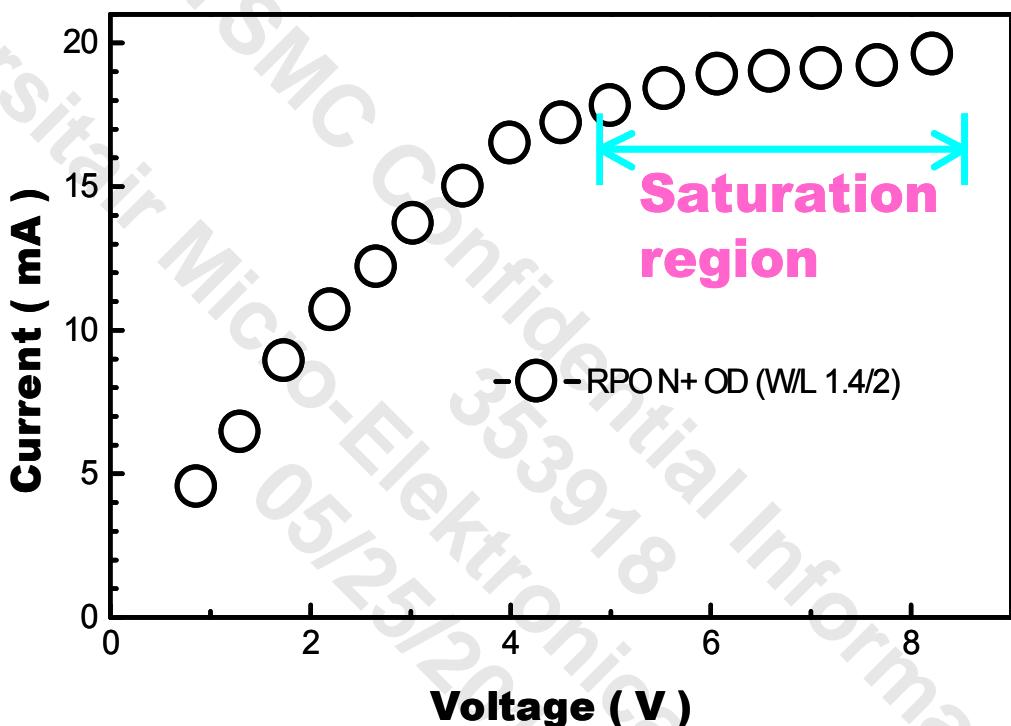


Fig. 11.2.5 High current IV characteristics of a RPO N+ OD resistor

The ESD implant is a process scheme to enhance the device ESD performance without changing the device layout since it only covers the drain region and needs to have 0.4um space from the poly gate. The current ESD implant recipe is P-type ESD implant. It can reduce the device breakdown voltage and create the higher electrical field during the snapback region, resulting in better ESD performance. At TSMC, only one dosage exists for P-type ESD implants. The dosage for ESD implants is higher than the channel implant dosage for 3.3V and 2.5V devices, but lower than the channel implant dosage for 1.8V, 1.2V, 1.05V and 1.0V devices. So, the ESD implant is useful for 3.3V device, but is useless for 2.5V devices and of no use for devices below 1.8V.

## 11.2.3 ESD Dummy Layers Summary

### 11.2.3.1 SDI Dummy Layer

- SDI (CAD layer: 122) is a DRC layer but not for mask making. It is required to cover all the OD regions of the ESD related circuits (Regular IO, high voltage tolerant I/O, Power Clamp), including MOS and diode, that are connected to the pads. SDI is not necessary to cover the Well STRAP or ESD guard-ring.

### 11.2.3.2 ESD3 Dummy Layer Description

- ESD3 (CAD layer: 147) a tape-out layer. It is required for cascode NMOS in high voltage tolerant I/O (N2 and N3 shown in Figure 11.2.15). ESD3 includes the source, gate, and drain, but does not necessarily cover the Well STRAP or the ESD guard-ring.

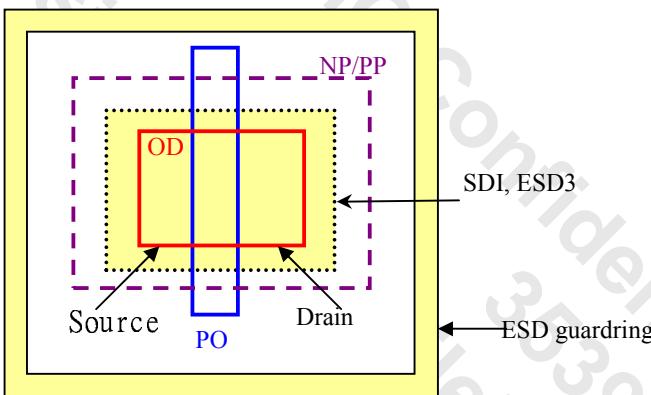


Figure 11.2.6 The SDI, ESD3 dummy layer layout

## 11.2.4 ESD circuits Definition

### 11.2.4.1 Regular IO

Regular I/O is composed of the NMOS and PMOS and the drains of the NMOS and PMOS connect to the pad directly (N1/P1 in Figure 11.2.10).

### 11.2.4.2 HV tolerant IO

The HV tolerant I/O is composed of the PMOS in floating NW (P2 Figure 11.2.15) and cascode NMOS and the drains of the floating NW PMOS and cascode NMOS connect to the pad directly (P2/N2/N3 in Figure 11.2.15). There are three kinds of HV tolerant IO listed below.

#### 11.2.4.2.1 5V tolerant I/O

5V tolerant I/O circuits using a 3.3V I/O device with  $V_{IN}$  criterion:  $V_{IN} > 3.3V$  but  $V_{IN} \leq (5V + 10\%)$ .

#### 11.2.4.2.2 3.3V tolerant I/O

3.3V tolerant I/O circuits using a 2.5V I/O device with  $V_{IN}$  criterion:  $V_{IN} > 2.5V$  but  $V_{IN} \leq (3.3V + 10\%)$ .

#### 11.2.4.2.3 2.5V tolerant I/O

2.5V tolerant I/O circuits using a 1.8V I/O device with  $V_{IN}$  criterion:  $V_{IN} > 1.8V$  but  $V_{IN} \leq (2.5V + 10\%)$ .

### 11.2.4.3 IO Buffer

The I/O Buffer includes regular I/O and HV tolerant I/O.

### 11.2.4.4 Power Clamp Device (Ncs)

The device is used for  $V_{DD}$  Pad to  $V_{SS}$  Pad protection (Ncs in Figure 11.2.10 and Figure 11.2.15). Please refer to section 11.2.6.4.

### 11.2.4.5 ESD Device

The ESD Device includes any device (NMOS, PMOS, I/O buffer, power clamp device, diodes, SCR and resistor) which connects to the pad directly and can be used to discharge the ESD current.

## 11.2.5 Requirements for ESD Implant Masks

- ESD implant is required for HV tolerant I/O NMOS unless TSMC approves. You have to draw ESD3 layer for mask making.
- For customers who use their own ESD design structure, or do not use HV tolerant NMOS, ESD implant is optional.

**Table 11.2.1 ESD Implant Masks for HV Tolerant I/O Circuits**

I/O Design Style	ESD3 (CAD layer 147) Requirement	ESD mask (no.111) Requirement
TSMC-style I/O with HV tolerant I/O circuits	Drawing Required	Yes
TSMC-style I/O without HV tolerant I/O circuits	No need	No need
Non TSMC-style ESD	Depends	Depends

## 11.2.6 ESD Guidelines

- TSMC's ESD spec is 2KV for Human Body Model (HBM) and 200V for Machine Model (MM)
- These design guidelines are designed to increase ESD protection levels to TSMC specifications.
- These guidelines are developed from our test chip silicon data. The test structures in these test chips include most of the failure cases we have studied. Yet, there might be other weak paths that are not captured by these guidelines. Thus, chip level ESD testing should be carried out.

### 11.2.6.1 General Guideline for ESD Protection

No.	Description	Label	Dimension
ESD.WARN.1	SDI is not in whole chip. If SDI does not exist, the ESD related DRC will not work well.		
ESD.WARN.2	SDI enclosure of ACTIVE		$\geq 0$
ESD.1g	Use thin oxide transistor for thin oxide power clamp and thin oxide I/O buffers; use thick oxide transistor for the thick oxide Power Clamp and thick oxide I/O buffers (Figure 11.2.7). DRC will flag the following 2 conditions: 1) ((MOS INTERACT OD2) INTERACT SDI) connected to (MOS NOT INTERACT OD2) 2) ((MOS NOT INTERACT OD2) INTERACT SDI) connected to (MOS INTERACT OD2) DRC will exclude Drain/Source/Gate connected to PW STRAP.		
ESD.2g <sup>U</sup>	NMOS and PMOS for I/O buffer and Power Clamp follow finger type structure with unique finger dimension and layout style.		
ESD.3g	Unit finger width of NMOS and PMOS for I/O buffer and Power Clamp Device (Figure 11.2.8)	G	= 15-60
ESD.4g	The OD area of the edge side of I/O buffer and Power Clamp should be Source or Bulk rather than Drain (Figure 11.2.8), to avoid an unwanted parasitic bipolar effect or an abnormal discharge path in ESD zapping. DRC will flag (((OD INTERACT SDI) NOT PO) INTERACT one Gate) does not connect to STRAP.		
ESD.5g	Same type OD of the I/O buffer and Power Clamp should be surrounded by a guard-ring. All other type ODs should be placed outside this guard-ring. (Figure 11.2.8) DRC will flag the following two conditions, 1) Different type ODs in the most inner guard-ring. 2) OD not inside the most inner guard-ring		
ESD.6g	Butted STRAP and the STRAP which are between two sources of the N/PMOS in the same I/O buffer and Power Clamp are strictly prohibited. (Figure 11.2.9) DRC will flag Butted STRAP and the STRAP which is within 2um space of two sources of (MOS INTERACT SDI) connected to same pad.		
ESD.7g	Except the ESD device, either one of the following two conditions must be followed.		
	1) the space of two same type ODs		$\geq 2.4$
	2) two same type ODs should be separated by different types of OD.		
	The same type ODs are N+OD and N+OD in the same PW, or P+OD and P+OD in the same NW, which connect to two different pads		
ESD.8g <sup>U</sup>	Value of resistor R in Figure 11.2.10		$\geq 200 \Omega$

No.	Description	Label		Dimension
ESD.9g <sup>U</sup>	N/PMOS (N4/P4) of ESD secondary protection in Figure 11.2.10 1) Channel width 2) Should be added after the resistor R (on the far side of R from the pad). 3) NOT in SDI 4) ESD implant and RPO are not needed in these secondary protection devices.		≥	20
ESD.10g <sup>U</sup>	Total width of metal lines connecting the bond pad and the ESD devices. (Figure 11.2.8)	I	≥	10
ESD.11g <sup>U</sup>	Via number for each layer in the ESD discharge current path.		≥	100
ESD.12g	It is not allowed to use OD RPO resistors or NW resistors connected to PAD (Figure 11.2.10 and Figure 11.2.11). DRC will use (((RPDMY OR RH) AND OD) AND RPO) to recognize OD RPO resistor. DRC will use (NWDMY INTERACT NW) to recognize NW resistor.			
ESD.13g <sup>U</sup>	Total metal width for Power and Ground bus line (Figure 11.2.12)		≥	20
ESD.14g <sup>U</sup>	Resistance of the bus line from the V <sub>DD</sub> or V <sub>SS</sub> pad to any I/O pad (Figure 11.2.12)		≤	3Ω
ESD.15g <sup>U</sup>	Bypass discharge cells should be inserted between each separate V <sub>DD</sub> and V <sub>SS</sub> to avoid ESD damage to internal circuits. This preventative measure is of special importance to the isolated powers used only by a small circuit (< 5K gates). The connections are illustrated in Figure 11.2.13. (For more details, please see the “Tips for the Power Bus” section in this chapter.)			

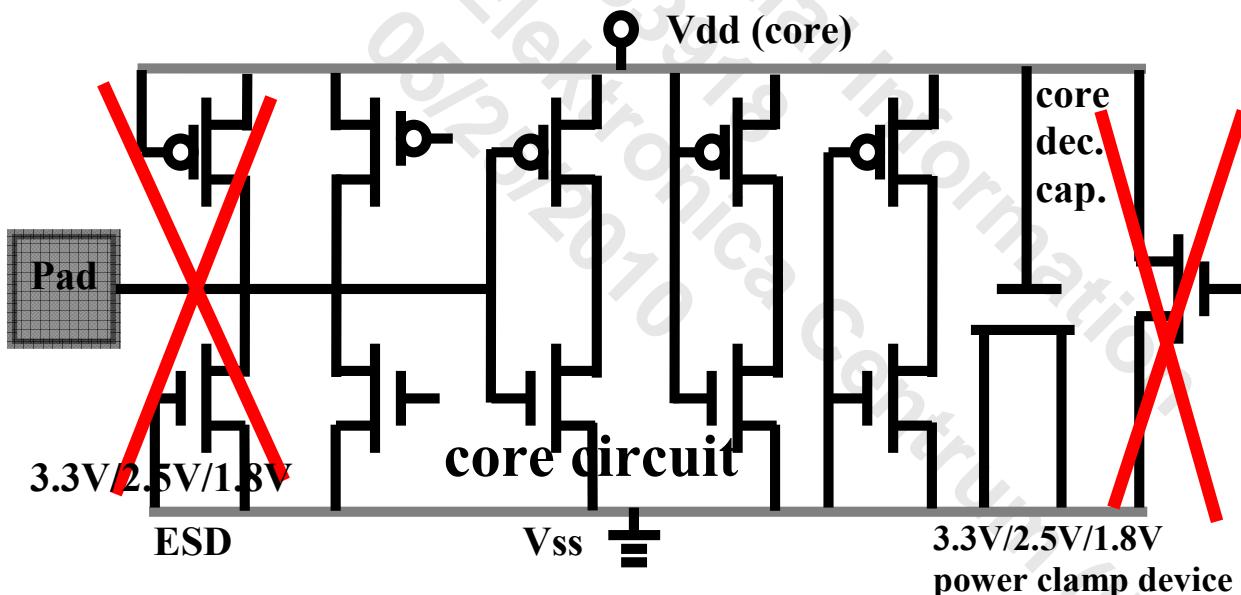


Figure 11.2.7 Use thin oxide transistor for the ESD protection of thin oxide circuits

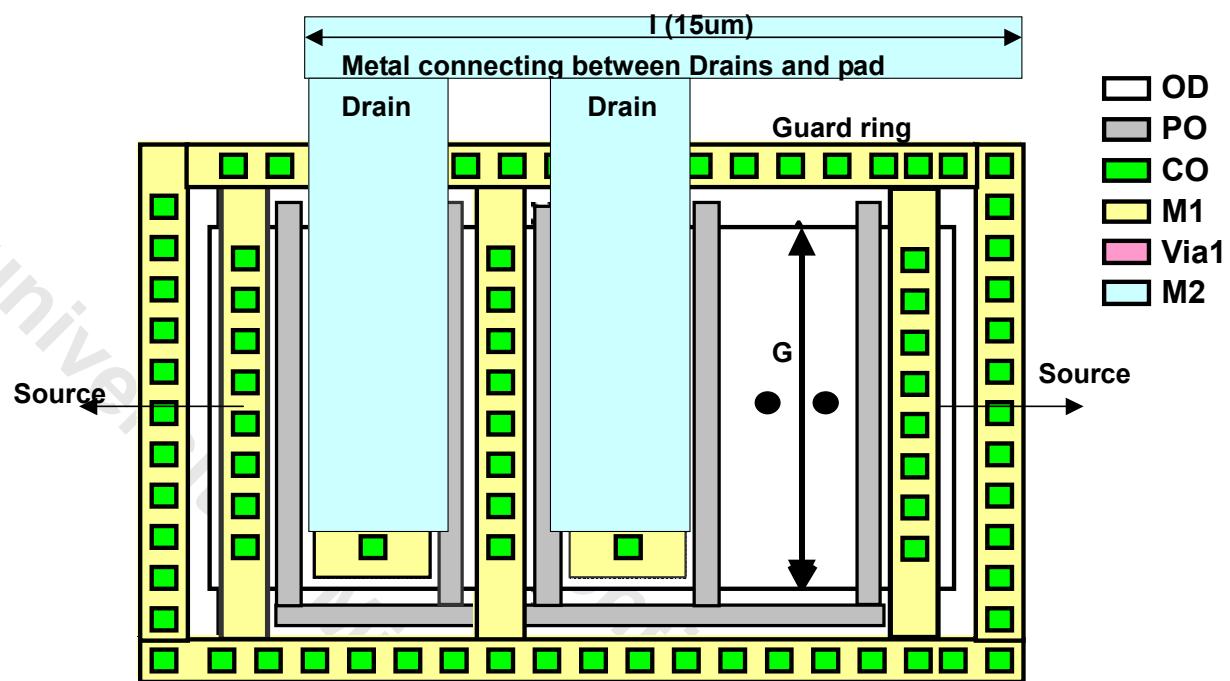


Figure 11.2.8 NMOS and PMOS Layouts for I/O Buffer

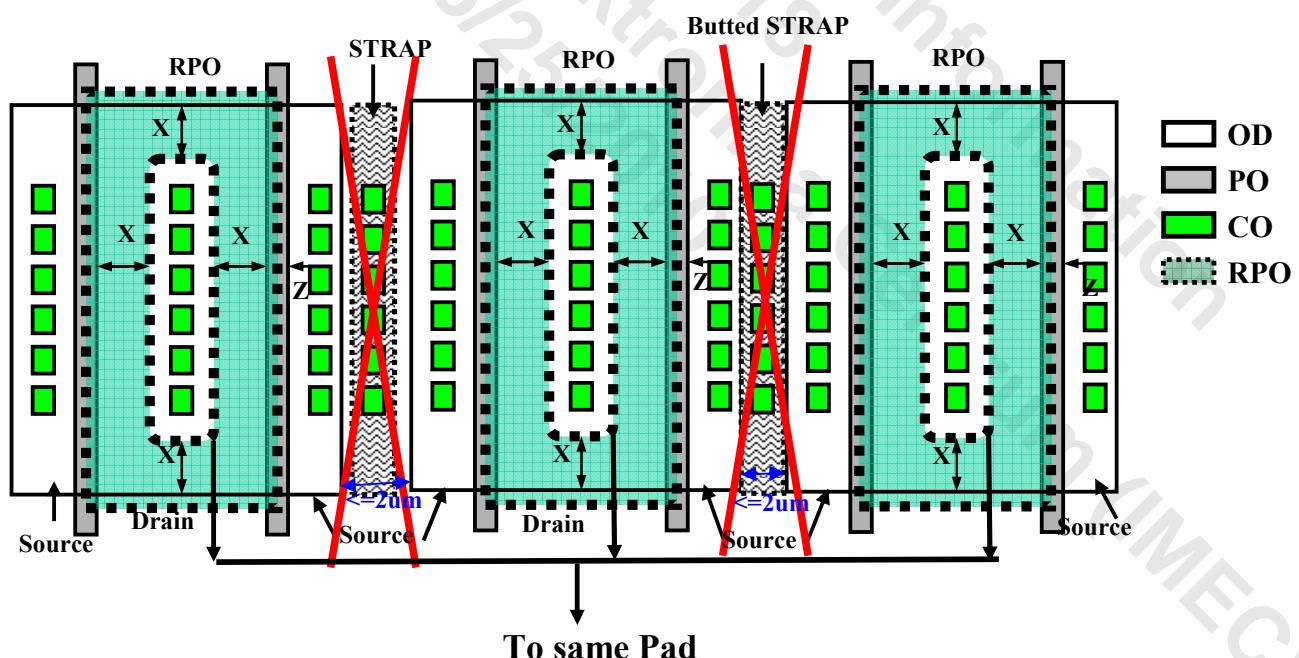


Figure 11.2.9 Butting or Inserted STRAP between two sources of I/O buffer is prohibited

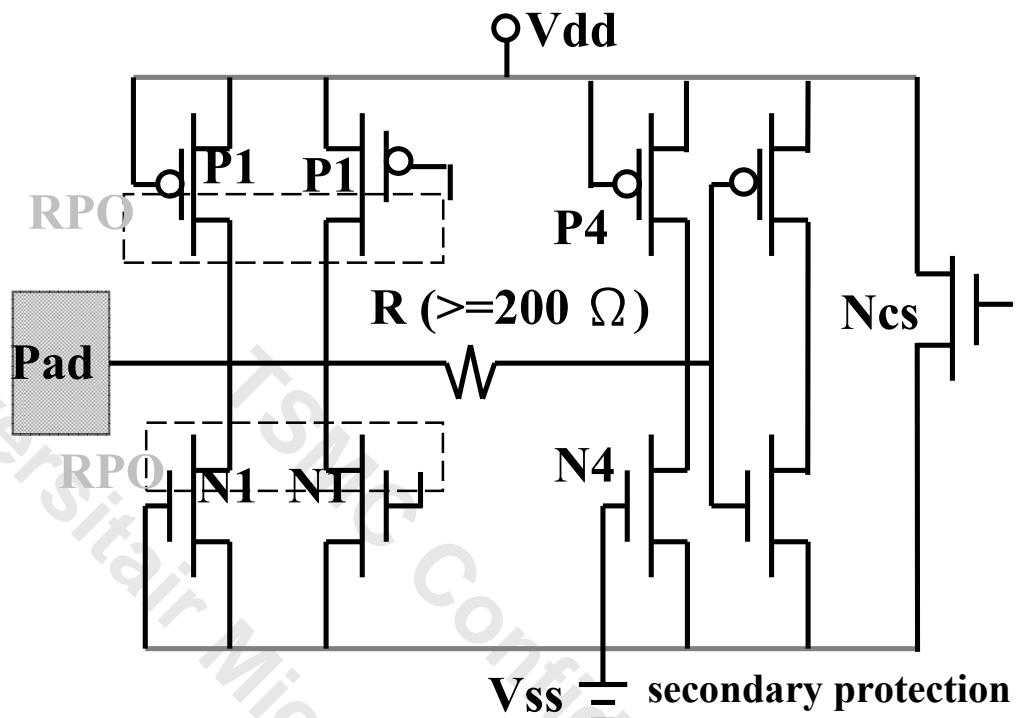


Figure 11.2.10 Regular I/O

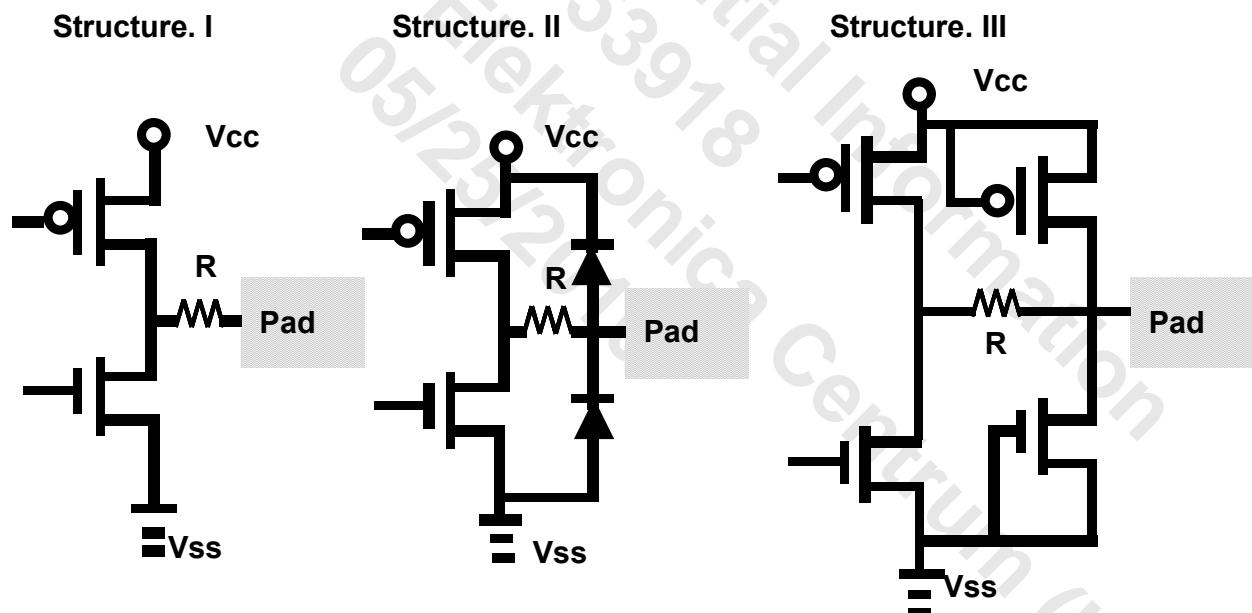


Figure 11.2.11 A resistor before the output transistor

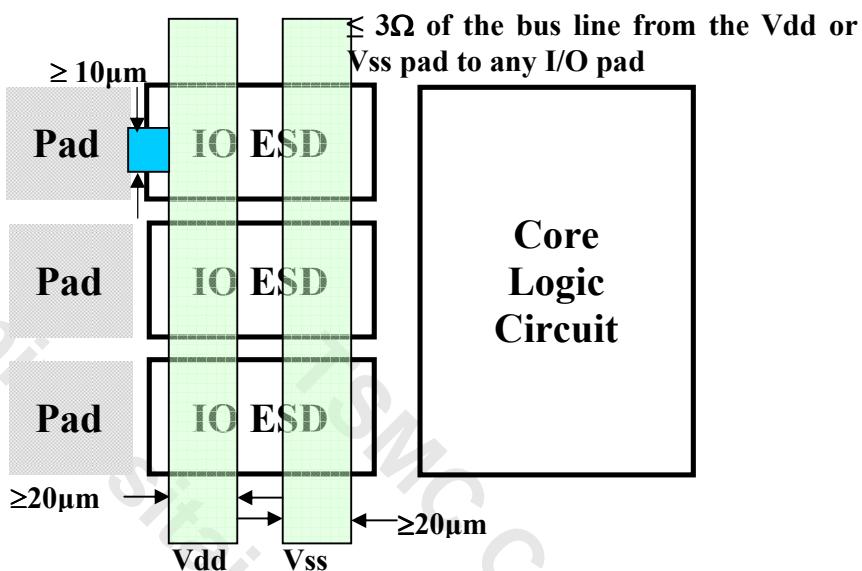


Figure 11.2.12 Bus-Lines Design

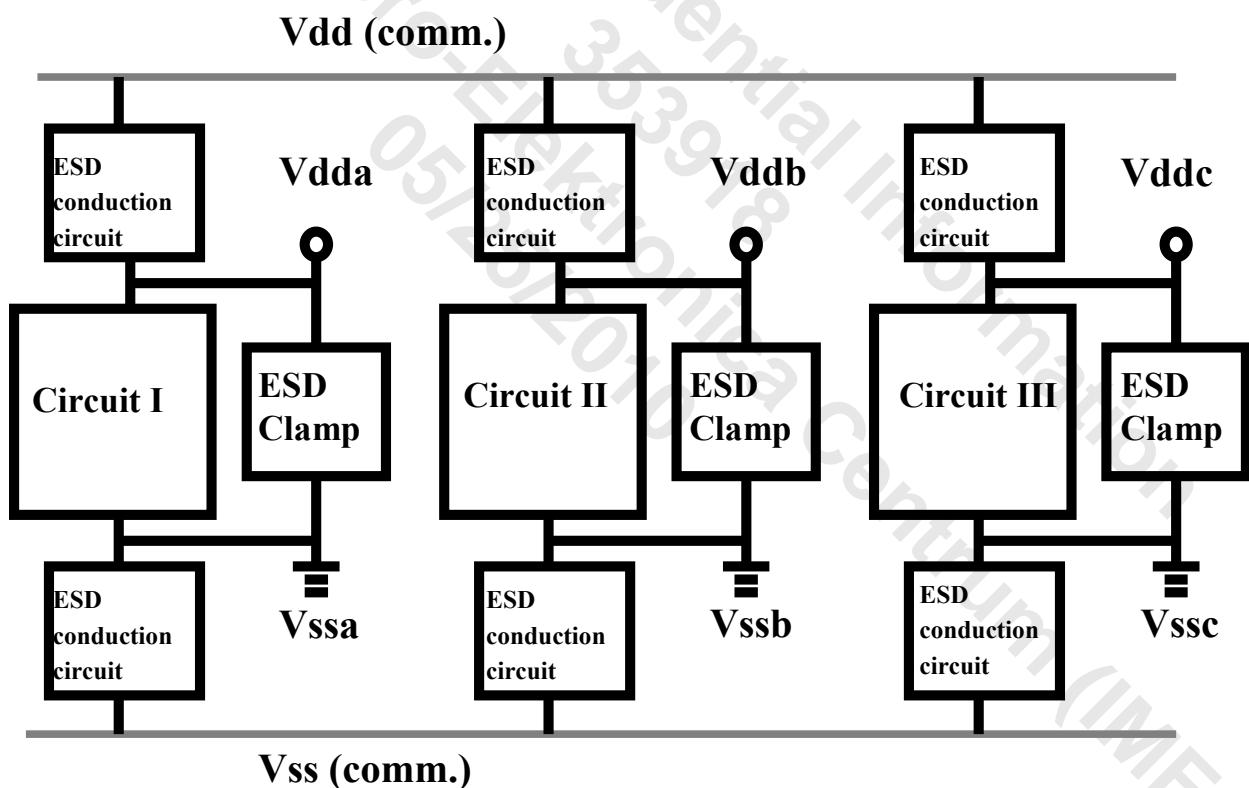


Figure 11.2.13 Schematic of a Multiple Power ESD Protection Design

## 11.2.6.2 Regular I/O (3.3V/2.5V/1.8V/1.2V/1.05V/1.0V RPO Device)

- DRC deck uses (N+ACTIVE AND SDI) AND (all of the related gates partially overlap RPO) to recognize NMOS of Regular I/O.
- DRC deck uses (P+ ACTIVE AND SDI) AND (all of the related gates partially overlap RPO) to recognize PMOS of Regular I/O.

No.	Description	Label	Dimension
ESD.16g	Total finger width for NMOS in same connection of gate or in same connection of drain.		$\geq$ 360
ESD.17g	Total finger width for PMOS in same connection of gate or in same connection of drain.		$\geq$ 360
ESD.18g	Channel length		
	3.3V Regular I/O (in OD33)	L	$\geq$ 0.4
	2.5V Regular I/O (in OD25)	L	$\geq$ 0.35
	1.8V Regular I/O (in OD18)	L	$\geq$ 0.2
	1.2V/1.05V/1.0V Regular I/O (not in OD2)	L	$\geq$ 0.15
ESD.19g	The NMOS and PMOS should have an unsilicided area on the drain side. That is, the RPO mask should block the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device.		
ESD.20g	Overlap of RPO on the drain side to the poly gate (N1/P1 in Figure 10.2.5 and Figure 11.2.9)	Z	= 0.06
ESD.21g	Width of the RPO on the drain side for NMOS. (Figure 11.2.14)	X	$\geq$ 1.95
ESD.22g	Width of the RPO on the drain side for PMOS. (Figure 11.2.14)	X	$\geq$ 1.0
ESD.23g	Space of poly to CO on the source side (Figure 11.2.14)	Y	$\geq$ 0.4

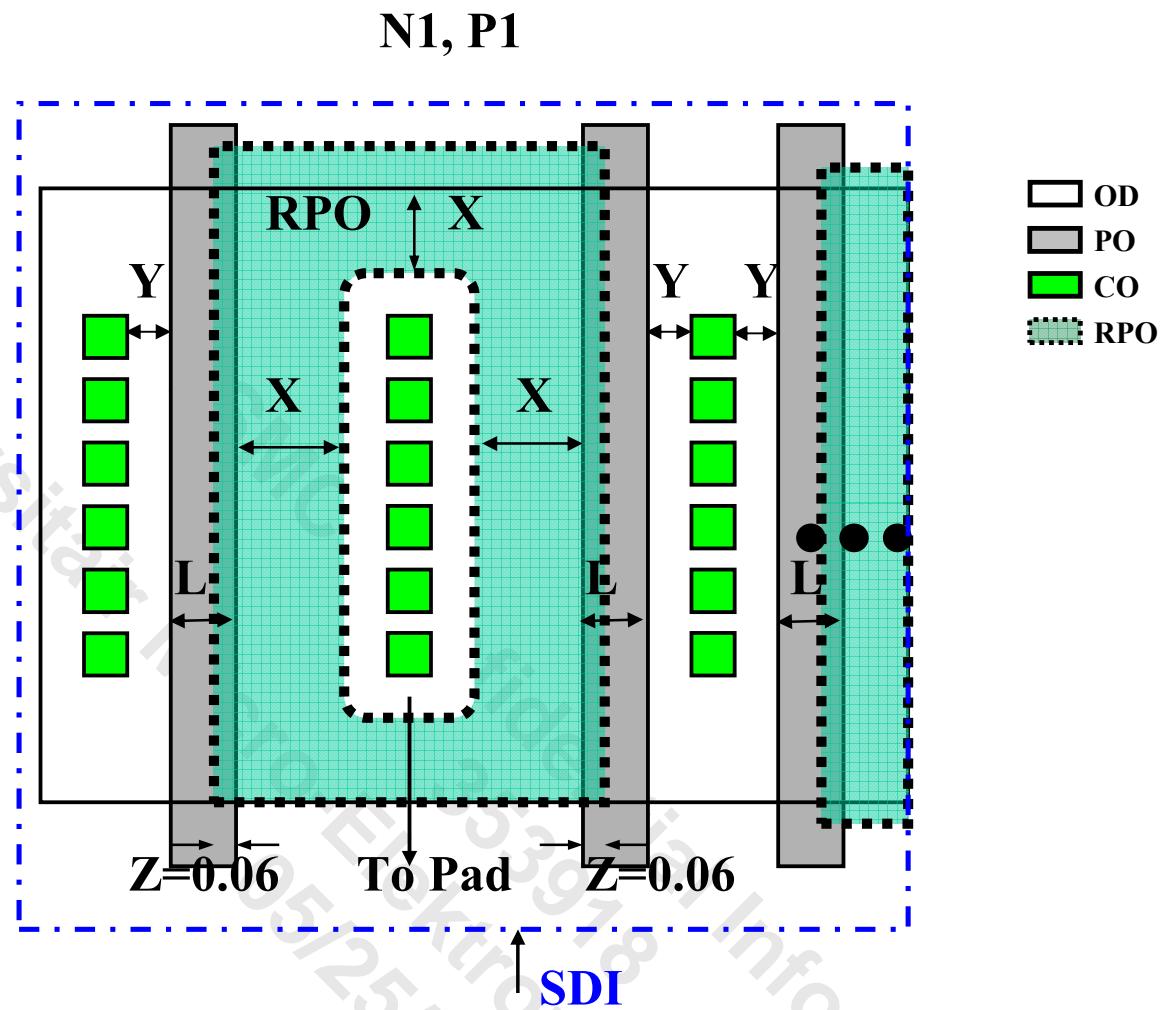


Figure 11.2.14 NMOS and PMOS (N1 and P1 in Figure 10.2.5) for regular I/O

### 11.2.6.3 HV Tolerant I/O

- DRC deck uses (N+ACTIVE AND SDI) AND (some of the related Gate fully inside RPO and some of the related Gate partial overlap RPO) to recognize the NMOS of HV tolerant I/O.
- DRC deck uses (P+ ACTIVE AND SDI) AND (all of the related gates partially overlap RPO) to recognize PMOS of HV tolerant I/O, whose layout is same as PMOS of Regular I/O.
- You have to draw ESD3, which is identical to SDI, in the N2 and N3 transistors. The ESD3 will be used to generate ESD mask by logic operation.

No.	Description	Label		Dimension
ESD.24g	Total finger width for NMOS in same connection of gate or in same connection of drain. ESD.24g has been checked by ESD.16g.		$\geq$	360
ESD.25g	Total finger width for PMOS in same connection of gate or in same connection of drain. ESD.25g has been checked by ESD.17g.		$\geq$	360
ESD.26g	Channel length N2,N3, P2 in Figure 11.2.15, Figure 11.2.16 and Figure 11.2.17.  5V tolerant I/O (in OD33) 3.3V tolerant I/O (in OD25) 2.5V tolerant I/O (in OD18)  PMOS in ESD.26g has been checked by ESD.18g.		L	$\geq$ 0.4
ESD.27g	The NMOS and PMOS should have an unsilicided area on the drain side. That is, the RPO mask should block the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device. PMOS in ESD.27g has been checked by ESD.19g.			
ESD.28g	For NMOS (N2 and N3 in Figure 11.2.15), the RPO needs to cover all inactive poly gates and extend to overlap the N3 gate by Z=0.06um. (Figure 11.2.15) (Figure 11.2.16)	Z	=	0.06
ESD.29g	For PMOS (P2 in Figure 11.2.15 and Figure 11.2.17), overlap of RPO on the drain side to the poly gate ESD.29g has been checked by ESD.20g.	Z	=	0.06
ESD.30g	Width of the RPO on the drain side for NMOS. (Figure 11.2.16)	X	$\geq$	1.95
ESD.31g	Width of the RPO on the drain side for PMOS. (P2 in Figure 11.2.15) (Figure 11.2.17) ESD.31g has been checked by ESD.22g.	X	$\geq$	1
ESD.32g	Space of poly to CO on the source side (Figure 11.2.16) (Figure 11.2.17) PMOS in ESD.32g has been checked by ESD.23g.	Y	$\geq$	0.4
ESD.33g	For NMOS (N2 and N3 in Figure 11.2.15), space of the N2 gate to the N3 gate. (Figure 11.2.16)	S	=	0.25
ESD.34g	The NMOS should have ESD3. DRC only flags (no ESD3 INTERACT N+ACTIVE) for the NMOS of HV tolerant I/O.			
ESD.35g <sup>U</sup>	In order to avoid turning on the diode of P+/NW (P2 in Figure 11.2.15), it is recommended to use floating NW, as your circuit design allows.			

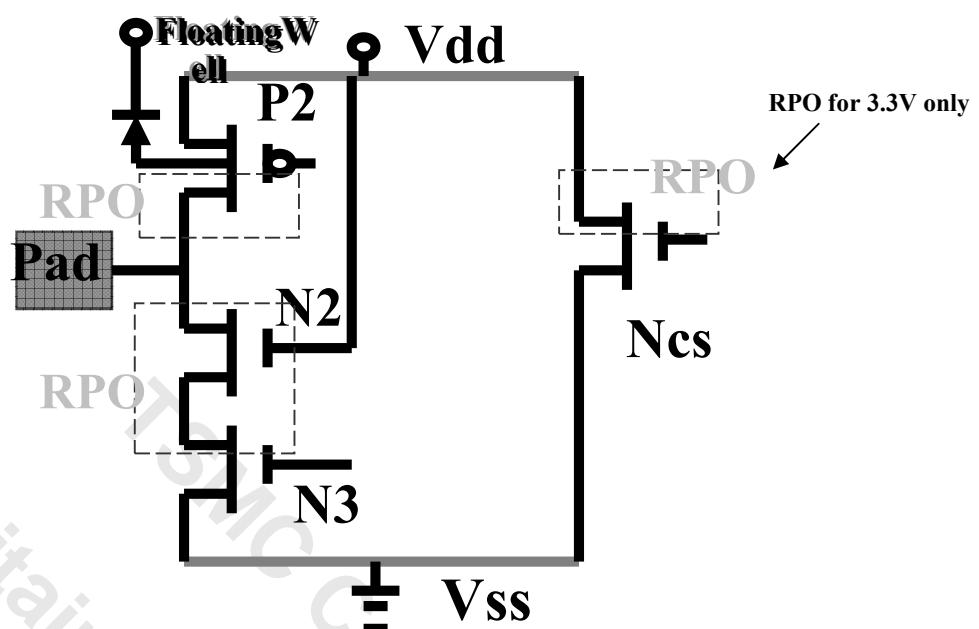


Figure 11.2.15 The schematic of HV Tolerant I/O buffer

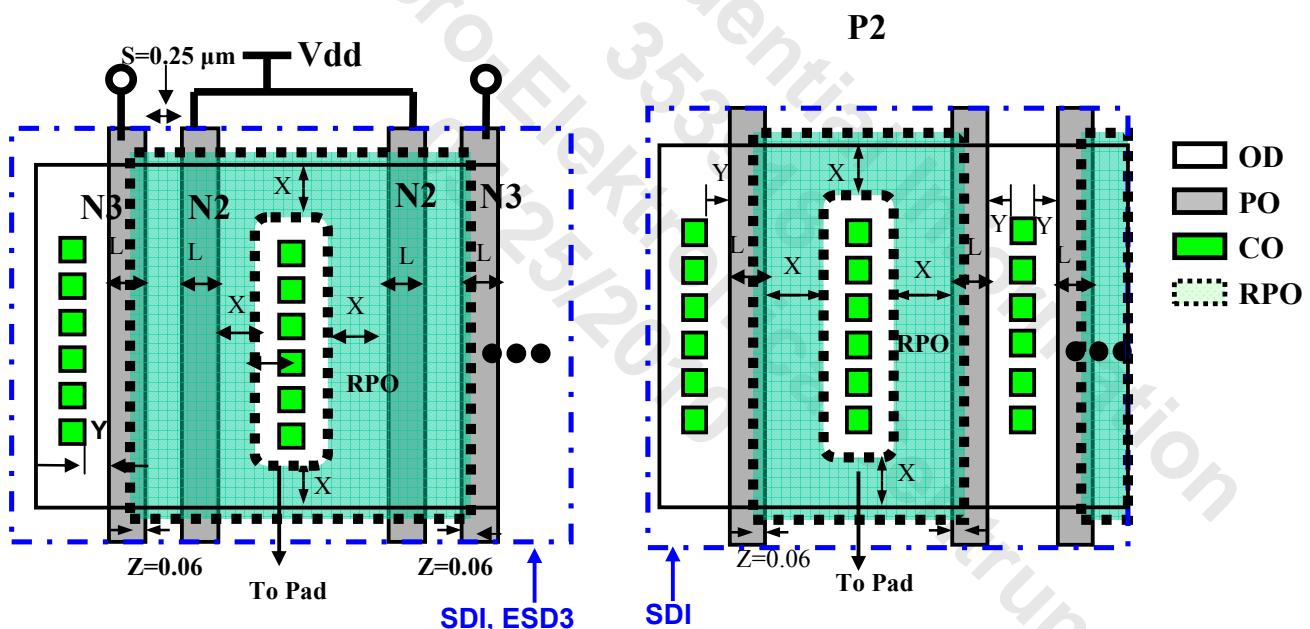


Figure 11.2.16 HV Tolerant NMOS  
(N2/N3 in Figure 11.2.15)

Figure 11.2.17 HV Tolerant PMOS  
(P2 in Figure 11.2.15)

### 11.2.6.4 Power Clamp Device (Ncs)

- DRC deck uses (N+ ACTIVE AND SDI) AND (all of the related gates partially overlap RPO) to recognize 3.3V Power Clamp, whose layout is same as NMOS of Regular I/O.
- DRC deck uses ((N+ ACTIVE AND SDI) NOT INTERACT RPO) to recognize 2.5V/1.8V/1.2V/1.05V/1.0V Power Clamp

No.	Description	Label	Dimension
ESD.36g	Total finger width for 3.3V Power Clamp in same connection of gate or in same connection of drain. (Ncs in Figure 11.2.18). ESD.36g has been checked by ESD.16g.		$\geq$ 360
ESD.37g	Total finger width for 2.5V/1.8V/1.2V/1.05V/1.0V Power Clamp in same connection of gate or in same connection of drain. (Ncs in Figure 11.2.19)		$\geq$ 900
ESD.38g	Channel length		
	3.3V Power Clamp (in OD33) Has checked by ESD.16g.	L	$\geq$ 0.4
	2.5V Power Clamp (in OD25)	L	$\geq$ 0.35
	1.8V Power Clamp (in OD18)	L	$\geq$ 0.2
	1.2V/1.05V/1.0V Power Clamp (not in OD2)	L	$\geq$ 0.15
ESD.39g	The 3.3V Power Clamp (Ncs in Figure 11.2.18) should have an unsilicidized area on the drain side. That is, the RPO mask should block the drain side of the device (except the contact region which should remain silicidized). DRC only flags no RPO in this device. 3.3V Power Clamp in ESD.39g has been checked by ESD.19g.		
ESD.40g	For 3.3V Power Clamp (Ncs in Figure 11.2.18), the RPO needs to cover all inactive poly gates and extend to overlap the second poly gate by Z=0.06um. ESD.40g has been checked by ESD.20g	Z	= 0.06
ESD.41g	Width of the RPO on the drain side for 3.3V Power Clamp (Ncs in Figure 11.2.18) ESD.41g has been checked by ESD.21g	X	$\geq$ 1.95
ESD.42g	Space of poly to CO on the source side for 3.3V Power Clamp (Ncs in Figure 11.2.18) ESD.42g has been checked by ESD.23g	Y	$\geq$ 0.4
ESD.43g <sup>U</sup>	Space of poly to CO on the drain/source side for 2.5V/ 1.8V/ 1.2V/ 1.05V/ 1.0V Power Clamp (Figure 11.2.19) except RC Power Clamp.	Y	$\geq$ 0.2

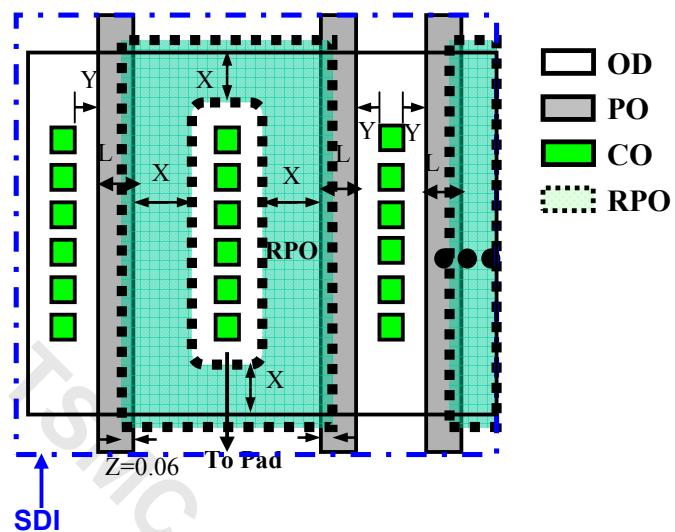


Figure 11.2.18 Ncs Layout for 3.3V in Figure 11.2.10 and Figure 11.2.15

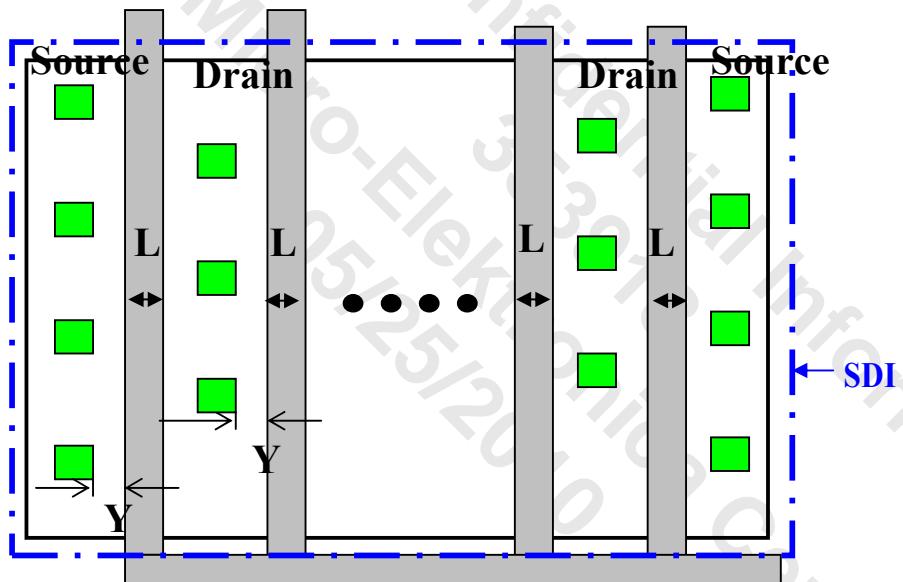


Figure 11.2.19 Ncs Layout for 2.5V, 1.8V, 1.2V, 1.05V, and 1.0V in Figure 11.2.10 and Figure 11.2.15

## 11.2.6.5 RPO and ESD Implant Summary

I/O Device	3.3V/ 2.5V/ 1.8V/ 1.2V/ 1.05V/ 1.0V NMOS for Regular IO	3.3V/ 2.5V/ 1.8V/ 1.2V/ 1.05V/1.0V PMOS for Regular IO	NMOS of 5V/3.3V/2.5V HV Tolerant IO	PMOS of 5V/3.3V/2.5V HV Tolerant IO	3.3V NMOS for Power Clamp	2.5V/1.8V/ 1.2V/1.05V/ 1.0V NMOS for Power Clamp
Minimum RPO width on drain side (X)	1.95	1.0	1.95	1.0	1.95	No need
RPO-to-N2(Z) =	Overlap poly by 0.06	Overlap poly by 0.06	Completely cover N2	Overlap poly by 0.06	Overlap poly by 0.06	No need
N2-to-N3 space =	NA	NA	0.25	NA	NA	No need
RPO coverage in the diffusion region between poly gates	NA	NA	Completely cover diffusion	NA	NA	No need
RPO-to-N3 (Z) =	NA	NA	Overlap N3 by 0.06	NA	NA	No need
ESD implant	3.3V/ 2.5V: Option 1.8V/ 1.2V/ 1.05V/ 1.0V: No need	No	Yes	No	Option	No need
Dummy layer for DRC	SDI	SDI	SDI	SDI	SDI	SDI
Dummy layer for ESD mask making	3.3V/ 2.5V: Option 1.8V/ 1.2V/ 1.05V/ 1.0V: No need	No	ESD3	No	Option: ESD3	No need
Illustration	Figure 11.2.14	Figure 11.2.14	Figure 11.2.15	Figure 11.2.17	Figure 11.2.18	Figure 11.2.19

## 11.2.6.6 Additional Two ESD Structures

In this section, we keep supporting the two previous kinds of ESD structures (design rule before V1.3). However, it is recommended to use the updated structures (section 11.2.6.2~4) to simplify the ESD device structure.

### 11.2.6.6.1 1.8V Regular IO

- DRC deck uses ((N+ ACTIVE AND SDI) INTERACT RPO) AND (the related Gate NOT INTERACT RPO) to recognize 1.8V NMOS of Regular I/O.
- DRC deck uses ((P+ ACTIVE AND SDI) INTERACT RPO) AND (the related Gate NOT INTERACT RPO) to recognize 1.8V PMOS of Regular I/O.
- The ESD performance of this structure is worse than that in section 11.2.6.2, so recommend to use the structure of section 11.2.6.2 for 1.8V regular IO.

No.	Description	Label	Dimension
ESD.44g	Total finger width for NMOS in same connection of gate or in same connection of drain. ESD.44g has been checked by ESD.16g.		$\geq$ 360
ESD.45g	Total finger width for PMOS in same connection of gate or in same connection of drain. ESD.45g has been checked by ESD.17g.		$\geq$ 360
ESD.46g	Channel length (in OD18)	L	$\geq$ 0.2
ESD.47g	The NMOS and PMOS should have an unsilicidized area on the drain side. That is, the RPO mask should be in the drain side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device.		
ESD.48g	RPO on the drain side space to the poly gate (N1/P1 in Figure 11.2.10) and (Figure 11.2.20).	S	= 0.45
ESD.49g	Width of the RPO on the drain side for NMOS. (Figure 11.2.20)	X	$\geq$ 1.5
ESD.50g	Width of the RPO on the drain side for PMOS. (Figure 11.2.20)	X	$\geq$ 1.5
ESD.51g	Space of poly to CO on the source side (Figure 11.2.20)	Y	$\geq$ 0.4
ESD.52g	1.8V regular IO INTERACT OD_25 or OD_33 is not recommended.		

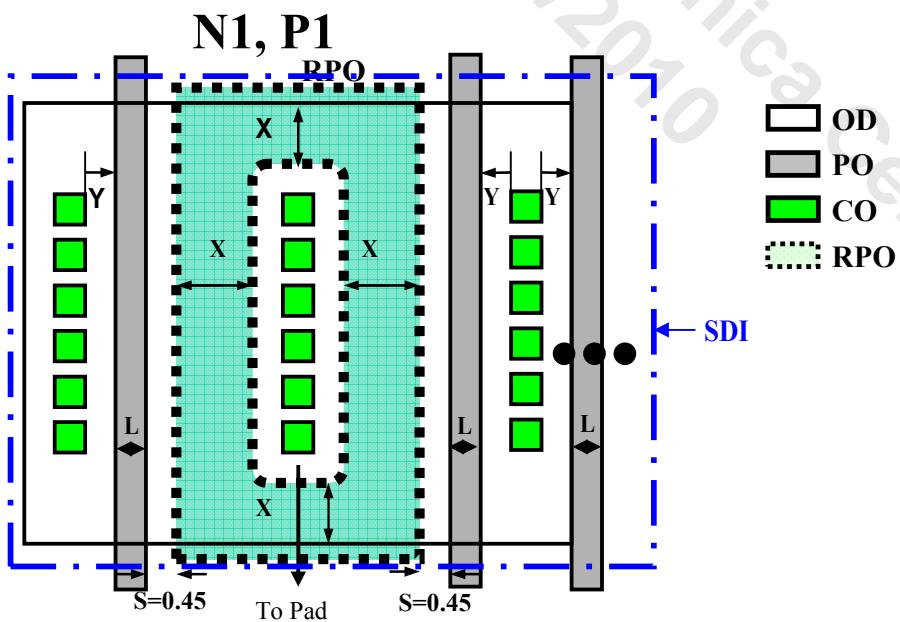


Figure 11.2.20 1.8V I/O NMOS and PMOS (N1 and P1 in Figure 11.2.10)

### 11.2.6.6.2 3.3V, 2.5V Power Clamp (Ncs)

- DRC deck uses ((N+ ACTIVE AND SDI) INTERACT RPO) AND (the related Gate fully inside RPO) to recognize 3.3V, 2.5V Power Clamp.

No.	Description	Label	Dimension
ESD.53g	Total finger width in same connection of gate or in same connection of drain. ESD.53g has been checked by ESD.16g.		$\geq$ 360
ESD.54g	Channel length		
	3.3V Power Clamp (in OD33)	L	$\geq$ 0.4
	2.5V Power Clamp (in OD25)	L	$\geq$ 0.35
ESD.55g	The NMOS should have an unsilicided area on the drain/source side. That is, the RPO mask should be in the drain/source side of the device (except the contact region which should remain silicided). DRC only flags no RPO in this device.		
ESD.56g	Width of the RPO on the drain side for NMOS. (Figure 11.2.21). DRC recognizes the drain side by N+OD NOT connected to PW STRAP.	X	$\geq$ 1.95
ESD.57g	Space of poly to CO on the source side (Figure 11.2.21)	Y	$\geq$ 0.4

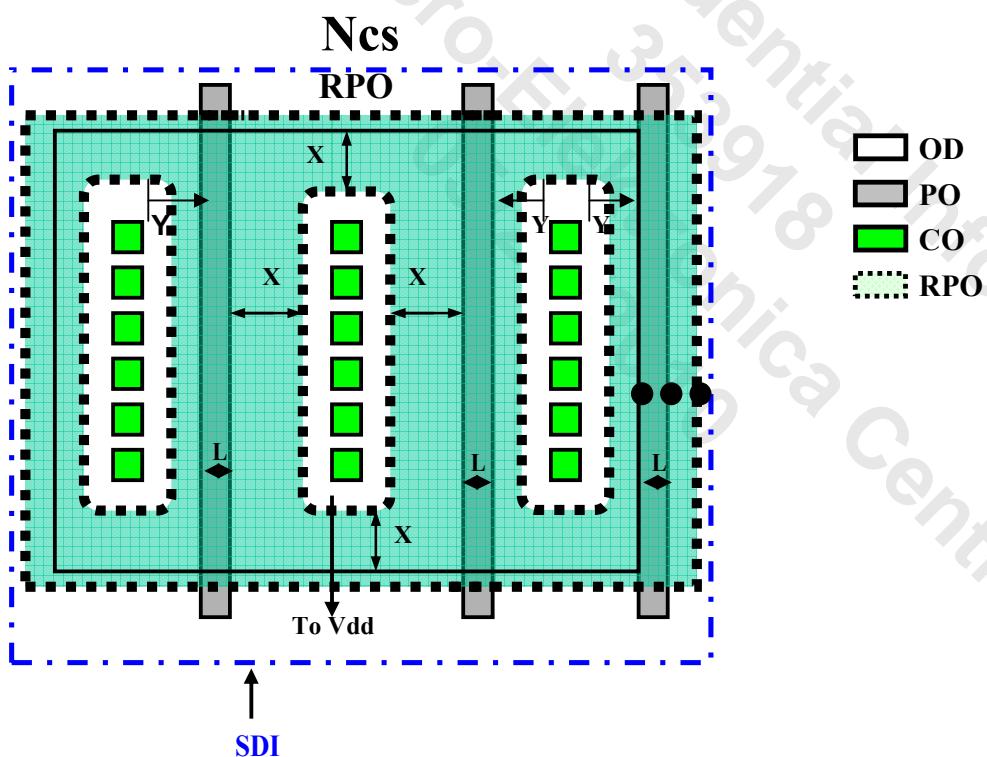


Figure 11.2.21 Ncs Layout for 3.3V or 2.5V in Figure 11.2.10 and Figure 11.2.15

## 11.2.6.7 CDM Protection for Cross Domain Interface

CDM is an increasingly important issue for modern integrated circuits in N90 technology and beyond as the gate oxide thickness keeps on shrinking and the number of power domains continues increasing. With respect to the CDM protection, the cross-domain interface is the most crucial situation as compared with the I/O input gate (defined as ESD.9g in DRM), the gate directly connected to power/ground, and the long signal path without parasitic junction diode. It is because that the fatal CDM charges are mostly accumulated at the power/ground metal buses and easily damage the gate oxide at the interface when the discharge current path crosses the different power domains.

To prevent this kind of CDM damage for the complex power domains, the protection scheme is proposed as Figure 11.2.22 shown. The protection network consists of a resistor, a pair of gate-ground NMOS and gate-Vdd PMOS and active power clamp cells. The resistance and related device dimensions are listed in the following Table 1. Basically, the protection transistors have to be placed as close to the receiver gates as possible, and share the same power/ground and well of the receiver cell. A global active clamp cell should be placed near the cross-domain interface to help conducting the CDM currents. Additionally, the resistance of power bus between the global active power clamp cells is recommended to be smaller than  $1\Omega$ . The turn-on resistance of “current conducting element” should be as small as possible to minimize the voltage drop during CDM zapping.

**Cross Domain interface**

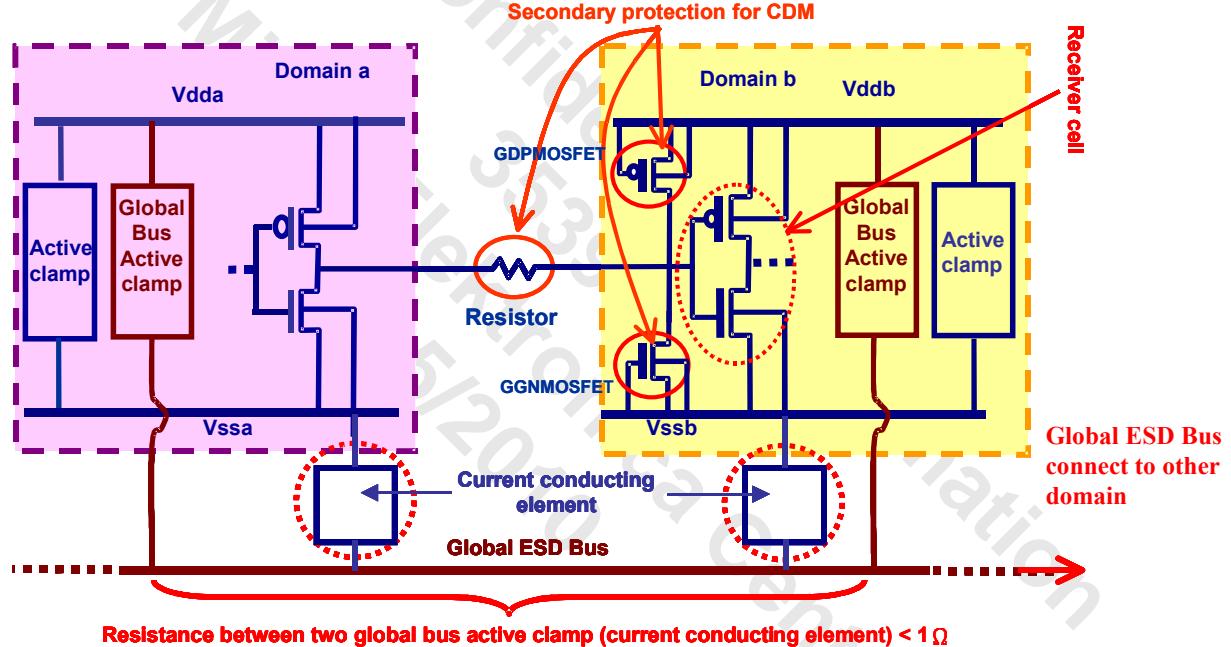


Figure 11.2.22 The protection scheme for cross-domain CDM

**Table 1 The dimensions of CDM protection devices**

Rule No.	Description	Label	Op.	Rule
ESD.58g <sup>U</sup>	Total finger width of 3.3V/ 2.5V/ 1.8V/ 1.2V/ 1.05V/ 1.0V cross-domain secondary protection. (GGN/GDPMOSFET in Figure 11.2.22)		$\geq$	20
ESD.59g <sup>U</sup>	Channel Length of 5V domain b secondary protection. (GGN/GDP MOSFET in Figure 11.2.22)		=	0.8
ESD.59.1g <sup>U</sup>	Channel Length of 3.3V domain b secondary protection. (GGN/GD PMOSFET in Figure 11.2.22)		=	0.4
ESD.59.2g <sup>U</sup>	Channel Length of 2.5V domain b secondary protection. (GGN/GD PMOSFET in Figure 11.2.22)		=	0.35
ESD.59.3g <sup>U</sup>	Channel Length of 1.8V domain b secondary protection. (GGN/GD PMOSFET in Figure 11.2.22)		=	0.2
ESD.59.4g <sup>U</sup>	Channel Length of 1.2V/1.05V/1.0V domain b secondary protection. (GGN/GD PMOSFET in Figure 11.2.22)		=	0.15
ESD.60g <sup>U</sup>	RPO poly resistor is recommended for cross-domain protection. (Resistor in Figure 11.2.22)		$\geq$	200 $\Omega$
ESD.61g <sup>U</sup>	Bus resistance between two global bus active clamps		<	1 $\Omega$

## 11.2.7 Tips for the Power

To avoid ESD damage to internal circuits, the ESD protection design is intended not only for the input, output, or power pins, but also for the whole chip. Of special concern are the digital and analog circuits. In the mixed-mode ICs, separate digital and analog powers are used, and the interface devices between the digital and analog circuits are especially sensitive to ESD damage.

To achieve a better ESD immunity, add inter-power ESD protection circuits by using the following:

1. Add ESD clamping cells/circuits to provide discharge paths between  $V_{DD}$  and  $V_{SS}$  as many as possible. Each set of  $V_{DD}$  and  $V_{SS}$  must have its own power clamp cells.
2. Cross-couple power clamps between multi-power supplies are necessary including  $V_{dd(x)}$  to  $V_{ss(y)}$  and  $V_{dd(x)}$  to  $V_{dd(y)}$ . The x and y denote different power supply combination.
3. Use thin oxide transistors for power-pin ESD protection of thin oxide circuits; thick oxide transistors for power-pin ESD protection of thick oxide circuits.
4. For the ESD conduction circuits connecting separate power lines and the applications of ESD conduction circuits, please refer to the following recommendations in "Approach1".

### 11.2.7.1 Approach 1

All power lines are connected through ESD conduction circuits to a common  $V_{DD}$  and  $V_{SS}$  (Figure 11.2.13).

For a  $V_{DD}$  to  $V_{SS}$  ESD clamping circuit, the recommended ESD protection device is the gate-driven NMOS.

The recommended application guidelines for ESD conduction circuits and ESD clamping circuits are:

- 1) For 1.8V, 2.5V power protection, the recommended minimum width for ESD clamping NMOS is 1000  $\mu\text{m}$ . The larger the better for the total width if there is enough space.
- 2) For 1.0V/1.05V/1.2V power protection, the recommended minimum width is 1900  $\mu\text{m}$ . If there is enough space, the larger total channel width the better ESD immunity.
- 3) Use at least one clamping and/or conduction cell for every  $1.0\Omega$  of power line resistance.
- 4) Power lines should keep ultra low resistance and avoid disconnect. For different powers or grounds with same potential, use bi-directional cell to link them such as diodes.
- 5) The suggested layout for ESD conduction diodes is a finger type P+/N-Well diode with a total area larger than  $2500 \mu\text{m}^2$ , and a periphery length longer than 1100  $\mu\text{m}$ . The OD's and contacts for both ends of the diode should be in an inter-digitated configuration to keep series resistance low and a more uniform current flow.
- 6) Each component of power clamp cell must be surrounded by double guard rings to avoid latch up.
- 7) The turn-on detector circuits should be well designed to avoid mis-trigger subjected to power noise or glitch, for example the RC time constant and the junctions acting as minority collectors.
- 8) Guard rings directly connected to  $V_{DD}$  or  $V_{SS}$  power pad should be as wide as possible, for example the width  $\geq 10\mu\text{m}$ , to avoid burnout of parasitic junction diode during a severe ESD event.
- 9) All layout guidelines are the same as those for I/O buffers, except the source side metal connection should be treated the same as the drain side because the ESD pulse can come from either side.

## 11.2.8 ESD test methodology

### 11.2.8.1 Stress condition and Measurement condition

The ESD test items include HBM and MM which need to meet MIL-STD 883 and EIAJ IC-121, or JEDEC standards. The rise time and decay time of HBM are within 10ns and 150ns, respectively. The rise time and period of MM are within 10ns and 80ns, respectively. The specification for HBM is 2KV and for MM is 200V. The peak currents for 2KV HBM is 1.2A-1.48A and for MM 200V is 2.8A-3.8A.

The ESD test is performed at room temperature. The sample size for ESD test is three devices and each device are stressed three times at each voltage level. The DC parametric and functional testing at room temperature is performed on all devices before ESD testing. The test devices need to meet device data sheet requirements and the DC parameters.

The pin zapping combinations depend on the number of power pin groups like VDD1, VDD2, VSS1, VSS2, GND, etc. Please refer to MIL-STD 883 and EIAJ IC-121, or JEDEC standards.

### 11.2.8.2 Failure criteria

The dc parametric and functional testing of the device should be characterized after each voltage level to check the device ESD failure threshold. The device will be defined as a failure if, after exposure to ESD pulses, it no longer meets the device data sheet requirements using DC parameter and functional testing.

# 12 Reliability Rules and Models

This chapter provides information about the following:

- 12.1 Terminology
- 12.2 Front-end process reliability rules and models
- 12.3 Back-end process reliability rules
- 12.4 Product early failure rate screening guidelines
- 12.5 e-Reliability model system introduction

The information in this chapter can help you meet their product application needs and their design-in reliability goals. The following sections include descriptions about gate oxide integrity, hot carrier effect injection (HCI), threshold stability ( $V_t$  stability), PMOS negative bias temperature instability (NBTI) and current density (EM) specifications.

To provide better and more customized service, TSMC offers an on-line e\_Reliability model system for reliability assessments of 90nm G (general purpose) technology.

## 12.1 Terminology

This section provides definitions for key terms that include in this chapter.

Term	Definition
<b>MTTF</b>	the lifetime in which 50% of the population has failed
<b>0.1% cumulative failure</b>	the lifetime in which 0.1% of the population has failed

## 12.2 Front-End Process Reliability Rules and Models

This section provides information about overdrive voltage, gate oxide integrity, HCI degradation,  $V_t$  instability and negative bias temperature instability.

### 12.2.1 Guidelines for Overdrive Voltage

The 90nm has been qualified for over-drive voltage application in the following. Detail information please refer to 90nm qualification report.

#### 12.2.1.1 Core Device Overdrive Voltage

90nm G: core device are designed to operate at  $V_{cc}=1.0V$ ; and can be operated at over-drive voltage  $V_{cc}=1.2V$  with 5% tolerance.

90nm GT/ 80nmGC/ 80nm GT: core device are designed to operate at  $V_{cc}=1.2V$  with 5% tolerance; over-drive voltage is not allowed.

90nm LP/ 80nmLP: core device are designed to operate at  $V_{cc}=1.2V$ ; and can be operated at over-drive voltage  $V_{cc}=1.4V$  with 5% tolerance.

## 12.2.2 Guidelines for Gate Oxide Integrity

This section provides information to help you predict gate oxide reliability and prevent a time dependent dielectric breakdown (TDDB). TDDB is the breakdown of gate oxide induced by a combination of voltage, junction temperature, and oxide thickness.



**Warning:** Following the guidelines in this section ensures a reliability performance of a 0.1% cumulative failure rate for reference conditions as a function of transistor type, oxide thickness and area, junction temperature, and applied gate voltage. Deviations from these guidelines could result in a potentially unreliable integrated circuit. For specific memory or analog capacitor applications, please consult with TSMC to ensure the required product level reliability specification can be met.

### 12.2.2.1 Gate Oxide Life Time Prediction Model

**For core thin gate oxide:**

$$\text{Time to failure} \propto (V_{cc})^{-n} \times \exp(E_a/K_T) \times (A_{ox})^{-1/\beta} \dots \quad \text{equation (1)}$$

**For I/O thick gate oxide:**

$$\text{Time to failure} \propto \exp(-\gamma \times V_{cc}) \times \exp(E_a/K_T) \times (A_{ox})^{-1/\beta} \dots \quad \text{equation (2)}$$

Where:

**A<sub>ox</sub>** is the total gate oxide area on silicon (unit:  $\mu\text{m}^2$ )

**T** is the absolute junction temperature (unit: K)

**V<sub>cc</sub>** is the gate voltage (unit: volt)

**n** is the power law exponent of the voltage acceleration factor for core thin gate oxide

**$\gamma$**  is the voltage acceleration factor for I/O thick gate oxide

**E<sub>a</sub>** is the thermal activation energy

**k** is the Boltzmann's constant ( $(8.617 \times 10^{-5}) \text{ eV/K}$ )

**$\beta$**  is the Weibull shape factor (distribution spread)

### 12.2.2.2 Failure Mechanism

When an electron current is passed through gate oxide, defects such as electron traps, interface states, positively charged donor-like traps, etc., and so on, gradually build up in the gate oxide until a conduction path is formed, followed by thermal run away.

According to the anode hole injection model, injected electrons generate holes at the anode that can tunnel back into the oxide. Intrinsic breakdown occurs when a critical hole density is reached.

## 12.2.2.3 Test Methodology

### 12.2.2.3.1 Measurement Conditions

- $I_g$  is the gate current with  $V_b=V_s=V_d=GND$ .  $T=125^{\circ}C$ .
- $V_g$  is set to 5.0 ~ 8.5 volts for thick (I/O) gate oxide.
- $V_g$  is set to 2.0 ~ 3.5 volts for thin (core) gate oxide.

### 12.2.2.3.2 Stress Conditions

At least 30 samples constitute a sample size for each stress condition:

- To determine the **voltage acceleration factor ( $\gamma$ )**, 3 stress voltages are used at each fixed stress temperature.
- To determine the **thermal activation energy ( $E_a$ )**, 3 stress temperatures are used at each fixed stress voltage.

### 12.2.2.3.3 Failure Criteria

The failure criterion for core thin (core) gate oxide is an onset of the first soft breakdown when there is an gate current ( $I_g$ ) progressively increasing in noise or variance. The failure criterion for thick (I/O) gate oxide is a hard breakdown.

The following table provides an example of maximum gate voltage ( $V_{ccmax}$ ) calculations for 90nm G core gate oxide applications. The reference conditions are a gate oxide area of  $0.1 \text{ cm}^2$ , a cumulative failure rate of 0.1%, and a duty factor of 100%.

If the operation conditions do not include in the table, designers can get access the lifetime and the  $V_{ccmax}$  prediction through TSMC's on-line e-Reliability model for 90nmG.

**Table 12.2.1 90nm G/GT/LP, 85nm LP and 80nmGC/GT/HS/LP Core Maximum Gate Voltage for Reference Condition with 0% Tolerance;**

**Area (Aox=0.1cm<sup>2</sup>);  
Failure Rate (Fref=0.1%)  
Duty Factor of 100%**

90G/GT Core device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	1.53	1.50	1.47	1.44	10	1.41	1.36	1.32	1.29
7	1.55	1.51	1.48	1.46	7	1.42	1.38	1.34	1.30
5	1.56	1.52	1.49	1.47	5	1.44	1.39	1.35	1.32

90LP Core device:

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	2.2	2.16	2.13	2.11	10	2.16	2.09	2.03	1.98
7	2.21	2.18	2.15	2.12	7	2.18	2.11	2.05	2.00
5	2.23	2.19	2.16	2.14	5	2.20	2.13	2.07	2.01

85LP 1.2V Core device:

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	2.19	2.16	2.13	2.10	10	2.24	2.18	2.12	2.07
7	2.20	2.17	2.14	2.11	7	2.26	2.19	2.13	2.09
5	2.21	2.18	2.15	2.12	5	2.27	2.21	2.15	2.10

80GT Core device:

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	1.48	1.45	1.42	1.40	10	1.45	1.40	1.36	1.32
7	1.50	1.46	1.44	1.41	7	1.46	1.41	1.37	1.34
5	1.51	1.47	1.45	1.42	5	1.48	1.43	1.39	1.35

80GC Core device:

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	1.47	1.44	1.41	1.38	10	1.41	1.36	1.31	1.27
7	1.49	1.45	1.42	1.40	7	1.42	1.37	1.33	1.29
5	1.50	1.46	1.43	1.41	5	1.44	1.38	1.34	1.30

80LP Core device:

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	2.33	2.29	2.25	2.22	10	2.23	2.17	2.11	2.05
7	2.35	2.31	2.27	2.23	7	2.25	2.18	2.12	2.07
5	2.37	2.32	2.28	2.25	5	2.27	2.20	2.14	2.08

80HS Core device:

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	1.19	1.17	1.14	1.12	10	1.19	1.16	1.13	1.10
7	1.20	1.18	1.15	1.13	7	1.20	1.17	1.14	1.11
5	1.21	1.19	1.16	1.14	5	1.21	1.18	1.15	1.12

**Table 12.2.2 90nm G/GT/LP, 85nm LP and 80nm GC/GT/HS/LP IO Maximum Gate Voltage for Reference Condition with 0% Tolerance;**  
**Area (Aox=0.01cm<sup>2</sup>);**  
**Failure Rate (Fref=0.1%)**  
**Duty Factor of 100%**

90G\_LP 2.5VIO device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	4.00	3.88	3.78	3.69	10	4.79	4.64	4.52	4.40
7	4.04	3.93	3.83	3.73	7	4.83	4.69	4.56	4.44
5	4.08	3.97	3.87	3.78	5	4.87	4.73	4.60	4.49

85LP 2.5V I/O device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	4.33	4.19	4.07	3.96	10	4.45	4.27	4.12	3.97
7	4.37	4.23	4.11	4.00	7	4.50	4.32	4.16	4.02
5	4.42	4.28	4.15	4.04	5	4.55	4.37	4.21	4.07

85LP 3.3V I/O device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	5.08	4.96	4.85	4.76	10	5.16	5.03	4.91	4.81
7	5.15	5.03	4.92	4.83	7	5.23	5.10	4.99	4.88
5	5.22	5.10	4.99	4.90	5	5.31	5.18	5.06	4.96

80GT 2.5VIO device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	4.11	3.97	3.84	3.73	10	4.49	4.33	4.19	4.06
7	4.16	4.02	3.89	3.78	7	4.54	4.38	4.24	4.11
5	4.20	4.06	3.94	3.82	5	4.58	4.42	4.28	4.15

80GC 2.5VIO device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	4.05	3.91	3.78	3.66	10	4.40	4.23	4.07	3.93
7	4.10	3.96	3.83	3.71	7	4.45	4.28	4.12	3.98
5	4.15	4.00	3.87	3.76	5	4.50	4.32	4.17	4.03

80LP 2.5VIO device

NMOS					PMOS				
LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C	LifeTime (years)	T= 65°C	T= 85°C	T= 105°C	T= 125°C
10	4.10	3.95	3.81	3.69	10	4.69	4.52	4.37	4.23
7	4.15	4.00	3.86	3.74	7	4.73	4.57	4.41	4.28
5	4.20	4.05	3.91	3.79	5	4.78	4.61	4.46	4.32

## 12.2.3 Guidelines for Hot Carrier Injection Effect (HCI)

Hot carriers are holes or electrons that have been accelerated to a high energy by a local electric field. Hot carrier degradation can have a significantly impact circuit performance and functionality. It is important for circuit designers to carefully check the lifetime degradation of their designs caused by hot carriers injection (HCI). Cumulative degradation and process variation must be taken into account for both burn-in, field operation, and overdrive applications.

### 12.2.3.1 Life Time Prediction Model for Device Degradation

Owing to the importance of hot carrier injection on circuit operation, you should employ detailed models to calculate device degradation during circuit operation and to simulate the impact on circuit operation. The following is a general model for the degradation of device characteristics:

$$MTTF = A \times f(L,W) \times (\Delta\%)^{1/n} \times \exp[B \times (1/V_{ds})] \times \exp[E_a/k(1/T)] \quad \text{equation (3)}$$

where:

**MTTF** is the mean time to failure

**L** is the drawn channel length (unit:  $\mu\text{m}$ )

**W** is the drawn channel width (unit:  $\mu\text{m}$ )

$\Delta\%$  is the percentage degradation of an electrical parameter (for example, 10%  $I_{dsat}$ , 10%  $G_m$ .)

**V<sub>ds</sub>** is the drain to source bias (unit: volt)

**n** is the power law factor of time dependent degradation

**E<sub>a</sub>** is the activation energy

**k** is the Boltzmann constant ( $(8.617 \times 10^{-5}) \text{ eV/K}$ )

**T** is the absolute junction temperature (unit: K)

**A** and **B** are empirical fitting parameters

### 12.2.3.2 Failure Mechanism:

A percentage of these energetic hot carriers will impact the lattice and create electron-hole pairs. The created electron-hole pairs will create even more pairs later on. If the hot carriers have a kinetic energy larger than the silicon-insulator barrier height, some of these carriers may surmount the barrier and be propelled toward the insulator that has a moderate or higher gate bias. These carriers can either be trapped in the oxide region or at the Si-SiO<sub>2</sub> interface. The trapped charges from HCI stress have the following effect on the transistors:

1. Shift in the  $V_t$  (threshold voltage) of the device.
2. Reduced the mobility of the conducting carriers.
3. Reduced device drain current.
4. Increased effective series resistance, from a charge trapped above the S/D extension region.
5. Degraded sub-threshold slope.

These transistor changes are dependent on the amount of HCI stress that is incurred. The HCI stress in the transistor is dependent on several factors:  $L_{gate}$ ,  $V_{ds}$ ,  $V_{gs}$ ,  $V_{bs}$ , and temperature.

## 12.2.3.3 Test Methodology

### 12.2.3.3.1 Measurement Conditions

1.  $I_{dsat}$  is the forward saturation region drain current with  $V_d=V_g=V_{cc}$ ,  $V_s=V_b=GND$ .
2.  $I_{dlin}$  is the forward linear region drain current with  $V_d=0.1 \times V_{cc}V_{cc}$ ,  $V_g=V_{cc}$ ,  $V_s=V_b=GND$ .
3.  $G_m$  is the maximum transconductance by with  $V_d=0.1V$ ,  $V_s=V_b=GND$ .
4.  $V_t$  is the threshold voltage extrapolated at maximum transconductance.

### 12.2.3.3.2 Stress Conditions

1. The core device is stressed at  $V_d=V_g < 90\%$  device breakdown voltage;  $V_s=V_b=GND$ .
2. The IO device is stressed at a given  $V_d < 90\%$  device breakdown voltage;  $V_g$  is at the maximum substrate current for a given  $V_d$ ;  $V_s=V_b=GND$ .

### 12.2.3.3.3 Dimension Ranges of Stress Devices

1. **Channel Length:** 0.09  $\mu m$  ~ 0.12  $\mu m$  for core N/PMOS devices,  
0.26  $\mu m$  ~ 0.415  $\mu m$  for 2.5V I/O N/PMOS devices,
2. **Channel Width:** 0.3  $\mu m$  ~ 10  $\mu m$  for core N/PMOS devices,  
0.6  $\mu m$  ~ 10  $\mu m$  for 2.5V I/O N/PMOS devices

### 12.2.3.3.4 Failure Criteria:

The failure criterion for all devices is 10% degradation.

Spec= DC 0.2 years, AC/DC factor= 50 for core and IO.

### 12.2.3.3.5 DC Lifetime and Vmax

DC Lifetime definition: 0.1% cum

Criteria:  $I_{dsat}$  shift 10%

N90LP:

1.2V Core (STDVT): NMOS = 113.55 yrs @ 1.32V, Vmax of NMOS=1.5V for W/L=10/0.1um, 25°C  
PMOS = 1.67E+5yrs @1.32V, Vmax of PMOS= 1.8V for W/L=10/0.1um, 25°C  
2.5V IO: NMOS = 1.9 yrs @ 2.75V; PMOS = 128.18yrs @ 2.75V for W/L = 10/0.28um, 25°C;

N90G:

1.0V Core (STDVT): NMOS = 2447.12 yrs @ 1.1V, Vmax of NMOS=1.26V for W/L=10/0.1um, 25°C  
PMOS = 9.25E+4yrs @1.1V, Vmax of PMOS= 1.4V for W/L=10/0.1um, 25°C  
2.5V IO: NMOS = 1.45 yrs @ 2.75V; PMOS = 23.18 yrs @ 2.75V for W/L = 10/0.28um, 25°C;

N90GT:

1.2V Core (STDVT): NMOS = 12.09 yrs @ 1.26V, Vmax of NMOS=1.4V for W/L=10/0.1um, 25°C  
PMOS = 320.21 yrs @1.26V, Vmax of PMOS= 1.4V for W/L=10/0.1um, 25°C  
2.5V IO: NMOS = 1.47 yrs @ 2.75V; PMOS = 26yrs @ 2.75V for W/L = 10/0.28um, 25°C;

## N85LP:

1.2V Core (STDVT): NMOS = 100.07 yrs @ 1.32V, Vmax of NMOS=1.56V for W/L=9.4/0.094um, 25°C  
PMOS = 4748.4yrs @1.32V, Vmax of PMOS= 1.73V for W/L=9.4/0.094um, 25°C  
2.5V IO: NMOS = 1.26 yrs @ 2.75V; PMOS = 15.43yrs @ 2.75V for W/L = 9.4/0.28um, 25°C;  
3.3V IO: NMOS = 0.33 yrs @ 3.63V; PMOS = 0.72yrs @ 3.63V for W/L = 9.4/0.38um, 25°C;

## N85G:

1.0V Core (STDVT): NMOS = 7.40e3 yrs @ 1.32V, Vmax of NMOS=1.44V for W/L=9.4/0.094um, 25°C  
PMOS = 1.4e5yrs @1.32V, Vmax of PMOS= 1.53V for W/L=9.4/0.094um, 25°C  
1.8V IO: NMOS = 0.54 yrs @ 1.98V; PMOS = 7.51yrs @ 1.98V for W/L = 9.4/0.2um, 25°C;  
2.5V IO: NMOS = 1.23 yrs @ 2.75V; PMOS = 19.36yrs @ 2.75V for W/L = 9.4/0.28um, 25°C;  
3.3V IO: NMOS = 0.33 yrs @ 3.63V; PMOS = 0.69yrs @ 3.63V for W/L = 9.4/0.38um, 25°C;

## N80LP:

1.2V Core (STDVT): NMOS = 28.1 yrs @ 1.32V, Vmax of NMOS=1.45V for W/L=9/0.09um, 25°C  
PMOS = 3221.09yrs @1.32V, Vmax of PMOS= 1.5V for W/L=9/0.09um, 25°C  
2.5V IO: NMOS = 5.44yrs @ 2.75V; PMOS = 20.05yrs @ 2.75V for W/L = 9/0.28um, 25°C;

## N80GC:

1.0V Core (STDVT): NMOS = 1259.97 yrs @ 1.1V, Vmax of NMOS=1.4V for W/L=9/0.09um, 25°C  
PMOS = 9.99E+4yrs @1.32V, Vmax of PMOS= 1.4V for W/L=9/0.09um, 25°C  
2.5V IO: NMOS = 4.59yrs @ 2.75V; PMOS = 22.82yrs @ 2.75V for W/L = 9/0.28um, 25°C;

## N80GT:

1.2V Core (STDVT): NMOS = 7.58 yrs @ 1.32V, Vmax of NMOS=1.45V for W/L=9/0.09um, 25°C  
PMOS = 514.7yrs @1.32V, Vmax of PMOS= 1.5V for W/L=9/0.09um, 25°C  
2.5V IO: NMOS = 1.68yrs @ 2.75V; PMOS = 170.86yrs @ 2.75V for W/L = 9/0.28um, 25°C;

## 12.2.4 Guidelines for Threshold Instability

### 12.2.4.1 Failure Mechanism

Mobile ionic contaminants in an MOS device can induce instability in device characteristic. To monitor the ion-induced instability of NMOS, TSMC's test methodology uses the threshold voltage shift ( $V_t$ ) under voltage stress in a high temperature environment. TSMC's test methodology can also monitor PMOS interface states that are induced by hole injection.

### 12.2.4.2 Test Methodology

The following table shows the specifications for  $V_t$  shift testing.

**Table 12.2.2 V<sub>t</sub> Shift Specifications**

	1.0V / 1.2V Core PMOS	1.0V / 1.2V Core NMOS	2.5V I/O PMOS	2.5V I/O NMOS	1.8V / 3.3V I/O PMOS	1.8V / 3.3V I/O NMOS
<b>V<sub>t</sub> shift</b>	15%	15%	15%	15%	15%	15%
<b>W/L (μm)</b>	On rule	On rule	On rule	On rule	On rule	On rule

**Table Notes:**

**V<sub>t</sub> shift** =  $(V_t \text{ post-}V_t \text{ initial}) / V_t \text{ initial} \times 100\%$ .

**V<sub>t</sub> initial** and **V<sub>t</sub> post** are measured at room temperature.

**Stress Voltage** is 1.1 V<sub>cc</sub>.

**Stress environment temperature** is 150°C.

**W** is the drawn channel width (unit: μm).

**L** is the drawn channel length (unit: μm).

## 12.2.5 Guidelines for Negative Bias Temperature Instability (NBTI)

Negative Bias Temperature Instability (NBTI) is a key reliability item below 65nm technology that is of newer aging issue in p-channel MOS devices stressed with negative gate voltages. The high temperature and bias on Gate terminal will cause significantly NBTI effect, which increase in the threshold voltage and decrease in drain current. It is significant for circuit designers to consider the lifetime degradation ratio of their designs caused by negative bias temperature instability (NBTI) and must be taken into account for burn-in, field operation, and overdrive applications from process variation.

### 12.2.5.1 Lifetime Prediction Model for Negative Bias Temperature Instability

The lifetime for the negative bias temperature instability (NBTI) is correlated with voltage, temperature, parametric failure criteria, device length, and device width.

$$MTTF = A \times f(L, W) \times (I_{dsat}\%)^{1/n} \times \exp[-\gamma \times V_g] \times \exp[E_a/k(1/T)]$$

**equation (4)**

where:

**L** is the drawn channel length (unit:  $\mu\text{m}$ )

**W** is the drawn channel width (unit:  $\mu\text{m}$ )

**$I_{dsat}\%$**  is the criteria of  $I_{dsat}$  degradation percentage

**n** is the power law factor of time dependent degradation

**$V_g$**  is the operation gate bias (unit: volt)

**$\gamma$**  is the voltage acceleration factor

**$E_a$**  is the activation energy

**k** is the Boltzmann constant ( $(8.617 \times 10^{-5}) \text{ eV/K}$ )

**T** is the absolute junction temperature (unit:K )

**A** is a constant

### 12.2.5.2 Lifetime Prediction Model for AC

For an acceptable specification, the AC lifetime must be considered. Currently, TSMC's proposed standard is an AC-to-DC factor of 2, based on the assumption that the off-state operation occupies half the product's operation time. The accepted AC lifetime is 10 years, with a DC lifetime of 5 years at temperature 125°C.

### 12.2.5.3 Failure Mechanism

The PMOS device has a lower mobility than the NMOS device. Mobility for a PMOS device is decreased further, and significantly, by the negative bias stress on the transistor gate under a high temperature environment. A hole injected under negative bias into the oxide-substrate interface increases interface states. The electrochemical reaction induces device instability that is enhanced by boron implanted in the gate poly engineering process. Logic circuits could suffer from the driving current decrease . , and analog circuits could suffer from the mismatching or shift of the threshold voltage.

Negative bias temperature stress under constant voltage (DC) causes the generation of interface trap (NIT) before the gate oxide & Si substrate, which translate to device  $V_t$  shift & Ion loss. The NBTI effect is more severe for PMOS than NMOS due to the process of holes in the PMOS inversion layer that are known to interact with oxide state.

## 12.2.5.4 Test Methodology

### 12.2.5.4.1 Measurement Condition

$I_{dsat}$  is the forward saturation region of drain current with  $V_d = V_g = V_{cc}$ ,  $V_s = V_b = \text{GND}$  at a high stress temperature.

### 12.2.5.4.2 Stress Conditions

1. **Sample size** is at least 5 samples for each stress condition.
2. **Voltage range** is 7 ~ 13 MV/cm for core devices, and 8 ~ 11 MV/cm for I/O devices.
3. **Temperature range** is 125°C ~ 175°C.
4. **Channel length** is 0.09 μm ~ 1.2 μm for core devices, and 0.26 μm ~ 1.2 μm for 2.5V I/O devices.
5. **Channel Wwidth** is 0.3 μm ~ 10 μm for core devices, and 0.5 μm ~ 10 μm for I/O devices.

### 12.2.5.4.3 Failure Criteria

The failure criteriaon for parameters of NBTI is  $I_{dsat}$  10% degradation.

Spec= DC 5 years, AC/DC factor= 2

### 12.2.5.4.4 DC Lifetime and Vmax

DC Lifetime definition: 0.1% cum.

N90LP

- a) Criteria:  $I_{dsat}$  shift 10%:

1.2V Core (STDVT): PMOS = 49.7yrs @ 1.32V for W/L=10/0.1, 125C  
 $V_{max}$  of PMOS = 1.5 V for W/L=10/0.1, 125C  
2.5V IO: PMOS = 26.47yrs @ 2.75V for W/L=10/0.28, 125C  
 $V_{max}$  of PMOS = 3.0V for W/L=10/0.28, 125C

- b) Criteria: VT shift 50mA:

1.2V Core (STDVT): PMOS = 44.36yrs @ 1.32V for W/L=10/0.1, 125C  
 $V_{max}$  of PMOS = 1.5V for W/L=10/0.1, 125C

N90G

- a) Criteria:  $I_{dsat}$  shift 10%:

1.0V Core (STDVT): PMOS = 86.64yrs @ 1.1V for W/L=10/0.1, 125C  
 $V_{max}$  of PMOS = 1.3 V for W/L=10/0.1, 125C  
2.5V IO: PMOS = 26.72yrs @ 2.75V for W/L=10/0.28, 125C  
 $V_{max}$  of PMOS = 3.0V for W/L=10/0.28, 125C

- b) Criteria: VT shift 50mA:

1.2V Core (STDVT): PMOS = 90.58yrs @ 1.32V for W/L=10/0.1, 125C  
 $V_{max}$  of PMOS = 1.3V for W/L=10/0.1, 125C

## N90GT

- a) Criteria: Idsat shift 10%:

1.2V Core (STDVT): PMOS = 58.94yrs @ 1.32V for W/L=10/0.1, 125C

Vmax of PMOS = 1.5 V for W/L=10/0.1, 125C

2.5V IO: PMOS = 26.47yrs @ 2.75V for W/L=10/0.28, 125C

Vmax of PMOS = 3.0V for W/L=10/0.28, 125C

- b) Criteria: VT shift 50mA:

1.2V Core (STDVT): PMOS = 6.66yrs @ 1.32V for W/L=10/0.1, 125C

Vmax of PMOS = 1.33V for W/L=10/0.1, 125C

## N85LP

- a) Criteria: Idsat shift 10%:

1.2V Core (STDVT): PMOS = 44.57yrs @ 1.32V for W/L=9.4/0.094um, 125C

Vmax of PMOS = 1.5 V for W/L=9.4/0.094um, 125C

2.5V IO: PMOS = 35.99yrs @ 2.75V for W/L=9.4/0.28, 125C

Vmax of PMOS = 3.1V for W/L=9.4/0.28, 125C

3.3V IO: PMOS = 10.83yrs @ 3.63V for W/L=9.4/0.38, 125C

Vmax of PMOS = 3.8V for W/L=9.4/0.38, 125C

## N85G

- a) Criteria: Idsat shift 10%:

1.0V Core (STDVT): PMOS = 52.76yrs @ 1.1V for W/L=9.4/0.094um, 125C

Vmax of PMOS = 1.3 V for W/L=9.4/0.094um, 125C

1.8V IO: PMOS = 6.52yrs @ 1.98V for W/L=9.4/0.28, 125C

Vmax of PMOS = 2.0V for W/L=9.4/0.28, 125C

2.5V IO: PMOS = 36.14yrs @ 2.75V for W/L=9.4/0.28, 125C

Vmax of PMOS = 3.1V for W/L=9.4/0.28, 125C

3.3V IO: PMOS = 9.42yrs @ 3.63V for W/L=9.4/0.38, 125C

Vmax of PMOS = 3.79V for W/L=9.4/0.38, 125C

## N80LP

- a) Criteria: Idsat shift 10%:

1.2V Core (STDVT): PMOS = 24.12yrs @ 1.32V for W/L=9/0.09, 125C

Vmax of PMOS = 1.45 V for W/L=9/0.09, 125C

2.5V IO: PMOS = 42.09yrs @ 2.75V for W/L=9/0.28, 125C

Vmax of PMOS = 3.0V for W/L=9/0.28, 125C

- b) Criteria: VT shift 50mA:

1.2V Core (STDVT): PMOS = 23.42yrs @ 1.32V for W/L=9/0.09, 125C

Vmax of PMOS = 1.45V for W/L=9/0.09, 125C

## N80GC

- a) Criteria: Idsat shift 10%:

1.0V Core (STDVT): PMOS = 89.61yrs @ 1.1V for W/L=9/0.09, 125C

Vmax of PMOS = 1.3 V for W/L=9/0.09, 125C

2.5V IO: PMOS = 35.19yrs @ 2.75V for W/L=9/0.28, 125C

Vmax of PMOS = 3.0V for W/L=9/0.28, 125C

- b) Criteria: VT shift 50mA:

1.0V Core (STDVT): PMOS = 189.25yrs @ 1.1V for W/L=9/0.09, 125C

Vmax of PMOS = 1.3V for W/L=9/0.09, 125C

## N80GT

- a) Criteria: Idsat shift 10%:

1.2V Core (STDVT): PMOS = 31.43yrs @ 1.32V for W/L=9/0.09, 125C

Vmax of PMOS = 1.45 V for W/L=9/0.09, 125C

2.5V IO: PMOS = 42.69yrs @ 2.75V for W/L=9/0.28, 125C

Vmax of PMOS = 3.0V for W/L=9/0.28, 125C

- b) Criteria: VT shift 50mA:

1.2V Core (STDVT): PMOS = 5.61yrs @ 1.32V for W/L=9/0.09, 125C

Vmax of PMOS = 1.32V for W/L=9/0.09, 125C

## 12.3 Back-End Process Reliability Rules

### 12.3.1 Guidelines for Stress Migration(SM)

The Cu vias are frequently subjected to significant stress. The stress frequently causes voids, commonly referred to stress migration (SM) or stress-induced voids (SIV).

#### 12.3.1.1 Failure Mechanism

The stress result from the different coefficient of thermal expansion (CTE) between Cu and the surrounding material will drive micro-vacancy in Cu to diffuse and agglomerate through interfacial surface and grain boundary. Eventually the stressed-induced voids may significantly affect the electrical characteristics and may cause the semiconductor structure to fail.

#### 12.3.1.2 Test Methodology

##### 12.3.1.2.1 Measurement Condition

The measurement is performed under 25°C using wafer-level probing after oven bake. Stress Conditions

1. **Sample size** is >130die(2 wafers) per lot. Totally 3 lots are required.
2. **Temperature range** is 150~200°C.
3. **Stress time** is 500hr.
4. **Test structures** are:
  - i. Vias chain-1 (single via with metal width = min. width under/above via).
  - ii. Vias chain-2 (single via with metal width = max. width allowed for 1 via in SM design rule
  - iii. Vias chain-3 (dual via with metal width = max. width allowed for 2 vias in SM design rule
  - iv. Stacked via chain (single via with metal width = max. width allowed for 1 via in SM design rule

##### 12.3.1.2.2 Failure Criteria

1. The failure criterion is resistance >x% shift in terms of wafer-level test.

x depends on test structure sensitivity and probe condition, generally ranges from 10% to 500%.

2. Specification: No failure allowed within 3 lots.

#### 12.3.1.3 SM design rule

Please refer to below rule codes of chapter4.

VIAx.R.2, VIAx.R.3, VIAx.R.4, VIAx.R.5, VIAx.R.6, VIAx.R.11, VIAy.R.2, VIAy.R.3, VIAy.R.4, VIAy.R.5, VIAy.R.6, VIAx.R.2, VIAx.R.3

## 12.3.2 Guidelines for Low-k Dielectric Integrity

This section provides information to help you predict LK dielectric reliability and prevent a time dependent dielectric breakdown (TDDB). IMD TDDB is the breakdown of LK dielectric induced by a combination of operation voltage, temperature, and oxide thickness.

### 12.3.2.1 Low-k Dielectric Lifetime Prediction Model

$$TTF \text{ (Time to failure)} \propto \exp(-\gamma \times E_d) \times \exp(E_a/KT) \times (L_{ox})^{-1/\beta}$$

Where:

$L_{ox}$  is the total metal length in the same metal layer (unit:  $\mu\text{m}$ )

$T$  is the absolute operation temperature (unit: K)

$E_d$  is the induced electric field applied to LK dielectric (unit: MVolt/cm)

$\gamma$  is the field acceleration factor for LK dielectric

$E_a$  is the thermal activation energy

$k$  is the Boltzmann's constant ( $(8.617 \times 10^{-5}) \text{ eV/K}$ )

$\beta$  is the Weibull shape factor (distribution spread)

### 12.3.2.2 Failure Mechanism

While the current passed through LK dielectric and formed a conduction path, it would result in LK dielectric breakdown.

The possible failure mechanisms after IMD-TDDB test could be as followings.

1. Dielectric interface breakdown (ie: LK dielectric porosity, ESL integration, Cu ions residue...etc.)
2. Dielectric bulk breakdown (ie: trench barrier formation, LK dielectric porosity...etc.)

### 12.3.2.3 Test Methodology

#### 12.3.2.3.1 Measurement Conditions

$I_g$  is the leakage current between metal lines at  $T=125^\circ\text{C}$ .

$E_d$  (constant stress field) is set to  $2 \sim 4 \text{ MV/cm}$  for LK dielectric.

#### 12.3.2.3.2 Stress Conditions

At least 16 samples constitute a sample size for each stress condition:

1. To determine the **field acceleration factor** ( $\gamma$ ), 3 stress voltages are used at each fixed stress temperature.
2. Monitor parameter:  $I_g$  (leakage current) between metal lines.
3. A DUT is considered as failed if  $I_g(T_{bd}) > 100 * I_g(T_0)$ .
4. Specification: 0.1% cumulative DC lifetime at  $1.1V_{cc} > 10 \text{ yrs} @ 125^\circ\text{C}$ .

## 12.3.3 N90 Cu Current Density (EM) Specification

This section provides information to evaluate the quality of 90nm Cu process and to determine the EM specification of metal line, via, stack via, contact under normal operation condition.

### 12.3.3.1 Electromigration Lifetime Prediction Model

$$TTF = A \times J^{-n} \times \exp(Ea/kT)$$

TTF : Time to Failure

A: a constant which contains a factor involving the cross-sectional area of the film

n: exponent of current density ( n =1 )

J: current density flowing in metal

Ea: activation energy ( Ea =0.9eV)

k: Boltzman's constant

T: temperature

### 12.3.3.2 Failure Mechanism

When a stress current is applied, Cu ions move from cathode to anode under electromigration, vacancy will generate at cathode and it will cause resistance increasing.

### 12.3.3.3 Rating factor for Maximum DC Current

$I_{max}$  is the maximum DC current allowed for metal lines, vias, or contacts.  $I_{max}$  is based on 0.1% point of measurement data at a 10% resistance increase after 100K hours of continuous operation at 110°C. Use the following table to calculate  $I_{max}$  if the junction temperature differs from 110°C.

Temperature	105C	110C	125C
Rating factor of $I_{max}$	1.434	1.000	0.358

For example,  $I_{max}$  (at 125°C) = 0.358 ×  $I_{max}$  (at 110°C).

## 12.3.3.4 Maximum DC Current for Metal Lines, contact and Vias ( $T_j = 110^\circ\text{C}$ )

### 12.3.3.4.1 General

The table provides the maximum allowed DC current,  $I_{\max}$  for each of the metals, contact and vias at junction temperature of  $110^\circ\text{C}$  and lifetime of 100,000 hours. In the table,  $w$  (in  $\mu\text{m}$ ) represents the width of the metal line.

Metal Wiring Level / Interlevel connection	Metal Length, L (mm)	$I_{\max}$ (mA)
M1	Any length of metal	$2 \times (w-0.02)$
Mx	Any length of metal	$2.6 \times (w-0.02)$
Mn (3XTM)	Any length of metal	$7.2 \times (w-0.02)$
My (2XTM)	Any length of metal	$4.48 \times (w-0.02)$
UTM	Any length of metal	$27.2 \times (w-0.02)$
Contact (size: $0.12 \times 0.12 \mu\text{m}^2$ )	Any length of metal	0.294 per contact
Vx (size : $0.13 \times 0.13 \mu\text{m}^2$ )	Any length of metal	0.189 per via
Vn (3XTM) (size : $0.36 \times 0.36 \mu\text{m}^2$ )	Any length of metal	1.452 per via
Vy (2XTM) (size : $0.26 \times 0.26 \mu\text{m}^2$ )	Any length of metal	0.757 per via
Vu (UTM) (size : $0.36 \times 0.36 \mu\text{m}^2$ )	Any length of metal	1.452 per via

### 12.3.3.4.2 Dependence of metal length (length<20 $\mu$ m)

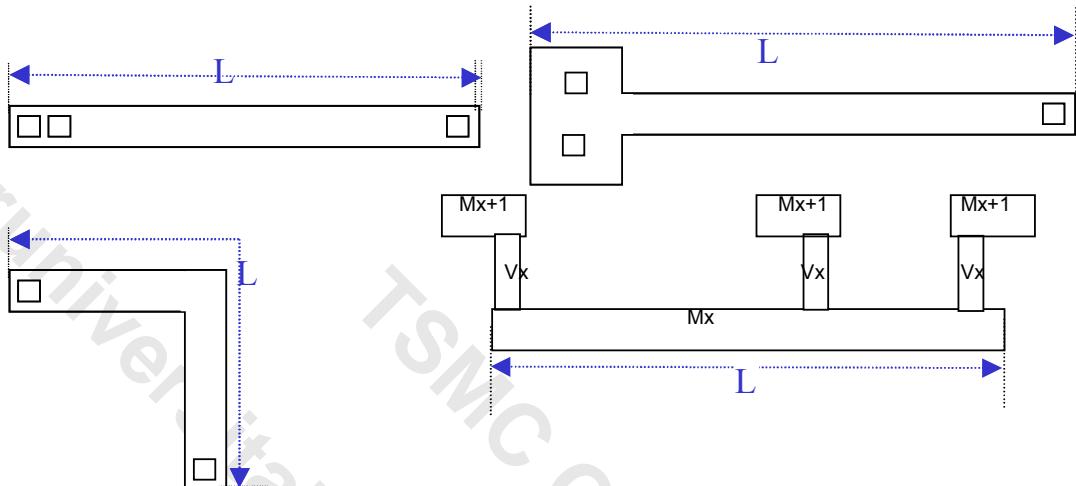
For a metal line length less than 20  $\mu$ m, an enhancement adjustment factor for the DC current limits of the following table must be obeyed. In this table, the junction temperature is 110°C, the lifetime is 100,000 hours, and w (in  $\mu$ m) represents the width of the N90 metal line and L (in  $\mu$ m) represents the metal length of the N90 metal line on silicon.

Metal Wiring Level / Interlevel connection	Metal Length, L (mm)	$I_{max}$ (mA)
M1	$L \geq 20$	$2 \times (w-0.02)$
	$20 > L > 5$	$(20/L) \times 2.0 \times (w-0.02)$
	$L \leq 5$	$4 \times 2.0 \times (w-0.02)$
Mx	$L \geq 20$	$2.6 \times (w-0.02)$
	$20 > L > 5$	$(20/L) \times 2.6 \times (w-0.02)$
	$L \leq 5$	$4 \times 2.6 \times (w-0.02)$
Mn (3XTM)	$L \geq 20$	$7.2 \times (w-0.02)$
	$20 > L > 5$	$(20/L) \times 7.2 \times (w-0.02)$
	$L \leq 5$	$4 \times 7.2 \times (w-0.02)$
My (2XTM)	$L \geq 20$	$4.48 \times (w-0.02)$
	$20 > L > 5$	$(20/L) \times 4.48 \times (w-0.02)$
	$L \leq 5$	$4 \times 4.48 \times (w-0.02)$
UTM	$L \geq 20$	$27.2 \times (w-0.02)$
	$20 > L > 5$	$(20/L) \times 27.2 \times (w-0.02)$
	$L \leq 5$	$4 \times 27.2 \times (w-0.02)$
Vx (size : 0.13 x 0.13 $\mu$ m <sup>2</sup> )	$L \geq 20$	0.189 per via
	$20 > L > 5$	$(20/L) \times 0.189$ per via
	$L \leq 5$	$4 \times 0.189$ per via
Vn (3XTM) (size : 0.36 x 0.36 $\mu$ m <sup>2</sup> )	$L \geq 20$	1.452 per via
	$20 > L > 5$	$(20/L) \times 1.452$ per via
	$L \leq 5$	$4 \times 1.452$ per via
Vy (2XTM) (size : 0.26 x 0.26 $\mu$ m <sup>2</sup> )	$L \geq 20$	0.757 per via
	$20 > L > 5$	$(20/L) \times 0.757$ per via
	$L \leq 5$	$4 \times 0.757$ per via
Vu (UTM) (size : 0.36x 0.36 $\mu$ m <sup>2</sup> )	$L \geq 20$	1.452 per via
	$20 > L > 5$	$(20/L) \times 1.452$ per via
	$L \leq 5$	$4 \times 1.452$ per via

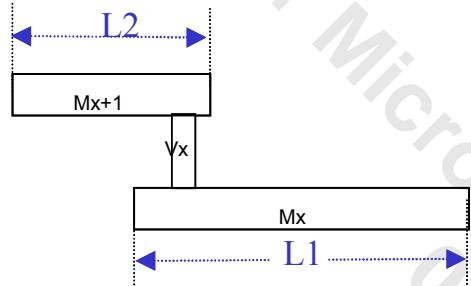
Note :  $I_{max}$  for short length rule and  $I_{max}$  of via array/CO array rule can't collateral at the same time

## (1) Metal Length Definition (L):

The total length of metal wiring level is from one line-end site to another site line-end site of metal.



## (2) The higher of the upper\_metal and lower\_metal Length is used for Via length rule.



If L1 is larger than L2,  $I_{max}$  of via for short length is based on L1.

If L2 is larger than L1,  $I_{max}$  of via for short length is based on L2.

For example : Via1 connect to 10um-length M1 and 5um-length M2.

$$I_{max} \text{ of M1} = (20/10) \times 2.0 \times (w-0.02)$$

$$I_{max} \text{ of M2} = 4 \times 2.6 \times (w-0.02)$$

$$I_{max} \text{ of Via1} = (20/10) \times 0.189$$

### 12.3.3.5 DC Current Specifications for Stacked Vias

The table provides the maximum allowed DC current,  $I_{max}$ , for stacked vias at junction temperature of 110°C.

Interlevel Connection	$I_{max}$ (mA)	
Vxx	0.189	per stack
Vxy	0.189	per stack
Vxn	0.189	per stack
Vxu	0.189	per stack
Vxyn	0.189	per stack
Vxnu	0.189	per stack
Vyy	0.757	per stack
Vyn	0.757	per stack
Vnn	1.452	per stack
Vnu	1.452	per stack

## 12.3.3.6 Dependence of Via array/ Contact array on DC current (T<sub>j</sub> = 110°C)

For Via or Contact number exceeding 2 (including 2; Via array or Contact array structure), an adjustment factor for the line, Via and Contact DC current limits of the following table must be obeyed. In this table, the junction temperature is 110°C.

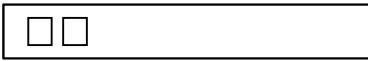
Interlevel connection	Numbers of via	I <sub>max</sub> (mA)	
M1	Single via	2	$\times (w-0.02)$
	Via array	$2 \times 2$	$\times (w-0.02)$
Mx	Single via	2.6	$\times (w-0.02)$
	Via array	$2 \times 2.6$	$\times (w-0.02)$
My (2XTM)	Single via	4.48	$\times (w-0.02)$
	Via array	$2 \times 4.48$	$\times (w-0.02)$
Mn (3XTM)	Single via	7.2	$\times (w-0.02)$
	Via array	$2 \times 7.2$	$\times (w-0.02)$
Mu (UTM)	Single contact	27.2	$\times (w-0.02)$
	Via array	$2 \times 27.2$	$\times (w-0.02)$
Contact (Size 0.12 x 0.12 um)	Single contact	0.294	per contact
	Contact array	$2 \times 0.294$	per contact
V1 (size : 0.13 x 0.13 μm <sup>2</sup> )	Single via	0.189	per via
	Via array	$2 \times 0.189$	per via
Vx (size : 0.13 x 0.13 μm <sup>2</sup> )	Single via	0.189	per via
	Via array	$2 \times 0.189$	per via
Vy (2XTM) (size : 0.26 x 0.26 μm <sup>2</sup> )	Single via	0.757	per via
	Via array	$2 \times 0.757$	per via
Vn (3XTM) (size : 0.36 x 0.36 μm <sup>2</sup> )	Single via	1.452	per via
	Via array	$2 \times 1.452$	per via
Vu (UTM) (size : 0.36 x 0.36 μm <sup>2</sup> )	Single via	1.452	per via
	Via array	$2 \times 1.452$	per via

Note: I<sub>max</sub> for short length rule and I<sub>max</sub> of via arrar/ Contact array rule can't collateral at the same time.

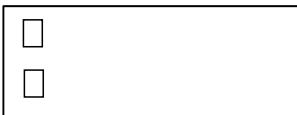
Note : I<sub>max</sub> for short length rule and I<sub>max</sub> of via array/Contact array rule can't collateral at the same time.

- (1) In this table, via array/ contact array is defined as via number/contact number larger than 2 (including 2), including parallel and perpendicular to the direction of current flow via structure.
- (2) For the use of via array/ contact array structure, the allowable current values equal to the allowable current per via/ contact (the above table) times the number of vias/ contacts.

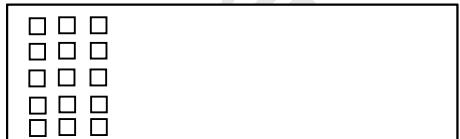
(A)



(B)



(C)



If via size is 0.13umx0.13um, total I<sub>max</sub> of vias

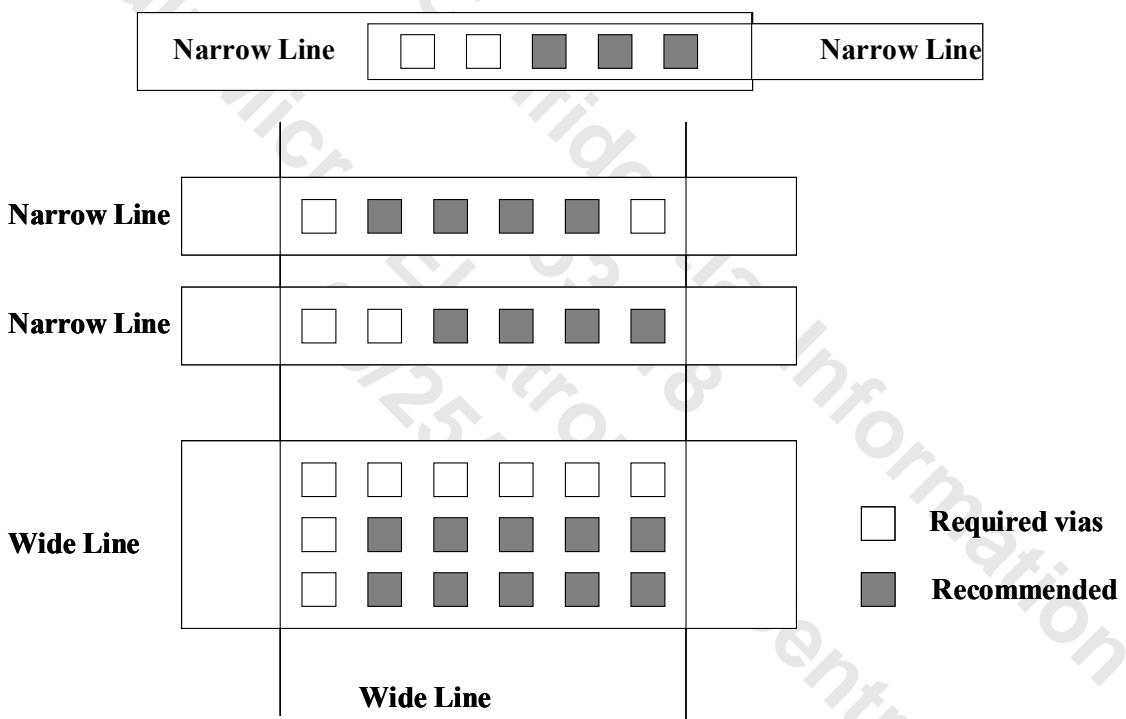
Type A: Total I<sub>max</sub> of 2 vias =  $2 \times 0.189 \times 2 = 0.756$  mA

Type B: Total I<sub>max</sub> of 2 vias =  $2 \times 0.189 \times 2 = 0.756$  mA

Type C: Toal I<sub>max</sub> of 15 vias =  $2 \times 0.189 \times 15 = 5.67$  mA

## 12.3.3.7 DC Operation, Required Number of Vias

1. If space permits, it is preferable to have more contacts or vias than the EM rules require.
2. At a minimum rule, the EM current rules require one via.
  - a. Example 1, if M1 is 0.12  $\mu\text{m}$  and the current density is 2 mA/ $\mu\text{m}$ ; that is, the current is  $2*(0.12-0.02) = 0.2 \text{ mA}$ , only one VIA1 is necessary to ensure the reliability margin.
  - b. Example 2, if M2 is 0.14  $\mu\text{m}$  and the current density is 2.6 mA/ $\mu\text{m}$ ; that is, the current is  $2.6*(0.14-0.02) = 0.312 \text{ mA}$ , only one VIA1 and one VIA2 are necessary to ensure the reliability margin.
3. To determine the required number of vias, please proceed as follow:
  - a. From the DC current given in 12.3.3.4, determine the necessary line width (W-line)
  - b. Calculate the Maximum allowed  $I_{dc\_line}$  for the given line width (W-line).
  - c. Calculate the required number of contacts or vias to carry line current  $I_{dc\_line}$  : Number of vias =  $I_{dc\_line} / I_{dc\_via}$ .
4. Recommended Rule : The number of contacts and vias placed across a line (perpendicular to direction of current flow) must be maximized to increase reliability by providing redundancy in the case of blocked or resistive vias. ( increases as much as the line width permits).



## 12.3.4 N85 DC Current Density (EM) Specifications

This section provides information to evaluate the quality of N85 Cu process and to determine the EM lifetime of metal line, via, stack via, contact under normal operation condition.

### 12.3.4.1 Maximum DC Current

$I_{max}$  is the maximum DC current allowed for metal lines, vias, or contacts.  $I_{max}$  is based on 0.1% point of measurement data at a 110% resistance increased after 100K hours of continuous operation at 110°C. Use the following table to calculate  $I_{max}$  if the junction temperature differs from 110°C.

Temperature	105C	110C	115C	120C	125C
Rating factor of $I_{max}$	1.434	1.000	0.704	0.500	0.358

For example,  $I_{max}$  (at 125°C) =  $0.358 \times I_{max}$  (at 110°C)

### 12.3.4.2 Maximum DC Current for Metal Lines, Contacts and Vias ( $T_j = 110^\circ\text{C}$ )

#### 12.3.4.2.1 General

The table provides the maximum allowed DC current,  $I_{max}$  for each of the metal, contacts and vias at junction temperature of 110°C. *In the tables, w (in  $\mu\text{m}$ ) represents the width of the N85 drawn metal line.*

Metal Wiring Level / Interlevel connection	Metal Length, L ( $\mu\text{m}$ )	$I_{max}$ (mA)
M1	Any length of metal	$2.155 \times (w \times 0.94 - 0.02)$
Mx	Any length of metal	$2.796 \times (w \times 0.94 - 0.02)$
Mn (3XTM)	Any length of metal	$7.684 \times (w \times 0.94 - 0.02)$
My (2XTM)	Any length of metal	$4.789 \times (w \times 0.94 - 0.02)$
UTM	Any length of metal	$28.936 \times (w \times 0.94 - 0.02)$
Contact (size: $0.113 \times 0.113 \mu\text{m}^2$ )	Any length of metal	0.294 per contact
Vx (size : $0.122 \times 0.122 \mu\text{m}^2$ )	Any length of metal	0.189 per via
Vn (3XTM) (size : $0.338 \times 0.338 \mu\text{m}^2$ )	Any length of metal	1.452 per via
Vy (2XTM) (size : $0.244 \times 0.244 \mu\text{m}^2$ )	Any length of metal	0.757 per via
Vu (UTM) (size : $0.338 \times 0.338 \mu\text{m}^2$ )	Any length of metal	1.452 per via

### 12.3.4.2.2 Dependence of metal length (length<20μm)

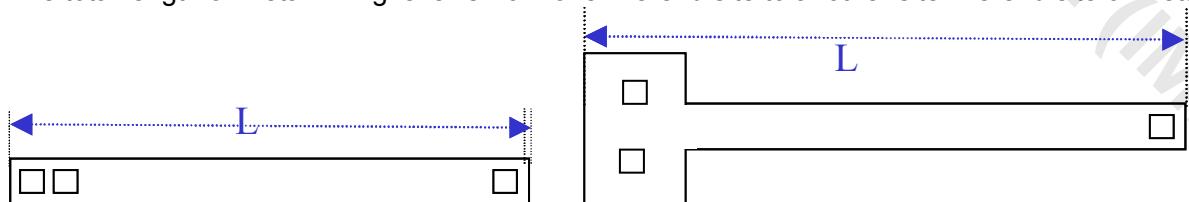
For a metal line length less than 20 μm, an enhancement adjustment factor for the DC current limits of the following table must be obeyed. In this table, the junction temperature is 110°C, and w (in μm) represents the width of the N85 drawn metal line and L (in μm) represents the metal length of the N85 drawn metal line.

Metal Wiring Level / Interlevel connection	Metal Length, L (μm)	$I_{max}$ (mA)
M1	$L \geq 20$	$2.155 \times (wx0.94-0.02)$
	$20 > L > 5$	$(20/L) \times 2.155 \times (wx0.94-0.02)$
	$L \leq 5$	$4 \times 2.155 \times (wx0.94-0.02)$
Mx	$L \geq 20$	$2.796 \times (wx0.94-0.02)$
	$20 > L > 5$	$(20/L) \times 2.796 \times (wx0.94-0.02)$
	$L \leq 5$	$4 \times 2.796 \times (wx0.94-0.02)$
Mn (3XTM)	$L \geq 20$	$7.684 \times (wx0.94-0.02)$
	$20 > L > 5$	$(20/L) \times 7.684 \times (wx0.94-0.02)$
	$L \leq 5$	$4 \times 7.684 \times (wx0.94-0.02)$
My (2XTM)	$L \geq 20$	$4.789 \times (wx0.94-0.02)$
	$20 > L > 5$	$(20/L) \times 4.789 \times (wx0.94-0.02)$
	$L \leq 5$	$4 \times 4.789 \times (wx0.94-0.02)$
UTM	$L \geq 20$	$28.936 \times (wx0.94-0.02)$
	$20 > L > 5$	$(20/L) \times 28.936 \times (wx0.94-0.02)$
	$L \leq 5$	$4 \times 28.936 \times (wx0.94-0.02)$
Vx (size : $0.122 \times 0.122 \mu\text{m}^2$ )	$L \geq 20$	0.189 per via
	$20 > L > 5$	$(20/L) \times 0.189$ per via
	$L \leq 5$	$4 \times 0.189$ per via
Vn (3XTM) (size : $0.338 \times 0.338 \mu\text{m}^2$ )	$L \geq 20$	1.452 per via
	$20 > L > 5$	$(20/L) \times 1.452$ per via
	$L \leq 5$	$4 \times 1.452$ per via
Vu (UTM) (size : $0.338 \times 0.338 \mu\text{m}^2$ )	$L \geq 20$	1.452 per via
	$20 > L > 5$	$(20/L) \times 1.452$ per via
	$L \leq 5$	$4 \times 1.452$ per via
Vy (2XTM) (size : $0.244 \times 0.244 \mu\text{m}^2$ )	$L \geq 20$	0.757 per via
	$20 > L > 5$	$(20/L) \times 0.757$ per via
	$L \leq 5$	$4 \times 0.757$ per via

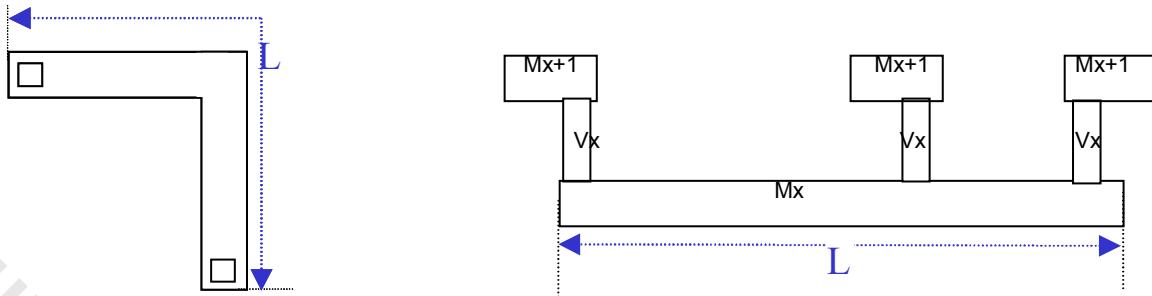
Note :  $I_{max}$  of via for short length and  $I_{max}$  of via in via array can't collateral at the same time.

#### 1. Metal Length Definition (L):

The total length of metal wiring level is from one line-end site to another site line-end site of metal.

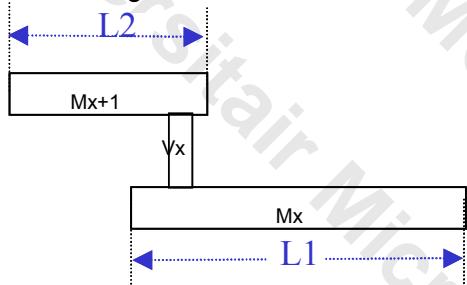


2. The higher of the upper\_metal and lower\_metal Length is used for Via length rule.



If L1 is larger than L2,  $I_{max}$  of via for short length is based on L1.

If L2 is larger than L1,  $I_{max}$  of via for short length is based on L2.



For example : Via1 connect to 10um-length M1 and 5um-length M2.

$$I_{max} \text{ of M1} = (20/10) \times 2.155 \times (wx0.94-0.02)$$

$$I_{max} \text{ of M2} = 4 \times 2.796 \times (wx0.94-0.02)$$

$$I_{max} \text{ of Via1} = (20/10) \times 0.189$$

#### 12.3.4.2.3 DC Current Specifications for Stacked Vias

The table provides the maximum allowed DC current,  $I_{max}$ , for stacked vias at the junction temperature of 110°C.

Interlevel Connection	$I_{max}$ (mA)	
Vxx	0.189	per stack
Vxy	0.189	per stack
Vxn	0.189	per stack
Vxu	0.189	per stack
Vxyn	0.189	per stack
Vxnu	0.189	per stack
Vyy	0.757	per stack
Vyn	0.757	per stack
Vnu	1.452	per stack
Vnn	1.452	per stack

### 12.3.4.3 Dependence of Via array on DC current ( $T_j = 110^\circ\text{C}$ )

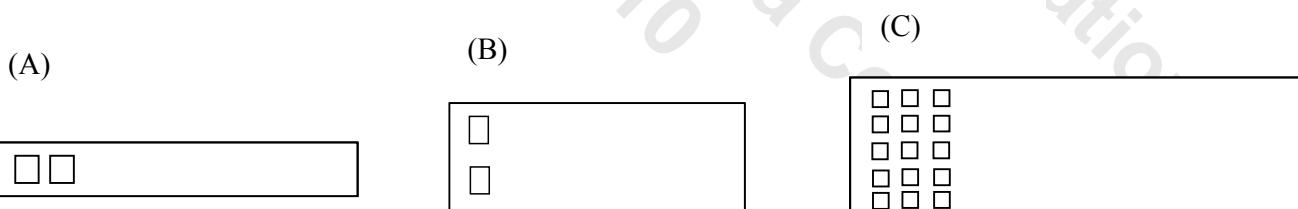
For Via number exceeding 2 (including 2; Via array structure), an adjustment factor for the Via DC current limits of the following table must be obeyed. In this table, the junction temperature is  $110^\circ\text{C}$ .

Interlevel connection	Numbers of via	$I_{\max}$ (mA)	
M1	Single via	2.155	$\times (wx0.94-0.02)$
	Via array	$2 \times 2.155$	$\times (wx0.94-0.02)$
Mx	Single via	2.796	$\times (wx0.94-0.02)$
	Via array	$2 \times 2.796$	$\times (wx0.94-0.02)$
My (2XTM)	Single via	4.789	$\times (wx0.94-0.02)$
	Via array	$2 \times 4.789$	$\times (wx0.94-0.02)$
Mn (3XTM)	Single via	7.684	$\times (wx0.94-0.02)$
	Via array	$2 \times 7.684$	$\times (wx0.94-0.02)$
Mu (UTM)	Single contact	28.936	$\times (wx0.94-0.02)$
	Via array	$2 \times 28.936$	$\times (wx0.94-0.02)$
Contact (Size $0.113 \times 0.113 \mu\text{m}^2$ )	Single contact	0.294	per contact
	Contact array	$2 \times 0.294$	per contact
Vx (size : $0.122 \times 0.122 \mu\text{m}^2$ )	Single via	0.189	per via
	Via array	$2 \times 0.189$	per via
Vy (2XTM) (size : $0.244 \times 0.244 \mu\text{m}^2$ )	Single via	0.757	per via
	Via array	$2 \times 0.757$	per via
Vu (UTM) (size : $0.338 \times 0.338 \mu\text{m}^2$ )	Single via	1.452	per via
	Via array	$2 \times 1.452$	per via
Vn (3XTM) (size : $0.338 \times 0.338 \mu\text{m}^2$ )	Single via	1.452	per via
	Via array	$2 \times 1.452$	per via

Note :  $I_{\max}$  of via for short length and  $I_{\max}$  of via in via array can't collateral at the same time.

(1)In this table, via array is defined as via number larger than 2 (including 2), including parallel and perpendicular to the direction of current flow via structure.

(2)For the use of Via array structure, the allowable current values equal to the allowable current per via (the above table) times the number of vias.



If via size is  $0.122\text{um} \times 0.122\text{um}$ ,  $I_{\max}$  of via

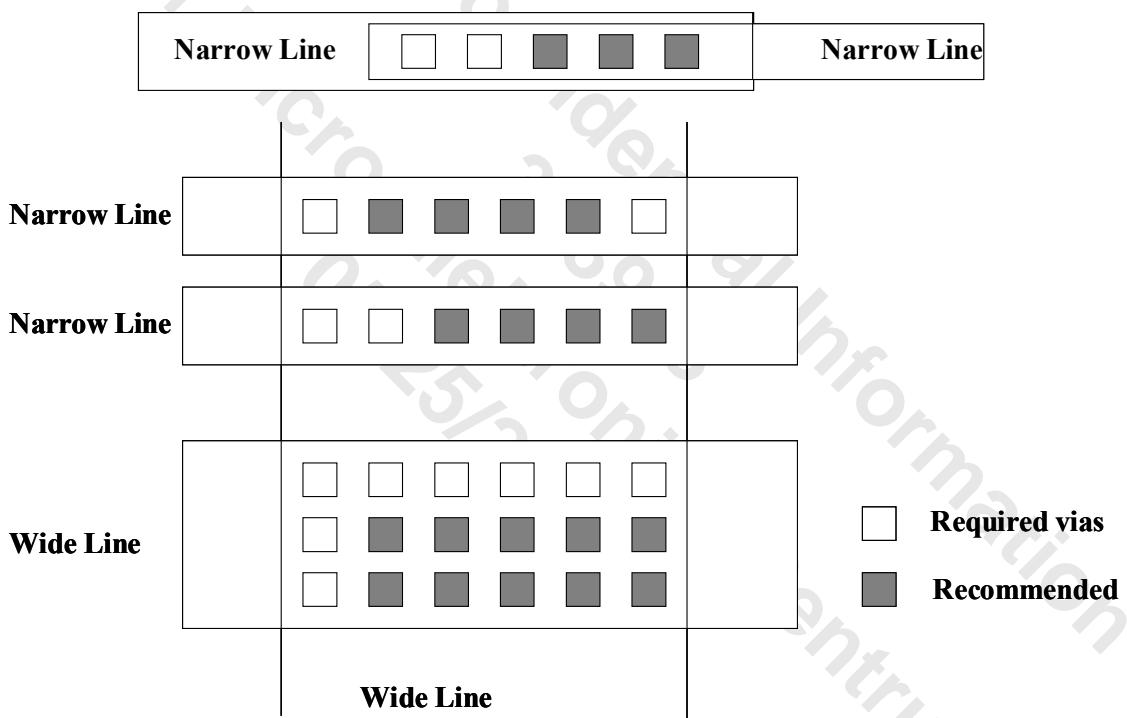
Type A :  $I_{\max}$  of via =  $2 \times 0.189 \times 2 = 0.756 \text{ mA}$

Type B :  $I_{\max}$  of via =  $2 \times 0.189 \times 2 = 0.756 \text{ mA}$

Type C :  $I_{\max}$  of via =  $2 \times 0.189 \times 15 = 5.67 \text{ mA}$

## 12.3.4.4 DC Operation, Required Number of Vias

1. If space permits, it is preferable to have more contacts or vias than the EM rules require.
2. At a minimum rule, the EM current rules require one via.
  - a. Example 1, if M1 is 0.12 µm and the current density is 2.155 mA/µm; that is, the current is  $2.155 * (0.12 \times 0.94 - 0.02) = 0.2$  mA, two VIA1 are necessary to ensure the reliability margin.
  - b. Example 2, if M2 is 0.14µm and the current density is 2.796 mA/µm; that is, the current is  $2.796 * (0.14 \times 0.94 - 0.02) = 0.312$  mA, only two VIA1 and two VIA2 are necessary to ensure the reliability margin.
3. To determine the required number of vias, please proceed as follow:
  - a. From the DC current given in 12.3.4.2, determine the necessary line width (W-line)
  - b. Calculate the Maximum allowed  $I_{dc\_line}$  for the given line width (W-line).
  - c. Calculate the required number of contacts or vias to carry line current  $I_{dc\_line}$  : Number of vias =  $I_{dc\_line} / I_{dc\_via}$ .
4. Recommended Rule : The number of contacts and vias placed across a line (perpendicular to direction of current flow) must be maximized to increase reliability by providing redundancy in the case of blocked or resistive vias. (increases as much as the line width permits).



## 12.3.5 N80 DC Current Density (EM) Specifications

This section provides information to evaluate the quality of N80 Cu process and to determine the EM lifetime of metal line, via, stack via, contact under normal operation condition.

### 12.3.5.1 Maximum DC Current

$I_{max}$  is the maximum DC current allowed for metal lines, vias, or contacts.  $I_{max}$  is based on 0.1% point of measurement data at a 110% resistance increased after 100K hours of continuous operation at 110°C. Use the following table to calculate  $I_{max}$  if the junction temperature differs from 110°C.

Temperature	105C	110C	115C	120C	125C
Rating factor of $I_{max}$	1.434	1.000	0.704	0.500	0.358

For example,  $I_{max}$  (at 125°C) =  $0.358 \times I_{max}$  (at 110°C)

### 12.3.5.2 Maximum DC Current for Metal Lines, Contacts and Vias ( $T_j = 110^\circ\text{C}$ )

#### 12.3.5.2.1 General

The table provides the maximum allowed DC current,  $I_{max}$  for each of the metal, contacts and vias at junction temperature of 110°C. *In the tables, w (in  $\mu\text{m}$ ) represents the width of the N80 drawn metal line.*

Metal Wiring Level / Interlevel connection	Metal Length, L ( $\mu\text{m}$ )	$I_{max}$ (mA)
M1	Any length of metal	$2.273 \times (w \times 0.9 - 0.02)$
Mx	Any length of metal	$2.943 \times (w \times 0.9 - 0.02)$
Mn (3XTM)	Any length of metal	$8.045 \times (w \times 0.9 - 0.02)$
My (2XTM)	Any length of metal	$5.021 \times (w \times 0.9 - 0.02)$
Contact (size: $0.108 \times 0.108 \mu\text{m}^2$ )	Any length of metal	0.294 per contact
Vx (size : $0.117 \times 0.117 \mu\text{m}^2$ )	Any length of metal	0.189 per via
Vn (3XTM) (size : $0.324 \times 0.324 \mu\text{m}^2$ )	Any length of metal	1.452 per via
Vy (2XTM) (size : $0.234 \times 0.234 \mu\text{m}^2$ )	Any length of metal	0.757 per via

### 12.3.5.2.2 Dependence of metal length (length<20μm)

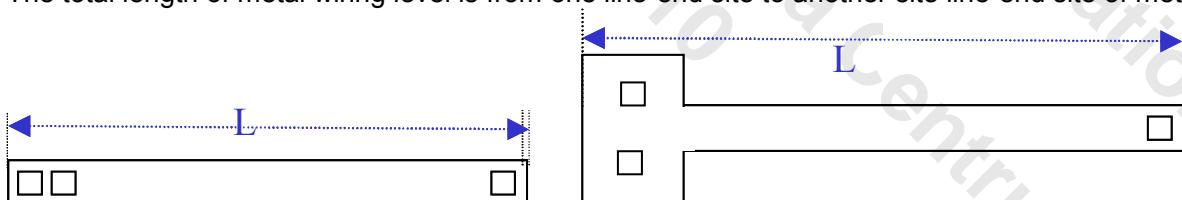
For a metal line length less than 20 μm, an enhancement adjustment factor for the DC current limits of the following table must be obeyed. In this table, the junction temperature is 110°C, and w (in μm) represents the width of the N80 drawn metal line and L (in μm) represents the metal length of the N80 drawn metal line.

Metal Wiring Level / Interlevel connection	Metal Length, L (μm)	$I_{max}$ (mA)
M1	$L \geq 20$	$2.273 \times (wx0.9-0.02)$
	$20 > L > 5$	$(20/L) \times 2.273 \times (wx0.9-0.02)$
	$L \leq 5$	$4 \times 2.273 \times (wx0.9-0.02)$
Mx	$L \geq 20$	$2.943 \times (wx0.9-0.02)$
	$20 > L > 5$	$(20/L) \times 2.943 \times (wx0.9-0.02)$
	$L \leq 5$	$4 \times 2.943 \times (wx0.9-0.02)$
Mn (3XTM)	$L \geq 20$	$8.045 \times (wx0.9-0.02)$
	$20 > L > 5$	$(20/L) \times 8.045 \times (wx0.9-0.02)$
	$L \leq 5$	$4 \times 8.045 \times (wx0.9-0.02)$
My (2XTM)	$L \geq 20$	$5.021 \times (wx0.9-0.02)$
	$20 > L > 5$	$(20/L) \times 5.021 \times (wx0.9-0.02)$
	$L \leq 5$	$4 \times 5.021 \times (wx0.9-0.02)$
Vx (size : $0.117 \times 0.117 \mu\text{m}^2$ )	$L \geq 20$	0.189 per via
	$20 > L > 5$	$(20/L) \times 0.189$ per via
	$L \leq 5$	$4 \times 0.189$ per via
Vn (3XTM) (size : $0.324 \times 0.324 \mu\text{m}^2$ )	$L \geq 20$	1.452 per via
	$20 > L > 5$	$(20/L) \times 1.452$ per via
	$L \leq 5$	$4 \times 1.452$ per via
Vy (2XTM) (size : $0.234 \times 0.234 \mu\text{m}^2$ )	$L \geq 20$	0.757 per via
	$20 > L > 5$	$(20/L) \times 0.757$ per via
	$L \leq 5$	$4 \times 0.757$ per via

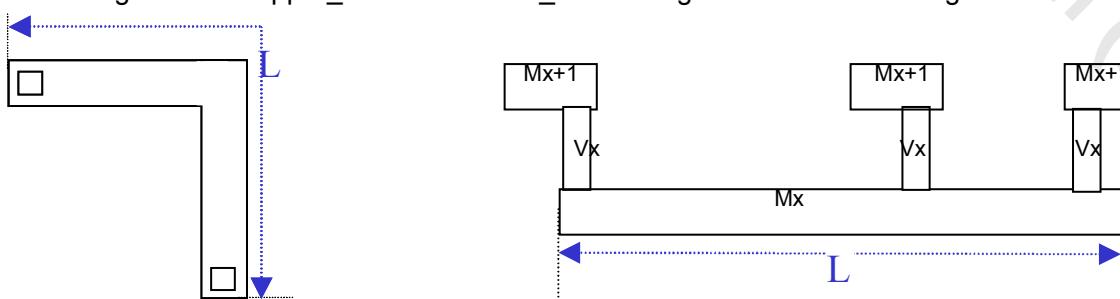
Note :  $I_{max}$  of via for short length and  $I_{max}$  of via in via array can't collateral at the same time.

#### 1. Metal Length Definition (L):

The total length of metal wiring level is from one line-end site to another site line-end site of metal.

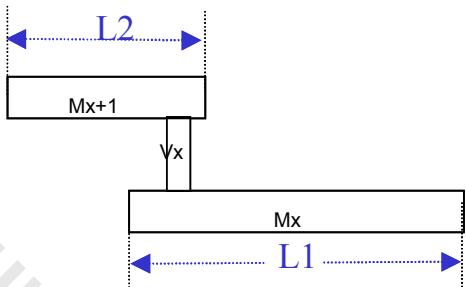


#### 2. The higher of the upper\_metal and lower\_metal Length is used for Via length rule.



If L1 is larger than L2,  $I_{max}$  of via for short length is based on L1.

If L2 is larger than L1,  $I_{max}$  of via for short length is based on L2.



For example : Via1 connect to 10um-length M1 and 5um-length M2.

$$I_{max} \text{ of M1} = (20/10) \times 2.273 \times (wx0.9-0.02)$$

$$I_{max} \text{ of M2} = 4 \times 2.943 \times (wx0.9-0.02)$$

$$I_{max} \text{ of Via1} = (20/10) \times 0.189$$

### 12.3.5.2.3 DC Current Specifications for Stacked Vias

The table provides the maximum allowed DC current,  $I_{max}$ , for stacked vias at the junction temperature of 110°C.

Interlevel Connection	$I_{max}$ (mA)	
V <sub>xx</sub>	0.189	per stack
V <sub>xy</sub>	0.189	per stack
V <sub>xn</sub>	0.189	per stack
V <sub>xyn</sub>	0.189	per stack
V <sub>yy</sub>	0.757	per stack
V <sub>yn</sub>	0.757	per stack
V <sub>nn</sub>	1.452	per stack

### 12.3.5.3 Dependence of Via array on DC current ( $T_j = 110^\circ\text{C}$ )

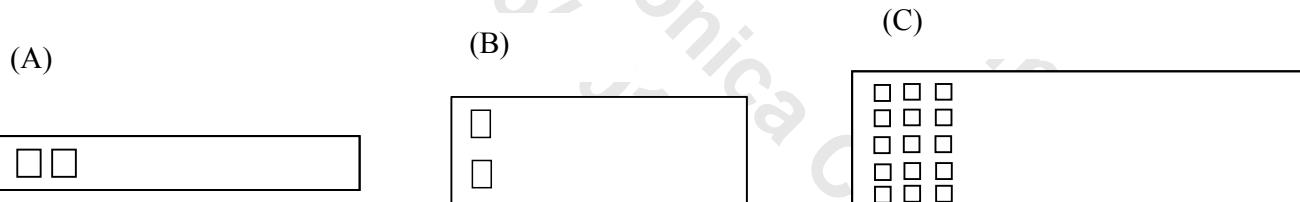
For Via number exceeding 2 (including 2; Via array structure), an adjustment factor for the Via DC current limits of the following table must be obeyed. In this table, the junction temperature is  $110^\circ\text{C}$ .  $w$  (in  $\mu\text{m}$ ) represents the width of the N80 drawn metal line.

Interlevel connection	Numbers of via	$I_{\max}$ (mA)
M1	Single via	2.273 $\times (wx0.9-0.02)$
	Via array	$2 \times 2.273 \times (wx0.9-0.02)$
Mx	Single via	2.943 $\times (wx0.9-0.02)$
	Via array	$2 \times 2.943 \times (wx0.9-0.02)$
My (2XTM)	Single via	5.021 $\times (wx0.9-0.02)$
	Via array	$2 \times 5.021 \times (wx0.9-0.02)$
Mn (3XTM)	Single via	8.045 $\times (wx0.9-0.02)$
	Via array	$2 \times 8.045 \times (wx0.9-0.02)$
Contact (Size 0.108 x 0.108 $\mu\text{m}$ )	Single contact	0.294 per contact
	Contact array	$2 \times 0.294$ per contact
Vx (size : $0.117 \times 0.117 \mu\text{m}^2$ )	Single via	0.189 per via
	Via array	$2 \times 0.189$ per via
Vy (2XTM) (size : $0.234 \times 0.234 \mu\text{m}^2$ )	Single via	0.757 per via
	Via array	$2 \times 0.757$ per via
Vn (3XTM) (size : $0.324 \times 0.324 \mu\text{m}^2$ )	Single via	1.452 per via
	Via array	$2 \times 1.452$ per via

Note :  $I_{\max}$  of via for short length and  $I_{\max}$  of via in via array can't collateral at the same time.

(1) In this table, via array is defined as via number larger than 2 (including 2), including parallel and perpendicular to the direction of current flow via structure.

(2) For the use of Via array structure, the allowable current values equal to the allowable current per via (the above table) times the number of vias.



If via size is  $0.117\mu\text{m} \times 0.117\mu\text{m}$ ,  $I_{\max}$  of via

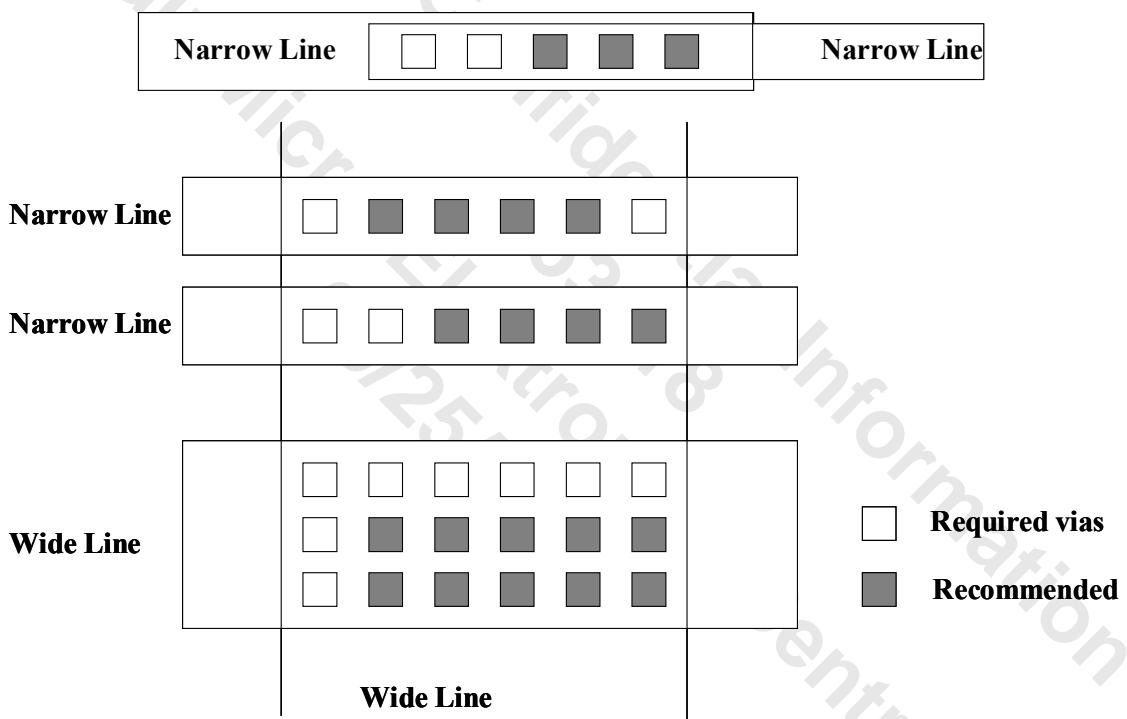
Type A :  $I_{\max}$  of via =  $2 \times 0.189 \times 2 = 0.756 \text{ mA}$

Type B :  $I_{\max}$  of via =  $2 \times 0.189 \times 2 = 0.756 \text{ mA}$

Type C :  $I_{\max}$  of via =  $2 \times 0.189 \times 15 = 5.67 \text{ mA}$

## 12.3.5.4 DC Operation, Required Number of Vias

1. If space permits, it is preferable to have more contacts or vias than the EM rules require.
2. At a minimum rule, the EM current rules require one via.
  - a. Example 1, if M1 is 0.108 µm and the current density is 2.273 mA/µm; that is, the current is  $2.273 \times (0.108 - 0.02) = 0.182$  mA, only one VIA1 is necessary to ensure the reliability margin.
  - b. Example 2, if M2 is 0.126 µm and the current density is 2.943 mA/µm; that is, the current is  $2.943 \times (0.126 - 0.02) = 0.312$  mA, only two VIA1 and two VIA2 are necessary to ensure the reliability margin.
3. To determine the required number of vias, please proceed as follow:
  - a. From the DC current given in 12.3.5.2, determine the necessary line width (W-line)
  - b. Calculate the Maximum allowed  $I_{dc\_line}$  for the given line width (W-line).
  - c. Calculate the required number of contacts or vias to carry line current  $I_{dc\_line}$  : Number of vias =  $I_{dc\_line} / I_{dc\_via}$ .
4. Recommended Rule : The number of contacts and vias placed across a line (perpendicular to direction of current flow) must be maximized to increase reliability by providing redundancy in the case of blocked or resistive vias. (increases as much as the line width permits).



## 12.3.6 N90/N85/N80 Cu Metal AC Operation

The AC operations of N85/N80 can be directly shrunk from N90.

### 12.3.6.1 Pulsed Signal Terminology

The general terminology for a pulsed DC or AC signal is:

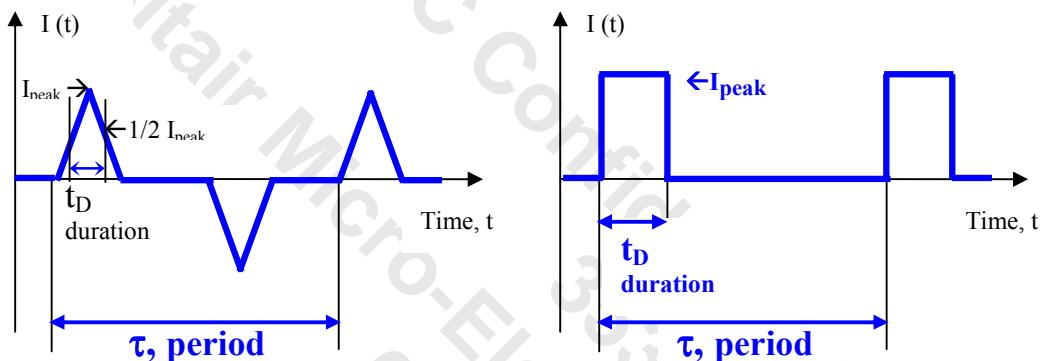
Period ( $\tau$ )

Duration ( $t_D$ )

For your convenience, you could measure the pulse width of  $I_{peak}$  at half the peak to define the duration ( $t_D$ ).

The definition of  $I_{peak}$  is:

$$I_{peak} = \max(|I(t)|)$$



### 12.3.6.2 Average Value of the Current

$I_{avg}$  is the average value of the current, which is the effective DC current. Therefore,  $I_{avg}$  rules are identical to  $I_{max}$  rules. Please refer to the DC EM sections. The temperature de-rating table is also applicable to the  $I_{avg}$  rule for a junction temperature different from 110°C.

The definition of  $I_{avg}$  is:

$$I_{avg} = \left[ \left( \int_0^{\tau} I(t) dt \right) / \tau \right]$$

### 12.3.6.3 Root-Mean-Square Current

$I_{rms}$  is the root-mean-square of the current through a metal line. The definition of  $I_{rms}$  is:

$$I_{rms} = \left[ \left( \int_0^{\tau} I(t)^2 dt \right) / \tau \right]^{1/2}$$

The following tables provide the maximum  $I_{rms}$  allowed for each of the metal wiring levels at a junction temperature of 110°C. In the table,  $w$  (in  $\mu\text{m}$ ) represents the width of the metal line and  $\Delta T$  ( $^{\circ}\text{C}$ ) is the temperature rise due to Joule heating.

#### 12.3.6.3.1 AC Operation, Maximum Root-Mean-Square Current for LK Dielectrics (1P9M process)

Metal level	$I_{rms}$ (mA)
M1	Sqrt [ 18.51 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 0.484) ]$
M2 (Mx1)	Sqrt [ 5.936 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 0.654) ]$
M3 (Mx2)	Sqrt [ 3.110 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 1.248) ]$
M4 (Mx3)	Sqrt [ 2.108 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 1.842) ]$
M5 (Mx4)	Sqrt [ 1.594 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 2.436) ]$
M6 (Mx5)	Sqrt [ 1.282 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 3.030) ]$
M7 (Mx6)	Sqrt [ 1.072 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 3.624) ]$
M8 (Mn1)	Sqrt [ 2.584 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 4.159) ]$
M9 (Mn2)	Sqrt [ 2.306 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 4.664) ]$
M8 (My1)	Sqrt [ 1.634 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 4.095) ]$
M9 (My2)	Sqrt [ 1.508 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 4.435) ]$
M9 (UTM)	Sqrt [ 7.854 $\times \Delta T \times (w - 0.02) \times ((w - 0.02) + 5.025) ]$

#### Example Root-Mean-Square Current for $\Delta T = 5^{\circ}\text{C}$

Metal level	$I_{rms}$ (mA)
M1	Sqrt [ 92.55 $\times (w - 0.02) \times ((w - 0.02) + 0.484) ]$
M2 (Mx1)	Sqrt [ 29.68 $\times (w - 0.02) \times ((w - 0.02) + 0.654) ]$
M3 (Mx2)	Sqrt [ 15.55 $\times (w - 0.02) \times ((w - 0.02) + 1.248) ]$
M4 (Mx3)	Sqrt [ 10.54 $\times (w - 0.02) \times ((w - 0.02) + 1.842) ]$
M5 (Mx4)	Sqrt [ 7.97 $\times (w - 0.02) \times ((w - 0.02) + 2.436) ]$
M6 (Mx5)	Sqrt [ 6.41 $\times (w - 0.02) \times ((w - 0.02) + 3.030) ]$
M7 (Mx6)	Sqrt [ 5.36 $\times (w - 0.02) \times ((w - 0.02) + 3.624) ]$
M8 (Mn1)	Sqrt [ 12.92 $\times (w - 0.02) \times ((w - 0.02) + 4.159) ]$
M9 (Mn2)	Sqrt [ 11.53 $\times (w - 0.02) \times ((w - 0.02) + 4.664) ]$
M8 (My1)	Sqrt [ 8.17 $\times (w - 0.02) \times ((w - 0.02) + 4.095) ]$
M9 (My2)	Sqrt [ 7.54 $\times (w - 0.02) \times ((w - 0.02) + 4.435) ]$
M9 (UTM)	Sqrt [ 39.26 $\times (w - 0.02) \times ((w - 0.02) + 5.025) ]$

### 12.3.6.3.2 AC Operation, Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options)

The table in section 12.3.6.3.1 applies to 1P9M process. For other metallization options (in table 2.5.3), please use Irms of M8 and M9 as the first and second Mn or My, respectively.

For example, 1P7M with M1 as ML1, M2 ~ M6 as Mx, and M7 as Mn, the Irms rules are:

Metal level	Irms (mA)
M1	Sqrt [ 18.51 × Δ T × (w - 0.02) × ((w - 0.02) + 0.484 ) ]
M2 (Mx1)	Sqrt [ 5.936 × Δ T × (w - 0.02) × ((w - 0.02) + 0.654 ) ]
M3 (Mx2)	Sqrt [ 3.110 × Δ T × (w - 0.02) × ((w - 0.02) + 1.248 ) ]
M4 (Mx3)	Sqrt [ 2.108 × Δ T × (w - 0.02) × ((w - 0.02) + 1.842 ) ]
M5 (Mx4)	Sqrt [ 1.594 × Δ T × (w - 0.02) × ((w - 0.02) + 2.436 ) ]
M6 (Mx5)	Sqrt [ 1.282 × Δ T × (w - 0.02) × ((w - 0.02) + 3.030 ) ]
M7(3XTM)	Sqrt [ 2.584 × Δ T × (w - 0.02) × ((w - 0.02) + 4.159 ) ]

Another example, 1P7M with M1 as ML1, M2 ~ M5 as Mx, M6 and M7 as Mn, the Irms rules are:

Metal level	Irms (mA)
M1	Sqrt [ 18.51 × Δ T × (w - 0.02) × ((w - 0.02) + 0.484 ) ]
M2 (Mx1)	Sqrt [ 5.936 × Δ T × (w - 0.02) × ((w - 0.02) + 0.654 ) ]
M3 (Mx2)	Sqrt [ 3.110 × Δ T × (w - 0.02) × ((w - 0.02) + 1.248 ) ]
M4 (Mx3)	Sqrt [ 2.108 × Δ T × (w - 0.02) × ((w - 0.02) + 1.842 ) ]
M5 (Mx4)	Sqrt [ 1.594 × Δ T × (w - 0.02) × ((w - 0.02) + 2.436 ) ]
M6 (3XTM)	Sqrt [ 2.584 × Δ T × (w - 0.02) × ((w - 0.02) + 4.159 ) ]
M7 (3XTM)	Sqrt [ 2.306 × Δ T × (w - 0.02) × ((w - 0.02) + 4.664 ) ]

## 12.3.6.4 PeakCurrent

$$I_{\text{peak}} = \max (|I(t)|)$$

$I_{\text{peak}}$  is the current at which a metal line undergoes excessive Joule heating and can begin to melt. This current should be used infrequently.

The limit for the peak current,  $I_{\text{peak}}$ , can be calculated by using the following formula:

$$I_{\text{peak}} = \frac{I_{\text{peak\_DC}}}{\sqrt{r}}$$

$r$  is the duty ratio, which is equal to the pulse duration divided by the period,

$$r = \frac{t_D}{\tau}$$

where  $I_{\text{peak\_DC}}$  is provided in the following table. In the table, w (in  $\mu\text{m}$ ) represents the width of the metal line.

Metal Level	$I_{\text{peak\_DC}}$ (mA)
M1	$50.0 \times (w-0.02)$
M2	$32.5 \times (w-0.02)$
M3	$32.5 \times (w-0.02)$
M4	$32.5 \times (w-0.02)$
M5	$32.5 \times (w-0.02)$
M6	$32.5 \times (w-0.02)$
M7	$32.5 \times (w-0.02)$
M8 (3XTM)	$63.0 \times (w-0.02)$
M9 (3XTM)	$63.0 \times (w-0.02)$
M8 (2XTM)	$39.2 \times (w-0.02)$
M9 (2XTM)	$39.2 \times (w-0.02)$
M9 (UTM)	$126 \times (w-0.02)$

The  $I_{\text{peak}}$  rule applies to the periodic AC or pulsed DC signals.

For a single event high current pulse or signals which cannot be specified by duty ratio, please follow the ESD guidelines in Chapter 11.

The  $I_{\text{peak}}$  rules provided in this section are applicable to signals with a pulse width ( $t_D$ ) of less than 1 $\mu\text{sec}$ . No temperature adjustment factor for the  $I_{\text{rms}}$  and  $I_{\text{peak}}$  is given.

The  $I_{\text{rms}}$  and  $I_{\text{peak}}$  of contacts and vias do not include because the heating in contacts and vias is negligible and is usually determined by metal or substrate. If the metal width is increased to some extent and only one via is used in that metal, then the heating in the via cannot be considered negligible. However, if the design follows the SM rules, via heating can be negligible. Please follow the VIAx.R.2~6,11, VIAy.R.2~6, and VIAz.R.2 rules to make sure that the via heating is not a problem.

## 12.3.7 N90/N85/N80 AP RDL (AP-MD) Current Density (EM) Specification

### 12.3.7.1 Maximum DC Current

$J_{max}$  is maximum DC current allowed per  $\mu\text{m}$  of AP RDL (AP-MD) metal line width or per CB via. The number is based on 0.1% point of measurement data at 10% resistance increase after 100K hours of continuous operation at 110°C. Use the following table to calculate  $I_{max}$  if the junction temperature differs from 110°C.

Temperature	105C	110C	115C	120C	125C
Rating factor of $I_{max}$	1.150	1.000	0.872	0.763	0.670

For example,  $J_{max}$  (at 125°C) =  $0.670 \times J_{max}$  (at 110°C).

### 12.3.7.2 Maximum DC Current for AP RDL Metal (AP-MD) Lines ( $T_j = 110^\circ\text{C}$ )

The table provides the maximum allowed DC current,  $I_{max}$  for each of the metal wiring levels at junction temperature of 110°C. In the table,  $w$  (in  $\mu\text{m}$ ) represents the width of the drawn metal line.

N90 AP RDL (AP-MD) Current Density (EM) Specification:

Metal Wiring Level	$I_{max}$ (mA)	RDL thickness
AP RDL	$2.7 \times w$	14.5K Å
AP RDL	$5.21 \times w$	28K Å

N85 AP RDL (AP-MD) Current Density (EM) Specification:

Metal Wiring Level	$I_{max}$ (mA)	RDL thickness
AP RDL	$2.87 \times w \times 0.94$	14.5K Å
AP RDL	$5.54 \times w \times 0.94$	28K Å

N80 AP RDL (AP-MD) Current Density (EM) Specification:

Metal Wiring Level	$I_{max}$ (mA)	RDL thickness
AP RDL	$3.0 \times w \times 0.9$	14.5K Å
AP RDL	$5.79 \times w \times 0.9$	28K Å

### 12.3.7.3 Maximum DC Current for AP RDL (RV) Vias (CB-VD) ( $T_j = 110^\circ\text{C}$ )

The table provides the maximum allowed DC current,  $I_{max}$  for each of the contact and via at junction temperature of 110°C. In the table, the sizes of contact and via are also noted.

Interlevel Connection	$I_{max}$ (mA)	Size
RV	7	per RV $3 \times 3 \mu\text{m}^2$

## 12.3.8 N90/N85/N80 AP RDL AC Operation

The general terminology for AP RDL is the same as Cu interconnects.

The following tables provide the maximum  $I_{rms}$  allowed for AP RDL at a junction temperature of 110°C. In the table,  $w$  (in  $\mu\text{m}$ ) represents the width of the RDL line and  $\Delta T$  ( $^{\circ}\text{C}$ ) is the temperature rise due to Joule heating.

Metal level	$I_{rms}$ (mA)	RDL Thickness
AP RDL	Sqrt [ $1.71 \times \Delta T \times w \times (w + 5.207)$ ]	<b>14.5K Å</b>
AP RDL	Sqrt [ $3.30 \times \Delta T \times w \times (w + 5.207)$ ]	<b>28K Å</b>

The  $I_{peak}$  rule for AP RDL is 58 mA/ $\mu\text{m}$  for RDL thickness=14.5 KA.

The  $I_{peak}$  rule for AP RDL is 112 mA/ $\mu\text{m}$  for RDL thickness=28.0 KA.

## 12.3.9 N90/N85/N80 Poly Current Density Guidelines

The maximum current density for poly resistor (unsilicided) is 0.375 mA/ $\mu\text{m}$  at a junction temperature of 110°C. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 100K hours of continuous operation.

Use the following table to calculate  $I_{max}$  if the junction temperature differs from 110°C. For a junction temperature below 105°C, use the rule at 105°C.

J	1	1	1
F	1	1	0

For example,  $I_{max}$  (at 125°C) =  $0.927 \times I_{max}$  (at 110°C).

This rule is applicable to N+, and P+ unsilicided poly resistors.

For silicided poly, the maximum DC current density should be less than 6mA/ $\mu\text{m}$  at a junction temperature of 110°C. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 100K hours of continuous operation.

## 12.3.10 N90/N85/N80 OD Current Density Guidelines

For diffusion (OD) unsilicided resistors and/or silicided interconnect, no  $I_{max}$  rule is given. Since diffusion (OD) is crystalline silicon with implantation, no electromigration or Joule heating problems occur. If the design follows contact, metal, and via current density rules, there will be no reliability concern for diffusion (OD).

## 12.4 Product Early Failure Rate Screening Guidelines

The guidelines in this section can help you improve product Early Failure Rate (EFR) either in wafer level or package level. Dynamic Voltage Stress (DVS) testing or low noise margin (LNM) testing methods at the wafer level could be applied for AlCu and pure Cu processes.

### 12.4.1 Wafer Level Screening

TSMC's wafer level screening methodology includes DVS stress and LNM methods.

#### 12.4.1.1 Wafer-Level Screening - DVS

TSMC recommend you to check the following items before DVS screening:

1. DVS stress voltage cannot apply on circuitry with voltage regulator to avoid unnecessary damage.
2. DVS stress voltage cannot apply on analog circuitry.
3. Try to avoid spiking noise signal during DVS stress.

##### 12.4.1.1.1 Stress Voltage Setting

Schmoo plot verification prior to formal stress is recommended for stress voltage settings. You should avoid introducing any artificial damage (for example, latch-up, EOS, localized over-stress, and so on).

After the stress test, it is recommended that you verify the correlation between product burn-in result and wafer level screening data.

##### 12.4.1.1.2 Stress Time

A stress duration of 500 ms to 1000 ms has proven to be effective. You need to compare that effectiveness against the costs of testing before finalizing the stress time.

##### 12.4.1.1.3 Screening Criteria

You can choose any one of the following criteria. The following criteria should correlate to package level burn in failure rate and define the acceptance specification.

1. **Tightened  $I_{sb}$ :** Defined by the  $I_{sb}$  cumulated distribution plot from production lots.
2. **Delta  $I_{sb}$ :** Defined by the delta  $I_{sb}$  cumulated distribution plot
3. **Low voltage or high frequency functionality test:** Defined by  $V_{ccmin}$  or scan like test

## 12.4.1.2 Wafer-Level Screening - LNM

It has been demonstrated that devices with low noise margins (LNM) are reliably weaker parts. Reliably weaker parts can be identified successfully by comparing CP sort bin (speed, data retention, and  $V_{ccmin}$ ) degradation between the ambient temperature and the high temperature (HT).

TSMC recommend you to check the following items before LNM screening:

1. Be sure of  $I_{sb}$  or  $I_{ddq}$  current specifications available at high temperature.
2. Be sure of product can be operated at a high temperature and have toggle test pattern.
3. Be sure of speed index or  $V_{ddmin}$  datalog could be extracted as a reliability assessment parameter.
4. Be sure of testing hardware setup like probe card and tester environment were stable and reliable for high temperature testing.

### 12.4.1.2.1 HT Temperature Setting

HT screening without artificial damage greatly depends on the product design windows or margins at HT. These windows or margins need to be checked by wafer sorting

### 12.4.1.2.2 Stress Duration

A temperature of 85°C can increase device gate leakage ( $I_g$ ) by 8% ~ 10% and, thus, narrow down the noise margin. You need to judge the reliability requirements and design a balanced test regime that avoids unnecessary over-stress to the product. Please consult TSMC before implementing this method.

### 12.4.1.2.3 Screening Criteria

1. **Tightened  $V_{ddmin}$ :** The tailing parts in a  $V_{ddmin}$  distribution are dice with the lowest LNM. A tight  $V_{ddmin}$  specification is defined by the  $V_{ddmin}$  distribution plot of the production lots. STD+3 sigma is recommended.
2. **Delta speed:** A delta of speed is defined by the delta speed distribution plot of the production lots.
3. **Functional test screening:** High temperature narrows the noise margin. Thus, the function test at HT directly screens out dice with the LNM.

## 12.4.2 Package-Level Screening – Product Burn-In

### Recommendations:

1. **Voltage:**  $1.4 \times V_{cc}$  to core;  $1.1 \times V_{cc}$  to I/O and  $V_{ih}$ .
2. **Temperature:** Depends on the product transistor counts and burn-in patterns design. To avoid thermal run away, you should estimate the whole chip leakage by using a specific burn in pattern and check the thermal resistance of package material before setting this temperature.
3. **Pattern:** ATPG (Automatic Test Pattern Generation) or the scan pattern with the highest transistor coverage is recommended.
4. **Duration:** Less than 6 hours or judging from bathtub curve to meet specific product early failure rate criteria.

## 12.4.3 Soft Error Rate

TSMC follows JEDEC's JESD89 in the domain of SER. So the definition, test methodology, FIT calculation and so on will follow the description in JESD89.

### Introduction

Soft errors are nondestructive functional errors induced by energetic ion strikes. Soft errors are a subset of single event effects (SEE), and include single-event upsets (SEU), multiple-bit upsets (MBU), single-event functional interrupts (SEFI), single-event transients (SET) that, if latched, become SEU, and single-event latch-up (SEL) where the formation of parasitic bipolar action in CMOS wells induce a low-impedance path between power and ground, producing a high current condition (SEL can also cause latent and hard errors).

In general, soft errors may be induced by alpha particles emitted from radioactive impurities in materials nearby the sensitive volume, such as packaging, solder bumps, etc., and by highly ionizing secondary particles produced from the reaction of both thermal and high-energy terrestrial neutrons with component materials.

There are two fundamental methods to determine a product's SER. One is to test a large number of actual production devices for a long enough period of time (weeks or months) until enough soft errors have been accumulated to give a reasonably confident estimate of the SER. This is generally referred to as a real-time or unaccelerated SER testing. Real-time testing has the advantage of being a direct measurement of the actual product SER requiring no extrapolation, assumptions, or special experimental structures, equipment, etc. (provided the test is performed in a building location similar to the actual use environment). However, Real-time testing requires expensive systems monitoring hundreds or thousands of devices in parallel, for long periods of time.

The other method commonly employed to allow more rapid SER estimations and to clarify the source of errors is accelerated-SER (ASER) testing. In ASER testing, devices are exposed to a specific radiation source whose intensity is much higher than the ambient levels of radiation the device would normally encounter. ASER allows useful data to be obtained in a fraction of the time required by real-time, unaccelerated real-time testing. Only a few units are needed and complete evaluations can often be done in a few hours or days instead of weeks or months. The disadvantages of ASER are that the results must be extrapolated to use conditions and that several different radiation sources must be used to ensure that the estimation accounts for soft errors induced by both alpha particle and cosmic-ray-neutron events.

TSMC's soft errors measurement, including alpha and neutron, are ASER that follows JEDEC Standard (JESD89).

## 12.4.3.1 Alpha SER

### Introduction

Uranium and thorium impurities found in trace amounts in the various production and packaging materials emit alpha particles. Alpha particles are strongly ionizing, so those that impinge on the active device create bursts of free electron-hole pairs in the silicon. This charge disruption can be collected at pn junctions (much like charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. The alpha flux is independent of altitude, and is only a function of the type, location, and amount radioactive impurities present in the component or its package.

### 12.4.3.1.1 Alpha Source

Different types of alpha sources can be used to simulate the alpha emission from uranium and thorium impurities. Here is the information of the alpha source used in TSMC.

Source :  $^{241}\text{Am}$

Energy : 5.4MeV

Activity : 3722.2 Bq (=0.1006uCi)

Area : 1320.25 mm<sup>2</sup>

Alpha particle source Flux : 2.819/mm<sup>2</sup>-sec (= Activity / Area)

Packaged component alpha Flux : 27.8E-10 /mm<sup>2</sup>-sec or 0.001 c/cm<sup>2</sup>-h

G factor : Calculated from the die size and DUT-to-alpha source space.

Acceleration factor : G \* (Alpha particle source Flux / Packaged component alpha Flux)

### 12.4.3.1.2 Test Condition

#### 12.4.3.1.2.1 Packaging for alpha particle testing

Unlike real-time and accelerated neutron and proton test methods where the package type is not critical, for accelerated alpha particle testing the DUT's surface must be directly exposed to the isotope source without any intervening solid material and with a minimal air gap.

Recommended DUT package types are the ceramic dual-in-line (CERDIP) or pin-grid array (CERPGA) package. Certainly, other package types that offer access to the top surface of the chip can also be used but these types in particular are mechanically robust particularly when used with zero-insertion force (ZIF) sockets allowing reliable loading and unloading over many cycles.

The die should be mounted and wirebonded within the well or cavity such that the surface of the die is as close as possible to the top surface of the package without anything, such as the bond wires, projecting above this plane. This configuration is required to minimize the alpha source-to-die spacing, while providing a convenient indexing surface for the isotope source. The metal lid for the package should be installed with tape to protect the DUT between tests.

If the product to be tested is already encapsulated in a plastic package, the material over the die must be etched back to fully expose the active area. If the manufacturer's packaging includes an alpha shielding layer, typically polyimide, over the surface of the die, this must be left in place at full thickness for accurate testing. In this case it is best to have unpackaged, but coated, samples of the DUT provided by the manufacturer for alpha testing, rather than attempting to etch back the existing packaging material. Lead-over-chip (LOC) packages are not suitable since the lead frame shadows a large portion of the device. FC packages with solder bumps distributed over the face of the die are also not suitable for the same reason.

#### 12.4.3.1.2.2 Test pattern

The basic test pattern for all memory circuits is a logical checkerboard, alternating by address and bit. If detailed layout information for the DUT is available, a physical checkerboard is also useful. A determination of the best test pattern is left to the discretion of the tester, but must be documented in the test report.

The use of physical data patterns, i.e. patterns that are related to the actual layout of the DUT, rather than the logical addressing are recommended where possible. These patterns may provide insight into the ionizing radiation sensitivity of the DUT. Because layout information is generally proprietary only DUT manufacturers would generally be expected to be able to meet this recommendation.

Some devices, particularly dynamic RAMs (DRAMs) and logic elements often have a “preferred” soft-error failure, either  $0 \rightarrow 1$  or  $1 \rightarrow 0$ . The selected test pattern must consider this possibility in its design. For testing when there is no a priori knowledge of the device the test pattern should balance the number of 0’s and 1’s. If the relative failure rates are known, perhaps from previous test experience, the test pattern can be adjusted to improve statistics of the less likely transition. The use of an unbalanced test pattern must be described fully in the final report and data analysis.

#### 12.4.3.1.3 FIT Calculation

To determine the actual field product failure rate from soft errors requires extrapolating the accelerated test results to the nominal use conditions. The product SER under normal use conditions can be obtained by multiplying the observed SER (rate of soft errors) during the accelerated testing by the ratio of the alpha particle flux reaching the DUT active device area under normal use conditions and the alpha flux reaching the DUT active device areas during the test according to the following equation.

$$\text{Unaccelerated Alpha Particle SER} = \frac{\text{ASER}}{\text{Acceleration\_factor}}$$

Where ASER is the soft error rate obtained from the DUT during accelerated testing, and Acceleration\_factor is calculated in the section of 9.4.3.1.1. As mentioned earlier, since the accelerated source uses an alpha particle source with a flux that is significantly higher than the nominal package environment, this Acceleration\_factor is in the range of  $10^5$  to  $10^{14}$  and consequently the unaccelerated SER will be significantly lower than the ASER observed during accelerated testing. This equation and method is not part of the actual requirement However, all alpha particle SER data must include a description of the assumption made for geometry factor along with all experimental parameters (e.g. source size, DUT active area, source-to-DUT spacing, etc.) that would enable an outside observer to verify that the assumptions used were valid.

Finally, it is not uncommon to use dedicated test structures instead of the final product during accelerated testing. This is particularly true if in cases where a technology’s alpha-particle SER sensitivity is being determined prior to actual qualified production. It is recommended that alpha testing of at least a few actual production components be done following test chip data to ensure that the test chip used is representative of the SER sensitivity in actual products.

## 12.4.3.2 Cosmic (Neutron) SER

### Introduction

Terrestrial cosmic rays, at sea level up to moderate altitudes, are dominated by neutrons, with some contributions from other particles like protons and pions. Neutrons interact with Si and other nuclei via strong nuclear interactions. These processes produce a variety of secondary particles - protons, neutrons, alpha particles and heavy recoil nuclei. Some of these secondary particles are strongly ionizing, so those that impinge on the active device create bursts of free electron-hole pairs in the silicon. This charge disruption can be collected at pn junctions (much like charge created by light), producing a current spike (noise pulse) in the circuit. These current spikes can be large enough to alter the data state on some circuits. This section deals with the method of determining a component's sensitivity to high-energy neutron events from accelerated experiments.

This section deals strictly with SER induced by high-energy neutron events. The high energy neutron flux is dependent on altitude, latitude, and solar activity.

### 12.4.3.2.1 Neutron Beam Selection

A spallation neutron source, such as the ICE House (formerly known as the Weapons Neutron Research, WNR) facility at the Los Alamos National or the TRIUMF Neutron Facility allows one to measure the SEU rate and derive an *averaged* SEU cross section. Because the neutrons produced from a spallation source cover a wide energy spectrum, the user cannot extract a SEU cross section at a specific energy from such measurements, but rather obtains the contribution of SEU events from neutrons of all energies within the spectrum. The major reason that a spallation neutron source is widely used is that the shape of the energy spectrum from this beam is similar to the spectrum of the terrestrial neutrons on the ground. In Figure 9-1, we compare the neutron spectra from the beams at Los Alamos and TRIUMF with the scaled neutron spectrum at ground level.

The ICE House spectrum in Figure 9-1 is at the location of the LANL fission detector, which was at a point 19.97 meters down the flight path from the tungsten target. DUTs are located further down the flight path, so that the neutron flux will be reduced by the following ratio  $r^2/(r+d)^2$ , where  $r$  is the distance to the detector (19.97 m in this case) and  $d$  is the distance between the detector and the DUT. At TRIUMF the spectrum in Figure 9-1 also applies at the location of the DUT so no correction needs to be made.

When testing with a spallation neutron source, the SEUs recorded will be due primarily to the high energy (e.g.  $> 10$  MeV) neutrons. The SEU contribution of the neutrons in the  $1 < E < 10$  MeV range is small,  $< 10\%$ , but these neutrons comprise  $\sim 40\%$  of all neutrons  $> 1$  MeV in the terrestrial spectrum (as can be seen in Fig. 12.4.1). Further, if a spallation neutron source is used that contains thermal neutrons, which is not true at Los Alamos, care must be taken to subtract out the SEUs that are caused by the thermal neutrons.

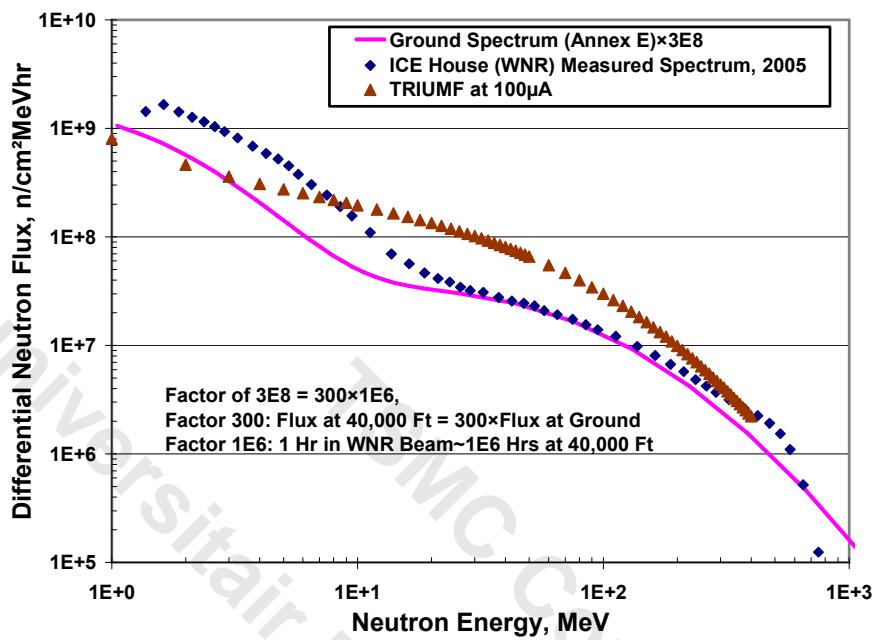


Figure 12.4.1: Comparison of Los Alamos and TRIUMF neutron beam spectra with terrestrial neutron spectrum

### 12.4.3.2.2 Basic Test Methodology

The basic test methodology for memory arrays is storing a known data pattern in the array while the part is exposed to the accelerated beam and comparing the stored pattern that is present after the device has been irradiated. At some time during and/or after the exposure, the data is evaluated to identify the number of changes in the pattern as errors. Other circuits may have different tester requirements.

### 12.4.3.2.3 FIT Calculation

#### 12.4.3.2.3.1 Cross-section and FIT calculation

The cross-section defines the sensitivity of a device. The cross-section per bit is defined as  $\sigma = N/(F \cdot C)$  where N is the total number of errors, F is the fluence and C is the number of bits of the tested memory. In this document the cross-section is given in  $\text{cm}^2/\text{bit}$ .

Since the WNR neutron beam has a neutron energy spectrum very similar to that of the terrestrial neutron energy spectrum, the cross-section per bit obtained at WNR can be used directly to estimate the terrestrial failure rate.

According to the JEDEC specification, the FIT rate is calculated using the value of neutron flux for New-York City,  $f_{\text{NYC}} = 14 \text{ n/cm}^2/\text{hour}$  for neutrons with energy above 10 MeV. The FIT is calculated in TSMC's report for a memory capacity of 1 Mbit. Thus, FIT is given by the following formula:

$$\text{FIT} = \sigma \cdot f_{\text{NYC}} \cdot 10^9 \cdot 2^{20} \text{ (errors / } 10^9 \text{ hour / 1 Mbit)}$$

Where  $\sigma$  is the cross-section per bit given in  $\text{cm}^2/\text{bit}$ , and  $f_{\text{NYC}}$  is the flux given in  $\text{n/cm}^2/\text{hour}$ .

The FIT is calculated using the neutron flux for New-York City, and for a memory capacity of 1 Mbit. The neutron flux depends on the altitude and location.

#### 12.4.3.2.3.2 Accuracy of Result

The accuracy of the measured cross-section is the sum of the following components:

The error rate is generally described by a Poisson distribution, cf. appendix C.1 of JEDEC. The standard deviation depends on the number of errors observed. If N errors occur, the standard deviation is  $\sqrt{N}$ . Thus the cross-section accuracy is  $1/\sqrt{N}$ .

There are cases of interest where small numbers of events are observed (including the case where no events occur). The cross section can be bounded for such cases using the upper and lower counting events in the table below, extracted from appendix C.2 of JEDEC. In using this table, the first column is the actual number of events observed in the experiment. The upper and lower limits show how high (or low) the number of events could actually be if the experiment were continued for much longer time periods.

Accuracy of the fluence measurement for each run. This accuracy is better than 3% for the WNR facility.

95% confidence limit

Events	Lower limit	Upper limit
0	0.0	3.7
1	0.1	5.6
2	0.2	7.2
3	0.6	8.8
4	1.0	10.2
5	1.6	11.7
6	2.2	13.1
7	2.8	14.4
8	3.4	15.8
9	4.0	17.1
10	4.7	18.4
20	12.2	30.9
50	37.1	65.9
100	81.4	121.6

## 12.4.3.3 Suggestion to Improve SER

### 12.4.3.3.1 SER Mitigation Options

Many papers discussed about SER mitigation options and some are experimented in TSMC. Here lists the SER mitigation options that have been published.

**Error Correction Codes:** By far, the most effective method of dealing with soft errors in memory components is by employing additional circuitry for error detection and/or correction. Typically, error correction is achieved by adding extra bits to each data vector encoding the data so that the “information distance” between any two possible data vectors is, at least, three. Larger information distances can be achieved with more parity bits and additional circuitry – but in general, the single error correctin double error detection (SECDED) schemes are favored. In these systems, if a single error occurs (a change of plus or minus one in information space), there is no chance that the corrupted vector will be mistaken for its nearest neighbors (since the information distance is three). In fact, if two errors occur in the same “correction word”, a valid error vector will still be produced. The only limitation is that with two errors the error vector will not be unique to a single data value, thus only detection of double-bit errors is supported. There are two suggestions to make the ECC more reliable. First, scramble and interleaving must be taken into consideration. Physical adjacent bits should not map to the same logic word. Second, memory scrubbing can correct latent errors before they build up to cause uncorrectable errors. The combination of ECC and scrubbing gives a very high-reliable framework only area penalty must be concerned.

**Reduction of Alpha –Particle Upset:** The effect of alpha-particle-induced upset in semiconductors has been known for over two decades due to trace contamination of Thorium and Uranium in the chip packaging materials and lead in the solder and flip-chip bumps. Unlike neutrons, the amount of alpha particles can be: 1) controlled by the process technology and 2) shielded from the sensitive areas of the chip. Low alpha particle mold compounds and thick polyimide coatings( $>15 \mu m$ ) are used to shield the chip from package-induced alpha particles. For flip-chip-mounted devices, “keep-out” designs are used where the sensitive memory arrays are maintained at a sufficient distance so that alpha particles generated from the lead bumps must traverse large angles through the top layers (and therefore, significant material thickness) before they arrive at the sensitive volume of the circuit. Low alpha count lead can also be used, but there is a significant increase in material cost for this isotopic purity.

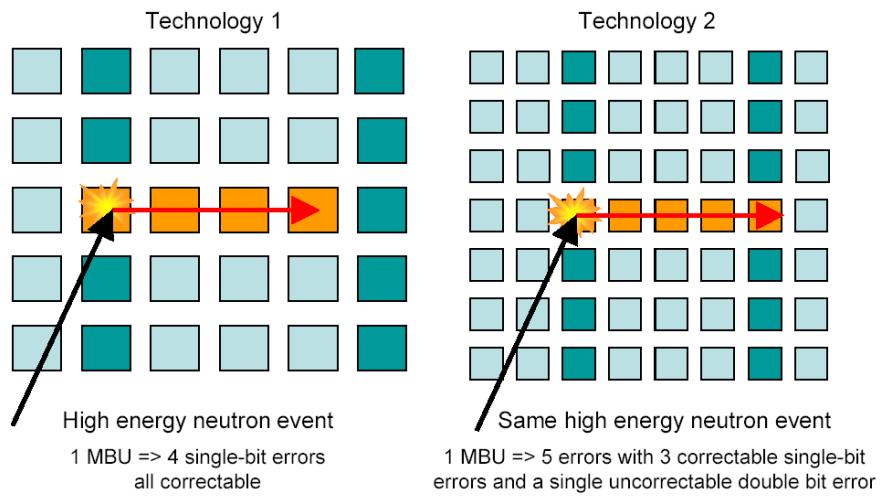
**Elimination of Borophosphosilicate Glass (BPSG):** BPSG is used as a planarization and gettering layer immediately about the transistors. However, the  $^{10}B$  isotope has a large capture cross section for thermal neutrons, which leads to energetic fission byproducts (a  $^7Li$  recoil, an alpha particle, and a gamma ray) and increased SERs. The development of chemmechanical polishing (CMP) techniques for planarization in deep submicrometer designs have largely replaced the need for BPSG in logic and SRAM processes, so SER due to thermal neutrons can be eliminated.

**Added SRAM Capacitance:** Addition of a metal-insulator-metal (MIM) node capacitor can reduce the SRAM cell-upset rate from high-energy neutrons by roughly an order of magnitude, but not eliminate cell upset altogether. However, there can also be a penalty on the write cycle of  $\sim 20$  ps/fF. In TSMC, the 1T-MiM reduces SER FIT over one order of magnitude than 6T-SRAM in the same technology generation.

**Triple Well Structure:** Triple well structures have been widely used for both a better electrical isolation and a reduction of the noise originating from the substrate. As most actual devices are processed in a p-substrate, triple well is usually designated as deep n-well (DNW) or also n+ buried layer. DNW theoretically reduces the SER sensitivity as the electrons generated deep inside the substrate are more efficiently collected by the extended n buried zone and then better evacuated through n-well ties. Practically, DNW shows no improvement in TSMC 90nm SRAM.

### 12.4.3.3.2 ECC & MBU

The Error Correcting Code(ECC) function is a very efficient way to reduce SER though the circuit area overhead is considerable. But there still is the limitation of ECC function. When the errors occur in the same multiplexer(MUX) under the same wordline(WL), it will become a uncorrectable error. As the bitcell area scales down, the occurrence of uncorrectable error will increase due to the Multiple-Bit-Upset(MBU). The illustration below can explain this phenomenon.

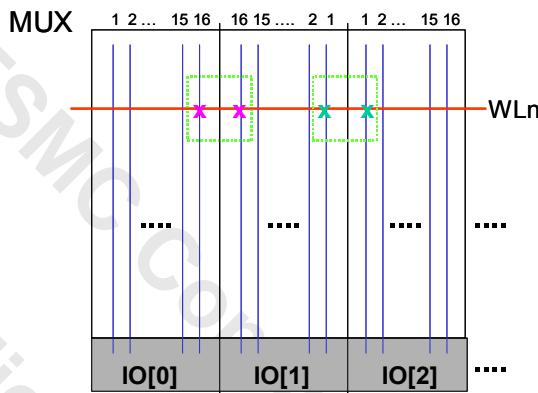


### 12.4.3.3.3 Design Suggestion for MBU

In order to avoid the uncorrectable error due to MBU, TSMC has two suggestions.

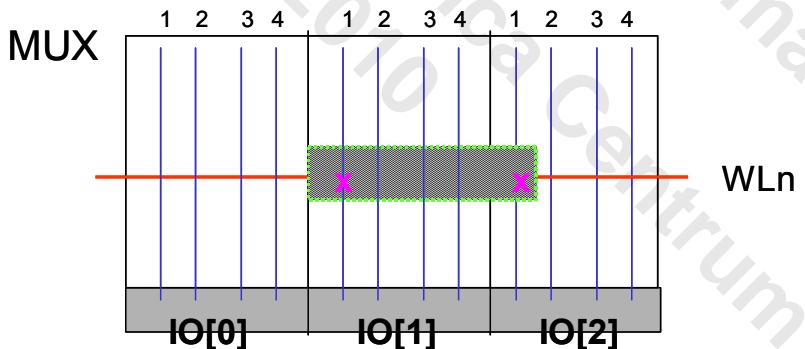
#### 1. Avoid Mirror type scramble layout.

Please refer to the illustration below as an example. If the I/O boundary is hit, it will make the word uncorrectable, because ECC can't correct 2(or more) errors in one word accessed. It's recommended to avoid this type design.



#### 2. Use MUX-8 or higher design

Please refer to the illustration below as an example. If one MBU possibly includes 5 adjacent fail bits, however, it happens in MUX-4 design. It will cause an uncorrectable error. For this issue, increasing the MUX number can raise the tolerance of MBU. Now the observed maximum adjacent bits number of one MBU due to neutron strike in N90 generation is 6. So it's recommended to use MUX-8 or higher design.



## 12.5 e-Reliability Model System Introduction

The system objectives are to provide a simple, consistent and instant way to address our customers' needs for reliability assessment in designing and production. TSMC provides a user-friendly reliability calculator on TSMC Online.

### 12.5.1 What is the e-Reliability Model System?

The system provides you reliability assessment for TSMC's process technologies, that includes intrinsic and product-level reliability.

A. Intrinsic reliability assessment:

This includes gate oxide integrity (GOI), hot carrier injection (HCI), negative bias temperature instability (NBTI), electron migration (EM), and time depend dielectric breakdown of inter-metal dielectric (IMD-TDDB)

B. Product-level reliability assessment:

This includes early failure rate (EFR), long term failure rate (LTFR), and estimates of voltage overdrive capability, the impact of voltage overshoot on circuit reliability, and allowable junction temperature.

### 12.5.2 Why the e-Reliability Model System?

The e-Reliability model system will help you achieve built-in reliability design and attain their business goals by using

1. A simple and instant way to do circuit lifetime prediction.
2. A model to predict production failure rate.
3. A solution provider to customize voltage/temperature/layout configurations.

### 12.5.3 Where to access the e-Reliability Model System?

The e-Reliability model system is built into TSMC Online on the Web in the Quality & Reliability section. There are two ways to use this system:

1. From overall Reliability Assessment, which provides an estimate of circuit lifetime for a user-defined set of circuit operating conditions and transistor and interconnect layout geometry.
2. From advanced Reliability Assessment, which provides (a) Reliability assessment for individual failure items under a given set of circuit operating conditions and layout geometry. (b) Product-level reliability (EFR, LTFR) or voltage/temperature estimates, resulting from user level-defined operating conditions and die size.

# 13 Electrical Parameters Summary

- 13.1 Available MOS transistors
- 13.2 Key parameters of MOS transistors in CLN90G
- 13.3 Key parameters of MOS transistors in CLN90GT
- 13.4 Key parameters of MOS transistors in CLN90LP
- 13.5 Key parameters of MOS transistors in CLN85G
- 13.6 Key parameters of MOS transistors in CLN85LP
- 13.7 Key parameters of MOS transistors in CLN80GC
- 13.8 Key parameters of MOS transistors in CLN80GT
- 13.9 Key parameters of MOS transistors in CLN80HS
- 13.10 Key parameters of MOS transistors in CLN80LP
- 13.11 Key parameters for bipolar transistors
- 13.12 Key parameters for junction diodes
- 13.13 Resistor model
- 13.14 Resistor models for unsilicided N+/P+ poly resistors
- 13.15 Resistor models for unsilicided N+/P+ diffusion resistors
- 13.16 Interconnect model
- 13.17 MIM capacitor model
- 13.18 RTMOM capacitor model
- 13.19 Inductor model

All the dimensions in this chapter are wafer dimensions, unless specified otherwise. The electrical parameters are given for T=25°C, unless specified otherwise.

The electrical parameters in this chapter are dependent on the following documents. Please be sure to use the most update version for circuit design.

Technology		Core/IO	Doc NO.	Version
CLN90	G	1.0V/1.8V	T-N90-LO-SP-001	V1.5
		1.0V/2.5V	T-N90-LO-SP-002	V2.0
		1.0V/3.3V	T-N90-LO-SP-003	V2.1
		1.0V/ 1.8V, 3.3V	T-N90-CL-SP-005	V1.5
	GT	1.2V/2.5V	T-N90-CL-SP-013	V1.3
		1.2V/1.8V	T-N90-CL-SP-028	V1.2
	LP	1.2V/2.5V	T-N90-LO-SP-008	V2.2
		1.2V/3.3V	T-N90-LO-SP-009	V2.3
CLN85	G	1.0V/1.8V	T-N85-CL-SP-004	V1.0
		1.0V/2.5V	T-N85-CL-SP-006	V1.0
		1.0V/3.3V	T-N85-CL-SP-002	V1.2
		1.0V/ 1.8V, 3.3V	T-N85-CL-SP-007	V1.0
	LP	1.2V/2.5V	T-N85-CL-SP-001	V1.1
		1.2V/3.3V	T-N85-CL-SP-003	V1.1
CLN80	GC	1.0V/2.5V	T-N80-CL-SP-014	V1.1
		1.0V/3.3V	T-N80-CL-SP-015	V1.1
	GT	1.2V/2.5V	T-N80-CL-SP-001	V1.1
		1.2V/1.8V	T-N80-CL-SP-003	V1.0
	HS	1.05V/1.8V	T-N80-CL-SP-002	V1.1
		1.05V/2.5V	T-N80-CL-SP-004	V1.0
	LP	1.2V/2.5V	T-N80-CL-SP-005	V1.0
CMN90	G for MS	1.0V/1.8V	T-N90-CM-SP-011	V1.2
		1.0V/2.5V	T-N90-CM-SP-012	V2.0
		1.0V/3.3V	T-N90-CM-SP-011	V1.2
		1.0V/ 1.8V, 3.3V	T-N90-CM-SP-011	V1.2
	GT for MS	1.2V/2.5V	T-N90-CM-SP-007	V1.1
		1.2V/1.8V	T-N90-CM-SP-021	V1.0
	LP for MS	1.2V/2.5V	T-N90-CM-SP-001	V2.0
		1.2V/3.3V	T-N90-CM-SP-003	V2.0
	G for RF	1.0V/2.5V	T-N90-CM-SP-013	V1.1
		1.0V/3.3V	T-N90-CM-SP-016	V1.1
	LP for RF	1.2V/2.5V	T-N90-CM-SP-004	V1.2
		1.2V/3.3V	T-N90-CM-SP-005	V1.2
CMN85	G for MS	1.0V/2.5V	T-N85-CM-SP-003	V1.1
		1.0V/3.3V	T-N85-CM-SP-004	V1.1
	LP for MS	1.2V/2.5V	T-N85-CM-SP-001	V1.1
		1.2V/3.3V	T-N85-CM-SP-002	V1.1
CMN80	GC for MS	1.0V/2.5V	T-N80-CM-SP-001	V1.2
		1.0V/3.3V	T-N80-CM-SP-002	V1.1

## 13.1 Available MOS Transistors

### 13.1.1 CLN90G (1.0V)

	Model name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.0V Standard Vt MOS	nch	pch	23.3	25.0	0.1	0.1
1.0V High Vt MOS	nch_hvt	pch_hvt	23.3	25.0	0.1	0.1
1.0V Low Vt MOS	nch_lvt	pch_lvt	23.3	25.0	0.1	0.1
1.8V MOS	nch_18	pch_18	34.5	37.0	0.20	0.20
2.5V MOS	nch_25	pch_25	55.4	58.2	0.28	0.28
3.3V MOS	nch_33	pch_33	72.0	75.0	0.38	0.38
1.0V Native MOS	nch_na	-	23.3	-	0.2	-
1.8V Native MOS	nch_na18	-	34.5	-	0.8	-
2.5V Native MOS	nch_na25	-	55.4	-	1.2	-
3.3V Native MOS	nch_na33	-	72.0	-	1.2	-

### 13.1.2 CLN90GT (1.2V)

	Model name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.2V Standard Vt MOS	nch	pch	23.3	25.0	0.1	0.1
1.2V High Vt MOS	nch_hvt	pch_hvt	23.3	25.0	0.1	0.1
1.2V Low Vt MOS	nch_lvt	pch_lvt	23.3	25.0	0.1	0.1
1.8V MOS	nch_18	pch_18	34.5	37.0	0.20	0.20
2.5V MOS	nch_25	nch_25	55.4	58.2	0.28	0.28
1.2V Native MOS	nch_na	-	23.3	-	0.2	-
1.8V Native MOS	nch_na18	-	34.5	-	0.8	-
2.5V Native MOS	nch_na25	-	55.4	-	1.2	-

### 13.1.3 CLN90LP (1.2V)

	Model Name		Eletirc Tox(A)		Minimum Length(um)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.2V SVT MOS	nch	pch	28.3	30	0.1	0.1
1.2V HVT MOS	nch_hvt	pch_hvt	28.3	30	0.1	0.1
1.2V LVT MOS	nch_lvt	pch_lvt	28.3	30	0.1	0.1
1.2V ULVT MOS	nch_ulvt	pch_ulvt	28.3	30	0.1	0.1
2.5V MOS	nch_25	pch_25	55.4	58.2	0.28	0.28
1.2V Native MOS	nch_na	-	28.3	-	0.2	-
3.3V Native MOS	nch_na33	-	72	-	1.2	-

### 13.1.4 CLN85G (1.0V)

	Model Name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.00V_Standard_Vt_MOS	nch	pch	23.3	25	0.094	0.094
1.00V_High_Vt_MOS	nch_hvt	pch_hvt	23.3	25	0.094	0.094
1.00V_Low_Vt_MOS	nch_lvt	pch_lvt	23.3	25	0.094	0.094
1.80V_MOS	nch_18	pch_18	34.5	37	0.188	0.188
2.50V_MOS	nch_25	pch_25	55.4	58.2	0.2632	0.2632
3.30V_MOS	nch_33	pch_33	72	75	0.3572	0.3572
1.00V_Native_Vt_MOS	nch_na	---	23.3	-	0.188	-
1.80V_Native_Vt_MOS	nch_na18	---	34.5	-	0.752	-
2.50V_Native_MOS	nch_na25	-	55.4	-	1.128	-
3.30V_Native_Vt_MOS	nch_na33	---	72	-	1.128	-

### 13.1.5 CLN85LP (1.2V)

	Model Name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.2V_Standard_Vt_MOS	nch	pch	28.3	30	0.094	0.094
1.2V_High_Vt_MOS	nch_hvt	pch_hvt	28.3	30	0.094	0.094
1.2V_Low_Vt_MOS	nch_lvt	pch_lvt	28.3	30	0.094	0.094
1.2V_Ultra_Low_Vt_MOS	nch_ulvt	pch_ulvt	28.3	30	0.094	0.094
1.2V_Native_MOS	nch_na	-	28.3	-	0.188	-
2.5V_MOS	nch_25	pch_25	55.4	58.2	0.2632	0.2632
3.3V_MOS	nch_33	pch_33	72	75	0.3572	0.3572
2.5V_Native_MOS	nch_na25	-	55.4	-	1.128	-
3.3V_Native_MOS	nch_na33	-	72	-	1.128	-

### 13.1.6 CLN80GC (1.0V)

	Model name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.0V Standard Vt MOS	nch	pch	23.4	25.0	0.09	0.09
1.0V High Vt MOS	nch_hvt	pch_hvt	23.4	25.0	0.09	0.09
1.0V Low Vt MOS	nch_lvt	pch_lvt	23.4	25.0	0.09	0.09
1.0V Ultra Low Vt MOS	nch_ulvt	pch_ulvt	23.4	25.0	0.09	0.09
2.5V MOS	nch_25	pch_25	54.4	58.3	0.279	0.279
3.3V MOS	nch_33	pch_33	72.0	75.0	0.373	0.373
1.0V Native MOS	nch_na	-	23.4	-	0.270	-
2.5V Native MOS	nch_na25	-	54.4	-	1.188	-
3.3V Native MOS	nch_na33	-	72.0	-	1.188	-

### 13.1.7 CLN80GT (1.2V)

	Model name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.2V Standard Vt MOS	nch	pch	23.2	25.0	0.09	0.09
1.2V High Vt MOS	nch_hvt	pch_hvt	23.2	25.0	0.09	0.09
1.8V MOS	nch_18	pch_18	35.1	38.4	0.198	0.198
2.5V MOS	nch_25	pch_25	56.0	59.2	0.279	0.279
1.2V Native MOS	nch_na	-	23.2	-	0.198	-
1.8V Native MOS	nch_na18	-	35.1	-	0.792	-
2.5V Native MOS	nch_na25	-	56.0	-	1.188	-

### 13.1.8 CLN80HS (1.05V)

	Model name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.05V Standard Vt MOS	nch	pch	19.1	20.5	0.09	0.09
1.05V High Vt MOS	nch_hvt	pch_hvt	19.1	20.5	0.09	0.09
1.05V Low Vt MOS	nch_lvt	pch_lvt	19.1	20.5	0.09	0.09
1.8V MOS	nch_18	pch_18	35.2	38.4	0.198	0.198
2.5V MOS	nch_25	pch_25	54.4	58.3	0.279	0.279
1.2V Native MOS	nch_na	-	19.1	-	0.27	-
1.8V Native MOS	nch_na18	-	35.2	-	0.792	-
2.5V Native MOS	nch_na25	-	54.4	-	1.197	-

[T-N80-CL-SP-002 (1.05V/1.8V) v1.2 -> v1.1] => value 1.05V/ 2.5V in SPCIE document

[T-N80-CL-SP-001 (1.05V/2.5V) v1.1 -> v1.0 => value 1.05V/ 2.5V in SPCIE document

### 13.1.9 CLN80LP (1.2V)

	Model name		Electric_Tox (Å)		Minimum Length (μm)	
	NMOS	PMOS	NMOS	PMOS	NMOS	PMOS
1.2V Standard Vt MOS	nch	pch	28.2	30.3	0.09	0.09
1.2V High Vt MOS	nch_hvt	pch_hvt	28.2	30.3	0.09	0.09
2.5V MOS	nch_25	pch_25	58.9	61.5	0.279	0.279

## 13.2 Key Parameters of MOS Transistors in CLN90G

### 13.2.1 1.0V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V Standard V<sub>t</sub> MOS in CLN90G process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition		
ΔL (x <sub>l</sub> +/- dx <sub>l</sub> )			um	-0.035±0.005		-0.035±0.005				
ΔW(x <sub>w</sub> +/- dx <sub>w</sub> )			um	0.01±0.008		0.01±0.008				
Electrical_Tox			Å	23.3±0.600		25±0.600				
V <sub>t_gm</sub>	10	10	V	0.221		0.172		V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0		
				0.027	-0.027	0.024	-0.024			
				0.344		0.324				
	0.6	0.1		0.052	-0.052	0.052	-0.052			
				0.282		0.320				
				0.067	-0.074	0.064	-0.064			
V <sub>t_lin</sub>	10	10	V	0.162		0.180		V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0		
				0.028	-0.028	0.025	-0.023			
				0.279		0.347				
	0.6	0.1		0.058	-0.059	0.059	-0.059			
				0.232		0.344				
				0.076	-0.085	0.075	-0.074			
V <sub>t_sat</sub>	10	10	V	0.156		0.162		V <sub>g</sub> @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0		
				0.194		0.240				
				0.161		0.267				
DIBL	0.6	0.1	V	0.085085		-0.1066		V <sub>b</sub> =0, V <sub>t_lin</sub> -V <sub>t_sat</sub>		
Id_lin	0.6	0.1	uA/um	117.94		30.718		Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0		
				113.32		31.22				
Id_sat	0.6	0.1		634.73		240.79		Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0		
				-15.1%	15.1%	-18.0%	20.2%			
	0.12	0.1		654.16		235.86				
				-22.2%	24.7%	-25.1%	24.4%			
Ioff	0.6	0.1	pA/um	11486		4618.5		Id @V <sub>g</sub> =0, V <sub>d</sub> =1.0Vdd, V <sub>s</sub> =V <sub>b</sub> =0		
				0.174	7.082	0.144	6.374			
Sub V <sub>t</sub> slope	0.6	0.1	mV/dec	97.078		102.89		Slope @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0, V <sub>g1</sub> =V <sub>t_sat</sub> -0.05, V <sub>g2</sub> =V <sub>t_sat</sub> -0.06		
Ig_inv	10	10	nA/um <sup>2</sup>	24.636		7.9075		Ig @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>s</sub> =V <sub>b</sub> =0		
Body effect	0.6	0.1	V	0.050		0.062		ΔV <sub>t_sat</sub> @V <sub>b</sub> =-V <sub>dd</sub> /2 and V <sub>b</sub> =0		
Isub	0.6	0.1	nA/um	1.130E-01		7.121E-04		I <sub>bmax</sub> @V <sub>s</sub> =V <sub>b</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , sweep V <sub>g</sub>		
Covl	0.6	0.1	fF/um	2.88E-01		2.39E-01		C <sub>gd</sub> @V <sub>g</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0		
C <sub>j</sub>			fF/um <sup>2</sup>	0.98		1.14		V <sub>rev</sub> =0V		
Inverter FO=1 Delay	Wn/Wp= 3.5/5	0.1	ps/gate	9.34664			RO_Td(ring oscillator delay time) @ V=V <sub>dd</sub> (Fan_out=1)			
				2.00066		-1.47071				

## 13.2.2 1.0V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V High V<sub>t</sub> MOS in CLN90G process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition
ΔL (xL +/- dxL)			um	-0.035±0.005		-0.035±0.005		
ΔW(xw +/- dxw)			um	0.01±0.008		0.01±0.008		
Electrical_Tox			Å	23.3±0.600		25±0.600		
Vt_gm	10	10	V	0.356	0.327	Vg @ Vd=0.05V, Vs=Vb=0		
				0.026	-0.026	0.028	-0.028	
	0.6	0.1		0.448	0.397			
				0.054	-0.055	0.047	-0.052	
	0.12	0.1		0.365	0.392			
				0.084	-0.082	0.058	-0.067	
Vt_lin	10	10	V	0.281	0.347	Vg @ Vd=0.05V, Vs=Vb=0		
				0.026	-0.025	0.028	-0.025	
	0.6	0.1		0.374	0.423			
				0.057	-0.057	0.052	-0.059	
	0.12	0.1		0.314	0.417			
				0.092	-0.089	0.066	-0.073	
Vt_sat	10	10	V	0.274	0.341	Vg @ Vd=Vdd, Vs=Vb=0		
				0.284	0.327			
				0.247	0.347			
DIBL	0.6	0.1	V	0.090154	-0.096421	Vb=0, Vt_lin-Vt_sat		
Id_lin	0.6	0.1	uA/um	101.13	26.779	Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0		
				103.81	26.94			
Id_sat	0.6	0.1	uA/um	506.93	194.81	Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0		
				-17.1%	17.5%	-19.7%	20.3%	
	0.12	0.1		545.27	186.53			
				-23.8%	24.3%	-24.6%	24.9%	
loff	0.6	0.1	pA/um	1282	680.4	Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0		
				0.210	5.626	0.197	5.608	
Sub Vt slope	0.6	0.1	mV/dec	98.067	105.05	Slope @ Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06		
Ig_inv	10	10	nA/um <sup>2</sup>	22.987	8.2789	Ig @ Vg=Vdd, Vd=Vs=Vb=0		
Body effect	0.6	0.1	V	0.063	0.084	ΔVt_sat @ Vb=-Vdd/2 and Vb=0		
Isub	0.6	0.1	nA/um	1.380E-01	9.253E-04	Ibmax @ Vs=Vb=0, Vd=Vdd, sweep Vg		
Covl	0.6	0.1	fF/um	2.78E-01	2.28E-01	Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0		
Cj			fF/um <sup>2</sup>	1.09	1.17	Vrev=0V		
Inverter FO=1 Delay	Wn/Wp= 3.5/5	0.1	ps/gate	12.3939		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)		
				2.7441	-2.178			

### 13.2.3 1.0V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V Low V<sub>t</sub> MOS in CLN90G process.

	W (μm)	L (μm)	Unit	NMOS		PMOS		Definition	
ΔL (xl +/- dxl)			um	-0.035±0.005		-0.035±0.005			
ΔW(xw +/- dxw)			um	0.01±0.008		0.01±0.008			
Electrical_Tox			A	23.3±0.600		25±0.600			
Vt_gm	10	10	V	0.227		0.170		Vg @Vd=0.05V, Vs=Vb=0	
				0.025	-0.026	0.027	-0.027		
				0.263		0.264			
	0.6	0.1		0.056	-0.054	0.057	-0.055		
				0.227		0.274			
				0.077	-0.076	0.063	-0.064		
Vt_lin	10	10	V	0.161		0.177		Vg @Vd=0.05V, Vs=Vb=0	
				0.027	-0.027	0.028	-0.024		
				0.208		0.287			
	0.6	0.1		0.059	-0.060	0.065	-0.062		
				0.176		0.294			
				0.087	-0.087	0.076	-0.076		
Vt_sat	10	10	V	0.156		0.164		Vg @Vd=Vdd, Vs=Vb=0	
				0.112		0.173			
				0.108		0.205			
DIBL	0.6	0.1	V	0.095325		-0.11439		Vb=0, Vt_lin-Vt_sat	
Id_lin	0.6	0.1	uA/um	133.32		33.921		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				119.24		33.085			
Id_sat	0.6	0.1	uA/um	742.12		288.51		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-16.0%	17.1%	-21.1%	20.4%		
	0.12	0.1		743.16		270.48			
				-25.1%	28.3%	-27.3%	31.5%		
loff	0.6	0.1	pA/um	81926		25876		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.126	7.412	0.128	6.072		
Sub Vt slope	0.6	0.1	mV/dec	89.118		100.37		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um2	23.983		11.177		Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.6	0.1	V	0.046		0.050		ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.6	0.1	nA/um	1.520E+00		5.255E-03		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.6	0.1	fF/um	2.87E-01		2.48E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	0.987		1.13		Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.5/5	0.1	ps/gate	7.49414			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)		
				1.78106		-1.2694			

## 13.2.4 1.8V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.8V Standard V<sub>t</sub> MOS in CLN90G process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.055 \pm 0.008$	$-0.055 \pm 0.008$		
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0 \pm 0.012$	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$34.5 \pm 1.333$	$37.0 \pm 1.333$		
Vt_gm	10	10	V	0.343	0.381	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.051   -0.051	0.052   -0.051		
				0.451	0.444		
	10.0	0.2		0.059   -0.060	0.062   -0.058		
				0.450	0.448		
				0.073   -0.068	0.080   -0.071		
Vt_lin	10	10		0.288	0.396	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.053   -0.053	0.054   -0.054		
				0.384	0.431		
	10.0	0.2		0.066   -0.067	0.068   -0.064		
				0.370	0.459		
				0.082   -0.077	0.088   -0.078		
Vt_sat	10	10	V	0.279	0.381	$V_g @ V_d=V_{dd}, V_s=V_b=0$	
				0.325	0.364		
				0.312	0.393		
DIBL	10.0	0.2	V	0.060	0.066	$V_b=0, V_t_{lin}-V_t_{sat}$	
Id_lin	10.0	0.2	$\mu\text{A}/\mu\text{m}$	82.4	25.8	$Id @ V_g=V_{dd}, V_d=0.05\text{V}, V_s=V_b=0$	
				77.3	20.0		
Id_sat	10.0	0.2	$\mu\text{A}/\mu\text{m}$	680	310	$Id @ V_g=V_{dd}, V_d=V_{dd}, V_s=V_b=0$	
				14.2%   -13.0%	14.3%   -12.8%		
	0.40	0.2		652	256		
				19.3%   -17.3%	19.1%   -17.6%		
Ioff	10.0	0.2	pA/ $\mu\text{m}$	66	19	$Id @ V_g=0, V_d=1.0V_{dd}, V_s=V_b=0$	
				4.2E+02   -55	1.2E+02   -16		
Sub Vt slope	10.0	0.2	mV/dec	87	95	Slope @ $V_d=V_{dd}, V_s=V_b=0, V_{g1}=V_t_{sat}-0.05, V_{g2}=V_t_{sat}-0.06$	
Ig_inv	10	10	nA/ $\text{um}^2$	0	0	$Ig @ V_g=V_{dd}, V_d=V_s=V_b=0$	
Body effect	10.0	0.2	V	0.143	0.160	$\Delta V_t_{sat} @ V_b=-V_{dd}/2 \text{ and } V_b=0$	
Isub	10.0	0.2	nA/ $\text{um}$	6.66E+00	8.03E-02	$I_{bmax} @ V_s=V_b=0, V_d=V_{dd}, \text{sweep } V_g$	
Covl			fF/ $\text{um}$	0.266	0.238	$C_{gd} @ V_g=0, V_d=V_{dd}, V_s=V_b=0$	
Cj			fF/ $\text{um}^2$	0.966	1.078	$V_{rev}=0\text{V}$	
Inverter FO=1 Delay	Wn/Wp = 3.5/5	0.2	ps/gate	16.28		RO_Td(ring oscillator delay time) @ $V=V_{dd}$ (Fan_out=1)	
				2.48	-2.09		

## 13.2.5 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN90G process.

	W ( $\mu$ m)	L ( $\mu$ m)	Unit	NMOS	PMOS	Definition	
$\Delta L$ (x1 +/- dx1)			um	-0.015±0.01	-0.015±0.01		
$\Delta W(xw+/-dxw)$			um	0±0.012	0±0.012		
Electrical_Tox			$\text{\AA}$	55.4±3.000	58.2±3.000		
Vt_gm	10	10	V	0.512	0.615	Vg @Vd=0.05V, Vs=Vb=0	
				0.031   -0.031	0.031   -0.031		
				0.579	0.512		
				0.050   -0.050	0.050   -0.051		
				0.506	0.505		
	0.4	0.28		0.075   -0.075	0.080   -0.081		
				0.461	0.651		
				0.032   -0.032	0.034   -0.034		
				0.528	0.528		
				0.053   -0.053	0.057   -0.058		
Vt_lin	10	0.28	V	0.463	0.545	Vg @Vd=0.05V, Vs=Vb=0	
				0.080   -0.081	0.088   -0.088		
				0.451	0.637		
				0.442	0.463		
				0.390	0.486		
DIBL	10	0.28	V	0.086665	-0.065344	Vb=0, Vt_lin-Vt_sat	
Id_lin	10	0.28	uA/um	48.6	16.2	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				45.5	13.8		
Id_sat	10	0.28	uA/um	580	289	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-7.6%   8.0%	-8.4%   7.9%		
	0.4	0.28		566	253		
				-13.2%   14.0%	-13.2%   13.1%		
loff	10	0.28	pA/um	1.410	3.540	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.212   5.299	0.269   4.061		
Sub Vt slope	10	0.28	mV/dec	101	106	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um <sup>2</sup>	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	10	0.28	V	0.160	0.293	$\Delta Vt_{sat}$ @Vb=-Vdd/2 and Vb=0	
Isub	10	0.28	nA/um	2.071E+02	1.149E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	10	0.28	fF/um	1.97E-01	2.10E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.08	1.08	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp=5/3.5	0.28	ps/gate	27.19		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.96	-1.66		

## 13.2.6 3.3V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 3.3V Standard V<sub>t</sub> MOS in CLN90G process.

	W ( $\mu$ m)	L ( $\mu$ m)	Unit	NMOS	PMOS	Definition	
$\Delta L$ (x1 +/- dx1)			um	-0.015±0.012	-0.015±0.012		
$\Delta W$ (xw+/- dxw)			um	0±0.012	0±0.012		
Electrical_Tox			$\text{\AA}$	72±3.000	75±3.000		
Vt_gm	10	10	V	0.595	0.683	Vg @Vd=0.05V, Vs=Vb=0	
				0.023   -0.023	0.034   -0.034		
	10	0.38		0.680	0.626		
				0.060   -0.060	0.050   -0.050		
	0.4	0.38		0.616	0.620		
				0.070   -0.070	0.060   -0.060		
Vt_lin	10	10	V	0.542	0.736	Vg @Vd=0.05V, Vs=Vb=0	
				0.024   -0.024	0.037   -0.037		
	10	0.38		0.633	0.663		
				0.063   -0.062	0.055   -0.055		
	0.4	0.38		0.564	0.671		
				0.076   -0.074	0.067   -0.067		
Vt_sat	10	10	V	0.527	0.719	Vg @Vd=Vdd, Vs=Vb=0	
				0.559	0.613		
	0.4	0.38		0.500	0.615		
DIBL	10	0.38	V	0.0734	-0.0496	Vb=0, Vt_lin-Vt_sat	
Id_lin	10	0.38	uA/um	36.14	12.38	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				34.43	10.87		
Id_sat	10	0.38	uA/um	589	286	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-5.9%   6.0%	-7.9%   7.9%		
	0.4	0.38		580	264		
				-8.2%   9.6%	-9.5%   9.6%		
Ioff	10	0.38	pA/um	0.10953	0.12622	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.276   4.333	0.558   2.285		
Sub Vt slope	10	0.38	mV/dec	96	104	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	10	0.38	V	0.255	0.309	$\Delta Vt_{sat}$ @Vb=-Vdd/2 and Vb=0	
Isub	10	0.38	nA/um	8.591E+02	1.113E+01	lbmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	10	0.38	fF/um	1.65E-01	1.73E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	0.962	1.04	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.5/5	0.38	ps/gate	34.4		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				2.15	-1.87		

## 13.2.7 1.0V Native NMOS

The following table summarizes the key parameters for 1.0V native NMOS in CLN90G process.

	<b>W (<math>\mu</math> m)</b>	<b>L (<math>\mu</math> m)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			$\mu$ m	$-0.055 \pm 0.005$			
$\Delta W(x_w +/- dx_w)$			$\mu$ m	$0.010 \pm 0.008$			
Electrical_Tox			$\text{\AA}$	$23.3 \pm 0.6$			
Vt_gm	10	10	V	-0.004		$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.035	-0.035		
				0.172			
	10	0.2		0.054	-0.060		
				0.166			
				0.062	-0.066		
Vt_lin	10	10	V	-0.059		$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.036	-0.036		
				0.112			
	10	0.2		0.058	-0.063		
				0.112			
				0.066	-0.070		
Vt_sat	10	10	V	-0.088		$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
				0.057			
				0.062			
DIBL	10	0.2	V	0.055		$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	10	0.2	$\mu A / \mu m$	87.2		$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
				81.7			
Id_sat	10	0.2	$\mu A / \mu m$	586		$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				14.4%   -12.6%			
	0.5	0.2		563			
				17.4%   -15.2%			
Ioff	10	0.2	$pA / \mu m$	138100		$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				6.8E+05   -1.2E+05			
Sub Vt slope	10	0.2	mV/dec	77		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g 1 = V_t_{sat} - 0.05, V_g 2 = V_t_{sat} - 0.06$	
Ig_inv	10	10	nA/ $\mu m^2$	24		$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	10	0.2	V	0.021		$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	10	0.2	nA/ $\mu m$	0.06		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/ $\mu m$	0.275		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/ $\mu m^2$	0.144		$V_{rev} = 0V$	

## 13.2.8 1.8V Native NMOS

The following table summaries the key parameters for 1.8V native NMOS in CLN90G process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			μ m	$-0.04 \pm 0.008$		
$\Delta W(x_w +/- dx_w)$			μ m	$0 \pm 0.012$		
Electrical_Tox			Å	$34.5 \pm 1.333$		
$V_t_{gm}$	10	10	V	-0.022	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.051   -0.051		
				0.071		
	10	0.8		0.070   -0.070		
				0.078		
				0.080   -0.080		
$V_t_{lin}$	10	10		-0.076	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.053   -0.053		
				0.019		
	10	0.8		0.072   -0.073		
				0.035		
				0.084   -0.083		
$V_t_{sat}$	10	10	V	-0.119	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	10	0.8		-0.016		
	0.5	0.8		-0.039		
DIBL	10	0.8	V	0.035	$V_b = 0, V_t_{lin} - V_t_{sat}$	
$I_d_{lin}$	10	0.8	$\mu A / \mu m$	29.8	$I_d @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
				27.7		
$I_d_{sat}$	10	0.8	$\mu A / \mu m$	485	$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				11.4%   -10.4%		
	0.5	0.8		450		
				15.2%   -13.5%		
$I_{off}$	10	0.8	$pA / \mu m$	199900	$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				1.1E+06   -1.7E+05		
Sub Vt slope	10	0.8	mV/dec	79	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g1 = V_t_{sat} - 0.05, V_g2 = V_t_{sat} - 0.06$	
$I_g_{inv}$	10	10	nA/um <sup>2</sup>	0	$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	10	0.8	V	0.020	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
$I_{sub}$	10	0.8	nA/um	0.29	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{ sweep } V_g$	
Covl			fF/um	0.280	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
$C_j$			fF/um <sup>2</sup>	0.142	$V_{rev} = 0V$	

### 13.2.9 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN90G process.

	<b>W ( <math>\mu\text{m}</math> )</b>	<b>L ( <math>\mu\text{m}</math> )</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>
$\Delta L$ ( $x_1 +/- dx_1$ )			um	$-0.04 \pm 0.01$		
$\Delta W$ ( $x_w +/- dx_w$ )			um	$0 \pm 0.012$		
Electrical_Tox			A	$55.4 \pm 3.000$		
Vt_gm	10	10	V	-0.141	Vg @ $V_d=0.05\text{V}$ , $V_s=V_b=0$	
				0.058	-0.058	
				-0.167		
	10	1.2		0.086	-0.087	
				-0.145		
				0.087	-0.087	
Vt_lin	10	10	V	-0.157	Vg @ $V_d=0.05\text{V}$ , $V_s=V_b=0$	
				0.060	-0.060	
				-0.189		
	0.5	1.2		0.089	-0.089	
				-0.159		
				0.090	-0.091	
Vt_sat	10	10	V	-0.166	Vg @ $V_d=V_{dd}$ , $V_s=V_b=0$	
				-0.260		
				-0.192		
DIBL	10	1.2	V	0.071485	$V_b=0$ , $V_t_{lin}-V_t_{sat}$	
Id_lin	10	1.2	uA/um	20.0	Id @ $V_g=V_{dd}$ , $V_d=0.05\text{V}$ , $V_s=V_b=0$	
				18.5		
Id_sat	10	1.2	uA/um	451	Id @ $V_g=V_{dd}$ , $V_d=V_{dd}$ , $V_s=V_b=0$	
				-10.4%    11.7%		
	0.5	1.2		427		
				-13.0%    14.9%		
loff	10	1.2	pA/um	8.04E+06	Id @ $V_g=0$ , $V_d=1.0V_{dd}$ , $V_s=V_b=0$	
				0.402    1.952		
Sub Vt slope	10	1.2	mV/dec	68	Slope @ $V_d=V_{dd}$ , $V_s=V_b=0$ , $V_g1=V_t_{sat}-0.05$ , $V_g2=V_t_{sat}-0.06$	
lg_inv	10	10	nA/um <sup>2</sup>	0	lg @ $V_g=V_{dd}$ , $V_d=V_s=V_b=0$	
Body effect	10	1.2	V	0.041	$\Delta V_t_{sat}$ @ $V_b=-V_{dd}/2$ and $V_b=0$	
Isub	10	1.2	nA/um	1.57	Ibmax @ $V_s=V_b=0$ , $V_d=V_{dd}$ , sweep $V_g$	
Covl	10	1.2	fF/um	0.186	Cgd @ $V_g=0$ , $V_d=V_{dd}$ , $V_s=V_b=0$	
Cj			fF/um <sup>2</sup>	0.124	Vrev=0V	

## 13.2.10 3.3V Native NMOS

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	Definition	
$\Delta L$ ( $x_1 +/- dx_1$ )			um	-0.045±0.012		
$\Delta W(x_w+/- dx_w)$			um	0±0.012		
Electrical_Tox			$\text{\AA}$	72±3.000		
Vt_gm	10	10	V	-0.145	Vg @Vd=0.05V, Vs=Vb=0	
				0.049 -0.049		
	10	1.2		-0.173		
				0.076 -0.077		
	0.5	1.2		-0.140		
				0.077 -0.077		
Vt_lin	10	10	V	-0.164	Vg @Vd=0.05V, Vs=Vb=0	
				0.051 -0.051		
	10	1.2		-0.189		
				0.079 -0.080		
	0.5	1.2		-0.145		
				0.081 -0.081		
Vt_sat	10	10	V	-0.172	Vg @Vd=Vdd, Vs=Vb=0	
	10	1.2		-0.307		
	0.5	1.2		-0.180		
DIBL	10	1.2	V	0.11796	Vb=0, Vt_lin-Vt_sat	
Id_lin	10	1.2	uA/um	20.3	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.5	1.2		20.0		
Id_sat	10	1.2	uA/um	545	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-8.6% 9.3%		
	0.5	1.2		509		
				-11.3% 12.7%		
loff	10	1.2	pA/um	1.04E+07	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.525 1.668		
Sub Vt slope	10	1.2	mV/dec	71	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um <sup>2</sup>	0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	10	1.2	V	0.053	$\Delta V_{t\_sat}$ @Vb=-Vdd/2 and Vb=0	
Isub	10	1.2	nA/um	24.03	Idmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	10	1.2	fF/um	0.179	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.139	Vrev=0V	

The following table summarizes the key parameters for 3.3V native NMOS in CLN90G process.

## 13.3 Key Parameters of MOS Transistors in CLN90GT

### 13.3.1 1.2V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Standard V<sub>t</sub> MOS in CLN90GT process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l + -dx_l)$			$\mu\text{m}$	$-0.037 \pm 0.005$	$-0.037 \pm 0.005$		
$\Delta W(x_w + -dx_w)$			$\mu\text{m}$	$0.015 \pm 0.008$	$0.015 \pm 0.008$		
Electrical_Tox			$\text{\AA}$	$23.3 \pm 0.6$	$25.0 \pm 0.6$		
Vt_gm	10	10	V	0.216	0.165	$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$	
				0.040   -0.040	0.040   -0.041		
				0.342	0.265		
				0.065   -0.073	0.053   -0.065		
				0.287	0.265		
	0.12	0.1		0.090   -0.099	0.074   -0.089		
				0.159	0.176		
				0.042   -0.042	0.042   -0.042		
				0.271	0.279		
				0.072   -0.083	0.063   -0.076		
Vt_lin	0.6	0.1	V	0.231	0.279	$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$	
				0.101   -0.110	0.083   -0.099		
				0.152	0.167		
				0.153	0.153		
				0.127	0.180		
DIBL	0.6	0.1	V	0.118	0.126	$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	0.6	0.1	$\mu\text{A}/\mu\text{m}$	149.9	39.4	$Id @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$	
	0.12	0.1		161.3	43.4		
Id_sat	0.6	0.1	$\mu\text{A}/\mu\text{m}$	936	416	$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				19.5%   -15.3%	22.1%   -16.9%		
	0.12	0.1		1047	432		
				26.7%   -22.3%	26.4%   -23.5%		
Ioff	0.6	0.1	pA/ $\mu\text{m}$	41480	45090	$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				27.917   0.0892	12.934   0.12422		
Sub Vt slope	0.6	0.1	mV/dec	99	103	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$	
Ig_inv	10	10	nA/um <sup>2</sup>	61	14	$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	0.6	0.1	V	0.057	0.036	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	0.6	0.1	nA/um	2.00E+00	5.25E-02	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/um	0.270	0.241	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/um <sup>2</sup>	0.981	1.115	$V_{rev} = 0\text{V}$	
Inverter FO=1 Delay	Wn/Wp = 3.5/5	0.1	ps/gate	6.51		RO_Td(ring oscillator delay time) @ $V = V_{dd}$ (Fan_out=1)	
				1.197	-1.095		

### 13.3.2 1.2V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V high V<sub>t</sub> MOS in CLN90GT process.

	<b>W (μ m)</b>	<b>L (μ m)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>	
ΔL (xl +/-dxl)			μ m	-0.037 ± 0.005	-0.037 ± 0.005		
ΔW(xw+/-dxw)			μ m	0.015 ± 0.008	0.015 ± 0.008		
Electrical_Tox			Å	23.3 ± 0.6	25.0 ± 0.6		
Vt_gm	10	10	V	0.279	0.171	Vg @Vd=0.05V, Vs=Vb=0	
				0.040 -0.041	0.040 -0.041		
	0.6	0.1		0.394	0.322		
				0.057 -0.063	0.051 -0.061		
	0.12	0.1		0.329	0.317		
				0.085 -0.093	0.074 -0.083		
Vt_lin	10	10	V	0.220	0.179	Vg @Vd=0.05V, Vs=Vb=0	
				0.042 -0.042	0.042 -0.042		
	0.6	0.1		0.327	0.342		
				0.063 -0.070	0.060 -0.071		
	0.12	0.1		0.267	0.339		
				0.094 -0.102	0.085 -0.095		
Vt_sat	10	10	V	0.215	0.160	Vg @Vd=Vdd, Vs=Vb=0	
	0.6	0.1		0.206	0.228		
	0.12	0.1		0.169	0.238		
DIBL	0.6	0.1	V	0.121	0.114	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.6	0.1	μ A/ μ m	138.9	36.7	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.12	0.1		154.7	39.8		
Id_sat	0.6	0.1	μ A/ μ m	863	360	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				19.3% -15.3%	22.1% -16.9%		
	0.12	0.1		996	386		
				27.1% -22.4%	25.3% -23.1%		
Ioff	0.6	0.1	pA/ μ m	10020	5565	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				21.687 0.102	11.7987 0.14128		
Sub Vt slope	0.6	0.1	mV/dec	98	103	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um2	60	14	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.6	0.1	V	0.066	0.071	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.6	0.1	nA/um	9.20E-01	2.11E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.268	0.224	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	1.033	1.115	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.5/5	0.1	ps/gate	7.54		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.415	-1.348		

### 13.3.3 1.2V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V low V<sub>t</sub> MOS in CLN90GT process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.037 \pm 0.005$	$-0.037 \pm 0.005$		
$\Delta W (x_w +/- dx_w)$			$\mu\text{m}$	$0.015 \pm 0.008$	$0.015 \pm 0.008$		
Electrical_Tox			$\text{\AA}$	$23.3 \pm 0.6$	$25.0 \pm 0.6$		
Vt_gm	10	10	V	0.216	0.165	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.039 -0.040	0.040 -0.041		
				0.339	0.260		
	0.6	0.1		0.068 -0.079	0.061 -0.071		
				0.287	0.260		
				0.094 -0.106	0.083 -0.096		
Vt_lin	10	10		0.159	0.176	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.041 -0.041	0.042 -0.042		
				0.268	0.273		
	0.6	0.1		0.076 -0.088	0.071 -0.082		
				0.231	0.275		
				0.106 -0.119	0.095 -0.108		
Vt_sat	10	10	V	0.152	0.167	$V_g @ V_d=V_{dd}, V_s=V_b=0$	
				0.126	0.135		
				0.107	0.166		
DIBL	0.6	0.1	V	0.142	0.138	$V_b=0, V_t_{lin}-V_t_{sat}$	
Id_lin	0.6	0.1	$\mu\text{A}/\mu\text{m}$	155.8	41.3	$Id @ V_g=V_{dd}, V_d=0.05\text{V}, V_s=V_b=0$	
				168.3	45.3		
Id_sat	0.6	0.1	$\mu\text{A}/\mu\text{m}$	985	442	$Id @ V_g=V_{dd}, V_d=V_{dd}, V_s=V_b=0$	
				21.8% -16.2%	24.6% -17.8%		
	0.12	0.1		1097	456		
				29.4% -23.5%	28.7% -24.7%		
Ioff	0.6	0.1	pA/ $\mu\text{m}$	93380	80880	$Id @ V_g=0, V_d=1.0V_{dd}, V_s=V_b=0$	
				35.896 0.0712	19.51 0.0957		
Sub Vt slope	0.6	0.1	mV/dec	101	105	Slope @ $V_d=V_{dd}, V_s=V_b=0, V_{g1}=V_t_{sat}-0.05, V_{g2}=V_t_{sat}-0.06$	
Ig_inv	10	10	nA/ $\mu\text{m}^2$	61	14	$Ig @ V_g=V_{dd}, V_d=V_s=V_b=0$	
Body effect	0.6	0.1	V	0.049	0.031	$\Delta V_t_{sat} @ V_b=-V_{dd}/2 \text{ and } V_b=0$	
Isub	0.6	0.1	nA/ $\mu\text{m}$	2.18E+00	5.76E-02	$I_{bmax} @ V_s=V_b=0, V_d=V_{dd}, \text{sweep } V_g$	
Covl			fF/ $\mu\text{m}$	0.270	0.241	$C_{gd} @ V_g=0, V_d=V_{dd}, V_s=V_b=0$	
Cj			fF/ $\mu\text{m}^2$	0.98	1.14	$V_{rev}=0\text{V}$	
Inverter FO=1 Delay	Wn/Wp = 3.5/5	0.1	ps/gate	5.9776		RO_Td(ring oscillator delay time) @ $V=V_{dd}$ (Fan_out=1)	
				1.2264	-1.0896		

### 13.3.4 1.8V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.8V Standard V<sub>t</sub> MOS in CLN90GT process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.055 \pm 0.008$	$-0.055 \pm 0.008$		
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0 \pm 0.012$	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$34.5 \pm 1.333$	$37.0 \pm 1.333$		
Vt_gm	10	10	V	0.343	0.381	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.051 -0.051	0.052 -0.051		
	10.0	0.2		0.451	0.444		
				0.059 -0.060	0.062 -0.058		
	0.40	0.2		0.450	0.448		
				0.073 -0.068	0.080 -0.071		
Vt_lin	10	10	V	0.288	0.396	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.053 -0.053	0.054 -0.054		
	10.0	0.2		0.384	0.431		
				0.066 -0.067	0.068 -0.064		
	0.40	0.2		0.370	0.459		
				0.082 -0.077	0.088 -0.078		
Vt_sat	10	10	V	0.279	0.381	$V_g @ V_d=V_{dd}, V_s=V_b=0$	
				0.325	0.364		
	10.0	0.2		0.312	0.393		
DIBL	10.0	0.2	V	0.060	0.066	$V_b=0, V_t_{lin}-V_t_{sat}$	
Id_lin	10.0	0.2	$\mu\text{A}/\mu\text{m}$	82.4	25.8	$Id @ V_g=V_{dd}, V_d=0.05\text{V}, V_s=V_b=0$	
				77.3	20.0		
Id_sat	10.0	0.2	$\mu\text{A}/\mu\text{m}$	680	310	$Id @ V_g=V_{dd}, V_d=V_{dd}, V_s=V_b=0$	
				14.2% -13.0%	14.3% -12.8%		
	0.40	0.2		652	256		
				19.3% -17.3%	19.1% -17.6%		
Ioff	10.0	0.2	pA/ $\mu\text{m}$	66 4.2E+02	19 -55	$Id @ V_g=0, V_d=1.0V_{dd}, V_s=V_b=0$	
Sub Vt slope	10.0	0.2	mV/dec	87	95	Slope @ $V_d=V_{dd}, V_s=V_b=0, Vg1=V_t_{sat}-0.05, Vg2=V_t_{sat}-0.06$	
Ig_inv	10	10	nA/um <sup>2</sup>	0	0	$Ig @ V_g=V_{dd}, V_d=V_s=V_b=0$	
Body effect	10.0	0.2	V	0.143	0.160	$\Delta V_t_{sat} @ V_b=-V_{dd}/2 \text{ and } V_b=0$	
Isub	10.0	0.2	nA/um	6.66E+00	8.03E-02	$Ib_{max} @ V_s=V_b=0, V_d=V_{dd}, \text{sweep } V_g$	
Covl			fF/um	0.266	0.238	$C_{gd} @ V_g=0, V_d=V_{dd}, V_s=V_b=0$	
Cj			fF/um <sup>2</sup>	0.966	1.078	$V_{rev}=0\text{V}$	
Inverter FO=1 Delay	Wn/Wp = 3.5/5	0.2	ps/gate	16.28		RO_Td(ring oscillator delay time) @ $V=V_{dd}$ (Fan_out=1)	
				2.48	-2.09		

### 13.3.5 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN90GT process.

	<b>W (μ m)</b>	<b>L (μ m)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
Δ L (xl +/-dxl)			μ m	-0.015 ± 0.01		-0.015 ± 0.01		
Δ W(xw +/-dxw)			μ m	0 ± 0.012		0 ± 0.012		
Electrical_Tox			Å	55.4 ± 3		58.2 ± 3		
Vt_gm	10	10	V	0.528		0.611	Vg @Vd=0.05V, Vs=Vb=0	
				0.061	-0.059	0.056		
	10.0	0.28		0.578		0.506		
				0.057	-0.055	0.064		
	0.40	0.28		0.526		0.521		
				0.086	-0.088	0.081		
Vt_lin	10	10	V	0.473		0.649	Vg @Vd=0.05V, Vs=Vb=0	
				0.062	-0.061	0.059		
	10.0	0.28		0.544		0.521		
				0.060	-0.058	0.069		
	0.40	0.28		0.491		0.548		
				0.091	-0.092	0.089		
Vt_sat	10	10	V	0.463		0.635	Vg @Vd=Vdd, Vs=Vb=0	
				0.468		0.468		
	0.40	0.28		0.428		0.501		
DIBL	10.0	0.28	V	0.076		0.054	Vb=0, Vt_lin-Vt_sat	
Id_lin	10.0	0.28	μ A/ μ m	47.7		16.6	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				44.8		13.9		
Id_sat	10.0	0.28	μ A/ μ m	577		290	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				11.8%	-11.1%	13.7%		
	0.40	0.28		566		254		
				17.5%	-15.4%	18.3%		
Ioff	10.0	0.28	pA/ μ m	1		2	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				4.5E+00	-1	1.0E+01		
Sub Vt slope	10.0	0.28	mV/dec	92		101	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um2	0		0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	10.0	0.28	V	0.170		0.259	Δ Vt_sat @Vb=-Vdd/2 and Vb=0	
Isub	10.0	0.28	nA/um	2.00E+02		1.26E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.197		0.210	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	1.08		1.08	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.5/5	0.28	ps/gate	27.6494			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				3.0664		-2.7137		

### 13.3.6 1.2V Native NMOS

The following table summarizes the key parameters for 1.2V native NMOS in CLN90GT process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (xl +/- dxl)$			μm	$-0.055 \pm 0.005$		
$\Delta W(xw +/- dxw)$			μm	$0.015 \pm 0.008$		
Electrical_Tox			Å	$23.3 \pm 0.6$		
Vt_gm	10	10	V	-0.004	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.035   -0.035		
				0.172		
	10	0.2		0.054   -0.060		
				0.166		
				0.062   -0.066		
Vt_lin	10	10	V	-0.059	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.036   -0.037		
				0.112		
	10	0.2		0.058   -0.063		
				0.112		
				0.066   -0.070		
Vt_sat	10	10	V	-0.095	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
				0.051		
				0.056		
DIBL	10	0.2	V	0.061	$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	10	0.2	$\mu A / \mu m$	96.8	$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
				91.6		
Id_sat	10	0.2	$\mu A / \mu m$	763	$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				12.1%   -10.6%		
	0.5	0.2		739		
				14.8%   -13.1%		
Ioff	10	0.2	pA/ $\mu m$	161000 5.8839   0.165	$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
Sub Vt slope	10	0.2	mV/dec	77	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$	
Ig_inv	10	10	nA/ $\mu m^2$	60	$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	10	0.2	V	0.025	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	10	0.2	nA/ $\mu m$	0.60	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/ $\mu m$	0.272	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/ $\mu m^2$	0.144	$V_{rev} = 0V$	

### 13.3.7 1.8V Native NMOS

The following table summarizes the key parameters for 1.8V native NMOS in CLN90GT process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			μm	$-0.04 \pm 0.008$		
$\Delta W(x_w +/- dx_w)$			μm	$0 \pm 0.012$		
Electrical_Tox			Å	$34.5 \pm 1.333$		
Vt_gm	10	10	V	-0.022	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.051   -0.051		
	10	0.8		0.071		
				0.070   -0.070		
	0.5	0.8		0.078		
				0.080   -0.080		
Vt_lin	10	10	V	-0.076	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.053   -0.053		
	10	0.8		0.019		
				0.072   -0.073		
	0.5	0.8		0.035		
				0.084   -0.083		
Vt_sat	10	10	V	-0.119	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	10	0.8		-0.016		
	0.5	0.8		-0.039		
DIBL	10	0.8	V	0.035	$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	10	0.8	$\mu A / \mu m$	29.8	$I_d @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
				27.7		
Id_sat	10	0.8	$\mu A / \mu m$	485	$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				11.4%   -10.4%		
	0.5	0.8		450		
				15.2%   -13.5%		
Ioff	10	0.8	$pA / \mu m$	199900	$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				1.1E+06   -1.7E+05		
Sub Vt slope	10	0.8	mV/dec	79	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g 1 = V_t_{sat} - 0.05, V_g 2 = V_t_{sat} - 0.06$	
Ig_inv	10	10	nA/um <sup>2</sup>	0	$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	10	0.8	V	0.020	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	10	0.8	nA/um	0.29	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{ sweep } V_g$	
Covl			fF/um	0.280	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/um <sup>2</sup>	0.142	$V_{rev} = 0V$	

### 13.3.8 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN90GT process.

	<b>W (μ m)</b>	<b>L (μ m)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			μ m	-0.04 ± 0.01		
$\Delta W(x_w +/- dx_w)$			μ m	0 ± 0.012		
Electrical_Tox			Å	55.4 ± 3		
$V_t_{gm}$	10	10	V	-0.140	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.058   -0.058		
				-0.166		
				0.085   -0.086		
	0.5	1.2		-0.145		
				0.086   -0.086		
				-0.158		
				0.060   -0.060		
$V_t_{lin}$	10	10	V	-0.190	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.088   -0.089		
	0.5	1.2		-0.161		
				0.089   -0.090		
$V_t_{sat}$	10	10	V	-0.169	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	10	1.2		-0.264		
	0.5	1.2		-0.194		
DIBL	10	1.2	V	0.074	$V_b = 0, V_t_{lin} - V_t_{sat}$	
$I_d_{lin}$	10	1.2	$\mu A / \mu m$	20.1	$I_d @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
				18.7		
$I_d_{sat}$	10	1.2	$\mu A / \mu m$	454	$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				11.8%   -10.5%		
	0.5	1.2		429		
				14.7%   -12.9%		
$I_{off}$	10	1.2	$pA / \mu m$	8203000	$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				7.7E+06   -5.0E+06		
Sub Vt slope	10	1.2	mV/dec	71	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g 1 = V_t_{sat} - 0.05, V_g 2 = V_t_{sat} - 0.06$	
$I_g_{inv}$	10	10	nA/um <sup>2</sup>	0	$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	10	1.2	V	0.043	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
$I_{sub}$	10	1.2	nA/um	1.56	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/um	0.189	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
$C_j$			fF/um <sup>2</sup>	0.124	$V_{rev} = 0V$	

## 13.4 Key Parameters of MOS Transistors in CLN90LP

### 13.4.1 1.2V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Standard V<sub>t</sub> MOS in CLN90LP process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L$ ( $x_1 +/- dx_1$ )			um	-0.02±0.005	-0.02±0.005		
$\Delta W$ ( $xw +/- dxw$ )			um	0.01±0.008	0.01±0.008		
Electrical_Tox			Å	28.3±0.670	30±0.670		
V <sub>t_gm</sub>	10	10	V	0.259	0.203	V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
				0.027 -0.027	0.027 -0.027		
	0.6	0.1		0.483	0.409		
				0.056 -0.058	0.060 -0.060		
	0.12	0.1		0.374	0.378		
				0.093 -0.095	0.093 -0.092		
V <sub>t_lin</sub>	10	10	V	0.207	0.220	V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
				0.029 -0.029	0.028 -0.028		
	0.6	0.1		0.417	0.439		
				0.064 -0.066	0.066 -0.064		
	0.12	0.1		0.339	0.410		
				0.104 -0.106	0.102 -0.099		
V <sub>t_sat</sub>	10	10	V	0.194	0.194	V <sub>g</sub> @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
	0.6	0.1		0.333	0.340		
	0.12	0.1		0.281	0.332		
DIBL	0.6	0.1	V	0.084	-0.099	V <sub>b</sub> =0, V <sub>t_lin</sub> -V <sub>t_sat</sub>	
Id_lin	0.6	0.1	uA/um	96.4	24.6	Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
	0.12	0.1		91.2	26.1		
Id_sat	0.6	0.1	uA/um	530	215	Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
				-14.8% 14.6%	-18.2% 17.6%		
	0.12	0.1		517	222		
				-32.7% 32.8%	-26.6% 29.5%		
Ioff	0.6	0.1	pA/um	300	236	Id @V <sub>g</sub> =0, V <sub>d</sub> =1.0V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
				0.129 8.101	0.100 10.707		
Sub V <sub>t</sub> slope	0.6	0.1	mV/dec	103.94	105.16	Slope @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0, V <sub>g1</sub> =V <sub>t_sat</sub> -0.05, V <sub>g2</sub> =V <sub>t_sat</sub> -0.06	
Ig_inv	10	10	nA/um <sup>2</sup>	0.1480	0.0115	Ig @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>s</sub> =V <sub>b</sub> =0	
Body effect	0.6	0.1	V	0.077	0.089	$\Delta V_{t\_sat}$ @V <sub>b</sub> =-V <sub>dd</sub> /2 and V <sub>b</sub> =0	
Isub	0.6	0.1	nA/um	1.432E+00	2.602E-03	I <sub>bmax</sub> @V <sub>s</sub> =V <sub>b</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , sweep V <sub>g</sub>	
Covl	0.6	0.1	fF/um	2.68E-01	2.24E-01	C <sub>gd</sub> @V <sub>g</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
Cj			fF/um <sup>2</sup>	0.981	1.09	V <sub>rev</sub> =0V	
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.1	ps/gate	12.76		RO_Td(ring oscillator delay time) @ V=V <sub>dd</sub> (Fan_out=1)	
				2.37	-1.81		

## 13.4.2 1.2V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V high V<sub>t</sub> MOS in CLN90LP process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			um	-0.02±0.005	-0.02±0.005		
$\Delta W(x_w +/- dx_w)$			um	0.01±0.008	0.01±0.008		
Electrical_Tox			$\text{\AA}$	28.3±0.670	30±0.670		
Vt_gm	10	10	V	0.400	0.432	Vg @Vd=0.05V, Vs=Vb=0	
				0.026	-0.026		
	0.6	0.1		0.589	0.517		
				0.060	-0.063		
	0.12	0.1		0.463	0.453		
				0.090	-0.090		
Vt_lin	10	10	V	0.336	0.443	Vg @Vd=0.05V, Vs=Vb=0	
				0.028	-0.027		
	0.6	0.1		0.521	0.555		
				0.067	-0.071		
	0.12	0.1		0.412	0.485		
				0.101	-0.100		
Vt_sat	10	10	V	0.324	0.432	Vg @Vd=Vdd, Vs=Vb=0	
	0.6	0.1		0.437	0.479		
	0.12	0.1		0.345	0.422		
DIBL	0.6	0.1	V	0.083964	-0.076049	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.6	0.1	uA/um	74.99	20.087	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.12	0.1		77.86	21.609		
Id_sat	0.6	0.1	uA/um	399	153	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-18.1%	18.6%		
	0.12	0.1		428	174		
				-26.1%	27.4%		
loff	0.6	0.1	pA/um	16.1	6.8	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.121	11.43		
Sub Vt slope	0.6	0.1	mV/dec	116	106	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um2	0.1480	0.0115	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.6	0.1	V	0.105	0.128	$\Delta Vt_{sat} @Vb=-Vdd/2$ and $Vb=0$	
Isub	0.6	0.1	nA/um	2.09E-01	5.98E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.6	0.1	fF/um	2.54E-01	2.05E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	1.057	1.124	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp=5/3.5	0.1	ps/gate	18.33	-2.850	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	

### 13.4.3 1.2V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V low V<sub>t</sub> MOS in CLN90LP process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_1 +/- dx_1)$			um	-0.026±0.005	-0.026±0.005		
$\Delta W(xw +/- dxw)$			um	0.01±0.008	0.01±0.008		
Electrical_Tox			$\text{\AA}$	28.3±0.670	30±0.670		
Vt_gm	10	10	V	0.256	0.199	Vg @Vd=0.05V, Vs=Vb=0	
				0.027 -0.027	0.027 -0.027		
	0.6	0.1		0.475	0.392		
				0.066 -0.065	0.060 -0.061		
	0.12	0.1		0.376	0.368		
				0.094 -0.100	0.091 -0.089		
Vt_lin	10	10	V	0.207	0.216	Vg @Vd=0.05V, Vs=Vb=0	
				0.029 -0.029	0.028 -0.028		
	0.6	0.1		0.412	0.421		
				0.078 -0.075	0.068 -0.072		
	0.12	0.1		0.332	0.402		
				0.112 -0.115	0.103 -0.103		
Vt_sat	10	10	V	0.196	0.191	Vg @Vd=Vdd, Vs=Vb=0	
	0.6	0.1		0.302	0.310		
	0.12	0.1		0.259	0.319		
DIBL	0.6	0.1	V	0.10992	-0.11046	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.6	0.1	uA/um	102.82	25.64	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.12	0.1		92.583	25.128		
Id_sat	0.6	0.1	uA/um	570	240	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-17.2% 17.2%	-20.3% 20.1%		
	0.12	0.1		558	230		
				-26.1% 26.2%	-30.3% 33.7%		
Ioff	0.6	0.1	pA/um	575	806	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.050 20.095	0.106 15.206		
Sub Vt slope	0.6	0.1	mV/dec	108	111	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um <sup>2</sup>	0.1480	0.0115	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.6	0.1	V	0.069	0.080	$\Delta V_t$ _sat @Vb=-Vdd/2 and Vb=0	
Isub	0.6	0.1	nA/um	1.47E+00	2.69E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.6	0.1	fF/um	2.68E-01	2.23E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.981	1.09	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.1	ps/gate	11.30		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				2.714	-1.829		

## 13.4.4 1.2V Ultra Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Ultra Low V<sub>t</sub> MOS in CLN90LP process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_1 +/- dx_1)$			um	-0.026±0.005	-0.026±0.005		
$\Delta W(x_w +/- dx_w)$			um	0.01±0.008	0.01±0.008		
Electrical_Tox			$\text{\AA}$	28.3±0.670	30±0.670		
Vt_gm	10	10	V	0.248	0.187	Vg @Vd=0.05V, Vs=Vb=0	
				0.026	-0.026		
	0.6	0.1		0.401	0.343		
				0.066	-0.065		
	0.12	0.1		0.311	0.325		
				0.094	-0.100		
Vt_lin	10	10	V	0.194	0.202	Vg @Vd=0.05V, Vs=Vb=0	
				0.029	-0.028		
	0.6	0.1		0.334	0.369		
				0.079	-0.075		
	0.12	0.1		0.267	0.360		
				0.115	-0.115		
Vt_sat	10	10	V	0.183	0.184	Vg @Vd=Vdd, Vs=Vb=0	
	0.6	0.1		0.222	0.233		
	0.12	0.1		0.173	0.264		
DIBL	0.6	0.1	V	0.1120	-0.1364	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.6	0.1	uA/um	108.5	27.9	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.12	0.1		100.6	27.9		
Id_sat	0.6	0.1	uA/um	654	274	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-17.0% 17.0%	-20.4% 20.5%		
	0.12	0.1		649	268		
				-26.5% 26.2%	-31.1% 36.2%		
Ioff	0.6	0.1	pA/um	7906	5277	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
Sub Vt slope	0.6	0.1	mV/dec	111	106	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
lg_inv	10	10	nA/um <sup>2</sup>	0.138	0.013	lg @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.6	0.1	V	0.053	0.060	$\Delta V_{t\_sat}$ @Vb=-Vdd/2 and Vb=0	
Isub	0.6	0.1	nA/um	2.388E+00	3.796E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.6	0.1	fF/um	2.76E-01	2.35E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.9587	1.089	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp=5/3.5	0.1	ps/gate	8.86	-1.32	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	

## 13.4.5 2.5V Standard V<sub>t</sub> MOS

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_1 +/- dx_1)$			um	-0.015±0.01	-0.015±0.01		
$\Delta W(x_w +/- dx_w)$			um	0±0.012	0±0.012		
Electrical_Tox			$\text{\AA}$	55.4±3.000	58.2±3.000		
Vt_gm	10	10	V	0.512	0.615	Vg @Vd=0.05V, Vs=Vb=0	
				0.031 -0.031	0.031 -0.031		
	10	0.28		0.579	0.512		
				0.050 -0.050	0.050 -0.051		
	0.4	0.28		0.506	0.505		
				0.075 -0.075	0.080 -0.081		
Vt_lin	10	10		0.461	0.651	Vg @Vd=0.05V, Vs=Vb=0	
				0.032 -0.032	0.034 -0.034		
	10	0.28		0.528	0.528		
				0.053 -0.053	0.057 -0.058		
	0.4	0.28		0.463	0.545		
				0.080 -0.081	0.088 -0.088		
Vt_sat	10	10	V	0.451	0.637	Vg @Vd=Vdd, Vs=Vb=0	
				0.442	0.463		
	0.4	0.28		0.390	0.486		
DIBL	10	0.28	V	0.086665	-0.065344	Vb=0, Vt_lin-Vt_sat	
Id_lin	10	0.28	uA/um	48.6	16.2	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				45.5	13.8		
Id_sat	10	0.28	uA/um	580	289	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-7.6% 8.0%	-8.4% 7.9%		
	0.4	0.28		566	253		
				-13.2% 14.0%	-13.2% 13.1%		
loff	10	0.28	pA/um	1.410	3.540	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.212 5.299	0.269 4.061		
Sub Vt slope	10	0.28	mV/dec	101	106	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um <sup>2</sup>	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	10	0.28	V	0.160	0.293	$\Delta V_t$ _sat @Vb=-Vdd/2 and Vb=0	
Isub	10	0.28	nA/um	2.071E+02	1.149E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	10	0.28	fF/um	1.97E-01	2.10E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.08	1.08	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 5/3.5	0.28	ps/gate	27.19		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.96	-1.66		

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN90LP process.

## 13.4.6 3.3V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 3.3V Standard V<sub>t</sub> MOS in CLN90LP process.

	W ( $\mu$ m)	L ( $\mu$ m)	Unit	NMOS	PMOS	Definition	
$\Delta L$ (x1 +/- dx1)			um	-0.015±0.012	-0.015±0.012		
$\Delta W$ (xw+/- dxw)			um	0±0.012	0±0.012		
Electrical_Tox			$\text{\AA}$	72±3.000	75±3.000		
Vt_gm	10	10	V	0.595	0.683	Vg @Vd=0.05V, Vs=Vb=0	
				0.023   -0.023	0.034   -0.034		
	10	0.38		0.680	0.626		
				0.060   -0.060	0.050   -0.050		
	0.4	0.38		0.616	0.620		
				0.070   -0.070	0.060   -0.060		
Vt_lin	10	10	V	0.542	0.736	Vg @Vd=0.05V, Vs=Vb=0	
				0.024   -0.024	0.037   -0.037		
	10	0.38		0.633	0.663		
				0.063   -0.062	0.055   -0.055		
	0.4	0.38		0.564	0.671		
				0.076   -0.074	0.067   -0.067		
Vt_sat	10	10	V	0.527	0.719	Vg @Vd=Vdd, Vs=Vb=0	
				0.559	0.613		
	0.4	0.38		0.500	0.615		
DIBL	10	0.38	V	0.0734	-0.0496	Vb=0, Vt_lin-Vt_sat	
Id_lin	10	0.38	uA/um	36.14	12.38	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				34.43	10.87		
Id_sat	10	0.38	uA/um	589	286	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-5.9%   6.0%	-7.9%   7.9%		
	0.4	0.38		580	264		
				-8.2%   9.6%	-9.5%   9.6%		
Ioff	10	0.38	pA/um	0.10953	0.12622	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.276   4.333	0.558   2.285		
Sub Vt slope	10	0.38	mV/dec	96	104	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	10	10	nA/um2	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	10	0.38	V	0.255	0.309	$\Delta Vt_{sat}$ @Vb=-Vdd/2 and Vb=0	
Isub	10	0.38	nA/um	8.591E+02	1.113E+01	lbmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	10	0.38	fF/um	1.65E-01	1.73E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	0.962	1.04	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.5/5	0.38	ps/gate	34.4		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				2.15	-1.87		

## 13.4.7 1.2V Native NMOS

The following table summarizes the key parameters for 1.2V native NMOS in CLN90LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>		
$\Delta L (x_1 +/- dx_1)$			um	$-0.026 \pm 0.005$				
$\Delta W(x_w +/- dx_w)$			um	$0.005 \pm 0.008$				
Electrical_Tox			Å	$28.3 \pm 0.670$				
Vt_gm	10	10	V	0.051		$V_g @ V_d = 0.05V, V_s = V_b = 0$		
				0.040	-0.040			
				0.194				
	10	0.33		0.055	-0.051			
				0.261				
				0.067	-0.064			
Vt_lin	10	10	V	0.009		$V_g @ V_d = 0.05V, V_s = V_b = 0$		
				0.042	-0.042			
				0.148				
	10	0.33		0.057	-0.053			
				0.203				
				0.074	-0.070			
Vt_sat	10	10	V	-0.029		$V_g @ V_d = V_{dd}, V_s = V_b = 0$		
				0.092				
				0.149				
DIBL	10	0.33	V	0.056		$V_b = 0, V_t_{lin} - V_t_{sat}$		
Id_lin	10	0.33	uA/um	53.8		$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$		
				68.4				
Id_sat	10	0.33	uA/um	478		$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$		
				-11.8%	11.9%			
	0.5	0.2		522				
				-15.4%	16.9%			
Ioff	10	0.33	pA/um	22182		$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$		
				0.177	4.931			
Sub Vt slope	10	0.33	mV/dec	78		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$		
Ig_inv	10	10	nA/um <sup>2</sup>	0.116		$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$		
Body effect	10	0.33	V	0.017		$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$		
Isub	10	0.33	nA/um	0.265		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$		
Covl	10	0.2	fF/um	0.355		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$		
Cj			fF/um <sup>2</sup>	0.139		$V_{rev} = 0V$		

## 13.4.8 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN90LP process.

	<b>W ( <math>\mu</math> m)</b>	<b>L ( <math>\mu</math> m)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>		
$\Delta L$ (x <sub>l</sub> +/- dx <sub>l</sub> )			um	$-0.04 \pm 0.01$				
$\Delta W$ (x <sub>w</sub> +/- dx <sub>w</sub> )			um	$0 \pm 0.012$				
Electrical_Tox			$\text{\AA}$	$55.4 \pm 3.000$				
Vt_gm	10	10	V	-0.141		Vg @ Vd=0.05V, Vs=Vb=0		
				0.058	-0.058			
	10	1.2		-0.167				
				0.086	-0.087			
	0.5	1.2		-0.145				
				0.087	-0.087			
Vt_lin	10	10	V	-0.157		Vg @ Vd=0.05V, Vs=Vb=0		
				0.060	-0.060			
	10	1.2		-0.189				
				0.089	-0.089			
	0.5	1.2		-0.159				
				0.090	-0.091			
Vt_sat	10	10	V	-0.166		Vg @ Vd=Vdd, Vs=Vb=0		
				-0.260				
	0.5	1.2		-0.192				
DIBL	10	1.2	V	0.071485		$V_b=0$ , $V_t_{lin}-V_t_{sat}$		
Id_lin	10	1.2	uA/um	20.0		$Id @ V_g=V_{dd}, V_d=0.05V, V_s=V_b=0$		
				18.5				
Id_sat	10	1.2	uA/um	451		$Id @ V_g=V_{dd}, V_d=V_{dd}, V_s=V_b=0$		
				-10.4%	11.7%			
	0.5	1.2		427				
				-13.0%	14.9%			
loff	10	1.2	pA/um	8.04E+06		$Id @ V_g=0, V_d=1.0V_{dd}, V_s=V_b=0$		
				0.402	1.952			
Sub Vt slope	10	1.2	mV/dec	68		Slope @ $V_d=V_{dd}, V_s=V_b=0, V_{g1}=V_{t\_sat}-0.05, V_{g2}=V_{t\_sat}-0.06$		
Ig_inv	10	10	nA/um2	0		$Ig @ V_g=V_{dd}, V_d=V_s=V_b=0$		
Body effect	10	1.2	V	0.041		$\Delta V_{t\_sat} @ V_b=-V_{dd}/2$ and $V_b=0$		
Isub	10	1.2	nA/um	1.57		$I_{bmax} @ V_s=V_b=0, V_d=V_{dd}$ , sweep $V_g$		
Covl	10	1.2	fF/um	0.186		$C_{gd} @ V_g=0, V_d=V_{dd}, V_s=V_b=0$		
Cj			fF/um2	0.124		$V_{rev}=0V$		

## 13.4.9 3.3V Native NMOS

The following table summarizes the key parameters for 3.3V native NMOS in CLN90LP process.

	<b>W (<math>\mu\text{m}</math>)</b>	<b>L (<math>\mu\text{m}</math>)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>	
$\Delta L (x_1 +/- dx_1)$			um	$-0.045 \pm 0.012$			
$\Delta W(x_w +/- dx_w)$			um	$0 \pm 0.012$			
Electrical_Tox			$\text{\AA}$	$72 \pm 3.000$			
Vt_gm	10	10	V	-0.145	Vg @ Vd=0.05V, Vs=Vb=0		
				0.049   -0.049			
				-0.173			
	10	1.2		0.076   -0.077			
				-0.140			
				0.077   -0.077			
Vt_lin	10	10	V	-0.164	Vg @ Vd=0.05V, Vs=Vb=0		
				0.051   -0.051			
				-0.189			
	10	1.2		0.079   -0.080			
				-0.145			
				0.081   -0.081			
Vt_sat	10	10	V	-0.172	Vg @ Vd=Vdd, Vs=Vb=0		
				-0.307			
				-0.180			
DIBL	10	1.2	V	0.11796	Vb=0, Vt_lin-Vt_sat		
Id_lin	10	1.2	uA/um	20.3	Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0		
				20.0			
Id_sat	10	1.2	uA/um	545	Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0		
				-8.6%   9.3%			
	0.5	1.2		509			
				-11.3%   12.7%			
loff	10	1.2	pA/um	1.04E+07	Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0		
				0.525   1.668			
Sub Vt slope	10	1.2	mV/dec	71	Slope @ Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06		
Ig_inv	10	10	nA/um <sup>2</sup>	0	Ig @ Vg=Vdd, Vd=Vs=Vb=0		
Body effect	10	1.2	V	0.053	$\Delta V_{t\_sat}$ @ Vb=-Vdd/2 and Vb=0		
Isub	10	1.2	nA/um	24.03	Ibmax @ Vs=Vb=0, Vd=Vdd, sweep Vg		
Covl	10	1.2	fF/um	0.179	Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0		
Cj			fF/um <sup>2</sup>	0.139	Vrev=0V		

## 13.5 Key Parameters of MOS Transistors in CLN85G

### 13.5.1 1.0V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V Standard V<sub>t</sub> MOS in CLN85G process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			um	-0.029±0.005		-0.029±0.005		
ΔW(xw+/-dxw)			um	0.01±0.008		0.01±0.008		
Electrical_Tox			Å	23.3±0.600		25±0.600		
Vt_gm	9.4	9.4	V	0.221	0.174		Vg @Vd=0.05V, Vs=Vb=0	
	0.564	0.094		0.027   -0.027	0.025   -0.025			
	0.1128	0.094		0.327	0.344			
	9.4	9.4		0.054   -0.054	0.052   -0.053			
	0.564	0.094		0.257	0.328			
	0.1128	0.094		0.078   -0.080	0.064   -0.064			
Vt_lin	9.4	9.4	V	0.161	0.182		Vg @Vd=0.05V, Vs=Vb=0	
	0.564	0.094		0.028   -0.028	0.025   -0.023			
	0.1128	0.094		0.267	0.355			
	9.4	9.4		0.059   -0.061	0.061   -0.061			
	0.564	0.094		0.212	0.348			
	0.1128	0.094		0.088   -0.091	0.073   -0.071			
Vt_sat	9.4	9.4	V	0.156	0.161		Vg @Vd=Vdd, Vs=Vb=0	
	0.564	0.094		0.184	0.251			
	0.1128	0.094		0.154	0.280			
DIBL	0.564	0.094	V	0.082669	-0.1044		Vb=0, Vt_lin-Vt_sat	
Id_lin	0.564	0.094	uA/um	119.47	30.487		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.1128	0.094		116.58	32.534			
Id_sat	0.564	0.094	uA/um	635.18	242.41		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
	0.1128	0.094		-15.4%   15.5%	-17.8%   19.9%			
	0.564	0.094		664.1	241.7			
	0.1128	0.094		-24.3%   27.6%	-25.5%   24.4%			
loff	0.564	0.094	pA/um	12736	4897.4		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
	0.1128	0.094		0.163   7.242	0.124   7.010			
Sub Vt slope	0.564	0.094	mV/dec	95.692	118.28		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	24.755	7.7621		Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.564	0.094	V	0.052	0.074		Δ Vt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.564	0.094	nA/um	1.322E-01	7.314E-04		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.564	0.094	fF/um	2.89E-01	2.39E-01		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.023	1.08		Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	9.66478			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.83932	-1.53805			

## 13.5.2 1.0V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V high V<sub>t</sub> MOS in CLN85G process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			um	$-0.029 \pm 0.005$		$-0.029 \pm 0.005$		
$\Delta W(x_w +/- dx_w)$			um	$0.01 \pm 0.008$		$0.01 \pm 0.008$		
Electrical_Tox			$\text{\AA}$	$23.3 \pm 0.600$		$25 \pm 0.600$		
V <sub>t_gm</sub>	9.4	9.4	V	0.339		0.320	Vg @ Vd=0.05V, Vs=Vb=0	
				0.026	-0.026	0.029		
	0.564	0.094		0.432		0.403		
				0.055	-0.056	0.047		
	0.1128	0.094		0.351		0.391		
				0.085	-0.083	0.058		
V <sub>t_lin</sub>	9.4	9.4		0.272		0.337	Vg @ Vd=0.05V, Vs=Vb=0	
				0.026	-0.024	0.029		
	0.564	0.094		0.369		0.423		
				0.059	-0.059	0.055		
	0.1128	0.094		0.305		0.419		
				0.094	-0.091	0.068		
V <sub>t_sat</sub>	9.4	9.4	V	0.267		0.326	Vg @ Vd=Vdd, Vs=Vb=0	
				0.288		0.320		
	0.564	0.094		0.254		0.351		
DIBL	0.564	0.094	V	0.080557		-0.10253	Vb=0, V <sub>t_lin</sub> -V <sub>t_sat</sub>	
Id <sub>_lin</sub>	0.564	0.094	uA/um	102.94		26.319	Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.1128	0.094		104.39		26.278		
Id <sub>_sat</sub>	0.564	0.094	uA/um	509.04		195.07	Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-17.0%	17.2%	-20.1%		
	0.1128	0.094		552.77		180.22		
				-24.4%	23.9%	-25.8%		
Ioff	0.564	0.094	pA/um	1057.9		744.67	Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.212	5.627	0.184		
Sub Vt slope	0.564	0.094	mV/dec	96.475		112.93	Slope @ Vd=Vdd, Vs=Vb=0, Vg1=V <sub>t_sat</sub> -0.05, Vg2=V <sub>t_sat</sub> -0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	24.798		7.7753	Ig @ Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.564	0.094	V	0.067		0.083	$\Delta V_{t\_sat}$ @ Vb=-Vdd/2 and Vb=0	
Isub	0.564	0.094	nA/um	1.335E-01		1.806E-03	Ibmax @ Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.564	0.094	fF/um	2.78E-01		2.28E-01	Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.177		1.11	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	12.7915			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				3.0863		-2.104		

### 13.5.3 1.0V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V low V<sub>t</sub> MOS in CLN85G process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			um	-0.029±0.005		-0.029±0.005		
ΔW(xw +/- dxw)			um	0.01±0.008		0.01±0.008		
Electrical_Tox			Å	23.3±0.600		25±0.600		
Vt_gm	9.4	9.4	V	0.216		0.172	Vg @Vd=0.05V, Vs=Vb=0	
				0.026	-0.026	0.026		
	0.564	0.094		0.257		0.285		
				0.056	-0.054	0.059		
	0.1128	0.094		0.191		0.284		
				0.081	-0.078	0.063		
Vt_lin	9.4	9.4	V	0.157		0.182	Vg @Vd=0.05V, Vs=Vb=0	
				0.027	-0.027	0.029		
	0.564	0.094		0.203		0.298		
				0.061	-0.060	0.069		
	0.1128	0.094		0.148		0.304		
				0.091	-0.088	0.073		
Vt_sat	9.4	9.4	V	0.152		0.167	Vg @Vd=Vdd, Vs=Vb=0	
	0.564	0.094		0.112		0.181		
	0.1128	0.094		0.093		0.228		
DIBL	0.564	0.094	V	0.090996		-0.1169	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.564	0.094	uA/um	133.37		33.832	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.1128	0.094		131.18		35.853		
Id_sat	0.564	0.094	uA/um	743.75		287.39	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-15.8%	16.5%	-21.0%		
	0.1128	0.094		785.09		281.57		
				-23.4%	26.3%	-24.9%		
loff	0.564	0.094	pA/um	85943		27291	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.156	6.418	0.117		
Sub Vt slope	0.564	0.094	mV/dec	89.583		109.7	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat- 0.05, Vg2=Vt_sat-0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	25.276		7.7727	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.564	0.094	V	0.048		0.057	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.564	0.094	nA/um	1.465E+00		4.814E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.564	0.094	fF/um	2.88E-01		2.49E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.004		1.082	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	7.71217			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.49761		-1.11017		

### 13.5.4 1.8V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.8V Standard V<sub>t</sub> MOS in CLN85G process.

	W ( $\mu$ m)	L ( $\mu$ m)	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			um	-0.043±0.008	-0.043±0.008		
$\Delta W(x_w +/- dx_w)$			um	0±0.012	0±0.012		
Electrical_Tox			$\text{\AA}$	34.5±1.333	37±1.333		
V <sub>t_gm</sub>	9.4	9.4	V	0.355	0.395	Vg @ Vd=0.05V, Vs=Vb=0	
				0.051 -0.051	0.052 -0.051		
	9.4	0.188		0.447	0.443		
				0.060 -0.061	0.063 -0.059		
	0.376	0.188		0.453	0.457		
				0.074 -0.069	0.082 -0.072		
V <sub>t_lin</sub>	9.4	9.4		0.294	0.412	Vg @ Vd=0.05V, Vs=Vb=0	
				0.053 -0.053	0.054 -0.054		
	9.4	0.188		0.388	0.460		
				0.067 -0.068	0.068 -0.064		
	0.376	0.188		0.387	0.486		
				0.083 -0.077	0.090 -0.079		
V <sub>t_sat</sub>	9.4	9.4	V	0.286	0.400	Vg @ Vd=Vdd, Vs=Vb=0	
				0.335	0.396		
	0.376	0.188		0.328	0.425		
DIBL	9.4	0.188	V	0.053352	-0.063366	Vb=0, V <sub>t_lin</sub> -V <sub>t_sat</sub>	
Id <sub>_lin</sub>	9.4	0.188	uA/um	86.59	24	Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.376	0.188		82.281	20.17		
Id <sub>_sat</sub>	9.4	0.188	uA/um	675.3	309.36	Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-14.0% 16.1%	-12.9% 14.2%		
	0.376	0.188		667.84	262.29		
				-17.7% 19.5%	-18.1% 19.7%		
Ioff	9.4	0.188	pA/um	61.106	15.27	Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.151 7.820	0.171 6.466		
Sub V <sub>t</sub> slope	9.4	0.188	mV/dec	87.454	96.166	Slope @ Vd=Vdd, Vs=Vb=0, Vg1=V <sub>t_sat</sub> -0.05, Vg2=V <sub>t_sat</sub> -0.06	
Ig <sub>_inv</sub>	9.4	9.4	nA/um <sup>2</sup>	0	0	Ig @ Vg=Vdd, Vd=Vs=Vb=0	
Body effect	9.4	0.188	V	0.143	0.162	$\Delta V_{t\_sat}$ @ Vb=-Vdd/2 and Vb=0	
I <sub>sub</sub>	9.4	0.188	nA/um	8.185E+00	1.663E+00	I <sub>bmax</sub> @ Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	9.4	0.188	fF/um	2.66E-01	2.38E-01	C <sub>gd</sub> @ Vg=0, Vd=Vdd, Vs=Vb=0	
C <sub>j</sub>			fF/um <sup>2</sup>	0.981	1.041	V <sub>rev</sub> =0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.188	ps/gate	16.4563		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				2.6211	-2.1845		

## 13.5.5 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN85G process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
Δ L (xL +/- dxL)			um	0.0018±0.01		0.0018±0.01		
Δ W(xw +/- dxw)			um	0±0.012		0±0.012		
Electrical_Tox			Å	55.4±3.000		58.2±3.000		
Vt_gm	9.4	9.4	V	0.513		0.594	Vg @Vd=0.05V, Vs=Vb=0	
				0.031	-0.031	0.031		
	9.4	0.2632		0.582		0.505		
				0.050	-0.050	0.048		
	0.376	0.2632		0.493		0.493		
				0.077	-0.077	0.082		
Vt_lin	9.4	9.4	V	0.458		0.630	Vg @Vd=0.05V, Vs=Vb=0	
				0.033	-0.033	0.034		
	9.4	0.2632		0.528		0.525		
				0.054	-0.054	0.053		
	0.376	0.2632		0.440		0.524		
				0.083	-0.083	0.089		
Vt_sat	9.4	9.4	V	0.448		0.616	Vg @Vd=Vdd, Vs=Vb=0	
				0.449		0.466		
	0.376	0.2632		0.371		0.461		
DIBL	9.4	0.2632	V	0.079038		-0.058736	Vb=0, Vt_lin-Vt_sat	
Id_lin	9.4	0.2632	uA/um	50.711		16.174	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				51.064		15.274		
Id_sat	9.4	0.2632	uA/um	582.19		291.81	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-8.3%	8.1%	-8.1%		
	0.376	0.2632		613.55		286.07		
				-14.2%	14.1%	-12.9%		
loff	9.4	0.2632	pA/um	1.3584		2.0488	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.143	6.029	0.220		
Sub Vt slope	9.4	0.2632	mV/dec	96.732		101.71	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	9.4	0.2632	V	0.168		0.280	Δ Vt_sat @Vb=-Vdd/2 and Vb=0	
Isub	9.4	0.2632	nA/um	2.319E+02		1.146E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	9.4	0.2632	fF/um	1.97E-01		2.10E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.08		1.041	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.2632	ps/gate	26.7767		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)		
				1.9743		-1.6655		

## 13.5.6 3.3V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 3.3V Standard V<sub>t</sub> MOS in CLN85G process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		PMOS	Definition	
$\Delta L(xl +/- dxl)$			um	$0.0078 \pm 0.012$		$0.0078 \pm 0.012$		
$\Delta W(xw +/- dxw)$			um	$0 \pm 0.012$		$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$72 \pm 3.000$		$75 \pm 3.000$		
V <sub>t_gm</sub>	9.4	9.4	V	0.593		0.675	V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
				0.023	-0.023	0.034		
	9.4	0.3572		0.686		0.614		
				0.060	-0.059	0.050		
	0.376	0.3572		0.593		0.616		
				0.071	-0.070	0.061		
V <sub>t_lin</sub>	9.4	9.4		0.541		0.722	V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
				0.024	-0.024	0.037		
	9.4	0.3572		0.633		0.654		
				0.062	-0.062	0.055		
	0.376	0.3572		0.538		0.666		
				0.077	-0.076	0.068		
V <sub>t_sat</sub>	9.4	9.4	V	0.526		0.705	V <sub>g</sub> @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
	9.4	0.3572		0.558		0.602		
	0.376	0.3572		0.474		0.611		
DIBL	9.4	0.3572	V	0.075		-0.052	V <sub>b</sub> =0, V <sub>t_lin</sub> -V <sub>t_sat</sub>	
Id_lin	9.4	0.3572	uA/um	37.5		12.2	Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
	0.376	0.3572		36.6		10.8		
Id_sat	9.4	0.3572	uA/um	591		287	Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
				-5.9%	5.9%	-8.0%		
	0.376	0.3572		596		264		
				-7.9%	9.4%	-10.7%		
Ioff	9.4	0.3572	pA/um	0.161		0.157	Id @V <sub>g</sub> =0, V <sub>d</sub> =1.0V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
				0.284	1.162	0.509		
Sub Vt slope	9.4	0.3572	mV/dec	98.582		104.4	Slope @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0, V <sub>g1</sub> =V <sub>t_sat</sub> -0.05, V <sub>g2</sub> =V <sub>t_sat</sub> -0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		0	Ig @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>s</sub> =V <sub>b</sub> =0	
Body effect	9.4	0.3572	V	0.284		0.323	$\Delta V_{t\_sat}$ @V <sub>b</sub> =-V <sub>dd</sub> /2 and V <sub>b</sub> =0	
Isub	9.4	0.3572	nA/um	9.66E+02		9.96	Ibmax @V <sub>s</sub> =V <sub>b</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , sweep V <sub>g</sub>	
Covl	9.4	0.3572	fF/um	1.65E-01		1.73E-01	Cgd @V <sub>g</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
C <sub>j</sub>			fF/um <sup>2</sup>	0.962		1.04	V <sub>rev</sub> =0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.3572	ps/gate	34.0241			RO_Td(ring oscillator delay time) @ V=V <sub>dd</sub> (Fan_out=1)	
				2.153		-1.9008		

### 13.5.7 1.0V Native NMOS

The following table summarizes the key parameters for 1.0V native NMOS in CLN85G process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>
$\Delta L (x_l +/- dx_l)$			um	$-0.049 \pm 0.005$		
$\Delta W(x_w +/- dx_w)$			um	$0.01 \pm 0.008$		
Electrical_Tox			Å	$23.3 \pm 0.600$		
Vt_gm	9.4	9.4	V	-0.029		$V_g @ V_d = 0.05V, V_s = V_b = 0$
	9.4	0.188		0.035	-0.035	
	0.47	0.188		0.142		
				0.055	-0.060	
				0.148		
				0.064	-0.068	
Vt_lin	9.4	9.4	V	-0.080		$V_g @ V_d = 0.05V, V_s = V_b = 0$
	9.4	0.188		0.036	-0.037	
	0.47	0.188		0.085		
				0.059	-0.064	
				0.098		
				0.068	-0.072	
Vt_sat	9.4	9.4	V	-0.119		$V_g @ V_d = V_{dd}, V_s = V_b = 0$
	9.4	0.188		0.023		
	0.47	0.188		0.043		
DIBL	9.4	0.188	V	0.061225		$V_b = 0, V_t_{lin} - V_t_{sat}$
Id_lin	9.4	0.188	uA/um	91.613		$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$
	0.47	0.188		85.099		
Id_sat	9.4	0.188	uA/um	624.1		$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$
	0.47	0.188		-12.4%   14.1%		
				590.43		
				-15.5%   17.6%		
Ioff	9.4	0.188	pA/um	376830		$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$
Sub Vt slope	9.4	0.188	mV/dec	76.466		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	22.557		$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$
Body effect	9.4	0.188	V	0.009		$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$
Isub	9.4	0.188	nA/um	0.005		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$
Covl	9.4	0.188	fF/um	2.75E-01		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$
Cj			fF/um <sup>2</sup>	0.144		$V_{rev} = 0V$

## 13.5.8 1.8V Native NMOS

The following table summarizes the key parameters for 1.8V native NMOS in CLN85G process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		Definition
$\Delta L (x_l +/- dx_l)$			um	$-0.0232 \pm 0.008$		
$\Delta W(x_w +/- dx_w)$			um	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$34.5 \pm 1.333$		
Vt_gm	9.4	9.4	V	-0.043		Vg @ Vd=0.05V, Vs=Vb=0
	9.4	0.752		0.051	-0.051	
	0.47	0.752		0.054		
	9.4	9.4		0.071	-0.071	
	9.4	0.752		0.073		
	0.47	0.752		0.082	-0.082	
Vt_lin	9.4	9.4	V	-0.079		Vg @ Vd=0.05V, Vs=Vb=0
	9.4	0.752		0.052	-0.052	
	0.47	0.752		0.014		
	9.4	9.4		0.073	-0.073	
	9.4	0.752		0.038		
	0.47	0.752		0.086	-0.086	
Vt_sat	9.4	9.4	V	-0.115		Vg @ Vd=Vdd, Vs=Vb=0
	9.4	0.752		-0.040		
	0.47	0.752		-0.009		
DIBL	9.4	0.752	V	0.053556		$V_b=0, V_t_{lin}-V_t_{sat}$
Id_lin	9.4	0.752	uA/um	29.629		$Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0$
	0.47	0.752		26.31		
Id_sat	9.4	0.752	uA/um	476.96		$Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0$
	9.4	0.752		-10.4%	11.4%	
	0.47	0.752		428.33		
	0.47	0.752		-14.0%	15.7%	
loff	9.4	0.752	pA/um	391690		$Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0$
	9.4	0.752		0.140	5.752	
Sub Vt slope	9.4	0.752	mV/dec	79.773		Slope @ $Vd=Vdd, Vs=Vb=0, Vg1=Vt_{sat}-0.05, Vg2=Vt_{sat}-0.06$
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		$Ig @ Vg=Vdd, Vd=Vs=Vb=0$
Body effect	9.4	0.752	V	0.012		$\Delta Vt_{sat} @ Vb=-Vdd/2 \text{ and } Vb=0$
Isub	9.4	0.752	nA/um	0.301		$Ib_{max} @ Vs=Vb=0, Vd=Vdd, \text{sweep } Vg$
Covl	9.4	0.752	fF/um	2.84E-01		$Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0$
Cj			fF/um <sup>2</sup>	0.142		$V_{rev}=0V$

## 13.5.9 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN85G process.

	<b>W (<math>\mu\text{m}</math>)</b>	<b>L (<math>\mu\text{m}</math>)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>
$\Delta L (x_l +/- dx_l)$			um	$-0.0232 \pm 0.01$		
$\Delta W(x_w +/- dx_w)$			um	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$55.4 \pm 3.000$		
Vt_gm	9.4	9.4	V	-0.036		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
				0.059	-0.059	
	9.4	1.128		-0.057		
		1.128		0.086	-0.086	
	0.47	1.128		0.067		
		1.128		0.091	-0.091	
Vt_lin	9.4	9.4	V	-0.065		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
		1.128		0.062	-0.061	
	9.4	1.128		-0.088		
		1.128		0.090	-0.090	
	0.47	1.128		0.037		
		1.128		0.096	-0.096	
Vt_sat	9.4	9.4	V	-0.076		$V_g @ V_d = V_{dd}, V_s = V_b = 0$
	9.4	1.128		-0.162		
	0.47	1.128		-0.001		
DIBL	9.4	1.128	V	0.074161		$V_b = 0, V_t_{lin} - V_t_{sat}$
Id_lin	9.4	1.128	uA/um	18.159		$Id @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$
	0.47	1.128		16.054		
Id_sat	9.4	1.128	uA/um	403.02		$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$
		1.128		-11.3%	10.9%	
	0.47	1.128		349.95		
		1.128		-13.2%	14.7%	
loff	9.4	1.128	pA/um	2.19E+06		$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$
				0.223	2.785	
Sub Vt slope	9.4	1.128	mV/dec	87.308		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_{t\_sat} - 0.05, V_{g2} = V_{t\_sat} - 0.06$
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$
Body effect	9.4	1.128	V	0.046		$\Delta V_{t\_sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$
Isub	9.4	1.128	nA/um	1.062		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$
Covl	9.4	1.128	fF/um	1.85E-01		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$
Cj			fF/um <sup>2</sup>	0.1419		$V_{rev} = 0\text{V}$

## 13.5.10 3.3V Native NMOS

The following table summarizes the key parameters for 3.3V native NMOS in CLN85G process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			um	$-0.0222 \pm 0.012$			
$\Delta W(x_w +/- dx_w)$			um	$0 \pm 0.012$			
Electrical_Tox			Å	$72 \pm 3.000$			
Vt_gm	9.4	9.4	V	0.014		$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.050	-0.050		
	9.4	1.128		$-0.002$			
				0.078	-0.079		
	0.47	1.128		$0.106$			
				0.078	-0.079		
Vt_lin	9.4	9.4	V	$-0.005$		$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.053	-0.053		
	9.4	1.128		$-0.026$			
				0.082	-0.082		
	0.47	1.128		$0.070$			
				0.084	-0.085		
Vt_sat	9.4	9.4	V	$-0.015$		$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	9.4	1.128		$-0.166$			
	0.47	1.128		$0.014$			
DIBL	9.4	1.128	V	$0.14074$		$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	9.4	1.128	uA/um	$17.904$		$I_d @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
	0.47	1.128		$16.102$			
Id_sat	9.4	1.128	uA/um	$480.55$		$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				-8.4%	8.8%		
	0.47	1.128		$423.65$			
				-11.6%	12.8%		
loff	9.4	1.128	pA/um	$1.97E+06$		$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
Sub Vt slope	9.4	1.128	mV/dec	$100.78$		Slope @ $V_d = V_{dd}, V_s = V_b = 0$ , $V_{g1} = V_{t\_sat} - 0.05, V_{g2} = V_{t\_sat} - 0.06$	
lg_inv	9.4	9.4	nA/um <sup>2</sup>	$0$		$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	9.4	1.128	V	$0.062$		$\Delta V_{t\_sat} @ V_b = -V_{dd}/2$ and $V_b = 0$	
Isub	9.4	1.128	nA/um	$16.435$		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}$ , sweep $V_g$	
Covl	9.4	1.128	fF/um	$1.79E-01$		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/um <sup>2</sup>	$0.137$		$V_{rev} = 0V$	

## 13.6 Key Parameters of MOS Transistors in CLN85LP

### 13.6.1 1.2V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Standard V<sub>t</sub> MOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>
$\Delta L (x_l +/- d_xl)$			um	-0.014±0.005	-0.014±0.005	
$\Delta W(x_w +/- d_xw)$			um	0.01±0.008	0.01±0.008	
Electrical_Tox			Å	28.3±0.670	30±0.670	
Vt_gm	9.4	9.4	V	0.261	0.195	Vg @Vd=0.05V, Vs=Vb=0
	0.564	0.094		0.027   -0.027	0.028   -0.028	
	0.1128	0.094		0.487	0.421	
	9.4	9.4		0.057   -0.058	0.059   -0.059	
	0.564	0.094		0.408	0.391	
	0.1128	0.094		0.091   -0.094	0.093   -0.092	
Vt_lin	9.4	9.4	V	0.210	0.212	Vg @Vd=0.05V, Vs=Vb=0
	0.564	0.094		0.029   -0.029	0.030   -0.029	
	0.1128	0.094		0.421	0.448	
	9.4	9.4		0.063   -0.066	0.066   -0.064	
	0.564	0.094		0.352	0.427	
	0.1128	0.094		0.102   -0.106	0.104   -0.100	
Vt_sat	9.4	9.4	V	0.198	0.185	Vg @Vd=Vdd, Vs=Vb=0
	0.564	0.094		0.331	0.339	
	0.1128	0.094		0.290	0.347	
DIBL	0.564	0.094	V	0.089194	-0.10875	Vb=0, Vt_lin-Vt_sat
Id_lin	0.564	0.094	uA/um	95.116	23.727	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.1128	0.094		97.025	23.697	
Id_sat	0.564	0.094	uA/um	531.19	215.93	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	0.1128	0.094		-15.2%   14.8%	-17.9%   18.2%	
	0.564	0.094		566.83	214.46	
	0.1128	0.094		-24.1%   27.4%	-26.7%   27.3%	
loff	0.564	0.094	pA/um	262.83	256.26	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
	0.564	0.094		0.118   8.926	0.080   12.941	
Sub Vt slope	0.564	0.094	mV/dec	108.7	115.3	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0.14766	0.011502	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	0.564	0.094	V	0.074	0.082	$\Delta V_{t\_sat}$ @Vb=-Vdd/2 and Vb=0
Isub	0.564	0.094	nA/um	1.419E+00	2.289E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	0.564	0.094	fF/um	2.69E-01	2.24E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um <sup>2</sup>	0.981	1.09	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	12.60	-1.73	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.37		

## 13.6.2 1.2V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V high V<sub>t</sub> MOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			um	-0.014±0.005		-0.014±0.005		
ΔW(xw +/- dxw)			um	0.01±0.008		0.01±0.008		
Electrical_Tox			Å	28.3±0.670		30±0.670		
Vt_gm	9.4	9.4	V	0.384		0.432	Vg @Vd=0.05V, Vs=Vb=0	
				0.026	-0.026	0.026		
				0.605		0.524		
	0.564	0.094		0.058	-0.064	0.057		
				0.504		0.498		
				0.089	-0.089	0.095		
Vt_lin	9.4	9.4	V	0.323		0.448	Vg @Vd=0.05V, Vs=Vb=0	
				0.027	-0.027	0.028		
				0.532		0.558		
	0.564	0.094		0.066	-0.072	0.065		
				0.455		0.540		
				0.101	-0.100	0.105		
Vt_sat	9.4	9.4	V	0.312		0.436	Vg @Vd=Vdd, Vs=Vb=0	
				0.439		0.469		
				0.391		0.475		
DIBL	0.564	0.094	V	0.092951		-0.089189	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.564	0.094	uA/um	76.273		19.669	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.1128	0.094		80.545		19.664		
Id_sat	0.564	0.094	uA/um	398.36		152.96	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-18.3%	19.0%	-19.4%		
	0.1128	0.094		446.45		151.95		
				-27.3%	27.6%	-26.7%		
loff	0.564	0.094	pA/um	14.686		7.165	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.182	8.642	0.152		
Sub Vt slope	0.564	0.094	mV/dec	105.46		110.57	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0.15958		0.011677	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.564	0.094	V	0.103		0.130	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.564	0.094	nA/um	2.044E-01		4.635E-02	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.564	0.094	fF/um	2.55E-01		2.06E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.987		1.09	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	18.18			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				3.63		-2.81		

### 13.6.3 1.2V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V low V<sub>t</sub> MOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			um	-0.02±0.005	-0.02±0.005		
ΔW(xw +/- dxw)			um	0.01±0.008	0.01±0.008		
Electrical_Tox			Å	28.3±0.670	30±0.670		
Vt_gm	9.4	9.4	V	0.254	0.197	Vg @Vd=0.05V, Vs=Vb=0	
				0.027 -0.027	0.027 -0.027		
	0.564	0.094		0.470	0.399		
				0.066 -0.065	0.061 -0.056		
	0.1128	0.094		0.395	0.381		
				0.096 -0.102	0.097 -0.095		
Vt_lin	9.4	9.4		0.203	0.213	Vg @Vd=0.05V, Vs=Vb=0	
				0.029 -0.029	0.028 -0.028		
	0.564	0.094		0.409	0.425		
				0.077 -0.074	0.069 -0.065		
	0.1128	0.094		0.343	0.411		
				0.112 -0.115	0.109 -0.110		
Vt_sat	9.4	9.4	V	0.192	0.185	Vg @Vd=Vdd, Vs=Vb=0	
				0.301	0.304		
	0.564	0.094		0.268	0.325		
DIBL	0.564	0.094	V	0.10873	-0.12092	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.564	0.094	uA/um	101.04	25.526	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.1128	0.094		101.56	26.731		
Id_sat	0.564	0.094	uA/um	569.5	239.8	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-16.9% 16.7%	-20.4% 20.3%		
	0.1128	0.094		611.97	237.72		
				-25.1% 24.1%	-31.4% 34.9%		
Ioff	0.564	0.094	pA/um	590.38	923.18	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
Sub Vt slope	0.564	0.094	mV/dec	0.051 19.198	0.080 19.023	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0.14676	0.011347	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.564	0.094	V	0.067	0.077	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.564	0.094	nA/um	1.416E+00	2.666E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.564	0.094	fF/um	2.69E-01	2.24E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.957	1.09	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	10.9883		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				2.4397	-1.68328		

## 13.6.4 1.2V Ultra Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Ultra Low V<sub>t</sub> MOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			um	-0.02±0.005		-0.02±0.005		
ΔW(xw +/- dxw)			um	0.01±0.008		0.01±0.008		
Electrical_Tox			Å	28.3±0.670		30±0.670		
Vt_gm	9.4	9.4	V	0.249		0.180	Vg @Vd=0.05V, Vs=Vb=0	
				0.026	-0.026	0.027		
	0.564	0.094		0.403		0.344		
				0.068	-0.068	0.065		
	0.1128	0.094		0.338		0.341		
				0.097	-0.097	0.094		
Vt_lin	9.4	9.4	V	0.193		0.195	Vg @Vd=0.05V, Vs=Vb=0	
				0.030	-0.029	0.029		
	0.564	0.094		0.336		0.367		
				0.074	-0.074	0.071		
	0.1128	0.094		0.287		0.371		
				0.110	-0.107	0.103		
Vt_sat	9.4	9.4	V	0.186		0.176	Vg @Vd=Vdd, Vs=Vb=0	
				0.236		0.243		
	0.564	0.094		0.211		0.279		
DIBL	0.564	0.094	V	0.10006		-0.12363	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.564	0.094	uA/um	112.46		27.815	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.1128	0.094		113		29.18		
Id_sat	0.564	0.094	uA/um	654.75		273.75	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-16.6%	17.4%	-20.4%		
	0.1128	0.094		694.49		271.44		
				-27.9%	27.7%	-30.4%		
loff	0.564	0.094	pA/um	2925.2		4727.3	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.074	16.011	0.086		
Sub Vt slope	0.564	0.094	mV/dec	91.43		107.92	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0.14329		0.012016	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.564	0.094	V	0.056		0.065	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.564	0.094	nA/um	2.589E+00		2.559E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.564	0.094	fF/um	2.77E-01		2.35E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.9542		1.067	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.094	ps/gate	9.08541		-1.41268	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	

## 13.6.5 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>
ΔL (x <sub>l</sub> +/- dx <sub>l</sub> )			um	0.0018±0.01		0.0018±0.01	
ΔW(x <sub>w</sub> +/- dx <sub>w</sub> )			um	0±0.012		0±0.012	
Electrical_Tox			Å	55.4±3.000		58.2±3.000	
Vt_gm	9.4	9.4	V	0.527		0.616	V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0
				0.031	-0.031	0.031	
	9.4	0.2632		0.597		0.520	
				0.050	-0.049	0.050	
	0.376	0.2632		0.530		0.529	
				0.079	-0.079	0.083	
Vt_lin	9.4	9.4	V	0.471		0.654	V <sub>g</sub> @V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0
				0.032	-0.032	0.034	
	9.4	0.2632		0.537		0.534	
				0.054	-0.053	0.057	
	0.376	0.2632		0.481		0.561	
				0.085	-0.085	0.092	
Vt_sat	9.4	9.4	V	0.462		0.640	V <sub>g</sub> @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0
				0.453		0.468	
	0.376	0.2632		0.410		0.498	
DIBL	9.4	0.2632	V	0.083324		-0.066131	V <sub>b</sub> =0, V <sub>t</sub> _lin-V <sub>t</sub> _sat
Id_lin	9.4	0.2632	uA/um	51.461		16.259	Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0
	0.376	0.2632		50.353		13.982	
Id_sat	9.4	0.2632	uA/um	579.75		289.33	Id @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0
				-8.6%	8.1%	-8.1%	
	0.376	0.2632		583.01		258.45	
				-14.1%	13.6%	-13.3%	
loff	9.4	0.2632	pA/um	2.3289		2.2324	Id @V <sub>g</sub> =0, V <sub>d</sub> =1.0V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0
				0.251	4.198	0.266	
Sub V <sub>t</sub> slope	9.4	0.2632	mV/dec	104.44		105.85	Slope @V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0, V <sub>g1</sub> =V <sub>t</sub> _sat-0.05, V <sub>g2</sub> =V <sub>t</sub> _sat-0.06
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		0	Ig @V <sub>g</sub> =V <sub>dd</sub> , V <sub>d</sub> =V <sub>s</sub> =V <sub>b</sub> =0
Body effect	9.4	0.2632	V	0.166		0.293	ΔV <sub>t</sub> _sat @V <sub>b</sub> =-V <sub>dd</sub> /2 and V <sub>b</sub> =0
Isub	9.4	0.2632	nA/um	2.102E+02		1.114E+00	I <sub>bmax</sub> @V <sub>s</sub> =V <sub>b</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , sweep V <sub>g</sub>
Covl	9.4	0.2632	fF/um	1.97E-01		2.10E-01	C <sub>gd</sub> @V <sub>g</sub> =0, V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0
Cj			fF/um <sup>2</sup>	1.08		1.044	V <sub>rev</sub> =0V
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.2632	ps/gate	27.553		-1.7493	RO_Td(ring oscillator delay time) @ V=V <sub>dd</sub> (Fan_out=1)
				2.1206			

## 13.6.6 3.3V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 3.3V Standard V<sub>t</sub> MOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>
ΔL (xL +/- dxL)			um	0.0078±0.012		0.0078±0.012	
ΔW(xw +/- dxw)			um	0±0.012		0±0.012	
Electrical_Tox			Å	72±3.000		75±3.000	
Vt_gm	9.4	9.4	V	0.583		0.697	Vg @Vd=0.05V, Vs=Vb=0
				0.023	-0.023	0.034	
	9.4	0.3572		0.662		0.635	
				0.060	-0.060	0.050	
	0.376	0.3572		0.603		0.634	
				0.072	-0.071	0.062	
Vt_lin	9.4	9.4	V	0.533		0.746	Vg @Vd=0.05V, Vs=Vb=0
				0.024	-0.024	0.037	
	9.4	0.3572		0.617		0.668	
				0.063	-0.062	0.055	
	0.376	0.3572		0.558		0.677	
				0.077	-0.076	0.070	
Vt_sat	9.4	9.4	V	0.520		0.729	Vg @Vd=Vdd, Vs=Vb=0
				0.535		0.610	
	0.376	0.3572		0.488		0.610	
DIBL	9.4	0.3572	V	0.081206		-0.05784	Vb=0, Vt_lin-Vt_sat
Id_lin	9.4	0.3572	uA/um	39.159		12.112	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.376	0.3572		36.766		10.636	
Id_sat	9.4	0.3572	uA/um	587.73		286.15	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				-6.0%	6.0%	-7.9%	
	0.376	0.3572		582.46		262.6	
				-8.0%	9.5%	-10.2%	
loff	9.4	0.3572	pA/um	0.13057		0.13407	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				0.246	4.751	0.525	
Sub Vt slope	9.4	0.3572	mV/dec	92.77		107.19	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9.4	0.3572	V	0.236		0.302	ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9.4	0.3572	nA/um	9.340E+02		1.065E+01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl	9.4	0.3572	fF/um	1.65E-01		1.73E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um <sup>2</sup>	0.962		1.04	Vrev=0V
Inverter FO=1 Delay	Wn/Wp= 3.29/4.7	0.3572	ps/gate	34.396		-1.9039	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.2193			

## 13.6.7 1.2V Native NMOS

The following table summarizes the key parameters for 1.2V native NMOS in CLN85LP process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		Definition	
$\Delta L (x_l +/- dx_l)$			um	$-0.02 \pm 0.005$			
$\Delta W (x_w +/- dx_w)$			um	$0.01 \pm 0.008$			
Electrical_Tox			$\text{\AA}$	$28.3 \pm 0.670$			
Vt_gm	9.4	9.4	V	0.042		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$	
				0.041	-0.041		
	9.4	0.3102		0.179			
				0.055	-0.051		
	0.47	0.188		0.252			
				0.070	-0.066		
Vt_lin	9.4	9.4	V	-0.008		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$	
				0.043	-0.043		
	9.4	0.3102		0.128			
				0.058	-0.054		
	0.47	0.188		0.189			
				0.076	-0.073		
Vt_sat	9.4	9.4	V	-0.054		$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	9.4	0.3102		0.062			
	0.47	0.188		0.125			
DIBL	9.4	0.3102	V	0.066133		$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	9.4	0.3102	uA/um	58.267		$I_d @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$	
	0.47	0.188		73.734			
Id_sat	9.4	0.3102	uA/um	501.82		$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				-12.2%	12.8%		
	0.47	0.188		560.22			
				-14.9%	16.6%		
Ioff	9.4	0.3102	pA/um	60305		$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				0.183	4.698		
Sub Vt slope	9.4	0.3102	mV/dec	79.642		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_{t\_sat} - 0.05, V_{g2} = V_{t\_sat} - 0.06$	
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0.15028		$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	9.4	0.3102	V	0.015		$\Delta V_{t\_sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	9.4	0.3102	nA/um	0.312		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl	9.4	0.188	fF/um	3.55E-01		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/um <sup>2</sup>	0.1496		$V_{rev} = 0\text{V}$	

## 13.6.8 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN85LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>
$\Delta L (x_l +/- dx_l)$			um	$-0.0232 \pm 0.01$		
$\Delta W (x_w +/- dx_w)$			um	$0 \pm 0.012$		
Electrical_Tox			Å	$55.4 \pm 3.000$		
Vt_gm	9.4	9.4	V	-0.022		$V_g @ V_d = 0.05V, V_s = V_b = 0$
				0.049	-0.049	
	9.4	1.128		-0.051		
				0.084	-0.084	
	0.47	1.128		0.028		
				0.098	-0.097	
Vt_lin	9.4	9.4	V	-0.054		$V_g @ V_d = 0.05V, V_s = V_b = 0$
				0.053	-0.053	
	9.4	1.128		-0.080		
				0.087	-0.088	
	0.47	1.128		0.000		
				0.102	-0.102	
Vt_sat	9.4	9.4	V	-0.065		$V_g @ V_d = V_{dd}, V_s = V_b = 0$
		1.128		-0.153		
	0.47	1.128		-0.045		
DIBL	9.4	1.128	V	0.072571		$V_b = 0, V_t_{lin} - V_t_{sat}$
Id_lin	9.4	1.128	uA/um	18.027		$I_d @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$
	0.47	1.128		15.849		
Id_sat	9.4	1.128	uA/um	395.04		$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$
				-11.4%	12.0%	
	0.47	1.128		340.93		
				-12.0%	13.5%	
Ioff	9.4	1.128	pA/um	1.81E+06		$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$
Sub Vt slope	9.4	1.128	mV/dec	0.212	3.008	Slope @ $V_d = V_{dd}, V_s = V_b = 0$ , $V_{g1} = V_{t\_sat} - 0.05, V_{g2} = V_{t\_sat} - 0.06$
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$
Body effect	9.4	1.128	V	0.045		$\Delta V_{t\_sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$
Isub	9.4	1.128	nA/um	0.841		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}$ , sweep $V_g$
Covl	9.4	1.128	fF/um	1.85E-01		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$
Cj			fF/um <sup>2</sup>	0.1363		$V_{rev} = 0V$

## 13.6.9 3.3V Native NMOS

The following table summarizes the key parameters for 3.3V native NMOS in CLN85LP process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		Definition
$\Delta L (x_l +/- dx_l)$			um	$-0.0222 \pm 0.012$		
$\Delta W (x_w +/- dx_w)$			um	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$72 \pm 3.000$		
Vt_gm	9.4	9.4	V	-0.014		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
	9.4	1.128		0.060	-0.061	
	0.47	1.128		-0.051		
				0.085	-0.087	
					0.089	
				0.104	-0.105	
Vt_lin	9.4	9.4	V	-0.048		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
	9.4	1.128		0.063	-0.065	
	0.47	1.128		-0.080		
				0.089	-0.092	
					0.048	
				0.110	-0.111	
Vt_sat	9.4	9.4	V	-0.062		$V_g @ V_d = V_{dd}, V_s = V_b = 0$
	9.4	1.128		-0.222		
	0.47	1.128		-0.010		
DIBL	9.4	1.128	V	0.1418		$V_b = 0, V_t_{lin} - V_t_{sat}$
Id_lin	9.4	1.128	uA/um	18.384		$Id @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$
	0.47	1.128		15.963		
Id_sat	9.4	1.128	uA/um	484.93		$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$
	0.47	1.128		-7.9%      8.2%		
				416.66		
				-12.6%      13.3%		
Ioff	9.4	1.128	pA/um	3.57E+06		$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$
				0.332      2.216		
Sub Vt slope	9.4	1.128	mV/dec	96.989		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g1 = V_{t\_sat}-0.05, V_g2 = V_{t\_sat}-0.06$
Ig_inv	9.4	9.4	nA/um <sup>2</sup>	0		$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$
Body effect	9.4	1.128	V	0.061		$\Delta V_{t\_sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$
Isub	9.4	1.128	nA/um	16.967		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$
Covl	9.4	1.128	fF/um	1.79E-01		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$
Cj			fF/um <sup>2</sup>	0.13767		$V_{rev} = 0\text{V}$

## 13.7 Key Parameters of MOS Transistors in CLN80GC

### 13.7.1 1.0V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V Standard V<sub>t</sub> MOS in CLN80GC process.

	W (um)	L (um)	Unit	NMOS	PMOS	Definition	
ΔL (xl +/- dxl)			um	-0.031 ± 0.00333	-0.031 ± 0.00333		
ΔW(xw+/-dxw)			um	0.01 ± 0.008	0.01 ± 0.008		
Electrical_Tox			Å	23.4 ± 0.6	25.0 ± 0.6		
Vt_gm	9	9	V	0.262	-0.303	Vg @Vd=0.05V, Vs=Vb=0	
				0.028   -0.029	-0.028   0.030		
				0.408	-0.409		
	0.54	0.09		0.051   -0.051	-0.050   0.051		
				0.356	-0.402		
				0.077   -0.078	-0.073   0.072		
Vt_lin	9	9		0.201	-0.309	Vg @Vd=0.05V, Vs=Vb=0	
				0.030   -0.029	-0.029   0.030		
				0.350	-0.419		
	0.54	0.09		0.057   -0.057	-0.056   0.056		
				0.318	-0.415		
				0.088   -0.088	-0.085   0.084		
Vt_sat	9	9	V	0.193	-0.286	Vg @Vd=Vdd, Vs=Vb=0	
				0.243	-0.320		
				0.229	-0.328		
DIBL	0.54	0.09	V	-0.108	0.099	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	uA/um	112.2	-34.1	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				103.0	-34.1		
Id_sat	0.54	0.09	uA/um	603	-244	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				15.0%   -15.0%	17.0%   -17.1%		
	0.108	0.09		574	-235		
				28.5%   -26.1%	31.1%   -26.0%		
Ioff	0.54	0.09	pA/um	5253	-884	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				2.4E+04   -4398	3.8E+03   -681		
Sub Vt slope	0.54	0.09	mV/dec	104	111	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/um <sup>2</sup>	33	8	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.049	0.072	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	3.33E-01	1.54E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.241	0.198	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.019	0.9867	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	9.96445		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.87021	-1.45464		

## 13.7.2 1.0V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V High V<sub>t</sub> MOS in CLN80GC process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xl +/-dxl)			um	-0.031 ± 0.00333		-0.031 ± 0.00333		
ΔW(xw +/-dxw)			um	0.01 ± 0.008		0.01 ± 0.008		
Electrical_Tox			Å	23.4 ± 0.6		25.0 ± 0.6		
Vt_gm	9	9	V	0.322		-0.367	Vg @Vd=0.05V, Vs=Vb=0	
				0.029	-0.028	-0.027		
				0.457		-0.442		
				0.054	-0.054	-0.054		
				0.402		-0.436		
	0.54	0.09		0.085	-0.086	-0.067		
				0.262		-0.376		
				0.030	-0.028	-0.029		
				0.408		-0.451		
				0.055	-0.054	-0.055		
Vt_lin	0.54	0.09	V	0.369		-0.450	Vg @Vd=0.05V, Vs=Vb=0	
				0.094	-0.092	-0.071		
				0.256		-0.355		
				0.316		-0.355		
				0.296		-0.368		
	0.108	0.09		100.6		-31.6	Vg @Vd=Vdd, Vs=Vb=0	
				89.3		-32.7		
				506		-211		
				15.5%	-15.2%	17.0%		
				482		-206		
Id_sat	0.54	0.09	uA/um	27.8%	-24.3%	27.9%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				757		-380		
				2.3E+03	-555	1.5E+03		
				106		116		
				1.5E+03		-293		
	0.108	0.09		24		4		
				0.065		0.100		
				0.065		0.100		
				3.59E-02		4.43E-03		
				1.085		0.9818		
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	12.23		-1.34	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.8				

### 13.7.3 1.0V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V Low V<sub>t</sub> MOS in CLN80GC process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xl +/- dxl)			um	-0.031 ± 0.00333		-0.031 ± 0.00333		
ΔW(xw+/-dxw)			um	0.01 ± 0.008		0.01 ± 0.008		
Electrical_Tox			Å	23.4 ± 0.6		25.0 ± 0.6		
Vt_gm	9	9	V	0.206		-0.307	Vg @Vd=0.05V, Vs=Vb=0	
				0.028	-0.029	-0.028		
				0.352		-0.364		
	0.54	0.09		0.055	-0.055	-0.055		
				0.325		-0.367		
				0.084	-0.087	-0.067		
Vt_lin	9	9	V	0.148		-0.319	Vg @Vd=0.05V, Vs=Vb=0	
				0.031	-0.031	-0.030		
				0.299		-0.365		
	0.54	0.09		0.061	-0.062	-0.062		
				0.291		-0.377		
				0.093	-0.103	-0.076		
Vt_sat	9	9	V	0.139		-0.306	Vg @Vd=Vdd, Vs=Vb=0	
				0.195		-0.257		
				0.207		-0.282		
DIBL	0.54	0.09	V	-0.104		0.108	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	uA/um	123.8		-39.6	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.108	0.09		107.1		-38.4		
Id_sat	0.54	0.09	uA/um	692		-291	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				15.0%	-14.9%	17.0%		
	0.108	0.09		617		-278		
				27.8%	-24.4%	30.4%		
loff	0.54	0.09	pA/um	17170		-4655	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				1.1E+05	-15019	3.0E+04		
Sub Vt slope	0.54	0.09	mV/dec	107		109	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/um <sup>2</sup>	24		4	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.051		0.084	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	4.45E-02		8.97E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.251		0.216	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.9778		0.9857	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	8.46059			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.68888		-1.37604		

## 13.7.4 1.0V Ultra Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.0V Ultra Low V<sub>t</sub> MOS in CLN80GC process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition	
ΔL (xl +/- dxl)			um	-0.031±0.005	-0.031±0.005		
ΔW(xw+/-dxw)			um	0.01±0.008	0.01±0.008		
Electrical_Tox			Å	23.4±0.600	25±0.600		
Vt_gm	9	9	V	0.195	0.198	Vg @Vd=0.05V, Vs=Vb=0	
				0.031   -0.030	0.031   -0.030		
	0.54	0.09		0.308	0.316		
				0.051   -0.050	0.054   -0.054		
	0.108	0.09		0.284	0.338		
				0.082   -0.081	0.076   -0.073		
Vt_lin	9	9	V	0.140	0.204	Vg @Vd=0.05V, Vs=Vb=0	
				0.032   -0.032	0.034   -0.033		
	0.54	0.09		0.247	0.317		
				0.063   -0.061	0.064   -0.067		
	0.108	0.09		0.243	0.345		
				0.099   -0.095	0.089   -0.088		
Vt_sat	9	9	V	0.134	0.192	Vg @Vd=Vdd, Vs=Vb=0	
				0.120	0.195		
				0.151	0.241		
DIBL	0.54	0.09	V	0.127	-0.122	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	uA/um	134.1	41.6	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				110.9	39.3		
Id_sat	0.54	0.09	uA/um	778	329	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				-16.0%   16.6%	-18.0%   18.1%		
	0.108	0.09		645	288		
				-29.4%   31.6%	-28.4%   31.0%		
Ioff	0.54	0.09	pA/um	86173	23250	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				0.078   11.866	0.145   8.969		
Sub Vt slope	0.54	0.09	mV/dec	92.892	113.5	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/um2	30.69	8.01	lg @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.036	0.040	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	3.81E-01	3.65E-04	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl	0.54	0.09	fF/um	2.84E-01	2.37E-01	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	0.919	0.978	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp= 3.15/4.5	0.09	ps/gate	7.34		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.89	-1.28		

## 13.7.5 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN80GC process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>		<b>Definition</b>
ΔL (xL +/- dxL)			um	-0.014 ± 0.01		-0.014 ± 0.01		
ΔW(xw +/- dxw)			um	0 ± 0.012		0 ± 0.012		
Electrical_Tox			Å	54.4 ± 3		58.3 ± 3		
Vt_gm	9	9	V	0.525		-0.624		Vg @Vd=0.05V, Vs=Vb=0
	9	0.279		0.052	-0.052	-0.042	0.043	
	0.36	0.279		0.589		-0.541		
	9	9		0.062	-0.063	-0.057	0.059	
	9	0.279		0.530		-0.557		
	0.36	0.279		0.090	-0.092	-0.074	0.074	
Vt_lin	9	9	V	0.471		-0.662		Vg @Vd=0.05V, Vs=Vb=0
	9	0.279		0.053	-0.054	-0.045	0.045	
	0.36	0.279		0.536		-0.567		
	9	9		0.067	-0.070			
	9	0.279		0.481		-0.566		
	0.36	0.279		0.100	-0.102	-0.082	0.086	
Vt_sat	9	9	V	0.461		-0.646		Vg @Vd=Vdd, Vs=Vb=0
	9	0.279		0.469		-0.515		
	0.36	0.279		0.425		-0.511		
DIBL	9	0.279	V	0.067		0.052		Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.279	uA/um	48.9		-15.3		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.279		47.8		-17.8		
Id_sat	9	0.279	uA/um	581		-278		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
	9	0.279		14.8%	-12.1%	15.0%	-12.7%	
	0.36	0.279		575		-297		
	0.36	0.279		21.7%	-17.5%	18.7%	-15.7%	
loff	9	0.279	pA/um	0.84		-1.00		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
	9	0.279		1.4E+01	-0.80	4.2E+00	-0.76	
Sub Vt slope	9	0.279	mV/dec	90		102		Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um <sup>2</sup>	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.279	V	0.167		0.303		ΔVt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.279	nA/um	2.04E+02		8.31E-01		Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl			fF/um	0.188		0.191		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um <sup>2</sup>	1.01		1.02		Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.279	ps/gate	27.8277			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				3.506		-3.2093		

## 13.7.6 3.3V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 3.3V Standard V<sub>t</sub> MOS in CLN80GC process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.013 \pm 0.012$	$-0.013 \pm 0.012$		
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0 \pm 0.012$	$0 \pm 0.012$		
Electrical_Tox			$\text{Å}$	$72 \pm 3$	$75 \pm 3$		
V <sub>t_gm</sub>	9	9	V	0.598	-0.709	V <sub>g</sub> @ V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
				0.043   -0.043	-0.057   0.057		
	9	0.378		0.660	-0.657		
				0.059   -0.059	-0.058   0.057		
	0.36	0.378		0.602	-0.654		
				0.063   -0.065	-0.065   0.063		
V <sub>t_lin</sub>	9	9	V	0.542	-0.762	V <sub>g</sub> @ V <sub>d</sub> =0.05V, V <sub>s</sub> =V <sub>b</sub> =0	
				0.046   -0.046	-0.060   0.060		
	9	0.378		0.609	-0.699		
				0.067   -0.065	-0.065   0.063		
	0.36	0.378		0.555	-0.690		
				0.074   -0.073	-0.072   0.070		
V <sub>t_sat</sub>	9	9	V	0.529	-0.751	V <sub>g</sub> @ V <sub>d</sub> =V <sub>dd</sub> , V <sub>s</sub> =V <sub>b</sub> =0	
				0.537	-0.647		
	0.36	0.378		0.489	-0.644		
DIBL	9	0.378	V	0.072	0.051	$V_b=0$ , $V_t_{lin}-V_t_{sat}$	
Id_lin	9	0.378	$\mu\text{A}/\mu\text{m}$	41.2	-11.9	$Id @ V_g=V_{dd}, V_d=0.05V, V_s=V_b=0$	
	0.36	0.378		41.1	-13.9		
Id_sat	9	0.378	$\mu\text{A}/\mu\text{m}$	599	-275	$Id @ V_g=V_{dd}, V_d=V_{dd}, V_s=V_b=0$	
				11.4%   -11.2%	10.2%   -9.9%		
	0.36	0.378		608	-302		
				15.6%   -14.6%	14.6%   -13.4%		
Ioff	9	0.378	pA/ $\mu\text{m}$	0.17	-0.07	$Id @ V_g=0, V_d=1.0V_{dd}, V_s=V_b=0$	
Sub V <sub>t</sub> slope	9	0.378	mV/dec	123	118	Slope @ $V_d=V_{dd}$ , $V_s=V_b=0$ , $V_g1=V_t_{sat}-0.05$ , $V_g2=V_t_{sat}-0.06$	
Ig_inv	9	9	nA/ $\mu\text{m}^2$	0	0	$Ig @ V_g=V_{dd}, V_d=V_s=V_b=0$	
Body effect	9	0.378	V	0.282	0.410	$\Delta V_t_{sat} @ V_b=-V_{dd}/2$ and $V_b=0$	
Isub	9	0.378	nA/ $\mu\text{m}$	1.02E+03	1.11E+01	$I_{bmax} @ V_s=V_b=0, V_d=V_{dd}$ , sweep $V_g$	
Covl			fF/ $\mu\text{m}$	0.177	0.183	$C_{gd} @ V_g=0, V_d=V_{dd}, V_s=V_b=0$	
Cj			fF/ $\mu\text{m}^2$	0.948	1	$V_{rev}=0V$	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.279	ps/gate	34.94		RO_Td(ring oscillator delay time) @ $V=V_{dd}$ (Fan_out=1)	
				4.03	-3.17		

## 13.7.7 1.0V Native NMOS

The following table summarizes the key parameters for 1.0V native NMOS in CLN80GC process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	Definition
$\Delta L (x_l +/- dx_l)$			um	$-0.031 \pm 0.005$	
$\Delta W(x_w +/- dx_w)$			um	$0.01 \pm 0.008$	
Electrical_Tox			$\text{\AA}$	$23.4 \pm 0.6$	
Vt_gm	9	9	V	-0.020	$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
				0.037   -0.037	
	9	0.450		0.100	
				0.042   -0.044	
	0.45	0.270		0.152	
				0.049   -0.052	
Vt_lin	9	9	V	-0.076	$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
				0.038   -0.038	
	9	0.450		0.031	
				0.044   -0.048	
	0.45	0.270		0.095	
				0.052   -0.057	
Vt_sat	9	9	V	-0.135	$V_g @ V_d = V_{dd}, V_s = V_b = 0$
				-0.032	
	0.45	0.270		0.042	
DIBL	9	0.450	V	0.063	$V_b = 0, V_t_{lin} - V_t_{sat}$
Id_lin	9	0.450	uA/um	47.8	$Id @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$
	0.45	0.270		69.4	
Id_sat	9	0.450	uA/um	421	$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$
				11.8%   -10.8%	
	0.45	0.270		538	
				15.9%   -13.7%	
Ioff	9	0.450	pA/um	556200 1.3E+06   -3.8E+05	$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$
Sub Vt slope	9	0.450	mV/dec	92	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g1 = V_t_{sat} - 0.05, V_g2 = V_t_{sat} - 0.06$
Ig_inv	9	9	nA/um <sup>2</sup>	24	$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$
Body effect	9	0.450	V	0.008	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$
Isub	9	0.450	nA/um	1.77E-02	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$
Covl			fF/um	0.520	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$
Cj			fF/um <sup>2</sup>	0.146	$V_{rev} = 0\text{V}$

## 13.7.8 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN80GC process.

	<b>W (<math>\mu\text{m}</math>)</b>	<b>L (<math>\mu\text{m}</math>)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>
$\Delta L (x_l +/- dx_l)$			um	$-0.014 \pm 0.01$		
$\Delta W(x_w +/- dx_w)$			um	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$54.4 \pm 3$		
Vt_gm	9	9	V	-0.114		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
	9	1.197		0.061   -0.061		
	0.5	1.197		-0.129		
				0.087   -0.088		
				-0.082		
				0.089   -0.089		
Vt_lin	9	9	V	-0.144		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$
	9	1.197		0.063   -0.063		
	0.5	1.197		-0.156		
				0.090   -0.090		
				-0.114		
				0.092   -0.092		
Vt_sat	9	9	V	-0.159		$V_g @ V_d = V_{dd}, V_s = V_b = 0$
	9	1.197		-0.216		
	0.5	1.197		-0.153		
DIBL	9	1.197	V	0.060		$V_b = 0, V_t_{lin} - V_t_{sat}$
Id_lin	9	1.197	uA/um	19.9		$I_d @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$
	0.5	1.197		19.8		
Id_sat	9	1.197	uA/um	438		$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$
	9	1.197		11.9%   -10.7%		
	0.5	1.197		429		
	0.5	1.197		14.9%   -13.2%		
loff	9	1.197	pA/um	5080000		$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$
	9	1.197		6.8E+06	-	
	9	1.197		3.7E+06		
Sub Vt slope	9	1.197	mV/dec	83		Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_g1 = V_t_{sat} - 0.05, V_g2 = V_t_{sat} - 0.06$
lg_inv	9	9	nA/um <sup>2</sup>	0		$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$
Body effect	9	1.197	V	0.038		$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$
Isub	9	1.197	nA/um	1.39E+00		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$
Covl			fF/um	0.350		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$
Cj			fF/um <sup>2</sup>	0.1411		$V_{rev} = 0\text{V}$

## 13.7.9 3.3V Native NMOS

The following table summarizes the key parameters for 3.3V native NMOS in CLN80GC process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.013 \pm 0.012$			
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0 \pm 0.012$			
Electrical_Tox			$\text{A}$	$72.0 \pm 3$			
Vt_gm	9	9	V	-0.045		$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				0.030	-0.031		
				0.057	-0.058		
	0.5	1.197		0.049			
				0.062	-0.062		
				-0.079			
Vt_lin	9	9	V	0.051	-0.051	$V_g @ V_d=0.05\text{V}, V_s=V_b=0$	
				-0.102			
	0.5	1.197		0.078	-0.079		
				0.080	-0.081		
Vt_sat	9	9	V	-0.097		$V_g @ V_d=V_{dd}, V_s=V_b=0$	
				-0.218			
	0.5	1.197		-0.039			
DIBL	9	1.197	V	0.116		$V_b=0, V_t_{lin}-V_t_{sat}$	
Id_lin	9	1.197	$\mu\text{A}/\mu\text{m}$	19.0		$I_d @ V_g=V_{dd}, V_d=0.05\text{V}, V_s=V_b=0$	
	0.5	1.197		19.2			
Id_sat	9	1.197	$\mu\text{A}/\mu\text{m}$	497		$I_d @ V_g=V_{dd}, V_d=V_{dd}, V_s=V_b=0$	
				10.1%	-9.3%		
	0.5	1.197		478			
				14.2%	-12.7%		
Ioff	9	1.197	pA/ $\mu\text{m}$	3421000		$I_d @ V_g=0, V_d=1.0V_{dd}, V_s=V_b=0$	
				2.9E+06	-2.0E+06		
Sub Vt slope	9	1.197	mV/dec	92		Slope @ $V_d=V_{dd}, V_s=V_b=0, V_g1=V_t_{sat}-0.05, V_g2=V_t_{sat}-0.06$	
lg_inv	9	9	nA/um <sup>2</sup>	0		$I_g @ V_g=V_{dd}, V_d=V_s=V_b=0$	
Body effect	9	1.197	V	0.067		$\Delta V_t_{sat} @ V_b=-V_{dd}/2 \text{ and } V_b=0$	
Isub	9	1.197	nA/um	2.89E+01		$I_{bmax} @ V_s=V_b=0, V_d=V_{dd}, \text{sweep } V_g$	
Covl			fF/um	0.316		$C_{gd} @ V_g=0, V_d=V_{dd}, V_s=V_b=0$	
Cj			fF/um <sup>2</sup>	0.14		$V_{rev}=0\text{V}$	

## 13.8 Key Parameters of MOS Transistors in CLN80GT

### 13.8.1 1.2V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Standard V<sub>t</sub> MOS in CLN80GT process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.031 \pm 0.005$	$-0.029 \pm 0.005$		
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0.01 \pm 0.008$	$0.01 \pm 0.008$		
Electrical_Tox			$\text{\AA}$	$23.2 \pm 0.6$	$25.0 \pm 0.6$		
Vt_gm	9	9	V	0.210	0.143	Vg @Vd=0.05V, Vs=Vb=0	
				0.038 -0.038	0.038 -0.040		
	0.54	0.09		0.344	0.254		
				0.063 -0.075	0.053 -0.057		
	0.108	0.09		0.266	0.253		
				0.090 -0.102	0.074 -0.078		
	9	9		0.145	0.149		
				0.040 -0.040	0.040 -0.041		
	0.54	0.09		0.275	0.271		
				0.068 -0.080	0.062 -0.067		
	0.108	0.09		0.209	0.269		
				0.100 -0.111	0.088 -0.092		
Vt_sat	9	9	V	0.137	0.128	Vg @Vd=Vdd, Vs=Vb=0	
				0.168	0.134		
				0.119	0.156		
DIBL	0.54	0.09	V	0.107	0.137	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	$\mu\text{A}/\mu\text{m}$	152.1	38.0	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				152.8	40.7		
Id_sat	0.54	0.09	$\mu\text{A}/\mu\text{m}$	959	423	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				20.1% -16.3%	23.0% -17.2%		
	0.108	0.09		1065	443		
				30.4% -24.8%	30.0% -25.1%		
Ioff	0.54	0.09	pA/ $\mu\text{m}$	22430	101300	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				5.5E+05	-20520		
Sub Vt slope	0.54	0.09	mV/dec	277	354	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/ $\mu\text{m}^2$	66	15	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.110	0.107	$\Delta V_t$ sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/ $\mu\text{m}$	3.44E-02	2.13E-03	lbmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/ $\mu\text{m}$	0.337	0.324	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/ $\mu\text{m}^2$	0.935	1.043	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	7.1032		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.2015	-1.0577		

## 13.8.2 1.2V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V high V<sub>t</sub> MOS in CLN80GT process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS	PMOS	Definition	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.031 \pm 0.005$	$-0.029 \pm 0.005$		
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0.01 \pm 0.008$	$0.01 \pm 0.008$		
Electrical_Tox			A	$23.2 \pm 0.6$	$25.0 \pm 0.6$		
Vt_gm	9	9	V	0.269	0.145	Vg @Vd=0.05V, Vs=Vb=0	
				0.040	-0.041		
				0.039	-0.040		
	0.54	0.09		0.378	0.294		
				0.065	-0.071		
				0.059	-0.062		
Vt_lin	0.108	0.09		0.287	0.280	Vg @Vd=0.05V, Vs=Vb=0	
				0.090	-0.089		
				0.082	-0.084		
	9	9		0.199	0.150		
				0.041	-0.041		
				0.040	-0.041		
Vt_sat	0.54	0.09	V	0.307	0.318	Vg @Vd=Vdd, Vs=Vb=0	
				0.072	-0.078		
				0.068	-0.072		
	0.108	0.09		0.229	0.303		
				0.105	-0.103		
				0.094	-0.095		
DIBL	9	9		0.192	0.130	Vg @Vd=Vdd, Vs=Vb=0	
				0.209	0.205		
				0.145	0.206		
	0.54	0.09		V	0.098		
				V	0.113		
				V	0.130		
Id_lin	0.54	0.09	$\mu\text{A}/\mu\text{m}$	147.0	34.5	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				144.4	38.6		
				888	368		
	0.108	0.09		20.0%	-16.0%		
				22.7%	-17.1%		
				999	399		
Id_sat	0.54	0.09	$\mu\text{A}/\mu\text{m}$	30.9%	-24.4%	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				30.2%	-24.7%		
				7508	15150		
	0.108	0.09		1.4E+05	-6750		
				1.4E+05	-12958		
				1.4E+05	-12958		
loff	0.54	0.09	pA/ $\mu\text{m}$	7508	15150	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
Sub Vt slope	0.54	0.09	mV/dec	227	279	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/ $\mu\text{m}^2$	72	17	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.114	0.108	$\Delta V_t$ sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/ $\mu\text{m}$	4.91E-02	2.33E-04	Idmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/ $\mu\text{m}$	0.303	0.336	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/ $\mu\text{m}^2$	0.964	1.04	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	8.1204		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.5024	-1.2865		

### 13.8.3 1.8V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.8V Standard V<sub>t</sub> MOS in CLN80GT process.

	W ( $\mu\text{m}$ )	L ( $\mu\text{m}$ )	Unit	NMOS		PMOS		Definition		
$\Delta L (xl +/- dxl)$			$\mu\text{m}$	$-0.057 \pm 0.08$		$-0.057 \pm 0.08$				
$\Delta W(xw +/- dxw)$			$\mu\text{m}$	$0 \pm 0.012$		$0 \pm 0.012$				
Electrical_Tox			A	$35.1 \pm 1.333$		$38.4 \pm 1.333$				
Vt_gm	9	9	V	0.341		0.352		$Vg @ Vd=0.05\text{V}, Vs=Vb=0$		
				0.050	-0.050	0.051	-0.050			
				0.499		0.424				
	9.0	0.198		0.064	-0.056	0.058	-0.053			
				0.493		0.445				
				0.086	-0.079	0.079	-0.073			
Vt_lin	9	9		0.284		0.374		$Vg @ Vd=0.05\text{V}, Vs=Vb=0$		
				0.053	-0.053	0.053	-0.052			
				0.419		0.423				
	9.0	0.198		0.067	-0.056	0.065	-0.059			
				0.396		0.442				
				0.095	-0.080	0.089	-0.080			
Vt_sat	9	9		0.272		0.361		$Vg @ Vd=Vdd, Vs=Vb=0$		
				0.359		0.360				
				0.335		0.376				
	9.0	0.198		V		0.059				
				0.059		0.062				
				Vb=0, Vt_lin-Vt_sat						
Id_lin	9.0	0.198	$\mu\text{A}/\mu\text{m}$	87.4		22.4		$Id @ Vg=Vdd, Vd=0.05\text{V}, Vs=Vb=0$		
				84.2		20.3				
				668		298				
	9.0	0.198		14.2%	-14.5%	14.4%	-14.9%			
				677		273				
				21.3%	-19.8%	19.1%	-18.7%			
Id_sat	9.0	0.198	$\mu\text{A}/\mu\text{m}$	25		44		$Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0$		
				1.1E+02	-21	1.8E+02	-36			
				Slope @ Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06						
	9.0	0.198		89		101				
				Ioff @ Vg=0, Vd=1.0Vdd, Vs=Vb=0						
				$\Delta Vt_{sat} @ Vb=-Vdd/2 \text{ and } Vb=0$						
Sub Vt slope	9.0	0.198	mV/dec	0		0		$Ibmax @ Vs=Vb=0, Vd=Vdd, sweep Vg$		
				lg_inv @ Vg=Vdd, Vd=Vs=Vb=0						
				Body effect @ Vt_sat @ Vb=-Vdd/2 and Vb=0						
	9.0	0.198		0.162		0.182				
				Isub @ Vs=Vb=0, Vd=Vdd, sweep Vg						
				Covl @ Vg=0, Vd=Vdd, Vs=Vb=0						
Inverter FO=1 Delay	9	9	fF/um2	1.08		1.08		$Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0$		
				Cj @ Vg=0, Vd=Vdd, Vs=Vb=0						
				Vrev=0V						
	9.0	0.198		20.941				$RO\_Td(\text{ring oscillator delay time}) @ V=Vdd \text{ (Fan\_out}=1)$		
				0		0				

## 13.8.4 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN80GT process.

	W (μm)	L (μm)	Unit	NMOS	PMOS	Definition	
ΔL (xl +/- dxl)			μm	-0.014 ± 0.01	-0.014 ± 0.01		
ΔW(xw +/- dxw)			μm	0 ± 0.012	0 ± 0.012		
Electrical_Tox			A	56 ± 3	59.2 ± 3		
Vt_gm	9	9	V	0.520	0.599	Vg @Vd=0.05V, Vs=Vb=0	
				0.041 -0.041	0.041 -0.041		
				0.566	0.493		
				0.059 -0.056	0.057 -0.060		
				0.512	0.503		
	0.4	0.279		0.084 -0.077	0.076 -0.075		
		V	0.472	0.638			
			0.042 -0.042	0.044 -0.044			
			0.518	0.515			
			0.066 -0.067	0.062 -0.067			
Vt_lin	0.4	0.279	V	0.464	0.536	Vg @Vd=0.05V, Vs=Vb=0	
				0.087 -0.087	0.085 -0.086		
				0.462	0.622		
				0.439	0.451		
				0.396	0.468		
DIBL	9	0.279	V	0.079	0.064	Vb=0, Vt_lin-Vt_sat	
Id_lin	9	0.279	μA/μm	50.8	15.9	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
	0.4	0.279		49.4	14.4		
Id_sat	9	0.279	μA/μm	586	288	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				11.8% -10.9%	12.9% -12.0%		
	0.4	0.279		598	269		
				17.2% -15.3%	17.8% -15.4%		
loff	9	0.279	pA/μm	1	4	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				2.4E+01 -1	1.8E+01 -3		
Sub Vt slope	9	0.279	mV/dec	108	109	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/um <sup>2</sup>	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	9	0.279	V	0.074	0.130	Δ Vt_sat @Vb=-Vdd/2 and Vb=0	
Isub	9	0.279	nA/um	1.94E+02	1.61E+00	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.221	0.242	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	1.01	1.016	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.279	ps/gate	26.831		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				5.016	2.918		

## 13.8.5 1.2V Native NMOS

The following table summarizes the key parameters for 1.2V native NMOS in CLN80GT process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>		
$\Delta L (xl +/- dxl)$			μm	$-0.046 \pm 0.005$				
$\Delta W(xw +/- dxw)$			μm	$0.01 \pm 0.008$				
Electrical_Tox			A	$23.2 \pm 0.6$				
Vt_gm	9	9	V	-0.018		Vg @ Vd=0.05V, Vs=Vb=0		
				0.037	-0.037			
				0.151				
	0.45	0.198		0.055	-0.056			
				0.166				
				0.057	-0.058			
Vt_lin	9	9	V	-0.073		Vg @ Vd=0.05V, Vs=Vb=0		
				0.038	-0.038			
				0.052				
	0.45	0.198		0.060	-0.061			
				0.103				
				0.060	-0.069			
Vt_sat	9	9	V	-0.123		Vg @ Vd=Vdd, Vs=Vb=0		
	9	0.198		-0.091				
	0.45	0.198		0.027				
DIBL	9	0.198	V	0.143		Vb=0, Vt_lin-Vt_sat		
Id_lin	9	0.198	$\mu A/\mu m$	105.8		Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0		
	0.45	0.198		100.3				
Id_sat	9	0.198	$\mu A/\mu m$	825		Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0		
				11.9%	-10.6%			
	0.45	0.198		818				
				15.8%	-13.2%			
Ioff	9	0.198	$pA/\mu m$	3103000		Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0		
Sub Vt slope	9	0.198		5.7E+06	-2.0E+06			
lg_inv	9	9	nA/um <sup>2</sup>	70		lg @ Vg=Vdd, Vd=Vs=Vb=0		
Body effect	9	0.198	V	0.173		$\Delta Vt_{sat}$ @ Vb=-Vdd/2 and Vb=0		
Isub	9	0.198	nA/um	2.50E-02		lbmax @ Vs=Vb=0, Vd=Vdd, sweep Vg		
Covl			fF/um	0.288		Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0		
Cj			fF/um <sup>2</sup>	0.144		Vrev=0V		

## 13.8.6 1.8V Native NMOS

The following table summaries the key parameters for 1.8V native NMOS in CLN90GT process.

	<b>W ( <math>\mu\text{m}</math> )</b>	<b>L ( <math>\mu\text{m}</math> )</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			$\mu\text{m}$	$-0.04 \pm 0.044$			
$\Delta W(x_w +/- dx_w)$			$\mu\text{m}$	$0 \pm 0.012$			
Electrical_Tox			A	$35.1 \pm 1.333$			
Vt_gm	0.45	0.792	V	0.069		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$	
				0.055	-0.055		
				0.177			
				0.097	-0.096		
				0.206			
				0.108	-0.107		
Vt_lin	0.45	0.792	V	0.014		$V_g @ V_d = 0.05\text{V}, V_s = V_b = 0$	
				0.057	-0.057		
				0.115			
				0.108	-0.109		
				0.144			
				0.122	-0.122		
Vt_sat	0.45	0.792	V	-0.029		$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
				0.072			
				0.098			
DIBL	9	0.792	V	0.044		$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	0.45	0.792	$\mu\text{A}/\mu\text{m}$	30.2		$I_d @ V_g = V_{dd}, V_d = 0.05\text{V}, V_s = V_b = 0$	
				27.9			
Id_sat	0.45	0.792	$\mu\text{A}/\mu\text{m}$	472		$I_d @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				11.5%	-11.2%		
				435			
				14.9%	-14.2%		
Ioff	9	0.792	pA/ $\mu\text{m}$	17160		$I_d @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
Sub Vt slope	9	0.792	mV/dec	82		Slope @ $V_d = V_{dd}, V_s = V_b = 0$ , $V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$	
Ig_inv	9	9	nA/um <sup>2</sup>	0		$I_g @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	9	0.792	V	0.017		$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	9	0.792	nA/um	4.51		$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/um	0.373		$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/um <sup>2</sup>	0.159		$V_{rev} = 0\text{V}$	

## 13.8.7 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CLN80GT process.

	<b>W ( <math>\mu</math> m)</b>	<b>L ( <math>\mu</math> m)</b>	<b>Unit</b>	<b>NMOS</b>		<b>Definition</b>		
$\Delta L$ (xl +/- dxl)			$\mu$ m	$-0.01 \pm 0.01$				
$\Delta W$ (xw+/-dxw)			$\mu$ m	$0 \pm 0.012$				
Electrical_Tox			A	$56.0 \pm 3$				
Vt_gm	9	9	V	-0.100		Vg @Vd=0.05V, Vs=Vb=0		
				0.058	-0.058			
	9	1.188		-0.116				
				0.085	-0.085			
	0.5	1.188		-0.064				
				0.086	-0.087			
Vt_lin	9	9	V	-0.124		Vg @Vd=0.05V, Vs=Vb=0		
				0.060	-0.060			
	9	1.188		-0.147				
				0.087	-0.088			
	0.5	1.188		-0.090				
				0.090	-0.091			
Vt_sat	9	9	V	-0.132		Vg @Vd=Vdd, Vs=Vb=0		
	9	1.188		-0.211				
	0.5	1.188		-0.119				
DIBL	9	1.188	V	0.064		$V_b=0, V_{t\_lin}-V_{t\_sat}$		
Id_lin	9	1.188	$\mu A/\mu m$	19.5		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0		
	0.5	1.188		17.5				
Id_sat	9	1.188	$\mu A/\mu m$	439		Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0		
				11.9%	-10.3%			
	0.5	1.188		391				
				15.2%	-13.0%			
loff	9	1.188	$pA/\mu m$	4177000		Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0		
				8.5E+06	-3.0E+06			
Sub Vt slope	9	1.188	mV/dec	793		Slope @Vd=Vdd, Vs=Vb=0, $Vg1=V_{t\_sat}-0.05, Vg2=V_{t\_sat}-0.06$		
Ig_inv	9	9	nA/um <sup>2</sup>	0		Ig @Vg=Vdd, Vd=Vs=Vb=0		
Body effect	9	1.188	V	0.085		$\Delta V_{t\_sat}$ @ $V_b=-Vdd/2$ and $V_b=0$		
Isub	9	1.188	nA/um	1.77E-02		lbmax @Vs=Vb=0, Vd=Vdd, sweep Vg		
Covl			fF/um	0.384		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0		
Cj			fF/um <sup>2</sup>	0.124		Vrev=0V		

## 13.9 Key Parameters of MOS Transistors in CLN80HS

### 13.9.1 1.05V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.05V Standard V<sub>t</sub> MOS in CLN80HS process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>	
Δ L (xL +/- dxL)			μm	-0.045 ± 0.005	-0.043 ± 0.005		
Δ W(xw +/- dxw)			μm	0.01 ± 0.0072	0.01 ± 0.0072		
Electrical_Tox			Å	19.1 ± 0.6	20.5 ± 0.6		
Vt_gm	9	1.08	V	0.199	0.201	Vg @ Vd=0.05V, Vs=Vb=0	
				0.041 -0.041	0.043 -0.039		
				0.333	0.301		
	0.54	0.09		0.065 -0.073	0.058 -0.062		
				0.299	0.282		
				0.081 -0.090	0.089 -0.095		
Vt_lin	9	1.08		0.136	0.207	Vg @ Vd=0.05V, Vs=Vb=0	
				0.044 -0.044	0.046 -0.041		
				0.274	0.310		
	0.54	0.09		0.073 -0.082	0.067 -0.073		
				0.254	0.285		
				0.094 -0.104	0.098 -0.106		
Vt_sat	9	1.08	V	0.108	0.178	Vg @ Vd=Vdd, Vs=Vb=0	
				0.142	0.145		
				0.141	0.156		
DIBL	0.54	0.09	V	0.132	0.164	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	μA/μm	142.9	49.1	Id @ Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				132.7	60.3		
Id_sat	0.54	0.09	μA/μm	976	480	Id @ Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				21.9% -16.9%	23.1% -18.5%		
	0.108	0.09		1015	573		
				31.8% -24.7%	29.3% -24.6%		
Ioff	0.54	0.09	nA/μm	65 1.3E+03	85 -57	Id @ Vg=0, Vd=1.0Vdd, Vs=Vb=0	
Sub Vt slope	0.54	0.09	mV/dec	93	106	Slope @ Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	1.08	nA/um <sup>2</sup>	789	542	Ig @ Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.029	0.026	Δ Vt_sat @ Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	2.93E-01	2.82E-03	Ibmax @ Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.248	0.215	Cgd @ Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.959	0.962	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	5.6584 1.2876	-1.1393	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	

## 13.9.2 1.05V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.05V High V<sub>t</sub> MOS in CLN80HS process.

	<b>W ( μm)</b>	<b>L ( μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>	
Δ L (xl +/-dxl)			μm	-0.045 ± 0.005	-0.043 ± 0.005		
Δ W(xw+/-dxw)			μm	0.01 ± 0.0072	0.01 ± 0.0072		
Electrical_Tox			Å	19.1 ± 0.6	20.5 ± 0.6		
Vt_gm	9	1.08	V	0.230	0.216	Vg @Vd=0.05V, Vs=Vb=0	
				0.041 -0.042	0.044 -0.039		
				0.402	0.338		
				0.060 -0.068	0.058 -0.066		
				0.360	0.315		
	0.54	0.09		0.084 -0.095	0.083 -0.088		
				0.166	0.221		
				0.044 -0.051	0.046 -0.041		
				0.352	0.353		
				0.072 -0.081	0.064 -0.072		
Vt_lin	0.108	0.09	V	0.316	0.319	Vg @Vd=0.05V, Vs=Vb=0	
				0.097 -0.109	0.091 -0.097		
				0.134	0.186		
				0.234	0.221		
				0.216	0.209		
DIBL	0.54	0.09	V	0.117	0.132	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	μA/μm	128.9	45.4	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				123.8	56.6		
Id_sat	0.54	0.09	μA/μm	823	406	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				19.3% -16.9%	23.8% -18.6%		
	0.108	0.09		863	500		
				30.5% -24.0%	30.1% -24.6%		
Ioff	0.54	0.09	nA/μm	11 1.2E+02 -9	14 1.2E+02 -11	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
Sub Vt slope	0.54	0.09	mV/dec	101	103	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	1.08	nA/um <sup>2</sup>	856	537	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.047	0.037	Δ Vt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	2.40E-01	2.54E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.241	0.211	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.959	0.962	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	6.9462 1.5352	-1.3279	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	

### 13.9.3 1.05V Low V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.05V Low V<sub>t</sub> MOS in CLN80HS process.

	<b>W ( μm)</b>	<b>L ( μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>	
Δ L (xl +/-dxl)			μm	-0.045 ± 0.005	-0.043 ± 0.005		
Δ W(xw+/-dxw)			μm	0.01 ± 0.0072	0.01 ± 0.0072		
Electrical_Tox			Å	19.1 ± 0.6	20.5 ± 0.6		
Vt_gm	9	1.08	V	0.180	0.196	Vg @Vd=0.05V, Vs=Vb=0	
				0.041 -0.040	0.043 -0.039		
				0.275	0.270		
				0.063 -0.073	0.060 -0.061		
				0.250	0.258		
	0.54	0.09		0.078 -0.089	0.089 -0.095		
				0.118	0.204		
				0.044 -0.043	0.046 -0.041		
				0.216	0.275		
				0.072 -0.082	0.071 -0.078		
Vt_lin	0.108	0.09	V	0.198	0.260	Vg @Vd=0.05V, Vs=Vb=0	
				0.092 -0.103	0.100 -0.113		
				0.099	0.178		
				0.083	0.104		
				0.089	0.119		
DIBL	0.54	0.09	V	0.133	0.171	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	μA/μm	158.4	52.1	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				149.9	62.9		
Id_sat	0.54	0.09	μA/μm	1112	525	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				21.5% -16.5%	24.2% -18.8%		
	0.108	0.09		1169	628		
				30.9% -24.6%	31.0% -23.9%		
Ioff	0.54	0.09	nA/μm	325	200	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				6.3E+03 -292	3.3E+03 -178		
Sub Vt slope	0.54	0.09	mV/dec	114	100	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	1.08	nA/um <sup>2</sup>	896	504	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.023	0.020	Δ Vt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	3.35E-01	3.35E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.251	0.216	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um <sup>2</sup>	0.959	0.962	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.09	ps/gate	4.975		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				1.1248	-1.0057		

## 13.9.4 1.8V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.8V Standard V<sub>t</sub> MOS in CLN80HS process.

	<b>W ( μm)</b>	<b>L ( μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>
Δ L (xl +/-dxl)			μm	-0.053 ± 0.008	-0.053 ± 0.008	
Δ W(xw+/-dxw)			μm	0 ± 0.012	0 ± 0.012	
Electrical_Tox			Å	35.2 ± 1.333	38.4 ± 1.333	
Vt_gm	9	9	V	0.354	0.347	Vg @Vd=0.05V, Vs=Vb=0
				0.041 -0.041	0.041 -0.041	
	9	0.198		0.533	0.447	
				0.060 -0.060	0.058 -0.060	
	0.36	0.198		0.551	0.467	
			V	0.090 -0.090	0.076 -0.075	
	9	9		0.298	0.351	
				0.043 -0.043	0.043 -0.043	
	9	0.198		0.464	0.459	
				0.064 -0.064	0.065 -0.067	
Vt_lin	9	0.198	V	0.483	0.464	Vg @Vd=0.05V, Vs=Vb=0
				0.097 -0.097	0.085 -0.081	
	0.36	0.198		0.263	0.333	
				0.380	0.380	
Vt_sat	9	0.198	V	0.392	0.379	Vg @Vd=Vdd, Vs=Vb=0
				0.084	0.079	
	0.36	0.198		0.084	0.079	
Id_lin	9	0.198	μA/μm	79.4	22.3	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
				71.8	25.4	
Id_sat	9	0.198	μA/μm	660	296	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				13.9% -12.7%	14.0% -12.9%	
	0.36	0.198		620	314	
				21.0% -19.5%	19.1% -18.8%	
Ioff	9	0.198	pA/μm	9 2.6E+01 -6	17 8.2E+01 -13	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
Sub Vt slope	9	0.198	mV/dec	91	116	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um <sup>2</sup>	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.198	V	0.087	0.141	Δ Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.198	nA/um	5.70E+01	5.09E-01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl			fF/um	0.198	0.225	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um <sup>2</sup>	0.877	0.981	Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.198	ps/gate	16.8547 2.6815	-2.1854	RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)

## 13.9.5 2.5V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN80HS process.

	<b>W ( μm)</b>	<b>L ( μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>
Δ L (xl +/-dxl)			μm	-0.014 ± 0.01	-0.014 ± 0.01	
Δ W(xw+/-dxw)			μm	0 ± 0.012	0 ± 0.012	
Electrical_Tox			Å	54.4 ± 3	58.3 ± 3	
Vt_gm	9	9	V	0.581	0.568	Vg @Vd=0.05V, Vs=Vb=0
				0.052 -0.052	0.050 -0.050	
	9	0.279		0.620	0.506	
				0.058 -0.060	0.061 -0.061	
	0.36	0.279		0.550	0.501	
			V	0.088 -0.089	0.079 -0.078	
	9	9		0.534	0.604	
				0.053 -0.053	0.053 -0.053	
	9	0.279		0.564	0.530	
				0.064 -0.067	0.065 -0.068	
Vt_lin	9	0.279	V	0.491	0.491	Vg @Vd=0.05V, Vs=Vb=0
				0.097 -0.100	0.085 -0.088	
	0.36	0.279				
Vt_sat	9	9	V	0.524	0.587	Vg @Vd=Vdd, Vs=Vb=0
		0.279		0.505	0.475	
	0.36	0.279		0.440	0.437	
DIBL	9	0.279	V	0.059	0.055	Vb=0, Vt_lin-Vt_sat
Id_lin	9	0.279	μA/μm	46.4	15.6	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0
	0.36	0.279		46.9	19.3	
Id_sat	9	0.279	μA/μm	579	290	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0
				11.4% -10.6%	13.1% -11.6%	
	0.36	0.279		609	335	
				17.4% -15.4%	18.1% -15.0%	
Ioff	9	0.279	pA/μm	0	2	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0
				4.4E+00	0	
Sub Vt slope	9	0.279	mV/dec	91	100	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06
Ig_inv	9	9	nA/um <sup>2</sup>	0	0	Ig @Vg=Vdd, Vd=Vs=Vb=0
Body effect	9	0.279	V	0.209	0.141	Δ Vt_sat @Vb=-Vdd/2 and Vb=0
Isub	9	0.279	nA/um	2.13E+02	9.16E-01	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg
Covl			fF/um	0.179	0.189	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0
Cj			fF/um <sup>2</sup>	0.877	0.981	Vrev=0V
Inverter FO=1 Delay	Wn/Wp = 3.15/4.5	0.198	ps/gate	27.88		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)
				2.82	-2.48	

## 13.9.6 1.05V Native NMOS

The following table summarizes the key parameters for 1.05V native NMOS in CLN80HS process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			μm	$-0.045 \pm 0.005$		
$\Delta W(x_w +/- dx_w)$			μm	$0.01 \pm 0.0072$		
Electrical_Tox			Å	$19.1 \pm 0.6$		
Vt_gm	9	1.08	V	0.087	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.039   -0.039		
	0.89	0.27		0.169		
				0.051   -0.054		
	0.45	0.27		0.171		
				0.054   -0.056		
Vt_lin	9	1.08	V	0.024	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.041   -0.041		
	0.89	0.27		0.064		
				0.056   -0.060		
	0.45	0.27		0.087		
				0.059   -0.068		
Vt_sat	9	1.08	V	-0.028	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	0.89	0.27		-0.039		
	0.45	0.27		0.007		
DIBL	0.89	0.27	V	0.103	$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	0.89	0.27	$\mu A / \mu m$	81.1	$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
	0.45	0.27		78.5		
Id_sat	0.89	0.27	$\mu A / \mu m$	703	$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				13.8%   -12.3%		
	0.45	0.27		682		
				14.4%   -13.7%		
Ioff	0.89	0.27	nA/ μm	819 2.0E+03   -578	$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
Sub Vt slope	0.89	0.27	mV/dec	115	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$	
Ig_inv	9	1.08	nA/um <sup>2</sup>	428	$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	0.89	0.27	V	0.026	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	0.89	0.27	nA/um	1.15E-02	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{ sweep } V_g$	
Covl			fF/um	0.290	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/um <sup>2</sup>	0.159	$V_{rev} = 0V$	

## 13.9.7 1.8V Native NMOS

The following table summarizes the key parameters for 1.8V native NMOS in CLN80HS process.

	<b>W (<math>\mu</math> m)</b>	<b>L (<math>\mu</math> m)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			$\mu$ m	$-0.053 \pm 0.008$		
$\Delta W(x_w +/- dx_w)$			$\mu$ m	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$35.2 \pm 1.333$		
Vt_gm	9	9	V	0.186	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.052   -0.052		
	9	0.792		0.285		
				0.084   -0.083		
	0.45	0.792		0.309		
				0.094   -0.092		
Vt_lin	9	9	V	0.126	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.055   -0.055		
	9	0.792		0.216		
				0.094   -0.094		
	0.45	0.792		0.246		
				0.105   -0.104		
Vt_sat	9	9	V	0.065	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	9	0.792		0.163		
	0.45	0.792		0.183		
DIBL	9	0.792	V	0.052	$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	9	0.792	$\mu A / \mu m$	29.1	$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
	0.45	0.792		27.4		
Id_sat	9	0.792	$\mu A / \mu m$	447	$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				10.9%   -10.5%		
	0.45	0.792		418		
				14.7%   -14.2%		
Ioff	9	0.792	pA/ $\mu$ m	1102	$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				2.0E+04   -1.0E+03		
Sub Vt slope	9	0.792	mV/dec	80	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$	
Ig_inv	9	9	nA/ $\mu m^2$	0	$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	9	0.792	V	0.035	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	9	0.792	nA/ $\mu m$	8.01E+00	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/ $\mu m$	0.370	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/ $\mu m^2$	0.154	$V_{rev} = 0V$	

## 13.9.8 2.5V Native NMOS

The following table summarizes the key parameters for 2.5V native NMOS in CL80HS process.

	<b>W (<math>\mu</math> m)</b>	<b>L (<math>\mu</math> m)</b>	<b>Unit</b>	<b>NMOS</b>	<b>Definition</b>	
$\Delta L (x_l +/- dx_l)$			$\mu$ m	$0.01 \pm 0.01$		
$\Delta W(x_w +/- dx_w)$			$\mu$ m	$0 \pm 0.012$		
Electrical_Tox			$\text{\AA}$	$54.4 \pm 3$		
Vt_gm	9	9	V	-0.045	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.060   -0.060		
	9	1.197		-0.057		
				0.084   -0.084		
	0.45	1.197		0.005		
				0.089   -0.089		
Vt_lin	9	9	V	-0.083	$V_g @ V_d = 0.05V, V_s = V_b = 0$	
				0.063   -0.063		
	9	1.197		-0.107		
				0.089   -0.089		
	0.45	1.197		-0.029		
				0.091   -0.091		
Vt_sat	9	9	V	-0.096	$V_g @ V_d = V_{dd}, V_s = V_b = 0$	
	9	1.197		-0.179		
	0.45	1.197		-0.062		
DIBL	9	1.197	V	0.072	$V_b = 0, V_t_{lin} - V_t_{sat}$	
Id_lin	9	1.197	$\mu A / \mu m$	19.0	$Id @ V_g = V_{dd}, V_d = 0.05V, V_s = V_b = 0$	
	0.45	1.197		19.4		
Id_sat	9	1.197	$\mu A / \mu m$	430	$Id @ V_g = V_{dd}, V_d = V_{dd}, V_s = V_b = 0$	
				11.7%   -10.5%		
	0.45	1.197		420		
				15.3%   -13.3%		
Ioff	9	1.197	pA/ $\mu$ m	2701000	$Id @ V_g = 0, V_d = 1.0V_{dd}, V_s = V_b = 0$	
				4.3E+06   -2.0E+06		
Sub Vt slope	9	1.197	mV/dec	95	Slope @ $V_d = V_{dd}, V_s = V_b = 0, V_{g1} = V_t_{sat} - 0.05, V_{g2} = V_t_{sat} - 0.06$	
Ig_inv	9	9	nA/ $\mu m^2$	0	$Ig @ V_g = V_{dd}, V_d = V_s = V_b = 0$	
Body effect	9	1.197	V	0.039	$\Delta V_t_{sat} @ V_b = -V_{dd}/2 \text{ and } V_b = 0$	
Isub	9	1.197	nA/ $\mu m$	5.69E+01	$I_{bmax} @ V_s = V_b = 0, V_d = V_{dd}, \text{sweep } V_g$	
Covl			fF/ $\mu m$	0.350	$C_{gd} @ V_g = 0, V_d = V_{dd}, V_s = V_b = 0$	
Cj			fF/ $\mu m^2$	0.147	$V_{rev} = 0V$	

## 13.10 Key Parameters of MOS Transistors in CLN80LP

### 13.10.1 1.2V Standard V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V Standard V<sub>t</sub> MOS in CLN80LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>	<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			μm	-0.02 ± 0.005	-0.02 ± 0.005		
ΔW(xw +/- dxw)			μm	0.01 ± 0.008	0.01 ± 0.008		
Electrical_Tox			Å	28.3 ± 0.67	30.3 ± 0.67		
Vt_gm	9	9	V	0.250	0.185	Vg @Vd=0.05V, Vs=Vb=0	
				0.031   -0.031	0.031   -0.031		
	0.54	0.09		0.563	0.471		
				0.068   -0.074	0.057   -0.062		
	0.108	0.09		0.481	0.441		
				0.092   -0.102	0.084   -0.088		
Vt_lin	9	9	V	0.197	0.197	Vg @Vd=0.05V, Vs=Vb=0	
				0.032   -0.032	0.033   -0.033		
	0.54	0.09		0.481	0.497		
				0.077   -0.083	0.066   -0.069		
	0.108	0.09		0.411	0.465		
				0.109   -0.121	0.094   -0.098		
Vt_sat	9	9	V	0.175	0.157	Vg @Vd=Vdd, Vs=Vb=0	
				0.364	0.364		
	0.108	0.09		0.317	0.344		
DIBL	0.54	0.09	V	0.116	0.133	Vb=0, Vt_lin-Vt_sat	
Id_lin	0.54	0.09	μA/μm	97.7	25.4	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				96.2	27.6		
Id_sat	0.54	0.09	μA/μm	532	221	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				21.5%   -19.9%	21.0%   -19.7%		
	0.108	0.09		558	241		
				32.1%   -27.1%	31.2%   -27.5%		
loff	0.54	0.09	pA/μm	126	327	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0	
				1.8E+03   -116	3.1E+03   -291		
Sub Vt slope	0.54	0.09	mV/dec	103	131	Slope @Vd=Vdd, Vs=Vb=0, Vg1=Vt_sat-0.05, Vg2=Vt_sat-0.06	
Ig_inv	9	9	nA/um2	0.147111	0.00963309	Ig @Vg=Vdd, Vd=Vs=Vb=0	
Body effect	0.54	0.09	V	0.054	0.072	ΔVt_sat @Vb=-Vdd/2 and Vb=0	
Isub	0.54	0.09	nA/um	5.36E-01	9.41E-03	Ibmax @Vs=Vb=0, Vd=Vdd, sweep Vg	
Covl			fF/um	0.227	0.206	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
Cj			fF/um2	1.08	0.985	Vrev=0V	
Inverter FO=1 Delay	Wn/Wp=3.15/4.5	0.09	ps/gate	12.175		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	
				2.715	-2.098		

## 13.10.21.2V High V<sub>t</sub> MOS

The following table summarizes the key parameters for 1.2V high V<sub>t</sub> MOS in CLN80LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>	<b>Definition</b>	
ΔL (xL +/- dxL)			μm	-0.02 ± 0.005		-0.02 ± 0.005		
ΔW(xw+/-dxw)			μm	0.01 ± 0.008		0.01 ± 0.008		
Electrical_Tox			Å	28.3 ± 0.67		30.3 ± 0.67		
Vt_gm	9	9	V	0.396		0.434	Vg @Vd=0.05V, Vs=Vb=0	
				0.030	-0.030	0.031		
				0.677		0.597		
				0.063	-0.067	0.059		
				0.560		0.558		
	0.5	0.09		0.091	-0.090	0.086		
				0.331		0.448		
				0.032	-0.032	0.033		
				0.583		0.621		
				0.065	-0.067	0.064		
Vt_lin	0.5	0.09	V	0.495		0.565	Vg @Vd=0.05V, Vs=Vb=0	
				0.094	-0.101	0.091		
				0.410		0.471		
				0.115		0.117		
				78.4		20.3		
Vt_sat	0.11	0.09	μA/μm	82.1		23.5	Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0	
				395		151		
				21.4%	-19.7%	21.2%		
				454		169		
				32.0%	-26.7%	33.6%		
Id_sat	0.11	0.09	μA/μm	10		15	Id @Vg=Vdd, Vd=Vdd, Vs=Vb=0	
				5.8E+01	-8	5.4E+01		
				32.0%		28.3%		
				2.89E-01		8.12E-03		
				18.241				
Ioff	0.5	0.09	pA/μm	1.296		0.985	Cgd @Vg=0, Vd=Vdd, Vs=Vb=0	
				4.064		-3.256		
Inverter FO=1 Delay	Wn/Wp=3.15/ 4.5	0.09	ps/gate	1.296			RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)	

## **13.10.32.5V Standard Vt MOS**

The following table summarizes the key parameters for 2.5V Standard V<sub>t</sub> MOS in CLN80LP process.

	<b>W (μm)</b>	<b>L (μm)</b>	<b>Unit</b>	<b>NMOS</b>		<b>PMOS</b>		<b>Definition</b>		
Δ L (xl +/-dxl)			μ m	-0.014 ± 0.01		-0.014± 0.01				
Δ W(xw+/-dxw)			μ m	0 ± 0.012		0 ± 0.012				
Electrical_Tox			Å	58.7 ± 3		61.7 ± 3				
Vt_gm	9	9	V	0.511		0.505		Vg @Vd=0.05V, Vs=Vb=0		
				0.041	-0.041	0.041	-0.041			
				0.571		0.421				
				0.060	-0.063	0.051	-0.052			
				0.511		0.440				
	9.0	0.279		0.095	-0.096	0.072	-0.072			
		V	0.462		0.536					
			0.042	-0.041	0.044	-0.044				
			0.512		0.441					
			0.064	-0.066	0.056	-0.057				
Vt_lin	9.0	0.279	V	0.462		0.469		Vg @Vd=0.05V, Vs=Vb=0		
				0.101	-0.103	0.082	-0.082			
				0.101		-0.103				
				0.082		-0.082				
				-0.082		0.082				
Vt_sat	9	9	V	0.452		0.518		Vg @Vd=Vdd, Vs=Vb=0		
				0.438		0.379				
				0.398		0.404				
DIBL	9.0	0.279	V	0.074		0.062		Vb=0, Vt_lin-Vt_sat		
Id_lin	9.0	0.279	μ A/ μ m	51.1		15.8		Id @Vg=Vdd, Vd=0.05V, Vs=Vb=0		
				48.1		13.6				
Id_sat	9.0	0.279		576		292				
				12.4%	-10.5%	13.3%	-11.5%			
				572		256				
				17.6%	-14.9%	18.1%	-15.3%			
				2		18				
loff	9.0	0.279	pA/ μ m	3.2E+01	-1	6.7E+01	-13	Id @Vg=0, Vd=1.0Vdd, Vs=Vb=0		
Sub Vt slope	9.0	0.279	mV/dec	90		101				
Ig_inv	9	9	nA/um2	0		0		Ig @Vg=Vdd, Vd=Vs=Vb=0		
Body effect	9.0	0.279	V	0.182		0.280		Δ Vt_sat @Vb=-Vdd/2 and Vb=0		
Isub	9.0	0.279	nA/um	1.30E+02		2.19E+00		lbmax @Vs=Vb=0, Vd=Vdd, sweep Vg		
Covl			fF/um	0.187		0.195		Cgd @Vg=0, Vd=Vdd, Vs=Vb=0		
Cj			fF/um2	1.03		1.03		Vrev=0V		
Inverter FO=1 Delay	Wn/Wp=3.5 /5	0.279	ps/gate	24.98		-2.38		RO_Td(ring oscillator delay time) @ V=Vdd (Fan_out=1)		

## 13.11 Key Parameters for Bipolar

### 13.11.1 CLN90G

The following table summarizes the key parameters for bipolar in CLN90G process.

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.6505	0.6564	0.6467
	beta	1.2684	1.0973	1.4311
PNP5	Vbe	0.6503	0.6565	0.6462
	beta	1.3480	1.1886	1.4911
PNP2	Vbe	0.6442	0.6507	0.6399
	beta	1.7434	1.5559	1.9051

Vbe : VB=VC=0, IE=0.01uA\*Area

Beta : VB=VC=0, IE=0.01uA\*Area

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6405	0.6475	0.6358
	beta	3.5925	3.2224	3.9061
NPN5	Vbe	0.6373	0.6443	0.6325
	beta	3.9733	3.5883	4.2915
NPN2	Vbe	0.6323	0.6396	0.6273
	beta	5.1686	4.7673	5.4716

Vbe : VB=VC=0, IE=-0.01uA\*Area

Beta : VB=VC=0, IE=-0.01uA\*Area

### 13.11.2 CLN90GT

The following table summarizes the key parameters for bipolar in CLN90GT process.

Device	Parameter	TT	SS	FF	Device	Parameter	TT	SS	FF
PNP5	Vbe (V)	0.6865	0.6958	0.6793	NPN5	Vbe (V)	0.6733	0.6835	0.6654
	Beta	1.3718	1.1869	1.5539		Beta	4.1254	3.6162	4.6208

Vbe : VB=VC=0, IE=1uA

Beta : VB=VC=0, IE=1uA

### 13.11.3 CLN90LP

The following table summarizes the key parameters for bipolar in CLN90LP process.

Device	Parameter	TT	SS	FF
PNP10	Vbe	-0.6524	-0.6582	-0.6486
	beta	1.2588	1.0887	1.4206
PNP5	Vbe	0.6494	0.6553	0.6454
	beta	1.3914	1.2060	1.5669
PNP2	Vbe	-0.6453	-0.6516	-0.6411
	beta	1.8569	1.6213	2.0749

Vbe : VB=VC=0 , IE=-1e-8A\*area

Beta : VB=VC=0 , IE=-1e-8A\*area

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6400	0.6470	0.6353
	beta	4.1957	3.6882	4.6556
NPN5	Vbe	0.6375	0.6445	0.6328
	beta	4.6336	4.0897	5.1204
NPN2	Vbe	0.6314	0.6386	0.6264
	beta	5.5897	5.1059	5.9718

Vbe : VB=VC=0 , IE=1e-8A\*area

Beta : VB=VC=0 , IE=1e-8A\*area

## 13.11.4 CLN85G

The following table summaries the key parameters for bipolar in CLN85G process.

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.653	0.65875	0.64926
	beta	1.2015	1.0349	1.362
PNP5	Vbe	0.65131	0.65717	0.64747
	beta	1.3607	1.1719	1.5427
PNP2	Vbe	0.64664	0.65276	0.64258
	beta	1.6614	1.4394	1.8717

Vbe : VB=VC=0, IE=0.01uA\*Area

Beta : VB=VC=0, IE=0.01uA\*Area

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.64238	0.6493	0.63768
	beta	3.5513	3.1696	3.8803
NPN5	Vbe	0.64039	0.64746	0.63556
	beta	3.7852	3.4447	4.0581
NPN2	Vbe	0.63444	0.64175	0.62941
	beta	4.4301	4.1706	4.6026

Vbe : VB=VC=0, IE=-0.01uA\*Area

Beta : VB=VC=0, IE=-0.01uA\*Area

## 13.11.5 CLN85LP

The following table summaries the key parameters for bipolar in CLN85LP process.

Device	Parameter	TT	SS	FF
PNP10	Vbe	0.6534	0.6591	0.6498
	beta	1.2938	1.1024	1.4838
PNP5	Vbe	0.6513	0.6572	0.6475
	beta	1.4327	1.2292	1.6309
PNP2	Vbe	0.6458	0.652	0.6417
	beta	1.7983	1.5621	2.0202

Vbe : VB=VC=0, IE=0.01uA\*Area

Beta : VB=VC=0, IE=0.01uA\*Area

Device	Parameter	TT	SS	FF
NPN10	Vbe	0.6428	0.6497	0.6381
	beta	4.236	3.7359	4.6843
NPN5	Vbe	0.64	0.6471	0.6352
	beta	4.4402	4.049	4.7508
NPN2	Vbe	0.6336	0.6409	0.6286
	beta	4.9657	4.6771	5.1565

Vbe : VB=VC=0, IE=-0.01uA\*Area

Beta : VB=VC=0, IE=-0.01uA\*Area

## 13.11.6CLN80GC

The following table summaries the key parameters for bipolar in CLN80GC process.

Device	Parameter	TT	SS	FF
PNP5	Vbe (V)	0.6842	0.6896	0.6809
	Beta	0.9609	0.8186	1.1023

Device	Parameter	TT	SS	FF
NPN5	Vbe (V)	0.6753	0.6819	0.6709
	Beta	3.2962	2.8425	3.7313

Vbe : VB=VC=0V , IE=1uA

Beta: VB=VC=0V , IE=1uA

## 13.11.7CLN80GT

The following table summaries the key parameters for bipolar in CLN80GT process.

Device	Parameter	TT	SS	FF
PNP5	Vbe (V)	0.6838	0.6926	0.6771
	Beta	0.9300	0.7950	1.0717

Vbe : VB=VC=0, IE=1uA

Beta : VB=VC=0, IE=1uA

## 13.11.8CLN80HS

The following table summaries the key parameters for bipolar in CLN80HS process.

Device	Parameter	TT	SS	FF
PNP5	Vbe (V)	0.6852	0.6938	0.6787
	Beta	0.8068	0.6873	0.9260

Vbe : VB=VC=0, IE=1uA

Beta : VB=VC=0, IE=1uA

## 13.11.9CLN80LP

The following table summaries the key parameters for bipolar in CLN80LP process.

Device	Parameter	TT	SS	FF	Device	Parameter	TT	SS	FF
PNP5	Vbe (V)	0.6807	0.6894	0.6740	NPN5	Vbe (V)	-0.6718	-0.6817	-0.6641
	Beta	0.8961	0.7650	1.0266		Beta	2.8960	2.5112	3.2735

Vbe : VB=VC=0, IE=1uA

Beta : VB=VC=0, IE=1uA

## 13.12 Key Parameters for Junction Diodes

### 13.12.1 CLN90G

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
1.0V_Standard_Vt	N+/PW	9.800E-04	4.00E-11	3.70E-10	10.1	1.02	1.00E-10	1.770E-07	4.23E-13
	P+/NW	1.140E-03	6.00E-11	3.60E-10	9.3	1.02	1.00E-10	1.245E-07	3.77E-13
	NW/Psub	1.350E-04	8.73E-10	NA	11.7	1.02	4.80E-10	8.900E-07	8.40E-13
1.0V_High_Vt	N+/PW	1.090E-03	2.00E-11	4.20E-10	10.2	1.02	1.00E-10	2.000E-07	6.71E-13
	P+/NW	1.170E-03	6.00E-11	4.10E-10	9.4	1.02	1.00E-10	1.500E-07	5.60E-13
1.0V_Low_Vt	N+/PW	9.870E-04	3.50E-11	3.38E-10	10.1	1.02	1.00E-10	1.930E-07	3.40E-13
	P+/NW	1.129E-03	5.80E-11	3.05E-10	9.3	1.02	1.00E-10	1.560E-07	3.47E-13
2.5V	N+/PW	1.080E-03	8.25E-11	1.89E-10	9.8	1.02	1.00E-10	1.800E-07	7.50E-13
	P+/NW	1.080E-03	6.80E-11	1.88E-10	9.5	1.02	1.00E-10	1.500E-07	5.00E-13
1.0V_Native	N+/PW	1.440E-04	1.60E-10	1.39E-10	23	1.02	1.00E-10	9.000E-07	1.50E-12
2.5V_Native	N+/PW	1.240E-04	1.83E-10	1.04E-10	21.8	1.03	1.50E-10	1.300E-06	3.20E-12
DNW	DNWPSUB	1.370E-04	1.10E-09	NA	11.6	1.02	4.80E-10	1.000E-06	8.70E-13
	PWDNW	8.700E-04	7.10E-10	NA	10.4	1.02	2.00E-10	7.400E-07	8.70E-13
ESD	N+/PW	2.090E-03	1.32E-10	NA	5.9	1.02	1.00E-10	1.000E-07	1.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m<sup>2</sup>).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

## 13.12.2 CLN90GT

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
1.2V Standard Vt	N+/PW	9.81E-04	5.80E-11	3.57E-10	10.9	1.02	1.0E-10	2.36E-07	5.12E-13
	P+/NW	1.12E-03	7.10E-11	3.15E-10	9.7	1.02	1.0E-10	1.29E-07	4.10E-13
1.2V High Vt	N+/PW	1.03E-03	5.20E-11	3.87E-10	10.2	1.02	1.0E-10	2.00E-07	6.71E-13
	P+/NW	1.12E-03	7.20E-11	3.56E-10	9.5	1.02	1.0E-10	1.20E-07	3.90E-13
1.2V Low Vt	N+/PW	9.81E-04	5.80E-11	3.57E-10	10.9	1.02	1.0E-10	2.36E-07	5.12E-13
	P+/NW	1.12E-03	7.10E-11	3.15E-10	9.7	1.02	1.0E-10	1.29E-07	4.10E-13
1.8V Standard Vt	N+/PW	9.66E-04	5.42E-11	2.90E-10	10.5	1.01	1.0E-10	2.85E-07	6.90E-13
	P+/NW	1.08E-03	7.00E-11	3.09E-10	9.8	1.01	1.0E-10	1.90E-07	1.00E-12
2.5V Standard Vt	N+/PW	1.08E-03	8.25E-11	1.89E-10	10.6	1.02	1.0E-10	2.43E-07	4.85E-13
	P+/NW	1.08E-03	6.80E-11	1.88E-10	9.5	1.02	1.0E-10	1.50E-07	5.00E-13
1.2V Native	N+/Psub	1.44E-04	1.60E-10	1.39E-10	23.0	1.02	1.0E-10	9.00E-07	1.50E-12
1.8V Native	N+/Psub	1.42E-04	2.54E-10	1.08E-10	21.0	1.02	1.0E-10	1.00E-06	2.00E-12
2.5V Native	N+/Psub	1.24E-04	1.83E-10	1.04E-10	21.8	1.03	1.5E-10	1.30E-06	3.20E-12
NW	NW/Psub	1.35E-04	8.73E-10	-	11.7	1.02	4.8E-10	8.90E-07	8.40E-13
DNW	DNWPSUB	1.37E-04	1.10E-09	-	11.6	1.02	4.8E-10	1.00E-06	8.70E-13
	PWDNW	8.70E-04	7.10E-10	-	10.4	1.02	2.0E-10	7.40E-07	8.70E-13
ESD	N+/PW	2.09E-03	1.32E-10	-	5.9	1.02	1.0E-10	1.00E-07	1.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

CJ = Area component of junction capacitance (F/m<sup>2</sup>).

CJSW = STI perimeter component of junction capacitance (F/m).

CJSWG = Gate perimeter component of junction capacitance (F/m).

BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).

N, RS, IS, and ISW are forward bias related diode parameters.

### 13.12.3 CLN90LP

Device	Junction	CJ (F/m <sup>2</sup> )	CJSW (F/m)	CJSWG (F/m)	BV V	N	RS ohm/m <sup>2</sup>	IS A/m <sup>2</sup>	ISW A/m
1.2V_SVT	NDIO	9.81E-04	5.50E-11	2.73E-10	9.8	1.02	1.0E-10	2.00E-07	3.50E-13
	PDIO	1.09E-03	6.40E-11	2.41E-10	9.2	1.02	1.0E-10	1.40E-07	4.20E-13
	NWDIO	1.35E-04	8.73E-10	NA	11.7	1.02	4.8E-10	8.90E-07	8.40E-13
1.2V_HVT	NDIO	1.06E-03	4.40E-11	3.27E-10	9.9	1.00	1.0E-10	1.62E-07	4.40E-13
	PDIO	1.12E-03	6.40E-11	3.14E-10	9.1	1.00	1.0E-10	1.00E-07	3.20E-13
1.2V_LVT	NDIO	9.81E-04	5.50E-11	2.73E-10	9.8	1.02	1.0E-10	2.00E-07	3.50E-13
	PDIO	1.09E-03	6.40E-11	2.41E-10	9.2	1.02	1.0E-10	1.40E-07	4.20E-13
1.2V_ULVT	NDIO	9.59E-04	5.33E-11	2.65E-10	10.4	1.02	1.0E-10	2.90E-07	1.58E-12
	PDIO	1.09E-03	4.51E-11	1.70E-10	9.7	1.02	1.0E-10	1.53E-07	8.00E-13
3.30V	NDIO	9.62E-04	1.38E-10	2.48E-10	10.7	1.02	1.0E-10	4.10E-07	1.55E-12
	PDIO	1.04E-03	7.00E-11	1.53E-10	9.8	1.02	1.0E-10	3.60E-07	1.60E-12
1.2V_Native	NDIO	1.39E-04	1.59E-10	2.16E-10	17.5	1.02	1.0E-10	6.45E-07	1.04E-12
3.3V_Native	NDIO	1.39E-04	1.97E-10	1.26E-10	20.7	1.02	1.0E-10	9.00E-07	1.50E-12
DNW	DNWPSUB	1.37E-04	1.10E-09	NA	11.6	1.02	4.8E-10	1.00E-06	8.70E-13
	PWDNW	7.60E-04	7.50E-10	NA	11.8	1.02	2.0E-10	2.40E-07	6.00E-13
ESD	NDIO	2.09E-03	1.32E-10	NA	5.9	1.02	1.0E-10	1.00E-07	1.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJA = Area component of junction capacitance (F/m<sup>2</sup>).
- CJSW = STI perimeter component of junction capacitance (F/m).
- CJSWG = Gate perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V)

## 13.12.4CLN85G

Device	Junction	CJ (F/m <sup>2</sup> )	CJSW (F/m)	CJSWG (F/m)	BV V	N	RS ohm/m <sup>2</sup>	IS A/m <sup>2</sup>	ISW A/m
1.0V_Standard_Vt	<b>N+/PW</b>	1.023E-03	4.37E-11	3.70E-10	10.4	1.02	1.00E-10	4.500E-07	1.20E-12
	<b>P+/NW</b>	1.080E-03	5.52E-11	4.79E-10	9.7	1.02	1.00E-10	1.800E-07	7.00E-13
	<b>NW/Psub</b>	1.382E-04	8.68E-10	NA	11.7	1.02	4.80E-10	9.200E-07	1.08E-12
1.0V_High_Vt	<b>N+/PW</b>	1.177E-03	4.92E-11	4.20E-10	10.4	1.02	1.00E-10	4.200E-07	1.50E-12
	<b>P+/NW</b>	1.110E-03	5.24E-11	4.99E-10	9.6	1.02	1.00E-10	1.500E-07	7.50E-13
1.0V_Low_Vt	<b>N+/PW</b>	1.004E-03	4.30E-11	3.38E-10	10.5	1.02	1.00E-10	3.800E-07	1.10E-12
	<b>P+/NW</b>	1.082E-03	4.44E-11	4.31E-10	9.6	1.02	1.00E-10	1.400E-07	5.00E-13
3.3V	<b>N+/PW</b>	9.620E-04	1.38E-10	2.48E-10	10.65	1.02	1.00E-10	4.100E-07	1.55E-12
	<b>P+/NW</b>	1.040E-03	7.00E-11	1.53E-10	9.8	1.02	1.00E-10	4.000E-07	1.60E-12
1.0V_Native	<b>N+/PW</b>	1.440E-04	1.76E-10	1.64E-10	19.3	1.02	1.00E-10	1.000E-06	1.20E-12
3.3V_Native	<b>N+/PW</b>	1.370E-04	2.32E-10	1.43E-10	17.3	1.02	1.00E-10	1.200E-06	2.00E-12
DNW	<b>DNWPSUB</b>	1.170E-04	1.10E-09	NA	11.5	1.02	4.80E-10	1.000E-06	8.70E-13
	<b>PWDNW</b>	7.830E-04	6.93E-10	NA	11.9	1.02	2.00E-10	2.270E-07	4.30E-13
ESD	<b>N+/PW</b>	2.090E-03	1.32E-10	NA	5.9	1.02	1.00E-10	1.000E-07	1.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m<sup>2</sup>).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

## 13.12.5 CLN85LP

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
1.2V_Standard_Vt	N+/PW	9.810E-04	5.50E-11	2.73E-10	10.4	1.02	1.00E-10	1.400E-07	5.00E-13
	P+/NW	1.090E-03	6.40E-11	3.29E-10	9.6	1.02	1.00E-10	1.050E-07	4.50E-13
	NW/Psub	1.270E-04	8.95E-10	NA	11.5	1.02	4.80E-10	8.900E-07	9.00E-13
1.2V_High_Vt	N+/PW	9.870E-04	5.47E-11	3.27E-10	10.4	1.02	1.00E-10	4.000E-07	4.00E-12
	P+/NW	1.090E-03	5.66E-11	4.04E-10	9.6	1.02	1.00E-10	1.200E-07	1.00E-12
1.2V_Low_Vt	N+/PW	9.570E-04	4.54E-11	2.73E-10	10.4	1.02	1.00E-10	1.400E-07	5.00E-13
	P+/NW	1.090E-03	5.15E-11	3.29E-10	9.6	1.02	1.00E-10	1.050E-07	4.50E-13
1.2V_Ultra Low_Vt	N+/PW	9.542E-04	4.93E-11	2.65E-10	10.5	1.02	1.00E-10	3.600E-07	2.00E-12
	P+/NW	1.067E-03	5.25E-11	1.70E-10	9.7	1.02	1.00E-10	1.400E-07	8.50E-13
3.3V	N+/PW	9.620E-04	1.38E-10	2.48E-10	10.65	1.02	1.00E-10	4.100E-07	1.55E-12
	P+/NW	1.040E-03	7.38E-11	2.21E-10	9.8	1.02	1.00E-10	4.300E-07	9.80E-13
1.2V_Native	N+/PW	1.496E-04	1.82E-10	2.11E-10	18.5	1.02	1.00E-10	1.600E-06	7.00E-12
3.3V_Native	N+/PW	1.377E-04	2.38E-10	1.58E-10	17	1.02	1.00E-10	1.800E-06	6.00E-12
DNW	DNWPSUB	1.170E-04	1.10E-09	NA	11.5	1.02	4.80E-10	1.000E-06	8.70E-13
	PWDNW	7.700E-04	7.30E-10	NA	11.9	1.02	2.00E-10	1.800E-07	4.00E-13
ESD	N+/PW	2.090E-03	1.32E-10	NA	5.9	1.02	1.00E-10	1.000E-07	1.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

- CJ = Area component of junction capacitance (F/m<sup>2</sup>).
- CJSW = STI perimeter component of junction capacitance (F/m).
- BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).
- N, RS, IS, and ISW are forward bias related diode parameters.

## 13.12.6CLN80GC

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
1.0V Standard Vt	<b>N+/PW</b>	1.02E-03	6.38E-11	2.98E-10	10.3	1.01	1.0E-10	1.60E-07	8.50E-13
	<b>P+/NW</b>	9.88E-04	8.38E-11	3.19E-10	10.3	1.01	1.0E-10	1.60E-07	2.50E-13
1.0V High Vt	<b>N+/PW</b>	1.09E-03	6.62E-11	3.42E-10	10.5	1.01	1.0E-10	1.30E-07	3.50E-13
	<b>P+/NW</b>	9.82E-04	8.31E-11	3.66E-10	10.1	1.01	1.0E-10	1.20E-07	2.00E-13
1.0V Low Vt	<b>N+/PW</b>	9.78E-04	7.08E-11	3.00E-10	10.6	1.01	1.0E-10	1.50E-07	3.40E-13
	<b>P+/NW</b>	9.86E-04	8.36E-11	3.64E-10	10.1	1.01	1.0E-10	1.36E-07	2.70E-13
1.0V Ultra Low Vt	<b>N+/PW</b>	9.19E-04	7.35E-11	3.17E-10	10.8	1.01	1.00E-10	1.38E-07	2.00E-13
	<b>P+/NW</b>	9.78E-04	8.63E-11	3.37E-10	10.2	1.01	1.00E-10	1.05E-07	1.70E-13
2.5V	<b>N+/PW</b>	1.01E-03	1.22E-10	2.46E-10	10.3	1.02	1.0E-10	1.60E-07	8.50E-13
	<b>P+/NW</b>	1.02E-03	9.30E-11	2.70E-10	9.9	1.01	1.0E-10	7.0E-07	9.00E-14
1.0V Native	<b>N+/Psub</b>	1.46E-04	2.07E-10	1.31E-10	17.0	1.01	1.0E-10	7.00E-07	1.50E-12
2.5V Native	<b>N+/Psub</b>	1.41E-04	2.24E-10	1.30E-10	17.0	1.01	1.0E-10	7.00E-07	9.00E-13
NW	<b>NW/Psub</b>	1.33E-04	9.30E-10	---	11.6	1.01	1.0E-10	8.00E-07	8.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

CJ = Area component of junction capacitance (F/m<sup>2</sup>).

CJSW = STI perimeter component of junction capacitance (F/m).

CJSWG = Gate perimeter component of junction capacitance (F/m).

BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).

N, RS, IS, and ISW are forward bias related diode parameters.

## 13.12.7 CLN80GT

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
<b>1.2V Standard Vt</b>	<b>N+/PW</b>	1.01E-03	5.90E-11	3.38E-10	10.6	1.02	1.0E-10	2.38E-07	8.20E-13
	<b>P+/NW</b>	1.00E-03	7.70E-11	2.49E-10	10.0	1.02	1.0E-10	1.08E-07	5.20E-13
<b>1.2V High Vt</b>	<b>N+/PW</b>	1.01E-03	5.90E-11	3.56E-10	10.6	1.02	1.0E-10	2.38E-07	8.21E-13
	<b>P+/NW</b>	1.00E-03	7.70E-11	2.94E-10	10.0	1.02	1.0E-10	1.10E-07	5.20E-13
<b>1.8V Standard Vt</b>	<b>N+/PW</b>	9.20e-04	5.10e-11	2.820E-10	10.8	1.02	1.0E-10	1.25E-07	6.00E-13
	<b>P+/NW</b>	1.017e-03	7.80e-11	2.820E-10	10.0	1.02	1.0E-10	0.8E-07	4.00E-13
<b>2.5V Standard Vt</b>	<b>N+/PW</b>	9.99E-04	1.07E-10	1.99E-10	10.4	1.02	1.0E-10	1.80E-07	1.15E-12
	<b>P+/NW</b>	1.03E-03	7.50E-11	1.87E-10	9.9	1.02	1.0E-10	1.70E-07	7.00E-13
<b>1.2V Native</b>	<b>N+/Psub</b>	1.54E-04	1.90E-10	1.50E-10	18.5	1.02	1.0E-10	7.36E-07	1.08E-12
<b>1.8V Native</b>	<b>N+/Psub</b>	1.52E-04	1.92E-10	1.59E-10	17.4	1.02	1.0E-10	6.10E-07	1.29E-12
<b>2.5V Native</b>	<b>N+/Psub</b>	1.52E-04	1.92E-10	1.59E-10	17.4	1.02	1.0E-10	6.10E-07	1.29E-12
<b>NW</b>	<b>NW/Psub</b>	1.25E-04	8.99E-10	-	11.5	1.02	1.0E-10	6.82E-07	7.80E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

CJ = Area component of junction capacitance (F/m<sup>2</sup>).

CJSW = STI perimeter component of junction capacitance (F/m).

CJSWG = Gate perimeter component of junction capacitance (F/m).

BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).

N, RS, IS, and ISW are forward bias related diode parameters.

## 13.12.8 CLN80HS

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
<b>1.05V Standard Vt</b>	<b>N+/PW</b>	9.590E-04	9.80E-11	3.17E-10	10.7	1.02	1.00E-10	1.080E-07	1.68E-13
	<b>P+/NW</b>	9.620E-04	7.50E-11	2.17E-10	10.2	1.02	1.00E-10	1.070E-07	2.00E-13
<b>1.05V High Vt</b>	<b>N+/PW</b>	9.590E-04	9.80E-11	3.50E-10	10.75	1.02	1.00E-10	1.500E-07	3.00E-13
	<b>P+/NW</b>	9.620E-04	7.50E-11	2.75E-10	10.25	1.02	1.00E-10	1.300E-07	5.00E-13
<b>1.05V Low Vt</b>	<b>N+/PW</b>	9.590E-04	9.80E-11	2.86E-10	10.7	1.02	1.00E-10	1.760E-07	2.38E-13
	<b>P+/NW</b>	9.620E-04	7.50E-11	1.92E-10	10.2	1.02	1.00E-10	1.660E-07	3.20E-13
<b>1.8V Standard Vt</b>	<b>N+/PW</b>	8.770E-04	8.33E-11	2.87E-10	11.1	1.02	1.00E-10	1.050E-07	2.85E-13
	<b>P+/NW</b>	9.810E-04	6.50E-11	2.70E-10	10.1	1.02	1.00E-10	1.060E-07	3.30E-13
<b>2.5V Standard Vt</b>	<b>N+/PW</b>	1.03E-03	1.05E-10	2.14E-10	10.2	1.02	1.0E-10	1.30E-07	6.00E-13
	<b>P+/NW</b>	9.88E-04	7.00E-11	1.91E-10	10.0	1.03	1.0E-10	1.60E-07	6.00E-13
<b>1.05V Native</b>	<b>N+/Psub</b>	1.560E-04	1.95E-10	1.48E-10	17	1.02	1.00E-10	7.360E-07	1.08E-12
<b>1.8V Native</b>	<b>N+/Psub</b>	1.540E-04	1.99E-10	2.18E-10	17	1.02	1.00E-10	5.920E-07	1.01E-12
<b>2.5V Native</b>	<b>N+/Psub</b>	1.47E-04	2.11E-10	2.87E-10	16.9	1.02	1.0E-10	8.74E-07	1.24E-12
<b>NW</b>	<b>NW/Psub</b>	1.110E-04	7.72E-10	-	12	1.01	1.00E-10	5.480E-07	6.20E-13
<b>DNW</b>	<b>DNWPSUB</b>	1.310E-04	1.39E-09	-	11.6	1.02	1.00E-10	9.000E-07	7.45E-12
	<b>PWDNW</b>	7.960E-04	7.70E-10	-	12.1	1.02	1.00E-10	1.850E-07	4.90E-13
<b>ESD</b>	<b>N+/PW</b>	2.270E-03	1.11E-10	-	5.4	1.02	1.00E-10	1.000E-07	1.00E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

CJ = Area component of junction capacitance (F/m<sup>2</sup>).

CJSW = STI perimeter component of junction capacitance (F/m).

CJSWG = Gate perimeter component of junction capacitance (F/m).

BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).

N, RS, IS, and ISW are forward bias related diode parameters.

## 13.12.9 CLN80LP

Device	Junction	CJ	CJSW	CJSWG	BV	N	RS	IS	ISW
		(F/m <sup>2</sup> )	(F/m)	(F/m)	V		ohm/m <sup>2</sup>	A/m <sup>2</sup>	A/m
<b>1.2V Standard Vt</b>	<b>N+/PW</b>	1.09E-03	7.11E-11	2.91E-10	10.8	1.02	1.0E-10	1.83E-07	4.27E-13
	<b>P+/NW</b>	9.84E-04	7.30E-11	2.94E-10	10.3	1.02	1.0E-10	1.41E-07	3.40E-13
<b>1.2V High Vt</b>	<b>N+/PW</b>	1.31E-03	9.32E-11	3.38E-10	10.6	1.02	1.0E-10	1.94E-07	4.69E-13
	<b>P+/NW</b>	9.76E-04	6.90E-11	3.69E-10	10.3	1.02	1.0E-10	1.35E-07	3.65E-13
<b>2.5V Standard Vt</b>	<b>N+/PW</b>	1.00E-03	1.03E-10	1.98E-10	10.1	1.02	1.0E-10	2.10E-07	6.30E-13
	<b>P+/NW</b>	1.01E-03	7.30E-11	1.81E-10	10.1	1.02	1.0E-10	1.66E-07	4.75E-13
<b>NW</b>	<b>NW/Psub</b>	1.04E-04	7.72E-10	-	11.6	1.02	1.0E-10	9.18E-07	1.22E-12
<b>DNW</b>	<b>DNWPSUB</b>	1.21E-04	1.30E-09	-	11.6	1.02	1.0E-10	8.49E-07	4.45E-12
	<b>PWDNW</b>	7.60E-04	7.50E-10	-	11.9	1.02	1.0E-10	1.85E-07	4.90E-13

The area and perimeter components of junction capacitance listed in the table are at V=0 and T=25C.

CJ = Area component of junction capacitance (F/m<sup>2</sup>).

CJSW = STI perimeter component of junction capacitance (F/m).

CJSWG = Gate perimeter component of junction capacitance (F/m).

BV = Reverse-Biased Breakdown Voltage of STI-Bounded Junction (V).

N, RS, IS, and ISW are forward bias related diode parameters.

## 13.13 Resistor Model

This section does not include unsilicided N+/P+ Poly resistors. Please refer to next section for the electrical parameters of unsilicided poly resistor devices.

The following table lists the resistor model names and valid dimension ranges. The resistor model has a nominal temperature of 25 °C and a valid temperature range is from -40 °C through 125 °C. Each model contains one typical case (TT\_RES) and two corner cases, slow (SS\_RES) and fast (FF\_RES).

Except for unsilicided N+/P+ Poly resistors, most resistors were measured by applying voltages on one node, while grounding the other node and the substrate (if a connection was available). The voltage sweep was performed from 0V through +/- 3.3 V (provided there was no reliability issue). Most of the resistance data measurements were obtained using equation (1):

$$R(T, V) = R_0 \cdot (1 + TC1 \cdot \delta T + TC2 \cdot \delta T^2) \cdot (1 + VC1 \cdot \delta V + VC2 \cdot \delta V^2) \quad \text{equation (1)}$$

where

- $\delta T$  =  $T - 25^\circ\text{C}$
- $\delta V$  (in volt) = the voltage drop across the resistor
- $L$  = the length of the resistor

$R_0$  of equation 1 is the resistance value at 25 °C and at an infinitesimal applied voltage.  $R_0$  is related to sheet resistance,  $R_s$ :  $R_0 = R_s \cdot L / (W - \delta W)$  equation (2)

where

- $W$  = the layout drawn width
- $L$  = the layout drawn length
- $\delta W$  = the width offset

The following tables list the median sheet resistance values and their corresponding variations, temperature coefficients, and voltage coefficients in CLN90G/GT/LP process. The data was extracted based on the methodology described previously in this section.

*Note: An NW diffusion resistor under STI is subject to CMP variation. It is recommended that designers use an NW diffusion resistor under OD for their designs.*

### 13.13.1 CLN90G Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	90.06	ohm/sq	0.027u	-2.96E-01	-8.04E-06	-2.45E+00	1.51E-03	1.10E-06
		Rend0	8.46u	ohm.m	-	-6.89E-02	1.12E+03	-1.82E-01	1.25E-03	2.50E-06
rpodwo	P+OD w/o silicide resistor	Rsh	152.05	ohm/sq	0.0307u	-3.89E-01	-1.73E-06	-2.10E+00	1.11E-03	4.14E-06
		Rend0	29.5u	ohm.m	-	3.50E-02	2.59E+02	-9.92E-02	-1.00E-03	2.00E-06
rnpolywo	N+POLY w/o silicide resistor	Rsh	88.15	ohm/sq	0.106u	-7.88E-01	-9.80E-05	-2.45E+00	1.79E-04	-5.44E-07
		Rend0	14.4u	ohm.m	-	-2.27E-02	6.54E+02	7.66E-01	3.00E-03	8.00E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	399.55	ohm/sq	0.0809u	1.10E-03	-2.69E-05	2.96E+00	-1.94E-04	1.01E-06
		Rend0	86.7u	ohm.m	-	1.04E-02	-7.22E+00	1.72E-01	-8.00E-04	-5.00E-06
rppoly1	P+POLY silicide resistor (W>=2um)	Rsh	11.29	ohm/sq	0.0035u	2.40E-06	8.00E-13	-	2.85E-03	2.17E-07
rppolys	P+POLY silicide resistor (W<2um)	Rsh	11.29	ohm/sq	0.0035u	4.20E-07	2.00E-12	-	3.08E-03	6.70E-07
rnpoly1	N+POLY silicide resistor (W>=2um)	Rsh	10.90	ohm/sq	0.0152u	2.40E-06	1.00E-12	-	2.75E-03	-1.00E-06
rnpolys	N+POLY silicide resistor (W<2um)	Rsh	10.90	ohm/sq	0.0152u	5.00E-07	1.90E-12	-	3.18E-03	1.20E-06
rnodl	N+OD silicide resistor (W>=2um)	Rsh	10.94	ohm/sq	-0.0012u	3.66E-07	1.99E-12	-	3.02E-03	0.00E+00
rnodes	N+OD silicide resistor (W<2um)	Rsh	10.94	ohm/sq	-0.0012u	1.36E-07	7.63E-13	3.31E-03	9.00E-07	0.00E+00
rpodi1	P+OD silicide resistor (W>=2um)	Rsh	10.12	ohm/sq	0.002u	3.95E-07	2.22E-12	-	3.19E-03	0.00E+00
rpodi2	P+OD silicide resistor (W<2um)	Rsh	10.12	ohm/sq	0.002u	1.57E-07	7.82E-13	-	3.42E-03	7.34E-07
rnwod	N-Well under OD resistor	Rsh	330	ohm/sq	0.29u	1.10E-02	2.98E-06	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	546	ohm/sq	0.41u	9.60E-03	1.00E-07	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	700	ohm/sq	-	1.53E-02	-7.81E-04	-	2.43E-03	9.49E-06
-	DNW under STI	Rsh	600	ohm/sq	-	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	-	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	-	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.12/0.36	Rsh	0.0736	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm1s	Metal 1 with W/S=0.12/0.12	Rsh	0.1	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.0894	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm2l	Metal 2 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm2s	Metal 2 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm2w	Metal 2 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3l	Metal 3 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3s	Metal 3 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3w	Metal 3 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4l	Metal 4 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4s	Metal 4 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4w	Metal 4 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5l	Metal 5 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5s	Metal 5 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5w	Metal 5 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6l	Metal 6 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6s	Metal 6 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6w	Metal 6 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7l	Metal 7 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7s	Metal 7 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7w	Metal 7 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm8l	Metal 8 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm8s	Metal 8 with W/S=0.42/0.42	Rsh	0.0221	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm8w	Metal 8 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9l	Metal 9 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9s	Metal 9 with W/S=0.42/0.42	Rsh	0.0221	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9w	Metal 9 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm10l	Metal 10 with W/S=3/4.5	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=3/2	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=3/1.5	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
-	RC_N+ (W/S=0.12/0.14)		18.0	ohm/ct	0	0.00	0.00	-	1.08E-03	5.92E-07
-	RC_P+ (W/S=0.12/0.14)		16.9	ohm/ct	0	0.00	0.00	-	1.05E-03	1.02E-07
-	RC_PO(N+) (W/S=0.12/0.14)		15.2	ohm/ct	0	0.00	0.00	-	1.03E-03	1.63E-07
-	RC PO(P+) (W/S=0.12/0.14)		15.0	ohm/ct	0	0.00	0.00	-	1.11E-03	4.23E-07
-	RC_VIA1 (W/S=0.13/0.15)		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA2 (W/S=0.13/0.15)		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA3 (W/S=0.13/0.15)		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA4 (W/S=0.13/0.15)		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA5 (W/S=0.13/0.15)		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA6 (W/S=0.13/0.15)		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA7 (W/S=0.36/0.34)		0.412	ohm/ct	0	0.00	0.00	-	2.56E-03	-1.38E-07
-	RC_VIA8 (W/S=0.36/0.34)		0.349	ohm/ct	0	0.00	0.00	-	2.56E-03	-1.38E-07
-	RC_VIA9 (W/S=3/3)		0.041	ohm/ct	0	0.00	0.00	-	3.37E-03	-7.91E-08

### 13.13.1.1 Silicide Rs

Rs	W	L	PCM target	Simulation (Rs/corner)
N+OD	0.11	50	10.8	10.82/35%/-35%
	0.44	50	-	10.91/21%/-23%
	2	50	-	10.94/15%/-15%
P+OD	0.11	50	10.3	10.31/35%/-35%
	0.44	50	-	10.16/20%/-22%
	2	50	-	10.14/15%/-15%
N+PO	0.1	50	12.9	12.87/30%/-30%
	0.4	50	-	11.34/19%/-15%
	2	50	-	11.04/20%/-20%
P+PO	0.1	50	11.4	11.71/40%/-40%
	0.4	50	-	11.39/26%/-27%
	2	50	-	11.36/20%/-20%

### 13.13.1.2 Non-Silicide Rs

Rs	W	L	PCM target	Simulation (Rs/corner)
N+OD(PRO)	0.44	50	-	96.27/19%/-16%
	2	50	91.6	91.64/10%/-10%
P+OD(RPO)	0.44	50	-	164.74/15%/-14%
	2	50	156	155.60/10%/-10%
N+PO(RPO)	0.4	50	-	121.12/21%/-17%
	2	50	94	94.04/10%/-10%
P+PO(RPO)	0.4	50	-	505.12/21%/-17%
	2	50	420	420.00/10%/-10%

## 13.13.2CLN90GT Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	92.99	ohm/sq	0.027u	-2.96E-01	-8.04E-06	-2.45E+00	1.51E-03	1.10E-06
		Rend0	8.46u	ohm.m	0	-6.89E-02	1.12E+03	-1.82E-01	1.25E-03	2.50E-06
rpodwo	P+OD w/o silicide resistor	Rsh	152.56	ohm/sq	0.0307u	-3.89E-01	-1.73E-06	-2.10E+00	1.11E-03	4.14E-06
		Rend0	29.5u	ohm.m	0	3.50E-02	2.59E+02	-9.92E-02	-1.00E-03	2.00E-06
rnpolywo	N+POLY w/o silicide resistor	Rsh	89.62	ohm/sq	0.0936u	-7.88E-01	-9.80E-05	-2.45E+00	1.79E-04	-5.44E-07
		Rend0	14.4u	ohm.m	0	-2.27E-02	-6.54E+02	7.66E-01	3.00E-03	8.00E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	402.1	ohm/sq	0.0689u	1.10E-03	-2.69E-05	2.96E+00	-1.94E-04	1.01E-06
		Rend0	86.7u	ohm.m	0	1.04E-02	-7.22E+00	1.72E-01	-8.00E-04	-5.00E-06
rppoly1	P+POLY silicide resistor (W>=2um)	Rsh	10.74	ohm/sq	0.0124u	2.32E-06	5.71E-12	-	2.74E-03	-1.41E-07
rppolys	P+POLY silicide resistor (W<2um)	Rsh	10.74	ohm/sq	0.0124u	1.82E-06	1.23E-12	-	3.08E-03	-1.39E-06
rnpoly1	N+POLY silicide resistor (W>=2um)	Rsh	10.38	ohm/sq	0.0243u	3.04E-06	3.35E-12	-	2.56E-03	-4.21E-07
rnpolys	N+POLY silicide resistor (W<2um)	Rsh	10.38	ohm/sq	0.0243u	1.51E-06	1.13E-12	-	3.12E-03	-1.91E-06
rnodl	N+OD silicide resistor (W>=2um)	Rsh	10.5	ohm/sq	0.0032u	4.91E-07	1.99E-12	-	2.85E-03	-2.29E-06
rnodes	N+OD silicide resistor (W<2um)	Rsh	10.5	ohm/sq	0.0032u	4.77E-07	7.63E-13	-	3.10E-03	3.96E-07
rpodl	P+OD silicide resistor (W>=2um)	Rsh	9.68	ohm/sq	0.0066u	4.53E-07	2.22E-12	-	2.63E-03	-9.56E-07
rpods	P+OD silicide resistor (W<2um)	Rsh	9.68	ohm/sq	0.0066u	6.04E-07	7.82E-13	-	3.25E-03	-4.18E-07
rnwod	N-Well under OD resistor	Rsh	330	ohm/sq	0.29u	1.24E-02	-2.98E-04	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	550	ohm/sq	0.41u	1.16E-02	-4.57E-04	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	780	ohm/sq	0	1.68E-02	-9.68E-04	-	2.50E-03	1.03E-05
-	DNW under STI	Rsh	600	ohm/sq	0	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	0	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	0	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.12/0.36	Rsh	0.0736	ohm/sq	0	0	0	-	2.92E-03	-1.22E-07
rm1s	Metal 1 with W/S=0.12/0.12	Rsh	0.1	ohm/sq	0	0	0	-	2.92E-03	-1.22E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.0894	ohm/sq	0	0	0	-	2.92E-03	-1.22E-07
rm2l	Metal 2 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm2s	Metal 2 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm2w	Metal 2 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm3l	Metal 3 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm3s	Metal 3 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm3w	Metal 3 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm4l	Metal 4 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm4s	Metal 4 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm4w	Metal 4 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm5l	Metal 5 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm5s	Metal 5 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm5w	Metal 5 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm6l	Metal 6 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm6s	Metal 6 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm6w	Metal 6 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm7l	Metal 7 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm7s	Metal 7 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm7w	Metal 7 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0	0	-	3.08E-03	-1.14E-07
rm8l	Metal 8 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0	0	-	3.51E-03	-3.60E-07
rm8s	Metal 8 with W/S=0.42/0.42	Rsh	0.0221	ohm/sq	0	0	0	-	3.51E-03	-3.60E-07
rm8w	Metal 8 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0	0	-	3.51E-03	-3.60E-07
rm9l	Metal 9 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0	0	-	3.51E-03	-3.60E-07
rm9s	Metal 9 with W/S=0.42/0.42	Rsh	0.0221	ohm/sq	0	0	0	-	3.51E-03	-3.60E-07
rm9w	Metal 9 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0	0	-	3.51E-03	-3.60E-07
rm10l	Metal 10 with W/S=3/4.5	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=3/2	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=3/1.5	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
-	RC_N+		17	ohm/ct	0	0	0	-	1.08E-03	5.92E-07
-	RC_P+		17	ohm/ct	0	0	0	-	1.05E-03	1.02E-07
-	RC_PO(N+)		14.5	ohm/ct	0	0	0	-	1.03E-03	1.63E-07
-	RC PO(P+)		14.5	ohm/ct	0	0	0	-	1.11E-03	4.23E-07
-	RC_VIA1		1.2	ohm/ct	0	0	0	-	1.36E-03	9.15E-08
-	RC_VIA2		1.2	ohm/ct	0	0	0	-	1.36E-03	9.15E-08
-	RC_VIA3		1.2	ohm/ct	0	0	0	-	1.36E-03	9.15E-08
-	RC_VIA4		1.2	ohm/ct	0	0	0	-	1.36E-03	9.15E-08
-	RC_VIA5		1.2	ohm/ct	0	0	0	-	1.36E-03	9.15E-08
-	RC_VIA6		1.2	ohm/ct	0	0	0	-	1.36E-03	9.15E-08
-	RC_VIA7		0.45	ohm/ct	0	0	0	-	2.56E-03	-1.38E-07
-	RC_VIA8		0.4	ohm/ct	0	0	0	-	2.56E-03	-1.38E-07
-	RC_VIA9		0.041	ohm/ct	0	0	0	-	3.37E-03	-7.91E-08

### 13.13.2.1 Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD	0.11	100	10.5	10.8/40.8%/-38.3%
	0.44	100	-	10.6/25.3%/-26.1%
	2	100	-	10.5/15.0%/-15.0%
P+OD	0.11	100	10	10.3/41.4%/-38.7%
	0.44	100	-	9.8/25.3%/-26.0%
	2	100	-	9.7/14.9%/-14.9%
N+PO	0.1	100	13.5	13.7/39.4%/-40.6%
	0.4	100	-	11.1/24.3%/-25.9%
	2	100	-	10.5/20.0%/-20.0%
P+PO	0.1	100	12.1	12.3/40.2%/-41.1%
	0.4	100	-	11.1/24.9%/-26.7%
	2	100	-	10.8/20.0%/-20.0%

### 13.13.2.2 Non-Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.44	100	-	99.2/27.4%/-22.6%
	2	100	-	94.4/17.5%/-16.8%
P+OD(RPO)	0.44	100	-	164.6/32.2%/-28.9%
	2	100	-	155.5/26.5%/-25.9%
N+PO(RPO)	0.4	100	-	125.7/29.6%/-23.7%
	2	100	-	95.3/17.2%/-16.6%
P+PO(RPO)	0.4	100	-	518.2/29.6%/-23.7%
	2	100	-	422.5/17.3%/-16.7%

### 13.13.3 CLN90LP Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	85.75	ohm/sq	0.027u	-2.96E-01	-8.04E-06	-2.45E+00	1.51E-03	1.10E-06
		Rend0	8.46u	ohm.m	-	-6.89E-02	1.12E+03	-1.82E-01	1.25E-03	2.50E-06
rpodwo	P+OD w/o silicide resistor	Rsh	152.05	ohm/sq	0.0307u	-3.89E-01	-1.73E-06	-2.10E+00	1.11E-03	4.14E-06
		Rend0	29.5u	ohm.m	-	3.50E-02	2.59E+02	-9.92E-02	-1.00E-03	2.00E-06
rnpolywo	N+POLY w/o silicide resistor	Rsh	86.6	ohm/sq	0.0936u	-7.88E-01	-9.80E-05	-2.45E+00	1.79E-04	-5.44E-07
		Rend0	14.4u	ohm.m	-	-2.27E-02	-6.54E+02	7.66E-01	3.00E-03	8.00E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	402.1	ohm/sq	0.0689u	1.10E-03	-2.69E-05	2.96E+00	-1.94E-04	1.01E-06
		Rend0	86.7u	ohm.m	-	1.04E-02	-7.22E+00	1.72E-01	-8.00E-04	-5.00E-06
rppoly	P+POLY silicide resistor (W>=2um)	Rsh	11.36	ohm/sq	-0.0086u	2.40E-06	8.00E-13	-	2.85E-03	2.17E-07
		Rsh	11.36	ohm/sq	-0.0086u	4.20E-07	2.00E-12	-	3.08E-03	6.70E-07
rnopoly	N+POLY silicide resistor (W>=2um)	Rsh	10.81	ohm/sq	0.0061u	2.40E-06	1.00E-12	-	2.75E-03	-1.00E-06
		Rsh	10.81	ohm/sq	0.0061u	5.00E-07	1.90E-12	-	3.18E-03	1.20E-06
rnodl	N+OD silicide resistor (W>=2um)	Rsh	10.94	ohm/sq	-0.0012u	3.66E-07	1.99E-12	-	3.02E-03	0.00E+00
rnodes	N+OD silicide resistor (W<2um)	Rsh	10.94	ohm/sq	-0.0012u	1.36E-07	7.63E-13	3.31E-03	9.00E-07	0.00E+00
rpoldl	P+OD silicide resistor (W>=2um)	Rsh	10.12	ohm/sq	0.002u	3.95E-07	2.22E-12	-	3.19E-03	0.00E+00
rpolds	P+OD silicide resistor (W<2um)	Rsh	10.12	ohm/sq	0.002u	1.57E-07	7.82E-13	-	3.42E-03	7.34E-07
rnwod	N-Well under OD resistor	Rsh	330	ohm/sq	0.29u	1.10E-02	2.98E-06	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	546	ohm/sq	0.41u	9.60E-03	1.00E-07	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	700	ohm/sq	-	1.53E-02	-7.81E-04	-	2.43E-03	9.49E-06
-	DNW under STI	Rsh	600	ohm/sq	-	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	-	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	-	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.12/0.36	Rsh	0.0736	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm1s	Metal 1 with W/S=0.12/0.12	Rsh	0.1	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.0894	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm2l	Metal 2 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm2s	Metal 2 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm2w	Metal 2 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3l	Metal 3 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3s	Metal 3 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3w	Metal 3 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4l	Metal 4 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4s	Metal 4 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4w	Metal 4 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5l	Metal 5 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5s	Metal 5 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5w	Metal 5 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6l	Metal 6 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6s	Metal 6 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6w	Metal 6 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7l	Metal 7 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7s	Metal 7 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7w	Metal 7 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm8l	Metal 8 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm8s	Metal 8 with W/S=0.42/0.42	Rsh	0.0221	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm8w	Metal 8 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9l	Metal 9 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9s	Metal 9 with W/S=0.42/0.42	Rsh	0.0221	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9w	Metal 9 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm10l	Metal 10 with W/S=3/4.5	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=3/2	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=3/1.5	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
-	RC_N+ (W/S=0.12/0.14)	-	18.0	ohm/ct	0	0.00	0.00	-	1.08E-03	5.92E-07
-	RC_P+ (W/S=0.12/0.14)	-	16.9	ohm/ct	0	0.00	0.00	-	1.05E-03	1.02E-07
-	RC_PO(N+) (W/S=0.12/0.14)	-	15.2	ohm/ct	0	0.00	0.00	-	1.03E-03	1.63E-07
-	RC_PO(P+) (W/S=0.12/0.14)	-	15.0	ohm/ct	0	0.00	0.00	-	1.11E-03	4.23E-07
-	RC_VIA1 (W/S=0.13/0.15)	-	1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA2 (W/S=0.13/0.15)	-	1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA3 (W/S=0.13/0.15)	-	1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA4 (W/S=0.13/0.15)	-	1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA5 (W/S=0.13/0.15)	-	1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA6 (W/S=0.13/0.15)	-	1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA7 (W/S=0.36/0.34)	-	0.41	ohm/ct	0	0.00	0.00	-	2.56E-03	-1.38E-07
-	RC_VIA8 (W/S=0.36/0.34)	-	0.35	ohm/ct	0	0.00	0.00	-	2.56E-03	-1.38E-07
-	RC_VIA9 (W/S=3/3)	-	0.35	ohm/ct	0	0.00	0.00	-	3.37E-03	-7.91E-08

### 13.13.3.1 Silicide Rs

Rs	W	L	PCM target	Simulation (Rs/corner)
N+OD	0.11	50	10.8	10.82/35%/-35%
	0.44	50	-	10.91/21%/-23%
	2	50		10.94/15%/-15%
P+OD	0.11	50	10.3	10.31/35%/-35%
	0.44	50	-	10.16/20%/-22%
	2	50		10.14/15%/-15%
N+PO	0.1	50	11.5	11.52/30%/-30%
	0.4	50	-	10.98/20%/-17%
	2	50		10.9/20%/-20%
P+PO	0.1	50	10.5	10.47/40%/-40%
	0.4	50	-	11.13/28%/-29%
	2	50		11.37/20%/-20%

### 13.13.3.2 Non-Silicide Rs

Rs	W	L	PCM target	Simulation (Rs/corner)
N+OD(PRO)	0.44	50	-	91.70/19%/-16%
	2	50	87.3	87.24/10%/-10%
P+OD(RPO)	0.44	50	-	164.74/15%/-14%
	2	50	156	155.60/10%/-10%
N+PO(RPO)	0.4	50	-	114.16/21%/-17%
	2	50	91.8	91.76/10%/-10%
P+PO(RPO)	0.4	50	-	489.92/21%/-17%
	2	50	420	420.0/10%/-10%

## 13.13.4CLN85G Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	90.56	ohm/sq	0.027u	-2.96E-01	-8.04E-06	-2.45E+00	1.51E-03	1.10E-06
		Rend0	8.46u	ohm.m	-	-6.89E-02	1.12E+03	-1.82E-01	1.25E-03	2.50E-06
rpodwo	P+OD w/o silicide resistor	Rsh	151.80	ohm/sq	0.0307u	-3.89E-01	-1.73E-06	-2.10E+00	1.11E-03	4.14E-06
		Rend0	29.5u	ohm.m	-	3.50E-02	2.59E+02	-9.92E-02	-1.00E-03	2.00E-06
rnpolywo	N+POLY w/o silicide resistor	Rsh	103.80	ohm/sq	0.106u	-7.88E-01	-9.80E-05	-2.45E+00	1.79E-04	-5.44E-07
		Rend0	14.4u	ohm.m	-	-2.27E-02	-6.54E+02	7.66E-01	3.00E-03	8.00E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	391.3	ohm/sq	0.0809u	1.10E-03	-2.69E-05	2.96E+00	-1.94E-04	1.01E-06
		Rend0	86.7u	ohm.m	-	1.04E-02	-7.22E+00	1.72E-01	-8.00E-04	-5.00E-06
rppoly1	P+POLY silicide resistor (W>=1.88um)	Rsh	11.30	ohm/sq	0.0031u	2.40E-06	8.00E-13	-	2.85E-03	2.17E-07
rppolys	P+POLY silicide resistor (W<1.88um)	Rsh	11.30	ohm/sq	0.0031u	4.20E-07	2.00E-12	-	3.08E-03	6.70E-07
rnpoly1	N+POLY silicide resistor (W>=1.88um)	Rsh	11.11	ohm/sq	0.0160u	2.40E-06	1.00E-12	-	2.75E-03	-1.00E-06
rnpolys	N+POLY silicide resistor (W<1.88um)	Rsh	11.11	ohm/sq	0.0160u	5.00E-07	1.90E-12	-	3.18E-03	1.20E-06
rnodl	N+OD silicide resistor (W>=1.88um)	Rsh	10.9	ohm/sq	-0.0246u	3.66E-07	1.99E-12	-	3.02E-03	0
rnodes	N+OD silicide resistor (W<1.88um)	Rsh	10.9	ohm/sq	-0.0246u	1.36E-07	7.63E-13	-	3.31E-03	9.00E-07
rpndl	P+OD silicide resistor (W>=1.88um)	Rsh	10.11	ohm/sq	-0.022u	3.95E-07	2.22E-12	-	3.19E-03	0
rpnds	P+OD silicide resistor (W<1.88um)	Rsh	10.11	ohm/sq	-0.022u	1.57E-07	7.82E-13	-	3.42E-03	7.34E-07
rnwod	N-Well under OD resistor	Rsh	293.8	ohm/sq	0.29u	1.10E-02	2.98E-06	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	535.6	ohm/sq	0.41u	9.60E-03	1.00E-07	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	780	ohm/sq	-	1.53E-02	-7.81E-04	-	2.43E-03	9.49E-06
-	DNW under STI	Rsh	600	ohm/sq	-	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	-	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	-	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.113/0.338	Rsh	0.0736	ohm/sq	-	-	-	-	2.92E-03	-1.22E-07
rm1s	Metal 1 with W/S=0.113/0.113	Rsh	0.1	ohm/sq	-	-	-	-	2.92E-03	-1.22E-07
rm1w	Metal 1 with W/S=0.305/0.152	Rsh	0.0894	ohm/sq	-	-	-	-	2.92E-03	-1.22E-07
rm2l	Metal 2 with W/S=0.132/0.395	Rsh	0.0604	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm2s	Metal 2 with W/S=0.132/0.132	Rsh	0.072	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm2w	Metal 2 with W/S=0.395/0.197	Rsh	0.069	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm3l	Metal 3 with W/S=0.132/0.395	Rsh	0.0604	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm3s	Metal 3 with W/S=0.132/0.132	Rsh	0.072	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm3w	Metal 3 with W/S=0.395/0.197	Rsh	0.069	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm4l	Metal 4 with W/S=0.132/0.395	Rsh	0.0604	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm4s	Metal 4 with W/S=0.132/0.132	Rsh	0.072	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm4w	Metal 4 with W/S=0.395/0.197	Rsh	0.069	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm5l	Metal 5 with W/S=0.132/0.395	Rsh	0.0604	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm5s	Metal 5 with W/S=0.132/0.132	Rsh	0.072	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm5w	Metal 5 with W/S=0.395/0.197	Rsh	0.069	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm6l	Metal 6 with W/S=0.132/0.395	Rsh	0.0604	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm6s	Metal 6 with W/S=0.132/0.132	Rsh	0.072	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm6w	Metal 6 with W/S=0.395/0.197	Rsh	0.069	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm7l	Metal 7 with W/S=0.132/0.395	Rsh	0.0604	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm7s	Metal 7 with W/S=0.132/0.132	Rsh	0.072	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm7w	Metal 7 with W/S=0.395/0.197	Rsh	0.069	ohm/sq	-	-	-	-	3.08E-03	-1.14E-07
rm8l	Metal 8 with W/S=0.395/0.592	Rsh	0.0214	ohm/sq	-	-	-	-	3.51E-03	-3.60E-07
rm8s	Metal 8 with W/S=0.395/0.395	Rsh	0.0225	ohm/sq	-	-	-	-	3.51E-03	-3.60E-07
rm8w	Metal 8 with W/S=0.395/1.184	Rsh	0.0204	ohm/sq	-	-	-	-	3.51E-03	-3.60E-07
rm9l	Metal 9 with W/S=0.395/0.592	Rsh	0.0214	ohm/sq	-	-	-	-	3.51E-03	-3.60E-07
rm9s	Metal 9 with W/S=0.395/0.395	Rsh	0.0225	ohm/sq	-	-	-	-	3.51E-03	-3.60E-07
rm9w	Metal 9 with W/S=0.395/1.184	Rsh	0.0204	ohm/sq	-	-	-	-	3.51E-03	-3.60E-07
rm10l	Metal 10 with W/S=3/4.5	Rsh	0.021	ohm/sq	-	-	-	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=3/2	Rsh	0.021	ohm/sq	-	-	-	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=3/1.5	Rsh	0.021	ohm/sq	-	-	-	-	3.89E-03	-1.50E-07
-	RC_N+		17.86	ohm/ct	-	-	-	-	1.08E-03	5.92E-07
-	RC_P+		16.96	ohm/ct	-	-	-	-	1.05E-03	1.02E-07
-	RC_PO(N+)		15.35	ohm/ct	-	-	-	-	1.03E-03	1.63E-07
-	RC PO(P+)		15.23	ohm/ct	-	-	-	-	1.11E-03	4.23E-07
-	RC_VIA1		1.11	ohm/ct	-	-	-	-	1.36E-03	9.15E-08
-	RC_VIA2		1.11	ohm/ct	-	-	-	-	1.36E-03	9.15E-08
-	RC_VIA3		1.11	ohm/ct	-	-	-	-	1.36E-03	9.15E-08
-	RC_VIA4		1.11	ohm/ct	-	-	-	-	1.36E-03	9.15E-08
-	RC_VIA5		1.11	ohm/ct	-	-	-	-	1.36E-03	9.15E-08
-	RC_VIA6		1.11	ohm/ct	-	-	-	-	1.36E-03	9.15E-08
-	RC_VIA7		0.45	ohm/ct	-	-	-	-	2.56E-03	-1.38E-07
-	RC_VIA8		0.35	ohm/ct	-	-	-	-	2.56E-03	-1.38E-07
-	RC_VIA9		0.041	ohm/ct	-	-	-	-	3.37E-03	-7.91E-08

### 13.13.4.1 Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD	0.11	50	8.80	8.81/35.2%/-35.3%
	0.44	50	-	10.29/23.6%/-25.3%
	2	50	10.77	10.77/15.0%/-15.0%
P+OD	0.11	50	8.34	8.34/34.7%/-35.0%
	0.44	50	-	9.60/22.8%/-24.7%
	2	50	10.00	10.00/15.0%/-15.0%
N+PO	0.1	50	13.41	13.40/29.6%/-30.1%
	0.4	50	-	11.62/17.6%/-13.7%
	2	50	11.26	11.26/20.0%/-20.0%
P+PO	0.1	50	11.70	11.70/41.0%/-41.0%
	0.4	50	-	11.40/26.7%/-27.1%
	2	50	11.38	11.38/20.0%/-20.0%

### 13.13.4.2 Non-Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.44	50	-	97.24/20.3%/-16.8%
	2	50	92.25	92.25/10.0%/-10.0%
P+OD(RPO)	0.44	50	-	165.3/15.4%/-13.9%
	2	50	155.62	155.60/10.0%/-10.0%
N+PO(RPO)	0.4	50	-	145.9/22.7%/-18.2%
	2	50	111.08	111.08/10.0%/-10.0%
P+PO(RPO)	0.4	50	-	503.2/22.6%/-17.6%
	2	50	412.42	412.40/10.0%/-10.0%

## 13.13.5 CLN85LP Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	85.36	ohm/sq	0.027u	-2.96E-01	-8.04E-06	-2.45E+00	1.51E-03	1.10E-06
		Rend0	8.46u	ohm.m	-	-6.89E-02	1.12E+03	-1.82E-01	1.25E-03	2.50E-06
rpodwo	P+OD w/o silicide resistor	Rsh	151.84	ohm/sq	0.0307u	-3.89E-01	-1.73E-06	-2.10E+00	1.11E-03	4.14E-06
		Rend0	29.5u	ohm.m	-	3.50E-02	2.59E+02	-9.92E-02	-1.00E-03	2.00E-06
rnpolywo	N+POLY w/o silicide resistor	Rsh	96.83	ohm/sq	0.0936u	-7.88E-01	-9.80E-05	-2.45E+00	1.79E-04	-5.44E-07
		Rend0	14.4u	ohm.m	-	-2.27E-02	-6.54E+02	7.66E-01	3.00E-03	8.00E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	391.9	ohm/sq	0.0689u	1.10E-03	-2.69E-05	2.96E+00	-1.94E-04	1.01E-06
		Rend0	86.7u	ohm.m	-	1.04E-02	-7.22E+00	1.72E-01	-8.00E-04	-5.00E-06
rppoly1	P+POLY silicide resistor (W>=2um)	Rsh	11.13	ohm/sq	-0.0117u	2.40E-06	8.00E-13	-	2.85E-03	2.17E-07
rppolys	P+POLY silicide resistor (W<2um)	Rsh	11.13	ohm/sq	-0.0117u	4.20E-07	2.00E-12	-	3.08E-03	6.70E-07
rnpoly1	N+POLY silicide resistor (W>=2um)	Rsh	10.82	ohm/sq	-0.0055u	2.40E-06	1.00E-12	-	2.75E-03	-1.00E-06
rnpolys	N+POLY silicide resistor (W<2um)	Rsh	10.82	ohm/sq	-0.0055u	5.00E-07	1.90E-12	-	3.18E-03	1.20E-06
rnodl	N+OD silicide resistor (W>=2um)	Rsh	10.78	ohm/sq	-0.0033u	3.66E-07	1.99E-12	-	3.02E-03	0.00E+00
rnodes	N+OD silicide resistor (W<2um)	Rsh	10.78	ohm/sq	-0.0033u	1.36E-07	7.63E-13	3.31E-03	9.00E-07	0.00E+00
rpndl	P+OD silicide resistor (W>=2um)	Rsh	10.02	ohm/sq	-0.0057u	3.95E-07	2.22E-12	-	3.19E-03	0.00E+00
rpndos	P+OD silicide resistor (W<2um)	Rsh	10.02	ohm/sq	-0.0057u	1.57E-07	7.82E-13	-	3.42E-03	7.34E-07
rnwod	N-Well under OD resistor	Rsh	299	ohm/sq	0.29u	1.10E-02	2.98E-06	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	550	ohm/sq	0.41u	9.60E-03	1.00E-07	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	700	ohm/sq	-	1.53E-02	-7.81E-04	-	2.43E-03	9.49E-06
-	DNW under STI	Rsh	600	ohm/sq	-	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	-	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	-	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.12/0.36	Rsh	0.0736	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm1s	Metal 1 with W/S=0.12/0.12	Rsh	0.1	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.0894	ohm/sq	0	0.00	0.00	-	2.92E-03	-1.22E-07
rm2l	Metal 2 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm2s	Metal 2 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm2w	Metal 2 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3l	Metal 3 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3s	Metal 3 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm3w	Metal 3 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4l	Metal 4 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4s	Metal 4 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm4w	Metal 4 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5l	Metal 5 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5s	Metal 5 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm5w	Metal 5 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6l	Metal 6 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6s	Metal 6 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm6w	Metal 6 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7l	Metal 7 with W/S=0.14/0.42	Rsh	0.0604	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7s	Metal 7 with W/S=0.14/0.14	Rsh	0.072	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm7w	Metal 7 with W/S=0.42/0.21	Rsh	0.069	ohm/sq	0	0.00	0.00	-	3.08E-03	-1.14E-07
rm8l	Metal 8 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm8s	Metal 8 with W/S=0.42/0.42	Rsh	0.0225	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm8w	Metal 8 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9l	Metal 9 with W/S=0.42/0.63	Rsh	0.0214	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9s	Metal 9 with W/S=0.42/0.42	Rsh	0.0225	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm9w	Metal 9 with W/S=0.42/1.26	Rsh	0.0204	ohm/sq	0	0.00	0.00	-	3.51E-03	-3.60E-07
rm10l	Metal 10 with W/S=3/4.5	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=3/2	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=3/1.5	Rsh	0.021	ohm/sq	0	0.00	0.00	-	3.89E-03	-1.50E-07
-	RC_N+		17.9	ohm/ct	0	0.00	0.00	-	1.08E-03	5.92E-07
-	RC_P+		16.9	ohm/ct	0	0.00	0.00	-	1.05E-03	1.02E-07
-	RC_PO(N+)		15.3	ohm/ct	0	0.00	0.00	-	1.03E-03	1.63E-07
-	RC_PO(P+)		15.2	ohm/ct	0	0.00	0.00	-	1.11E-03	4.23E-07
-	RC_VIA1		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA2		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA3		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA4		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA5		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA6		1.11	ohm/ct	0	0.00	0.00	-	1.36E-03	9.15E-08
-	RC_VIA7		0.45	ohm/ct	0	0.00	0.00	-	2.56E-03	-1.38E-07
-	RC_VIA8		0.35	ohm/ct	0	0.00	0.00	-	2.56E-03	-1.38E-07
-	RC_VIA9		0.35	ohm/ct	0	0.00	0.00	-	3.37E-03	-7.91E-08

### 13.13.5.1 Silicide Rs

Rs	W	L	PCM target	Simulation (Rs/corner)
N+OD	0.11	50	10.44	10.45/35%-35%
	0.44	50	-	10.69/20%-22%
	2	50	10.77	10.77/15%-15%
P+OD	0.11	50	9.5	9.5/35%-35%
	0.44	50	-	9.88/21%-23%
	2	50	10.00	10.0/15%-15%
N+PO	0.1	50	10.24	10.23/30%-30%
	0.4	50	-	10.67/21%-18%
	2	50	10.84	10.8/20%-20%
P+PO	0.1	50	9.91	9.91/40%-40%
	0.4	50	-	10.80/28%-29%
	2	50	11.12	11.12/20%-20%

### 13.13.5.2 Non-Silicide Rs

Rs	W	L	PCM target	Simulation (Rs/corner)
N+OD(PRO)	0.44	50	-	91.7/20%-17%
	2	50	86.96	86.96/10%-10%
P+OD(RPO)	0.44	50	-	165.35/15%-14%
	2	50	155.62	155.64/10%-10%
N+PO(RPO)	0.4	50	-	130.24/22%-18%
	2	50	103	102.92/10%-10%
P+PO(RPO)	0.4	50	-	484.32/22%-18%
	2	50	410.5	410.4/10%-10%

## 13.13.6 CLN80GC Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rmodwo	N+OD w/o silicide resistor	Rsh	99.5	ohm/sq	0.00746u	-3.89E-01	-2.35E-06	-1.91E+00	1.54E-03	9.70E-07
		Rendo	9.60u	ohm.m	-	-2.80E-02	-1.40E+02	6.69E-02	7.98E-04	-5.17E-07
rpodwo	P+OD w/o silicide resistor	Rsh	168.2	ohm/sq	0.0236u	-1.01E-01	-7.41E-07	-1.95E+00	1.23E-03	9.70E-07
		Rendo	29.5u	ohm.m	-	-4.71E-02	1.66E+02	2.99E-02	-3.20E-04	-4.19E-07
rnpolywo	N+POLY w/o silicide resistor	Rsh	140	ohm/sq	0.0865u	1.70E-03	2.06E-05	1.85E-01	-1.60E-05	3.70E-07
		Rendo	20.8u	ohm.m	-	3.64E-01	2.88E+02	6.95E-01	1.096E-03	2.44E-07
rppolywo	P+POLY w/o silicide resistor	Rsh	441.1	ohm/sq	0.0672u	1.22E-01	-9.34E-08	1.54E-07	-1.65E-04	6.19E-07
		Rendo	102u	ohm.m	-	-2.90E-03	7.18E+01	-3.80E+00	-1.26E-03	7.00E-07
rppoly1	P+POLY silicide (W>=1.8um)	Rsh	10.9	ohm/sq	-0.0015u	1.36E-07	4.37E-11	-	2.81E-03	2.21E-07
rppolys	P+POLY silicide (W<1.8um)	Rsh	10.9	ohm/sq	-0.0015u	6.06E-08	9.66E-12	-	3.11E-03	1.83E-07
rnpoly1	N+POLY silicide (W>=1.8um)	Rsh	10.85	ohm/sq	0.011u	5.58E-08	4.07E-11	-	2.64E-03	-1.94E-07
rnpolys	N+POLY silicide (W<1.8um)	Rsh	10.85	ohm/sq	0.011u	1.22E-08	9.36E-12	-	3.11E-03	-3.87E-08
rmodl	N+OD silicide (W>=1.8um)	Rsh	11.35	ohm/sq	-0.022u	6.21E-07	1.77E-12	-	2.91E-03	3.42E-07
rnodes	N+OD silicide (W<1.8um)	Rsh	11.35	ohm/sq	-0.022u	7.23E-07	7.23E-13	-	3.19E-03	1.05E-06
rpodl	P+OD silicide (W>=1.8um)	Rsh	10	ohm/sq	-0.024u	1.03E-06	2.06E-12	-	2.86E-03	1.52E-06
rpods	P+OD silicide (W<1.8um)	Rsh	10	ohm/sq	-0.024u	8.53E-07	8.53E-13	-	3.32E-03	1.92E-07
rnwod	N-Well under OD resistor	Rsh	299	ohm/sq	0.29u	1.24E-02	-2.98E-04	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	518	ohm/sq	0.41u	1.16E-02	-4.57E-04	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	780	ohm/sq	0	1.68E-02	-9.68E-04	-	2.50E-03	1.03E-05
-	DNW under STI	Rsh	600	ohm/sq	0	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	0	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	0	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.108/0.324	Rsh	0.0791	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1s	Metal 1 with W/S=0.108/0.108	Rsh	0.115	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.109	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm2l	Metal 2 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2s	Metal 2 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2w	Metal 2 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3l	Metal 3 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3s	Metal 3 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3w	Metal 3 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4l	Metal 4 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4s	Metal 4 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4w	Metal 4 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5l	Metal 5 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5s	Metal 5 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5w	Metal 5 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6l	Metal 6 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6s	Metal 6 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6w	Metal 6 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7l	Metal 7 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7s	Metal 7 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7w	Metal 7 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm8l	Metal 8 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8s	Metal 8 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8w	Metal 8 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9l	Metal 9 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9s	Metal 9 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9w	Metal 9 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm10l	Metal 10 with W/S=2.7/4.05	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=2.7/1.8	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=2.7/1.35	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
-	RC_N+		18	ohm/ct	0	0	0	-	1.594E-03	3.694E-08
-	RC_P+		18	ohm/ct	0	0	0	-	1.633E-03	-4.796E-08
-	RC_PO(N+)		15	ohm/ct	0	0	0	-	1.676E-03	-2.057E-07
-	RC_PO(P+)		15	ohm/ct	0	0	0	-	1.866E-03	-9.529E-08
-	RC_VIA1		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA2		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA3		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA4		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA5		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA6		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA7		0.5	ohm/ct	0	0	0	-	2.691E-03	-1.027E-06
-	RC_VIA8		0.5	ohm/ct	0	0	0	-	2.691E-03	-1.027E-06
-	RC_VIA9		0.05	ohm/ct	0	0	0	-	3.37E-03	-7.91E-08

### 13.13.6.1 Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD	0.099	90	9.3	9.3/40.7%/-37.9%
	0.396	90	-	10.8/26.1%/-26.7%
	1.8	90	-	11.2/15.0%/-15.0%
P+OD	0.099	90	8.1	8.1/40.4%/-37.7%
	0.396	90	-	9.4/26.1%/-26.7%
	1.8	90	-	9.9/15.0%/-15.0%
N+PO	0.09	90	12.4	12.4/40.5%/-40.5%
	0.36	90	-	11.2/24.8%/-26.4%
	1.8	90	-	10.9/20.0%/-20.0%
P+PO	0.09	90	10.7	10.7/41.0%/-41.0%
	0.36	90	-	10.9/25.5%/-27.2%
	1.8	90	-	10.9/20.0%/-20.0%

### 13.13.6.2 Non-Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.396	90	-	101.6/28.4%/-23.1%
	1.8	90	-	100.1/17.8%/-17.0%
P+OD(RPO)	0.396	90	-	166.2/33.0%/-29.3%
	1.8	90	-	171.1/26.6%/-26.1%
N+PO(RPO)	0.36	90	-	184.7/30.4%/-24.1%
	1.8	90	-	147.5/17.4%/-16.8%
P+PO(RPO)	0.36	90	-	544.4/30.7%/-24.2%
	1.8	90	-	460.4/17.6%/-16.9%

## 13.13.7 CLN80GT Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	99.5	ohm/sq	0.00746u	-3.89E-01	-2.35E-06	-1.91E+00	1.54E-03	9.70E-07
		Rendo	9.60u	ohm.m	-	-2.80E-02	-1.40E+02	6.69E-02	7.98E-04	-5.17E-07
rpolwo	P+OD w/o silicide resistor	Rsh	175	ohm/sq	0.0236u	-1.01E-01	-7.41E-07	-1.95E+00	1.23E-03	9.70E-07
		Rendo	29.5u	ohm.m	-	-4.71E-02	1.66E+02	2.99E-02	-3.20E-04	-4.19E-07
rnpolywo	N+POLY w/o silicide resistor	Rsh	129.4	ohm/sq	0.1u	1.70E-03	2.06E-05	1.85E-01	1.05E-04	3.04E-07
		Rendo	22u	ohm.m	-	3.64E-01	2.88E+02	6.95E-01	6.96E-04	2.44E-07
rppolywo	P+POLY w/o silicide resistor	Rsh	441.1	ohm/sq	0.0672u	1.22E-01	-9.34E-08	1.54E-07	-1.65E-04	6.19E-07
		Rendo	102u	ohm.m	-	-2.90E-03	7.18E+01	-3.80E+00	-1.26E-03	7.00E-07
rppolyl	P+POLY silicide (W>=1.8um)	Rsh	10.9	ohm/sq	-0.005u	1.01E-06	2.02E-12	-	2.81E-03	2.21E-07
rppolys	P+POLY silicide (W<1.8um)	Rsh	10.9	ohm/sq	-0.005u	1.01E-06	2.02E-12	-	3.11E-03	1.83E-07
rnpolyl	N+POLY silicide (W>=1.8um)	Rsh	10.85	ohm/sq	0.011u	1.93E-06	7.70E-13	-	2.64E-03	-1.94E-07
rnpolys	N+POLY silicide (W<1.8um)	Rsh	10.85	ohm/sq	0.011u	1.93E-06	7.70E-13	-	3.11E-03	-3.87E-08
rnodl	N+OD silicide (W>=1.8um)	Rsh	11.35	ohm/sq	-0.022u	7.23E-07	7.23E-13	-	2.91E-03	3.42E-07
rnodes	N+OD silicide (W<1.8um)	Rsh	11.35	ohm/sq	-0.022u	7.23E-07	7.23E-13	-	3.19E-03	1.05E-06
rpdol	P+OD silicide (W>=1.8um)	Rsh	10	ohm/sq	-0.024u	8.53E-07	8.53E-13	-	2.86E-03	1.52E-06
rpdos	P+OD silicide (W<1.8um)	Rsh	10	ohm/sq	-0.024u	8.53E-07	8.53E-13	-	3.32E-03	1.92E-07
rnwod	N-Well under OD resistor	Rsh	325	ohm/sq	0.29u	1.24E-02	-2.98E-04	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	540	ohm/sq	0.41u	1.16E-02	-4.57E-04	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	780	ohm/sq	0	1.68E-02	-9.68E-04	-	2.50E-03	1.03E-05
-	DNW under STI	Rsh	600	ohm/sq	0	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	0	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	0	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.108/0.324	Rsh	0.0791	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1s	Metal 1 with W/S=0.108/0.108	Rsh	0.115	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.109	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm2l	Metal 2 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2s	Metal 2 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2w	Metal 2 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3l	Metal 3 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3s	Metal 3 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3w	Metal 3 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4l	Metal 4 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4s	Metal 4 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4w	Metal 4 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5l	Metal 5 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5s	Metal 5 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5w	Metal 5 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6l	Metal 6 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6s	Metal 6 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6w	Metal 6 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7l	Metal 7 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7s	Metal 7 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7w	Metal 7 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm8l	Metal 8 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8s	Metal 8 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8w	Metal 8 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9l	Metal 9 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9s	Metal 9 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9w	Metal 9 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm10l	Metal 10 with W/S=2.7/4.05	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=2.7/1.8	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=2.7/1.35	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
-	RC_N+		18	ohm/ct	0	0	0	-	1.594E-03	3.694E-08
-	RC_P+		18	ohm/ct	0	0	0	-	1.633E-03	-4.796E-08
-	RC_PO(N+)		15	ohm/ct	0	0	0	-	1.676E-03	-2.057E-07
-	RC PO(P+)		15	ohm/ct	0	0	0	-	1.866E-03	-9.529E-08
-	RC_VIA1		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA2		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA3		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA4		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA5		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA6		1.6	ohm/ct	0	0	0	-	1.625E-03	-8.942E-08
-	RC_VIA7		0.5	ohm/ct	0	0	0	-	2.691E-03	-1.027E-06
-	RC_VIA8		0.5	ohm/ct	0	0	0	-	2.691E-03	-1.027E-06
-	RC_VIA9		0.05	ohm/ct	0	0	0	-	3.37E-03	-7.91E-08

### 13.13.7.1 Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD	0.099	90	9.3	9.3/40.7%/-37.9%
	0.396	90	-	10.8/26.0%/-26.7%
	1.8	90	-	11.2/14.9%/-14.9%
P+OD	0.099	90	8	8.0/40.4%/-37.7%
	0.396	90	-	9.4/26.1%/-26.7%
	1.8	90	-	9.9/15.0%/-15.0%
N+PO	0.09	90	12.4	12.4/40.4%/-40.5%
	0.36	90	-	11.2/24.8%/-26.4%
	1.8	90	-	10.9/19.9%/-20.0%
P+PO	0.09	90	10.3	10.3/40.1%/-40.4%
	0.36	90	-	10.8/25.4%/-27.1%
	1.8	90	-	10.9/20.0%/-20.0%

### 13.13.7.2 Non-Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.396	90	-	101.6/28.3%/-23.0%
	1.8	90	-	100.1/17.7%/-17.0%
P+OD(RPO)	0.396	90	-	186.7/32.9%/-29.2%
	1.8	90	-	178.0/26.6%/-26.0%
N+PO(RPO)	0.36	90	-	179.7/30.1%/-23.9%
	1.8	90	-	137.5/17.3%/-16.7%
P+PO(RPO)	0.36	90	-	544.6/30.7%/-24.2%
	1.8	90	-	460.5/17.5%/-16.8%

## 13.13.8 CLN80HS Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	98.63	ohm/sq	0.00585u	-5.66E-01	-8.39E-06	3.14E+00	1.60E-03	1.04E-06
		Rend0	10.214u	ohm.m	-	2.77E-01	6.63E+02	3.77E-01	6.81E-04	-3.09E-07
rpolwo	P+OD w/o silicide resistor	Rsh	196.39	ohm/sq	0.01010u	2.95E-02	1.98E-06	1.10E-05	1.20E-03	7.69E-07
		Rend0	26.141u	ohm.m	-	-2.34E-01	1.44E+02	7.81E-01	-5.78E-04	-9.18E-07
rnpolywo	N+POLY w/o silicide resistor	Rsh	93.24	ohm/sq	0.10156u	-5.00E-03	-1.79E-05	1.31E+00	3.06E-04	2.77E-07
		Rend0	14.458u	ohm.m	-	-1.11E+00	-1.01E+03	-7.34E-01	3.07E-04	-1.31E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	450.47	ohm/sq	0.08909u	3.12E-02	-7.04E-06	2.71E+00	-1.86E-04	6.12E-07
		Rend0	110.336u	ohm.m	-	-3.22E-01	3.78E+01	1.21E+00	-1.65E-03	6.30E-07
rppolyl	P+POLY silicide resistor ( $W \geq 1.8\text{um}$ )	Rsh	11.899	ohm/sq	0.0062u	1.82E-06	9.11E-13	-	2.69E-03	-1.00E-07
rppolys	P+POLY silicide resistor ( $W < 1.8\text{um}$ )	Rsh	11.899	ohm/sq	0.0062u	1.82E-06	9.11E-13	-	3.17E-03	3.59E-07
rnpolyl	N+POLY silicide resistor ( $W \geq 1.8\text{um}$ )	Rsh	11.714	ohm/sq	0.0266u	1.93E-06	7.70E-13	-	2.58E-03	-1.65E-07
rnpolys	N+POLY silicide resistor ( $W < 1.8\text{um}$ )	Rsh	11.714	ohm/sq	0.0266u	1.93E-06	7.70E-13	-	3.11E-03	3.77E-07
rnodl	N+OD silicide resistor ( $W \geq 1.8\text{um}$ )	Rsh	11.93	ohm/sq	-0.033u	6.35E-07	7.61E-13	-	2.90E-03	8.91E-08
rnodes	N+OD silicide resistor ( $W < 1.8\text{um}$ )	Rsh	11.93	ohm/sq	-0.033u	6.35E-07	7.61E-13	-	3.25E-03	3.31E-07
rprod1	P+OD silicide resistor ( $W \geq 1.8\text{um}$ )	Rsh	10.83	ohm/sq	-0.033u	7.44E-07	7.44E-13	-	2.85E-03	2.65E-08
rprod2	P+OD silicide resistor ( $W < 1.8\text{um}$ )	Rsh	10.83	ohm/sq	-0.033u	7.44E-07	7.44E-13	-	3.25E-03	6.01E-07
rnwod	N-Well under OD resistor	Rsh	325	ohm/sq	0.29u	1.24E-02	-2.98E-04	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	540	ohm/sq	0.41u	1.16E-02	-4.57E-04	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	780	ohm/sq	-	1.68E-02	-9.68E-04	-	2.50E-03	1.03E-05
-	DNW under STI	Rsh	600	ohm/sq	-	1.51E-02	-8.89E-04	-	2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq	-	1.03E-02	-5.01E-04	-	2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq	-	1.26E-02	-7.94E-04	-	2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.108/0.324	Rsh	0.0791	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1s	Metal 1 with W/S=0.108/0.108	Rsh	0.115	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.109	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm2l	Metal 2 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2s	Metal 2 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2w	Metal 2 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3l	Metal 3 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3s	Metal 3 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3w	Metal 3 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4l	Metal 4 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4s	Metal 4 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4w	Metal 4 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5l	Metal 5 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5s	Metal 5 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5w	Metal 5 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6l	Metal 6 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6s	Metal 6 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6w	Metal 6 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7l	Metal 7 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7s	Metal 7 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7w	Metal 7 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm8l	Metal 8 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8s	Metal 8 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8w	Metal 8 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9l	Metal 9 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9s	Metal 9 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9w	Metal 9 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm10l	Metal 10 with W/S=2.7/4.05	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=2.7/1.8	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=2.7/1.35	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
-	RC_N+		18	ohm/ct	0	0	0	-	1.59E-03	3.69E-08
-	RC_P+		18	ohm/ct	0	0	0	-	1.63E-03	-4.80E-08
-	RC_PO(N+)		15	ohm/ct	0	0	0	-	1.68E-03	-2.06E-07
-	RC_PO(P+)		15	ohm/ct	0	0	0	-	1.87E-03	-9.53E-08
-	RC_VIA1		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA2		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA3		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA4		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA5		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA6		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA7		0.5	ohm/ct	0	0	0	-	2.69E-03	-1.03E-06
-	RC_VIA8		0.5	ohm/ct	0	0	0	-	2.69E-03	-1.03E-06
-	RC_VIA9		0.05	ohm/ct	0	0	0	-	3.37E-03	-7.91E-08

### 13.13.8.1 Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD	0.099	90	8.80	9.2/39.7%/-40.3%
	0.396	90	11.79	11.3/25.7%/-27.8%
	1.8	90	11.49	12.0/14.6%/-14.6%
P+OD	0.099	90	7.96	8.2/40.2%/-38.4%
	0.396	90	10.57	10.1/26.1%/-27.2%
	1.8	90	10.45	10.8/14.8%/-14.8%
N+PO	0.09	90	16.63	16.6/40.2%/-40.6%
	0.36	90	12.84	12.7/24.2%/-25.6%
	1.8	90	11.89	11.9/19.9%/-20.0%
P+PO	0.09	90	12.78	12.8/40.2%/-40.2%
	0.36	90	12.44	12.1/25.0%/-26.6%
	1.8	90	11.94	11.9/19.9%/-20.0%

### 13.13.8.2 Non-Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.396	90	105.2	100.3/28.2%/-23.0%
	1.8	90	95.3	99.2/17.7%/-17.0%
P+OD(RPO)	0.396	90	209.3	202.1/32.6%/-29.1%
	1.8	90	195.1	198.1/26.6%/-26.0%
N+PO(RPO)	0.36	90	124.9	130.2/30.8%/-24.2%
	1.8	90	96.6	99.1/17.3%/-16.7%
P+PO(RPO)	0.36	90	573.0	601.1/30.5%/-24.1%
	1.8	90	481.2	476.4/17.4%/-16.7%

## 13.13.9 CLN80LP Resistor Model

Name	Structure	Type	TypeVal	Unit	dw	VC1	VC2	VC3	TC1	TC2
rnodwo	N+OD w/o silicide resistor	Rsh	96.33	ohm/sq	0.02431u	-3.89E-01	-2.35E-06	-1.91E+00	1.50E-03	1.37E-06
		Rendo	11.85u	ohm.m	-	-2.80E-02	-1.40E+02	6.69E-02	6.79E-04	-3.81E-08
rpolwo	P+OD w/o silicide resistor	Rsh	192.39	ohm/sq	0.04401u	-1.01E-01	-7.41E-07	-1.95E+00	1.24E-03	9.22E-07
		Rendo	39.67u	ohm.m	-	-4.71E-02	1.66E+02	2.99E-02	-5.22E-04	1.21E-07
rnpolywo	N+POLY w/o silicide resistor	Rsh	139.36	ohm/sq	0.09573u	1.70E-01	2.06E-05	1.85E-01	5.42E-08	2.52E-07
		Rendo	20.71u	ohm.m	-	3.64E-01	2.88E+02	6.95E-01	6.64E-05	3.60E-06
rppolywo	P+POLY w/o silicide resistor	Rsh	451.52	ohm/sq	0.07399u	1.22E-01	-9.34E-08	1.54E-07	-1.55E-04	5.96E-07
		Rendo	102.5u	ohm.m	-	-2.90E-03	7.18E+01	-3.80E+00	-1.06E-03	5.82E-07
rppolyl	P+POLY silicide (W>=1.8um)	Rsh	10.9	ohm/sq	-0.009u	3.84E-06	4.81E-12	-	2.81E-03	2.21E-07
rppolys	P+POLY silicide (W<1.8um)	Rsh	10.9	ohm/sq	-0.009u	1.01E-06	2.02E-12	-	3.11E-03	1.83E-07
rnpolyl	N+POLY silicide (W>=1.8um)	Rsh	11.05	ohm/sq	0.001u	3.76E-06	3.76E-12	-	2.64E-03	-1.94E-07
rnpolys	N+POLY silicide (W<1.8um)	Rsh	11.05	ohm/sq	0.001u	1.93E-06	7.70E-13	-	3.11E-03	-3.87E-08
rnodl	N+OD silicide (W>=1.8um)	Rsh	11.35	ohm/sq	-0.02u	6.21E-07	1.77E-12	-	2.91E-03	3.42E-07
rnodes	N+OD silicide (W<1.8um)	Rsh	11.35	ohm/sq	-0.02u	7.23E-07	7.23E-13	-	3.19E-03	1.05E-06
rpdol	P+OD silicide (W>=1.8um)	Rsh	10	ohm/sq	-0.018u	1.03E-06	2.06E-12	-	2.86E-03	1.52E-06
rpdos	P+OD silicide (W<1.8um)	Rsh	10	ohm/sq	-0.018u	8.53E-07	8.53E-13	-	3.32E-03	1.92E-07
rnwod	N-Well under OD resistor	Rsh	300	ohm/sq	0.29u	1.24E-02	-2.98E-04	-	2.83E-03	1.04E-05
rnwsti	N-well under STI resistor	Rsh	550	ohm/sq	0.41u	1.16E-02	-4.57E-04	-	1.73E-03	9.66E-06
-	DNW under OD	Rsh	780	ohm/sq		1.68E-02	-9.68E-04		2.50E-03	1.03E-05
-	DNW under STI	Rsh	600	ohm/sq		1.51E-02	-8.89E-04		2.66E-03	5.91E-06
-	R-well under OD	Rsh	880	ohm/sq		1.03E-02	-5.01E-04		2.42E-03	4.93E-06
-	R-Well under STI	Rsh	1100	ohm/sq		1.26E-02	-7.94E-04		2.07E-03	8.46E-06
rm1l	Metal 1 with W/S=0.108/0.324	Rsh	0.0791	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1s	Metal 1 with W/S=0.108/0.108	Rsh	0.115	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm1w	Metal 1 with W/S=0.324/0.162	Rsh	0.109	ohm/sq	0	0	0	-	2.85E-03	-5.35E-07
rm2l	Metal 2 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2s	Metal 2 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm2w	Metal 2 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3l	Metal 3 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3s	Metal 3 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm3w	Metal 3 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4l	Metal 4 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4s	Metal 4 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm4w	Metal 4 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5l	Metal 5 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5s	Metal 5 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm5w	Metal 5 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6l	Metal 6 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6s	Metal 6 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm6w	Metal 6 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7l	Metal 7 with W/S=0.126/0.378	Rsh	0.0614	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7s	Metal 7 with W/S=0.126/0.126	Rsh	0.1	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm7w	Metal 7 with W/S=0.378/0.189	Rsh	0.0876	ohm/sq	0	0	0	-	2.97E-03	-4.83E-07
rm8l	Metal 8 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8s	Metal 8 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm8w	Metal 8 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9l	Metal 9 with W/S=0.378/0.567	Rsh	0.0207	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9s	Metal 9 with W/S=0.378/0.378	Rsh	0.0217	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm9w	Metal 9 with W/S=0.378/1.134	Rsh	0.0194	ohm/sq	0	0	0	-	3.61E-03	-5.90E-08
rm10l	Metal 10 with W/S=2.7/4.05	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10s	Metal 10 with W/S=2.7/1.8	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
rm10w	Metal 10 with W/S=2.7/1.35	Rsh	0.021	ohm/sq	0	0	0	-	3.89E-03	-1.50E-07
-	RC_N+		18	ohm/ct	0	0	0	-	1.59E-03	3.69E-08
-	RC_P+		18	ohm/ct	0	0	0	-	1.63E-03	-4.80E-08
-	RC_PO(N+)		15	ohm/ct	0	0	0	-	1.68E-03	-2.06E-07
-	RC PO(P+)		15	ohm/ct	0	0	0	-	1.87E-03	-9.53E-08
-	RC_VIA1		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA2		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA3		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA4		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA5		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA6		1.6	ohm/ct	0	0	0	-	1.63E-03	-8.94E-08
-	RC_VIA7		0.5	ohm/ct	0	0	0	-	2.69E-03	-1.03E-06
-	RC_VIA8		0.5	ohm/ct	0	0	0	-	2.69E-03	-1.03E-06
-	RC_VIA9		0.05	ohm/ct	0	0	0	-	3.37E-03	-7.91E-08

### 13.13.9.1 Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD	0.099	90	9.42	9.4/39.7%/-38.1%
	0.396	90	-	10.8/25.8%/-26.7%
	1.8	90	-	11.2/14.9%/-14.9%
P+OD	0.099	90	8.51	8.5/40.1%/-38.3%
	0.396	90		9.6/25.8%/-26.8%
	1.8	90		9.9/15.0%/-15.0%
N+PO	0.09	90	10.96	11.2/37.5%/-38.5%
	0.36	90	-	11.1/24.3%/-25.9%
	1.8	90	-	11.1/19.6%/-19.6%
P+PO	0.09	90	9.72	9.9/39.3%/-39.8%
	0.36	90	-	10.6/25.4%/-27.1%
	1.8	90	-	10.9/20.0%/-19.9%

### 13.13.9.2 Non-Silicide Rs

Rs	W	L	PCM target	model (Rsh/corner)
N+OD(PRO)	0.396	90	-	102.9/29.0%/-23.4%
	1.8	90	-	97.9/17.8%/-17.0%
P+OD(RPO)	0.396	90	-	217.3/33.4%/-29.5%
	1.8	90	-	198.1/26.7%/-26.0%
N+PO(RPO)	0.36	90	-	190.4/30.9%/-24.3%
	1.8	90	-	147.7/17.4%/-16.7%
P+PO(RPO)	0.36	90	-	570.6/31.1%/-24.4%
	1.8	90	-	473.2/17.5%/-16.8%

## 13.13.10 CLM90 Resistor Model

Film	Valid Width	Rs Mean/Range	Unit	TC1	TC2	VC1	VC2	deltaW ( $\mu$ m)
M1	W/S=0.12/0.12	0.1 (+30/-40%)	$\Omega/\text{sq}$	2.92E-03	-1.22E-07	N/A	N/A	
M2-M7	W/S=0.14/0.14	0.072 $\pm 0.022$	$\Omega/\text{sq}$	3.077E-03	-1.14E-07	N/A	N/A	
M8 (3XTM)	W/S=0.42/0.42	0.022 $\pm 0.0055$	$\Omega/\text{sq}$	3.506E-03	-3.60E-07	N/A	N/A	
<b>M9 (UTM)</b>	<b>W/S=2/2</b>	<b>0.0050 <math>\pm 0.0010</math></b>	$\Omega/\text{sq}$	<b>3.412E-3</b>	<b>3.6894E-6</b>	<b>N/A</b>	<b>N/A</b>	
M10 (AI RDL)	W/S=3.0/2.0	0.021 $\pm$ 0.004	$\Omega/\text{sq}$	3.89E-03	-1.50E-07	N/A	N/A	
RC_VIA1	0.13x0.13	1.2 $\pm$ 0.6	$\Omega/\text{ct}$	1.36E-03	9.15E-08	N/A	N/A	-
RC_VIA2	0.13x0.13	1.2 $\pm$ 0.6	$\Omega/\text{ct}$	1.36E-03	9.15E-08	N/A	N/A	-
RC_VIA3	0.13x0.13	1.2 $\pm$ 0.6	$\Omega/\text{ct}$	1.36E-03	9.15E-08	N/A	N/A	-
RC_VIA4	0.13x0.13	1.2 $\pm$ 0.6	$\Omega/\text{ct}$	1.36E-03	9.15E-08	N/A	N/A	-
RC_VIA5	0.13x0.13	1.2 $\pm$ 0.6	$\Omega/\text{ct}$	1.36E-03	9.15E-08	N/A	N/A	-
RC_VIA6	0.13x0.13	1.2 $\pm$ 0.6	$\Omega/\text{ct}$	1.36E-03	9.15E-08	N/A	N/A	-
RC_VIA7	0.36X0.36	0.45 $\pm$ 0.22	$\Omega/\text{ct}$	2.56E-03	-1.38E-07	N/A	N/A	-
<b>RC_VIA8</b>	<b>0.36X0.36</b>	<b>0.37<math>\pm</math>0.26</b>	<b><math>\Omega/\text{ct}</math></b>	<b>1.479E-3</b>	<b>8.8673E-7</b>	<b>N/A</b>	<b>N/A</b>	<b>-</b>
RC_VIA9	3.0x3.0	0.041 $\pm$ 0.020	$\Omega/\text{ct}$	3.37E-03	-7.91E-08	N/A	N/A	

## 13.14 Unsilicided N+/P+ Poly Resistors Models

Two types of unsilicided poly resistor, N+ and P+, are available. These resistors were measured by sweeping current over one node while the other node was grounded.

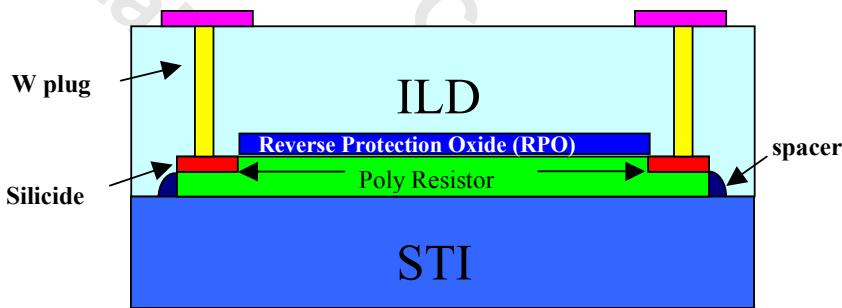
TSMC's reliability team suggests that these resistors might display reliability limitations if the applied current density exceeds  $375 \mu\text{A}/\mu\text{m}$ . Thus, TSMC limits the valid current density range for the resistor models to between 0 and  $375 \mu\text{A}/\mu\text{m}$ . The corresponding voltage range can be obtained using Ohm's law. TSMC further limits the application of these models only to resistors with widths  $\geq 0.4 \mu\text{m}$ , lengths  $\geq 0.8 \mu\text{m}$ , and square number  $\geq 1.0$ .



It is strongly recommended that users apply these models within valid current, voltage, and dimension ranges. An operation outside any of these ranges will lead to a significant error.

The following figure provides a cross-section depiction of the resistor's structure for either model type.

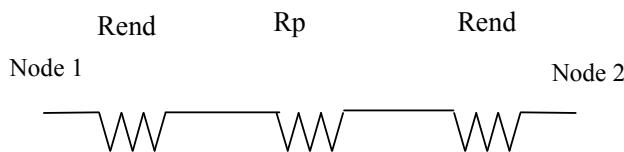
### Cross-Section Depiction: Resistor Structure



These unsilicided N+ and P+ poly resistors were modeled with the equivalent circuit shown in the following figure.

In the circuit model, the **R<sub>end</sub>** component represents the contributions from the interface resistance ( $R_{int}$ , due to the depletion of dopant near the interface between reverse protection oxide (RPO) and silicide) but do not include the contact resistance  $R_c$ . The **R<sub>p</sub>** component represents the primary contribution from the poly resistor.

### Equivalent Circuit Model



## 13.14.1 Resistor Model Equations

As shown in the previous equivalent circuit, the total resistance ( $\mathbf{R}$ ) is equal to the sum of the  $R_p$  plus two times  $R_{end}$ , as in equation (3):

$$R = R_p + 2R_{end} \quad \text{equation (3)}$$

In contrast to other resistor models, the voltage dependence of  $R_{end}$  and  $R_p$  components were modeled with the equations containing hyperbolic tangent terms, as in equations (4) and (5), which follow:

$$R_{end} = R_{end0} / (W - \delta W) \cdot (1 + tce1 \cdot \delta T + tce2 \cdot \delta T^2) \cdot \{1 + vce1 \cdot [\tanh(vce2 \cdot |\delta V_e|) + vce3] - \tanh(vce3)\} \quad \text{equation (4)}$$

$$R_p = R_{sh} \cdot (L - \delta L) / (W - \delta W) \cdot (1 + tcp1 \cdot \delta T + tcp2 \cdot \delta T^2) \cdot \{1 + vcp1 \cdot [\tanh(vcp2 \cdot |\delta V_p| / L) + vcp3] - \tanh(vcp3)\} \quad \text{equation (5)}$$

where

$\delta T$	=	$T - 25$ (in $^{\circ}\text{C}$ );
$\delta V_p$ and $\delta V_e$ (in volt)	=	the voltage drops across $R_p$ and $R_{end}$ components
$R_{end0}$	=	$R_{end}$ resistance value at $25^{\circ}\text{C}$ and an infinitesimal applied voltage
$\delta L$	=	the length offset

The constants  $tce1$ ,  $tce2$ ,  $vce1$ ,  $vce2$ ,  $vce3$ ,  $tcp1$ ,  $tcp2$ ,  $vcp1$ ,  $vcp2$ , and  $vcp3$  may not be found in the following table of median sheet resistance values and their corresponding variations.

To avoid simulation iteration problems, such as the occurrence of zero or negative resistances, the *empirical hyperbolic tangent equation* was used instead of a second order polynomial equation.

For temperature dependence modeling, the second order polynomial equation used by other resistor models is also employed here. Finally, the median sheet resistance values and their corresponding variations,  $R_{end0}$ , temperature coefficients, voltage coefficients extracted based on the methodology described above are reported in section 13.11. The simulation results of PCM pattern are listed in section 13.11.

## 13.15 Unsilicided N+/P+ Diffusion Resistors Models

Two types of unsilicided diffusion resistor, N+ and P+, are available. These resistors were measured by sweeping current over one node while the other node was grounded.

TSMC's reliability team suggests that these resistors might display reliability limitations if the applied current density exceeds  $800 \mu\text{A}/\mu\text{m}$ . Thus, TSMC limits the valid current density range for the resistor models to between 0 and  $800 \mu\text{A}/\mu\text{m}$ . The corresponding voltage range can be obtained using Ohm's law. TSMC further limits the application of these models only to resistors with widths  $\geq 0.4 \mu\text{m}$ , lengths  $\geq 0.8 \mu\text{m}$ , and square number  $\geq 1.0$ .



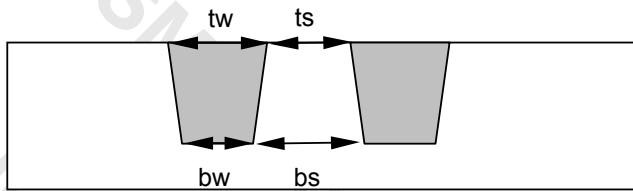
It is strongly recommended that users apply these models within valid current, voltage, and dimension ranges. An operation outside any of these ranges will lead to a significant error.

The cross-section schematic of the unsilicided diffusion resistor structure is similar to that of the unsilicided poly resistor structure. The difference is that the poly resistor is replaced with diffusion resistor. The same equivalent circuit as the unsilicided poly resistor models was employed to model these diffusion resistors. The important model parameters are listed in the section 13.11 and the simulation results of PCM pattern are listed in the section 13.11.

## 13.16 Interconnect Model

### 13.16.1 Conductor Layers

tw = top width of metal  
 bw = bottom width of metal  
 ts = top space of metal  
 bs = bottom space of metal



Profiles of CLN90 metal layers

	Typical Thickness (Å)	Maximum variation in thickness (%)	Minimum Drawn Width (μm)	Maximum Variation in width (%)	Minimum Drawn Spacing (μm)	Total Silicon Width Bias At bottom (μm)	Total Silicon Width bias At top (μm)	Distance between conductor layer and substrate under STI (Å)
M10 (AP RDL) on 3XTM	14500	+/-10	3	+/-10	2	0.389	-0.034	87150
M9 (3XTM)	8500	+20/-12	0.42	+/-10	0.42	0.005	0.144	68850
M8 (3XTM)	8500	+20/-12	0.42	+/-10	0.42	0.005	0.144	53200
M10 (AP RDL) on 2XTM	14500	+/-10	3	+/-10	2	0.389	-0.034	76050
M9 (2XTM)	5600	+20/-12	0.28	+/-10	0.42	-0.018	0.43	62450
M8 (2XTM)	5600	+20/-12	0.28	+/-10	0.42	-0.018	0.43	52350
M7	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	44750
M6	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	38450
M5	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	32150
M4	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	25850
M3	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	19550
M2	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	13250
M1	2400	+18/-10	0.12	+/-10	0.12	-0.002	0.038	7650
PO	1500	+/-10	0.1	+/-7	0.15	-0.02	-0.02	3700

## Profiles of CLN85 and CMN85 metal layers

	Typical Thickness (Å)	Maximum variation in thickness (%)	Minimum Drawn Width (µm)	Maximum Variation in width (%)	Minimum Drawn Spacing (µm)	Total Silicon Width Bias At bottom (µm)	Total Silicon Width bias At top (µm)	Distance between conductor layer and substrate under STI (Å)
<b>M10 (AP RDL)</b>	14500	+/-10	3	+/-10	2	0.389	-0.034	87150
<b>M9</b>	8500	+20/-12	0.395	+/-10	0.395	0.005	0.144	70650
<b>M8</b>	8500	+20/-12	0.395	+/-10	0.395	0.005	0.144	55000
<b>M7</b>	3100	+19/-11	0.132	+/-10	0.132	-0.005	0.04	44750
<b>M6</b>	3100	+19/-11	0.132	+/-10	0.132	-0.005	0.04	38450
<b>M5</b>	3100	+19/-11	0.132	+/-10	0.132	-0.005	0.04	32150
<b>M4</b>	3100	+19/-11	0.132	+/-10	0.132	-0.005	0.04	25850
<b>M3</b>	3100	+19/-11	0.132	+/-10	0.132	-0.005	0.04	19550
<b>M2</b>	3100	+19/-11	0.132	+/-10	0.132	-0.005	0.04	13250
<b>M1</b>	2400	+18/-10	0.113	+/-10	0.113	-0.002	0.038	7650
<b>PO</b>	1500	+/-10	0.094	+/-7	0.132	-0.029	-0.029	3700

## Profiles of CLN80 and CMN80 metal layers

	Typical Thickness (Å)	Maximum variation in thickness (%)	Minimum Drawn Width (µm)	Maximum Variation in width (%)	Minimum Drawn Spacing (µm)	Total Silicon Width Bias At bottom (µm)	Total Silicon Width bias At top (µm)	Distance between conductor layer and substrate under STI (Å)
<b>M10 (AP RDL) on 3XTM</b>	14500	+/-10	2.7	+/-10	1.8	0.35	-0.03	73500
<b>M9 (3XTM)</b>	8500	+20/-12	0.378	+/-10	0.378	0.012	0.085	57000
<b>M8 (3XTM)</b>	8500	+20/-12	0.378	+/-10	0.378	0.012	0.085	42800
<b>M7</b>	2,600	+19/-11	0.126	+/-10	0.126	-0.001	0.032	34500
<b>M6</b>	2,600	+19/-11	0.126	+/-10	0.126	-0.001	0.032	29900
<b>M5</b>	2,600	+19/-11	0.126	+/-10	0.126	-0.001	0.032	25300
<b>M4</b>	2,600	+19/-11	0.126	+/-10	0.126	-0.001	0.032	20700
<b>M3</b>	2,600	+19/-11	0.126	+/-10	0.126	-0.001	0.032	16100
<b>M2</b>	2,600	+19/-11	0.126	+/-10	0.126	-0.001	0.032	11500
<b>M1</b>	2,300	+18/-10	0.108	+/-10	0.108	-0.009	0.024	7200
<b>PO</b>	1200	+/-10	0.09	+/-7	0.135	-0.031	-0.02	3700

## Profiles of CMN90 metal layers

	Typical Thickness (Å)	Maximum variation in thickness (%)	Minimum Drawn Width (µm)	Maximum Variation in width (%)	Minimum Drawn Spacing (µm)	Total Silicon Width Bias At bottom (µm)	Total Silicon Width bias At top (µm)	Distance between conductor layer and substrate under STI (Å)
<b>M10 (AP RDL)</b>	14500	+/-10	3	+/-10	2	0.389	-0.034	112,900
<b>M9 (UTM)</b>	34000	+20/-12	2	+/-10	2	0.006	0.272	70,900
<b>M8 (3XTM)</b>	8500	+20/-12	0.42	+/-10	0.42	0.005	0.144	55,000
<b>M7</b>	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	44750
<b>M6</b>	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	38450
<b>M5</b>	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	32150
<b>M4</b>	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	25850
<b>M3</b>	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	19550
<b>M2</b>	3100	+19/-11	0.14	+/-10	0.14	-0.005	0.04	13250
<b>M1</b>	2400	+18/-10	0.12	+/-10	0.12	-0.002	0.038	7650
<b>PO</b>	1500	+/-10	0.1	+/-7	0.15	-0.02	-0.02	3700

## 13.16.2 Dielectric Layers

### 13.16.2.1 CLN90 3XTM

Dielectric Name	Thickness (Å)	Variation +/- (%)	dielectric constant	Comments
PASS6	6,000	10	8.1	Side-wall thickness 4600A
PASS5	4,000	10	4.2	Side-wall thickness 3000A
PASS4	2,500	10	4.2	
PASS3	750	10	8.1	
PASS2	4,000	10	4.2	
PASS1	750	10	8.1	
IMD9c	7,400	20/-12	4.2	
IMD9b	500	5	8.1	
IMD9a	7,250	7	4.2	IMD9a recess 600A after M9
IMD8d	500	5	5	
IMD8c	7,400	20/-12	4.2	
IMD8b	500	5	8.1	
IMD8a	7,250	7	4.2	IMD8a recess 600A after M8
IMD7c	500	5	5	
IMD7b	3,100	19/-11	2.9	
IMD7a	2,400	10	2.9	
IMD6d	300	10	4.2	
IMD6c	500	5	5	
IMD6b	3,100	19/-11	2.9	
IMD6a	2,400	10	2.9	
IMD5d	300	10	4.2	
IMD5c	500	5	5	
IMD5b	3,100	19/-11	2.9	
IMD5a	2,400	10	2.9	
IMD4d	300	10	4.2	
IMD4c	500	5	5	
IMD4b	3,100	19/-11	2.9	
IMD4a	2,400	10	2.9	
IMD3d	300	10	4.2	
IMD3c	500	5	5	
IMD3b	3,100	19/-11	2.9	
IMD3a	2,400	10	2.9	
IMD2d	300	10	4.2	
IMD2c	500	5	5	
IMD2b	3,100	19/-11	2.9	
IMD2a	2,400	10	2.9	
IMD1d	300	10	4.2	
IMD1c	500	5	5	
IMD1b	1,800	18/-10	2.9	
IMD1a	350	5	4.5	
ILD	4,400	15	4.2	ILD recess 250A after M1 etch
FOX	3,500	10	3.9	For Spacer and Liner, see

**NOTE 1:** The depth of the STI is 3500 Å, while the final thickness of the STI under PO is 3700 Å.  
 This means that the STI is about 200 Å higher than the OD.

**Note 2:** The spacer and liner around the Poly have been added to the cross-sectional schematic and are shown approximately. Their effective widths and dielectric constants are (550 Å, 6.0) for the dotted area and (150 Å, 5.5) for thick-lined area, respectively

### 13.16.2.2 CLN90 2XTM

Dielectric Name	Thickness (Å)	Variation +/- (%)	dielectric constant	Comments
PASS6	6000	10	8.1	Side-wall thickness 4600A
PASS5	4000	10	4.2	Side-wall thickness 3000A
PASS4	2500	10	4.2	
PASS3	750	10	8.1	
PASS2	4000	10	4.2	
PASS1	750	10	8.1	
IMD9c	4800	+20/-12	4.2	
IMD9b	300	5	8.1	
IMD9a	4500	7	4.2	IMD9a recess 500A after M9 etch
IMD8d	500	5	5	
IMD8c	4800	+20/-12	4.2	
IMD8b	300	5	8.1	
IMD8a	4500	7	4.2	IMD8a recess 500A after M8 etch
IMD2~7d	300	5	4.2	
IMD2~7c	500	5	5	
IMD2~7b	3100	+19/-11	2.9	
IMD2~7a	2400	10	2.9	
IMD1d	300	5	4.2	
IMD1c	500	5	5	
IMD1b	1800	+18/-10	2.9	
IMD1a	350	5	4.5	
ILD	4400	15	4.2	ILD recess 250A after M1 etch
STI	3500	10	3.9	Note 1/2

**NOTE 1:** The depth of the STI is 3500 Å, while the final thickness of the STI under PO is 3700 Å.  
 This means that the STI is about 200 Å higher than the OD.

**Note 2:** The spacer and liner around the Poly have been added to the cross-sectional schematic and are shown approximately. Their effective widths and dielectric constants are (550 Å, 6.0) for the dotted area and (150 Å, 5.5) for thick-lined area, respectively

### 13.16.2.3 CLN85 and CMN85 3XTM

Dielectric Name	Thickness (Å)	Variation +/- (%)	dielectric constant	Comments
PASS6	6,000	10	8.1	Side-wall thickness 4600A
PASS5	4,000	10	4.2	Side-wall thickness 3000A
PASS4	2,500	10	4.2	
PASS3	750	10	8.1	
PASS2	4,000	10	4.2	
PASS1	750	10	8.1	
IMD9c	7,400	+20/-12	4.2	
IMD9b	500	5	8.1	
IMD9a	7,250	7	4.2	IMD9a recess 600A after M9
IMD8d	500	5	5	
IMD8c	7,400	+20/-12	4.2	
IMD8b	500	5	8.1	
IMD8a	7,250	7	4.2	IMD8a recess 600A after M8
IMD7c	500	5	5	
IMD7b	3,100	+19/-11	2.9	
IMD7a	2,400	10	2.9	
IMD6d	300	10	4.2	
IMD6c	500	5	5	
IMD6b	3,100	+19/-11	2.9	
IMD6a	2,400	10	2.9	
IMD5d	300	10	4.2	
IMD5c	500	5	5	
IMD5b	3,100	+19/-11	2.9	
IMD5a	2,400	10	2.9	
IMD4d	300	10	4.2	
IMD4c	500	5	5	
IMD4b	3,100	+19/-11	2.9	
IMD4a	2,400	10	2.9	
IMD3d	300	10	4.2	
IMD3c	500	5	5	
IMD3b	3,100	+19/-11	2.9	
IMD3a	2,400	10	2.9	
IMD2d	300	10	4.2	
IMD2c	500	5	5	
IMD2b	3,100	+19/-11	2.9	
IMD2a	2,400	10	2.9	
IMD1d	300	10	4.2	
IMD1c	500	5	5	
IMD1b	1,800	+18/-10	2.9	
IMD1a	350	5	4.5	
ILD	4,400	15	4.2	ILD recess 250A after M1 etch
FOX	3,500	10	3.9	For Spacer and Liner, see

**NOTE 1:** The depth of the STI is 3500 Å, while the final thickness of the STI under PO is 3700 Å.  
 This means that the STI is about 200 Å higher than the OD.

**Note 2:** The spacer and liner around the Poly have been added to the cross-sectional schematic and are shown approximately. Their effective widths and dielectric constants are (550 Å, 6.0) for the dotted area and (150 Å, 5.5) for thick-lined area, respectively

### 13.16.2.4 CLN80 and CMN80 3XTM

Dielectric Name	Thickness (Å)	Variation +/- (%)	dielectric constant	Comments
PASS6	6000	10	8.1	
PASS5	4000	10	4.2	
PASS4	2500	10	4.2	
PASS3	750	10	8.1	
PASS2	4000	10	4.2	
PASS1	750	10	8.1	
IMD9c	7000	+20/-12	4.2	
IMD9b	500	5	8.1	
IMD9a	6200	7	4.2	IMD9a recess 1000A after M9 etch
IMD8d	500	5	5	
IMD8c	7000	+20/-12	4.2	
IMD8b	500	5	8.1	
IMD8a	6200	7	4.2	IMD8a recess 1000A after M8 etch
IMD2~7c	500	5	5	
IMD2~7b	2600	+19/-11	2.9	
IMD2~7a	1200	10	2.9	
IMD1c	500	5	5	
IMD1b	1650	+18/-10	2.9	
IMD1a	350	5	4.5	
ILD	4000	15	4.2	ILD recess 300A after M1 etch
STI	3500	10	3.9	Note 1/2

**NOTE 1:** The depth of the STI is 3500 Å, while the final thickness of the STI under PO is 3700 Å.  
 This means that the STI is about 200 Å higher than the OD.

**Note 2:** The spacer and liner around the Poly have been added to the cross-sectional schematic and are shown approximately. Their effective widths and dielectric constants are (520 Å, 6.0) for the dotted area and (100 Å, 7) for thick-lined area, respectively

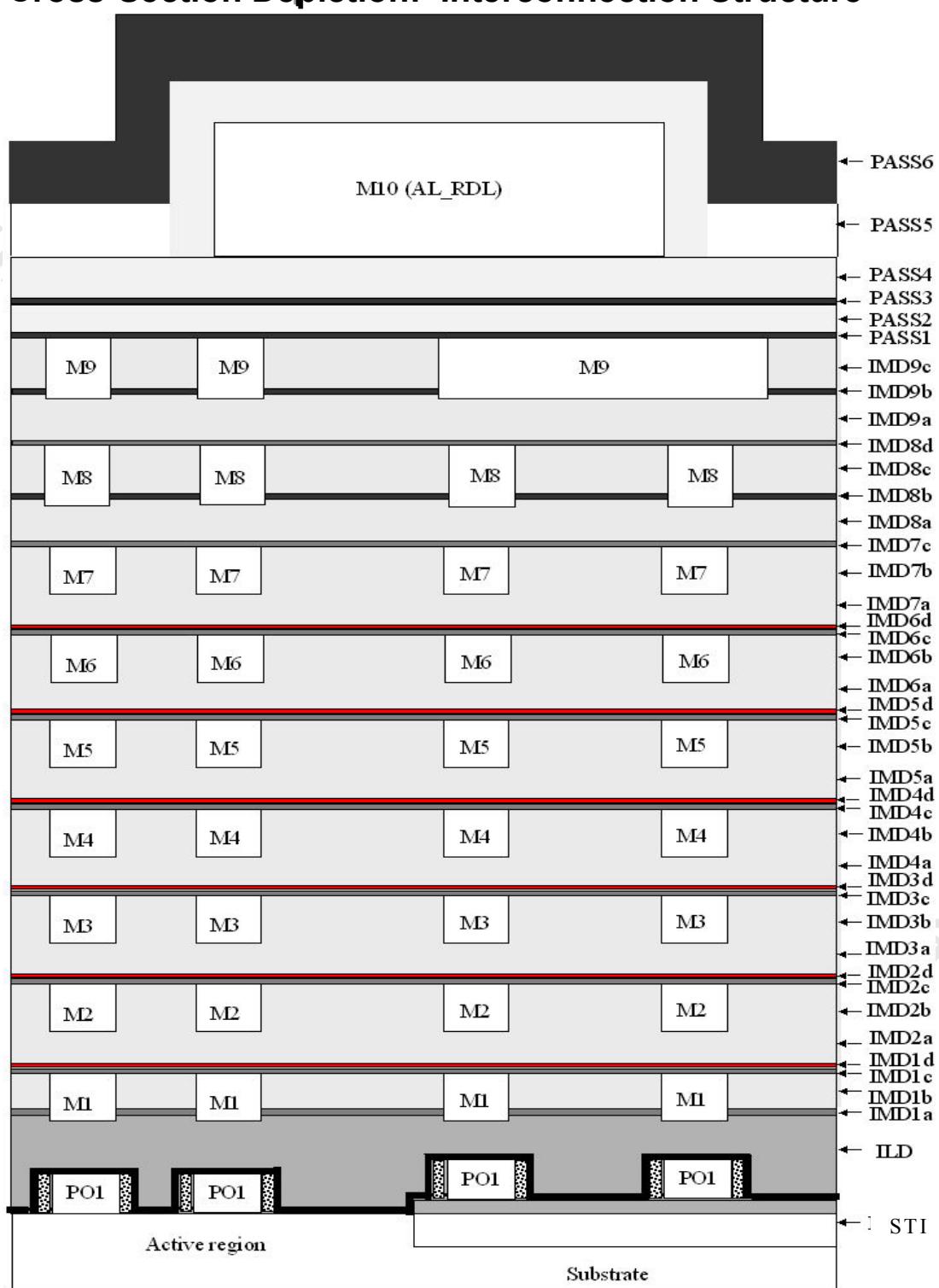
## 13.16.2.5CLM90

Dielectric Name	Thickness (Å)	Variation +/- (%)	dielectric constant	Comments
PASS6	6000	10	8.1	Side-wall thickness 4600A
PASS5	4000	10	4.2	Side-wall thickness 3000A
PASS4	2500	10	4.2	
PASS3	750	10	8.1	
PASS2	4000	10	4.2	
PASS1	750	10	8.1	
IMD9c	32300	+20/-20	4.2	
IMD9b	1100	10	8.1	
IMD9a	7250	7	4.2	IMD9a recess 600A after M9 etch
IMD8d	750	10	8.1	
IMD8c	7400	+20/-12	4.2	
IMD8b	500	5	8.1	
IMD8a	7250	7	4.2	IMD8a recess 600A after M8 etch
IMD2~7c	500	5	5	
IMD2~7b	3100	+19/-11	2.9	
IMD2~7a	2400	10	2.9	
IMD1c	500	5	4.5	
IMD1b	1800	+18/-10	2.9	
IMD1a	350	5	4.5	
ILD	4400	15	4.2	ILD recess 250A after M1 etch
STI	3500	10	3.9	Note 1/2

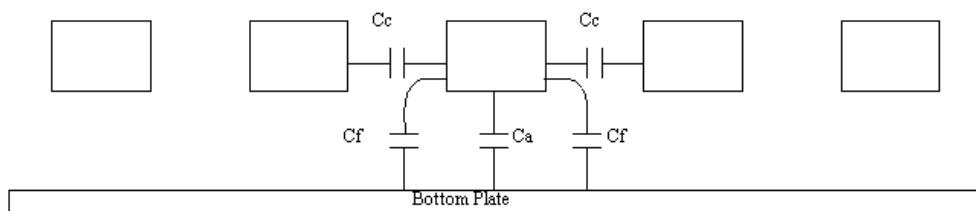
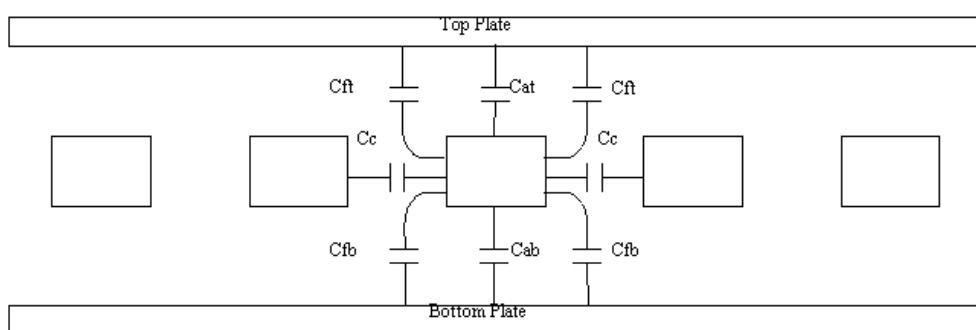
NOTE 1: The depth of the STI is 3500 Å, while the final thickness of the STI under PO is 3700 Å.  
 This means that the STI is about 200 Å higher than the OD.

Note 2: The spacer and liner around the Poly have been added to the cross-sectional schematic and are shown approximately. Their effective widths and dielectric constants are (550 Å, 6.0) for the dotted area and (150 Å, 5.5) for thick-lined area, respectively

## Cross-Section Depiction: Interconnection Structure



### 13.16.3 Conductors Array Between Two Infinite Plates

**Structure A****Structure B**

The information in the following table applies to the structure in the preceding figure.

(a) Structure A

<b>Structure A</b>	
$C_c$	Coupling capacitance between top central trace and its neighboring traces
$C_a$	Area capacitance between top central trace and infinite bottom ground plate
$C_f$	Fringe capacitance per side between top central trace and infinite bottom ground plate
$C_{bottom}$	$C_a + 2C_f$
$C_{sum}$	$C_a + 2C_f + 2C_c$
$C_{total}$	Total capacitance of the top central trace

(b) Structure B

<b>Structure B</b>	
$C_c$	Coupling capacitance between the middle central trace and its neighboring traces
$C_{at}$	Area capacitance between middle central trace and infinite top ground plate
$C_{ab}$	Area capacitance between middle central trace and infinite bottom ground plate
$C_{ft}$	Fringe capacitance per side between top central trace and infinite top ground plate
$C_{fb}$	Fringe capacitance per side between top central trace and infinite bottom ground plate
$C_{top}$	$C_{at} + 2C_{ft}$
$C_{bottom}$	$C_{ab} + 2C_{fb}$
$C_{sum}$	$(C_{at} + 2C_{ft}) + (C_{ab} + 2C_{fb}) + 2C_c$
$C_{total}$	Total capacitance of the middle central trace

### 13.16.3.1 M1MxMz process in CLN90G 1.0V/2.5V, no My/Mu, x=2~7, z=8~9

(a) Structure A 25 °C

Structure	(as drawn)		(after process bias)								
	width (um)	space (um)	Width (um)	Space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Ca (fF/um)	Cf (fF/um)	Csum/Ctotal
PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.60E-01	6.00E-02	2.71E-02	6.07E-03	1.05E-02	91.90%
	0.1	1.965	0.065	2	1.13E+01	8.99E-02	3.75E-03	8.08E-02	6.07E-03	3.74E-02	98.20%
M1-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.46E-01	1.07E-01	1.61E-02	6.47E-03	4.80E-03	93.90%
	0.12	2	0.1806	1.939	7.77E-02	7.96E-02	6.77E-03	6.32E-02	8.46E-03	2.73E-02	96.30%
M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.49E-01	1.06E-01	2.54E-02	1.24E-02	6.52E-03	95.20%
	0.12	2	0.1806	1.939	7.77E-02	9.91E-02	4.07E-03	8.87E-02	1.62E-02	3.63E-02	97.70%
M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.53E-01	1.03E-01	3.69E-02	1.94E-02	8.78E-03	96.20%
	0.12	2	0.1806	1.939	7.77E-02	1.18E-01	3.11E-03	1.10E-01	2.53E-02	4.25E-02	98.40%
M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.54E-01	1.03E-01	3.95E-02	2.09E-02	9.29E-03	96.30%
	0.12	2	0.1806	1.939	7.77E-02	1.22E-01	2.98E-03	1.14E-01	2.74E-02	4.35E-02	98.50%
M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.84E-02	1.17E-02	3.82E-03	3.92E-03	93.80%
	0.14	2	0.1785	1.961	5.89E-02	6.53E-02	9.79E-03	4.14E-02	4.34E-03	1.85E-02	93.40%
M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.80E-02	1.37E-02	5.08E-03	4.30E-03	94.30%
	0.14	2	0.1785	1.961	5.89E-02	6.94E-02	8.25E-03	4.92E-02	5.76E-03	2.17E-02	94.80%
M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.77E-02	1.49E-02	5.84E-03	4.54E-03	94.50%
	0.14	2	0.1785	1.961	5.89E-02	7.20E-02	7.56E-03	5.34E-02	6.62E-03	2.34E-02	95.30%
M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.76E-02	1.51E-02	5.96E-03	4.57E-03	94.60%
	0.14	2	0.1785	1.961	5.89E-02	7.24E-02	7.46E-03	5.41E-02	6.75E-03	2.37E-02	95.30%
M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.33E-02	2.84E-02	1.40E-02	7.23E-03	96.20%
	0.14	2	0.1785	1.961	5.89E-02	9.55E-02	4.55E-03	8.40E-02	1.58E-02	3.41E-02	97.50%
M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	9.16E-03	2.44E-03	3.36E-03	93.20%
	0.14	2	0.1785	1.961	5.89E-02	5.99E-02	1.17E-02	3.10E-02	2.77E-03	1.41E-02	91.00%
M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	9.96E-03	2.90E-03	3.53E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.14E-02	1.09E-02	3.48E-02	3.28E-03	1.58E-02	92.10%
M3-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.71E-02	1.04E-02	3.13E-03	3.62E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.23E-02	1.05E-02	3.66E-02	3.55E-03	1.65E-02	92.50%
M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	1.00E-01	1.04E-02	3.16E-03	3.64E-03	93.60%
	0.14	2	0.1785	1.961	5.89E-02	6.24E-02	1.05E-02	3.68E-02	3.59E-03	1.66E-02	92.60%
M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.72E-02	1.27E-02	4.55E-03	4.09E-03	94.00%
	0.14	2	0.1785	1.961	5.89E-02	6.73E-02	8.67E-03	4.61E-02	5.15E-03	2.05E-02	94.30%
M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.50E-02	2.85E-02	1.40E-02	7.27E-03	96.30%
	0.14	2	0.1785	1.961	5.89E-02	9.54E-02	4.50E-03	8.40E-02	1.58E-02	3.41E-02	97.50%
M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.86E-02	7.94E-03	1.79E-03	3.07E-03	92.80%
	0.14	2	0.1785	1.961	5.89E-02	5.78E-02	1.30E-02	2.53E-02	2.03E-03	1.16E-02	88.70%
M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.86E-02	8.38E-03	2.03E-03	3.18E-03	93.00%
	0.14	2	0.1785	1.961	5.89E-02	5.85E-02	1.25E-02	2.75E-02	2.30E-03	1.26E-02	89.60%
M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.92E-02	8.58E-03	2.14E-03	3.22E-03	93.10%
	0.14	2	0.1785	1.961	5.89E-02	5.89E-02	1.22E-02	2.85E-02	2.42E-03	1.30E-02	90.00%
M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.92E-02	8.61E-03	2.15E-03	3.23E-03	93.10%
	0.14	2	0.1785	1.961	5.89E-02	5.89E-02	1.22E-02	2.86E-02	2.44E-03	1.31E-02	90.10%
M4-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	9.63E-03	2.72E-03	3.46E-03	93.30%
	0.14	2	0.1785	1.961	5.89E-02	6.09E-02	1.12E-02	3.35E-02	3.08E-03	1.52E-02	91.60%
M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	1.28E-02	4.55E-03	4.12E-03	94.10%
	0.14	2	0.1785	1.961	5.89E-02	6.73E-02	8.55E-03	4.62E-02	5.15E-03	2.05E-02	94.10%
M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.52E-02	2.85E-02	1.40E-02	7.29E-03	96.30%
	0.14	2	0.1785	1.961	5.89E-02	9.55E-02	4.47E-03	8.41E-02	1.58E-02	3.42E-02	97.40%
M5-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.91E-02	7.24E-03	1.42E-03	2.91E-03	92.60%
	0.14	2	0.1785	1.961	5.89E-02	5.70E-02	1.38E-02	2.17E-02	1.60E-03	1.00E-02	86.50%
M5-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.87E-02	7.54E-03	1.56E-03	2.99E-03	92.70%
	0.14	2	0.1785	1.961	5.89E-02	5.74E-02	1.35E-02	2.31E-02	1.77E-03	1.07E-02	87.30%
M5-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.87E-02	7.67E-03	1.62E-03	3.02E-03	92.70%
	0.14	2	0.1785	1.961	5.89E-02	5.75E-02	1.33E-02	2.37E-02	1.84E-03	1.09E-02	87.60%
M5-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.87E-02	7.69E-03	1.63E-03	3.03E-03	92.80%
	0.14	2	0.1785	1.961	5.89E-02	5.75E-02	1.33E-02	2.38E-02	1.85E-03	1.10E-02	87.60%
M5-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.77E-02	8.28E-03	1.94E-03	3.17E-03	92.90%
	0.14	2	0.1785	1.961	5.89E-02	5.85E-02	1.26E-02	2.67E-02	2.19E-03	1.23E-02	88.90%
M5-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.97E-02	9.70E-03	2.72E-03	3.49E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.11E-02	1.11E-02	3.35E-02	3.08E-03	1.52E-02	91.20%
M5-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.76E-02	1.29E-02	4.55E-03	4.16E-03	94.10%
	0.14	2	0.1785	1.961	5.89E-02	6.76E-02	8.52E-03	4.64E-02	5.15E-03	2.06E-02	93.90%
M5-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.50E-02	2.86E-02	1.40E-02	7.34E-03	96.30%
	0.14	2	0.1785	1.961	5.89E-02	9.56E-02	4.45E-03	8.41E-02	1.58E-02	3.41E-02	97.30%
M6-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.91E-02	6.86E-03	1.17E-03	2.85E-03	92.40%
	0.14	2	0.1785	1.961	5.89E-02	5.73E-02	1.45E-02	1.91E-02	1.33E-03	8.91E-03	84.20%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M6-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.88E-02	7.09E-03	1.27E-03	2.91E-03	92.50%
	0.14	2	0.1785	1.961	5.89E-02	5.76E-02	1.43E-02	2.02E-02	1.43E-03	9.37E-03	84.80%
M6-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.88E-02	7.18E-03	1.31E-03	2.94E-03	92.50%
	0.14	2	0.1785	1.961	5.89E-02	5.77E-02	1.42E-02	2.06E-02	1.48E-03	9.57E-03	85.10%
M6-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.88E-02	7.20E-03	1.31E-03	2.94E-03	92.50%
	0.14	2	0.1785	1.961	5.89E-02	5.77E-02	1.42E-02	2.07E-02	1.49E-03	9.60E-03	85.10%
M6-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.96E-02	7.61E-03	1.50E-03	3.06E-03	92.70%
	0.14	2	0.1785	1.961	5.89E-02	5.82E-02	1.38E-02	2.26E-02	1.71E-03	1.05E-02	86.20%
M6-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.91E-02	8.47E-03	1.94E-03	3.27E-03	93.00%
	0.14	2	0.1785	1.961	5.89E-02	5.94E-02	1.28E-02	2.68E-02	2.19E-03	1.23E-02	88.10%
M6-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	9.94E-03	2.72E-03	3.61E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.20E-02	1.12E-02	3.36E-02	3.08E-03	1.53E-02	90.50%
M6-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.86E-02	1.31E-02	4.55E-03	4.29E-03	94.20%
	0.14	2	0.1785	1.961	5.89E-02	6.85E-02	8.67E-03	4.65E-02	5.15E-03	2.07E-02	93.20%
M6-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.47E-02	2.89E-02	1.40E-02	7.48E-03	96.30%
	0.14	2	0.1785	1.961	5.89E-02	9.63E-02	4.61E-03	8.42E-02	1.58E-02	3.42E-02	97.00%
M7-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.92E-02	6.84E-03	9.97E-04	2.92E-03	90.90%
	0.14	2	0.1785	1.961	5.89E-02	6.20E-02	1.69E-02	1.73E-02	1.13E-03	8.06E-03	82.30%
M7-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.92E-02	7.03E-03	1.07E-03	2.98E-03	91.00%
	0.14	2	0.1785	1.961	5.89E-02	6.21E-02	1.67E-02	1.81E-02	1.21E-03	8.43E-03	82.80%
M7-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.92E-02	7.11E-03	1.10E-03	3.01E-03	91.00%
	0.14	2	0.1785	1.961	5.89E-02	6.21E-02	1.66E-02	1.84E-02	1.24E-03	8.58E-03	83.00%
M7-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.92E-02	7.12E-03	1.10E-03	3.01E-03	91.00%
	0.14	2	0.1785	1.961	5.89E-02	6.22E-02	1.66E-02	1.84E-02	1.25E-03	8.60E-03	83.00%
M7-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	1.00E-01	7.42E-03	1.23E-03	3.10E-03	91.20%
	0.14	2	0.1785	1.961	5.89E-02	6.25E-02	1.63E-02	1.98E-02	1.39E-03	9.20E-03	83.90%
M7-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.99E-02	8.10E-03	1.50E-03	3.30E-03	91.40%
	0.14	2	0.1785	1.961	5.89E-02	6.31E-02	1.56E-02	2.27E-02	1.71E-03	1.05E-02	85.40%
M7-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.29E-01	1.00E-01	9.05E-03	1.94E-03	3.56E-03	91.80%
	0.14	2	0.1785	1.961	5.89E-02	6.44E-02	1.46E-02	2.70E-02	2.19E-03	1.24E-02	87.20%
M7-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.29E-01	1.00E-01	1.06E-02	2.72E-03	3.94E-03	92.20%
	0.14	2	0.1785	1.961	5.89E-02	6.70E-02	1.30E-02	3.39E-02	3.08E-03	1.54E-02	89.50%
M7-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.85E-02	1.39E-02	4.55E-03	4.67E-03	93.00%
	0.14	2	0.1785	1.961	5.89E-02	7.36E-02	1.04E-02	4.71E-02	5.15E-03	2.10E-02	92.40%
M7-M6	0.14	0.14	0.1575	0.1225	7.20E-02	2.34E-01	9.63E-02	3.01E-02	1.40E-02	8.05E-03	95.20%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	5.96E-03	8.61E-02	1.58E-02	3.51E-02	96.60%
M8-FOX	0.42	0.42	0.4945	0.3455	2.21E-02	3.01E-01	1.35E-01	9.17E-03	2.62E-03	3.28E-03	92.90%
	0.42	2	0.5005	1.919	2.00E-02	1.10E-01	3.91E-02	1.65E-02	2.65E-03	6.91E-03	86.30%
M8-OD	0.42	0.42	0.4945	0.3455	2.21E-02	3.00E-01	1.35E-01	9.45E-03	2.76E-03	3.34E-03	92.90%
	0.42	2	0.5005	1.919	2.00E-02	1.10E-01	3.90E-02	1.71E-02	2.80E-03	7.16E-03	86.50%
M8-PO1(OD)	0.42	0.42	0.4945	0.3455	2.21E-02	3.00E-01	1.35E-01	9.57E-03	2.83E-03	3.37E-03	92.90%
	0.42	2	0.5005	1.919	2.00E-02	1.10E-01	3.89E-02	1.74E-02	2.86E-03	7.28E-03	86.60%
M8-PO1(FOX)	0.42	0.42	0.4945	0.3455	2.21E-02	3.00E-01	1.35E-01	9.59E-03	2.84E-03	3.38E-03	92.90%
	0.42	2	0.5005	1.919	2.00E-02	1.10E-01	3.89E-02	1.75E-02	2.87E-03	7.29E-03	86.60%
M8-M1	0.42	0.42	0.4945	0.3455	2.21E-02	3.01E-01	1.35E-01	1.01E-02	3.11E-03	3.51E-03	93.10%
	0.42	2	0.5005	1.919	2.00E-02	1.10E-01	3.87E-02	1.87E-02	3.14E-03	7.78E-03	87.10%
M8-M2	0.42	0.42	0.4945	0.3455	2.21E-02	3.03E-01	1.36E-01	1.11E-02	3.64E-03	3.73E-03	93.30%
	0.42	2	0.5005	1.919	2.00E-02	1.11E-01	3.82E-02	2.12E-02	3.69E-03	8.73E-03	87.80%
M8-M3	0.42	0.42	0.4945	0.3455	2.21E-02	3.03E-01	1.35E-01	1.25E-02	4.40E-03	4.03E-03	93.60%
	0.42	2	0.5005	1.919	2.00E-02	1.12E-01	3.74E-02	2.45E-02	4.45E-03	1.00E-02	88.70%
M8-M4	0.42	0.42	0.4945	0.3455	2.21E-02	3.04E-01	1.35E-01	1.45E-02	5.55E-03	4.47E-03	93.90%
	0.42	2	0.5005	1.919	2.00E-02	1.14E-01	3.63E-02	2.96E-02	5.62E-03	1.20E-02	89.70%
M8-M5	0.42	0.42	0.4945	0.3455	2.21E-02	3.03E-01	1.34E-01	1.79E-02	7.52E-03	5.19E-03	94.40%
	0.42	2	0.5005	1.919	2.00E-02	1.17E-01	3.45E-02	3.79E-02	7.62E-03	1.51E-02	91.10%
M8-M6	0.42	0.42	0.4945	0.3455	2.21E-02	3.06E-01	1.33E-01	2.50E-02	1.17E-02	6.64E-03	95.30%
	0.42	2	0.5005	1.919	2.00E-02	1.25E-01	3.12E-02	5.34E-02	1.18E-02	2.08E-02	92.60%
M8-M7	0.42	0.42	0.4945	0.3455	2.21E-02	3.15E-01	1.28E-01	4.84E-02	2.60E-02	1.12E-02	96.50%
	0.42	2	0.5005	1.919	2.00E-02	1.53E-01	2.46E-02	9.63E-02	2.63E-02	3.50E-02	94.80%
M9-FOX	0.42	0.42	0.4945	0.3455	2.21E-02	3.24E-01	1.46E-01	8.19E-03	2.15E-03	3.02E-03	92.60%
	0.42	2	0.5005	1.919	2.00E-02	1.16E-01	4.25E-02	1.38E-02	2.17E-03	5.83E-03	85.30%
M9-OD	0.42	0.42	0.4945	0.3455	2.21E-02	3.21E-01	1.44E-01	8.38E-03	2.25E-03	3.07E-03	92.50%
	0.42	2	0.5005	1.919	2.00E-02	1.16E-01	4.23E-02	1.43E-02	2.27E-03	6.00E-03	85.30%
M9-PO1(OD)	0.42	0.42	0.4945	0.3455	2.21E-02	3.21E-01	1.44E-01	8.46E-03	2.29E-03	3.09E-03	92.60%
	0.42	2	0.5005	1.919	2.00E-02	1.16E-01	4.23E-02	1.45E-02	2.32E-03	6.07E-03	85.30%
M9-PO1(FOX)	0.42	0.42	0.4945	0.3455	2.21E-02	3.21E-01	1.44E-01	8.47E-03	2.29E-03	3.09E-03	92.60%
	0.42	2	0.5005	1.919	2.00E-02	1.16E-01	4.23E-02	1.45E-02	2.32E-03	6.08E-03	85.40%
M9-M1	0.42	0.42	0.4945	0.3455	2.21E-02	3.19E-01	1.43E-01	8.83E-03	2.47E-03	3.18E-03	92.60%
	0.42	2	0.5005	1.919	2.00E-02	1.16E-01	4.22E-02	1.52E-02	2.50E-03	6.37E-03	85.70%
M9-M2	0.42	0.42	0.4945	0.3455	2.21E-02	3.18E-01	1.43E-01	9.47E-03	2.79E-03	3.34E-03	92.70%
	0.42	2	0.5005	1.919	2.00E-02	1.16E-01	4.19E-02	1.67E-02	2.83E-03	6.92E-03	86.20%
M9-M3	0.42	0.42	0.4945	0.3455	2.21E-02	3.21E-01	1.44E-01	1.02E-02	3.22E-03	3.50E-03	92.90%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.42	2	0.5005	1.919	2.00E-02	1.17E-01	4.14E-02	1.86E-02	3.26E-03	7.66E-03	86.90%
M9-M4	0.42	0.42	0.4945	0.3455	2.21E-02	3.21E-01	1.44E-01	1.13E-02	3.80E-03	3.74E-03	93.10%
	0.42	2	0.5005	1.919	2.00E-02	1.18E-01	4.10E-02	2.11E-02	3.84E-03	8.64E-03	87.70%
M9-M5	0.42	0.42	0.4945	0.3455	2.21E-02	3.18E-01	1.42E-01	1.28E-02	4.62E-03	4.07E-03	93.40%
	0.42	2	0.5005	1.919	2.00E-02	1.18E-01	4.00E-02	2.47E-02	4.68E-03	9.99E-03	88.60%
M9-M6	0.42	0.42	0.4945	0.3455	2.21E-02	3.20E-01	1.42E-01	1.50E-02	5.92E-03	4.52E-03	93.80%
	0.42	2	0.5005	1.919	2.00E-02	1.20E-01	3.88E-02	3.02E-02	5.99E-03	1.21E-02	89.80%
M9-M7	0.42	0.42	0.4945	0.3455	2.21E-02	3.21E-01	1.42E-01	1.88E-02	8.21E-03	5.27E-03	94.40%
	0.42	2	0.5005	1.919	2.00E-02	1.23E-01	3.67E-02	3.94E-02	8.31E-03	1.56E-02	91.30%
M9-M8	0.42	0.42	0.4945	0.3455	2.21E-02	3.30E-01	1.35E-01	4.76E-02	2.60E-02	1.08E-02	96.30%
	0.42	2	0.5005	1.919	2.00E-02	1.57E-01	2.70E-02	9.51E-02	2.63E-02	3.44E-02	94.80%
M10-FOX	3	2	3.178	1.822	2.10E-02	1.73E-01	7.27E-02	1.96E-02	1.17E-02	3.94E-03	95.30%
	3	8	3.178	7.822	2.10E-02	8.68E-02	2.24E-02	3.81E-02	1.17E-02	1.32E-02	95.50%
M10-OD	3	2	3.178	1.822	2.10E-02	1.73E-01	7.23E-02	2.04E-02	1.21E-02	4.13E-03	95.50%
	3	8	3.178	7.822	2.10E-02	8.74E-02	2.21E-02	3.94E-02	1.21E-02	1.36E-02	95.60%
M10-PO1(OD)	3	2	3.178	1.822	2.10E-02	1.73E-01	7.23E-02	2.07E-02	1.23E-02	4.19E-03	95.50%
	3	8	3.178	7.822	2.10E-02	8.77E-02	2.20E-02	3.99E-02	1.23E-02	1.38E-02	95.70%
M10-PO1(FOX)	3	2	3.178	1.822	2.10E-02	1.73E-01	7.23E-02	2.07E-02	1.23E-02	4.19E-03	95.60%
	3	8	3.178	7.822	2.10E-02	8.77E-02	2.20E-02	4.00E-02	1.23E-02	1.38E-02	95.70%
M10-M1	3	2	3.178	1.822	2.10E-02	1.73E-01	7.17E-02	2.19E-02	1.31E-02	4.39E-03	95.80%
	3	8	3.178	7.822	2.10E-02	8.88E-02	2.15E-02	4.21E-02	1.31E-02	1.45E-02	95.80%
M10-M2	3	2	3.178	1.822	2.10E-02	1.74E-01	7.15E-02	2.40E-02	1.45E-02	4.73E-03	96.00%
	3	8	3.178	7.822	2.10E-02	9.04E-02	2.07E-02	4.58E-02	1.45E-02	1.57E-02	96.60%
M10-M3	3	2	3.178	1.822	2.10E-02	1.75E-01	7.08E-02	2.67E-02	1.63E-02	5.21E-03	96.40%
	3	8	3.178	7.822	2.10E-02	9.31E-02	1.98E-02	5.05E-02	1.63E-02	1.71E-02	96.80%
M10-M4	3	2	3.178	1.822	2.10E-02	1.75E-01	6.98E-02	3.01E-02	1.85E-02	5.82E-03	96.70%
	3	8	3.178	7.822	2.10E-02	9.63E-02	1.86E-02	5.63E-02	1.85E-02	1.89E-02	97.00%
M10-M5	3	2	3.178	1.822	2.10E-02	1.78E-01	6.91E-02	3.45E-02	2.14E-02	6.58E-03	97.10%
	3	8	3.178	7.822	2.10E-02	1.01E-01	1.73E-02	6.35E-02	2.14E-02	2.11E-02	97.30%
M10-M6	3	2	3.178	1.822	2.10E-02	1.81E-01	6.77E-02	4.07E-02	2.53E-02	7.69E-03	97.50%
	3	8	3.178	7.822	2.10E-02	1.07E-01	1.58E-02	7.31E-02	2.53E-02	2.39E-02	97.70%
M10-M7	3	2	3.178	1.822	2.10E-02	1.85E-01	6.57E-02	4.96E-02	3.11E-02	9.20E-03	97.80%
	3	8	3.178	7.822	2.10E-02	1.16E-01	1.39E-02	8.61E-02	3.11E-02	2.75E-02	98.00%
M10-M8	3	2	3.178	1.822	2.10E-02	2.04E-01	5.98E-02	8.12E-02	5.23E-02	1.45E-02	98.20%
	3	8	3.178	7.822	2.10E-02	1.50E-01	9.83E-03	1.28E-01	5.23E-02	3.81E-02	98.70%
M10-M9	3	2	3.178	1.822	2.10E-02	3.31E-01	4.68E-02	2.33E-01	1.62E-01	3.55E-02	98.90%
	3	8	3.178	7.822	2.10E-02	3.01E-01	5.15E-03	2.89E-01	1.62E-01	6.31E-02	99.40%

## (b) Structure B 25 °C

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M1-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.64E-01	5.24E-02	2.14E-02	6.07E-03	7.65E-03	3.41E-02	3.63E-03	1.52E-02	97.60%
	0.1	1.965	0.065	2	1.13E+01	1.19E-01	9.56E-05	4.70E-02	6.07E-03	2.05E-02	7.15E-02	3.63E-03	3.39E-02	100.00%
M2-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E-01	5.77E-02	2.26E-02	6.07E-03	8.24E-03	9.61E-03	2.46E-03	3.58E-03	93.90%
	0.1	1.965	0.065	2	1.13E+01	9.33E-02	6.48E-04	6.37E-02	6.07E-03	2.88E-02	2.83E-02	2.46E-03	1.29E-02	100.00%
M2-M1-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.50E-01	1.04E-01	1.18E-02	6.47E-03	2.68E-03	2.18E-02	1.22E-02	4.76E-03	96.70%
	0.12	2	0.1806	1.939	7.77E-02	1.14E-01	7.60E-04	4.13E-02	8.46E-03	1.64E-02	7.10E-02	1.60E-02	2.75E-02	100.00%
M2-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.52E-01	1.02E-01	2.13E-02	1.24E-02	4.45E-03	2.12E-02	1.22E-02	4.49E-03	97.90%
	0.12	2	0.1806	1.939	7.77E-02	1.27E-01	2.95E-04	6.38E-02	1.62E-02	2.38E-02	6.31E-02	1.60E-02	2.36E-02	100.00%
M2-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.56E-01	9.96E-02	3.25E-02	1.94E-02	6.57E-03	2.11E-02	1.22E-02	4.44E-03	98.70%
	0.12	2	0.1806	1.939	7.77E-02	1.44E-01	1.86E-04	8.46E-02	2.53E-02	2.96E-02	5.87E-02	1.60E-02	2.13E-02	100.00%
M2-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.57E-01	9.90E-02	3.50E-02	2.09E-02	7.04E-03	2.11E-02	1.22E-02	4.44E-03	98.80%
	0.12	2	0.1806	1.939	7.77E-02	1.47E-01	1.75E-04	8.88E-02	2.74E-02	3.07E-02	5.79E-02	1.60E-02	2.10E-02	100.00%
M3-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E-01	5.83E-02	2.37E-02	6.07E-03	8.81E-03	5.48E-03	1.31E-03	2.09E-03	93.00%
	0.1	1.965	0.065	2	1.13E+01	8.94E-02	1.40E-03	6.96E-02	6.07E-03	3.18E-02	1.69E-02	1.31E-03	7.80E-03	99.90%
M3-M1-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.44E-01	1.06E-01	1.24E-02	6.47E-03	2.98E-03	7.77E-03	3.98E-03	1.89E-03	95.00%
	0.12	2	0.1806	1.939	7.77E-02	8.82E-02	2.51E-03	5.05E-02	8.46E-03	2.10E-02	3.26E-02	5.21E-03	1.37E-02	99.90%
M3-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.47E-01	1.04E-01	2.20E-02	1.24E-02	4.80E-03	7.44E-03	3.98E-03	1.73E-03	96.30%
	0.12	2	0.1806	1.939	7.77E-02	1.06E-01	1.11E-03	7.53E-02	1.62E-02	2.96E-02	2.80E-02	5.21E-03	1.14E-02	100.00%
M3-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.32E-02	7.43E-03	3.82E-03	1.80E-03	2.56E-02	1.40E-02	5.81E-03	97.20%
	0.14	2	0.1785	1.961	5.89E-02	1.04E-01	1.57E-03	2.48E-02	4.34E-03	1.03E-02	7.64E-02	1.58E-02	3.03E-02	99.90%
M3-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.29E-02	9.49E-03	5.08E-03	2.20E-03	2.51E-02	1.40E-02	5.59E-03	97.50%
	0.14	2	0.1785	1.961	5.89E-02	1.07E-01	1.01E-03	3.08E-02	5.76E-03	1.25E-02	7.41E-02	1.58E-02	2.91E-02	100.00%
M3-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.52E-01	1.02E-01	3.33E-02	1.94E-02	6.98E-03	7.34E-03	3.98E-03	1.68E-03	97.20%
	0.12	2	0.1806	1.939	7.77E-02	1.24E-01	7.04E-04	9.69E-02	2.53E-02	3.58E-02	2.52E-02	5.21E-03	1.00E-02	100.00%
M3-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.53E-01	1.02E-01	3.59E-02	2.09E-02	7.46E-03	7.33E-03	3.98E-03	1.67E-03	97.30%
	0.12	2	0.1806	1.939	7.77E-02	1.27E-01	6.57E-04	1.01E-01	2.74E-02	3.69E-02	2.48E-02	5.21E-03	9.79E-03	100.00%
M3-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.35E-02	1.07E-02	5.84E-03	2.44E-03	2.49E-02	1.40E-02	5.49E-03	97.80%
	0.14	2	0.1785	1.961	5.89E-02	1.09E-01	8.10E-04	3.41E-02	6.62E-03	1.38E-02	7.29E-02	1.58E-02	2.85E-02	100.00%
M3-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.35E-02	1.09E-02	5.96E-03	2.47E-03	2.49E-02	1.40E-02	5.48E-03	97.80%
	0.14	2	0.1785	1.961	5.89E-02	1.09E-01	7.85E-04	3.46E-02	6.75E-03	1.39E-02	7.27E-02	1.58E-02	2.84E-02	100.00%
M3-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.33E-01	9.10E-02	2.39E-02	1.40E-02	4.97E-03	2.45E-02	1.40E-02	5.26E-03	99.10%
	0.14	2	0.1785	1.961	5.89E-02	1.27E-01	2.08E-04	6.07E-02	1.58E-02	2.24E-02	6.55E-02	1.58E-02	2.48E-02	100.00%
M4-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E-01	5.85E-02	2.44E-02	6.07E-03	9.18E-03	3.89E-03	8.89E-04	1.50E-03	92.70%
	0.1	1.965	0.065	2	1.13E+01	8.83E-02	1.90E-03	7.22E-02	6.07E-03	3.30E-02	1.21E-02	8.89E-04	5.59E-03	99.80%
M4-M1-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.45E-01	1.07E-01	1.31E-02	6.47E-03	3.31E-03	5.03E-03	2.38E-03	1.32E-03	94.50%
	0.12	2	0.1806	1.939	7.77E-02	8.33E-02	3.90E-03	5.38E-02	8.46E-03	2.27E-02	2.15E-02	3.11E-03	9.17E-03	99.70%
M4-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.46E-01	1.04E-01	2.27E-02	1.24E-02	5.14E-03	4.71E-03	2.38E-03	1.16E-03	95.90%
	0.12	2	0.1806	1.939	7.77E-02	1.02E-01	2.05E-03	7.93E-02	1.62E-02	3.16E-02	1.82E-02	3.11E-03	7.55E-03	99.90%
M4-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.74E-02	7.84E-03	3.82E-03	2.01E-03	9.18E-03	4.55E-03	2.32E-03	95.30%
	0.14	2	0.1785	1.961	5.89E-02	7.61E-02	4.13E-03	3.07E-02	4.34E-03	1.32E-02	3.69E-02	5.15E-03	1.59E-02	99.70%
M4-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.73E-02	9.91E-03	5.08E-03	2.42E-03	8.92E-03	4.55E-03	2.19E-03	95.70%
	0.14	2	0.1785	1.961	5.89E-02	7.95E-02	3.13E-03	3.78E-02	5.76E-03	1.60E-02	3.54E-02	5.15E-03	1.51E-02	99.90%
M4-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.45E-02	4.98E-03	2.44E-03	1.27E-03	2.61E-02	1.40E-02	6.07E-03	96.80%
	0.14	2	0.1785	1.961	5.89E-02	1.01E-01	2.32E-03	1.72E-02	2.77E-03	7.20E-03	7.92E-02	1.58E-02	3.17E-02	99.80%
M4-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.45E-02	5.76E-03	2.90E-03	1.43E-03	2.58E-02	1.40E-02	5.91E-03	96.90%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	1.95E-03	1.98E-02	3.28E-03	8.28E-03	7.82E-02	1.58E-02	3.12E-02	99.90%
M4-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.51E-01	1.02E-01	3.42E-02	1.94E-02	7.43E-03	4.65E-03	2.38E-03	1.13E-03	96.80%
	0.12	2	0.1806	1.939	7.77E-02	1.20E-01	1.38E-03	1.01E-01	2.53E-02	3.79E-02	1.63E-02	3.11E-03	6.60E-03	99.90%
M4-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.52E-01	1.02E-01	3.68E-02	2.09E-02	7.91E-03	4.63E-03	2.38E-03	1.12E-03	96.90%
	0.12	2	0.1806	1.939	7.77E-02	1.24E-01	1.31E-03	1.05E-01	2.74E-02	3.90E-02	1.60E-02	3.11E-03	6.45E-03	99.90%
M4-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.71E-02	1.11E-02	5.84E-03	2.65E-03	8.80E-03	4.55E-03	2.13E-03	96.00%
	0.14	2	0.1785	1.961	5.89E-02	8.18E-02	2.73E-03	4.16E-02	6.62E-03	1.75E-02	3.46E-02	5.15E-03	1.47E-02	99.90%
M4-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.63E-02	1.13E-02	5.96E-03	2.67E-03	8.78E-03	4.55E-03	2.12E-03	96.00%
	0.14	2	0.1785	1.961	5.89E-02	8.21E-02	2.67E-03	4.22E-02	6.75E-03	1.77E-02	3.45E-02	5.15E-03	1.47E-02	99.90%

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Structure	(as drawn)		(after process bias)											Csum/ Ctotal
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cat (fF/um)	Cft (fF/um)	
M4-M3-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.40E-02	6.19E-03	3.13E-03	1.53E-03	2.57E-02	1.40E-02	5.88E-03	97.00%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	1.79E-03	2.11E-02	3.55E-03	8.80E-03	7.77E-02	1.58E-02	3.09E-02	99.90%
M4-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.40E-02	6.25E-03	3.16E-03	1.54E-03	2.57E-02	1.40E-02	5.87E-03	97.00%
	0.14	2	0.1785	1.961	5.89E-02	1.03E-01	1.77E-03	2.13E-02	3.59E-03	8.87E-03	7.76E-02	1.58E-02	3.09E-02	99.90%
M4-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.49E-02	2.44E-02	1.40E-02	5.23E-03	8.48E-03	4.55E-03	1.97E-03	97.50%
	0.14	2	0.1785	1.961	5.89E-02	1.03E-01	1.20E-03	7.07E-02	1.58E-02	2.74E-02	2.97E-02	5.15E-03	1.23E-02	100.00%
M4-M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.39E-02	8.54E-03	4.55E-03	2.00E-03	2.52E-02	1.40E-02	5.61E-03	97.40%
	0.14	2	0.1785	1.961	5.89E-02	1.06E-01	1.12E-03	2.83E-02	5.15E-03	1.16E-02	7.49E-02	1.58E-02	2.95E-02	100.00%
M4-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.33E-01	9.10E-02	2.39E-02	1.40E-02	4.96E-03	2.45E-02	1.40E-02	5.28E-03	99.10%
	0.14	2	0.1785	1.961	5.89E-02	1.27E-01	2.02E-04	6.07E-02	1.58E-02	2.24E-02	6.55E-02	1.58E-02	2.48E-02	100.00%
M5-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E-01	5.85E-02	2.49E-02	6.07E-03	9.42E-03	3.03E-03	6.74E-04	1.18E-03	92.50%
	0.1	1.965	0.065	2	1.13E+01	8.78E-02	2.23E-03	7.36E-02	6.07E-03	3.37E-02	9.39E-03	6.74E-04	4.36E-03	99.60%
M5-M1-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.42E-01	1.05E-01	1.34E-02	6.47E-03	3.49E-03	3.74E-03	1.70E-03	1.02E-03	94.20%
	0.12	2	0.1806	1.939	7.77E-02	8.15E-02	4.78E-03	5.54E-02	8.46E-03	2.35E-02	1.60E-02	2.22E-03	6.89E-03	99.40%
M5-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.48E-01	1.05E-01	2.31E-02	1.24E-02	5.38E-03	3.48E-03	1.70E-03	8.93E-04	95.70%
	0.12	2	0.1806	1.939	7.77E-02	1.00E-01	2.65E-03	8.12E-02	1.62E-02	3.25E-02	1.35E-02	2.22E-03	5.65E-03	99.70%
M5-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.75E-02	8.35E-03	3.82E-03	2.26E-03	6.02E-03	2.72E-03	1.65E-03	94.70%
	0.14	2	0.1785	1.961	5.89E-02	7.01E-02	5.98E-03	3.29E-02	4.34E-03	1.43E-02	2.47E-02	3.08E-03	1.08E-02	99.40%
M5-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.78E-02	1.05E-02	5.08E-03	2.69E-03	5.79E-03	2.72E-03	1.54E-03	95.10%
	0.14	2	0.1785	1.961	5.89E-02	7.40E-02	4.83E-03	4.04E-02	5.76E-03	1.73E-02	2.36E-02	3.08E-03	1.03E-02	99.60%
M5-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.82E-02	5.35E-03	2.44E-03	1.45E-03	9.56E-03	4.55E-03	2.51E-03	94.90%
	0.14	2	0.1785	1.961	5.89E-02	7.16E-02	5.43E-03	2.15E-02	2.77E-03	9.37E-03	3.88E-02	5.15E-03	1.68E-02	99.40%
M5-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.75E-02	6.19E-03	2.90E-03	1.65E-03	9.42E-03	4.55E-03	2.44E-03	95.00%
	0.14	2	0.1785	1.961	5.89E-02	7.29E-02	4.86E-03	2.48E-02	3.28E-03	1.07E-02	3.81E-02	5.15E-03	1.65E-02	99.60%
M5-M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.46E-02	3.78E-03	1.79E-03	9.95E-04	2.66E-02	1.40E-02	6.28E-03	96.60%
	0.14	2	0.1785	1.961	5.89E-02	1.00E-01	2.86E-03	1.32E-02	2.03E-03	5.56E-03	8.08E-02	1.58E-02	3.25E-02	99.60%
M5-M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.42E-02	4.23E-03	2.03E-03	1.10E-03	2.64E-02	1.40E-02	6.21E-03	96.70%
	0.14	2	0.1785	1.961	5.89E-02	1.00E-01	2.65E-03	1.46E-02	2.30E-03	6.17E-03	8.02E-02	1.58E-02	3.22E-02	99.70%
M5-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.51E-01	1.02E-01	3.48E-02	1.94E-02	7.71E-03	3.43E-03	1.70E-03	8.65E-04	96.70%
	0.12	2	0.1806	1.939	7.77E-02	1.19E-01	1.87E-03	1.03E-01	2.53E-02	3.89E-02	1.21E-02	2.22E-03	4.92E-03	99.80%
M5-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.52E-01	1.02E-01	3.74E-02	2.09E-02	8.21E-03	3.42E-03	1.70E-03	8.60E-04	96.80%
	0.12	2	0.1806	1.939	7.77E-02	1.23E-01	1.77E-03	1.08E-01	2.74E-02	4.01E-02	1.18E-02	2.22E-03	4.81E-03	99.80%
M5-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.76E-02	1.17E-02	5.84E-03	2.91E-03	5.67E-03	2.72E-03	1.48E-03	95.30%
	0.14	2	0.1785	1.961	5.89E-02	7.64E-02	4.31E-03	4.44E-02	6.62E-03	1.89E-02	2.31E-02	3.08E-03	1.00E-02	99.70%
M5-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.75E-02	1.19E-02	5.96E-03	2.95E-03	5.65E-03	2.72E-03	1.47E-03	95.40%
	0.14	2	0.1785	1.961	5.89E-02	7.67E-02	4.24E-03	4.50E-02	6.75E-03	1.91E-02	2.30E-02	3.08E-03	9.96E-03	99.70%
M5-M3-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.72E-02	6.60E-03	3.13E-03	1.73E-03	9.33E-03	4.55E-03	2.39E-03	95.10%
	0.14	2	0.1785	1.961	5.89E-02	7.34E-02	4.59E-03	2.63E-02	3.55E-03	1.14E-02	3.77E-02	5.15E-03	1.63E-02	99.70%
M5-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.72E-02	6.65E-03	3.16E-03	1.75E-03	9.31E-03	4.55E-03	2.38E-03	95.10%
	0.14	2	0.1785	1.961	5.89E-02	7.35E-02	4.55E-03	2.65E-02	3.59E-03	1.15E-02	3.77E-02	5.15E-03	1.63E-02	99.70%
M5-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.35E-02	4.44E-03	2.14E-03	1.15E-03	2.63E-02	1.40E-02	6.17E-03	96.70%
	0.14	2	0.1785	1.961	5.89E-02	1.01E-01	2.55E-03	1.53E-02	2.42E-03	6.46E-03	7.99E-02	1.58E-02	3.20E-02	99.70%
M5-M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.35E-02	4.47E-03	2.15E-03	1.16E-03	2.63E-02	1.40E-02	6.16E-03	96.70%
	0.14	2	0.1785	1.961	5.89E-02	1.01E-01	2.54E-03	1.54E-02	2.44E-03	6.50E-03	7.99E-02	1.58E-02	3.20E-02	99.70%
M5-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.43E-02	2.51E-02	1.40E-02	5.57E-03	5.37E-03	2.72E-03	1.33E-03	96.80%
	0.14	2	0.1785	1.961	5.89E-02	9.85E-02	2.22E-03	7.44E-02	1.58E-02	2.93E-02	1.95E-02	3.08E-03	8.23E-03	99.90%
M5-M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.77E-02	8.94E-03	4.55E-03	2.20E-03	8.95E-03	4.55E-03	2.20E-03	95.60%
	0.14	2	0.1785	1.961	5.89E-02	7.77E-02	3.38E-03	3.49E-02	5.15E-03	1.49E-02	3.60E-02	5.15E-03	1.54E-02	99.90%
M5-M4-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.45E-02	5.45E-03	2.72E-03	1.37E-03	2.59E-02	1.40E-02	5.97E-03	96.90%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	2.07E-03	1.88E-02	3.08E-03	7.86E-03	7.86E-02	1.58E-02	3.14E-02	99.90%
M5-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.49E-02	2.44E-02	1.40E-02	5.23E-03	8.48E-03	4.55E-03	1.97E-03	97.50%
	0.14	2	0.1785	1.961	5.89E-02	1.03E-01	1.19E-03	7.06E-02	1.58E-02	2.74E-02	2.97E-02	5.15E-03	1.23E-02	100.00%
M5-M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.30E-02	8.55E-03	4.55E-03	2.00E-03	2.52E-02	1.40E-02	5.61E-03	97.40%
	0.14	2	0.1785	1.961	5.89E-02	1.06E-01	1.12E-03	2.83E-02	5.15E-03	1.16E-02	7.49E-02	1.58E-02	2.96E-02	100.00%
M5-M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.33E-01	9.10E-02	2.39E-02	1.40E-02	4.96E-03	2.45E-02	1.40E-02	5.28E-03	99.10%
	0.14	2	0.1785	1.961	5.89E-02	1.27E-01	2.02E-04	6.07E-02	1.58E-02	2.24E-02	6.55E-02	1.58E-02	2.48E-02	100.00%
M6-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E-01	5.86E-02	2.53E-02	6.07E-03	9.59E-03	2.48E-03	5.42E-04	9.71E-04	92.40%
	0.1	1.965	0.065	2	1.13E+01	8.75E-02	2.44E-03	7.44E-02	6.07E-03	3.42E-02	7.68E-03	5.42E-04	3.57E-03	99.40%
M6-M1-FOX	0.12	0.12	0.138	0.102										

Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cat (fF/um)	Cft (fF/um)	
	0.12	2	0.1806	1.939	7.77E-02	8.07E-02	5.30E-03	5.65E-02	8.46E-03	2.40E-02	1.28E-02	1.72E-03	5.53E-03	99.00%
M6-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.44E-01	1.03E-01	2.35E-02	1.24E-02	5.54E-03	2.77E-03	1.32E-03	7.27E-04	95.60%
	0.12	2	0.1806	1.939	7.77E-02	9.98E-02	3.06E-03	8.24E-02	1.62E-02	3.31E-02	1.07E-02	1.72E-03	4.51E-03	99.40%
M6-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.78E-02	8.78E-03	3.82E-03	2.48E-03	4.60E-03	1.94E-03	1.33E-03	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.78E-02	7.16E-03	3.41E-02	4.34E-03	1.49E-02	1.86E-02	2.19E-03	8.19E-03	98.70%
M6-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.81E-02	1.09E-02	5.08E-03	2.89E-03	4.37E-03	1.94E-03	1.22E-03	94.90%
	0.14	2	0.1785	1.961	5.89E-02	7.18E-02	5.87E-03	4.17E-02	5.76E-03	1.80E-02	1.77E-02	2.19E-03	7.77E-03	99.10%
M6-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.77E-02	5.83E-03	2.44E-03	1.69E-03	6.41E-03	2.72E-03	1.85E-03	94.20%
	0.14	2	0.1785	1.961	5.89E-02	6.53E-02	7.58E-03	2.32E-02	2.77E-03	1.02E-02	2.61E-02	3.08E-03	1.15E-02	98.80%
M6-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.79E-02	6.64E-03	2.90E-03	1.87E-03	6.21E-03	2.72E-03	1.75E-03	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.67E-02	6.90E-03	2.67E-02	3.28E-03	1.17E-02	2.56E-02	3.08E-03	1.13E-02	99.10%
M6-M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	4.18E-03	1.79E-03	1.20E-03	1.00E-02	4.55E-03	2.73E-03	94.60%
	0.14	2	0.1785	1.961	5.89E-02	7.01E-02	6.34E-03	1.66E-02	2.03E-03	7.30E-03	4.00E-02	5.15E-03	1.74E-02	98.80%
M6-M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.79E-02	4.62E-03	2.03E-03	1.30E-03	9.83E-03	4.55E-03	2.64E-03	94.70%
	0.14	2	0.1785	1.961	5.89E-02	7.05E-02	5.97E-03	1.84E-02	2.30E-03	8.08E-03	3.95E-02	5.15E-03	1.72E-02	99.10%
M6-M5-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.34E-02	3.10E-03	1.42E-03	8.40E-04	2.70E-02	1.40E-02	6.52E-03	96.50%
	0.14	2	0.1785	1.961	5.89E-02	9.96E-02	3.23E-03	1.07E-02	1.60E-03	4.52E-03	8.19E-02	1.58E-02	3.30E-02	99.40%
M6-M5-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.47E-02	3.35E-03	1.56E-03	8.95E-04	2.67E-02	1.40E-02	6.39E-03	96.50%
	0.14	2	0.1785	1.961	5.89E-02	9.98E-02	3.09E-03	1.16E-02	1.77E-03	4.93E-03	8.14E-02	1.58E-02	3.28E-02	99.50%
M6-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.48E-01	1.01E-01	3.50E-02	1.94E-02	7.80E-03	2.70E-03	1.32E-03	6.91E-04	96.50%
	0.12	2	0.1806	1.939	7.77E-02	1.19E-01	2.20E-03	1.04E-01	2.53E-02	3.95E-02	9.56E-03	1.72E-03	3.92E-03	99.60%
M6-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.49E-01	1.00E-01	3.75E-02	2.09E-02	8.29E-03	2.69E-03	1.32E-03	6.86E-04	96.60%
	0.12	2	0.1806	1.939	7.77E-02	1.23E-01	2.09E-03	1.09E-01	2.74E-02	4.07E-02	9.38E-03	1.72E-03	3.83E-03	99.70%
M6-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.70E-02	1.20E-02	5.84E-03	3.10E-03	4.24E-03	1.94E-03	1.15E-03	95.00%
	0.14	2	0.1785	1.961	5.89E-02	7.43E-02	5.30E-03	4.58E-02	6.62E-03	1.96E-02	1.73E-02	2.19E-03	7.55E-03	99.20%
M6-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.77E-02	1.23E-02	5.96E-03	3.15E-03	4.24E-03	1.94E-03	1.15E-03	95.10%
	0.14	2	0.1785	1.961	5.89E-02	7.47E-02	5.22E-03	4.64E-02	6.75E-03	1.98E-02	1.72E-02	2.19E-03	7.52E-03	99.30%
M6-M3-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	7.04E-03	3.13E-03	1.95E-03	6.13E-03	2.72E-03	1.71E-03	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.74E-02	6.59E-03	2.84E-02	3.55E-03	1.24E-02	2.54E-02	3.08E-03	1.12E-02	99.20%
M6-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.76E-02	7.04E-03	3.16E-03	1.94E-03	6.06E-03	2.72E-03	1.67E-03	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.74E-02	6.53E-03	2.85E-02	3.59E-03	1.25E-02	2.53E-02	3.08E-03	1.11E-02	99.20%
M6-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.75E-02	4.84E-03	2.14E-03	1.35E-03	9.77E-03	4.55E-03	2.61E-03	94.70%
	0.14	2	0.1785	1.961	5.89E-02	7.08E-02	5.81E-03	1.93E-02	2.42E-03	8.44E-03	3.93E-02	5.15E-03	1.71E-02	99.20%
M6-M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.79E-02	4.87E-03	2.15E-03	1.36E-03	9.78E-03	4.55E-03	2.61E-03	94.80%
	0.14	2	0.1785	1.961	5.89E-02	7.08E-02	5.79E-03	1.94E-02	2.44E-03	8.49E-03	3.93E-02	5.15E-03	1.71E-02	99.20%
M6-M5-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.47E-02	3.47E-03	1.62E-03	9.24E-04	2.67E-02	1.40E-02	6.36E-03	96.60%
	0.14	2	0.1785	1.961	5.89E-02	9.98E-02	3.02E-03	1.21E-02	1.84E-03	5.11E-03	8.13E-02	1.58E-02	3.27E-02	99.50%
M6-M5-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.47E-02	3.49E-03	1.63E-03	9.28E-04	2.67E-02	1.40E-02	6.35E-03	96.60%
	0.14	2	0.1785	1.961	5.89E-02	9.99E-02	3.01E-03	1.21E-02	1.85E-03	5.13E-03	8.12E-02	1.58E-02	3.27E-02	99.50%
M6-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.46E-02	2.56E-02	1.40E-02	5.84E-03	3.99E-03	1.94E-03	1.03E-03	96.70%
	0.14	2	0.1785	1.961	5.89E-02	9.70E-02	2.94E-03	7.62E-02	1.58E-02	3.02E-02	1.46E-02	2.19E-03	6.18E-03	99.60%
M6-M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.82E-02	9.46E-03	4.55E-03	2.46E-03	5.82E-03	2.72E-03	1.55E-03	95.00%
	0.14	2	0.1785	1.961	5.89E-02	7.19E-02	5.15E-03	3.73E-02	5.15E-03	1.61E-02	2.40E-02	3.08E-03	1.05E-02	99.60%
M6-M4-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.79E-02	5.85E-03	2.72E-03	1.57E-03	9.48E-03	4.55E-03	2.47E-03	95.00%
	0.14	2	0.1785	1.961	5.89E-02	7.23E-02	5.06E-03	2.35E-02	3.08E-03	1.02E-02	3.84E-02	5.15E-03	1.66E-02	99.50%
M6-M5-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.44E-02	4.05E-03	1.94E-03	1.06E-03	2.64E-02	1.40E-02	6.21E-03	96.60%
	0.14	2	0.1785	1.961	5.89E-02	1.00E-01	2.74E-03	1.41E-02	2.19E-03	5.94E-03	8.04E-02	1.58E-02	3.23E-02	99.60%
M6-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.43E-02	2.51E-02	1.40E-02	5.57E-03	5.38E-03	2.72E-03	1.33E-03	96.90%
	0.14	2	0.1785	1.961	5.89E-02	9.85E-02	2.22E-03	7.44E-02	1.58E-02	2.93E-02	1.95E-02	3.08E-03	8.23E-03	99.90%
M6-M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.82E-02	8.93E-03	4.55E-03	2.19E-03	8.93E-03	4.55E-03	2.19E-03	95.60%
	0.14	2	0.1785	1.961	5.89E-02	7.77E-02	3.38E-03	3.49E-02	5.15E-03	1.49E-02	3.60E-02	5.15E-03	1.54E-02	99.90%
M6-M5-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.45E-02	5.44E-03	2.72E-03	1.36E-03	2.59E-02	1.40E-02	5.95E-03	96.90%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	2.07E-03	1.88E-02	3.08E-03	7.86E-03	7.86E-02	1.58E-02	3.14E-02	99.90%
M6-M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.49E-02	2.44E-02	1.40E-02	5.23E-03	8.48E-03	4.55E-03	1.97E-03	97.50%
	0.14	2	0.1785	1.961	5.89E-02	1.03E-01	1.19E-03	7.06E-02	1.58E-02	2.74E-02	2.97E-02	5.15E-03	1.23E-02	100.00%
M6-M5-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.30E-02	8.55E-03	4.55E-03	2.00E-03	2.52E-02	1.40E-02	5.61E-03	97.40%
	0.14	2	0.1785	1.961	5.89E-02	1.06E-01	1.12E-03	2.83E-02	5.15E-03	1.16E-02	7.49E-02	1.58E-02	2.96E-02	100.00%
M6-M4-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.33E-01	9.10E-02	2.39E-02	1.40E-02	4.96E-03	2.45E-02	1.40E-02	5.28E-03	99.10%
	0.14	2	0.1785	1.961	5.89E-02</td									

Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cap (fF/um)	Cft (fF/um)	
FOX														
M7-M1-FOX	0.1	1.965	0.065	2	1.13E+01	8.74E-02	2.59E-03	7.51E-02	6.07E-03	3.45E-02	6.50E-03	4.54E-04	3.02E-03	99.20%
M7-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.44E-01	1.07E-01	1.43E-02	6.47E-03	3.90E-03	2.57E-03	1.08E-03	7.47E-04	94.20%
M7-M1-OD	0.12	2	0.1806	1.939	7.77E-02	8.03E-02	5.66E-03	5.72E-02	8.46E-03	2.44E-02	1.06E-02	1.41E-03	4.61E-04	98.60%
M7-M2-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.45E-01	1.04E-01	2.39E-02	1.24E-02	5.79E-03	2.34E-03	1.08E-03	6.33E-04	95.60%
M7-M2-FOX	0.12	2	0.1806	1.939	7.77E-02	9.95E-02	3.28E-03	8.32E-02	1.62E-02	3.35E-02	8.93E-03	1.41E-03	3.76E-03	99.30%
M7-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.81E-02	9.12E-03	3.82E-03	2.65E-03	3.76E-03	1.50E-03	1.13E-03	94.30%
M7-M2-OD	0.14	2	0.1785	1.961	5.89E-02	6.67E-02	7.85E-03	3.48E-02	4.34E-03	1.53E-02	1.49E-02	1.71E-03	6.60E-03	98.10%
M7-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.83E-02	1.12E-02	5.08E-03	3.07E-03	3.55E-03	1.50E-03	1.02E-03	94.70%
M7-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.84E-02	6.20E-03	2.44E-03	1.88E-03	4.96E-03	1.94E-03	1.51E-03	93.90%
M7-M3-FOX	0.14	2	0.1785	1.961	5.89E-02	6.28E-02	8.86E-03	2.41E-02	2.77E-03	1.07E-02	1.97E-02	2.19E-03	8.76E-03	98.00%
M7-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.83E-02	7.03E-03	2.90E-03	2.06E-03	4.78E-03	1.94E-03	1.42E-03	94.10%
M7-M3-OD	0.14	2	0.1785	1.961	5.89E-02	6.42E-02	8.13E-03	2.76E-02	3.28E-03	1.22E-02	1.93E-02	2.19E-03	8.56E-03	98.40%
M7-M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.80E-02	4.53E-03	1.79E-03	1.37E-03	6.68E-03	2.72E-03	1.98E-03	93.90%
M7-M4-FOX	0.14	2	0.1785	1.961	5.89E-02	6.33E-02	8.59E-03	1.79E-02	2.03E-03	7.96E-03	2.69E-02	3.08E-03	1.19E-02	98.00%
M7-M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.81E-02	5.04E-03	2.03E-03	1.51E-03	6.61E-03	2.72E-03	1.94E-03	94.00%
M7-M4-OD	0.14	2	0.1785	1.961	5.89E-02	6.40E-02	8.19E-03	1.99E-02	2.30E-03	8.82E-03	2.66E-02	3.08E-03	1.18E-02	98.40%
M7-M5-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.78E-02	3.41E-03	1.42E-03	9.99E-04	1.02E-02	4.55E-03	2.84E-03	94.50%
M7-M5-FOX	0.14	2	0.1785	1.961	5.89E-02	6.91E-02	6.88E-03	1.35E-02	1.60E-03	5.97E-03	4.07E-02	5.15E-03	1.77E-02	98.30%
M7-M5-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	3.70E-03	1.56E-03	1.07E-03	1.01E-02	4.55E-03	2.77E-03	94.50%
M7-M5-OD	0.14	2	0.1785	1.961	5.89E-02	6.94E-02	6.68E-03	1.47E-02	1.77E-03	6.48E-03	4.03E-02	5.15E-03	1.76E-02	98.50%
M7-M6-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.30E-02	2.61E-03	1.17E-03	7.22E-04	2.73E-02	1.40E-02	6.67E-03	96.50%
M7-M6-FOX	0.14	2	0.1785	1.961	5.89E-02	9.94E-02	3.48E-03	8.97E-03	1.33E-03	3.82E-03	8.26E-02	1.58E-02	3.34E-02	99.20%
M7-M6-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.34E-02	2.81E-03	1.27E-03	7.70E-04	2.72E-02	1.40E-02	6.61E-03	96.50%
M7-M6-OD	0.14	2	0.1785	1.961	5.89E-02	9.95E-02	3.38E-03	9.64E-03	1.43E-03	4.10E-03	8.23E-02	1.58E-02	3.33E-02	99.30%
M7-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.50E-01	1.02E-01	3.54E-02	1.94E-02	8.01E-03	2.26E-03	1.08E-03	5.90E-04	96.50%
M7-M1-PO1(OD)	0.12	2	0.1806	1.939	7.77E-02	1.19E-01	2.41E-03	1.05E-01	2.53E-02	3.99E-02	7.92E-03	1.41E-03	3.25E-03	99.50%
M7-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.51E-01	1.01E-01	3.80E-02	2.09E-02	8.51E-03	2.25E-03	1.08E-03	5.85E-04	96.60%
M7-M2-PO1(OD)	0.12	2	0.1806	1.939	7.77E-02	1.22E-01	2.30E-03	1.10E-01	2.74E-02	4.10E-02	7.77E-03	1.41E-03	3.18E-03	99.50%
M7-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.83E-02	1.25E-02	5.84E-03	3.32E-03	3.47E-03	1.50E-03	9.82E-04	95.00%
M7-M2-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	7.33E-02	5.92E-03	4.67E-02	6.62E-03	2.00E-02	1.38E-02	1.71E-03	6.07E-03	98.70%
M7-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.67E-02	1.27E-02	5.96E-03	3.37E-03	3.47E-03	1.50E-03	9.83E-04	94.90%
M7-M3-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	7.37E-02	5.84E-03	4.73E-02	6.75E-03	2.03E-02	1.38E-02	1.71E-03	6.05E-03	98.80%
M7-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.82E-02	7.44E-03	3.13E-03	2.15E-03	4.70E-03	1.94E-03	1.38E-03	94.20%
M7-M4-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	6.50E-02	7.82E-03	2.93E-02	3.55E-03	1.29E-02	1.91E-02	2.19E-03	8.45E-03	98.50%
M7-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.82E-02	7.49E-03	3.16E-03	2.16E-03	4.69E-03	1.94E-03	1.38E-03	94.20%
M7-M4-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	6.51E-02	7.78E-03	2.96E-02	3.59E-03	1.30E-02	1.91E-02	2.19E-03	8.44E-03	98.60%
M7-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.81E-02	5.25E-03	2.14E-03	1.56E-03	6.54E-03	2.72E-03	1.91E-03	94.10%
M7-M4-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	6.43E-02	8.03E-03	2.08E-02	2.42E-03	9.21E-03	2.65E-02	3.08E-03	1.17E-02	98.50%
M7-M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.81E-02	5.28E-03	2.15E-03	1.56E-03	6.53E-03	2.72E-03	1.91E-03	94.10%
M7-M5-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	6.43E-02	8.00E-03	2.10E-02	2.44E-03	9.26E-03	2.65E-02	3.08E-03	1.17E-02	98.60%
M7-M5-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	3.84E-03	1.62E-03	1.10E-03	1.00E-02	4.55E-03	2.75E-03	94.50%
M7-M5-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	6.96E-02	6.58E-03	1.53E-02	1.84E-03	6.71E-03	4.02E-02	5.15E-03	1.75E-02	98.60%
M7-M5-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	3.84E-03	1.63E-03	1.11E-03	1.00E-02	4.55E-03	2.74E-03	94.50%
M7-M6-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	6.96E-02	6.57E-03	1.53E-02	1.85E-03	6.74E-03	4.02E-02	5.15E-03	1.75E-02	98.70%
M7-M6-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.34E-02	2.89E-03	1.31E-03	7.90E-04	2.71E-02	1.40E-02	6.58E-03	96.50%
M7-M6-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	9.95E-02	3.34E-03	9.94E-03	1.48E-03	4.23E-03	8.22E-02	1.58E-02	3.32E-02	99.30%
M7-M6-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.34E-02	2.90E-03	1.31E-03	7.93E-04	2.71E-02	1.40E-02	6.57E-03	96.50%
M7-M7-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	6.96E-02	6.57E-03	1.53E-02	1.84E-03	6.71E-03	4.02E-02	5.15E-03	1.75E-02	98.60%
M7-M7-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	6.98E-02	6.23E-03	3.86E-02	5.15E-03	1.67E-02	1.81E-02	2.19E-03	7.93E-03	99.00%
M7-M8-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.76E-02	6.25E-03	2.72E-03	1.77E-03	6.22E-03	2.72E-03	1.75E-03	94.20%
M7-M8-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	6.61E-02	7.14E-03	2.53E-02	3.08E-03	1.11E-02	2.58E-02	3.08E-03	1.14E-02	99.00%
M7-M9-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.77E-02	4.47E-03	1.94E-03	1.27E-03	9.91E-03	4.55E-03	2.68E-03	94.70%
M7-M9-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	7.02E-02	6.10E-03	1.77E-02	2.19E-03	7.76E-03	3.96E-02	5.15E-03	1.72E-02	99.00%
M7-M10-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.45E-02	3.25E-03	1.50E-03	8.71E-04	2.68E-02	1.40E-02	6.42E-03	96.50%

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Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cat (fF/um)	Cft (fF/um)	
	0.14	2	0.1785	1.961	5.89E-02	9.98E-02	3.15E-03	1.13E-02	1.71E-03	4.79E-03	8.17E-02	1.58E-02	3.29E-02	99.40%
M7-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.32E-02	2.57E-02	1.40E-02	5.85E-03	4.00E-03	1.94E-03	1.03E-03	96.60%
	0.14	2	0.1785	1.961	5.89E-02	9.70E-02	2.94E-03	7.62E-02	1.58E-02	3.02E-02	1.45E-02	2.19E-03	6.18E-03	99.60%
M7-M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.78E-02	9.43E-03	4.55E-03	2.44E-03	5.80E-03	2.72E-03	1.54E-03	94.90%
	0.14	2	0.1785	1.961	5.89E-02	7.19E-02	5.15E-03	3.73E-02	5.15E-03	1.61E-02	2.40E-02	3.08E-03	1.05E-02	99.60%
M7-M5-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.76E-02	5.87E-03	2.72E-03	1.57E-03	9.48E-03	4.55E-03	2.47E-03	95.00%
	0.14	2	0.1785	1.961	5.89E-02	7.23E-02	5.06E-03	2.35E-02	3.08E-03	1.02E-02	3.84E-02	5.15E-03	1.66E-02	99.50%
M7-M6-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.38E-02	4.07E-03	1.94E-03	1.07E-03	2.65E-02	1.40E-02	6.25E-03	96.70%
	0.14	2	0.1785	1.961	5.89E-02	1.00E-01	2.74E-03	1.41E-02	2.19E-03	5.94E-03	8.04E-02	1.58E-02	3.23E-02	99.60%
M7-M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.43E-02	2.51E-02	1.40E-02	5.57E-03	5.38E-03	2.72E-03	1.33E-03	96.90%
	0.14	2	0.1785	1.961	5.89E-02	9.85E-02	2.22E-03	7.44E-02	1.58E-02	2.93E-02	1.95E-02	3.08E-03	8.23E-03	99.90%
M7-M5-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.82E-02	8.93E-03	4.55E-03	2.19E-03	8.93E-03	4.55E-03	2.19E-03	95.60%
	0.14	2	0.1785	1.961	5.89E-02	7.77E-02	3.38E-03	3.49E-02	5.15E-03	1.49E-02	3.60E-02	5.15E-03	1.54E-02	99.90%
M7-M6-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.45E-02	4.44E-03	2.72E-03	1.36E-03	2.59E-02	1.40E-02	5.95E-03	96.90%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	2.07E-03	1.88E-02	3.08E-03	7.86E-03	7.86E-02	1.58E-02	3.14E-02	99.90%
M7-M5-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.49E-02	2.44E-02	1.40E-02	5.23E-03	8.48E-03	4.55E-03	1.97E-03	97.50%
	0.14	2	0.1785	1.961	5.89E-02	1.03E-01	1.19E-03	7.06E-02	1.58E-02	2.74E-02	2.97E-02	5.15E-03	1.23E-02	100.00%
M7-M6-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.30E-02	8.55E-03	4.55E-03	2.00E-03	2.52E-02	1.40E-02	5.61E-03	97.40%
	0.14	2	0.1785	1.961	5.89E-02	1.06E-01	1.12E-03	2.83E-02	5.15E-03	1.16E-02	7.49E-02	1.58E-02	2.96E-02	100.00%
M7-M6-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.33E-01	9.10E-02	2.39E-02	1.40E-02	4.96E-03	2.45E-02	1.40E-02	5.28E-03	99.10%
	0.14	2	0.1785	1.961	5.89E-02	1.27E-01	2.02E-04	6.07E-02	1.58E-02	2.24E-02	6.55E-02	1.58E-02	2.48E-02	100.00%
M8-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E-01	5.87E-02	2.58E-02	6.07E-03	9.86E-03	1.76E-03	3.73E-04	6.91E-04	92.20%
	0.1	1.965	0.065	2	1.13E+01	8.74E-02	2.73E-03	7.58E-02	6.07E-03	3.48E-02	5.40E-03	3.73E-04	2.51E-03	99.10%
M8-M1-FOX	0.12	0.12	0.138	0.102	1.00E-01	2.44E-01	1.06E-01	1.45E-02	6.47E-03	4.01E-03	2.11E-03	8.67E-04	6.23E-04	94.10%
	0.12	2	0.1806	1.939	7.77E-02	8.00E-02	5.97E-03	5.79E-02	8.46E-03	2.47E-02	8.70E-03	1.13E-03	3.78E-03	98.20%
M8-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.47E-01	1.05E-01	2.42E-02	1.24E-02	5.93E-03	1.92E-03	8.67E-04	5.28E-04	95.60%
	0.12	2	0.1806	1.939	7.77E-02	9.92E-02	3.50E-03	8.40E-02	1.62E-02	3.39E-02	7.29E-03	1.13E-03	3.08E-03	99.10%
M8-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.88E-02	9.49E-03	3.82E-03	2.83E-03	3.05E-03	1.16E-03	9.43E-04	94.20%
	0.14	2	0.1785	1.961	5.89E-02	6.62E-02	8.45E-03	3.56E-02	4.34E-03	1.56E-02	1.19E-02	1.31E-03	5.27E-03	97.30%
M8-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.75E-02	1.16E-02	5.08E-03	3.25E-03	2.86E-03	1.16E-03	8.50E-04	94.60%
	0.14	2	0.1785	1.961	5.89E-02	7.03E-02	7.05E-03	4.35E-02	5.76E-03	1.88E-02	1.13E-02	1.31E-03	4.98E-03	97.90%
M8-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.92E-02	6.59E-03	2.44E-03	2.08E-03	3.87E-03	1.40E-03	1.23E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.15E-02	9.88E-03	2.49E-02	2.77E-03	1.10E-02	1.49E-02	1.59E-03	6.66E-03	96.80%
M8-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.87E-02	7.34E-03	2.90E-03	2.22E-03	3.66E-03	1.40E-03	1.13E-03	93.90%
	0.14	2	0.1785	1.961	5.89E-02	6.28E-02	9.08E-03	2.85E-02	3.28E-03	1.26E-02	1.46E-02	1.59E-03	6.49E-03	97.40%
M8-M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	4.97E-03	1.79E-03	1.59E-03	4.87E-03	1.77E-03	1.55E-03	93.60%
	0.14	2	0.1785	1.961	5.89E-02	6.03E-02	1.03E-02	1.89E-02	2.03E-03	8.42E-03	1.89E-02	2.00E-03	8.44E-03	96.80%
M8-M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	5.44E-03	2.03E-03	1.71E-03	4.74E-03	1.77E-03	1.49E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.12E-02	9.91E-03	2.10E-02	2.30E-03	9.34E-03	1.87E-02	2.00E-03	8.35E-03	97.20%
M8-M5-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	3.89E-03	1.42E-03	1.24E-03	6.37E-03	2.40E-03	1.99E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.13E-02	9.80E-03	1.49E-02	1.60E-03	6.66E-03	2.48E-02	2.72E-03	1.11E-02	96.90%
M8-M5-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	4.19E-03	1.56E-03	1.32E-03	6.26E-03	2.40E-03	1.93E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.16E-02	9.56E-03	1.62E-02	1.77E-03	7.22E-03	2.46E-02	2.72E-03	1.09E-02	97.30%
M8-M6-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	3.05E-03	1.17E-03	9.39E-04	9.05E-03	3.72E-03	2.67E-03	94.10%
	0.14	2	0.1785	1.961	5.89E-02	6.56E-02	8.29E-03	1.18E-02	1.33E-03	5.25E-03	3.55E-02	4.21E-03	1.56E-02	97.40%
M8-M6-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	3.25E-03	1.27E-03	9.94E-04	8.96E-03	3.72E-03	2.62E-03	94.10%
	0.14	2	0.1785	1.961	5.89E-02	6.60E-02	8.16E-03	1.27E-02	1.43E-03	5.65E-03	3.54E-02	4.21E-03	1.56E-02	97.60%
M8-M7-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.57E-02	2.41E-03	9.97E-04	7.09E-04	1.78E-02	2.82E-03	4.77E-03	94.40%
	0.14	2	0.1785	1.961	5.89E-02	8.51E-02	5.78E-03	8.88E-03	1.13E-03	3.88E-03	6.32E-02	9.39E-03	2.69E-02	98.40%
M8-M7-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.70E-02	2.56E-03	1.07E-03	7.47E-04	1.77E-02	2.82E-03	4.72E-03	94.50%
	0.14	2	0.1785	1.961	5.89E-02	8.51E-02	5.69E-03	9.45E-03	1.21E-03	4.12E-03	6.30E-02	9.39E-03	2.68E-02	98.50%
M8-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.51E-01	1.02E-01	3.58E-02	1.94E-02	8.21E-03	1.85E-03	8.67E-04	4.90E-04	96.40%
	0.12	2	0.1806	1.939	7.77E-02	1.18E-01	2.55E-03	1.06E-01	2.53E-02	4.03E-02	6.45E-03	1.13E-03	2.66E-03	99.40%
M8-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.51E-01	1.01E-01	3.83E-02	2.09E-02	8.69E-03	1.84E-03	8.67E-04	4.86E-04	96.60%
	0.12	2	0.1806	1.939	7.77E-02	1.22E-01	2.48E-03	1.10E-01	2.74E-02	4.14E-02	6.31E-03	1.13E-03	2.59E-03	99.40%
M8-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.78E-02	1.28E-02	5.84E-03	3.50E-03	2.79E-03	1.16E-03	8.13E-04	94.90%
	0.14	2	0.1785	1.961	5.89E-02	7.27E-02	6.40E-03	4.76E-02	6.62E-03	2.05E-02	1.10E-02	1.31E-03	4.83E-03	98.10%
M8-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.77E-02	1.30E-02	5.96E-03	3.54E-03	2.78E-03	1.16E-03	8.08E-04	94.90%
	0.14	2	0.1785	1.961	5.89E-02	7.31E-02	6.31E-0							

Structure	(as drawn)		(after process bias)											
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cat (fF/um)	Cft (fF/um)	Csum/ Ctotal
M8-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	5.65E-03	2.14E-03	1.76E-03	4.68E-03	1.77E-03	1.46E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.15E-02	9.72E-03	2.19E-02	2.42E-03	9.75E-03	1.86E-02	2.00E-03	8.29E-03	97.40%
M8-M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	5.68E-03	2.15E-03	1.77E-03	4.68E-03	1.77E-03	1.45E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.13E-02	9.64E-03	2.20E-02	2.44E-03	9.77E-03	1.85E-02	2.00E-03	8.24E-03	97.40%
M8-M5-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	4.32E-03	1.62E-03	1.35E-03	6.21E-03	2.40E-03	1.90E-03	93.80%
	0.14	2	0.1785	1.961	5.89E-02	6.18E-02	9.45E-03	1.68E-02	1.84E-03	7.47E-03	2.45E-02	2.72E-03	1.09E-02	97.40%
M8-M5-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	4.34E-03	1.63E-03	1.36E-03	6.20E-03	2.40E-03	1.90E-03	93.80%
	0.14	2	0.1785	1.961	5.89E-02	6.18E-02	9.43E-03	1.69E-02	1.85E-03	7.51E-03	2.45E-02	2.72E-03	1.09E-02	97.40%
M8-M6-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	3.34E-03	1.31E-03	1.02E-03	8.91E-03	3.72E-03	2.59E-03	94.20%
	0.14	2	0.1785	1.961	5.89E-02	6.61E-02	8.09E-03	1.31E-02	1.48E-03	5.81E-03	3.53E-02	4.21E-03	1.55E-02	97.70%
M8-M6-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	3.35E-03	1.31E-03	1.02E-03	8.90E-03	3.72E-03	2.59E-03	94.20%
	0.14	2	0.1785	1.961	5.89E-02	6.61E-02	8.08E-03	1.32E-02	1.49E-03	5.83E-03	3.53E-02	4.21E-03	1.55E-02	97.80%
M8-M7-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.70E-02	2.62E-03	1.10E-03	7.64E-04	1.77E-02	8.28E-03	4.70E-03	94.50%
	0.14	2	0.1785	1.961	5.89E-02	8.51E-02	5.64E-03	9.69E-03	1.24E-03	4.22E-03	6.29E-02	9.39E-03	2.67E-02	98.50%
M8-M7-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.70E-02	2.63E-03	1.10E-03	7.66E-04	1.77E-02	8.28E-03	4.70E-03	94.50%
	0.14	2	0.1785	1.961	5.89E-02	8.51E-02	5.64E-03	9.72E-03	1.25E-03	4.24E-03	6.29E-02	9.39E-03	2.67E-02	98.50%
M8-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.50E-02	2.64E-02	1.40E-02	6.24E-03	2.53E-03	1.16E-03	6.87E-04	96.50%
	0.14	2	0.1785	1.961	5.89E-02	9.59E-02	3.74E-03	7.84E-02	1.58E-02	3.13E-02	9.15E-03	1.31E-03	3.92E-03	99.10%
M8-M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.24E-01	9.92E-02	1.03E-02	4.55E-03	2.88E-03	3.39E-03	1.40E-03	9.92E-04	94.60%
	0.14	2	0.1785	1.961	5.89E-02	6.85E-02	7.06E-03	3.96E-02	5.15E-03	1.72E-02	1.36E-02	1.59E-03	6.00E-03	98.20%
M8-M4-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	6.72E-03	2.72E-03	2.00E-03	4.45E-03	1.77E-03	1.34E-03	93.90%
	0.14	2	0.1785	1.961	5.89E-02	6.32E-02	8.69E-03	2.65E-02	3.08E-03	1.17E-02	1.80E-02	2.00E-03	8.00E-03	98.00%
M8-M5-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	4.94E-03	1.94E-03	1.50E-03	6.00E-03	2.40E-03	1.80E-03	93.90%
	0.14	2	0.1785	1.961	5.89E-02	6.27E-02	8.89E-03	1.95E-02	2.19E-03	8.64E-03	2.41E-02	2.72E-03	1.07E-02	98.00%
M8-M6-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	3.74E-03	1.50E-03	1.12E-03	8.73E-03	3.72E-03	2.50E-03	94.20%
	0.14	2	0.1785	1.961	5.89E-02	6.65E-02	7.77E-03	1.48E-02	1.71E-03	6.55E-03	3.49E-02	4.21E-03	1.53E-02	98.10%
M8-M7-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.63E-02	2.90E-03	1.23E-03	8.34E-04	1.75E-02	8.28E-03	4.62E-03	94.50%
	0.14	2	0.1785	1.961	5.89E-02	8.53E-02	5.47E-03	1.08E-02	1.39E-03	4.68E-03	6.25E-02	9.39E-03	2.66E-02	98.70%
M8-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.38E-02	2.62E-02	1.40E-02	6.13E-03	3.01E-03	1.40E-03	8.07E-04	96.50%
	0.14	2	0.1785	1.961	5.89E-02	9.61E-02	3.48E-03	7.76E-02	1.58E-02	3.09E-02	1.09E-02	1.59E-03	4.65E-03	99.30%
M8-M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.80E-02	1.00E-02	4.55E-03	2.73E-03	4.10E-03	1.77E-03	1.17E-03	94.60%
	0.14	2	0.1785	1.961	5.89E-02	6.94E-02	6.49E-03	3.89E-02	5.15E-03	1.69E-02	1.67E-02	2.00E-03	7.33E-03	98.80%
M8-M5-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.77E-02	6.38E-03	2.72E-03	1.83E-03	5.64E-03	2.40E-03	1.62E-03	94.10%
	0.14	2	0.1785	1.961	5.89E-02	6.51E-02	7.65E-03	2.57E-02	3.08E-03	1.13E-02	2.33E-02	2.72E-03	1.03E-02	98.80%
M8-M6-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.78E-02	4.62E-03	1.94E-03	1.34E-03	8.49E-03	3.72E-03	2.38E-03	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.75E-02	7.07E-03	1.84E-02	2.19E-03	8.09E-03	3.42E-02	4.21E-03	1.50E-02	98.80%
M8-M7-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.76E-02	3.45E-03	1.50E-03	9.71E-04	1.72E-02	8.28E-03	4.47E-03	94.60%
	0.14	2	0.1785	1.961	5.89E-02	8.57E-02	5.11E-03	1.29E-02	1.71E-03	5.59E-03	6.18E-02	9.39E-03	2.62E-02	99.10%
M8-M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.48E-02	2.58E-02	1.40E-02	5.92E-03	3.69E-03	1.77E-03	9.60E-04	96.60%
	0.14	2	0.1785	1.961	5.89E-02	9.67E-02	3.12E-03	7.66E-02	1.58E-02	3.04E-02	1.34E-02	2.00E-03	5.70E-03	99.50%
M8-M5-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.73E-02	9.54E-03	4.55E-03	2.50E-03	5.21E-03	2.40E-03	1.41E-03	94.80%
	0.14	2	0.1785	1.961	5.89E-02	7.10E-02	5.57E-03	3.78E-02	5.15E-03	1.63E-02	2.16E-02	2.72E-03	9.46E-03	99.40%
M8-M6-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.79E-02	6.03E-03	2.72E-03	1.66E-03	8.06E-03	3.72E-03	2.17E-03	94.70%
	0.14	2	0.1785	1.961	5.89E-02	6.96E-02	5.93E-03	2.43E-02	3.08E-03	1.06E-02	3.30E-02	4.21E-03	1.44E-02	99.40%
M8-M7-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.73E-02	4.23E-03	1.94E-03	1.15E-03	1.67E-02	8.28E-03	4.21E-03	94.70%
	0.14	2	0.1785	1.961	5.89E-02	8.65E-02	4.60E-03	1.61E-02	2.19E-03	6.93E-03	6.08E-02	9.39E-03	2.57E-02	99.40%
M8-M5-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.40E-02	2.54E-02	1.40E-02	5.70E-03	4.83E-03	2.40E-03	1.22E-03	96.80%
	0.14	2	0.1785	1.961	5.89E-02	9.79E-02	2.51E-03	7.51E-02	1.58E-02	2.96E-02	1.75E-02	2.72E-03	7.41E-03	99.80%
M8-M6-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.77E-02	9.12E-03	4.55E-03	2.29E-03	7.54E-03	3.72E-03	1.91E-03	95.30%
	0.14	2	0.1785	1.961	5.89E-02	7.53E-02	4.14E-03	3.60E-02	5.15E-03	1.54E-02	3.09E-02	4.21E-03	1.33E-02	99.80%
M8-M7-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.29E-01	9.77E-02	5.63E-03	2.72E-03	1.46E-03	1.62E-02	8.28E-03	3.96E-03	95.00%
	0.14	2	0.1785	1.961	5.89E-02	8.83E-02	3.72E-03	2.14E-02	3.08E-03	9.16E-03	5.92E-02	9.39E-03	2.49E-02	99.70%
M8-M6-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.44E-02	2.48E-02	1.40E-02	5.41E-03	7.13E-03	3.72E-03	1.71E-03	97.20%
	0.14	2	0.1785	1.961	5.89E-02	1.01E-01	1.64E-03	7.23E-02	1.58E-02	2.82E-02	2.53E-02	4.21E-03	1.06E-02	99.90%
M8-M7-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.29E-01	9.74E-02	8.77E-03	4.55E-03	2.11E-03	1.57E-02	8.28E-03	3.70E-03	95.60%
	0.14	2	0.1785	1.961	5.89E-02	9.28E-02	2.37E-03	3.20E-02	5.15E-03	1.34E-02	5.60E-02	9.39E-03	2.33E-02	99.90%
M8-M7-M6	0.14	0.14	0.1575	0.1225	7.20E-02	2.32E-01	9.34E-02	2.42E-02	1.40E-02	5.13E-03	1.51E-02	8.28E-03	3.41E-03	97.30%
	0.14	2	0.1785	1.961	5.89E-02	1.16E-01	8.01E-04	6.66E-02	1.58E-02	2.54E-02	4.78E-02	9.39E-03	1.92E-02	100.00%
M9-PO1-FOX	0.1	0.14	0.065	0.175	1.13E+01	1.57E								

Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cat (fF/um)	Cft (fF/um)	
	0.12	2	0.1806	1.939	7.77E-02	7.98E-02	6.20E-03	5.86E-02	8.46E-03	2.51E-02	7.02E-03	9.01E-04	3.06E-03	97.80%
M9-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.47E-01	1.05E-01	2.45E-02	1.24E-02	6.09E-03	1.56E-03	6.89E-04	4.34E-04	95.50%
	0.12	2	0.1806	1.939	7.77E-02	9.91E-02	3.67E-03	8.47E-02	1.62E-02	3.43E-02	5.86E-03	9.01E-04	2.48E-03	98.80%
M9-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.72E-02	9.68E-03	3.82E-03	2.93E-03	2.40E-03	8.90E-04	7.56E-04	94.00%
	0.14	2	0.1785	1.961	5.89E-02	6.56E-02	8.86E-03	3.63E-02	4.34E-03	1.60E-02	9.33E-03	1.01E-03	4.16E-03	96.50%
M9-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.83E-02	1.20E-02	5.08E-03	3.44E-03	2.29E-03	8.90E-04	6.99E-04	94.50%
	0.14	2	0.1785	1.961	5.89E-02	6.98E-02	7.42E-03	4.42E-02	5.76E-03	1.92E-02	8.85E-03	1.01E-03	3.92E-03	97.20%
M9-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.77E-02	6.89E-03	2.44E-03	2.23E-03	2.99E-03	1.03E-03	9.84E-04	93.50%
	0.14	2	0.1785	1.961	5.89E-02	6.07E-02	1.05E-02	2.56E-02	2.77E-03	1.14E-02	1.13E-02	1.16E-03	5.09E-03	95.50%
M9-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.76E-02	7.88E-03	2.90E-03	2.49E-03	2.91E-03	1.03E-03	9.44E-04	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.22E-02	9.76E-03	2.93E-02	3.28E-03	1.30E-02	1.11E-02	1.16E-03	4.95E-03	96.20%
M9-M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.84E-02	5.50E-03	1.79E-03	1.85E-03	3.75E-03	1.21E-03	1.27E-03	93.30%
	0.14	2	0.1785	1.961	5.89E-02	5.91E-02	1.14E-02	1.97E-02	2.03E-03	8.82E-03	1.36E-02	1.37E-03	6.14E-03	95.00%
M9-M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.81E-02	6.00E-03	2.03E-03	1.98E-03	3.63E-03	1.21E-03	1.21E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	5.98E-02	1.09E-02	2.18E-02	2.30E-03	9.73E-03	1.35E-02	1.37E-03	6.04E-03	95.50%
M9-M5-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.85E-02	4.48E-03	1.42E-03	1.53E-03	4.63E-03	1.47E-03	1.58E-03	93.30%
	0.14	2	0.1785	1.961	5.89E-02	5.88E-02	1.16E-02	1.58E-02	1.60E-03	7.10E-03	1.66E-02	1.67E-03	7.46E-03	94.60%
M9-M5-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.83E-02	4.79E-03	1.56E-03	1.62E-03	4.51E-03	1.47E-03	1.52E-03	93.30%
	0.14	2	0.1785	1.961	5.89E-02	5.91E-02	1.13E-02	1.72E-02	1.77E-03	7.69E-03	1.64E-02	1.67E-03	7.37E-03	95.10%
M9-M6-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.85E-02	3.72E-03	1.17E-03	1.27E-03	5.84E-03	1.88E-03	1.98E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.02E-02	1.15E-02	1.31E-02	1.33E-03	5.87E-03	2.08E-02	2.14E-03	9.33E-03	94.50%
M9-M6-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.84E-02	3.94E-03	1.27E-03	1.34E-03	5.74E-03	1.88E-03	1.93E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.04E-02	1.13E-02	1.40E-02	1.43E-03	6.28E-03	2.06E-02	2.14E-03	9.26E-03	94.80%
M9-M7-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.83E-02	3.13E-03	9.97E-04	1.07E-03	7.91E-03	2.61E-03	2.65E-03	92.30%
	0.14	2	0.1785	1.961	5.89E-02	6.67E-02	1.21E-02	1.10E-02	1.13E-03	4.94E-03	2.80E-02	2.96E-03	1.25E-02	94.90%
M9-M7-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.83E-02	3.30E-03	1.07E-03	1.12E-03	7.82E-03	2.61E-03	2.60E-03	92.40%
	0.14	2	0.1785	1.961	5.89E-02	6.68E-02	1.20E-02	1.17E-02	1.21E-03	5.24E-03	2.78E-02	2.96E-03	1.24E-02	95.10%
M9-M8-FOX	0.42	0.42	0.4945	0.3455	2.21E-02	3.14E-01	1.27E-01	4.95E-03	2.62E-03	1.17E-03	4.55E-02	2.60E-02	9.72E-03	97.20%
	0.42	2	0.5005	1.919	2.00E-02	1.53E-01	2.25E-02	1.16E-02	2.65E-03	4.46E-03	9.34E-02	2.63E-02	3.35E-02	98.00%
M9-M8-OD	0.42	0.42	0.4945	0.3455	2.21E-02	3.13E-01	1.27E-01	5.24E-03	2.76E-03	1.24E-03	4.55E-02	2.60E-02	9.73E-03	97.30%
	0.42	2	0.5005	1.919	2.00E-02	1.53E-01	2.24E-02	1.22E-02	2.80E-03	4.70E-03	9.32E-02	2.63E-02	3.35E-02	98.10%
M9-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.50E-01	1.02E-01	3.61E-02	1.94E-02	8.37E-03	1.49E-03	6.89E-04	4.02E-04	96.40%
	0.12	2	0.1806	1.939	7.77E-02	1.18E-01	2.76E-03	1.07E-01	2.53E-02	4.06E-02	5.17E-03	9.01E-04	2.13E-03	99.20%
M9-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.51E-01	1.01E-01	3.86E-02	2.09E-02	8.81E-03	1.48E-03	6.89E-04	3.94E-04	96.50%
	0.12	2	0.1806	1.939	7.77E-02	1.22E-01	2.64E-03	1.11E-01	2.74E-02	4.17E-02	5.07E-03	9.01E-04	2.08E-03	99.20%
M9-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.80E-02	1.33E-02	5.84E-03	3.71E-03	2.23E-03	8.90E-04	6.69E-04	94.80%
	0.14	2	0.1785	1.961	5.89E-02	7.24E-02	6.77E-03	4.84E-02	6.62E-03	2.09E-02	8.61E-03	1.01E-03	3.80E-03	97.50%
M9-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.79E-02	1.35E-02	5.96E-03	3.77E-03	2.22E-03	8.90E-04	6.67E-04	94.80%
	0.14	2	0.1785	1.961	5.89E-02	7.28E-02	6.68E-03	4.90E-02	6.75E-03	2.11E-02	8.58E-03	1.01E-03	3.78E-03	97.50%
M9-M3-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	8.30E-03	3.13E-03	2.58E-03	2.85E-03	1.03E-03	9.14E-04	93.90%
	0.14	2	0.1785	1.961	5.89E-02	6.30E-02	9.40E-03	3.10E-02	3.55E-03	1.37E-02	1.09E-02	1.16E-03	4.89E-03	96.40%
M9-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.75E-02	8.36E-03	3.16E-03	2.60E-03	2.85E-03	1.03E-03	9.10E-04	93.80%
	0.14	2	0.1785	1.961	5.89E-02	6.32E-02	9.34E-03	3.13E-02	3.59E-03	1.39E-02	1.09E-02	1.16E-03	4.88E-03	96.50%
M9-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.78E-02	6.11E-03	2.14E-03	1.99E-03	3.52E-03	1.21E-03	1.16E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.01E-02	1.07E-02	2.28E-02	2.42E-03	1.02E-02	1.34E-02	1.37E-03	6.00E-03	95.80%
M9-M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.78E-02	6.14E-03	2.15E-03	2.00E-03	3.52E-03	1.21E-03	1.15E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.02E-02	1.07E-02	2.29E-02	2.44E-03	1.02E-02	1.34E-02	1.37E-03	6.00E-03	95.80%
M9-M5-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.84E-02	4.93E-03	1.62E-03	1.65E-03	4.46E-03	1.47E-03	1.50E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	5.93E-02	1.12E-02	1.78E-02	1.85E-03	7.99E-03	1.63E-02	1.67E-03	7.33E-03	95.30%
M9-M6-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.84E-02	4.04E-03	1.31E-03	1.37E-03	5.70E-03	1.88E-03	1.91E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.05E-02	1.12E-02	1.44E-02	1.48E-03	6.46E-03	2.06E-02	2.14E-03	9.22E-03	95.00%
M9-M6-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.84E-02	4.06E-03	1.31E-03	1.37E-03	5.69E-03	1.88E-03	1.90E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.05E-02	1.12E-02	1.45E-02	1.49E-03	6.48E-03	2.06E-02	2.14E-03	9.22E-03	95.00%
M9-M7-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.83E-02	3.38E-03	1.10E-03	1.14E-03	7.79E-03	2.61E-03	2.59E-03	92.40%
	0.14	2	0.1785	1.961	5.89E-02	6.69E-02	1.20E-02	1.20E-02	1.24E-03	5.37E-03	2.78E-02	2.96E-03	1.24E-02	95.20%
M9-M7-	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.83E-02	3.39E-03	1.10E-03	1.14E-03	7.79E-03	2.61E-03	2.59E-03	92.40%

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Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
PO1(FOX)														
	0.14	2	0.1785	1.961	5.89E-02	6.69E-02	1.20E-02	1.20E-02	1.25E-03	5.39E-03	2.77E-02	2.96E-03	1.24E-02	95.20%
M9-M8-PO1(OD)	0.42	0.42	0.4945	0.3455	2.21E-02	3.16E-01	1.28E-01	5.34E-03	2.83E-03	1.25E-03	4.54E-02	2.60E-02	9.68E-03	97.30%
	0.42	2	0.5005	1.919	2.00E-02	1.53E-01	2.23E-02	1.25E-02	2.86E-03	4.80E-03	9.32E-02	2.63E-02	3.34E-02	98.10%
M9-M8-PO1(FOX)	0.42	0.42	0.4945	0.3455	2.21E-02	3.16E-01	1.28E-01	5.35E-03	2.84E-03	1.26E-03	4.54E-02	2.60E-02	9.68E-03	97.30%
	0.42	2	0.5005	1.919	2.00E-02	1.53E-01	2.23E-02	1.25E-02	2.87E-03	4.81E-03	9.32E-02	2.63E-02	3.34E-02	98.10%
M9-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.43E-02	2.69E-02	1.40E-02	6.47E-03	2.01E-03	8.90E-04	5.59E-04	96.40%
	0.14	2	0.1785	1.961	5.89E-02	9.56E-02	4.00E-03	7.92E-02	1.58E-02	3.17E-02	7.15E-03	1.01E-03	3.07E-03	98.70%
M9-M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.82E-02	1.08E-02	4.55E-03	3.10E-03	2.62E-03	1.03E-03	7.96E-04	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.79E-02	7.63E-03	4.06E-02	5.15E-03	1.77E-02	1.03E-02	1.16E-03	4.56E-03	97.30%
M9-M4-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.82E-02	7.31E-03	2.72E-03	2.30E-03	3.37E-03	1.21E-03	1.08E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.20E-02	9.71E-03	2.74E-02	3.08E-03	1.22E-02	1.29E-02	1.37E-03	5.78E-03	96.50%
M9-M5-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.80E-02	5.59E-03	1.94E-03	1.83E-03	4.28E-03	1.47E-03	1.40E-03	93.50%
	0.14	2	0.1785	1.961	5.89E-02	6.02E-02	1.06E-02	2.06E-02	2.19E-03	9.19E-03	1.60E-02	1.67E-03	7.19E-03	96.00%
M9-M6-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.85E-02	4.44E-03	1.50E-03	1.47E-03	5.48E-03	1.88E-03	1.80E-03	93.50%
	0.14	2	0.1785	1.961	5.89E-02	6.09E-02	1.08E-02	1.62E-02	1.71E-03	7.27E-03	2.03E-02	2.14E-03	9.09E-03	95.60%
M9-M7-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.99E-02	3.74E-03	1.23E-03	1.26E-03	7.74E-03	2.61E-03	2.56E-03	92.60%
	0.14	2	0.1785	1.961	5.89E-02	6.71E-02	1.17E-02	1.33E-02	1.39E-03	5.93E-03	2.75E-02	2.96E-03	1.23E-02	95.70%
M9-M8-M1	0.42	0.42	0.4945	0.3455	2.21E-02	3.15E-01	1.28E-01	5.78E-03	3.11E-03	1.34E-03	4.51E-02	2.60E-02	9.57E-03	97.30%
	0.42	2	0.5005	1.919	2.00E-02	1.53E-01	2.21E-02	1.36E-02	3.14E-03	5.23E-03	9.30E-02	2.63E-02	3.33E-02	98.30%
M9-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.50E-02	2.66E-02	1.40E-02	6.34E-03	2.27E-03	1.03E-03	6.24E-04	96.40%
	0.14	2	0.1785	1.961	5.89E-02	9.57E-02	3.86E-03	7.88E-02	1.58E-02	3.15E-02	8.16E-03	1.16E-03	3.50E-03	98.90%
M9-M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.78E-02	1.06E-02	4.55E-03	3.01E-03	3.01E-03	1.21E-03	9.02E-04	94.40%
	0.14	2	0.1785	1.961	5.89E-02	6.83E-02	7.35E-03	4.01E-02	5.15E-03	1.75E-02	1.19E-02	1.37E-03	5.28E-03	97.70%
M9-M5-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.87E-02	7.00E-03	2.72E-03	2.14E-03	3.90E-03	1.47E-03	1.21E-03	93.80%
	0.14	2	0.1785	1.961	5.89E-02	6.27E-02	9.24E-03	2.70E-02	3.08E-03	1.20E-02	1.54E-02	1.67E-03	6.85E-03	97.00%
M9-M6-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	5.33E-03	1.94E-03	1.70E-03	5.17E-03	1.88E-03	1.64E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.20E-02	9.99E-03	2.01E-02	2.19E-03	8.94E-03	1.98E-02	2.14E-03	8.84E-03	96.50%
M9-M7-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.87E-02	4.36E-03	1.50E-03	1.43E-03	7.46E-03	2.61E-03	2.42E-03	92.60%
	0.14	2	0.1785	1.961	5.89E-02	6.78E-02	1.12E-02	1.58E-02	1.71E-03	7.05E-03	2.71E-02	2.96E-03	1.20E-02	96.40%
M9-M8-M2	0.42	0.42	0.4945	0.3455	2.21E-02	3.14E-01	1.27E-01	6.72E-03	3.64E-03	1.54E-03	4.49E-02	2.60E-02	9.47E-03	97.50%
	0.42	2	0.5005	1.919	2.00E-02	1.54E-01	2.17E-02	1.58E-02	3.69E-03	6.04E-03	9.28E-02	2.63E-02	3.32E-02	98.50%
M9-M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.46E-02	2.65E-02	1.40E-02	6.26E-03	2.65E-03	1.21E-03	7.19E-04	96.50%
	0.14	2	0.1785	1.961	5.89E-02	9.60E-02	3.67E-03	7.82E-02	1.58E-02	3.12E-02	9.51E-03	1.37E-03	4.07E-03	99.10%
M9-M5-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.77E-02	1.03E-02	4.55E-03	2.89E-03	3.56E-03	1.47E-03	1.05E-03	94.50%
	0.14	2	0.1785	1.961	5.89E-02	6.90E-02	6.94E-03	3.95E-02	5.15E-03	1.72E-02	1.42E-02	1.67E-03	6.27E-03	98.10%
M9-M6-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.86E-02	6.82E-03	2.72E-03	2.05E-03	4.81E-03	1.88E-03	1.46E-03	94.00%
	0.14	2	0.1785	1.961	5.89E-02	6.45E-02	8.70E-03	2.64E-02	3.08E-03	1.17E-02	1.90E-02	2.14E-03	8.45E-03	97.50%
M9-M7-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.85E-02	5.29E-03	1.94E-03	1.68E-03	7.13E-03	2.61E-03	2.26E-03	92.80%
	0.14	2	0.1785	1.961	5.89E-02	6.89E-02	1.04E-02	1.96E-02	2.19E-03	8.72E-03	2.65E-02	2.96E-03	1.18E-02	97.20%
M9-M8-M3	0.42	0.42	0.4945	0.3455	2.21E-02	3.14E-01	1.27E-01	7.95E-03	4.40E-03	1.78E-03	4.46E-02	2.60E-02	9.29E-03	97.60%
	0.42	2	0.5005	1.919	2.00E-02	1.55E-01	2.10E-02	1.88E-02	4.45E-03	7.17E-03	9.24E-02	2.63E-02	3.30E-02	98.90%
M9-M5-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.47E-02	2.62E-02	1.40E-02	6.14E-03	3.17E-03	1.47E-03	8.49E-04	96.60%
	0.14	2	0.1785	1.961	5.89E-02	9.64E-02	3.42E-03	7.74E-02	1.58E-02	3.08E-02	1.14E-02	1.67E-03	4.86E-03	99.20%
M9-M6-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.78E-02	1.01E-02	4.55E-03	2.79E-03	4.43E-03	1.88E-03	1.27E-03	94.70%
	0.14	2	0.1785	1.961	5.89E-02	7.05E-02	6.50E-03	3.88E-02	5.15E-03	1.68E-02	1.76E-02	2.14E-03	7.75E-03	98.40%
M9-M7-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.89E-02	6.82E-03	2.72E-03	2.05E-03	6.69E-03	2.61E-03	2.04E-03	93.10%
	0.14	2	0.1785	1.961	5.89E-02	7.12E-02	9.15E-03	2.59E-02	3.08E-03	1.14E-02	2.56E-02	2.96E-03	1.13E-02	98.00%
M9-M8-M4	0.42	0.42	0.4945	0.3455	2.21E-02	3.17E-01	1.28E-01	9.84E-03	5.55E-03	2.15E-03	4.42E-02	2.60E-02	9.10E-03	97.80%
	0.42	2	0.5005	1.919	2.00E-02	1.57E-01	2.01E-02	2.33E-02	5.62E-03	8.83E-03	9.19E-02	2.63E-02	3.28E-02	99.20%
M9-M6-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.44E-02	2.60E-02	1.40E-02	6.00E-03	3.97E-03	1.88E-03	1.04E-03	96.70%
	0.14	2	0.1785	1.961	5.89E-02	9.76E-02	3.18E-03	7.64E-02	1.58E-02	3.03E-02	1.42E-02	2.14E-03	6.03E-03	99.30%
M9-M7-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.78E-02	1.02E-02	4.55E-03	2.81E-03	6.19E-03	2.61E-03	1.79E-03	93.70%
	0.14	2	0.1785	1.961	5.89E-02	7.73E-02	7.06E-03	3.83E-02	5.15E-03	1.65E-02	2.39E-02	2.96E-03	1.05E-02	98.70%
M9-M8-M5	0.42	0.42	0.4945	0.3455	2.21E-02	3.15E-01	1.26E-01	1.30E-02	7.52E-03	2.74E-03	4.38E-02	2.60E-02	8.89E-03	98.10%
	0.42	2	0.5005	1.919	2.00E-02	1.60E-01	1.85E-02	3.06E-02	7.62E-03	1.15E-02	9.13E-02	2.63E-02	3.25E-02	99.60%
M9-M7-M6	0.14	0.14	0.1575	0.1225	7.20E-02	2.31E-01	9.47E-02	2.62E-02	1.40E-02	6.13E-03	5.62E-03	2.61E-03	1.50E-03	95.70%
	0.14	2	0.1785	1.961	5.89E-02	1.04E-01	3.71E-01	7.63E-02	1.58E-02	3.02E-02	1.96E-02	2.96E-03	8.31E-03	99.50%
M9-M8-M6	0.42	0.42	0.4945	0.3455	2.21E-02	3.18E-01	1.25E-01	1.97E-02	1.17E-02	3.99E-03	4.			

Structure	(as drawn)		(after process bias)											
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cab (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cat (fF/um)	Cft (fF/um)	Csum/ Ctotal
M10-M1-OD	0.12	0.12	0.138	0.102	1.00E-01	2.47E-01	1.05E-01	2.47E-02	1.24E-02	6.17E-03	1.30E-03	5.70E-04	3.65E-04	95.40%
	0.12	2	0.1806	1.939	7.77E-02	9.91E-02	3.78E-03	8.52E-02	1.62E-02	3.45E-02	4.91E-03	7.46E-04	2.08E-03	98.60%
M10-M2-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.75E-02	1.01E-02	3.82E-03	3.15E-03	2.06E-03	7.20E-04	6.70E-04	94.00%
	0.14	2	0.1785	1.961	5.89E-02	6.55E-02	9.08E-03	3.69E-02	4.34E-03	1.63E-02	7.73E-03	8.16E-04	3.46E-03	95.90%
M10-M2-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.68E-02	1.20E-02	5.08E-03	3.46E-03	1.87E-03	7.20E-04	5.74E-04	94.30%
	0.14	2	0.1785	1.961	5.89E-02	6.97E-02	7.62E-03	4.48E-02	5.76E-03	1.95E-02	7.32E-03	8.16E-04	3.25E-03	96.60%
M10-M3-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.80E-02	7.34E-03	2.44E-03	2.45E-03	2.54E-03	8.06E-04	8.67E-04	93.40%
	0.14	2	0.1785	1.961	5.89E-02	6.04E-02	1.09E-02	2.62E-02	2.77E-03	1.17E-02	9.23E-03	9.14E-04	4.16E-03	94.60%
M10-M3-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.74E-02	8.02E-03	2.90E-03	2.56E-03	2.36E-03	8.06E-04	7.75E-04	93.60%
	0.14	2	0.1785	1.961	5.89E-02	6.19E-02	1.01E-02	2.98E-02	3.28E-03	1.33E-02	8.96E-03	9.14E-04	4.02E-03	95.20%
M10-M4-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.92E-02	5.87E-03	1.79E-03	2.04E-03	3.07E-03	9.15E-04	1.08E-03	93.20%
	0.14	2	0.1785	1.961	5.89E-02	5.86E-02	1.19E-02	2.03E-02	2.03E-03	9.13E-03	1.08E-02	1.04E-03	4.88E-03	93.60%
M10-M4-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.76E-02	6.23E-03	2.03E-03	2.10E-03	2.90E-03	9.15E-04	9.93E-04	93.20%
	0.14	2	0.1785	1.961	5.89E-02	5.93E-02	1.14E-02	2.24E-02	2.30E-03	1.01E-02	1.06E-02	1.04E-03	4.79E-03	94.20%
M10-M5-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.87E-02	4.89E-03	1.42E-03	1.74E-03	3.70E-03	1.06E-03	1.32E-03	93.10%
	0.14	2	0.1785	1.961	5.89E-02	5.81E-02	1.24E-02	1.65E-02	1.60E-03	7.43E-03	1.26E-02	1.20E-03	5.72E-03	92.80%
M10-M5-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.97E-02	5.22E-03	1.56E-03	1.83E-03	3.60E-03	1.06E-03	1.27E-03	93.30%
	0.14	2	0.1785	1.961	5.89E-02	5.84E-02	1.21E-02	1.78E-02	1.77E-03	8.04E-03	1.25E-02	1.20E-03	5.64E-03	93.20%
M10-M6-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.21E-01	9.86E-02	4.20E-03	1.17E-03	1.51E-03	4.51E-03	1.26E-03	1.62E-03	93.10%
	0.14	2	0.1785	1.961	5.89E-02	5.88E-02	1.27E-02	1.38E-02	1.33E-03	6.21E-03	1.49E-02	1.42E-03	6.75E-03	91.80%
M10-M6-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	4.43E-03	1.27E-03	1.58E-03	4.41E-03	1.26E-03	1.58E-03	93.20%
	0.14	2	0.1785	1.961	5.89E-02	5.90E-02	1.25E-02	1.47E-02	1.43E-03	6.63E-03	1.48E-02	1.42E-03	6.68E-03	92.20%
M10-M7-FOX	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.86E-02	3.75E-03	9.97E-04	1.38E-03	5.80E-03	1.54E-03	2.13E-03	91.90%
	0.14	2	0.1785	1.961	5.89E-02	6.40E-02	1.42E-02	1.18E-02	1.13E-03	5.33E-03	1.83E-02	1.75E-03	8.26E-03	91.50%
M10-M7-OD	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.98E-02	3.94E-03	1.07E-03	1.44E-03	5.72E-03	1.54E-03	2.09E-03	92.00%
	0.14	2	0.1785	1.961	5.89E-02	6.41E-02	1.41E-02	1.25E-02	1.21E-03	5.64E-03	1.81E-02	1.75E-03	8.19E-03	91.80%
M10-M8-FOX	0.42	0.42	0.4945	0.3455	2.21E-02	3.05E-01	1.35E-01	5.32E-03	2.62E-03	1.35E-03	1.60E-02	8.13E-03	3.94E-03	95.30%
	0.42	2	0.5005	1.919	2.00E-02	1.18E-01	3.24E-02	1.23E-02	2.65E-03	4.81E-03	3.64E-02	8.23E-03	1.41E-02	95.90%
M10-M8-OD	0.42	0.42	0.4945	0.3455	2.21E-02	3.05E-01	1.35E-01	5.58E-03	2.76E-03	1.41E-03	1.60E-02	8.13E-03	3.91E-03	95.30%
	0.42	2	0.5005	1.919	2.00E-02	1.18E-01	3.23E-02	1.29E-02	2.80E-03	5.06E-03	3.63E-02	8.23E-03	1.40E-02	96.10%
M10-M9-FOX	0.42	0.42	0.4945	0.3455	2.21E-02	3.31E-01	1.35E-01	4.28E-03	2.15E-03	1.07E-03	4.59E-02	2.53E-02	1.03E-02	97.00%
	0.42	2	0.5005	1.919	2.00E-02	1.59E-01	2.47E-02	9.74E-03	2.17E-03	3.79E-03	9.53E-02	2.56E-02	3.49E-02	96.90%
M10-M9-OD	0.42	0.42	0.4945	0.3455	2.21E-02	3.30E-01	1.35E-01	4.47E-03	2.25E-03	1.11E-03	4.59E-02	2.53E-02	1.03E-02	97.00%
	0.42	2	0.5005	1.919	2.00E-02	1.59E-01	2.46E-02	1.02E-02	2.27E-03	3.95E-03	9.52E-02	2.56E-02	3.48E-02	97.00%
M10-M1-PO1(OD)	0.12	0.12	0.138	0.102	1.00E-01	2.50E-01	1.02E-01	3.63E-02	1.94E-02	8.48E-03	1.25E-03	5.70E-04	3.42E-04	96.40%
	0.12	2	0.1806	1.939	7.77E-02	1.18E-01	2.78E-03	1.07E-01	2.53E-02	4.09E-02	4.33E-03	7.46E-04	1.79E-03	99.10%
M10-M1-PO1(FOX)	0.12	0.12	0.138	0.102	1.00E-01	2.52E-01	1.01E-01	3.89E-02	2.09E-02	8.98E-03	1.25E-03	5.70E-04	3.39E-04	96.60%
	0.12	2	0.1806	1.939	7.77E-02	1.22E-01	2.73E-03	1.11E-01	2.74E-02	4.20E-02	4.23E-03	7.46E-04	1.74E-03	99.10%
M10-M2-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.78E-02	1.34E-02	5.84E-03	3.79E-03	1.84E-03	7.20E-04	5.58E-04	94.70%
	0.14	2	0.1785	1.961	5.89E-02	7.22E-02	6.96E-03	4.90E-02	6.62E-03	2.12E-02	7.11E-03	8.16E-04	3.15E-03	97.00%
M10-M2-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.77E-02	1.36E-02	5.96E-03	3.83E-03	1.83E-03	7.20E-04	5.54E-04	94.70%
	0.14	2	0.1785	1.961	5.89E-02	7.26E-02	6.87E-03	4.96E-02	6.75E-03	2.14E-02	7.09E-03	8.16E-04	3.13E-03	97.00%
M10-M3-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.75E-02	8.43E-03	3.13E-03	2.65E-03	2.30E-03	8.06E-04	7.49E-04	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.26E-02	9.68E-03	3.17E-02	3.55E-03	1.41E-02	8.87E-03	9.14E-04	3.98E-03	95.60%
M10-M3-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.75E-02	8.49E-03	3.16E-03	2.66E-03	2.30E-03	8.06E-04	7.45E-04	93.70%
	0.14	2	0.1785	1.961	5.89E-02	6.28E-02	9.63E-03	3.19E-02	3.59E-03	1.42E-02	8.85E-03	9.14E-04	3.97E-03	95.70%
M10-M4-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.76E-02	6.45E-03	2.14E-03	2.16E-03	2.85E-03	9.15E-04	9.69E-04	93.30%
	0.14	2	0.1785	1.961	5.89E-02	5.97E-02	1.12E-02	2.36E-02	2.44E-03	1.06E-02	1.05E-02	1.04E-03	4.76E-03	94.50%
M10-M4-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.76E-02	6.48E-03	2.15E-03	2.16E-03	2.85E-03	9.15E-04	9.66E-04	93.30%
	0.14	2	0.1785	1.961	5.89E-02	5.97E-02	1.12E-02	2.36E-02	2.44E-03	1.06E-02	1.05E-02	1.04E-03	4.75E-03	94.50%
M10-M5-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	5.34E-03	1.62E-03	1.86E-03	3.54E-03	1.06E-03	1.24E-03	93.20%
	0.14	2	0.1785	1.961	5.89E-02	5.87E-02	1.20E-02	1.85E-02	1.84E-03	8.33E-03	1.24E-02	1.20E-03	5.62E-03	93.50%
M10-M5-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.96E-02	5.38E-03	1.63E-03	1.87E-03	3.54E-03	1.06E-03	1.24E-03	93.20%

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Structure	(as drawn)		(after process bias)												
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)									
M10-M6-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	5.87E-02	1.19E-02	1.86E-02	1.85E-03	8.36E-03	1.24E-02	1.20E-03	5.62E-03	93.50%	
M10-M6-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	4.54E-03	1.31E-03	1.61E-03	4.37E-03	1.26E-03	1.56E-03	93.20%	
M10-M6-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	5.91E-02	1.24E-02	1.51E-02	1.48E-03	6.82E-03	1.47E-02	1.42E-03	6.65E-03	92.40%	
M10-M7-PO1(OD)	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	4.55E-03	1.31E-03	1.62E-03	4.37E-03	1.26E-03	1.56E-03	93.20%	
M10-M7-PO1(OD)	0.14	2	0.1785	1.961	5.89E-02	5.91E-02	1.24E-02	1.52E-02	1.49E-03	6.84E-03	1.47E-02	1.42E-03	6.65E-03	92.40%	
M10-M7-PO1(FOX)	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.91E-02	4.00E-03	1.10E-03	1.45E-03	5.62E-03	1.54E-03	2.04E-03	91.90%	
M10-M7-PO1(FOX)	0.14	2	0.1785	1.961	5.89E-02	6.42E-02	1.41E-02	1.28E-02	1.24E-03	5.78E-03	1.81E-02	1.75E-03	8.17E-03	91.90%	
M10-M8-PO1(OD)	0.42	0.42	0.4945	0.3455	2.21E-02	3.05E-01	1.35E-01	5.70E-03	2.83E-03	1.43E-03	1.59E-02	8.13E-03	3.89E-03	95.40%	
M10-M8-PO1(OD)	0.42	2	0.5005	1.919	2.00E-02	1.18E-01	3.23E-02	1.32E-02	2.86E-03	5.16E-03	3.62E-02	8.23E-03	1.40E-02	96.20%	
M10-M8-PO1(FOX)	0.42	0.42	0.4945	0.3455	2.21E-02	3.05E-01	1.35E-01	5.71E-03	2.84E-03	1.44E-03	1.59E-02	8.13E-03	3.89E-03	95.40%	
M10-M9-PO1(OD)	0.42	0.42	0.4945	0.3455	2.21E-02	3.30E-01	1.35E-01	4.55E-03	2.29E-03	1.13E-03	4.58E-02	2.53E-02	1.03E-02	97.00%	
M10-M9-PO1(FOX)	0.42	2	0.5005	1.919	2.00E-02	1.59E-01	2.46E-02	1.03E-02	2.32E-03	4.02E-03	9.51E-02	2.56E-02	3.48E-02	97.00%	
M10-M9-PO1(FOX)	0.42	0.42	0.4945	0.3455	2.21E-02	3.30E-01	1.35E-01	4.56E-03	2.29E-03	1.13E-03	4.58E-02	2.53E-02	1.03E-02	97.00%	
M10-M2-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.43E-02	2.72E-02	1.40E-02	6.62E-03	1.66E-03	7.20E-04	4.71E-04	96.40%	
M10-M3-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.20E-01	9.70E-02	1.09E-02	4.55E-03	3.16E-03	2.10E-03	8.06E-04	6.46E-04	94.20%	
M10-M4-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.74E-02	7.54E-03	5.15E-03	1.80E-02	8.30E-03	9.14E-04	3.69E-03	96.60%	
M10-M5-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.19E-01	9.74E-02	7.54E-03	5.15E-03	1.80E-02	8.30E-03	9.15E-04	8.76E-04	93.50%	
M10-M5-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.94E-02	6.03E-03	1.94E-03	2.04E-03	3.38E-03	1.06E-03	1.16E-03	93.40%	
M10-M6-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	5.00E-03	1.50E-03	1.75E-03	4.22E-03	1.26E-03	1.48E-03	93.30%	
M10-M7-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.56E-02	1.20E-02	5.93E-03	1.45E-03	1.76E-03	4.22E-03	1.42E-03	6.54E-03	93.10%
M10-M7-M1	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.56E-02	1.20E-02	5.93E-03	1.45E-03	1.76E-03	4.22E-03	1.42E-03	6.54E-03	92.00%
M10-M8-M1	0.42	0.42	0.4945	0.3455	2.21E-02	3.02E-01	1.33E-01	6.18E-03	3.11E-03	1.54E-03	1.58E-02	8.13E-03	3.82E-03	95.40%	
M10-M9-M1	0.42	2	0.5005	1.919	2.00E-02	1.19E-01	3.20E-02	1.44E-02	3.14E-03	5.61E-03	3.61E-02	8.23E-03	1.39E-02	96.40%	
M10-M9-M1	0.42	0.42	0.4945	0.3455	2.21E-02	3.31E-01	1.35E-01	4.86E-03	2.47E-03	1.20E-03	4.57E-02	2.53E-02	1.02E-02	97.00%	
M10-M3-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.38E-02	2.71E-02	1.40E-02	5.50E-03	1.85E-03	8.06E-04	5.21E-04	96.40%	
M10-M4-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.80E-02	1.09E-02	4.55E-03	3.19E-03	2.40E-03	9.15E-04	7.43E-04	94.40%	
M10-M5-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.79E-02	7.73E-03	4.09E-02	5.15E-03	1.79E-02	9.33E-03	1.04E-03	4.15E-03	96.80%
M10-M6-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.89E-02	7.56E-03	2.72E-03	2.42E-03	3.09E-03	1.06E-03	1.01E-03	93.70%	
M10-M7-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	9.00E-02	7.97E-02	3.08E-03	1.24E-02	1.16E-02	1.20E-03	5.20E-03	95.50%	
M10-M8-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.88E-02	5.93E-03	1.94E-03	2.00E-03	3.95E-03	1.26E-03	1.34E-03	93.50%	
M10-M9-M2	0.14	2	0.1785	1.961	5.89E-02	6.08E-02	1.11E-02	2.10E-02	2.19E-03	9.42E-03	1.41E-02	1.42E-03	6.36E-03	94.40%	
M10-M7-M2	0.14	0.14	0.1575	0.1225	7.20E-02	2.28E-01	1.00E-01	5.06E-03	1.50E-03	1.78E-03	5.28E-03	1.54E-03	1.87E-03	92.20%	
M10-M8-M2	0.42	0.42	0.4945	0.3455	2.21E-02	3.03E-01	1.34E-01	7.08E-03	3.64E-03	1.72E-03	1.55E-02	8.13E-03	3.71E-03	95.50%	
M10-M9-M2	0.42	2	0.5005	1.919	2.00E-02	1.19E-01	3.15E-02	1.66E-02	3.69E-03	6.48E-03	3.59E-02	8.23E-03	1.38E-02	96.80%	
M10-M9-M2	0.42	0.42	0.4945	0.3455	2.21E-02	3.34E-01	1.37E-01	5.42E-03	2.79E-03	1.32E-03	4.53E-02	2.53E-02	1.00E-02	97.10%	
M10-M4-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.49E-02	2.69E-02	1.40E-02	6.49E-03	2.08E-03	9.15E-04	5.82E-04	96.50%	
M10-M5-M3	0.14	2	0.1785	1.961	5.89E-02	9.57E-02	3.94E-03	7.91E-02	1.58E-02	3.17E-02	7.38E-03	1.04E-03	3.17E-03	98.70%	
M10-M5-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.85E-02	1.08E-02	4.55E-03	3.13E-03	2.74E-03	1.06E-03	8.38E-04	94.50%	
M10-M6-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.90E-02	7.48E-03	2.72E-03	2.38E-03	3.62E-03	1.26E-03	1.18E-03	93.80%	
M10-M7-M3	0.14	0.14	0.1575	0.1225	7.20E-02	2.25E-01	9.85E-02	6.02E-03	1.94E-03	2.04E-03	4.95E-03	1.54E-03	1.70E-03	92.30%	
M10-M8-M3	0.42	0.42	0.4945	0.3455	2.21E-02	3.05E-01	1.34E-01	8.40E-03	4.40E-03	2.00E-03	1.54E-02	8.13E-03	3.62E-03	95.70%	
M10-M9-M3	0.42	2	0.5005	1.919	2.00E-02	1.20E-01	3.08E-02	1.98E-02	4.45E-03	7.67E-03	3.57E-02	8.23E-03	1.37E-02	97.40%	
M10-M5-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.49E-02	2.67E-02	1.40E-02	6.39E-03	2.38E-03	1.06E-03	6.59E-04	96.50%	
M10-M6-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.22E-01	9.77E-02	1.08E-02	4.55E-03	3.11E-03	3.23E-03	1.26E-03	9.85E-04	94.50%	

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Structure	(as drawn)		(after process bias)											
	width (um)	space (um)	width (um)	space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Cap (fF/um)	Cfb (fF/um)	Ctop (fF/um)	Cap (fF/um)	Cft (fF/um)	Csum/ Ctotal
	0.14	2	0.1785	1.961	5.89E-02	6.96E-02	7.42E-03	4.02E-02	5.15E-03	1.75E-02	1.25E-02	1.42E-03	5.53E-03	97.00%
M10-M7-M4	0.14	0.14	0.1575	0.1225	7.20E-02	2.23E-01	9.73E-02	7.66E-03	2.72E-03	2.47E-03	4.60E-03	1.54E-03	1.53E-03	92.60%
	0.14	2	0.1785	1.961	5.89E-02	6.87E-02	1.10E-02	2.74E-02	3.08E-03	1.22E-02	1.65E-02	1.75E-03	7.38E-03	95.80%
M10-M8-M4	0.42	0.42	0.4945	0.3455	2.21E-02	3.04E-01	1.33E-01	1.03E-02	5.55E-03	2.38E-03	1.51E-02	8.13E-03	3.50E-03	96.00%
	0.42	2	0.5005	1.919	2.00E-02	1.22E-01	2.97E-02	2.45E-02	5.62E-03	9.43E-03	3.55E-02	8.23E-03	1.36E-02	97.90%
M10-M9-M4	0.42	0.42	0.4945	0.3455	2.21E-02	3.32E-01	1.35E-01	7.19E-03	3.80E-03	1.70E-03	4.49E-02	2.53E-02	9.80E-03	97.30%
	0.42	2	0.5005	1.919	2.00E-02	1.61E-01	2.35E-02	1.66E-02	3.84E-03	6.36E-03	9.38E-02	2.56E-02	3.41E-02	97.90%
M10-M6-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.26E-01	9.44E-02	2.68E-02	1.40E-02	6.40E-03	2.82E-03	1.26E-03	7.82E-04	96.60%
	0.14	2	0.1785	1.961	5.89E-02	9.69E-02	3.79E-03	7.81E-02	1.58E-02	3.12E-02	9.91E-03	1.42E-03	4.24E-03	98.70%
M10-M7-M5	0.14	0.14	0.1575	0.1225	7.20E-02	2.27E-01	9.83E-02	1.11E-02	4.55E-03	3.26E-03	4.13E-03	1.54E-03	1.29E-03	93.40%
	0.14	2	0.1785	1.961	5.89E-02	7.50E-02	8.65E-03	4.02E-02	5.15E-03	1.75E-02	1.53E-02	1.75E-03	6.78E-03	97.00%
M10-M8-M5	0.42	0.42	0.4945	0.3455	2.21E-02	3.05E-01	1.33E-01	1.35E-02	7.52E-03	2.99E-03	1.48E-02	8.13E-03	3.35E-03	96.40%
	0.42	2	0.5005	1.919	2.00E-02	1.25E-01	2.80E-02	3.21E-02	7.62E-03	1.23E-02	3.51E-02	8.23E-03	1.35E-02	98.50%
M10-M9-M5	0.42	0.42	0.4945	0.3455	2.21E-02	3.32E-01	1.36E-01	8.55E-03	4.62E-03	1.96E-03	4.43E-02	2.53E-02	9.54E-03	97.40%
	0.42	2	0.5005	1.919	2.00E-02	1.61E-01	2.28E-02	1.99E-02	4.68E-03	7.59E-03	9.33E-02	2.56E-02	3.39E-02	98.30%
M10-M7-M6	0.14	0.14	0.1575	0.1225	7.20E-02	2.30E-01	9.42E-02	2.73E-02	1.40E-02	6.69E-03	3.62E-03	1.54E-03	1.04E-03	95.50%
	0.14	2	0.1785	1.961	5.89E-02	1.02E-01	4.79E-03	7.91E-02	1.58E-02	3.16E-02	1.24E-02	1.75E-03	5.32E-03	98.70%
M10-M8-M6	0.42	0.42	0.4945	0.3455	2.21E-02	3.11E-01	1.33E-01	2.01E-02	1.17E-02	4.24E-03	1.45E-02	8.13E-03	3.20E-03	97.00%
	0.42	2	0.5005	1.919	2.00E-02	1.33E-01	2.50E-02	4.72E-02	1.18E-02	1.77E-02	3.48E-02	8.23E-03	1.33E-02	99.00%
M10-M9-M6	0.42	0.42	0.4945	0.3455	2.21E-02	3.33E-01	1.35E-01	1.06E-02	5.92E-03	2.36E-03	4.38E-02	2.53E-02	9.28E-03	97.60%
	0.42	2	0.5005	1.919	2.00E-02	1.63E-01	2.17E-02	2.49E-02	5.99E-03	9.45E-03	9.28E-02	2.56E-02	3.36E-02	98.90%
M10-M8-M7	0.42	0.42	0.4945	0.3455	2.21E-02	3.18E-01	1.27E-01	4.30E-02	2.60E-02	8.48E-03	1.44E-02	8.13E-03	3.12E-03	98.00%
	0.42	2	0.5005	1.919	2.00E-02	1.61E-01	1.87E-02	8.88E-02	2.63E-02	3.12E-02	3.36E-02	8.23E-03	1.27E-02	99.40%
M10-M9-M7	0.42	0.42	0.4945	0.3455	2.21E-02	3.31E-01	1.33E-01	1.43E-02	8.21E-03	3.06E-03	4.33E-02	2.53E-02	9.03E-03	98.10%
	0.42	2	0.5005	1.919	2.00E-02	1.66E-01	1.99E-02	3.33E-02	8.31E-03	1.25E-02	9.20E-02	2.56E-02	3.32E-02	99.40%
M10-M9-M8	0.42	0.42	0.4945	0.3455	2.21E-02	3.44E-01	1.29E-01	4.24E-02	2.60E-02	8.19E-03	4.27E-02	2.53E-02	8.70E-03	99.50%
	0.42	2	0.5005	1.919	2.00E-02	1.97E-01	1.16E-02	8.55E-02	2.63E-02	2.96E-02	8.86E-02	2.56E-02	3.15E-02	100.00%

### 13.16.3.2M1MxMz process in CLN85G 1.0V/2.5V, no My/Mu, x=2~7, z=8~9

(a) Structure A at 25 °C

Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.69E-01	6.49E-02	2.59E-02	6.07E-03	9.94E-03	92.10%
	0.094	1.8471	0.065	1.876	1.14E+01	8.96E-02	4.08E-03	7.97E-02	6.07E-03	3.68E-02	98.10%
M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.56E-01	1.13E-01	1.55E-02	6.14E-03	4.66E-03	94.00%
	0.113	1.88	0.1736	1.819	7.60E-02	7.94E-02	7.37E-03	6.15E-02	8.13E-03	2.67E-02	96.10%
M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.59E-01	1.11E-01	2.41E-02	1.17E-02	6.21E-03	95.20%
	0.113	1.88	0.1736	1.819	7.60E-02	9.84E-02	4.56E-03	8.68E-02	1.56E-02	3.56E-02	97.50%
M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.59E-01	1.07E-01	3.50E-02	1.84E-02	8.31E-03	96.10%
	0.113	1.88	0.1736	1.819	7.60E-02	1.17E-01	3.41E-03	1.08E-01	2.44E-02	4.21E-02	98.30%
M1-PO1(FOX)	0.113	0.113	0.131	0.095	1.00E-01	2.62E-01	1.07E-01	3.74E-02	1.99E-02	8.77E-03	96.30%
	0.113	1.88	0.1736	1.819	7.60E-02	1.21E-01	3.26E-03	1.12E-01	2.63E-02	4.31E-02	98.40%
M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	1.13E-02	3.63E-03	3.82E-03	93.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.54E-02	1.04E-02	4.01E-02	4.14E-03	1.80E-02	93.20%
M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	1.32E-02	4.82E-03	4.18E-03	94.40%
	0.132	1.88	0.1705	1.841	5.84E-02	6.93E-02	8.87E-03	4.78E-02	5.50E-03	2.11E-02	94.50%
M2-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.01E-01	1.44E-02	5.54E-03	4.41E-03	94.60%
	0.132	1.88	0.1705	1.841	5.84E-02	7.18E-02	8.16E-03	5.19E-02	6.32E-03	2.28E-02	95.00%
M2-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.01E-01	1.46E-02	5.66E-03	4.45E-03	94.60%
	0.132	1.88	0.1705	1.841	5.84E-02	7.22E-02	8.06E-03	5.25E-02	6.45E-03	2.30E-02	95.10%
M2-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.00E-01	2.70E-02	1.33E-02	6.88E-03	96.30%
	0.132	1.88	0.1705	1.841	5.84E-02	9.47E-02	4.96E-03	8.23E-02	1.51E-02	3.36E-02	97.40%
M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	8.85E-03	2.32E-03	3.27E-03	93.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.03E-02	1.24E-02	2.99E-02	2.64E-03	1.36E-02	90.70%
M3-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	9.60E-03	2.75E-03	3.43E-03	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.17E-02	1.15E-02	3.36E-02	3.14E-03	1.52E-02	91.80%
M3-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	1.00E-02	2.97E-03	3.52E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.26E-02	1.12E-02	3.53E-02	3.39E-03	1.59E-02	92.20%
M3-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	1.01E-02	3.00E-03	3.53E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.27E-02	1.11E-02	3.55E-02	3.43E-03	1.61E-02	92.30%
M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.02E-01	1.23E-02	4.32E-03	3.97E-03	94.10%
	0.132	1.88	0.1705	1.841	5.84E-02	6.73E-02	9.30E-03	4.47E-02	4.92E-03	1.99E-02	94.00%
M3-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.02E-01	2.71E-02	1.33E-02	6.93E-03	96.40%
	0.132	1.88	0.1705	1.841	5.84E-02	9.47E-02	4.91E-03	8.23E-02	1.51E-02	3.36E-02	97.30%
M4-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.04E-01	7.70E-03	1.70E-03	3.00E-03	93.00%
	0.132	1.88	0.1705	1.841	5.84E-02	5.83E-02	1.36E-02	2.44E-02	1.94E-03	1.12E-02	88.40%
M4-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.04E-01	8.13E-03	1.92E-03	3.10E-03	93.20%
	0.132	1.88	0.1705	1.841	5.84E-02	5.90E-02	1.31E-02	2.65E-02	2.19E-03	1.21E-02	89.30%
M4-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	8.32E-03	2.03E-03	3.15E-03	93.20%
	0.132	1.88	0.1705	1.841	5.84E-02	5.93E-02	1.29E-02	2.75E-02	2.31E-03	1.26E-02	89.70%
M4-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	8.35E-03	2.04E-03	3.15E-03	93.20%
	0.132	1.88	0.1705	1.841	5.84E-02	5.94E-02	1.28E-02	2.76E-02	2.33E-03	1.26E-02	89.70%
M4-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	9.35E-03	2.58E-03	3.39E-03	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.11E-02	1.18E-02	3.22E-02	2.94E-03	1.47E-02	91.30%
M4-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	1.23E-02	4.32E-03	4.00E-03	94.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.73E-02	9.18E-03	4.48E-02	4.92E-03	2.00E-02	93.90%
M4-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.01E-01	2.72E-02	1.33E-02	6.96E-03	96.40%
	0.132	1.88	0.1705	1.841	5.84E-02	9.47E-02	4.87E-03	8.24E-02	1.51E-02	3.36E-02	97.30%
M5-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.04E-01	7.04E-03	1.34E-03	2.85E-03	92.80%
	0.132	1.88	0.1705	1.841	5.84E-02	5.76E-02	1.44E-02	2.09E-02	1.53E-03	9.69E-03	86.20%
M5-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	7.34E-03	1.48E-03	2.93E-03	93.00%
	0.132	1.88	0.1705	1.841	5.84E-02	5.79E-02	1.40E-02	2.23E-02	1.69E-03	1.03E-02	86.90%
M5-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	7.46E-03	1.54E-03	2.96E-03	93.00%
	0.132	1.88	0.1705	1.841	5.84E-02	5.81E-02	1.39E-02	2.29E-02	1.76E-03	1.06E-02	87.30%
M5-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	7.48E-03	1.55E-03	2.96E-03	93.00%
	0.132	1.88	0.1705	1.841	5.84E-02	5.81E-02	1.39E-02	2.30E-02	1.77E-03	1.06E-02	87.30%
M5-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	8.04E-03	1.84E-03	3.10E-03	93.20%
	0.132	1.88	0.1705	1.841	5.84E-02	5.90E-02	1.32E-02	2.58E-02	2.10E-03	1.18E-02	88.60%
M5-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	9.39E-03	2.58E-03	3.40E-03	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.14E-02	1.17E-02	3.24E-02	2.94E-03	1.47E-02	90.90%
M5-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	1.24E-02	4.32E-03	4.04E-03	94.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.76E-02	9.14E-03	4.50E-02	4.92E-03	2.00E-02	93.60%
M5-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.01E-01	2.72E-02	1.33E-02	6.98E-03	96.40%
	0.132	1.88	0.1705	1.841	5.84E-02	9.49E-02	4.85E-03	8.24E-02	1.51E-02	3.37E-02	97.10%
M6-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	6.69E-03	1.11E-03	2.79E-03	92.70%

Structure	(as drawn)		(after process bias)									
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)		
	0.132	1.88	0.1705	1.841	5.84E-02	5.80E-02	1.51E-02	1.85E-02	1.27E-03	8.64E-03	83.90%	
M6-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	6.90E-03	1.20E-03	2.85E-03	92.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.82E-02	1.48E-02	1.95E-02	1.37E-03	9.07E-03	84.50%	
M6-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	6.99E-03	1.24E-03	2.87E-03	92.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.83E-02	1.48E-02	1.99E-02	1.42E-03	9.26E-03	84.80%	
M6-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	7.00E-03	1.25E-03	2.88E-03	92.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.83E-02	1.47E-02	2.00E-02	1.42E-03	9.29E-03	84.80%	
M6-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.03E-01	7.40E-03	1.43E-03	2.99E-03	92.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.88E-02	1.43E-02	2.19E-02	1.63E-03	1.01E-02	85.90%	
M6-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.05E-01	8.23E-03	1.84E-03	3.20E-03	93.20%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.98E-02	1.33E-02	2.59E-02	2.10E-03	1.19E-02	87.80%	
M6-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	9.61E-03	2.58E-03	3.52E-03	93.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.23E-02	1.19E-02	3.26E-02	2.94E-03	1.48E-02	90.40%	
M6-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.04E-01	1.26E-02	4.32E-03	4.16E-03	94.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.85E-02	9.28E-03	4.52E-02	4.92E-03	2.02E-02	93.10%	
M6-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.92E-02	2.75E-02	1.33E-02	7.13E-03	96.30%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.55E-02	4.99E-03	8.25E-02	1.51E-02	3.37E-02	96.90%	
M7-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.06E-01	6.67E-03	9.46E-04	2.86E-03	91.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.27E-02	1.74E-02	1.67E-02	1.08E-03	7.81E-03	82.00%	
M7-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.06E-01	6.85E-03	1.01E-03	2.92E-03	91.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.29E-02	1.72E-02	1.74E-02	1.15E-03	8.14E-03	82.50%	
M7-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.06E-01	6.93E-03	1.04E-03	2.94E-03	91.50%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.30E-02	1.72E-02	1.78E-02	1.19E-03	8.29E-03	82.70%	
M7-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.06E-01	6.94E-03	1.04E-03	2.95E-03	91.50%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.30E-02	1.72E-02	1.78E-02	1.19E-03	8.31E-03	82.70%	
M7-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.06E-01	7.25E-03	1.17E-03	3.04E-03	91.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.32E-02	1.68E-02	1.91E-02	1.33E-03	8.90E-03	83.50%	
M7-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.03E-01	7.88E-03	1.43E-03	3.23E-03	91.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.37E-02	1.61E-02	2.19E-02	1.63E-03	1.02E-02	85.00%	
M7-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.06E-01	8.82E-03	1.84E-03	3.49E-03	92.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.49E-02	1.52E-02	2.60E-02	2.10E-03	1.20E-02	86.80%	
M7-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.05E-01	1.03E-02	2.58E-03	3.85E-03	92.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.73E-02	1.37E-02	3.29E-02	2.94E-03	1.50E-02	89.40%	
M7-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.03E-01	1.34E-02	4.32E-03	4.55E-03	93.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.36E-02	1.11E-02	4.57E-02	4.92E-03	2.04E-02	92.30%	
M7-M6	0.132	0.132	0.1495	0.1145	7.21E-02	2.42E-01	1.01E-01	6.41E-03	8.42E-02	1.51E-02	3.45E-02	96.30%
	0.132	1.88	0.1705	1.841	5.84E-02	1.01E-01	6.41E-03	8.42E-02	1.51E-02	3.45E-02	96.30%	
M8-FOX	0.395	0.395	0.4695	0.3205	2.21E-02	3.12E-01	1.41E-01	8.94E-03	2.48E-03	3.23E-03	93.10%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.36E-02	3.06E-02	1.96E-02	2.52E-03	8.55E-03	86.30%	
M8-OD	0.395	0.395	0.4695	0.3205	2.21E-02	3.19E-01	1.44E-01	9.20E-03	2.62E-03	3.29E-03	93.20%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.38E-02	3.04E-02	2.05E-02	2.66E-03	8.90E-03	86.60%	
M8-PO1(OD)	0.395	0.395	0.4695	0.3205	2.21E-02	3.19E-01	1.44E-01	9.32E-03	2.69E-03	3.32E-03	93.30%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.39E-02	3.03E-02	2.08E-02	2.73E-03	9.06E-03	86.70%	
M8-PO1(FOX)	0.395	0.395	0.4695	0.3205	2.21E-02	3.19E-01	1.44E-01	9.33E-03	2.69E-03	3.32E-03	93.30%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.39E-02	3.03E-02	2.09E-02	2.73E-03	9.08E-03	86.70%	
M8-M1	0.395	0.395	0.4695	0.3205	2.21E-02	3.12E-01	1.41E-01	9.81E-03	2.95E-03	3.43E-03	93.20%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.43E-02	2.99E-02	2.24E-02	2.99E-03	9.72E-03	87.20%	
M8-M2	0.395	0.395	0.4695	0.3205	2.21E-02	3.17E-01	1.43E-01	1.07E-02	3.46E-03	3.64E-03	93.50%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.54E-02	2.92E-02	2.55E-02	3.51E-03	1.10E-02	88.10%	
M8-M3	0.395	0.395	0.4695	0.3205	2.21E-02	3.17E-01	1.43E-01	1.20E-02	4.18E-03	3.93E-03	93.80%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.68E-02	2.83E-02	2.96E-02	4.24E-03	1.27E-02	89.00%	
M8-M4	0.395	0.395	0.4695	0.3205	2.21E-02	3.17E-01	1.42E-01	1.39E-02	5.27E-03	4.34E-03	94.10%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.93E-02	2.70E-02	3.56E-02	5.35E-03	1.51E-02	90.10%	
M8-M5	0.395	0.395	0.4695	0.3205	2.21E-02	3.19E-01	1.42E-01	1.72E-02	7.14E-03	5.01E-03	94.60%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.04E-01	2.49E-02	4.51E-02	7.25E-03	1.89E-02	91.40%	
M8-M6	0.395	0.395	0.4695	0.3205	2.21E-02	3.24E-01	1.43E-01	2.38E-02	1.11E-02	6.35E-03	95.40%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.14E-01	2.17E-02	6.27E-02	1.12E-02	2.57E-02	93.00%	
M8-M7	0.395	0.395	0.4695	0.3205	2.21E-02	3.30E-01	1.37E-01	4.59E-02	2.47E-02	1.06E-02	96.60%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.46E-01	1.59E-02	1.07E-01	2.51E-02	4.12E-02	95.50%	
M9-FOX	0.395	0.395	0.4695	0.3205	2.21E-02	3.41E-01	1.54E-01	7.95E-03	2.04E-03	2.96E-03	92.90%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.82E-02	3.38E-02	1.63E-02	2.07E-03	7.12E-03	85.40%	
M9-OD	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.52E-01	8.15E-03	2.13E-03	3.01E-03	92.80%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.83E-02	3.36E-02	1.69E-02	2.17E-03	7.35E-03	85.60%	
M9-PO1(OD)	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.52E-01	8.23E-03	2.17E-03	3.03E-03	92.90%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.84E-02	3.36E-02	1.71E-02	2.21E-03	7.45E-03	85.70%	
M9-PO1(FOX)	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.52E-01	8.25E-03	2.18E-03	3.03E-03	92.90%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.84E-02	3.36E-02	1.71E-02	2.21E-03	7.46E-03	85.70%	
M9-M1	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.52E-01	8.56E-03	2.34E-03	3.11E-03	92.90%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.86E-02	3.34E-02	1.81E-02	2.38E-03	7.88E-03	86.10%	
M9-M2	0.395	0.395	0.4695	0.3205	2.21E-02	3.36E-01	1.52E-01	9.17E-03	2.65E-03	3.26E-03	93.00%	
	0.395	2.82	0.4765	2.738	1.97E-02	9.90E-02	3.29E-02	2.00E-02	2.69E-03	8.64E-03	86.70%	

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M9-M3	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.52E-01	9.96E-03	3.06E-03	3.45E-03	93.20%
	0.395	2.82	0.4765	2.738	1.97E-02	9.97E-02	3.24E-02	2.24E-02	3.10E-03	9.63E-03	87.50%
M9-M4	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.52E-01	1.10E-02	3.60E-03	3.68E-03	93.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.01E-01	3.17E-02	2.55E-02	3.66E-03	1.09E-02	88.40%
M9-M5	0.395	0.395	0.4695	0.3205	2.21E-02	3.38E-01	1.52E-01	1.23E-02	4.39E-03	3.97E-03	93.70%
	0.395	2.82	0.4765	2.738	1.97E-02	1.02E-01	3.07E-02	3.00E-02	4.46E-03	1.28E-02	89.40%
M9-M6	0.395	0.395	0.4695	0.3205	2.21E-02	3.36E-01	1.50E-01	1.44E-02	5.62E-03	4.40E-03	94.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.05E-01	2.92E-02	3.66E-02	5.70E-03	1.55E-02	90.70%
M9-M7	0.395	0.395	0.4695	0.3205	2.21E-02	3.37E-01	1.50E-01	1.80E-02	<b>7.79E-03</b>	5.10E-03	94.50%
	0.395	2.82	0.4765	2.738	1.97E-02	1.09E-01	2.67E-02	4.75E-02	7.91E-03	1.98E-02	92.20%
M9-M8	0.395	0.395	0.4695	0.3205	2.21E-02	3.47E-01	1.45E-01	4.52E-02	2.47E-02	1.02E-02	96.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.48E-01	1.76E-02	1.07E-01	2.51E-02	4.09E-02	95.70%
M10-FOX	3	2	3.178	1.822	2.10E-02	1.73E-01	7.27E-02	1.96E-02	1.17E-02	3.94E-03	95.30%
	3	8	3.178	7.822	2.10E-02	8.68E-02	2.24E-02	3.81E-02	1.17E-02	1.32E-02	95.50%
M10-OD	3	2	3.178	1.822	2.10E-02	1.73E-01	7.23E-02	2.04E-02	1.21E-02	4.13E-03	95.50%
	3	8	3.178	7.822	2.10E-02	8.74E-02	2.21E-02	3.94E-02	1.21E-02	1.36E-02	95.60%
M10-PO1(OD)	3	2	3.178	1.822	2.10E-02	1.73E-01	7.23E-02	2.07E-02	1.23E-02	4.19E-03	95.50%
	3	8	3.178	7.822	2.10E-02	8.77E-02	2.20E-02	3.99E-02	1.23E-02	1.38E-02	95.70%
M10-PO1(FOX)	3	2	3.178	1.822	2.10E-02	1.73E-01	7.23E-02	2.07E-02	1.23E-02	4.19E-03	95.60%
	3	8	3.178	7.822	2.10E-02	8.77E-02	2.20E-02	4.00E-02	1.23E-02	1.38E-02	95.70%
M10-M1	3	2	3.178	1.822	2.10E-02	1.73E-01	7.17E-02	2.19E-02	1.31E-02	4.39E-03	95.80%
	3	8	3.178	7.822	2.10E-02	8.88E-02	2.15E-02	4.21E-02	1.31E-02	1.45E-02	95.80%
M10-M2	3	2	3.178	1.822	2.10E-02	1.74E-01	7.15E-02	2.40E-02	1.45E-02	4.73E-03	96.00%
	3	8	3.178	7.822	2.10E-02	9.04E-02	2.07E-02	4.58E-02	1.45E-02	1.57E-02	96.60%
M10-M3	3	2	3.178	1.822	2.10E-02	1.75E-01	7.08E-02	2.67E-02	1.63E-02	5.21E-03	96.40%
	3	8	3.178	7.822	2.10E-02	9.31E-02	1.98E-02	5.05E-02	1.63E-02	1.71E-02	96.80%
M10-M4	3	2	3.178	1.822	2.10E-02	1.75E-01	6.98E-02	3.01E-02	1.85E-02	5.82E-03	96.70%
	3	8	3.178	7.822	2.10E-02	9.63E-02	1.86E-02	5.63E-02	1.85E-02	1.89E-02	97.00%
M10-M5	3	2	3.178	1.822	2.10E-02	1.78E-01	6.91E-02	3.45E-02	2.14E-02	6.58E-03	97.10%
	3	8	3.178	7.822	2.10E-02	1.01E-01	1.73E-02	6.35E-02	2.14E-02	2.11E-02	97.30%
M10-M6	3	2	3.178	1.822	2.10E-02	1.81E-01	6.77E-02	4.07E-02	2.53E-02	7.69E-03	97.50%
	3	8	3.178	7.822	2.10E-02	1.07E-01	1.58E-02	7.31E-02	2.53E-02	2.39E-02	97.70%
M10-M7	3	2	3.178	1.822	2.10E-02	1.85E-01	6.57E-02	4.96E-02	3.11E-02	9.20E-03	97.80%
	3	8	3.178	7.822	2.10E-02	1.16E-01	1.39E-02	8.61E-02	3.11E-02	2.75E-02	98.00%
M10-M8	3	2	3.178	1.822	2.10E-02	2.04E-01	5.98E-02	8.12E-02	5.23E-02	1.45E-02	98.20%
	3	8	3.178	7.822	2.10E-02	1.50E-01	9.83E-03	1.28E-01	5.23E-02	3.81E-02	98.70%
M10-M9	3	2	3.178	1.822	2.10E-02	3.31E-01	4.68E-02	2.33E-01	1.62E-01	3.55E-02	98.90%
	3	8	3.178	7.822	2.10E-02	3.01E-01	5.15E-03	2.89E-01	1.62E-01	6.31E-02	99.40%

## (b) Structure B at 25 °C

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M1-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.72E-01	5.77E-02	2.03E-02	6.07E-03	7.10E-03	3.24E-02	3.63E-03	1.44E-02	97.40%
	0.094	1.8471	0.065	1.876	1.14E+01	1.19E-01	1.20E-02	4.70E-02	6.07E-03	2.05E-02	7.14E-02	3.63E-03	3.39E-02	100.00%
M2-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.26E-02	2.15E-02	6.07E-03	7.71E-03	9.16E-03	2.46E-03	3.35E-03	93.90%
	0.094	1.8471	0.065	1.876	1.14E+01	9.33E-02	8.30E-04	6.35E-02	6.07E-03	2.87E-02	2.82E-02	2.46E-03	1.29E-02	100.00%
M2-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.60E-01	1.10E-01	1.12E-02	6.14E-03	2.55E-03	2.06E-02	1.16E-02	4.50E-03	96.60%
	0.113	1.88	0.1736	1.819	7.60E-02	1.13E-01	9.80E-04	4.07E-02	8.13E-03	1.63E-02	7.00E-02	1.54E-02	2.73E-02	100.00%
M2-M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.62E-01	1.08E-01	2.01E-02	1.17E-02	4.19E-03	2.00E-02	1.16E-02	4.21E-03	97.80%
	0.113	1.88	0.1736	1.819	7.60E-02	1.26E-01	3.62E-04	6.30E-02	1.56E-02	2.37E-02	6.24E-02	1.54E-02	2.35E-02	100.00%
M2-M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.66E-01	1.06E-01	3.07E-02	1.84E-02	6.17E-03	1.99E-02	1.16E-02	4.16E-03	98.60%
	0.113	1.88	0.1736	1.819	7.60E-02	1.42E-01	1.47E-04	8.37E-02	2.44E-02	2.97E-02	5.81E-02	1.54E-02	2.14E-02	100.00%
M2-M1-PO1(FOX)	0.113	0.113	0.131	0.095	1.00E-01	2.66E-01	1.05E-01	3.31E-02	1.99E-02	6.61E-03	1.99E-02	1.16E-02	4.16E-03	98.70%
	0.113	1.88	0.1736	1.819	7.60E-02	1.45E-01	2.11E-04	8.77E-02	2.63E-02	3.07E-02	5.73E-02	1.54E-02	2.09E-02	100.00%
M3-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.31E-02	2.26E-02	6.07E-03	8.26E-03	5.23E-03	1.31E-03	1.96E-03	93.00%
	0.094	1.8471	0.065	1.876	1.14E+01	8.94E-02	1.71E-03	6.91E-02	6.07E-03	3.15E-02	1.68E-02	1.31E-03	7.74E-03	99.90%
M3-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.55E-01	1.12E-01	1.19E-02	6.14E-03	2.87E-03	7.43E-03	3.78E-03	1.82E-03	95.00%
	0.113	1.88	0.1736	1.819	7.60E-02	8.76E-02	3.03E-03	4.95E-02	8.13E-03	2.07E-02	3.19E-02	5.01E-03	1.35E-02	99.90%
M3-M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.59E-01	1.11E-01	2.08E-02	1.17E-02	4.53E-03	7.04E-03	3.78E-03	1.63E-03	96.30%
	0.113	1.88	0.1736	1.819	7.60E-02	1.05E-01	1.39E-03	7.42E-02	1.56E-02	2.93E-02	2.76E-02	5.01E-03	1.13E-02	100.00%
M3-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.85E-02	7.07E-03	3.63E-03	1.72E-03	2.42E-02	1.33E-02	5.49E-03	97.10%
	0.132	1.88	0.1705	1.841	5.84E-02	1.03E-01	1.89E-03	2.44E-02	4.14E-03	1.01E-02	7.51E-02	1.51E-02	3.00E-02	99.90%
M3-M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	1.00E-01	8.98E-03	4.82E-03	2.08E-03	2.38E-02	1.33E-02	5.26E-03	97.50%
	0.132	1.88	0.1705	1.841	5.84E-02	1.06E-01	1.26E-03	3.04E-02	5.50E-03	1.24E-02	7.29E-02	1.51E-02	2.89E-02	100.00%
M3-M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.62E-01	1.08E-01	3.16E-02	1.84E-02	6.59E-03	6.97E-03	3.78E-03	1.60E-03	97.10%
	0.113	1.88	0.1736	1.819	7.60E-02	1.22E-01	8.75E-04	9.56E-02	2.44E-02	3.56E-02	2.49E-02	5.01E-03	9.96E-03	100.00%
M3-M1-PO1(FOX)	0.113	0.113	0.131	0.095	1.00E-01	2.63E-01	1.08E-01	3.40E-02	1.99E-02	7.04E-03	6.96E-03	3.78E-03	1.59E-03	97.30%
	0.113	1.88	0.1736	1.819	7.60E-02	1.26E-01	8.16E-04	9.97E-02	2.63E-02	3.67E-02	2.45E-02	5.01E-03	9.74E-03	100.00%
M3-M2-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.87E-02	1.02E-02	5.54E-03	2.32E-03	2.36E-02	1.33E-02	5.19E-03	97.70%
	0.132	1.88	0.1705	1.841	5.84E-02	1.08E-01	1.02E-03	3.37E-02	6.32E-03	1.37E-02	7.18E-02	1.51E-02	2.84E-02	100.00%
M3-M2-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.86E-02	1.04E-02	5.66E-03	2.35E-03	2.36E-02	1.33E-02	5.18E-03	97.70%
	0.132	1.88	0.1705	1.841	5.84E-02	1.08E-01	9.92E-04	3.42E-02	6.45E-03	1.38E-02	7.17E-02	1.51E-02	2.83E-02	100.00%
M3-M2-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.42E-01	9.70E-02	2.26E-02	1.33E-02	4.67E-03	2.32E-02	1.33E-02	4.96E-03	99.00%
	0.132	1.88	0.1705	1.841	5.84E-02	1.25E-01	2.70E-04	5.99E-02	1.51E-02	2.24E-02	4.67E-02	1.51E-02	2.48E-02	100.00%
M4-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.33E-02	2.33E-02	6.07E-03	8.63E-03	3.72E-03	8.89E-04	1.42E-03	92.80%
	0.094	1.8471	0.065	1.876	1.14E+01	8.83E-02	2.25E-03	7.15E-02	6.07E-03	3.27E-02	1.20E-02	8.89E-04	5.54E-03	99.70%
M4-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.54E-01	1.12E-01	1.25E-02	6.14E-03	3.20E-03	4.82E-03	2.26E-03	1.28E-03	94.50%
	0.113	1.88	0.1736	1.819	7.60E-02	8.29E-02	4.52E-03	5.26E-02	8.13E-03	2.22E-02	2.09E-02	2.99E-03	8.98E-03	99.60%
M4-M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.58E-01	1.11E-01	2.16E-02	1.17E-02	4.96E-03	4.53E-03	2.26E-03	1.13E-03	95.90%
	0.113	1.88	0.1736	1.819	7.60E-02	1.01E-01	2.40E-03	7.80E-02	1.56E-02	3.12E-02	1.79E-02	2.99E-03	7.46E-03	99.80%
M4-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	7.49E-03	3.63E-03	1.93E-03	8.75E-03	4.32E-03	2.22E-03	95.30%
	0.132	1.88	0.1705	1.841	5.84E-02	7.57E-02	4.78E-03	2.99E-02	4.14E-03	1.29E-02	3.59E-02	4.92E-03	1.55E-02	99.70%
M4-M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	9.42E-03	4.82E-03	2.30E-03	8.45E-03	4.32E-03	2.07E-03	95.70%
	0.132	1.88	0.1705	1.841	5.84E-02	7.90E-02	3.70E-03	3.69E-02	5.50E-03	1.57E-02	3.46E-02	4.92E-03	1.48E-02	99.80%
M4-M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.98E-02	4.75E-03	2.32E-03	1.22E-03	2.48E-02	1.33E-02	5.77E-03	96.80%
	0.132	1.88	0.1705	1.841	5.84E-02	1.00E-01	2.71E-03	1.68E-02	2.64E-03	7.10E-03	7.78E-02	1.51E-02	3.13E-02	99.70%
M4-M3-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.99E-02	5.49E-03	2.75E-03	1.37E-03	2.45E-02	1.33E-02	5.60E-03	96.90%
	0.132	1.88	0.1705	1.841	5.84E-02	1.01E-01	2.33E-03	1.95E-02	3.14E-03	8.16E-03	7.68E-02	1.51E-02	3.09E-02	99.80%
M4-M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.61E-01	1.08E-01	3.24E-02	1.84E-02	7.03E-03	4.42E-03	2.26E-03	1.08E-03	96.80%
	0.113	1.88	0.1736	1.819	7.60E-02	1.19E-01	1.66E-03	9.96E-02	2.44E-02	3.76E-02	1.61E-02	2.99E-03	6.53E-03	99.90%
M4-M1-PO1(FOX)	0.113	0.113	0.131	0.095	1.00E-01	2.64E-01	1.08E-01	3.48E-02	1.99E-02	7.47E-03	4.40E-03	2.26E-03	1.07E-03	96.90%
	0.113	1.88	0.1736	1.819	7.60E-02	1.23E-01	1.56E-03	1.04E-01	2.63E-02	3.88E-02	1.58E-02	2.99E-03	6.39E-03	99.90%
M4-M2-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.02E-01	1.06E-02	5.54E-03	2.52E-03	3.85E-03	4.32E-03	2.02E-03	95.90%
	0.132	1.88	0.1705	1.841	5.84E-02	8.12E-02	3.25E-03	4.07E-02	6.32E-03	1.72E-02	3.39E-02	4.92E-03	1.45E-02	99.90%
M4-M2-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.02E-01	1.08E-02	5.66E-03	2.56E-03	3.87E-03	4.32E-03	2.03E-03	96.00%
	0.132	1.88	0.1705	1.841	5.84E-02	8.15E-02	3.20E-03	4.13E-02	6.45E-03	1.74E-02	3.38E-02	4.92E-03	1.44E-02	99.90%
M4-M3-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.88E-02	5.91E-03	2.97E-03	1.47E-03	2.44E-02	1.33E-02	5.59E-03	97.00%
	0.132	1.88	0.1705	1.841	5.84E-02	1.02E-01	2.15E-03	2.08E-02	3.39E-03	8.69E-03	7.64E-02	1.51E-02	3.06E-02	99.90%
M4-M3-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.86E-02	5.96E-03	3.00E-03	1.48E-03	2			

Structure	(as drawn)		(after process bias)										Csum/ Ctotal		
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft		
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)									
M5-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	7.98E-03	3.63E-03	2.17E-03	5.76E-03	2.58E-03	1.59E-03	94.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.99E-02	6.72E-03	3.19E-02	4.14E-03	1.39E-02	2.39E-02	2.94E-03	1.05E-02	99.20%	
M5-M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.03E-01	9.96E-03	4.82E-03	2.57E-03	5.51E-03	2.58E-03	1.47E-03	95.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.36E-02	5.51E-03	3.93E-02	5.50E-03	1.69E-02	2.30E-02	2.94E-03	1.00E-02	99.50%	
M5-M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	5.17E-03	2.32E-03	1.43E-03	9.22E-03	4.32E-03	2.45E-03	95.00%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.15E-02	6.13E-03	2.09E-02	2.64E-03	9.13E-03	3.77E-02	4.92E-03	1.64E-02	99.20%	
M5-M3-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.02E-01	5.95E-03	2.75E-03	1.60E-03	9.03E-03	4.32E-03	2.35E-03	95.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.25E-02	5.54E-03	2.40E-02	3.14E-03	1.04E-02	3.70E-02	4.92E-03	1.60E-02	99.50%	
M5-M4-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.92E-02	3.64E-03	1.70E-03	9.68E-04	2.53E-02	1.33E-02	6.02E-03	96.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.92E-02	3.27E-03	1.29E-02	1.94E-03	5.47E-03	7.93E-02	1.51E-02	3.21E-02	99.50%	
M5-M4-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.92E-02	4.05E-03	1.92E-03	1.06E-03	2.51E-02	1.33E-02	5.91E-03	96.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.96E-02	3.06E-03	1.43E-02	2.19E-03	6.08E-03	7.87E-02	1.51E-02	3.18E-02	99.60%	
M5-M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.61E-01	1.08E-01	3.30E-02	1.84E-02	7.31E-03	3.26E-03	1.61E-03	8.27E-04	96.60%	
	0.113	1.88	0.1736	1.819	7.60E-02	1.18E-01	2.17E-03	1.02E-01	2.44E-02	3.86E-02	1.19E-02	2.13E-03	4.86E-03	99.70%	
M5-M1-PO1(FOX)	0.113	0.113	0.131	0.095	1.00E-01	2.62E-01	1.07E-01	3.55E-02	1.99E-02	7.79E-03	3.26E-03	1.61E-03	8.22E-04	96.70%	
	0.113	1.88	0.1736	1.819	7.60E-02	1.22E-01	2.06E-03	1.06E-01	2.63E-02	3.97E-02	1.16E-02	2.13E-03	4.76E-03	99.80%	
M5-M2-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	1.12E-02	5.54E-03	2.82E-03	5.45E-03	2.58E-03	1.44E-03	95.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.60E-02	4.95E-03	4.33E-02	6.32E-03	1.85E-02	2.25E-02	2.94E-03	9.76E-03	99.60%	
M5-M2-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	1.14E-02	5.66E-03	2.85E-03	5.44E-03	2.58E-03	1.43E-03	95.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.63E-02	4.88E-03	4.39E-02	6.45E-03	1.87E-02	2.24E-02	2.94E-03	9.72E-03	99.60%	
M5-M3-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	6.33E-03	2.97E-03	1.68E-03	8.93E-03	4.32E-03	2.31E-03	95.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.31E-02	5.26E-03	2.56E-02	3.39E-03	1.11E-02	3.67E-02	4.92E-03	1.59E-02	99.60%	
M5-M3-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.02E-01	6.36E-03	3.00E-03	1.68E-03	8.88E-03	4.32E-03	2.28E-03	95.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.32E-02	5.23E-03	2.58E-02	3.43E-03	1.12E-02	3.67E-02	4.92E-03	1.59E-02	99.60%	
M5-M4-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.97E-02	4.23E-03	2.03E-03	1.10E-03	2.49E-02	1.33E-02	5.84E-03	96.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.97E-02	2.96E-03	1.50E-02	2.31E-03	6.36E-03	7.84E-02	1.51E-02	3.17E-02	99.60%	
M5-M4-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.97E-02	4.25E-03	2.04E-03	1.10E-03	2.49E-02	1.33E-02	5.84E-03	96.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.98E-02	2.94E-03	1.51E-02	2.33E-03	6.40E-03	7.84E-02	1.51E-02	3.16E-02	99.70%	
M5-M2-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.00E-01	2.38E-02	1.33E-02	5.28E-03	5.11E-03	2.58E-03	1.26E-03	96.90%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.76E-02	2.64E-03	7.30E-02	1.51E-02	2.89E-02	1.92E-02	2.94E-03	8.12E-03	99.80%	
M5-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	8.51E-03	4.32E-03	2.10E-03	8.49E-03	4.32E-03	2.09E-03	95.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.73E-02	3.98E-03	3.41E-02	4.92E-03	1.46E-02	3.51E-02	4.92E-03	1.51E-02	99.80%	
M5-M4-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.98E-02	5.20E-03	2.58E-03	1.31E-03	2.46E-02	1.33E-02	5.66E-03	96.90%	
	0.132	1.88	0.1705	1.841	5.84E-02	1.01E-01	2.46E-03	1.84E-02	2.94E-03	7.75E-03	7.72E-02	1.51E-02	3.10E-02	99.80%	
M5-M3-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.99E-02	2.32E-02	1.33E-02	4.95E-03	8.05E-03	4.32E-03	1.87E-03	97.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	1.02E-01	1.48E-03	6.94E-02	1.51E-02	2.72E-02	2.92E-02	4.92E-03	1.21E-02	100.00%	
M5-M4-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.90E-02	8.13E-03	4.32E-03	1.91E-03	2.39E-02	1.33E-02	5.31E-03	97.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	1.04E-01	1.39E-03	2.79E-02	4.92E-03	1.15E-02	7.38E-02	1.51E-02	2.93E-02	100.00%	
M5-M4-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.44E-01	9.77E-02	2.26E-02	1.33E-02	4.67E-03	4.72E-03	2.32E-02	1.33E-02	4.96E-03	99.00%
	0.132	1.88	0.1705	1.841	5.84E-02	1.25E-01	2.69E-04	5.98E-02	1.51E-02	2.24E-02	6.47E-02	1.51E-02	2.48E-02	100.00%	
M6-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.34E-02	2.41E-02	6.07E-03	9.03E-03	2.37E-03	5.42E-04	9.16E-04	92.60%	
	0.094	1.8471	0.065	1.876	1.14E+01	8.76E-02	2.80E-03	7.37E-02	6.07E-03	3.38E-02	7.60E-03	5.42E-04	3.53E-03	99.30%	
M6-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.55E-01	1.12E-01	1.34E-02	6.14E-03	3.62E-03	2.93E-03	1.25E-03	8.40E-04	94.30%	
	0.113	1.88	0.1736	1.819	7.60E-02	8.03E-02	5.95E-03	5.50E-02	8.13E-03	2.34E-02	1.24E-02	1.66E-03	5.39E-03	98.80%	
M6-M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.54E-01	1.09E-01	2.23E-02	1.17E-02	5.28E-03	2.65E-03	1.25E-03	6.97E-04	95.50%	
	0.113	1.88	0.1736	1.819	7.60E-02	9.90E-02	3.45E-03	8.09E-02	1.56E-02	3.27E-02	1.06E-02	1.66E-03	4.45E-03	99.40%	
M6-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.04E-01	8.45E-03	3.63E-03	2.41E-03	4.43E-03	1.84E-03	1.29E-03	94.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.78E-02	7.88E-03	3.30E-02	4.14E-03	1.44E-02	1.80E-02	2.10E-03	7.94E-03	98.50%	
M6-M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	6.32E-03	2.75E-03	1.79E-03	5.92E-03	2.58E-03	1.67E-03	94.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.66E-02	7.67E-03	2.58E-02	3.14E-03	1.13E-02	2.48E-02	2.94E-03	1.09E-02	98.90%	
M6-M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.03E-01	4.03E-03	1.70E-03	1.16E-03	9.61E-03	4.32E-03	2.65E-03	94.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.98E-02	7.01E-03	1.61E-02	1.94E-03	7.08E-03	3.87E-02	4.92E-03	1.69E-02	98.60%	
M6-M4-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	4.44E-03	1.92E-03	1.26E-03	9.43E-03	4.32E-03	2.56E-03	94.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.03E-02	6.68E-03	1.79E-02	2.19E-03	7.84E-03	3.83E-02	4.92E-03	1.67E-02	98.90%	
M6-M5-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.92E-02	2.95E-03	1.34E-03	8.02E-04	2.56E-02	1.33E-02	6.17E-03	96.50%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.88E-02	3.65E-03	1.04E-02	1.53E-03	4.46E-03	8.03E-02	1.51E-02	3.26E-02	99.20%	
M6-M5-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.98E-02	3.20E-03	1.48E-03	8.60E-04	2.54E-02	1.33E-			

Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M6-M4-PO1(OD)	0.132	1.88	0.1705	1.841	5.84E-02	6.75E-02	7.31E-03	2.77E-02	3.43E-03	1.21E-02	2.45E-02	2.94E-03	1.08E-02	99.10%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	4.64E-03	2.03E-03	1.31E-03	9.36E-03	4.32E-03	2.52E-03	94.80%
	0.132	1.88	0.1705	1.841	5.84E-02	7.06E-02	6.52E-03	1.87E-02	2.31E-03	8.20E-03	3.82E-02	4.92E-03	1.66E-02	99.10%
M6-M4-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	4.67E-03	2.04E-03	1.31E-03	9.35E-03	4.32E-03	2.52E-03	94.80%
M6-M5-PO1(OD)	0.132	1.88	0.1705	1.841	5.84E-02	7.06E-02	6.50E-03	1.88E-02	2.33E-03	8.25E-03	3.81E-02	4.92E-03	1.66E-02	99.10%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.90E-02	3.33E-03	1.54E-03	8.93E-04	2.54E-02	1.33E-02	6.06E-03	96.60%
	0.132	1.88	0.1705	1.841	5.84E-02	9.90E-02	3.44E-03	1.18E-02	1.76E-03	5.02E-03	7.97E-02	1.51E-02	3.23E-02	99.40%
M6-M5-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.90E-02	3.34E-03	1.55E-03	8.97E-04	2.54E-02	1.33E-02	6.06E-03	96.60%
M6-M2-M1	0.132	1.88	0.1705	1.841	5.84E-02	9.90E-02	3.43E-03	1.19E-02	1.77E-03	5.05E-03	7.97E-02	1.51E-02	3.23E-02	99.40%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	9.88E-02	2.44E-02	1.33E-02	5.57E-03	3.82E-03	1.84E-03	9.91E-04	96.60%
	0.132	1.88	0.1705	1.841	5.84E-02	9.61E-02	3.38E-03	7.46E-02	1.51E-02	2.98E-02	1.42E-02	2.10E-03	6.08E-03	99.50%
M6-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.08E-03	4.32E-03	2.38E-03	5.59E-03	2.58E-03	1.51E-03	95.00%
M6-M4-M1	0.132	1.88	0.1705	1.841	5.84E-02	7.17E-02	5.85E-03	3.62E-02	4.92E-03	1.57E-02	2.33E-02	2.94E-03	1.02E-02	99.40%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.02E-01	5.63E-03	2.58E-03	1.52E-03	9.07E-03	4.32E-03	2.38E-03	95.00%
	0.132	1.88	0.1705	1.841	5.84E-02	7.21E-02	5.76E-03	2.28E-02	2.94E-03	9.94E-03	3.73E-02	4.92E-03	1.62E-02	99.40%
M6-M5-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.91E-02	3.89E-03	1.84E-03	1.03E-03	2.51E-02	1.33E-02	5.94E-03	96.70%
M6-M3-M2	0.132	1.88	0.1705	1.841	5.84E-02	9.94E-02	3.15E-03	1.38E-02	2.10E-03	5.84E-03	7.89E-02	1.51E-02	3.19E-02	99.60%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.00E-01	2.38E-02	1.33E-02	5.27E-03	5.11E-03	2.58E-03	1.26E-03	96.90%
	0.132	1.88	0.1705	1.841	5.84E-02	9.75E-02	2.63E-03	7.29E-02	1.51E-02	2.89E-02	1.92E-02	2.94E-03	8.11E-03	99.80%
M6-M4-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	8.51E-03	4.32E-03	2.10E-03	8.49E-03	4.32E-03	2.09E-03	95.60%
M6-M5-M2	0.132	1.88	0.1705	1.841	5.84E-02	7.73E-02	3.98E-03	3.41E-02	4.92E-03	1.46E-02	3.51E-02	4.92E-03	1.51E-02	99.80%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.99E-02	5.19E-03	2.58E-03	1.31E-03	2.45E-02	1.33E-02	5.65E-03	96.90%
	0.132	1.88	0.1705	1.841	5.84E-02	1.01E-01	2.46E-03	1.84E-02	2.94E-03	7.75E-03	7.72E-02	1.51E-02	3.10E-02	99.80%
M6-M4-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.99E-02	2.32E-02	1.33E-02	4.95E-03	8.05E-03	4.32E-03	1.87E-03	97.40%
M6-M5-M3	0.132	1.88	0.1705	1.841	5.84E-02	1.02E-01	1.48E-03	6.94E-02	1.51E-02	2.72E-02	2.92E-02	4.92E-03	1.21E-02	100.00%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.90E-02	8.13E-03	4.32E-03	1.91E-03	2.39E-02	1.33E-02	5.31E-03	97.40%
	0.132	1.88	0.1705	1.841	5.84E-02	1.04E-01	1.39E-03	2.79E-02	4.92E-03	1.15E-02	7.38E-02	1.51E-02	2.93E-02	100.00%
M6-M5-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.44E-01	9.77E-02	2.26E-02	1.33E-02	4.67E-03	2.32E-02	1.33E-02	4.96E-03	99.00%
M7-PO1-FOX	0.132	1.88	0.1705	1.841	5.84E-02	1.25E-01	2.69E-04	5.98E-02	1.51E-02	2.24E-02	6.47E-02	1.51E-02	2.48E-02	100.00%
	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.35E-02	2.44E-02	6.07E-03	9.16E-03	2.01E-03	4.54E-04	7.80E-04	92.50%
	0.094	1.8471	0.065	1.876	1.14E+01	8.75E-02	2.95E-03	7.44E-02	6.07E-03	3.42E-02	6.43E-03	4.54E-04	2.99E-03	99.10%
M7-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.54E-01	1.12E-01	1.37E-02	6.14E-03	3.78E-03	2.47E-03	1.02E-03	7.25E-04	94.20%
M7-M1-OD	0.113	1.88	0.1736	1.819	7.60E-02	7.99E-02	6.29E-03	5.57E-02	8.13E-03	2.38E-02	1.03E-02	1.36E-03	4.50E-03	98.40%
	0.113	0.113	0.131	0.095	1.00E-01	2.57E-01	1.10E-01	2.28E-02	1.17E-02	5.52E-03	2.24E-03	1.02E-03	6.07E-04	95.60%
	0.113	1.88	0.1736	1.819	7.60E-02	9.87E-02	3.71E-03	8.17E-02	1.56E-02	3.31E-02	8.75E-03	1.36E-03	3.70E-03	99.10%
M7-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.04E-01	8.79E-03	3.63E-03	2.58E-03	3.62E-03	1.43E-03	1.10E-03	94.40%
M7-M2-OD	0.132	1.88	0.1705	1.841	5.84E-02	6.67E-02	8.58E-03	3.37E-02	4.14E-02	1.48E-02	1.44E-02	1.63E-03	6.38E-03	97.70%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.03E-01	1.08E-02	4.82E-03	2.98E-03	3.42E-03	1.43E-03	9.94E-04	94.80%
	0.132	1.88	0.1705	1.841	5.84E-02	7.07E-02	7.20E-03	4.13E-02	5.50E-03	1.79E-02	1.38E-02	1.63E-03	6.08E-03	98.30%
M7-M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	5.99E-03	2.32E-03	1.84E-03	4.78E-03	1.84E-03	1.47E-03	94.10%
M7-M3-OD	0.132	1.88	0.1705	1.841	5.84E-02	6.30E-02	9.64E-03	2.32E-02	2.64E-03	1.03E-02	1.90E-02	2.10E-03	8.45E-03	97.60%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	6.78E-03	2.75E-03	2.01E-03	4.61E-03	1.84E-03	1.39E-03	94.20%
	0.132	1.88	0.1705	1.841	5.84E-02	6.43E-02	8.90E-03	2.67E-02	3.14E-03	1.18E-02	1.86E-02	2.10E-03	8.26E-03	98.10%
M7-M4-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	4.44E-03	1.70E-03	1.37E-03	6.52E-03	2.58E-03	1.97E-03	94.10%
M7-M4-OD	0.132	1.88	0.1705	1.841	5.84E-02	6.34E-02	9.36E-03	1.73E-02	1.94E-03	7.68E-03	2.60E-02	2.94E-03	1.15E-02	97.70%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	4.87E-03	1.92E-03	1.47E-03	6.37E-03	2.58E-03	1.90E-03	94.20%
	0.132	1.88	0.1705	1.841	5.84E-02	6.41E-02	8.97E-03	1.92E-02	2.19E-03	8.51E-03	2.57E-02	2.94E-03	1.14E-02	98.10%
M7-M5-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.02E-01	3.29E-03	1.34E-03	9.72E-04	9.81E-03	4.32E-03	2.75E-03	94.60%
M7-M5-OD	0.132	1.88	0.1705	1.841	5.84E-02	6.90E-02	7.58E-03	1.31E-02	1.53E-03	5.79E-03	3.94E-02	4.92E-03	1.72E-02	98.00%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.02E-01	3.56E-03	1.48E-03	1.04E-03	9.69E-03	4.32E-03	2.69E-03	94.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.94E-02	7.37E-03	1.43E-02	1.69E-03	6.31E-03	3.92E-02	4.92E-03	1.71E-02	98.30%
M7-M6-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.93E-02	2.49E-03	1.11E-03	6.89E-04	2.59E-02	1.33E-02	6.31E-03	96.50%
M7-M6-OD	0.132	1.88	0.1705	1.841	5.84E-02	9.85E-02	3.89E-03	8.78E-03	1.27E-03	3.76E-03	8.10E-02	1.51E-02	3.29E-02	99.00%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.95E-02	2.68E-03	1.20E-03	7.41E-04	2.58E-02	1.33E-02	6.29E-03	96.50%
	0.132	1.88	0.1705	1.841	5.84E-02	9.86E-02	3.80E-03	9.44E-03	1.37E-03	4.04E-03	8.07E-02	1.51E-02	3.28E-02	99.10%
M7-M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.61E-01	1.08E-01							

Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	
	(um)	(um)	(um)	(um)	(Ohm□)	(fF/um)								
PO1(FOX)														
M7-M6-PO1(OD)	0.132	1.88	0.1705	1.841	5.84E-02	6.95E-02	7.26E-03	1.49E-02	1.77E-03	6.56E-03	3.91E-02	4.92E-03	1.71E-02	98.50%
	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.96E-02	2.76E-03	1.24E-03	7.60E-04	2.58E-02	1.33E-02	6.26E-03	96.60%
	0.132	1.88	0.1705	1.841	5.84E-02	9.87E-02	3.76E-03	9.73E-03	1.42E-03	4.16E-03	8.06E-02	1.51E-02	3.27E-02	99.20%
M7-M6-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.96E-02	2.77E-03	1.25E-03	7.63E-04	2.58E-02	1.33E-02	6.26E-03	96.60%
	0.132	1.88	0.1705	1.841	5.84E-02	9.87E-02	3.75E-03	9.77E-03	1.42E-03	4.17E-03	8.06E-02	1.51E-02	3.27E-02	99.20%
M7-M2-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.00E-01	2.48E-02	1.33E-02	5.77E-03	3.06E-03	1.43E-03	8.18E-04	96.60%
	0.132	1.88	0.1705	1.841	5.84E-02	9.54E-02	3.82E-03	7.57E-02	1.51E-02	3.03E-02	1.14E-02	1.63E-03	4.87E-03	99.30%
M7-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.47E-03	4.32E-03	2.58E-03	4.24E-03	1.84E-03	1.20E-03	94.80%
	0.132	1.88	0.1705	1.841	5.84E-02	6.96E-02	6.95E-03	3.74E-02	4.92E-03	1.62E-02	1.75E-02	2.10E-03	7.70E-03	98.80%
M7-M4-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	6.07E-03	2.58E-03	1.75E-03	6.04E-03	2.58E-03	1.73E-03	94.40%
	0.132	1.88	0.1705	1.841	5.84E-02	6.61E-02	7.92E-03	2.45E-02	2.94E-03	1.08E-02	2.50E-02	2.94E-03	1.10E-02	98.80%
M7-M5-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	4.29E-03	1.84E-03	1.22E-03	9.49E-03	4.32E-03	2.59E-03	94.70%
	0.132	1.88	0.1705	1.841	5.84E-02	7.01E-02	6.82E-03	1.72E-02	2.10E-03	7.54E-03	3.84E-02	4.92E-03	1.68E-02	98.80%
M7-M6-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.97E-02	3.10E-03	1.43E-03	8.37E-04	2.55E-02	1.33E-02	6.11E-03	96.50%
	0.132	1.88	0.1705	1.841	5.84E-02	9.89E-02	3.56E-03	1.10E-02	1.63E-03	4.71E-03	8.01E-02	1.51E-02	3.25E-02	99.30%
M7-M3-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	9.92E-02	2.44E-02	1.33E-02	5.56E-03	3.82E-03	1.84E-03	9.90E-04	96.70%
	0.132	1.88	0.1705	1.841	5.84E-02	9.61E-02	3.38E-03	7.46E-02	1.51E-02	2.98E-02	1.42E-02	2.10E-03	6.07E-03	99.50%
M7-M4-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.04E-03	4.32E-03	2.36E-03	5.56E-03	2.58E-03	1.49E-03	95.00%
	0.132	1.88	0.1705	1.841	5.84E-02	7.17E-02	5.85E-03	3.62E-02	4.92E-03	1.57E-02	2.33E-02	2.94E-03	1.02E-02	99.40%
M7-M5-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	5.64E-03	2.58E-03	1.53E-03	9.08E-03	4.32E-03	2.38E-03	95.00%
	0.132	1.88	0.1705	1.841	5.84E-02	7.21E-02	5.75E-03	2.28E-02	2.94E-03	9.95E-03	3.73E-02	4.92E-03	1.62E-02	99.40%
M7-M6-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.97E-02	3.88E-03	1.84E-03	1.02E-03	2.51E-02	1.33E-02	5.92E-03	96.70%
	0.132	1.88	0.1705	1.841	5.84E-02	9.94E-02	3.15E-03	1.38E-02	2.10E-03	5.84E-03	7.89E-02	1.51E-02	3.19E-02	99.60%
M7-M4-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.00E-01	2.38E-02	1.33E-02	5.27E-03	5.11E-03	2.58E-03	1.26E-03	96.90%
	0.132	1.88	0.1705	1.841	5.84E-02	9.75E-02	2.63E-03	7.29E-02	1.51E-02	2.89E-02	1.92E-02	2.94E-03	8.11E-03	99.80%
M7-M5-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	8.51E-03	4.32E-03	2.10E-03	8.49E-03	4.32E-03	2.09E-03	95.60%
	0.132	1.88	0.1705	1.841	5.84E-02	7.73E-02	3.98E-03	3.41E-02	4.92E-03	1.46E-02	3.51E-02	4.92E-03	1.51E-02	99.80%
M7-M6-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.99E-02	5.19E-03	2.58E-03	1.31E-03	2.45E-02	1.33E-02	5.65E-03	96.90%
	0.132	1.88	0.1705	1.841	5.84E-02	1.01E-01	2.46E-03	1.84E-02	2.94E-03	7.75E-03	7.72E-02	1.51E-02	3.10E-02	99.80%
M7-M5-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	9.99E-02	2.32E-02	1.33E-02	4.95E-03	8.05E-03	4.32E-03	1.87E-03	97.40%
	0.132	1.88	0.1705	1.841	5.84E-02	1.02E-01	1.48E-03	6.94E-02	1.51E-02	2.72E-02	2.92E-02	4.92E-03	1.21E-02	100.00%
M7-M6-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.90E-02	8.13E-03	4.32E-03	1.91E-03	2.39E-02	1.33E-02	5.31E-03	97.40%
	0.132	1.88	0.1705	1.841	5.84E-02	1.04E-01	1.39E-03	2.79E-02	4.92E-03	1.15E-02	7.38E-02	1.51E-02	2.93E-02	100.00%
M7-M6-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.44E-01	9.77E-02	2.26E-02	1.33E-02	4.67E-03	3.22E-02	1.33E-02	4.96E-03	99.00%
	0.132	1.88	0.1705	1.841	5.84E-02	1.25E-01	2.69E-04	5.98E-02	1.51E-02	2.24E-02	6.47E-02	1.51E-02	2.48E-02	100.00%
M8-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.36E-02	2.46E-02	6.07E-03	9.29E-03	1.68E-03	3.73E-04	6.53E-04	92.40%
	0.094	1.8471	0.065	1.876	1.14E+01	8.75E-02	3.09E-03	7.50E-02	6.07E-03	3.45E-02	5.34E-03	3.73E-04	2.48E-03	98.90%
M8-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.54E-01	1.11E-01	1.37E-02	6.14E-03	3.79E-03	2.00E-03	8.23E-04	5.87E-04	94.10%
	0.113	1.88	0.1736	1.819	7.60E-02	7.97E-02	6.60E-03	5.64E-02	8.13E-03	2.41E-02	8.46E-03	1.09E-03	3.68E-03	98.00%
M8-M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.56E-01	1.10E-01	2.31E-02	1.17E-02	5.67E-03	1.84E-03	8.23E-04	5.07E-04	95.60%
	0.113	1.88	0.1736	1.819	7.60E-02	9.85E-02	3.93E-03	8.24E-02	1.56E-02	3.34E-02	7.14E-03	1.09E-03	3.02E-03	98.90%
M8-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	9.14E-03	3.63E-03	2.76E-03	2.94E-03	1.10E-03	9.18E-04	94.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.62E-02	9.17E-03	3.44E-02	4.14E-03	1.51E-02	1.14E-02	1.26E-03	5.09E-03	96.90%
M8-M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	1.11E-02	4.82E-03	3.16E-03	2.75E-03	1.10E-03	8.26E-04	94.70%
	0.132	1.88	0.1705	1.841	5.84E-02	7.02E-02	7.73E-03	4.21E-02	5.50E-03	1.83E-02	1.09E-02	1.26E-03	4.83E-03	97.60%
M8-M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	6.30E-03	2.32E-03	1.99E-03	3.69E-03	1.33E-03	1.18E-03	93.80%
	0.132	1.88	0.1705	1.841	5.84E-02	6.17E-02	1.06E-02	2.39E-02	2.64E-03	1.96E-02	1.44E-02	1.52E-03	6.42E-03	96.40%
M8-M3-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	7.20E-03	2.75E-03	2.22E-03	3.59E-03	1.33E-03	1.13E-03	94.00%
	0.132	1.88	0.1705	1.841	5.84E-02	6.31E-02	9.86E-03	2.74E-02	3.14E-03	1.21E-02	1.40E-02	1.52E-03	6.26E-03	97.00%
M8-M4-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	4.82E-03	1.70E-02	1.56E-03	4.72E-03	1.68E-03	1.52E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.07E-02	1.11E-02	1.82E-02	1.94E-03	8.11E-03	1.82E-02	1.91E-03	8.13E-03	96.30%
M8-M4-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	5.26E-03	1.92E-03	1.67E-03	4.58E-03	1.68E-03	1.45E-03	93.80%
	0.132	1.88	0.1705	1.841	5.84E-02	6.15E-02	1.07E-02	2.02E-02	2.19E-03	8.99E-03	1.80E-02	1.91E-03	8.04E-03	96.80%
M8-M5-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	3.77E-03	1.34E-03	1.21E-03	6.16E-03	2.27E-03	1.94E-03	93.80%
	0.132	1.88	0.1705	1.841	5.84E-02	6.15E-02	1.06E-02	1.44E-02	1.53E-03	6.41E-03	2.39E-02	2.59E-03	1.07E-02	96.50%
M8-M5-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	4.05E-03	1.48E-03	1.29E-03	6.04E-03	2.27E-03	1.88E-03	93.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.19E-02	1.03E-02	1.56E-02	1.69E-03					

Structure	(as drawn)		(after process bias)										Csum/ Ctotal		
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft		
	(um)	(um)	(um)	(um)	(Ohm□)	(fF/um)									
PO1(FOX)															
M8-M4-PO1(OD)	0.132	1.88	0.1705	1.841	5.84E-02	6.39E-02	9.44E-03	2.94E-02	3.43E-03	1.30E-02	1.39E-02	1.52E-03	6.18E-03	97.30%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	5.47E-03	2.03E-03	1.72E-03	4.53E-03	1.68E-03	1.42E-03	93.90%	
M8-M4-PO1(FOX)	0.132	1.88	0.1705	1.841	5.84E-02	6.18E-02	1.05E-02	2.11E-02	2.31E-03	9.39E-03	1.79E-02	1.91E-03	7.99E-03	97.00%	
M8-M5-PO1(OD)	0.132	1.88	0.1705	1.841	5.84E-02	6.20E-02	1.02E-02	1.61E-02	1.76E-03	7.20E-03	2.36E-02	2.59E-03	1.05E-02	97.00%	
M8-M5-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	4.20E-03	1.55E-03	1.33E-03	5.99E-03	2.27E-03	1.86E-03	93.90%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.21E-02	1.02E-02	1.62E-02	1.77E-03	7.23E-03	2.36E-02	2.59E-03	1.05E-02	97.00%	
M8-M6-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	3.22E-03	1.24E-03	9.90E-04	8.57E-03	3.53E-03	2.52E-03	94.30%	
M8-M6-PO1(FOX)	0.132	1.88	0.1705	1.841	5.84E-02	6.59E-02	8.80E-03	1.26E-02	1.42E-03	5.60E-03	3.40E-02	4.03E-03	1.50E-02	97.40%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	3.23E-03	1.25E-03	9.93E-04	8.57E-03	3.53E-03	2.52E-03	94.30%	
M8-M7-PO1(OD)	0.132	1.88	0.1705	1.841	5.84E-02	6.59E-02	8.79E-03	1.27E-02	1.42E-03	5.62E-03	3.40E-02	4.03E-03	1.50E-02	97.40%	
M8-M7-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.02E-01	2.52E-03	1.04E-03	7.41E-04	1.69E-02	7.86E-03	4.54E-03	94.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	8.47E-02	6.27E-03	9.43E-03	1.19E-03	4.12E-03	6.13E-02	8.97E-03	2.62E-02	98.30%	
M8-M7-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.02E-01	2.53E-03	1.04E-03	7.44E-04	1.69E-02	7.86E-03	4.54E-03	94.60%	
M8-M2-M1	0.132	1.88	0.1705	1.841	5.84E-02	8.47E-02	6.26E-03	9.46E-03	1.19E-03	4.13E-03	6.13E-02	8.97E-03	2.61E-02	98.30%	
M8-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.01E-01	2.52E-02	1.33E-02	5.98E-03	2.43E-03	1.10E-03	6.66E-04	96.50%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.51E-02	4.18E-03	7.67E-02	1.51E-02	3.08E-02	8.95E-03	1.26E-03	3.85E-03	98.90%	
M8-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.92E-03	4.32E-03	2.80E-03	3.26E-03	1.33E-03	9.66E-04	94.60%	
M8-M4-M1	0.132	1.88	0.1705	1.841	5.84E-02	6.84E-02	7.76E-03	3.84E-02	4.92E-03	1.67E-02	1.31E-02	1.52E-03	5.82E-03	98.00%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	6.49E-03	2.58E-03	1.96E-03	4.30E-03	1.68E-03	1.31E-03	94.10%	
M8-M5-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	4.83E-03	1.84E-03	1.50E-03	5.87E-03	2.27E-03	1.80E-03	94.00%	
M8-M6-M1	0.132	1.88	0.1705	1.841	5.84E-02	6.28E-02	9.67E-03	1.88E-02	2.10E-03	8.33E-03	2.32E-02	2.59E-03	1.03E-02	97.60%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	3.64E-03	1.43E-03	1.10E-03	8.47E-03	3.53E-03	2.47E-03	94.40%	
M8-M7-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.02E-01	6.63E-02	8.49E-03	1.43E-02	1.63E-03	6.31E-03	3.36E-02	4.03E-03	97.80%
M8-M3-M2	0.132	1.88	0.1705	1.841	5.84E-02	6.09E-02	6.09E-03	1.05E-02	1.33E-03	4.57E-03	6.09E-02	8.97E-03	2.60E-02	98.50%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.00E-01	2.49E-02	1.33E-02	5.83E-03	2.87E-03	1.33E-03	7.72E-04	96.50%	
M8-M4-M2	0.132	1.88	0.1705	1.841	5.84E-02	9.53E-02	3.93E-03	7.60E-02	1.51E-02	3.04E-02	1.06E-02	1.52E-03	4.56E-03	99.20%	
M8-M5-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.61E-03	4.32E-03	2.65E-03	3.94E-03	1.68E-03	1.13E-03	94.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.92E-02	7.21E-03	3.77E-02	4.92E-03	1.64E-02	1.61E-02	1.91E-03	7.11E-03	98.60%	
M8-M5-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.02E-01	6.15E-03	2.58E-03	1.79E-03	5.43E-03	2.27E-03	1.58E-03	94.20%	
M8-M6-M2	0.132	1.88	0.1705	1.841	5.84E-02	6.51E-02	8.44E-03	2.48E-02	2.94E-03	1.09E-02	2.25E-02	2.59E-03	9.93E-03	98.50%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	4.45E-03	1.84E-03	1.31E-03	8.17E-03	3.53E-03	2.32E-03	94.50%	
M8-M7-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.21E-03	4.32E-03	2.44E-03	5.04E-03	2.27E-03	1.38E-03	94.90%	
M8-M4-M3	0.132	1.88	0.1705	1.841	5.84E-02	8.52E-02	5.74E-03	1.25E-02	1.63E-03	5.46E-03	6.02E-02	8.97E-03	2.56E-02	98.90%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.93E-02	2.46E-02	1.33E-02	5.65E-03	3.53E-03	1.68E-03	9.27E-04	96.60%	
M8-M5-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	9.21E-03	4.32E-03	2.44E-03	5.04E-03	2.27E-03	1.38E-03	94.90%	
M8-M6-M3	0.132	1.88	0.1705	1.841	5.84E-02	7.08E-02	6.28E-03	3.67E-02	4.92E-03	1.59E-02	2.10E-02	2.59E-03	9.20E-03	99.20%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	5.79E-03	2.58E-03	1.60E-03	7.72E-03	3.53E-03	2.10E-03	94.70%	
M8-M7-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.03E-01	4.10E-03	1.84E-03	1.13E-03	1.61E-02	7.86E-03	4.12E-03	94.80%	
M8-M5-M4	0.132	1.88	0.1705	1.841	5.84E-02	6.80E-02	5.20E-03	1.57E-02	2.10E-03	6.79E-03	5.93E-02	8.97E-03	2.52E-02	99.30%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.02E-01	3.31E-03	1.43E-03	9.42E-04	1.65E-02	7.86E-03	4.31E-03	94.70%	
M8-M4-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.93E-02	2.46E-02	1.33E-02	5.65E-03	3.53E-03	1.68E-03	9.27E-04	96.60%	
M8-M5-M3	0.132	1.88	0.1705	1.841	5.84E-02	9.58E-02	3.54E-03	7.51E-02	1.51E-02	3.00E-02	1.31E-02	1.91E-03	5.62E-03	99.40%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	9.21E-03	4.32E-03	2.44E-03	5.04E-03	2.27E-03	1.38E-03	94.90%	
M8-M6-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	5.79E-03	2.58E-03	1.60E-03	7.72E-03	3.53E-03	2.10E-03	94.70%	
M8-M7-M3	0.132	1.88	0.1705	1.841	5.84E-02	7.21E-02	3.38E-01	1.03E-01	4.10E-03	1.84E-03	1.13E-03	1.61E-02	7.86E-03	4.12E-03	94.80%
	0.132	1.88	0.1705	1.841	5.84E-02	8.07E-02	4.32E-03	2.09E-02	2.94E-03	8.97E-02	5.78E-02	8.97E-03	2.44E-02	99.70%	
M8-M6-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.00E-01	2.34E-02	1.33E-02	5.09E-03	6.73E-03	3.53E-03	1.60E-03	97.10%	
M8-M7-M5	0.132	1.88	0.1705	1.841	5.84E-02	7.50E-02	4.79E-03	3.50E-02	4.92E-03	1.51E-02	3.01E-02	4.03E-03	1.30E-02	99.70%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	1.01E-01	5.43E-03	2.58E-03	1.43E-03	1.56E-02	7.86E-03	3.86E-03	95.00%	
M8-M7-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.00E-01	5.43E-03	2.58E-03	1.43E-03	1.56E-02	7.86E-03	3.86E-03	95.00%	
M8-M5-M4	0.132	1.88	0.1705	1.841	5.84E-02	8.77E-02	4.32E-03	2.09E-02	2.94E-03	8.97E-02	5.78E-02	8.97E-03	2.44E-02	99.70%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.00E-01	2.40E-02	1.33E-02	5.38E-03	4.57E-03	2.27E-03	1.15E-03	96.80%	
M8-M6-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.00E-01	2.34E-02	1.33E-02	5.09E-03	6.73E-03	3.53E-03	1.60E-03	97.10%	
M8-M7-M5	0.132	1.88	0.1705	1.841	5.84E-02	1.00E-01	1.99E-03	7.10E-02	1.51E-02	2.79E-02	2.49E-02	4.03E-03	1.04E-02	99.90%	
	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.00E-01								

Structure	(as drawn)		(after process bias)										Csum/ Ctotal	
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M9-M4-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	5.80E-03	1.92E-03	1.94E-03	3.52E-03	1.15E-03	1.18E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.02E-02	1.17E-02	2.09E-02	2.19E-03	9.37E-03	1.29E-02	1.31E-03	5.81E-03	95.00%
M9-M5-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	4.35E-03	1.34E-03	1.50E-03	4.48E-03	1.40E-03	1.54E-03	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	5.92E-02	1.23E-02	1.52E-02	1.53E-03	6.82E-03	1.59E-02	1.59E-03	7.16E-03	94.10%
M9-M5-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	4.65E-03	1.48E-03	1.59E-03	4.38E-03	1.40E-03	1.49E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	5.96E-02	1.20E-02	1.65E-02	1.69E-03	7.40E-03	1.58E-02	1.59E-03	7.10E-03	94.60%
M9-M6-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	3.61E-03	1.11E-03	1.25E-03	5.66E-03	1.79E-03	1.93E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.06E-02	1.22E-02	1.26E-02	1.27E-03	5.65E-03	2.00E-02	2.04E-03	8.97E-03	93.90%
M9-M6-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	3.82E-03	1.20E-03	1.31E-03	5.56E-03	1.79E-03	1.89E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.08E-02	1.20E-02	1.34E-02	1.37E-03	6.04E-03	1.98E-02	2.04E-03	8.90E-03	94.30%
M9-M7-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.03E-01	3.03E-03	9.46E-04	1.04E-03	7.66E-03	2.48E-03	2.59E-03	92.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.70E-02	1.29E-02	1.06E-02	1.08E-03	4.75E-03	2.68E-02	2.83E-03	1.20E-02	94.30%
M9-M7-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.03E-01	3.20E-03	1.01E-03	1.10E-03	5.78E-03	2.48E-03	2.55E-03	92.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.71E-02	1.28E-02	1.12E-02	1.15E-03	5.04E-03	2.67E-02	2.83E-03	1.19E-02	94.60%
M9-M8-FOX	0.395	0.395	0.4695	0.3205	2.21E-02	3.28E-01	1.35E-01	4.73E-03	2.48E-03	1.12E-03	4.32E-02	2.47E-02	9.24E-03	97.30%
	0.395	2.82	0.4765	2.738	1.97E-02	1.46E-01	1.31E-02	1.35E-02	2.52E-03	5.51E-03	1.04E-01	2.51E-02	3.97E-02	98.80%
M9-M8-OD	0.395	0.395	0.4695	0.3205	2.21E-02	3.27E-01	1.35E-01	4.94E-03	2.62E-03	1.16E-03	4.29E-02	2.47E-02	9.10E-03	97.20%
	0.395	2.82	0.4765	2.738	1.97E-02	1.46E-01	1.30E-02	1.43E-02	2.66E-03	5.80E-03	1.04E-01	2.51E-02	3.96E-02	98.90%
M9-M1-PO1(OD)	0.113	0.113	0.131	0.095	1.00E-01	2.61E-01	1.08E-01	3.40E-02	1.84E-02	7.81E-03	1.40E-03	6.54E-04	3.74E-04	96.30%
	0.113	1.88	0.1736	1.819	7.60E-02	1.17E-01	2.98E-03	1.05E-01	2.44E-02	4.03E-02	5.09E-03	8.66E-04	2.11E-03	99.10%
M9-M1-PO1(FOX)	0.113	0.113	0.131	0.095	1.00E-01	2.62E-01	1.08E-01	3.67E-02	1.99E-02	8.41E-03	1.42E-03	6.54E-04	3.81E-04	96.60%
	0.113	1.88	0.1736	1.819	7.60E-02	1.21E-01	2.85E-03	1.09E-01	2.63E-02	4.14E-02	4.99E-03	8.66E-04	2.06E-03	99.10%
M9-M2-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.03E-01	1.27E-02	5.54E-03	3.57E-03	2.13E-03	8.45E-04	6.44E-04	94.80%
	0.132	1.88	0.1705	1.841	5.84E-02	7.22E-02	7.40E-03	4.70E-02	6.32E-03	2.03E-02	8.35E-03	9.63E-04	3.69E-03	97.20%
M9-M2-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.03E-01	1.29E-02	5.66E-03	3.61E-03	2.12E-03	8.45E-04	6.39E-04	94.90%
	0.132	1.88	0.1705	1.841	5.84E-02	7.25E-02	7.31E-03	4.76E-02	6.45E-03	2.06E-02	8.32E-03	9.63E-04	3.68E-03	97.20%
M9-M3-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	8.02E-03	2.97E-03	2.52E-03	2.76E-03	9.73E-04	8.92E-04	94.00%
	0.132	1.88	0.1705	1.841	5.84E-02	6.32E-02	1.01E-02	3.00E-02	3.39E-03	1.33E-02	1.06E-02	1.11E-03	4.73E-03	96.10%
M9-M3-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	8.08E-03	3.00E-03	2.54E-03	2.75E-03	9.73E-04	8.88E-04	94.00%
	0.132	1.88	0.1705	1.841	5.84E-02	6.33E-02	1.00E-02	3.02E-02	3.43E-03	1.34E-02	1.05E-02	1.11E-03	4.72E-03	96.10%
M9-M4-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	5.98E-03	2.03E-03	1.98E-03	3.45E-03	1.15E-03	1.15E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.05E-02	1.15E-02	2.19E-02	2.31E-03	9.78E-03	1.29E-02	1.31E-03	5.77E-03	95.30%
M9-M4-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	6.05E-03	2.04E-03	2.00E-03	3.46E-03	1.15E-03	1.15E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.06E-02	1.14E-02	2.20E-02	2.33E-03	9.84E-03	1.28E-02	1.31E-03	5.77E-03	95.30%
M9-M5-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	4.79E-03	1.54E-03	1.62E-03	4.33E-03	1.40E-03	1.46E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	5.98E-02	1.19E-02	1.71E-02	1.76E-03	7.66E-03	1.57E-02	1.59E-03	7.06E-03	94.70%
M9-M5-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	4.80E-03	1.55E-03	1.63E-03	4.32E-03	1.40E-03	1.46E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	5.98E-02	1.19E-02	1.72E-02	1.77E-03	7.69E-03	1.57E-02	1.59E-03	7.06E-03	94.80%
M9-M6-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	3.92E-03	1.24E-03	1.34E-03	5.52E-03	1.79E-03	1.87E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.08E-02	1.19E-02	1.89E-02	1.91E-03	7.66E-03	1.57E-02	1.59E-03	7.06E-03	94.40%
M9-M6-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	3.93E-03	1.25E-03	1.34E-03	5.52E-03	1.79E-03	1.86E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.08E-02	1.19E-02	1.89E-02	1.92E-03	7.68E-03	1.57E-02	1.59E-03	7.06E-03	94.80%
M9-M7-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	3.92E-03	1.24E-03	1.34E-03	5.52E-03	1.79E-03	1.87E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.08E-02	1.19E-02	1.89E-02	1.92E-03	7.68E-03	1.57E-02	1.59E-03	7.06E-03	94.40%
M9-M7-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.04E-01	3.93E-03	1.25E-03	1.34E-03	5.52E-03	1.79E-03	1.86E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.08E-02	1.19E-02	1.89E-02	1.92E-03	7.68E-03	1.57E-02	1.59E-03	7.06E-03	94.40%
M9-M8-PO1(OD)	0.395	0.395	0.4695	0.3205	2.21E-02	3.28E-01	1.35E-01	5.06E-03	2.69E-03	1.18E-03	4.28E-02	2.47E-02	9.07E-03	97.30%
	0.395	2.82	0.4765	2.738	1.97E-02	1.46E-01	1.29E-02	1.46E-02	2.73E-03	5.94E-03	1.04E-01	2.51E-02	3.96E-02	98.90%
M9-M2-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	9.88E-02	2.54E-02	1.33E-02	6.05E-03	1.88E-03	8.45E-04	5.19E-04	96.30%
	0.132	1.88	0.1705	1.841	5.84E-02	9.48E-02	4.44E-03	7.76E-02	1.51E-02	3.12E-02	6.99E-03	9.63E-04	3.01E-03	98.60%
M9-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	4.92E-03	2.43E-03	3.01E-03	2.52E-03	9.73E-04	7.74E-04	94.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.79E-02	8.32E-03	3.93E-02	4.92E-03	1.72E-02	9.93E-03	1.11E-03	4.41E-03	97.00%
M9-M4-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	7.07E-03	2.58E-03	2.25E-03	3.26E-03	1.15E-03	1.06E-03	93.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.22E-02	1.05E-02	2.64E-02	2.94E-03	1.31E-02	1.24E-02	1.31E-03	5.57E-03	96.10%
M9-M5-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	5.42E-03	1.84E-03	1.79E-03	4.14E-03	1.40E-03	1.37E-03	93.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.06E-02	1.03E-02	1.98E-02	2.10E-03	8.84E-03	1.54E-02	1.59E-03	6.91E-03	95.50%
M9-M6-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	4.34E-03	1.43E-03	1.46E-03	5.35E-03			

Structure	(as drawn)		(after process bias)												
	width (um)	space (um)	width	space	Rs (Ohm/□)	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/ Ctotal	
			(um)	(um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)		
M9-M7-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.05E-01	4.24E-03	1.43E-03	1.41E-03	7.24E-03	2.48E-03	2.38E-03	92.90%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.80E-02	1.20E-02	1.52E-02	1.63E-03	6.79E-03	2.60E-02	2.83E-03	1.16E-02	95.90%	
M9-M8-M2	0.395	0.395	0.4695	0.3205	2.21E-02	3.28E-01	1.35E-01	6.38E-03	3.46E-03	1.46E-03	4.26E-02	2.47E-02	8.93E-03	97.40%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.47E-01	1.22E-02	1.84E-02	3.51E-03	7.45E-03	1.03E-01	2.51E-02	3.92E-02	99.20%	
M9-M4-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.99E-02	2.51E-02	1.33E-02	5.94E-03	2.52E-03	1.15E-03	6.86E-04	96.50%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.52E-02	4.11E-03	7.66E-02	1.51E-02	3.07E-02	9.30E-03	1.31E-03	4.00E-03	98.90%	
M9-M5-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.81E-03	4.32E-03	2.75E-03	3.38E-03	1.40E-03	9.91E-04	94.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.88E-02	7.63E-03	3.83E-02	4.92E-03	1.67E-02	1.38E-02	1.59E-03	6.09E-03	97.80%	
M9-M6-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	6.58E-03	2.58E-03	2.00E-03	4.64E-03	1.79E-03	1.43E-03	94.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.46E-02	9.44E-03	2.55E-02	2.94E-03	1.13E-02	1.84E-02	2.04E-03	8.16E-03	97.10%	
M9-M7-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.04E-01	5.12E-03	1.84E-03	1.64E-03	6.90E-03	2.48E-03	2.21E-03	93.00%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.89E-02	1.12E-02	1.88E-02	2.10E-03	8.38E-03	2.54E-02	2.83E-03	1.13E-02	96.70%	
M9-M8-M3	0.395	0.395	0.4695	0.3205	2.21E-02	3.31E-01	1.36E-01	7.56E-03	4.18E-03	1.69E-03	4.22E-02	2.47E-02	8.75E-03	97.60%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.49E-01	1.15E-02	2.19E-02	4.24E-03	8.81E-03	1.03E-01	2.51E-02	3.89E-02	99.50%	
M9-M5-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.00E-01	2.49E-02	1.33E-02	5.84E-03	3.03E-03	1.40E-03	8.14E-04	96.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.56E-02	3.85E-03	7.59E-02	1.51E-02	3.04E-02	1.11E-02	1.59E-03	4.77E-03	99.10%	
M9-M6-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	9.70E-03	4.32E-03	2.69E-03	4.26E-03	1.79E-03	1.23E-03	94.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.05E-02	7.19E-03	3.76E-02	4.92E-03	1.64E-02	1.71E-02	2.04E-03	7.53E-03	98.10%	
M9-M7-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.03E-01	6.60E-03	2.58E-03	2.01E-03	6.49E-03	2.48E-03	2.00E-03	93.20%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.21E-02	2.36E-01	1.00E-01	2.49E-02	1.33E-02	5.84E-03	3.03E-03	1.40E-03	8.14E-04	96.60%
M9-M8-M4	0.395	0.395	0.4695	0.3205	2.21E-02	3.30E-01	1.36E-01	9.34E-03	5.27E-03	2.04E-03	4.18E-02	2.47E-02	8.55E-03	97.80%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.50E-01	1.05E-02	2.69E-02	5.35E-03	1.08E-02	1.02E-01	2.51E-02	3.85E-02	99.70%	
M9-M6-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.00E-01	2.47E-02	1.33E-02	5.72E-03	3.79E-03	1.79E-03	1.00E-03	96.70%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.68E-02	3.60E-03	7.49E-02	1.51E-02	2.99E-02	1.39E-02	2.04E-03	5.93E-03	99.20%	
M9-M7-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.03E-01	9.76E-03	4.32E-03	2.72E-03	5.96E-03	2.48E-03	1.74E-03	93.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	7.12E-02	9.96E-03	2.50E-02	2.94E-03	1.10E-02	2.47E-02	2.83E-03	1.09E-02	97.60%	
M9-M8-M5	0.395	0.395	0.4695	0.3205	2.21E-02	3.30E-01	1.36E-01	9.34E-03	5.27E-03	2.04E-03	4.18E-02	2.47E-02	8.55E-03	97.80%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.54E-01	9.10E-03	3.50E-02	7.25E-03	1.39E-02	1.01E-01	2.51E-02	3.78E-02	99.80%	
M9-M7-M6	0.132	0.132	0.1495	0.1145	7.21E-02	2.42E-01	1.01E-01	2.49E-02	1.33E-02	5.82E-03	5.36E-03	2.48E-03	1.44E-03	95.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	9.68E-02	3.60E-03	7.49E-02	1.51E-02	2.99E-02	1.39E-02	2.04E-03	5.93E-03	99.20%	
M9-M8-M6	0.395	0.395	0.4695	0.3205	2.21E-02	3.32E-01	1.34E-01	1.86E-02	1.11E-02	3.77E-03	4.10E-02	2.47E-02	8.15E-03	98.60%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.62E-01	6.95E-03	5.02E-02	1.12E-02	1.95E-02	9.83E-02	2.51E-02	3.66E-02	100.00%	
M9-M8-M7	0.395	0.395	0.4695	0.3205	2.21E-02	3.40E-01	1.29E-01	4.00E-02	2.47E-02	7.67E-03	4.09E-02	2.47E-02	8.10E-03	99.50%	
	0.395	2.82	0.4765	2.738	1.97E-02	1.90E-01	3.59E-03	8.98E-02	2.51E-02	3.24E-02	9.26E-02	2.51E-02	3.38E-02	100.00%	
M10-PO1-FOX	0.094	0.1316	0.065	0.1606	1.14E+01	1.66E-01	6.37E-02	2.50E-02	6.07E-03	9.45E-03	1.16E-03	2.53E-04	4.54E-04	92.20%	
	0.094	1.8471	0.065	1.876	1.14E+01	8.76E-02	3.29E-03	7.62E-02	6.07E-03	3.50E-02	3.70E-03	2.53E-04	1.72E-03	98.70%	
M10-M1-FOX	0.113	0.113	0.131	0.095	1.00E-01	2.55E-01	1.12E-01	1.44E-02	6.14E-03	4.14E-03	1.40E-03	5.41E-04	4.31E-04	94.10%	
	0.113	1.88	0.1736	1.819	7.60E-02	7.94E-02	6.94E-03	5.76E-02	8.13E-03	2.47E-02	5.73E-03	7.17E-04	2.51E-03	97.20%	
M10-M1-OD	0.113	0.113	0.131	0.095	1.00E-01	2.57E-01	1.10E-01	2.36E-02	1.17E-02	5.94E-03	1.25E-03	5.41E-04	3.55E-04	95.40%	
	0.113	1.88	0.1736	1.819	7.60E-02	9.83E-02	4.19E-03	8.36E-02	1.56E-02	3.40E-02	4.81E-03	7.17E-04	2.05E-03	98.40%	
M10-M2-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	9.76E-03	3.63E-03	3.07E-03	1.99E-03	6.83E-04	6.53E-04	94.10%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.56E-02	9.76E-03	3.56E-02	4.14E-03	1.57E-02	7.47E-03	7.79E-04	3.34E-03	95.50%	
M10-M2-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.02E-01	1.18E-02	4.82E-03	3.47E-03	1.84E-03	6.83E-04	5.80E-04	94.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.96E-02	8.27E-03	4.34E-02	5.50E-03	1.89E-02	7.09E-03	7.79E-04	3.15E-03	96.30%	
M10-M3-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	7.11E-03	2.32E-03	2.39E-03	2.46E-03	7.65E-04	8.46E-04	93.60%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.07E-02	1.16E-02	2.51E-02	2.64E-03	1.13E-02	8.85E-03	8.73E-04	3.99E-03	94.00%	
M10-M3-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	7.92E-03	2.75E-03	2.59E-03	2.33E-03	7.65E-04	7.84E-04	93.80%	
	0.132	1.88	0.1705	1.841	5.84E-02	6.22E-02	1.08E-02	2.87E-02	3.14E-03	1.28E-02	8.62E-03	8.73E-04	3.87E-03	94.80%	
M10-M4-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	5.68E-03	1.70E-03	1.99E-03	2.97E-03	8.69E-04	1.05E-03	93.30%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.90E-02	1.26E-02	1.95E-02	1.94E-03	8.77E-03	1.04E-02	9.91E-04	4.69E-03	93.10%	
M10-M4-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	6.16E-03	1.92E-03	2.12E-03	2.87E-03	8.69E-04	1.00E-03	93.50%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.97E-02	1.21E-02	2.15E-02	2.19E-03	9.67E-03	1.02E-02	9.91E-04	4.60E-03	93.70%	
M10-M5-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	4.75E-03	1.34E-03	1.71E-03	3.59E-03	1.01E-03	1.29E-03	93.30%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.86E-02	1.30E-02	1.59E-02	1.53E-03	7.16E-03	1.22E-02	1.15E-03	5.51E-03	92.30%	
M10-M5-OD	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	5.07E-03	1.48E-03	1.79E-03	3.49E-03	1.01E-03	1.24E-03	93.40%	
	0.132	1.88	0.1705	1.841	5.84E-02	5.88E-02	1.27E-02	1.71E-02	1.69E-03	7.71E-03	1.20E-02	1.15E-03	5.41E-03	92.60%	
M10-M6-FOX	0.132	0.132	0.1495	0.1145	7.21E-02	2.30E-01	1.03E-01	4.08E-03	1.11E-03	1.48E-0					

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm□)	(fF/um)								
	0.132	1.88	0.1705	1.841	5.84E-02	7.20E-02	7.58E-03	4.76E-02	6.32E-03	2.06E-02	6.90E-03	7.79E-04	3.06E-03	96.70%
M10-M2-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.03E-01	1.32E-02	5.66E-03	3.79E-03	1.79E-03	6.83E-04	5.52E-04	94.90%
	0.132	1.88	0.1705	1.841	5.84E-02	7.24E-02	7.49E-03	4.82E-02	6.45E-03	2.09E-02	6.87E-03	7.79E-04	3.05E-03	96.70%
M10-M3-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	8.32E-03	2.97E-03	2.68E-03	2.28E-03	7.65E-04	7.58E-04	93.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.28E-02	1.04E-02	3.05E-02	3.39E-03	1.36E-02	8.55E-03	8.73E-04	3.84E-03	95.20%
M10-M3-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	8.39E-03	3.00E-03	2.69E-03	2.28E-03	7.65E-04	7.55E-04	93.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.29E-02	1.03E-02	3.08E-02	3.43E-03	1.37E-02	8.53E-03	8.73E-04	3.83E-03	95.30%
M10-M4-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	6.38E-03	2.03E-03	2.18E-03	2.83E-03	8.69E-04	9.79E-04	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.00E-02	1.19E-02	2.25E-02	2.31E-03	1.01E-02	1.01E-02	9.91E-04	4.57E-03	93.90%
M10-M4-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.03E-01	6.41E-03	2.04E-03	2.18E-03	2.82E-03	8.69E-04	9.76E-04	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.01E-02	1.19E-02	2.26E-02	2.33E-03	1.01E-02	1.01E-02	9.91E-04	4.56E-03	94.00%
M10-M5-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.33E-01	1.05E-01	5.20E-03	1.54E-03	1.83E-03	3.45E-03	1.01E-03	1.22E-03	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	5.90E-02	1.26E-02	1.78E-02	1.77E-03	8.01E-03	1.19E-02	1.15E-03	5.38E-03	92.80%
M10-M5-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.31E-01	1.04E-01	5.22E-03	1.55E-03	1.84E-03	3.44E-03	1.01E-03	1.22E-03	93.40%
	0.132	1.88	0.1705	1.841	5.84E-02	5.90E-02	1.26E-02	1.77E-02	1.76E-03	7.97E-03	1.19E-02	1.15E-03	5.38E-03	92.90%
M10-M6-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.05E-01	4.41E-03	1.24E-03	1.58E-03	4.25E-03	1.19E-03	1.53E-03	93.40%
	0.132	1.88	0.1705	1.841	5.84E-02	5.96E-02	1.30E-02	1.45E-02	1.42E-03	6.55E-03	1.41E-02	1.36E-03	6.39E-03	91.80%
M10-M6-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.05E-01	4.42E-03	1.25E-03	1.59E-03	4.24E-03	1.19E-03	1.53E-03	93.40%
	0.132	1.88	0.1705	1.841	5.84E-02	5.96E-02	1.30E-02	1.46E-02	1.42E-03	6.58E-03	1.41E-02	1.36E-03	6.39E-03	91.80%
M10-M7-PO1(OD)	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.05E-01	3.92E-03	1.04E-03	1.44E-03	5.53E-03	1.47E-03	2.03E-03	92.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.47E-02	1.47E-02	1.23E-02	1.19E-03	5.55E-03	1.74E-02	1.67E-03	7.84E-03	91.30%
M10-M7-PO1(FOX)	0.132	0.132	0.1495	0.1145	7.21E-02	2.38E-01	1.05E-01	3.93E-03	1.04E-03	1.44E-03	5.52E-03	1.47E-03	2.03E-03	92.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.47E-02	1.47E-02	1.23E-02	1.19E-03	5.57E-03	1.74E-02	1.67E-03	7.84E-03	91.30%
M10-M8-PO1(OD)	0.395	0.395	0.4695	0.3205	2.21E-02	3.19E-01	1.42E-01	5.43E-03	2.69E-03	1.37E-03	1.52E-02	7.72E-03	3.72E-03	95.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.06E-01	2.17E-02	1.62E-02	2.73E-03	6.73E-03	4.39E-02	7.84E-03	1.80E-02	97.50%
M10-M8-PO1(FOX)	0.395	0.395	0.4695	0.3205	2.21E-02	3.20E-01	1.42E-01	5.47E-03	2.69E-03	1.39E-03	1.52E-02	7.72E-03	3.75E-03	95.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.06E-01	2.17E-02	1.62E-02	2.73E-03	6.75E-03	4.39E-02	7.84E-03	1.80E-02	97.50%
M10-M9-PO1(OD)	0.395	0.395	0.4695	0.3205	2.21E-02	3.45E-01	1.44E-01	4.33E-03	2.17E-03	1.08E-03	4.34E-02	2.40E-02	9.71E-03	97.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.52E-01	1.50E-02	1.21E-02	2.21E-03	4.96E-03	1.07E-01	2.43E-02	4.12E-02	98.00%
M10-M9-PO1(FOX)	0.395	0.395	0.4695	0.3205	2.21E-02	3.45E-01	1.44E-01	4.34E-03	2.18E-03	1.08E-03	4.34E-02	2.40E-02	9.71E-03	97.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.52E-01	1.50E-02	1.22E-02	2.21E-03	4.98E-03	1.07E-01	2.43E-02	4.12E-02	98.00%
M10-M2-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	9.97E-02	2.59E-02	1.33E-02	6.31E-03	1.59E-03	6.83E-04	4.52E-04	96.40%
	0.132	1.88	0.1705	1.841	5.84E-02	9.47E-02	4.58E-03	7.82E-02	1.51E-02	3.15E-02	5.75E-03	7.79E-04	2.49E-03	98.30%
M10-M3-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	1.07E-02	4.32E-03	3.20E-03	2.08E-03	7.65E-04	6.57E-04	94.40%
	0.132	1.88	0.1705	1.841	5.84E-02	6.76E-02	8.58E-03	3.99E-02	4.92E-03	1.75E-02	8.02E-03	8.73E-04	3.58E-03	96.20%
M10-M4-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.02E-01	7.29E-03	2.58E-03	2.36E-03	2.58E-03	8.69E-04	8.54E-04	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.18E-02	1.09E-02	2.71E-02	2.94E-03	1.21E-02	9.77E-03	9.91E-04	4.39E-03	94.80%
M10-M5-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.02E-01	5.73E-03	1.84E-03	1.95E-03	3.21E-03	1.01E-03	1.10E-03	93.40%
	0.132	1.88	0.1705	1.841	5.84E-02	5.99E-02	1.20E-02	2.05E-02	2.10E-03	9.21E-03	1.17E-02	1.15E-03	5.27E-03	93.80%
M10-M6-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.29E-01	1.02E-01	4.77E-03	1.43E-03	1.67E-03	4.02E-03	1.19E-03	1.41E-03	93.30%
	0.132	1.88	0.1705	1.841	5.84E-02	6.01E-02	1.26E-02	1.63E-02	1.63E-03	7.36E-03	1.39E-02	1.36E-03	6.29E-03	92.50%
M10-M7-M1	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	1.04E-01	4.26E-03	1.17E-03	1.54E-03	5.38E-03	1.47E-03	1.96E-03	92.20%
	0.132	1.88	0.1705	1.841	5.84E-02	6.50E-02	1.45E-02	1.36E-02	1.33E-03	6.12E-03	1.72E-02	1.67E-03	7.75E-03	91.80%
M10-M8-M1	0.395	0.395	0.4695	0.3205	2.21E-02	3.18E-01	1.41E-01	5.89E-03	2.95E-03	1.47E-03	1.50E-02	7.72E-03	3.65E-03	95.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.07E-01	2.14E-02	1.76E-02	2.99E-03	7.32E-03	4.37E-02	7.84E-03	1.80E-02	97.70%
M10-M9-M1	0.395	0.395	0.4695	0.3205	2.21E-02	3.46E-01	1.44E-01	4.63E-03	2.34E-03	1.14E-03	4.32E-02	2.40E-02	9.62E-03	97.10%
	0.395	2.82	0.4765	2.738	1.97E-02	1.52E-01	1.48E-02	1.30E-02	2.38E-03	5.32E-03	1.07E-01	2.43E-02	4.11E-02	98.10%
M10-M3-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	1.00E-01	2.58E-02	1.33E-02	6.26E-03	1.77E-03	7.65E-04	5.00E-04	96.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.50E-02	1.45E-02	1.36E-02	1.33E-03	6.12E-03	1.72E-02	1.67E-03	7.75E-03	91.80%
M10-M4-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	1.05E-02	4.32E-03	3.11E-03	2.31E-03	8.69E-04	7.23E-04	94.50%
	0.132	1.88	0.1705	1.841	5.84E-02	6.78E-02	8.40E-03	3.96E-02	4.92E-03	1.74E-02	9.03E-03	9.91E-04	4.02E-03	96.50%
M10-M5-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.34E-01	1.05E-01	7.31E-03	2.58E-03	2.37E-03	2.99E-03	1.01E-03	9.91E-04	93.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.23E-02	1.06E-02	2.69E-02	2.94E-03	1.20E-02	1.12E-02	1.15E-03	5.02E-03	95.10%
M10-M6-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.04E-01	5.75E-03	1.84E-03	1.95E-03	3.82E-03	1.19E-03	1.31E-03	93.70%
	0.132	1.88	0.1705	1.841	5.84E-02	6.11E-02	1.18E-02	2.02E-02	2.10E-03	9.06E-03	1.36E-02	1.36E-03	6.12E-03	93.90%
M10-M7-M2	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.04E-01	4.91E-03	1.43E-03	1.74E-03	5.13E-03	1.47E-03	1.83E-03	92.40%
	0.132	1.88	0.1705	1.841	5.84E-02	6.55E-02	1.39E-02	1.62E-02	1.63E-03	7.27E-03	1.6			

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
	0.132	1.88	0.1705	1.841	5.84E-02	6.35E-02	1.04E-02	2.66E-02	2.94E-03	1.18E-02	1.31E-02	1.36E-03	5.85E-03	95.20%
M10-M7-M3	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.05E-01	5.87E-03	1.84E-03	2.01E-03	4.83E-03	1.47E-03	1.68E-03	92.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.67E-02	1.31E-02	2.00E-02	2.10E-03	8.94E-03	1.64E-02	1.67E-03	7.39E-03	93.90%
M10-M8-M3	0.395	0.395	0.4695	0.3205	2.21E-02	3.19E-01	1.41E-01	7.95E-03	4.18E-03	1.89E-03	1.46E-02	7.72E-03	3.42E-03	95.70%
	0.395	2.82	0.4765	2.738	1.97E-02	1.09E-01	1.99E-02	2.42E-02	4.24E-03	9.97E-03	4.32E-02	7.84E-03	1.77E-02	98.50%
M10-M9-M3	0.395	0.395	0.4695	0.3205	2.21E-02	3.46E-01	1.44E-01	5.90E-03	3.06E-03	1.42E-03	4.28E-02	2.40E-02	9.42E-03	97.20%
	0.395	2.82	0.4765	2.738	1.97E-02	1.53E-01	1.41E-02	1.66E-02	3.10E-03	6.77E-03	1.06E-01	2.43E-02	4.06E-02	98.60%
M10-M5-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.99E-02	2.54E-02	1.33E-02	6.07E-03	2.26E-03	1.01E-03	6.29E-04	96.50%
	0.132	1.88	0.1705	1.841	5.84E-02	9.53E-02	4.23E-03	7.71E-02	1.51E-02	3.10E-02	8.28E-03	1.15E-03	3.56E-03	98.50%
M10-M6-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.32E-01	1.03E-01	1.03E-02	4.32E-03	3.02E-03	3.11E-03	1.19E-03	9.57E-04	94.60%
	0.132	1.88	0.1705	1.841	5.84E-02	6.94E-02	8.06E-03	3.89E-02	4.92E-03	1.70E-02	1.21E-02	1.36E-03	5.36E-03	96.70%
M10-M7-M4	0.132	0.132	0.1495	0.1145	7.21E-02	2.35E-01	1.03E-01	7.42E-03	2.58E-03	2.42E-03	4.45E-03	1.47E-03	1.49E-03	92.90%
	0.132	1.88	0.1705	1.841	5.84E-02	6.89E-02	1.17E-02	2.64E-02	2.94E-03	1.17E-02	1.59E-02	1.67E-03	7.10E-03	95.20%
M10-M8-M4	0.395	0.395	0.4695	0.3205	2.21E-02	3.20E-01	1.41E-01	9.83E-03	5.27E-03	2.28E-03	1.44E-02	7.72E-03	3.35E-03	96.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.11E-01	1.87E-02	2.97E-02	5.35E-03	1.22E-02	4.27E-02	7.84E-03	1.74E-02	98.90%
M10-M9-M4	0.395	0.395	0.4695	0.3205	2.21E-02	3.48E-01	1.45E-01	6.84E-03	3.60E-03	1.62E-03	4.24E-02	2.40E-02	9.23E-03	97.30%
	0.395	2.82	0.4765	2.738	1.97E-02	1.53E-01	1.36E-02	1.93E-02	3.66E-03	7.85E-03	1.05E-01	2.43E-02	4.03E-02	98.80%
M10-M6-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.36E-01	9.97E-02	2.54E-02	1.33E-02	6.06E-03	2.68E-03	1.19E-03	7.43E-04	96.60%
	0.132	1.88	0.1705	1.841	5.84E-02	9.61E-02	4.17E-03	7.67E-02	1.51E-02	3.08E-02	9.71E-03	1.36E-03	4.17E-03	98.50%
M10-M7-M5	0.132	0.132	0.1495	0.1145	7.21E-02	2.37E-01	1.03E-01	1.07E-02	4.32E-03	3.17E-03	3.98E-03	1.47E-03	1.26E-03	93.50%
	0.132	1.88	0.1705	1.841	5.84E-02	7.49E-02	9.33E-03	3.89E-02	4.92E-03	1.70E-02	1.48E-02	1.67E-03	6.58E-03	96.60%
M10-M8-M5	0.395	0.395	0.4695	0.3205	2.21E-02	3.21E-01	1.41E-01	1.28E-02	7.14E-03	2.85E-03	1.41E-02	7.72E-03	3.20E-03	96.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.15E-01	1.69E-02	3.86E-02	7.25E-03	1.57E-02	4.21E-02	7.84E-03	1.71E-02	99.30%
M10-M9-M5	0.395	0.395	0.4695	0.3205	2.21E-02	3.49E-01	1.45E-01	8.13E-03	4.39E-03	1.87E-03	4.20E-02	2.40E-02	8.99E-03	97.40%
	0.395	2.82	0.4765	2.738	1.97E-02	1.55E-01	1.29E-02	2.32E-02	4.46E-03	9.36E-03	1.05E-01	2.43E-02	4.01E-02	99.10%
M10-M7-M6	0.132	0.132	0.1495	0.1145	7.21E-02	2.39E-01	9.93E-02	2.60E-02	1.33E-02	6.38E-03	3.46E-03	1.47E-03	9.98E-04	95.50%
	0.132	1.88	0.1705	1.841	5.84E-02	1.02E-01	5.27E-03	7.73E-02	1.51E-02	3.11E-02	1.21E-02	1.67E-03	5.22E-03	98.50%
M10-M8-M6	0.395	0.395	0.4695	0.3205	2.21E-02	3.27E-01	1.42E-01	1.91E-02	1.11E-02	3.99E-03	1.38E-02	7.72E-03	3.02E-03	97.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.25E-01	1.41E-02	5.51E-02	1.12E-02	2.19E-02	4.09E-02	7.84E-03	1.65E-02	99.60%
M10-M9-M6	0.395	0.395	0.4695	0.3205	2.21E-02	3.52E-01	1.46E-01	1.01E-02	5.62E-03	2.23E-03	4.14E-02	2.40E-02	8.72E-03	97.70%
	0.395	2.82	0.4765	2.738	1.97E-02	1.57E-01	1.18E-02	2.88E-02	5.70E-03	1.15E-02	1.03E-01	2.43E-02	3.95E-02	99.50%
M10-M8-M7	0.395	0.395	0.4695	0.3205	2.21E-02	3.31E-01	1.35E-01	4.07E-02	2.47E-02	8.00E-03	1.36E-02	7.72E-03	2.96E-03	98.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.55E-01	9.36E-03	9.78E-02	2.51E-02	3.64E-02	3.83E-02	7.84E-03	1.52E-02	99.80%
M10-M9-M7	0.395	0.395	0.4695	0.3205	2.21E-02	3.48E-01	1.44E-01	1.36E-02	7.79E-03	2.89E-03	4.09E-02	2.40E-02	8.46E-03	98.00%
	0.395	2.82	0.4765	2.738	1.97E-02	1.60E-01	9.96E-03	3.81E-02	7.91E-03	1.51E-02	1.02E-01	2.43E-02	3.88E-02	99.80%
M10-M9-M8	0.395	0.395	0.4695	0.3205	2.21E-02	3.59E-01	1.39E-01	4.00E-02	2.47E-02	7.65E-03	4.02E-02	2.40E-02	8.11E-03	99.50%
	0.395	2.82	0.4765	2.738	1.97E-02	1.94E-01	4.20E-03	9.08E-02	2.51E-02	3.29E-02	9.45E-02	2.43E-02	3.51E-02	100.00%

### 13.16.3.3 M1MxMz process in CLN80GC 1.0V/2.5V, no My/Mu, x=2~7, z=8~9

(a) Structure A at 25 °C

Structure	(as drawn)		(after process bias)								
	width (um)	space (um)	Width (um)	Space (um)	Rs (Ohm/□)	Ctotal (fF/um)	Cc (fF/um)	Cbottom (fF/um)	Ca (fF/um)	Cf (fF/um)	Csum/Ctotal
PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.63E-01	6.14E-02	2.66E-02	5.51E-03	1.06E-02	92.0%
	0.09	2	0.059	2.031	1.08E+01	8.86E-02	3.43E-03	8.03E-02	5.51E-03	3.74E-02	98.4%
M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.30E-01	9.96E-02	1.55E-02	5.74E-03	4.90E-03	93.2%
	0.108	2	0.1538	1.954	7.80E-02	8.12E-02	6.59E-03	6.50E-02	7.64E-03	2.87E-02	96.3%
M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.30E-01	9.60E-02	2.58E-02	1.16E-02	7.08E-03	94.8%
	0.108	2	0.1538	1.954	7.80E-02	1.03E-01	3.85E-03	9.33E-02	1.55E-02	3.89E-02	97.8%
M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.36E-01	9.55E-02	3.55E-02	1.72E-02	9.16E-03	95.8%
	0.108	2	0.1538	1.954	7.80E-02	1.21E-01	3.10E-03	1.12E-01	2.29E-02	4.48E-02	98.4%
M1-PO1(FOX)	0.108	0.108	0.1155	0.1005	1.15E-01	2.37E-01	9.49E-02	3.80E-02	1.87E-02	9.69E-03	96.0%
	0.108	2	0.1538	1.954	7.80E-02	1.25E-01	2.96E-03	1.17E-01	2.49E-02	4.61E-02	98.5%
M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.11E-02	1.24E-02	4.06E-03	4.17E-03	93.1%
	0.126	2	0.1818	1.944	5.74E-02	7.03E-02	9.60E-03	4.69E-02	5.22E-03	2.08E-02	94.0%
M2-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.25E-02	1.48E-02	5.74E-03	4.54E-03	93.8%
	0.126	2	0.1818	1.944	5.74E-02	7.65E-02	7.73E-03	5.76E-02	7.37E-03	2.51E-02	95.4%
M2-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.01E-02	1.65E-02	6.60E-03	4.95E-03	94.1%
	0.126	2	0.1818	1.944	5.74E-02	7.99E-02	7.08E-03	6.24E-02	8.48E-03	2.70E-02	95.8%
M2-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.01E-02	1.68E-02	6.77E-03	5.01E-03	94.1%
	0.126	2	0.1818	1.944	5.74E-02	8.05E-02	6.97E-03	6.33E-02	8.70E-03	2.73E-02	95.9%
M2-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.55E-02	4.09E-02	2.14E-02	9.73E-03	96.4%
	0.126	2	0.1818	1.944	5.74E-02	1.23E-01	3.84E-03	1.13E-01	2.75E-02	4.26E-02	98.1%
M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.08E-01	9.11E-02	9.83E-03	2.74E-03	3.54E-03	92.4%
	0.126	2	0.1818	1.944	5.74E-02	6.44E-02	1.14E-02	3.65E-02	3.52E-03	1.65E-02	92.0%
M3-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.25E-02	1.11E-02	3.42E-03	3.84E-03	92.9%
	0.126	2	0.1818	1.944	5.74E-02	6.71E-02	1.02E-02	4.21E-02	4.39E-03	1.89E-02	93.2%
M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.12E-02	1.16E-02	3.71E-03	3.95E-03	93.0%
	0.126	2	0.1818	1.944	5.74E-02	6.83E-02	9.76E-03	4.43E-02	4.76E-03	1.98E-02	93.6%
M3-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.12E-02	1.17E-02	3.76E-03	3.97E-03	93.0%
	0.126	2	0.1818	1.944	5.74E-02	6.85E-02	9.68E-03	4.47E-02	4.83E-03	2.00E-02	93.6%
M3-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.03E-02	1.55E-02	6.06E-03	4.73E-03	93.9%
	0.126	2	0.1818	1.944	5.74E-02	7.75E-02	7.34E-03	5.94E-02	7.79E-03	2.58E-02	95.5%
M3-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.21E-01	8.59E-02	4.09E-02	2.14E-02	9.75E-03	96.5%
	0.126	2	0.1818	1.944	5.74E-02	1.22E-01	3.78E-03	1.12E-01	2.75E-02	4.25E-02	98.0%
M4-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.31E-02	8.71E-03	2.07E-03	3.32E-03	92.3%
	0.126	2	0.1818	1.944	5.74E-02	6.17E-02	1.26E-02	3.03E-02	2.66E-03	1.38E-02	90.0%
M4-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.31E-02	9.37E-03	2.43E-03	3.47E-03	92.5%
	0.126	2	0.1818	1.944	5.74E-02	6.31E-02	1.18E-02	3.38E-02	3.13E-03	1.54E-02	91.1%
M4-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.30E-02	9.63E-03	2.58E-03	3.53E-03	92.6%
	0.126	2	0.1818	1.944	5.74E-02	6.37E-02	1.16E-02	3.51E-02	3.31E-03	1.59E-02	91.5%
M4-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.15E-02	9.68E-03	2.60E-03	3.54E-03	92.4%
	0.126	2	0.1818	1.944	5.74E-02	6.38E-02	1.16E-02	3.53E-02	3.34E-03	1.60E-02	91.5%
M4-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.13E-02	1.13E-02	3.53E-03	3.90E-03	92.9%
	0.126	2	0.1818	1.944	5.74E-02	6.76E-02	9.97E-03	4.30E-02	4.54E-03	1.93E-02	93.1%
M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.03E-02	1.56E-02	6.06E-03	4.77E-03	94.0%
	0.126	2	0.1818	1.944	5.74E-02	7.78E-02	7.32E-03	5.95E-02	7.79E-03	2.58E-02	95.3%
M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.51E-02	4.10E-02	2.14E-02	9.79E-03	96.5%
	0.126	2	0.1818	1.944	5.74E-02	1.23E-01	3.78E-03	1.13E-01	2.75E-02	4.26E-02	98.2%
M5-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.32E-02	7.99E-03	1.66E-03	3.16E-03	92.1%
	0.126	2	0.1818	1.944	5.74E-02	6.07E-02	1.36E-02	2.62E-02	2.14E-03	1.20E-02	88.1%
M5-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.18E-02	8.44E-03	1.89E-03	3.27E-03	92.1%
	0.126	2	0.1818	1.944	5.74E-02	6.14E-02	1.31E-02	2.86E-02	2.43E-03	1.31E-02	89.0%
M5-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.30E-02	8.60E-03	1.97E-03	3.31E-03	92.3%
	0.126	2	0.1818	1.944	5.74E-02	6.17E-02	1.29E-02	2.94E-02	2.54E-03	1.34E-02	89.3%
M5-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.30E-02	8.63E-03	1.99E-03	3.32E-03	92.3%
	0.126	2	0.1818	1.944	5.74E-02	6.18E-02	1.28E-02	2.96E-02	2.56E-03	1.35E-02	89.4%
M5-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.29E-02	9.56E-03	2.49E-03	3.53E-03	92.6%
	0.126	2	0.1818	1.944	5.74E-02	6.37E-02	1.17E-02	3.44E-02	3.20E-03	1.56E-02	90.9%
M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.15E-02	1.14E-02	3.53E-03	3.95E-03	93.0%
	0.126	2	0.1818	1.944	5.74E-02	6.80E-02	9.93E-03	4.32E-02	4.54E-03	1.93E-02	92.8%
M5-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	1.57E-02	6.06E-03	4.82E-03	94.0%
	0.126	2	0.1818	1.944	5.74E-02	7.81E-02	7.29E-03	5.96E-02	7.79E-03	2.59E-02	95.0%
M5-M4	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.54E-02	4.11E-02	2.14E-02	9.87E-03	96.5%
	0.126	2	0.1818	1.944	5.74E-02	1.23E-01	3.81E-03	1.13E-01	2.75E-02	4.27E-02	98.0%
M6-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.13E-02	7.60E-03	1.39E-03	3.10E-03	91.7%
	0.126	2	0.1818	1.944	5.74E-02	6.09E-02	1.46E-02	2.32E-02	1.79E-03	1.07E-02	86.1%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
M6-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.24E-02	7.94E-03	1.54E-03	3.20E-03	91.9%
	0.126	2	0.1818	1.944	5.74E-02	6.14E-02	1.42E-02	2.49E-02	1.98E-03	1.15E-02	86.9%
M6-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.22E-02	8.06E-03	1.60E-03	3.23E-03	91.9%
	0.126	2	0.1818	1.944	5.74E-02	6.16E-02	1.41E-02	2.55E-02	2.06E-03	1.17E-02	87.2%
M6-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.30E-02	8.08E-03	1.61E-03	3.23E-03	92.0%
	0.126	2	0.1818	1.944	5.74E-02	6.16E-02	1.40E-02	2.56E-02	2.07E-03	1.18E-02	87.2%
M6-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.21E-02	8.71E-03	1.92E-03	3.39E-03	92.1%
	0.126	2	0.1818	1.944	5.74E-02	6.27E-02	1.33E-02	2.90E-02	2.47E-03	1.32E-02	88.5%
M6-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.24E-02	9.80E-03	2.49E-03	3.65E-03	92.5%
	0.126	2	0.1818	1.944	5.74E-02	6.48E-02	1.20E-02	3.45E-02	3.20E-03	1.56E-02	90.3%
M6-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.15E-02	1.17E-02	3.53E-03	4.06E-03	93.0%
	0.126	2	0.1818	1.944	5.74E-02	6.90E-02	1.02E-02	4.32E-02	4.54E-03	1.94E-02	92.2%
M6-M4	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.10E-02	1.60E-02	6.06E-03	4.96E-03	94.1%
	0.126	2	0.1818	1.944	5.74E-02	7.91E-02	7.57E-03	5.97E-02	7.79E-03	2.60E-02	94.7%
M6-M5	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.50E-02	4.15E-02	2.14E-02	1.00E-02	96.5%
	0.126	2	0.1818	1.944	5.74E-02	1.24E-01	4.04E-03	1.13E-01	2.75E-02	4.27E-02	97.9%
M7-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.23E-02	7.50E-03	1.19E-03	3.16E-03	90.3%
	0.126	2	0.1818	1.944	5.74E-02	6.47E-02	1.69E-02	2.09E-02	1.53E-03	9.69E-03	84.5%
M7-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.23E-02	7.79E-03	1.31E-03	3.24E-03	90.4%
	0.126	2	0.1818	1.944	5.74E-02	6.50E-02	1.66E-02	2.22E-02	1.68E-03	1.03E-02	85.2%
M7-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.14E-01	9.27E-02	7.89E-03	1.35E-03	3.27E-03	90.5%
	0.126	2	0.1818	1.944	5.74E-02	6.51E-02	1.65E-02	2.27E-02	1.73E-03	1.05E-02	85.4%
M7-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.14E-01	9.27E-02	7.90E-03	1.35E-03	3.28E-03	90.5%
	0.126	2	0.1818	1.944	5.74E-02	6.52E-02	1.64E-02	2.28E-02	1.74E-03	1.05E-02	85.4%
M7-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.42E-02	8.39E-03	1.57E-03	3.41E-03	90.8%
	0.126	2	0.1818	1.944	5.74E-02	6.58E-02	1.59E-02	2.52E-02	2.01E-03	1.16E-02	86.5%
M7-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.16E-01	9.39E-02	9.17E-03	1.92E-03	3.62E-03	91.0%
	0.126	2	0.1818	1.944	5.74E-02	6.70E-02	1.50E-02	2.90E-02	2.47E-03	1.33E-02	88.0%
M7-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.30E-02	1.03E-02	2.49E-03	3.91E-03	91.3%
	0.126	2	0.1818	1.944	5.74E-02	6.92E-02	1.37E-02	3.47E-02	3.20E-03	1.57E-02	89.7%
M7-M4	0.126	0.126	0.1415	0.1105	1.00E-01	2.14E-01	9.18E-02	1.23E-02	3.53E-03	4.37E-03	91.8%
	0.126	2	0.1818	1.944	5.74E-02	7.34E-02	1.18E-02	4.36E-02	4.54E-03	1.95E-02	91.6%
M7-M5	0.126	0.126	0.1415	0.1105	1.00E-01	2.16E-01	9.19E-02	1.67E-02	6.06E-03	5.33E-03	92.9%
	0.126	2	0.1818	1.944	5.74E-02	8.34E-02	9.04E-03	6.04E-02	7.79E-03	2.63E-02	94.1%
M7-M6	0.126	0.126	0.1415	0.1105	1.00E-01	2.23E-01	8.53E-02	4.23E-02	2.14E-02	1.04E-02	95.3%
	0.126	2	0.1818	1.944	5.74E-02	1.28E-01	5.17E-03	1.15E-01	2.75E-02	4.37E-02	97.6%
M8-FOX	0.378	0.378	0.4265	0.3295	2.17E-02	3.09E-01	1.39E-01	1.02E-02	2.97E-03	3.62E-03	93.3%
	0.378	2	0.4318	1.946	1.86E-02	1.10E-01	3.82E-02	1.99E-02	3.00E-03	8.47E-03	87.4%
M8-OD	0.378	0.378	0.4265	0.3295	2.17E-02	3.08E-01	1.38E-01	1.06E-02	3.19E-03	3.71E-03	93.4%
	0.378	2	0.4318	1.946	1.86E-02	1.11E-01	3.80E-02	2.11E-02	3.23E-03	8.94E-03	87.7%
M8-PO1(OD)	0.378	0.378	0.4265	0.3295	2.17E-02	3.08E-01	1.38E-01	1.08E-02	3.27E-03	3.75E-03	93.4%
	0.378	2	0.4318	1.946	1.86E-02	1.11E-01	3.79E-02	2.15E-02	3.31E-03	9.10E-03	87.9%
M8-PO1(FOX)	0.378	0.378	0.4265	0.3295	2.17E-02	3.08E-01	1.38E-01	1.08E-02	3.29E-03	3.76E-03	93.4%
	0.378	2	0.4318	1.946	1.86E-02	1.11E-01	3.79E-02	2.16E-02	3.33E-03	9.13E-03	87.9%
M8-M1	0.378	0.378	0.4265	0.3295	2.17E-02	3.09E-01	1.39E-01	1.16E-02	3.69E-03	3.94E-03	93.6%
	0.378	2	0.4318	1.946	1.86E-02	1.11E-01	3.73E-02	2.36E-02	3.74E-03	9.94E-03	88.5%
M8-M2	0.378	0.378	0.4265	0.3295	2.17E-02	3.07E-01	1.37E-01	1.27E-02	4.32E-03	4.21E-03	93.7%
	0.378	2	0.4318	1.946	1.86E-02	1.12E-01	3.65E-02	2.67E-02	4.37E-03	1.12E-02	89.2%
M8-M3	0.378	0.378	0.4265	0.3295	2.17E-02	3.06E-01	1.37E-01	1.43E-02	5.20E-03	4.56E-03	94.0%
	0.378	2	0.4318	1.946	1.86E-02	1.13E-01	3.55E-02	3.11E-02	5.26E-03	1.29E-02	89.9%
M8-M4	0.378	0.378	0.4265	0.3295	2.17E-02	3.07E-01	1.36E-01	1.67E-02	6.53E-03	5.10E-03	94.4%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	3.41E-02	3.73E-02	6.61E-03	1.53E-02	90.9%
M8-M5	0.378	0.378	0.4265	0.3295	2.17E-02	3.08E-01	1.36E-01	2.07E-02	8.78E-03	5.98E-03	94.9%
	0.378	2	0.4318	1.946	1.86E-02	1.21E-01	3.20E-02	4.71E-02	8.89E-03	1.91E-02	92.0%
M8-M6	0.378	0.378	0.4265	0.3295	2.17E-02	3.10E-01	1.34E-01	2.89E-02	1.34E-02	7.73E-03	95.6%
	0.378	2	0.4318	1.946	1.86E-02	1.31E-01	2.87E-02	6.50E-02	1.36E-02	2.57E-02	93.3%
M8-M7	0.378	0.378	0.4265	0.3295	2.17E-02	3.22E-01	1.28E-01	5.38E-02	2.82E-02	1.28E-02	96.6%
	0.378	2	0.4318	1.946	1.86E-02	1.63E-01	2.29E-02	1.09E-01	2.86E-02	4.03E-02	95.2%
M9-FOX	0.378	0.378	0.4265	0.3295	2.17E-02	3.25E-01	1.46E-01	8.93E-03	2.36E-03	3.29E-03	92.8%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	4.16E-02	1.63E-02	2.38E-03	6.93E-03	86.0%
M9-OD	0.378	0.378	0.4265	0.3295	2.17E-02	3.27E-01	1.47E-01	9.21E-03	2.50E-03	3.36E-03	92.8%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	4.14E-02	1.70E-02	2.53E-03	7.22E-03	86.2%
M9-PO1(OD)	0.378	0.378	0.4265	0.3295	2.17E-02	3.27E-01	1.47E-01	9.31E-03	2.54E-03	3.38E-03	92.8%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	4.13E-02	1.72E-02	2.58E-03	7.32E-03	86.3%
M9-PO1(FOX)	0.378	0.378	0.4265	0.3295	2.17E-02	3.27E-01	1.47E-01	9.33E-03	2.55E-03	3.39E-03	92.8%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	4.13E-02	1.72E-02	2.58E-03	7.33E-03	86.3%
M9-M1	0.378	0.378	0.4265	0.3295	2.17E-02	3.27E-01	1.47E-01	9.81E-03	2.79E-03	3.51E-03	92.9%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	4.11E-02	1.84E-02	2.83E-03	7.81E-03	86.7%
M9-M2	0.378	0.378	0.4265	0.3295	2.17E-02	3.25E-01	1.46E-01	1.04E-02	3.13E-03	3.65E-03	93.0%
	0.378	2	0.4318	1.946	1.86E-02	1.16E-01	4.07E-02	2.01E-02	3.17E-03	8.48E-03	87.3%
M9-M3	0.378	0.378	0.4265	0.3295	2.17E-02	3.24E-01	1.45E-01	1.13E-02	3.57E-03	3.87E-03	93.2%

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Structure	(as drawn)		(after process bias)								
	width	space	Width	Space	Rs	Ctotal	Cc	Cbottom	Ca	Cf	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	
	0.378	2	0.4318	1.946	1.86E-02	1.17E-01	4.02E-02	2.23E-02	3.62E-03	9.35E-03	87.9%
M9-M4	0.378	0.378	0.4265	0.3295	2.17E-02	3.23E-01	1.45E-01	1.24E-02	4.16E-03	4.10E-03	93.4%
	0.378	2	0.4318	1.946	1.86E-02	1.18E-01	3.96E-02	2.52E-02	4.21E-03	1.05E-02	88.6%
M9-M5	0.378	0.378	0.4265	0.3295	2.17E-02	3.24E-01	1.45E-01	1.39E-02	4.96E-03	4.44E-03	93.6%
	0.378	2	0.4318	1.946	1.86E-02	1.19E-01	3.87E-02	2.91E-02	5.03E-03	1.20E-02	89.5%
M9-M6	0.378	0.378	0.4265	0.3295	2.17E-02	3.28E-01	1.46E-01	1.59E-02	6.17E-03	4.88E-03	94.0%
	0.378	2	0.4318	1.946	1.86E-02	1.21E-01	3.74E-02	3.47E-02	6.24E-03	1.42E-02	90.5%
M9-M7	0.378	0.378	0.4265	0.3295	2.17E-02	3.28E-01	1.45E-01	1.93E-02	8.13E-03	5.59E-03	94.5%
	0.378	2	0.4318	1.946	1.86E-02	1.25E-01	3.54E-02	4.34E-02	8.23E-03	1.76E-02	91.7%
M9-M8	0.378	0.378	0.4265	0.3295	2.17E-02	3.38E-01	1.36E-01	5.32E-02	2.82E-02	1.25E-02	96.5%
	0.378	2	0.4318	1.946	1.86E-02	1.66E-01	2.51E-02	1.08E-01	2.86E-02	3.98E-02	95.2%

## (b) Structure B at 25 °C

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M1-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.66E-01	5.36E-02	2.01E-02	5.51E-03	7.31E-03	3.46E-02	3.60E-03	1.55E-02	97.4%
	0.09	2	0.059	2.031	1.08E+01	1.18E-01	6.99E-05	4.46E-02	5.51E-03	1.95E-02	7.29E-02	3.60E-03	3.47E-02	100.0%
M2-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	5.87E-02	2.11E-02	5.51E-03	7.79E-03	1.13E-02	2.82E-03	4.22E-03	94.1%
	0.09	2	0.059	2.031	1.08E+01	9.32E-02	3.81E-04	5.97E-02	5.51E-03	2.71E-02	3.27E-02	2.82E-03	1.49E-02	100.0%
M2-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.40E-01	9.45E-02	1.13E-02	5.74E-03	2.76E-03	3.27E-02	1.75E-02	7.63E-03	96.9%
	0.108	2	0.1538	1.954	7.80E-02	1.36E-01	4.33E-04	3.89E-02	7.64E-03	1.56E-02	9.65E-02	2.33E-02	3.66E-02	100.0%
M2-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.42E-01	9.23E-02	2.13E-02	1.16E-02	4.85E-03	3.20E-02	1.75E-02	7.28E-03	98.2%
	0.108	2	0.1538	1.954	7.80E-02	1.51E-01	1.87E-04	6.32E-02	1.55E-02	2.38E-02	8.71E-02	2.33E-02	3.19E-02	100.0%
M2-M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.45E-01	9.01E-02	3.08E-02	1.72E-02	6.83E-03	3.19E-02	1.75E-02	7.22E-03	99.0%
	0.108	2	0.1538	1.954	7.80E-02	1.65E-01	1.29E-04	8.15E-02	2.29E-02	2.93E-02	8.28E-02	2.33E-02	2.98E-02	100.0%
M2-M1-PO1(FOX)	0.108	0.108	0.1155	0.1005	1.15E-01	2.47E-01	8.95E-02	3.34E-02	1.87E-02	7.35E-03	3.19E-02	1.75E-02	7.22E-03	99.1%
	0.108	2	0.1538	1.954	7.80E-02	1.68E-01	1.20E-04	8.59E-02	2.49E-02	3.05E-02	8.19E-02	2.33E-02	2.93E-02	100.0%
M3-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	5.94E-02	2.21E-02	5.51E-03	8.30E-03	6.68E-03	1.57E-03	2.56E-03	93.0%
	0.09	2	0.059	2.031	1.08E+01	8.85E-02	8.75E-04	6.61E-02	5.51E-03	3.03E-02	2.07E-02	1.57E-03	9.54E-03	100.0%
M3-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.32E-01	9.91E-02	1.17E-02	5.74E-03	2.96E-03	1.01E-02	4.95E-03	2.55E-03	94.9%
	0.108	2	0.1538	1.954	7.80E-02	9.51E-02	1.60E-03	4.90E-02	7.64E-03	2.07E-02	4.29E-02	6.59E-03	1.81E-02	100.0%
M3-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.34E-01	9.72E-02	2.18E-02	1.16E-02	5.09E-03	9.69E-03	4.95E-03	2.37E-03	96.5%
	0.108	2	0.1538	1.954	7.80E-02	1.14E-01	6.09E-04	7.58E-02	1.55E-02	3.02E-02	3.68E-02	6.59E-03	1.51E-02	100.0%
M3-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.21E-01	8.44E-02	7.80E-03	4.06E-03	1.87E-03	3.84E-02	2.14E-02	8.48E-03	97.2%
	0.126	2	0.1818	1.944	5.74E-02	1.35E-01	1.05E-03	2.67E-02	5.22E-03	1.08E-02	1.06E-01	2.75E-02	3.94E-02	100.0%
M3-M2-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.34E-02	1.06E-02	5.74E-03	2.43E-03	3.78E-02	2.14E-02	8.22E-03	97.7%
	0.126	2	0.1818	1.944	5.74E-02	1.39E-01	5.65E-04	3.46E-02	7.37E-03	1.36E-02	1.03E-01	2.75E-02	3.77E-02	100.0%
M3-M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.37E-01	9.49E-02	3.13E-02	1.72E-02	7.07E-03	9.58E-03	4.95E-03	2.32E-03	97.2%
	0.108	2	0.1538	1.954	7.80E-02	1.30E-01	4.05E-04	9.50E-02	2.29E-02	3.60E-02	3.40E-02	6.59E-03	1.37E-02	100.0%
M3-M1-PO1(FOX)	0.108	0.108	0.1155	0.1005	1.15E-01	2.38E-01	9.43E-02	3.39E-02	1.87E-02	7.59E-03	9.57E-03	4.95E-03	2.31E-03	97.4%
	0.108	2	0.1538	1.954	7.80E-02	1.34E-01	3.78E-04	9.95E-02	2.49E-02	3.73E-02	3.35E-02	6.59E-03	1.35E-02	100.0%
M3-M2-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.21E-01	8.36E-02	1.20E-02	6.60E-03	2.70E-03	3.76E-02	2.14E-02	8.12E-03	98.0%
	0.126	2	0.1818	1.944	5.74E-02	1.41E-01	4.49E-04	3.83E-02	8.48E-03	1.49E-02	1.01E-01	2.75E-02	3.70E-02	100.0%
M3-M2-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.22E-01	8.37E-02	1.23E-02	6.77E-03	2.76E-03	3.76E-02	2.14E-02	8.10E-03	98.0%
	0.126	2	0.1818	1.944	5.74E-02	1.41E-01	4.31E-04	3.90E-02	8.70E-03	1.52E-02	1.01E-01	2.75E-02	3.68E-02	100.0%
M3-M2-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.31E-01	7.85E-02	3.59E-02	2.14E-02	7.26E-03	3.72E-02	2.14E-02	7.88E-03	99.7%
	0.126	2	0.1818	1.944	5.74E-02	1.75E-01	7.92E-05	8.32E-02	2.75E-02	7.28E-02	9.12E-02	2.75E-02	3.18E-02	100.0%
M4-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	5.97E-02	2.28E-02	5.51E-03	8.65E-03	4.82E-03	1.09E-03	1.87E-03	92.6%
	0.09	2	0.059	2.031	1.08E+01	8.70E-02	1.32E-03	6.91E-02	5.51E-03	3.18E-02	1.51E-02	1.09E-03	7.03E-03	99.9%
M4-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.31E-01	9.97E-02	1.23E-02	5.74E-03	3.27E-03	6.37E-03	2.88E-03	1.74E-03	94.2%
	0.108	2	0.1538	1.954	7.80E-02	8.76E-02	2.82E-03	5.32E-02	7.64E-03	2.28E-02	2.86E-02	3.84E-03	1.24E-02	99.9%
M4-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.32E-01	9.70E-02	2.25E-02	1.16E-02	5.45E-03	6.02E-03	2.88E-03	1.57E-03	95.8%
	0.108	2	0.1538	1.954	7.80E-02	1.08E-01	1.28E-03	8.11E-02	1.55E-02	3.28E-02	2.42E-02	3.84E-03	1.02E-02	100.0%
M4-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.06E-02	8.16E-03	4.06E-03	2.05E-03	1.19E-02	6.06E-03	2.90E-03	95.2%
	0.126	2	0.1818	1.944	5.74E-02	8.80E-02	2.85E-03	3.35E-02	5.22E-03	1.41E-02	4.88E-02	7.79E-03	2.05E-02	99.9%
M4-M2-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	8.94E-02	1.09E-02	5.74E-03	2.58E-03	1.15E-02	6.06E-03	2.72E-03	95.8%
	0.126	2	0.1818	1.944	5.74E-02	9.29E-02	1.86E-03	4.28E-02	7.37E-03	1.77E-02	4.64E-02	7.79E-03	1.93E-02	100.0%
M4-M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.41E-02	5.48E-03	2.74E-03	1.37E-03	3.89E-02	2.14E-02	8.75E-03	96.9%
	0.126	2	0.1818	1.944	5.74E-02	1.32E-01	1.54E-03	1.94E-02	3.52E-03	7.93E-03	1.09E-01	2.75E-02	4.09E-02	99.9%
M4-M3-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.45E-02	6.66E-03	3.42E-03	1.62E-03	3.85E-02	2.14E-02	8.56E-03	97.1%
	0.126	2	0.1818	1.944	5.74E-02	1.33E-01	1.14E-03	2.33E-02	4.39E-03	9.43E-03	1.08E-01	2.75E-02	4.00E-02	100.0%
M4-M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.38E-01	9.58E-02	3.21E-02	1.72E-02	7.46E-03	5.92E-03	2.88E-03	1.52E-03	96.7%
	0.108	2	0.1538	1.954	7.80E-02	1.24E-01	8.90E-04	1.00E-01	2.29E-02	3.88E-02	2.21E-02	3.84E-03	9.15E-03	100.0%
M4-M1-PO1(FOX)	0.108	0.108	0.1155	0.1005	1.15E-01	2.39E-01	9.52E-02	3.47E-02	1.87E-02	8.00E-03	5.90E-03	2.88E-03	1.51E-03	96.8%
	0.108	2	0.1538	1.954	7.80E-02	1.28E-01	8.41E-04	1.05E-01	2.49E-02	4.01E-02	2.17E-02	3.84E-03	8.95E-03	100.0%
M4-M2-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	8.91E-02	1.23E-02	6.60E-03	2.86E-03	1.14E-02	6.06E-03	2.67E-03	96.1%
	0.126	2	0.1818	1.944	5.74E-02	9.54E-02	1.56E-03	4.70E-02	8.48E-03	1.92E-02	4.53E-02	7.79E-03	1.88E-02	100.0%
M4-M2-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	8.91E-02	1.26E-02	6.77E-03	2.91E-03	1.14E-02	6.06E-03	2.66E-03	96.1%
	0.126	2	0.1818	1.944	5.74E-02	9.59E-02	1.51E-03	4.78E-02	8.70E-03	1.95E-02	4.51E-02	7.79E-03	1.87E-02	100.0%
M4-M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.21E-01	8.45E-02	7.11E-03	3.71E-03	1.70E-03	3.83E-02	2.14E-02	8.43E-03	97.2%
	0.126	2	0.1818	1.944	5.74E-02	1.34E-01	1.01E-03	2.48E-02	4.76E-03	1.00E-02	1.07E-01	2.75E-02	3.97E-02	100.0%
M4-M3-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.21E-01	8.45E-02	7.21E-03	3.76E-03	1.72E-03	3.83E-02	2.14E-02	8.42E-03	97.2%
	0.126	2	0.1818	1.944	5.74E-02	1.34E-01	9.88E-04	2.51E-0						

Structure	(as drawn)		(after process bias)												
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/Ctotal	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)		
M5-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.30E-01	9.93E-02	1.28E-02	5.74E-03	3.51E-03	4.76E-03	2.03E-03	1.37E-03	93.9%	
	0.108	2	0.1538	1.954	7.80E-02	8.48E-02	3.77E-03	5.55E-02	7.64E-03	2.39E-02	2.15E-02	2.71E-03	9.42E-03	99.7%	
M5-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.32E-01	9.73E-02	2.30E-02	1.16E-02	5.67E-03	4.42E-03	2.03E-03	1.19E-03	95.5%	
	0.108	2	0.1538	1.954	7.80E-02	1.06E-01	1.88E-03	8.37E-02	1.55E-02	3.41E-02	1.81E-02	2.71E-03	7.67E-03	99.9%	
M5-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.04E-02	8.60E-03	4.06E-03	2.27E-03	7.50E-03	3.53E-03	1.99E-03	94.3%	
	0.126	2	0.1818	1.944	5.74E-02	7.88E-02	4.58E-03	3.65E-02	5.22E-03	1.56E-02	3.30E-02	4.54E-03	1.42E-02	99.7%	
M5-M2-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.05E-02	1.14E-02	5.74E-03	2.82E-03	7.21E-03	3.53E-03	1.84E-03	94.9%	
	0.126	2	0.1818	1.944	5.74E-02	8.44E-02	3.31E-03	4.64E-02	7.37E-03	1.95E-02	3.12E-02	4.54E-03	1.34E-02	99.9%	
M5-M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	5.81E-03	2.74E-03	1.53E-03	1.22E-02	6.06E-03	3.08E-03	94.8%	
	0.126	2	0.1818	1.944	5.74E-02	8.35E-02	3.83E-03	2.46E-02	3.52E-03	1.06E-02	5.10E-02	7.79E-03	2.16E-02	99.7%	
M5-M3-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	6.95E-03	3.42E-03	1.77E-03	1.19E-02	6.06E-03	2.93E-03	95.1%	
	0.126	2	0.1818	1.944	5.74E-02	8.53E-02	3.12E-03	2.93E-02	4.39E-03	1.25E-02	4.97E-02	7.79E-03	2.10E-02	99.9%	
M5-M4-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.47E-02	4.28E-03	2.07E-03	1.10E-03	3.94E-02	2.14E-02	8.99E-03	96.8%	
	0.126	2	0.1818	1.944	5.74E-02	1.30E-01	1.98E-03	1.52E-02	2.66E-03	6.28E-03	1.11E-01	2.75E-02	4.17E-02	99.8%	
M5-M4-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.47E-02	4.91E-03	2.43E-03	1.24E-03	3.90E-02	2.14E-02	8.79E-03	96.8%	
	0.126	2	0.1818	1.944	5.74E-02	1.31E-01	1.69E-03	1.75E-02	3.13E-03	7.20E-03	1.10E-01	2.75E-02	4.12E-02	99.9%	
M5-M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.36E-01	9.54E-02	3.27E-02	1.72E-02	7.76E-03	4.34E-03	2.03E-03	1.15E-03	96.4%	
	0.108	2	0.1538	1.954	7.80E-02	1.23E-01	1.39E-03	1.03E-01	2.29E-02	4.02E-02	1.64E-02	2.71E-03	6.86E-03	99.9%	
M5-M1-PO1(FOX)	0.108	0.108	0.1155	0.1005	1.15E-01	2.37E-01	9.45E-02	3.53E-02	1.87E-02	8.31E-03	4.33E-03	2.03E-03	1.15E-03	96.5%	
	0.108	2	0.1538	1.954	7.80E-02	1.27E-01	1.32E-03	1.08E-01	2.49E-02	4.15E-02	1.61E-02	2.71E-03	6.71E-03	99.9%	
M5-M2-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.02E-02	1.28E-02	6.60E-03	3.10E-03	7.10E-03	3.53E-03	1.78E-03	95.2%	
	0.126	2	0.1818	1.944	5.74E-02	8.72E-02	2.90E-03	5.08E-02	8.48E-03	2.12E-02	3.05E-02	4.54E-03	1.30E-02	99.9%	
M5-M2-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.02E-02	1.31E-02	6.77E-03	3.15E-03	7.08E-03	3.53E-03	1.78E-03	95.3%	
	0.126	2	0.1818	1.944	5.74E-02	8.78E-02	2.83E-03	5.17E-02	8.70E-03	2.15E-02	3.04E-02	4.54E-03	1.29E-02	99.9%	
M5-M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.07E-02	7.42E-03	3.71E-03	1.86E-03	1.18E-02	6.06E-03	2.86E-03	95.1%	
	0.126	2	0.1818	1.944	5.74E-02	8.62E-02	2.86E-03	3.12E-02	4.76E-03	1.32E-02	4.92E-02	7.79E-03	2.07E-02	99.9%	
M5-M3-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.06E-02	7.51E-03	3.76E-03	1.87E-03	1.18E-02	6.06E-03	2.85E-03	95.2%	
	0.126	2	0.1818	1.944	5.74E-02	8.64E-02	2.82E-03	3.15E-02	4.83E-03	1.33E-02	4.91E-02	7.79E-03	2.07E-02	99.9%	
M5-M4-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.47E-02	5.16E-03	2.58E-03	1.29E-03	3.89E-02	2.14E-02	8.74E-03	96.9%	
	0.126	2	0.1818	1.944	5.74E-02	1.31E-01	1.59E-03	1.84E-02	3.31E-03	7.54E-03	1.10E-01	2.75E-02	4.10E-02	99.9%	
M5-M4-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.47E-02	5.21E-03	2.60E-03	1.30E-03	3.89E-02	2.14E-02	8.73E-03	96.9%	
	0.126	2	0.1818	1.944	5.74E-02	1.31E-01	1.58E-03	1.85E-02	3.34E-03	7.60E-03	1.09E-01	2.75E-02	4.10E-02	99.9%	
M5-M2-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.44E-02	3.70E-02	2.14E-02	7.80E-03	6.78E-03	3.53E-03	1.62E-03	97.3%	
	0.126	2	0.1818	1.944	5.74E-02	1.27E-01	1.16E-03	1.00E-01	2.75E-02	3.62E-02	2.49E-02	4.54E-03	1.02E-02	100.0%	
M5-M3-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	8.91E-02	1.14E-02	6.06E-03	2.66E-03	1.14E-02	6.06E-03	2.67E-03	95.9%	
	0.126	2	0.1818	1.944	5.74E-02	9.35E-02	1.67E-03	4.43E-02	7.79E-03	1.82E-02	4.59E-02	7.79E-03	1.91E-02	100.0%	
M5-M4-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.21E-01	8.45E-02	6.85E-03	3.53E-03	1.66E-03	3.84E-02	2.14E-02	8.52E-03	97.2%	
	0.126	2	0.1818	1.944	5.74E-02	1.31E-01	1.58E-03	1.85E-02	3.34E-03	7.60E-03	1.09E-01	2.75E-02	4.10E-02	99.9%	
M5-M3-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.42E-02	3.62E-02	2.14E-02	7.42E-03	1.10E-02	6.06E-03	2.49E-03	98.0%	
	0.126	2	0.1818	1.944	5.74E-02	1.34E-01	1.518E-04	9.49E-02	2.75E-02	3.37E-02	3.79E-02	7.79E-03	1.51E-02	100.0%	
M5-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.22E-01	8.42E-02	1.11E-02	6.06E-03	2.50E-03	3.77E-02	2.14E-02	8.14E-03	97.9%	
	0.126	2	0.1818	1.944	5.74E-02	1.39E-01	4.89E-04	3.59E-02	7.79E-03	1.41E-02	1.02E-01	2.75E-02	3.73E-02	100.0%	
M5-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.31E-01	7.85E-02	3.59E-02	2.14E-02	7.26E-02	3.72E-02	2.14E-02	7.88E-03	99.7%	
	0.126	2	0.1818	1.944	5.74E-02	1.74E-01	1.52E-04	8.29E-02	2.75E-02	2.77E-02	9.07E-02	2.75E-02	3.16E-02	100.0%	
M6-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	5.99E-02	2.37E-02	5.51E-03	9.11E-03	3.14E-03	6.72E-04	1.23E-03	92.3%	
	0.09	2	0.059	2.031	1.08E+01	8.59E-02	1.88E-03	7.20E-02	5.51E-03	3.32E-02	9.87E-03	6.72E-04	4.60E-03	99.7%	
M6-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.30E-01	9.94E-02	1.31E-02	5.74E-03	3.70E-03	3.84E-03	1.57E-03	1.13E-03	93.8%	
	0.108	2	0.1538	1.954	7.80E-02	8.33E-02	4.45E-03	5.67E-02	7.64E-03	2.45E-02	1.72E-02	2.09E-03	7.57E-03	99.5%	
M6-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.33E-01	9.75E-02	2.33E-02	1.16E-02	5.86E-03	3.51E-03	1.57E-03	9.72E-04	95.4%	
	0.108	2	0.1538	1.954	7.80E-02	1.05E-01	2.36E-03	8.53E-02	1.55E-02	3.49E-02	1.44E-02	2.09E-03	6.16E-03	99.7%	
M6-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.13E-02	9.02E-03	4.06E-03	2.48E-03	5.66E-03	2.49E-03	1.59E-03	94.0%	
	0.126	2	0.1818	1.944	5.74E-02	7.50E-02	5.89E-03	3.79E-02	5.22E-03	1.64E-02	2.49E-02	3.20E-03	1.09E-02	99.5%	
M6-M2-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.08E-02	1.18E-02	5.74E-03	3.73E-02	2.04E-02	2.36E-02	3.20E-03	1.02E-02	99.7%
M6-M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.10E-02	6.18E-03	2.74E-03	1.72E-03	7.81E-03	3.53E-03	2.14E-03	93.9%	
	0.126	2	0.1818	1.944	5.74E-02	7.36E-02	5.83E-03	2.69E-02	3.52E-03	1.17E-02	3.46E-02	4.54E-03	1.50E-02	99.5%	
M6-M3-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	5.22E-03	2.43E-03	1.39E-03	2.13E-02	3.46E-03	1.23E-02	94.6%	
	0.126	2	0.1818	1.944	5.74E-02	8.24E-02	4.13E-03	2.24E-02	3.13E-03	9.62E-03	5.15E-02	7.79E-03	2.19E-02	99.7%	
M6-M4-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.48E-02	3.53E-03	1.66E-03	9.32E-04	3				

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M6-M2-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.02E-02	1.33E-02	6.60E-03	3.33E-03	5.29E-03	2.49E-03	1.40E-03	94.8%
	0.126	2	0.1818	1.944	5.74E-02	8.39E-02	3.95E-03	5.28E-02	8.48E-03	2.22E-02	2.30E-02	3.20E-03	9.89E-03	99.7%
M6-M2-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.02E-02	1.35E-02	6.77E-03	3.38E-03	5.27E-03	2.49E-03	1.39E-03	94.9%
	0.126	2	0.1818	1.944	5.74E-02	8.45E-02	3.86E-03	5.37E-02	8.70E-03	2.25E-02	2.29E-02	3.20E-03	9.83E-03	99.7%
M6-M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.08E-01	9.06E-02	7.82E-03	3.71E-03	2.06E-03	7.44E-03	3.53E-03	1.95E-03	94.2%
	0.126	2	0.1818	1.944	5.74E-02	7.68E-02	4.64E-03	3.40E-02	4.76E-03	1.46E-02	3.33E-02	4.54E-03	1.44E-02	99.8%
M6-M3-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.06E-02	7.95E-03	3.76E-03	2.10E-03	7.46E-03	3.53E-03	1.97E-03	94.3%
	0.126	2	0.1818	1.944	5.74E-02	7.70E-02	4.58E-03	3.44E-02	4.83E-03	1.48E-02	3.33E-02	4.54E-03	1.44E-02	99.8%
M6-M4-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	5.47E-03	2.58E-03	1.45E-03	1.22E-02	6.06E-03	3.07E-03	94.7%
	0.126	2	0.1818	1.944	5.74E-02	8.28E-02	3.95E-03	2.34E-02	3.31E-03	1.01E-02	5.12E-02	7.79E-03	2.17E-02	99.7%
M6-M4-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	5.52E-03	2.60E-03	1.46E-03	1.22E-02	6.06E-03	3.06E-03	94.7%
	0.126	2	0.1818	1.944	5.74E-02	8.29E-02	3.92E-03	2.36E-02	3.34E-03	1.01E-02	5.12E-02	7.79E-03	2.17E-02	99.7%
M6-M5-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.46E-02	4.10E-03	1.97E-03	1.06E-03	3.95E-02	2.14E-02	9.04E-03	96.7%
	0.126	2	0.1818	1.944	5.74E-02	1.30E-01	2.05E-03	1.46E-02	2.54E-03	6.05E-03	1.11E-01	2.75E-02	4.18E-02	99.8%
M6-M5-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.46E-02	4.13E-03	1.99E-03	1.07E-03	3.95E-02	2.14E-02	9.03E-03	96.7%
	0.126	2	0.1818	1.944	5.74E-02	1.30E-01	2.04E-03	1.47E-02	2.56E-03	6.09E-03	1.11E-01	2.75E-02	4.18E-02	99.8%
M6-M2-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.57E-02	3.76E-02	2.14E-02	8.07E-03	4.97E-03	2.49E-03	1.24E-03	97.0%
	0.126	2	0.1818	1.944	5.74E-02	1.25E-01	1.78E-03	1.03E-01	2.75E-02	3.76E-02	1.86E-02	3.20E-03	7.70E-03	99.9%
M6-M3-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	1.18E-02	6.06E-03	2.87E-03	7.10E-03	3.53E-03	1.79E-03	95.1%
	0.126	2	0.1818	1.944	5.74E-02	8.51E-02	3.07E-03	4.80E-02	7.79E-03	2.01E-02	3.09E-02	4.54E-03	1.32E-02	99.9%
M6-M4-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.02E-02	7.14E-03	3.53E-03	1.81E-03	1.19E-02	6.06E-03	2.90E-03	95.1%
	0.126	2	0.1818	1.944	5.74E-02	8.56E-02	2.99E-03	3.00E-02	4.54E-03	1.27E-02	4.95E-02	7.79E-03	2.08E-02	99.9%
M6-M5-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.48E-02	5.01E-03	2.49E-03	1.26E-03	3.90E-02	2.14E-02	8.77E-03	96.8%
	0.126	2	0.1818	1.944	5.74E-02	1.31E-01	1.66E-03	1.79E-02	3.20E-03	7.33E-03	1.10E-01	2.75E-02	4.11E-02	99.9%
M6-M3-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.44E-02	3.70E-02	2.14E-02	7.80E-03	6.78E-03	3.53E-03	1.62E-03	97.3%
	0.126	2	0.1818	1.944	5.74E-02	1.27E-01	1.16E-03	1.00E-01	2.75E-02	3.62E-02	2.49E-02	4.54E-03	1.02E-02	100.0%
M6-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	8.91E-02	1.14E-02	6.06E-03	2.66E-03	1.14E-02	6.06E-03	2.68E-03	95.9%
	0.126	2	0.1818	1.944	5.74E-02	9.35E-02	1.67E-03	4.43E-02	7.79E-03	1.82E-02	4.59E-02	7.79E-03	1.91E-02	100.0%
M6-M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.44E-02	6.85E-03	3.53E-03	1.66E-03	3.84E-02	2.14E-02	8.52E-03	97.2%
	0.126	2	0.1818	1.944	5.74E-02	1.33E-01	1.08E-03	2.39E-02	4.54E-03	9.67E-03	1.07E-01	2.75E-02	3.99E-02	100.0%
M6-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.42E-02	3.62E-02	2.14E-02	7.42E-03	1.10E-02	6.06E-03	2.49E-03	98.0%
	0.126	2	0.1818	1.944	5.74E-02	1.34E-01	5.18E-04	9.49E-02	2.75E-02	3.37E-02	3.79E-02	7.79E-03	1.51E-02	100.0%
M6-M5-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.22E-01	8.42E-02	1.11E-02	6.06E-03	2.50E-03	3.77E-02	2.14E-02	8.14E-03	97.9%
	0.126	2	0.1818	1.944	5.74E-02	1.39E-01	4.89E-04	3.59E-02	7.79E-03	1.41E-02	1.02E-01	2.75E-02	3.73E-02	100.0%
M6-M5-M4	0.126	0.126	0.1415	0.1105	1.00E-01	2.31E-01	7.85E-02	3.59E-02	2.14E-02	7.26E-03	3.72E-02	2.14E-02	7.88E-03	99.7%
	0.126	2	0.1818	1.944	5.74E-02	1.27E-01	1.16E-03	1.00E-01	2.75E-02	2.77E-02	9.07E-02	2.75E-02	3.16E-02	100.0%
M7-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	5.99E-02	2.40E-02	5.51E-03	9.25E-03	2.68E-03	5.64E-04	1.06E-03	92.2%
	0.09	2	0.059	2.031	1.08E+01	8.57E-02	2.06E-03	7.28E-02	5.51E-03	3.36E-02	8.41E-03	5.64E-04	3.92E-03	99.6%
M7-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.31E-01	9.97E-02	1.35E-02	5.74E-03	3.86E-03	3.23E-03	1.28E-03	9.74E-04	93.7%
	0.108	2	0.1538	1.954	7.80E-02	8.25E-02	4.91E-03	5.77E-02	7.64E-03	2.50E-02	1.44E-02	1.70E-03	6.35E-03	99.2%
M7-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.32E-01	9.75E-02	2.37E-02	1.16E-02	6.05E-03	2.94E-03	1.28E-03	8.32E-04	95.3%
	0.108	2	0.1538	1.954	7.80E-02	1.04E-01	2.71E-03	8.63E-02	1.55E-02	3.54E-02	1.20E-02	1.70E-03	5.14E-03	99.6%
M7-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.15E-02	9.37E-03	4.06E-03	2.65E-03	4.61E-03	1.92E-03	3.14E-03	93.8%
	0.126	2	0.1818	1.944	5.74E-02	7.32E-02	6.77E-03	3.89E-02	5.22E-03	1.69E-02	2.01E-02	2.47E-03	8.80E-03	99.1%
M7-M2-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.03E-02	1.22E-02	5.74E-03	3.21E-03	4.33E-03	1.92E-03	1.21E-03	94.3%
	0.126	2	0.1818	1.944	5.74E-02	7.93E-02	5.26E-03	4.94E-02	7.37E-03	2.10E-02	1.89E-02	2.47E-03	8.22E-03	99.4%
M7-M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.08E-01	9.10E-02	6.57E-03	2.74E-03	1.91E-03	5.98E-03	2.49E-03	1.74E-03	93.5%
	0.126	2	0.1818	1.944	5.74E-02	6.97E-02	7.28E-03	2.82E-02	3.52E-03	1.23E-02	2.63E-02	3.20E-03	1.15E-02	99.1%
M7-M3-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.16E-02	7.75E-03	3.42E-03	2.17E-03	5.74E-03	2.49E-03	1.62E-03	93.8%
	0.126	2	0.1818	1.944	5.74E-02	7.20E-02	6.33E-03	3.34E-02	4.39E-03	1.45E-02	2.55E-02	3.20E-03	1.11E-02	99.4%
M7-M4-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.12E-02	4.94E-03	2.07E-03	1.43E-03	8.14E-03	3.53E-03	2.30E-03	93.6%
	0.126	2	0.1818	1.944	5.74E-02	7.13E-02	6.79E-03	2.15E-02	2.66E-03	9.39E-03	3.57E-02	4.54E-03	1.56E-02	99.1%
M7-M4-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.10E-02	5.61E-03	2.43E-03	1.59E-03	7.92E-03	3.53E-03	2.20E-03	93.8%
	0.126	2	0.1818	1.944	5.74E-02	7.23E-02	6.21E-03	2.45E-02	3.13E-03	1.07E-02	3.50E-02	4.54E-03	1.52E-02	99.4%
M7-M5-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.05E-02	3.80E-03	1.66E-03	1.07E-03	1.28E-02	6.06E-03	3.38E-03	94.4%
	0.126	2	0.1818	1.944	5.74E-02	8.04E-02	5.18E-03	1.62E-02	2.14E-03	7.03E-03	5.32E-02	7.79E-03	2.27E-02	99.2%
M7-M5-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.04E-02	4.23E-03	1.89E-03	1.17E-03	1.26E-02	6.06E-03	3.29E-03	94.5%
	0.126	2	0.1818	1.944	5.74E-02	8.09E-02	4.87E-03	1.81E-02	2.43E-03	7.82E-03	5.26E-02	7.79E-03		

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
PO1(FOX)														
	0.126	2	0.1818	1.944	5.74E-02	8.29E-02	4.64E-03	5.49E-02	8.70E-03	2.31E-02	1.83E-02	2.47E-03	7.93E-03	99.5%
M7-M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.15E-02	8.25E-03	3.71E-03	2.27E-03	5.66E-03	2.49E-03	1.58E-03	93.9%
	0.126	2	0.1818	1.944	5.74E-02	7.32E-02	5.99E-03	3.55E-02	4.76E-03	1.54E-02	2.52E-02	3.20E-03	1.10E-02	99.5%
M7-M3-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.15E-02	8.34E-03	3.76E-03	2.29E-03	5.65E-03	2.49E-03	1.58E-03	93.9%
	0.126	2	0.1818	1.944	5.74E-02	7.34E-02	5.93E-03	3.59E-02	4.83E-03	1.55E-02	2.52E-02	3.20E-03	1.10E-02	99.5%
M7-M4-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.08E-01	9.09E-02	5.85E-03	2.58E-03	1.64E-03	7.82E-03	3.53E-03	2.15E-03	93.8%
	0.126	2	0.1818	1.944	5.74E-02	7.28E-02	5.99E-03	2.56E-02	3.31E-03	1.12E-02	3.48E-02	4.54E-03	1.51E-02	99.5%
M7-M4-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.08E-01	9.09E-02	5.89E-03	2.60E-03	1.65E-03	7.82E-03	3.53E-03	2.14E-03	93.8%
	0.126	2	0.1818	1.944	5.74E-02	7.29E-02	5.96E-03	2.59E-02	3.34E-03	1.13E-02	3.48E-02	4.54E-03	1.51E-02	99.5%
M7-M5-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.03E-02	4.39E-03	1.97E-03	1.21E-03	1.26E-02	6.06E-03	3.25E-03	94.5%
	0.126	2	0.1818	1.944	5.74E-02	8.12E-02	4.75E-03	1.88E-02	2.54E-03	8.12E-03	5.25E-02	7.79E-03	2.23E-02	99.5%
M7-M5-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.03E-02	4.42E-03	1.99E-03	1.21E-03	1.26E-02	6.06E-03	3.25E-03	94.5%
	0.126	2	0.1818	1.944	5.74E-02	8.12E-02	4.73E-03	1.89E-02	2.56E-03	8.17E-03	5.24E-02	7.79E-03	2.23E-02	99.5%
M7-M6-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.46E-02	3.40E-03	1.60E-03	8.99E-04	3.98E-02	2.14E-02	9.18E-03	96.6%
	0.126	2	0.1818	1.944	5.74E-02	1.30E-01	2.39E-03	1.22E-02	2.06E-03	5.05E-03	1.12E-01	2.75E-02	4.24E-02	99.7%
M7-M6-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.46E-02	3.42E-03	1.61E-03	9.04E-04	3.98E-02	2.14E-02	9.18E-03	96.6%
	0.126	2	0.1818	1.944	5.74E-02	1.30E-01	2.39E-03	1.22E-02	2.07E-03	5.07E-03	1.12E-01	2.75E-02	4.24E-02	99.7%
M7-M2-M1	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.48E-02	3.81E-02	2.14E-02	8.33E-03	3.95E-03	1.92E-03	1.01E-03	96.8%	
	0.126	2	0.1818	1.944	5.74E-02	1.24E-01	2.27E-03	1.04E-01	2.75E-02	3.84E-02	1.48E-02	2.47E-03	6.19E-03	99.8%
M7-M3-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.04E-02	1.22E-02	6.06E-03	3.09E-03	5.31E-03	2.49E-03	1.41E-03	94.7%
	0.126	2	0.1818	1.944	5.74E-02	1.81E-02	4.15E-03	4.99E-02	7.79E-03	2.11E-02	2.33E-02	3.20E-03	1.01E-02	99.7%
M7-M4-M1	0.126	0.1415	0.1105	1.00E-01	2.07E-01	8.98E-02	7.57E-03	3.53E-03	2.02E-03	7.55E-03	3.53E-03	2.01E-03	94.1%	
	0.126	2	0.1818	1.944	5.74E-02	7.62E-02	4.81E-03	3.28E-02	4.54E-03	1.41E-02	3.36E-02	4.54E-03	1.45E-02	99.7%
M7-M5-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	5.32E-03	2.49E-03	1.41E-03	1.22E-02	6.06E-03	3.09E-03	94.7%
	0.126	2	0.1818	1.944	5.74E-02	8.26E-02	4.05E-03	2.28E-02	3.20E-03	9.80E-03	5.14E-02	7.79E-03	2.18E-02	99.7%
M7-M6-M1	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.48E-02	4.02E-03	1.92E-03	1.05E-03	3.95E-02	2.14E-02	9.07E-03	96.7%	
	0.126	2	0.1818	1.944	5.74E-02	1.30E-01	2.10E-03	1.43E-02	2.47E-03	5.92E-03	1.11E-01	2.75E-02	4.19E-02	99.8%
M7-M3-M2	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.46E-02	3.75E-02	2.14E-02	8.06E-03	4.97E-03	2.49E-03	1.24E-03	97.0%	
	0.126	2	0.1818	1.944	5.74E-02	1.25E-01	1.78E-03	1.03E-01	2.75E-02	3.76E-02	1.86E-02	3.20E-03	7.70E-03	99.9%
M7-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	1.18E-02	6.06E-03	2.86E-03	7.10E-03	3.53E-03	1.78E-03	95.1%
	0.126	2	0.1818	1.944	5.74E-02	8.51E-02	3.07E-03	4.80E-02	7.79E-03	2.01E-02	3.09E-02	4.54E-03	1.32E-02	99.9%
M7-M5-M2	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.08E-02	7.14E-03	3.53E-03	1.80E-03	1.19E-02	6.06E-03	2.90E-03	95.1%	
	0.126	2	0.1818	1.944	5.74E-02	8.55E-02	2.99E-03	3.00E-02	4.54E-03	1.27E-02	4.94E-02	7.79E-03	2.08E-02	99.9%
M7-M6-M2	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.47E-02	5.01E-03	2.49E-03	1.26E-03	3.89E-02	2.14E-02	8.77E-03	96.8%	
	0.126	2	0.1818	1.944	5.74E-02	1.25E-01	1.78E-03	1.03E-01	2.75E-02	3.76E-02	1.86E-02	3.20E-03	7.70E-03	99.9%
M7-M4-M3	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.44E-02	3.70E-02	2.14E-02	7.80E-03	6.78E-03	3.53E-03	1.62E-03	97.3%	
	0.126	2	0.1818	1.944	5.74E-02	1.27E-01	1.16E-03	1.00E-01	2.75E-02	3.62E-02	2.49E-02	4.54E-03	1.02E-02	100.0%
M7-M5-M3	0.126	0.1415	0.1105	1.00E-01	2.11E-01	9.08E-02	7.14E-03	3.53E-03	1.80E-03	1.19E-02	6.06E-03	2.90E-03	95.9%	
	0.126	2	0.1818	1.944	5.74E-02	9.35E-02	1.67E-03	4.43E-02	7.79E-03	1.82E-02	4.59E-02	7.79E-03	1.91E-02	100.0%
M7-M6-M3	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.44E-02	6.85E-03	3.53E-03	1.66E-03	3.84E-02	2.14E-02	8.52E-03	97.2%	
	0.126	2	0.1818	1.944	5.74E-02	1.33E-01	1.08E-03	2.39E-02	4.54E-03	9.67E-03	1.07E-01	2.75E-02	3.99E-02	100.0%
M7-M5-M4	0.126	0.1415	0.1105	1.00E-01	2.20E-01	8.42E-02	3.62E-02	2.14E-02	7.42E-03	1.10E-02	6.06E-03	2.49E-03	98.0%	
	0.126	2	0.1818	1.944	5.74E-02	1.34E-01	5.18E-04	9.49E-02	2.75E-02	3.37E-02	3.79E-02	7.79E-03	1.51E-02	100.0%
M7-M6-M4	0.126	0.1415	0.1105	1.00E-01	2.22E-01	8.42E-02	1.11E-02	6.06E-03	2.50E-03	3.77E-02	2.14E-02	8.14E-03	97.9%	
	0.126	2	0.1818	1.944	5.74E-02	1.39E-01	4.89E-04	3.59E-02	7.79E-03	1.41E-02	1.02E-01	2.75E-02	3.73E-02	100.0%
M7-M6-M5	0.126	0.1415	0.1105	1.00E-01	2.31E-01	7.85E-02	3.59E-02	2.14E-02	7.26E-03	3.72E-02	2.14E-02	7.88E-03	99.7%	
	0.126	2	0.1818	1.944	5.74E-02	1.74E-01	1.52E-04	8.29E-02	2.75E-02	2.77E-02	9.07E-02	2.75E-02	3.16E-02	100.0%
M8-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	6.00E-02	2.43E-02	5.51E-03	9.41E-03	2.19E-03	4.54E-04	8.67E-04	92.1%
	0.09	2	0.059	0.2031	1.08E+01	8.56E-02	2.25E-03	7.37E-02	5.51E-03	3.41E-02	6.87E-03	4.54E-04	3.21E-03	99.4%
M8-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.30E-01	9.96E-02	1.38E-02	5.74E-03	4.05E-03	2.62E-03	1.00E-03	8.09E-04	93.6%
	0.108	2	0.1538	1.954	7.80E-02	8.19E-02	5.38E-03	5.86E-02	7.64E-03	2.55E-02	1.15E-02	1.33E-03	5.09E-03	98.8%
M8-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.32E-01	9.72E-02	2.41E-02	1.16E-02	6.25E-03	2.36E-03	1.00E-03	6.79E-04	95.3%
	0.108	2	0.1538	1.954	7.80E-02	1.04E-01	3.07E-03	8.73E-02	1.55E-02	3.59E-02	9.53E-03	1.33E-03	4.10E-03	99.3%
M8-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.08E-01	9.03E-02	9.79E-03	4.06E-03	2.87E-03	3.63E-03	1.43E-03	1.10E-03	93.5%
	0.126	2	0.1818	1.944	5.74E-02	7.19E-02	7.67E-03	3.99E-02	5.22E-03	1.73E-02	1.55E-02	1.84E-03	6.83E-03	98.4%
M8-M2-OD	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.18E-02	8.24E-03	3.42E-03	2.41E-03	4.30E-03	1.72E-03	1.29E-03	99.7%	
	0.126	2	0.1818	1.944	5.74E-02	6.72E-02	8.29E-03	2.61E-02	5.74E-03	3.43E-03	3.39E-03	1.43E-03	9.79E-04	94.2%
M8-M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.16E-02	4.35E-03	1.66E-03	1.34E-03	7.33E-03	2.91E-03	2.21E-03	93.2%
	0.126	2	0											

Structure	(as drawn)		(after process bias)												
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cab	Cfb	Ctop	Cat	Cft	Csum/Ctotal	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)	(fF/um)		
M8-M6-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.09E-02	3.79E-03	1.54E-03	1.12E-03	1.02E-02	4.44E-03	2.88E-03	93.8%	
	0.126	2	0.1818	1.944	5.74E-02	7.37E-02	6.76E-03	1.61E-02	1.98E-03	7.06E-03	4.32E-02	5.71E-03	1.87E-02	98.8%	
M8-M7-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.12E-02	2.79E-03	1.19E-03	8.00E-04	1.95E-02	9.36E-03	5.07E-03	94.3%	
	0.126	2	0.1818	1.944	5.74E-02	9.48E-02	4.88E-03	1.12E-02	1.53E-03	4.83E-03	7.29E-02	1.20E-02	3.04E-02	99.0%	
M8-M7-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.16E-01	9.08E-02	3.02E-03	1.31E-03	5.59E-04	1.93E-02	9.36E-03	4.99E-03	94.3%	
	0.126	2	0.1818	1.944	5.74E-02	9.49E-02	4.72E-03	1.21E-02	1.68E-03	5.23E-03	7.25E-02	1.20E-02	3.03E-02	99.1%	
M8-M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.35E-01	9.47E-02	3.38E-02	1.72E-02	8.32E-03	2.29E-03	1.00E-03	6.45E-04	96.1%	
	0.108	2	0.1538	1.954	7.80E-02	1.21E-01	2.34E-03	1.07E-01	2.29E-02	4.20E-02	8.62E-03	1.33E-03	3.65E-03	99.5%	
M8-M1-PO1(FOX)	0.108	0.108	0.1155	0.1005	1.15E-01	2.36E-01	9.43E-02	3.64E-02	1.87E-02	8.87E-03	2.28E-03	1.00E-03	6.39E-04	96.3%	
	0.108	2	0.1538	1.954	7.80E-02	1.25E-01	2.23E-03	1.12E-01	2.49E-02	4.33E-02	8.46E-03	1.33E-03	3.56E-03	99.6%	
M8-M2-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	1.40E-02	6.60E-03	3.71E-03	3.31E-03	1.43E-03	9.39E-04	94.5%	
	0.126	2	0.1818	1.944	5.74E-02	8.11E-02	5.45E-03	5.52E-02	8.48E-03	2.34E-02	1.42E-02	1.84E-03	6.18E-03	99.0%	
M8-M2-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	1.44E-02	6.77E-03	3.80E-03	3.31E-03	1.43E-03	9.41E-04	94.5%	
	0.126	2	0.1818	1.944	5.74E-02	8.17E-02	5.35E-03	5.61E-02	8.70E-03	2.37E-02	1.41E-02	1.84E-03	6.15E-03	99.0%	
M8-M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.17E-02	8.75E-03	3.71E-03	2.52E-03	4.22E-03	1.72E-03	1.25E-03	93.6%	
	0.126	2	0.1818	1.944	5.74E-02	7.06E-02	7.25E-03	3.68E-02	4.76E-03	1.60E-02	1.85E-02	2.22E-03	8.13E-03	98.8%	
M8-M3-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.17E-02	8.84E-03	3.76E-03	2.54E-03	4.21E-03	1.72E-03	1.24E-03	93.6%	
	0.126	2	0.1818	1.944	5.74E-02	7.08E-02	7.18E-03	3.72E-02	4.83E-03	1.62E-02	1.84E-02	2.22E-03	8.11E-03	98.8%	
M8-M4-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.19E-02	6.43E-03	2.58E-03	1.92E-03	5.41E-03	2.17E-03	1.62E-03	93.3%	
	0.126	2	0.1818	1.944	5.74E-02	6.78E-02	8.05E-03	2.73E-02	3.31E-03	1.20E-02	2.36E-02	2.78E-03	1.04E-02	98.8%	
M8-M4-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.19E-02	6.47E-03	2.60E-03	1.93E-03	5.40E-03	2.17E-03	1.62E-03	93.3%	
	0.126	2	0.1818	1.944	5.74E-02	6.79E-02	8.01E-03	2.75E-02	3.34E-03	1.21E-02	2.35E-02	2.78E-03	1.04E-02	98.8%	
M8-M5-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.15E-02	4.96E-03	1.97E-03	1.49E-03	7.11E-03	2.91E-03	2.10E-03	93.4%	
	0.126	2	0.1818	1.944	5.74E-02	6.84E-02	7.81E-03	2.12E-02	2.54E-03	9.32E-03	3.08E-02	3.74E-03	1.35E-02	98.8%	
M8-M5-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.15E-02	4.99E-03	1.99E-03	1.50E-03	7.10E-03	2.91E-03	2.09E-03	93.4%	
	0.126	2	0.1818	1.944	5.74E-02	6.84E-02	7.78E-03	2.13E-02	2.56E-03	9.38E-03	3.07E-02	3.74E-03	1.35E-02	98.8%	
M8-M6-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.13E-02	3.91E-03	1.60E-03	1.15E-03	1.01E-02	4.44E-03	2.85E-03	93.8%	
	0.126	2	0.1818	1.944	5.74E-02	7.39E-02	6.66E-03	1.66E-02	2.06E-03	7.28E-03	4.31E-02	5.71E-03	1.87E-02	98.9%	
M8-M6-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.05E-02	3.93E-03	1.61E-03	1.16E-03	1.01E-02	4.44E-03	2.85E-03	93.8%	
	0.126	2	0.1818	1.944	5.74E-02	7.39E-02	6.64E-03	1.67E-02	2.07E-03	7.32E-03	4.30E-02	5.71E-03	1.87E-02	98.9%	
M8-M7-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.16E-01	9.08E-02	3.11E-03	1.35E-03	8.80E-04	1.93E-02	9.36E-03	4.97E-03	94.3%	
	0.126	2	0.1818	1.944	5.74E-02	9.50E-02	4.66E-03	1.25E-02	1.73E-03	5.38E-03	7.24E-02	1.20E-02	3.02E-02	99.2%	
M8-M7-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.16E-01	9.08E-02	3.12E-03	1.35E-03	8.83E-04	1.93E-02	9.36E-03	4.96E-03	94.3%	
	0.126	2	0.1818	1.944	5.74E-02	9.50E-02	4.65E-03	1.25E-02	1.74E-03	5.40E-03	7.24E-02	1.20E-02	3.02E-02	99.2%	
M8-M2-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.46E-02	3.85E-02	2.14E-02	8.53E-03	3.01E-03	1.43E-03	7.87E-04	96.7%	
	0.126	2	0.1818	1.944	5.74E-02	1.23E-01	2.78E-03	1.06E-01	2.75E-02	3.91E-02	1.14E-02	1.84E-03	4.76E-03	99.6%	
M8-M3-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.03E-02	1.28E-02	6.06E-03	3.37E-03	3.91E-03	1.72E-03	1.09E-03	94.4%	
	0.126	2	0.1818	1.944	5.74E-02	7.96E-02	5.24E-03	5.15E-02	7.79E-03	2.19E-02	1.70E-02	2.22E-03	7.39E-03	99.3%	
M8-M4-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.03E-02	8.12E-03	3.53E-03	2.30E-03	5.10E-03	2.17E-03	1.47E-03	93.6%	
	0.126	2	0.1818	1.944	5.74E-02	7.12E-02	6.69E-02	3.47E-02	4.54E-03	1.51E-02	2.26E-02	2.78E-03	9.91E-03	99.2%	
M8-M5-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.04E-02	5.93E-03	2.49E-03	1.72E-03	6.82E-03	2.91E-03	1.95E-03	93.5%	
	0.126	2	0.1818	1.944	5.74E-02	7.01E-02	6.94E-03	2.56E-02	3.20E-03	1.12E-02	3.01E-02	3.74E-03	1.32E-02	99.2%	
M8-M6-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.09E-02	4.50E-03	1.92E-03	1.29E-03	9.83E-03	4.44E-03	2.70E-03	93.9%	
	0.126	2	0.1818	1.944	5.74E-02	7.47E-02	6.12E-03	1.95E-02	2.47E-03	8.49E-03	4.24E-02	5.71E-03	1.84E-02	99.2%	
M8-M7-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.09E-02	3.50E-03	1.57E-03	9.64E-04	1.89E-02	9.36E-03	4.78E-03	94.3%	
	0.126	2	0.1818	1.944	5.74E-02	9.24E-02	4.40E-03	1.43E-02	2.01E-03	6.13E-03	7.17E-02	1.20E-02	2.99E-02	99.4%	
M8-M3-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.49E-02	3.83E-02	2.14E-02	8.44E-03	3.58E-03	1.72E-03	9.29E-04	96.8%	
	0.126	2	0.1818	1.944	5.74E-02	1.24E-02	1.24E-01	2.47E-03	1.05E-01	2.75E-02	3.87E-02	1.34E-02	2.22E-03	5.61E-03	99.7%
M8-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.08E-02	1.25E-02	6.06E-03	3.20E-03	4.73E-03	2.17E-03	1.28E-03	94.6%	
	0.126	2	0.1818	1.944	5.74E-02	8.08E-02	4.61E-03	5.06E-02	7.79E-03	2.14E-02	2.07E-02	2.78E-03	8.94E-03	99.6%	
M8-M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.00E-02	7.77E-03	3.53E-03	2.12E-03	6.45E-03	2.91E-03	1.77E-03	93.9%	
	0.126	2	0.1818	1.944	5.74E-02	7.40E-02	5.60E-03	3.37E-02	4.54E-03	1.46E-02	2.88E-02	3.74E-03	1.25E-02	99.6%	
M8-M6-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.07E-02	5.54E-03	2.49E-03	1.52E-03	9.49E-03	4.44E-03	2.52E-03	94.1%	
	0.126	2	0.1818	1.944	5.74E-02	7.64E-02	5.27E-03	4.21E-02	3.20E-03	4.73E-03	2.17E-03	1.28E-03	94.6%		
M8-M7-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.02E-02	4.22E-02	1.92E-03	1.15E-03	1.88E-02	9.36E-03	4.70E-03	94.5%	
	0.126	2	0.1818	1.944	5.74E-02	9.61E-02	3.93E-03	1.71E-02	2.47E-03	7.30E-03	7.08E-02	1.20E-02	2.94E-02	99.6%	
M8-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.52E-02	3.78E-02	2.14E-02	8.20E-03	4.39E-03	2.17E-03	1.11E-03	96.9%	
	0.126	2	0.1818	1.944	5.74E-02	1.24E-01	2.06E-03	1.04E-01	2.75E-02	3.81E-02</td					

Structure	(as drawn)		(after process bias)											
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)								
M8-M7-M4	0.126	2	0.1818	1.944	5.74E-02	8.84E-02	2.49E-03	4.66E-02	7.79E-03	1.94E-02	3.68E-02	5.71E-03	1.55E-02	99.9%
M8-M6-M5	0.126	0.126	0.1415	0.1105	1.00E-01	2.14E-01	8.92E-02	7.05E-03	3.53E-03	1.76E-03	1.78E-02	9.36E-03	4.24E-03	94.9%
M8-M7-M5	0.126	2	0.1818	1.944	5.74E-02	1.00E-01	2.38E-03	2.82E-02	4.54E-03	1.18E-02	6.73E-02	1.20E-02	2.77E-02	99.9%
M8-M7-M6	0.126	0.126	0.1415	0.1105	1.00E-01	2.26E-01	8.41E-02	3.62E-02	2.14E-02	7.41E-03	1.69E-02	9.36E-03	3.75E-03	97.8%
M9-PO1-FOX	0.09	0.135	0.059	0.166	1.08E+01	1.59E-01	6.01E-02	2.46E-02	5.51E-03	9.56E-03	1.73E-03	3.53E-04	6.87E-04	92.0%
M9-M1-FOX	0.108	0.108	0.1155	0.1005	1.15E-01	2.29E-01	9.88E-02	1.43E-02	5.74E-03	4.26E-03	2.06E-03	7.56E-04	6.52E-04	93.5%
M9-M1-OD	0.108	0.108	0.1155	0.1005	1.15E-01	2.26E-01	9.81E-02	2.75E-02	3.22E-02	5.36E-02	1.20E-02	2.08E-02		100.0%
M9-M2-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	9.81E-02	2.75E-02	3.53E-02	2.99E-02	5.71E-03	1.21E-02		100.0%
M9-M2-OD	0.126	2	0.1818	1.944	5.74E-02	1.08E-01	1.28E-03	4.19E-02	7.79E-03	1.70E-02	6.31E-02	1.20E-02	2.55E-02	100.0%
M9-M3-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.26E-01	8.41E-02	3.62E-02	2.14E-02	7.41E-03	1.69E-02	9.36E-03	3.75E-03	97.8%
M9-M3-OD	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.07E-02	1.31E-02	5.74E-03	3.68E-03	2.59E-03	1.04E-03	7.75E-04	94.1%
M9-M4-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.31E-01	9.70E-02	2.45E-02	1.16E-02	6.45E-03	1.83E-03	7.56E-04	5.39E-04	95.2%
M9-M4-OD	0.126	2	0.1818	1.944	5.74E-02	7.73E-02	6.63E-03	5.16E-02	7.37E-03	2.21E-02	1.10E-02	1.34E-03	4.81E-03	98.1%
M9-M5-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.21E-02	7.55E-03	2.74E-03	2.40E-03	3.38E-03	1.19E-03	1.10E-03	93.0%
M9-M5-OD	0.126	2	0.1818	1.944	5.74E-02	6.57E-02	9.75E-03	3.03E-02	3.52E-03	1.34E-02	1.39E-02	1.52E-03	6.19E-03	96.9%
M9-M6-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.07E-02	8.78E-03	3.42E-03	2.68E-03	3.20E-03	1.19E-03	1.01E-03	93.2%
M9-M6-OD	0.126	2	0.1818	1.944	5.74E-02	6.83E-02	8.65E-03	3.58E-02	4.39E-03	1.57E-02	1.35E-02	1.52E-03	5.98E-03	97.5%
M9-M7-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.25E-02	4.99E-03	1.66E-03	1.67E-03	4.92E-03	1.65E-03	1.64E-03	92.8%
M9-M7-OD	0.126	2	0.1818	1.944	5.74E-02	6.33E-02	1.09E-02	1.96E-02	2.14E-03	8.73E-03	1.96E-02	2.12E-03	8.75E-03	96.3%
M9-M8-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.22E-02	6.76E-03	2.43E-03	2.16E-03	3.91E-03	1.38E-03	1.26E-03	93.0%
M9-M8-OD	0.126	2	0.1818	1.944	5.74E-02	6.49E-02	9.84E-03	2.72E-02	3.13E-03	1.21E-02	1.61E-02	1.77E-03	7.18E-03	97.1%
M9-M9-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.25E-02	4.99E-03	1.66E-03	1.67E-03	4.92E-03	1.65E-03	1.64E-03	92.8%
M9-M9-OD	0.126	2	0.1818	1.944	5.74E-02	6.33E-02	1.09E-02	1.96E-02	2.14E-03	8.73E-03	1.96E-02	2.12E-03	8.75E-03	96.3%
M9-M10-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.22E-02	5.47E-03	1.89E-03	1.79E-03	4.77E-03	1.65E-03	1.56E-03	92.9%
M9-M10-OD	0.126	2	0.1818	1.944	5.74E-02	6.41E-02	1.04E-02	2.18E-02	2.43E-03	9.70E-03	1.94E-02	2.12E-03	8.62E-03	96.8%
M9-M11-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.24E-02	4.22E-03	1.39E-03	1.42E-03	6.08E-03	2.05E-03	2.02E-03	92.8%
M9-M11-OD	0.126	2	0.1818	1.944	5.74E-02	6.46E-02	1.09E-02	1.65E-02	1.79E-03	7.34E-03	2.39E-02	2.63E-03	1.06E-02	96.2%
M9-M12-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.21E-02	4.58E-03	1.54E-03	1.52E-03	5.95E-03	2.05E-03	1.95E-03	92.8%
M9-M12-OD	0.126	2	0.1818	1.944	5.74E-02	6.51E-02	1.06E-02	1.80E-02	1.98E-03	8.02E-03	2.37E-02	2.63E-03	1.05E-02	96.6%
M9-M13-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.22E-02	5.47E-03	1.89E-03	1.79E-03	4.77E-03	1.65E-03	1.56E-03	92.9%
M9-M13-OD	0.126	2	0.1818	1.944	5.74E-02	6.41E-02	1.04E-02	2.18E-02	2.43E-03	9.70E-03	1.94E-02	2.12E-03	8.62E-03	96.8%
M9-M14-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.23E-02	3.67E-03	1.19E-03	1.24E-03	8.02E-03	2.70E-03	2.66E-03	91.8%
M9-M14-OD	0.126	2	0.1818	1.944	5.74E-02	7.06E-02	1.15E-02	1.41E-02	1.53E-03	6.29E-03	3.09E-02	3.47E-03	1.37E-02	96.4%
M9-M15-FOX	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.28E-02	3.94E-03	1.31E-03	1.32E-03	7.89E-03	2.70E-03	2.60E-03	91.9%
M9-M15-OD	0.126	2	0.1818	1.944	5.74E-02	7.08E-02	1.13E-02	1.53E-02	1.68E-03	6.79E-03	3.06E-02	3.47E-03	1.36E-02	96.7%
M9-M16-FOX	0.378	0.378	0.4265	0.3295	2.17E-02	3.22E-01	1.29E-01	5.81E-03	2.97E-03	1.42E-03	5.05E-02	2.82E-02	1.11E-02	97.5%
M9-M16-OD	0.378	2	0.4318	1.946	1.86E-02	1.62E-01	2.03E-02	1.45E-02	3.00E-03	5.76E-03	1.05E-01	2.86E-02	3.82E-02	98.6%
M9-M17-FOX	0.378	0.378	0.4265	0.3295	2.17E-02	3.22E-01	1.29E-01	6.22E-03	3.19E-03	1.51E-03	5.03E-02	2.82E-02	1.10E-02	97.6%
M9-M17-OD	0.378	2	0.4318	1.946	1.86E-02	1.63E-01	2.01E-02	1.56E-02	3.23E-03	6.16E-03	1.05E-01	2.86E-02	3.81E-02	98.7%
M9-M1-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.35E-01	9.50E-02	3.43E-02	1.72E-02	8.55E-03	1.77E-03	7.56E-04	5.08E-04	96.1%
M9-M1-PO1(FOX)	0.108	2	0.1538	1.954	7.80E-02	1.21E-01	2.54E-03	1.08E-01	2.29E-02	4.26E-02	6.64E-03	1.01E-03	2.82E-03	99.4%
M9-M2-PO1(OD)	0.108	0.108	0.1155	0.1005	1.15E-01	2.36E-01	9.44E-02	3.69E-02	1.87E-02	9.09E-03	1.76E-03	7.56E-04	5.03E-04	96.2%
M9-M2-PO1(FOX)	0.108	2	0.1538	1.954	7.80E-02	1.25E-01	2.42E-03	1.13E-01	2.49E-02	4.39E-02	6.50E-03	1.01E-03	2.75E-03	99.4%
M9-M3-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	1.45E-02	6.60E-03	3.96E-03	2.52E-03	1.04E-03	7.41E-04	94.4%
M9-M3-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	8.04E-02	6.05E-03	5.63E-02	8.48E-03	2.39E-02	1.06E-02	1.34E-03	4.65E-03	98.3%
M9-M4-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.04E-02	1.48E-02	6.77E-03	4.02E-03	2.51E-03	1.04E-03	7.33E-04	94.4%
M9-M4-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	8.10E-02	5.95E-03	5.72E-02	8.70E-03	2.42E-02	1.06E-02	1.34E-03	4.62E-03	98.3%
M9-M5-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.16E-02	9.30E-03	3.71E-03	2.80E-03	3.14E-03	1.19E-03	9.76E-04	93.4%
M9-M5-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	6.93E-02	8.22E-03	3.80E-02	4.76E-03	1.66E-02	1.33E-02	1.52E-03	5.89E-03	97.7%
M9-M6-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.19E-02	9.40E-03	3.76E-03	2.82E-03	3.13E-03	1.19E-03	9.71E-04	93.5%
M9-M6-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	6.95E-02	8.15E-03	3.84E-02	4.83E-03	1.68E-02	1.33E-02	1.52E-03	5.88E-03	97.7%
M9-M7-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.10E-01	9.22E-02	7.04E-03	2.58E-03	2.23E-03	3.85E-03	1.38E-03	1.24E-03	93.0%
M9-M7-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	6.54E-02	9.57E-03	2.85E-02	3.31E-03	1.26E-02	1.60E-02	1.77E-03	7.12E-03	97.3%
M9-M8-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.18E-02	7.09E-03	2.60E-03	2.24E-03	3.84E-03	1.38E-03	1.23E-03	93.0%
M9-M8-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	6.55E-02	9.53E-03	2.87E-02	3.34E-03	1.27E-02	1.60E-02	1.77E-03	7.11E-03	97.3%
M9-M9-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.21E-02	5.66E-03	1.97E-03	1.84E-03	4.72E-03	1.65E-03	1.54E-03	92.9%
M9-M9-PO1(FOX)	0.126	2	0.1818	1.944	5.74E-02	6.53E-02	1.02E-02	2.27E-02	2.54E					

Structure	(as drawn)		(after process bias)												
	width	space	width	space	Rs	Ctotal	Cc	Cbottom	Cap	Cfb	Ctop	Cat	Cft	Csum/Ctotal	
	(um)	(um)	(um)	(um)	(Ohm/□)	(fF/um)									
PO1(OD)															
M9-M7-PO1(FOX)	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.28E-02	4.05E-03	1.35E-03	1.35E-03	7.84E-03	2.70E-03	2.57E-03	91.9%	
M9-M8-PO1(OD)	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.28E-02	4.05E-03	1.35E-03	1.35E-03	7.84E-03	2.70E-03	2.57E-03	91.9%	
M9-M8-PO1(FOX)	0.378	0.378	0.4265	0.3295	2.17E-02	3.22E-01	1.29E-01	6.36E-03	3.27E-03	1.54E-03	5.03E-02	2.82E-02	1.10E-02	97.6%	
M9-M8-PO1(OD)	0.378	0.378	0.4265	0.3295	2.17E-02	3.22E-01	1.29E-01	6.38E-03	3.29E-03	1.55E-03	5.03E-02	2.82E-02	1.10E-02	97.6%	
M9-M2-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.47E-02	3.90E-02	2.14E-02	8.80E-03	2.25E-03	1.04E-03	6.04E-04	96.6%	
M9-M3-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.05E-02	1.34E-02	6.06E-03	3.67E-03	2.86E-03	1.19E-03	8.37E-04	94.3%	
M9-M4-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.13E-02	8.78E-03	3.53E-03	2.62E-03	3.58E-03	1.38E-03	1.10E-03	93.4%	
M9-M5-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.17E-02	6.67E-03	2.49E-03	2.09E-03	4.47E-03	1.65E-03	1.41E-03	93.1%	
M9-M6-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.17E-02	5.29E-02	7.79E-03	2.26E-02	1.22E-02	1.52E-03	5.33E-03	98.4%	
M9-M7-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.27E-02	4.53E-03	1.57E-03	1.48E-03	7.64E-03	2.70E-03	2.47E-03	92.0%	
M9-M8-M1	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.25E-02	4.73E-02	3.20E-03	1.21E-02	1.88E-02	2.12E-03	8.33E-03	97.6%	
M9-M6-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.17E-02	5.38E-03	1.92E-03	1.73E-03	5.68E-03	2.05E-03	1.82E-03	93.0%	
M9-M7-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.27E-02	4.53E-03	1.57E-03	1.48E-03	7.64E-03	2.70E-03	2.47E-03	92.0%	
M9-M8-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.49E-02	3.88E-02	2.14E-02	8.71E-03	2.53E-03	1.19E-03	6.74E-04	96.6%	
M9-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.04E-02	1.32E-02	6.06E-03	3.54E-03	3.25E-03	1.38E-03	9.34E-04	94.3%	
M9-M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.25E-02	6.62E-02	2.73E-02	3.20E-03	1.21E-02	1.88E-02	2.12E-03	8.33E-03	97.6%
M9-M6-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.17E-02	5.38E-03	1.92E-03	1.73E-03	5.68E-03	2.05E-03	1.82E-03	93.0%	
M9-M7-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.19E-02	5.20E-03	1.92E-03	1.69E-03	5.68E-03	2.05E-03	1.82E-03	93.0%	
M9-M8-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.21E-02	5.20E-03	1.92E-03	1.69E-03	5.68E-03	2.05E-03	1.82E-03	93.0%	
M9-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.46E-02	3.86E-02	2.14E-02	8.59E-03	2.91E-03	1.38E-03	7.66E-04	96.7%	
M9-M5-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.23E-02	5.20E-03	1.92E-02	3.92E-02	1.10E-02	1.77E-03	6.08E-03	98.6%	
M9-M6-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.05E-02	8.58E-03	3.53E-03	2.52E-03	4.15E-03	1.65E-03	1.25E-03	93.5%	
M9-M7-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.27E-02	4.53E-03	1.57E-03	1.48E-03	7.64E-03	2.70E-03	2.47E-03	92.0%	
M9-M8-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.49E-02	3.88E-02	2.14E-02	8.71E-03	2.53E-03	1.19E-03	6.74E-04	96.6%	
M9-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.04E-02	1.32E-02	6.06E-03	3.54E-03	3.25E-03	1.38E-03	9.34E-04	94.3%	
M9-M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.19E-02	5.30E-03	1.92E-03	1.69E-03	5.73E-03	2.70E-03	2.33E-03	92.1%	
M9-M6-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.26E-02	4.01E-02	2.13E-02	4.27E-03	9.41E-03	2.97E-02	3.47E-03	1.31E-02	97.9%
M9-M7-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.16E-02	4.32E-03	1.92E-03	4.97E-02	2.82E-02	1.07E-02	97.8%		
M9-M8-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.29E-02	4.29E-03	1.92E-03	4.37E-03	8.11E-03	1.04E-01	2.86E-02	3.79E-02	99.1%
M9-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.46E-02	3.86E-02	2.14E-02	8.59E-03	2.91E-03	1.38E-03	7.66E-04	96.7%	
M9-M5-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.21E-02	5.06E-03	1.92E-02	3.92E-02	1.10E-02	1.77E-03	4.59E-03	99.5%	
M9-M6-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	1.30E-02	6.06E-03	3.45E-03	3.79E-03	1.65E-03	1.07E-03	94.4%	
M9-M7-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.28E-02	5.17E-02	1.77E-02	3.79E-03	2.20E-02	1.63E-02	2.12E-03	7.87E-03	98.2%
M9-M8-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.06E-02	6.50E-03	2.49E-03	2.01E-03	5.38E-03	2.05E-03	1.67E-03	93.2%	
M9-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.09E-02	8.35E-03	3.53E-03	2.41E-03	4.98E-03	2.05E-03	1.47E-03	93.6%	
M9-M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.19E-02	5.30E-03	1.92E-03	1.69E-03	5.73E-03	2.70E-03	2.33E-03	92.1%	
M9-M6-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.26E-02	4.01E-02	2.13E-02	4.27E-03	9.41E-03	2.97E-02	3.47E-03	1.31E-02	97.9%
M9-M7-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.16E-02	4.32E-03	1.92E-03	4.97E-02	2.82E-02	1.07E-02	97.8%		
M9-M8-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.29E-02	4.29E-03	1.92E-03	4.37E-03	8.11E-03	1.04E-01	2.86E-02	3.79E-02	99.1%
M9-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.46E-02	3.86E-02	2.14E-02	8.59E-03	2.91E-03	1.38E-03	7.66E-04	96.7%	
M9-M5-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.21E-02	5.06E-03	1.92E-02	3.92E-02	1.10E-02	1.77E-03	4.59E-03	99.5%	
M9-M6-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	1.30E-02	6.06E-03	3.45E-03	3.79E-03	1.65E-03	1.07E-03	94.4%	
M9-M7-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.28E-02	5.17E-02	1.77E-02	3.79E-03	2.20E-02	1.63E-02	2.12E-03	7.87E-03	98.2%
M9-M8-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.06E-02	6.50E-03	2.49E-03	2.01E-03	5.38E-03	2.05E-03	1.47E-03	93.6%	
M9-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.09E-02	3.50E-02	4.54E-03	1.52E-02	2.15E-02	2.63E-03	9.44E-03	98.6%	
M9-M5-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.19E-02	5.30E-03	1.92E-02	3.92E-02	1.10E-02	1.77E-03	4.59E-03	99.5%	
M9-M6-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.27E-02	5.20E-02	3.20E-03	1.15E-02	2.89E-02	3.47E-03	1.27E-02	98.4%	
M9-M7-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	9.30E-02	5.20E-02	3.23E-03	4.94E-02	2.82E-02	1.06E-02	98.0%		
M9-M8-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.17E-01	9.22E-02	4.82E-02	3.24E-03	1.82E-02	4.30E-02	1.04E-01	2.86E-02	3.79E-02	99.4%
M9-M4-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.18E-01	8.46E-02	3.85E-02	2.14E-02	8.51E-03	2.38E-02	1.21E-02	2.12E-03	98.9%	
M9-M5-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.13E-01	9.21E-02	5.06E-03	1.92E-02	3.92E-02	1.10E-02	1.77E-03	4.59E-03	99.5%	
M9-M6-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.09E-01	9.02E-02	1.30E-02	6.06E-03	3.45E-03	3.79E-03	1.65E-03	1.07E-03	94.4%	
M9-M7-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.15E-01	9.28E-02	5.17E-02	1.77E-02	3.79E-03	2.20E-02	1.63E-02	2.12E-03	7.87E-03	98.2%
M9-M8-M3	0.126	0.126	0.1415	0.1105	1.00E-01	2.07E-01	9.06E-02	6.50E-03	2.49E-03	2.01E-03	5.38E-03	2.05E-03	1.47E-03	93.6%	
M9-M4-M2	0.126	0.126	0.1415	0.1105	1.00E-01	2.19E-01	8.09E-02	3.50E-02	4.54E-03	1.52E-02	2.15E-02	2.63E-03	9.44E-03	98.6%	
M9-M5-M2	0.126	0.126	0.1415	0.1105	1.0										

## 13.17 MIM Capacitor Model

### 13.17.1 Model Usage Guide

Metal-insulator-metal (MiM) capacitor with and without underground metal was modeled based on the two-port S-parameter measurement and Y-parameter fitting. There are two model options in the capacitance density, namely 1.0fF/um<sup>2</sup>, 1.5fF/um<sup>2</sup> and 2.0fF/um<sup>2</sup> for different process with and without underground metal that can be used for metal layer from four to nine. As for MiM capacitor with UTM direct contact (UDC), process can be used for metal layer from four to eight. Designers need to select only one type of density for their design based on their requirement respectively.

Square and rectangular capacitors of different sizes (W\*L): 5x5, 10x10, 20x20, 30x30, 100x100, 10x50, and 10x100 were measured and fitted. MIM capacitor scalable models were generated with minimum length (L) and width (W) at 4μm and the maximum length and width at 100μm where length is always higher than or equal to width.

### 13.17.2 Test Structure and Measurement Procedures

Layout of the MIM structures is as shown in Fig. 13.17.2.1 and 13.17.2.2. It is designed as a two-port network with underground metal connected to ground for MIM capacitor. Two-port S parameter was performed with frequency sweep from 200 MHz to 30.0 GHz. Open and short test structure measurements are used as RF deembedding for each MIM.

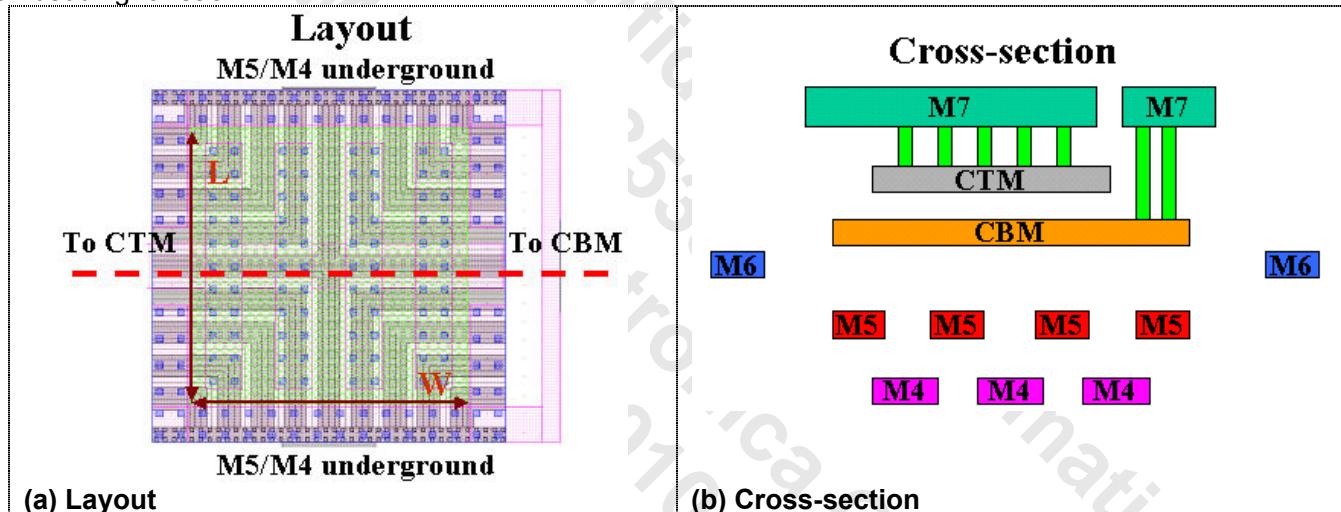


Fig. 13.17.2.1: (a) Layout and (b) its Cross-section of MIMcap with underground metal

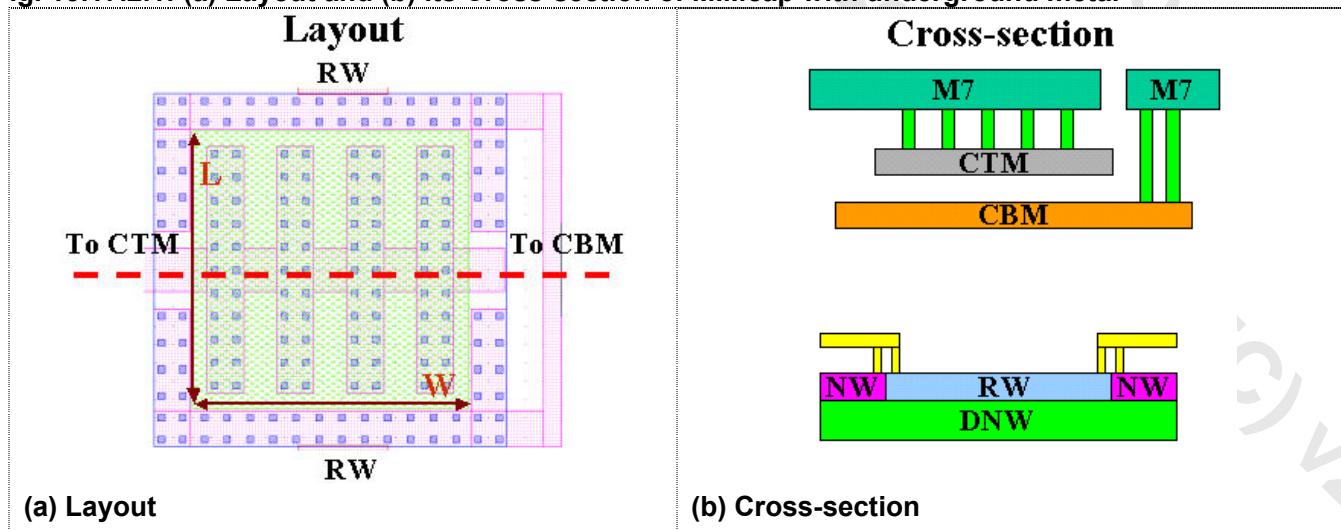


Fig. 13.17.2.2: (a) Layout and (b) its Cross-section of MiMcap without underground metal

### 13.17.3 Equivalent Circuit Model

The equivalent circuit model for the MIM with underground metal capacitor structure is shown in Fig. 13.17.3.1 and 13.17.3.2. Description of the equivalent circuit is summarized below:

The inter-metal dielectric  $C_{mim}$  models the main element of the capacitor.

$R_{top}$  and  $L_{top}$  are the parasitics existing in the electrode connected to port 1(Top)

$R_{bot}$  and  $L_{bot}$  are the parasitics existing in the electrode connected to port 2(Bottom)

$C_{ox}$  of MIM represents the capacitance between port2 bottom-plate metal to underground metal.

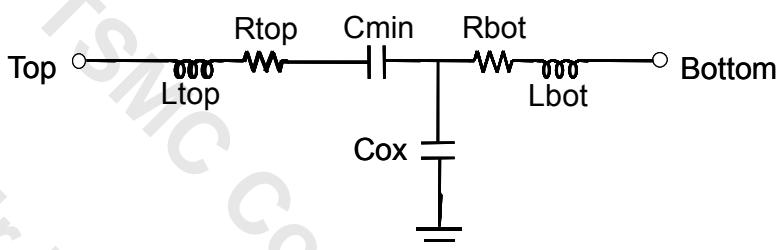


Fig. 13.17.3.1: Equivalent circuit of the MIM with underground metal structure

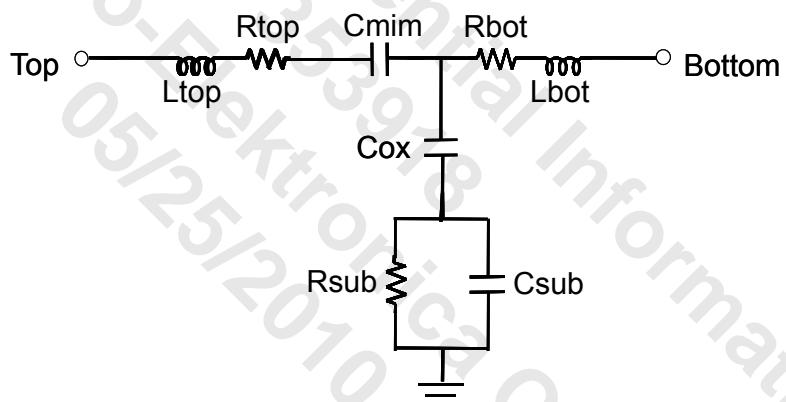


Fig. 13.17.3.2: Equivalent circuit of the MIM without underground metal structure

## 13.17.4 Model Details

### 13.17.4.1 Scaling Rule

The scaling equations for the various elements R, L and C are empirically determined and shown in Table 13.17.4.1.1 and 13.17.4.1.2

**Table 13.17.4.1.1 Sub-circuit elements for MIMCAP with and without underground metal.**

Component	Scaling Rule
$L_{top}$ (H)	$l_{top\_para}$
$R_{top}$ ( $\Omega$ )	$r_{top\_para} tc1 = 3e-3$
$C_{mim}$ (F)	$1.5fF \Rightarrow cmim\_para \cdot (1+v(n2,n3) \cdot -3.33e-5 + (abs(v(n2,n3))^2) \cdot -2.92e-5)$ $2.0fF \Rightarrow cmim\_para \cdot (1+v(n2,n3) \cdot -1.014e-5 + (abs(v(n2,n3))^2) \cdot -2.9674e-5)$
$R_{bot}$ ( $\Omega$ )	$r_{bot\_para} tc1 = 3e-3$
$L_{bot}$ (H)	$l_{bot\_para}$
$C_{ox}$ (F)	$cox\_para$
where,	
$l_{top\_para}$	$((0.24 \cdot (wt \cdot 1e6) \cdot (\log((wt \cdot 1e6) / (lt \cdot 1e6 + 0.05))) + 1.19 + 0.022 \cdot (lt \cdot 1e6 + 0.05) / (wt \cdot 1e6)) / 1 + 1.5) / (3 + 1.78) \cdot 1e-12$
$l_{bot\_cbm}$	$((0.24 \cdot (wt \cdot 1e6 + 3.52) \cdot (\log((wt \cdot 1e6 + 3.52) / ((lt \cdot 1e6 + 3.52) + 0.2))) + 1.19 + 0.022 \cdot ((lt \cdot 1e6 + 3.52) + 0.2) / (wt \cdot 1e6 + 3.52)) / 1 + 1.5) / 3 \cdot 1e-12$
$l_{bot\_lead}$	$((0.606 + 0.24 \cdot ((lt \cdot 1e6 + 3.52) / 2) \cdot (\log(((lt \cdot 1e6 + 3.52) / 2) / (1 + 0.85))) + 1.19 + 0.022 \cdot (1 + 0.85) / ((lt \cdot 1e6 + 3.52) / 2)) / 1 + 1.5) / 2 \cdot 1e-12$
$l_{bot\_para}$	$(l_{bot\_cbm} + l_{bot\_lead})$
$via\_v$	$int((lt \cdot 1e6 / 2 - 1.253) / (0.927) + 1)$
$res\_v$	$(via\_v - 1) \cdot (2 \cdot via\_v - 1) / (6 \cdot via\_v) \cdot 0.009138 + 23.975 / via\_v$
$via\_h$	$int((wt \cdot 1e6 - 2.76) / (2.41) + 1)$
$r_{top\_para}$	$(0.067499195 + (via\_h - 1) \cdot (2 \cdot via\_h - 1) / (6 \cdot via\_h) \cdot 0.009970339 + res\_v / 2 / via\_h + 0.1)$
$r1$	$(lt \cdot 1e6 + 0.2) / 2 / (wt \cdot 1e6 + 0.2) \cdot 0.257 / 3$
$r3$	$(wt \cdot 1e6 + 0.2) / 2 / (lt \cdot 1e6 + 0.2) \cdot 0.257 / 3$
$rcbm$	$(1 / (2 / r1 + 2 / r3))$
$via\_left$	$int(((wt \cdot 1e6 + 3.52) - 0.83 + ((lt \cdot 1e6 + 3.52) / 2 - 2.85)) - 0.76) / (0.93) + 1$
$res\_left$	$0.00283494 + (via\_left - 1) \cdot (2 \cdot via\_left - 1) / (6 \cdot via\_left) \cdot 0.008079578 + 0.6625 / via\_left$
$via\_vert$	$int(((lt \cdot 1e6 + 3.52) / 2 - 2.85) - 0.76) / (0.93) + 1$
$res\_vert$	$0.00283494 + (via\_vert - 1) \cdot (2 \cdot via\_vert - 1) / (6 \cdot via\_vert) \cdot 0.008079578 + 0.6625 / via\_vert$
$res\_cbm$	$1 / (1 / res\_left + 1 / res\_vert)$
$res\_lead$	$(1.6 / 1.66 + (lt \cdot 1e6 + 3.52) / 2 / 1) \cdot 0.02353$
$res\_upper$	$res\_cbm + res\_lead$
$r_{bot\_para}$	$(res\_upper / 2 + rcbm + 0.1)$
$cmim\_para$	$1.5fF \Rightarrow (((wt - 0.083u) \cdot (lt - 0.083u) \cdot 1e12 \cdot 1.575) + 2 \cdot ((wt - 0.083u) + (lt - 0.083u)) \cdot 1e6 \cdot 0.183 + 0.188 \cdot 1e-15 \cdot (1 + (temper - 25) \cdot -5.13e-5 + (temper - 25) \cdot (temper - 25) \cdot 0)$ , where $-0.083um$ is a electrical offset. $2.0fF \Rightarrow (((wt - 0.057u) \cdot (lt - 0.057u) \cdot 1e12 \cdot 2.029) + 2 \cdot ((wt - 0.057u) + (lt - 0.057u)) \cdot 1e6 \cdot 0.203 + 0.178 \cdot 1e-15 \cdot (1 + (temper - 25) \cdot -1.189e-5 + (temper - 25) \cdot (temper - 25) \cdot -0.004e-6)$ , where $-0.057um$ is a electrical offset.
$cox\_para$	$((lt \cdot 1e6 + 3.52) \cdot (wt \cdot 1e6 + 3.52) \cdot 0.056595238 + 0.05472 + (lt \cdot 1e6 + 3.52) \cdot 0.007125) \cdot 0.65 \cdot 1e-15$ : MIMcap with underground metal $((lt \cdot 1e6 + 3.52) \cdot (wt \cdot 1e6 + 3.52) \cdot 0.00908 + 0.05472 + (lt \cdot 1e6 + 3.52) \cdot 0.007125) \cdot 1e-15$ : For MIMcap without underground metal
$r_{sub\_para}$	$(1 / (2 / ((lt \cdot 1e6 + 3.52) / 2 / (wt \cdot 1e6 + 3.52) * 1100 / 3) + 2 / ((wt \cdot 1e6 + 3.52) / 2 / ((lt \cdot 1e6 + 3.52) * 1100 / 3))) * (-0.0000114365 * (temper - 25) * (temper - 25) + 0.0045985091 * (temper - 25) + 1)$ : For MIMcap without underground metal
$c_{sub\_para}$	$(312 / r_{sub\_para}) * 1e-15$ : For MIMcap without underground metal

Table 13.17.4.1.2: Sub-circuit elements for UDC MIMCAP with and without underground metal.

Component	Scaling Rule
$L_{top}$ (H)	$I_{top\_para}$
$R_{top}$ ( $\Omega$ )	$r_{top\_para} \text{ tc1} = 3e-3$
$C_{mim}$ (F)	$1.5fF \Rightarrow cmim\_para \cdot (1+v(n2,n3) \cdot -3.33e-5 + (\text{abs}(v(n2,n3))^2) \cdot -2.92e-5)$ $2.0fF \Rightarrow cmim\_para \cdot (1+v(n2,n3) \cdot -1.014e-5 + (\text{abs}(v(n2,n3))^2) \cdot -2.9674e-5)$
$R_{bot}$ ( $\Omega$ )	$r_{bot\_para} \text{ tc1} = 3e-3$
$L_{bot}$ (H)	$I_{bot\_para}$
$C_{ox}$ (F)	$cox\_para$
where,	
$I_{top\_para}$	$((0.24 \cdot (wt \cdot 1e6) \cdot (\log((wt \cdot 1e6) / (lt \cdot 1e6 + 0.05)) + 1.19 + 0.022 \cdot (lt \cdot 1e6 + 0.05) / (wt \cdot 1e6)) / 1 + 1.5) / (3 + 1.78) \cdot 1e-12)$
$I_{bot\_cbm}$	$((0.24 \cdot (wt \cdot 1e6 + 3.52) \cdot (\log((wt \cdot 1e6 + 3.52) / ((lt \cdot 1e6 + 3.52) + 0.2)) + 1.19 + 0.022 \cdot ((lt \cdot 1e6 + 3.52) + 0.2) / (wt \cdot 1e6 + 3.52)) / 1 + 1.5) / 3 \cdot 1e-12$
$I_{bot\_lead}$	$((0.606 + 0.24 \cdot ((lt \cdot 1e6 + 3.52) / 2) \cdot (\log(((lt \cdot 1e6 + 3.52) / 2) / (1 + 0.85)) + 1.19 + 0.022 \cdot (1 + 0.85) / ((lt \cdot 1e6 + 3.52) / 2)) / 2 \cdot 1e-12)$
$I_{bot\_para}$ $via\_v$	$(I_{bot\_cbm} + I_{bot\_lead})$ $\text{int}((lt \cdot 1e6 / 2 - 1.253) / (0.927) + 1)$
$res\_v$	$(via\_v - 1) \cdot (2 \cdot via\_v - 1) / (6 \cdot via\_v) \cdot 0.00134379 + 16.975 / via\_v$
$via\_h$	$\text{int}((wt \cdot 1e6 - 6) / (4.6) + 2)$
$r_{top\_para}$	$(0.016308 + (via\_h - 1) \cdot (2 \cdot via\_h - 1) / (6 \cdot via\_h) \cdot 0.004016 + res\_v / 2 / via\_h + 0.12)$
$r1$	$(lt \cdot 1e6 + 3.92) / 2 / (wt \cdot 1e6 + 3.92) \cdot 0.30304 / 3$
$r3$	$(wt \cdot 1e6 + 3.92) / 2 / (lt \cdot 1e6 + 3.92) \cdot 0.30304 / 3$
$rcbm$	$(1 / (2 / r1 + 2 / r3))$
$via\_left$	$\text{int}(((wt \cdot 1e6 + 8.04) - 1.03 + ((lt \cdot 1e6 + 8.04) / 2 - 4.21)) - 0.76) / (0.93) + 1$
$res\_left$	$0.000460194 + (via\_left - 1) \cdot (2 \cdot via\_left - 1) / (6 \cdot via\_left) \cdot 0.001311553 + 0.6035 / via\_left$
$via\_vert$	$\text{int}(((lt \cdot 1e6 + 8.04) / 2 - 4.21) - 0.76) / (0.93) + 1$
$res\_vert$	$0.000460194 + (via\_vert - 1) \cdot (2 \cdot via\_vert - 1) / (6 \cdot via\_vert) \cdot 0.001311553 + 0.6035 / via\_vert$
$res\_cbm$	$1 / (1 / res\_left + 1 / res\_vert)$
$res\_lead$	$(2 / 2.06 + (lt \cdot 1e6 + 8.04) / 2 / 2) \cdot 0.00474$
$res\_upper$	$res\_cbm + res\_lead$
$r_{bot\_para}$	$(res\_upper / 2 + rcbm + 0.12)$
$cmim\_para$	$1.5fF \Rightarrow (((wt - 0.076u) \cdot (lt - 0.076u) \cdot 1e12 \cdot 1.561) + 2 \cdot ((wt - 0.076u) + (lt - 0.076u)) \cdot 1e6 \cdot 0.547 + 0.180) \cdot 1e-15 \cdot (1 + (\text{temper} - 25)) \cdot -5.13e-5 + (\text{temper} - 25) \cdot (\text{temper} - 25) \cdot 0$ , where $-0.076um$ is a electrical offset. $2.0fF \Rightarrow (((wt - 0.079u) \cdot (lt - 0.079u) \cdot 1e12 \cdot 2.073) + 2 \cdot ((wt - 0.079u) + (lt - 0.079u)) \cdot 1e6 \cdot 0.239 + 0.203) \cdot 1e-15 \cdot (1 + (\text{temper} - 25)) \cdot -1.189e-5 + (\text{temper} - 25) \cdot (\text{temper} - 25) \cdot -0.004e-6$ , where $-0.079um$ is a electrical offset.
$cox\_para$	$((lt \cdot 1e6 + 8.04) \cdot (wt \cdot 1e6 + 8.04) \cdot 0.056595238 + 0.05472 + (lt \cdot 1e6 + 8.04) \cdot 0.007125) \cdot 0.65 \cdot 1e-15$ : For MIMcap with shield $((lt \cdot 1e6 + 8.04) \cdot (wt \cdot 1e6 + 8.04) \cdot 0.00908 + 0.05472 + (lt \cdot 1e6 + 8.04) \cdot 0.007125) \cdot 1e-15$ : For MIMcap without shield
$r_{sub\_para}$	$(1 / (2 / ((lt \cdot 1e6 + 8.04) / 2 / (wt \cdot 1e6 + 8.04) * 1100 / 3) + 2 / ((wt \cdot 1e6 + 8.04) / 2 / ((lt \cdot 1e6 + 8.04) * 1100 / 3))) * (-0.0000114365 * (\text{temper} - 25) * (\text{temper} - 25) + 0.0045985091 * (\text{temper} - 25) + 1)$ : For MIMcap without shielding
$c_{sub\_para}$	$(312 / r_{sub\_para}) * 1e-15$ : For MIMcap without shielding

### 13.17.4.2 Model Parameter

The values for equivalent circuit elements are shown in Table 13.17.4.2.1, 13.17.4.2.2 and 13.17.4.2.3.

**Table 13.17.4.2.1: Equivalent circuit parameters for MIMCAP with underground metal.**

Lt(μm)	5	10	20	30	100	50	100
Wt(μm)	5	10	20	30	100	10	10
L <sub>top</sub> (pH)	2.761	3.246	4.215	5.185	11.972	2.032	1.566
R <sub>top</sub> (Ω)	6.162	0.777	0.341	0.271	0.306	0.301	0.252
R <sub>bot</sub> (mΩ)	214.418	230.021	286.136	345.827	787.443	456.577	764.278
L <sub>bot</sub> (pH)	3.403	4.87	8.112	11.618	39.663	13.848	28.907
C <sub>ox</sub> (fF)	2.745	6.822	20.495	41.524	394.738	26.902	52.002

**Table 13.17.4.2.2: Equivalent circuit parameters for UDC 1.5fF and 2.0fF MIMCAP with underground metal.**

Lt(μm)	4	10	20	30	100	50	100
Wt(μm)	4	10	20	30	100	10	10
L <sub>top</sub> (pH)	2.164	2.746	3.715	4.685	11.472	1.537	1.066
R <sub>top</sub> (Ω)	8.624	0.986	0.311	0.225	0.172	0.303	0.223
R <sub>bot</sub> (mΩ)	164.22	159.57	162.31	167.24	210.81	171.21	198.84
L <sub>bot</sub> (pH)	4.422	6.294	9.670	13.265	41.605	15.417	30.467
C <sub>ox</sub> (fF)	5.424	12.091	20.089	53.444	429.94	38.822	72.235

**Table 13.17.4.2.3: Equivalent circuit parameters for UDC 1.5fF and 2.0fF MIMCAP without underground metal.**

Lt( μm)	10	20	30	100	50	100
Wt( μm)	10	20	30	100	10	10
L <sub>top</sub> (pH)	2.746	3.715	4.685	11.472	1.537	1.066
R <sub>top</sub> (Ω)	0.986	0.311	0.225	0.172	0.303	0.223
R <sub>bot</sub> (mΩ)	159.57	162.31	167.24	210.81	171.21	198.84
L <sub>bot</sub> (pH)	6.294	9.670	13.265	41.605	15.417	30.467
C <sub>ox</sub> (fF)	2.502	5.856	10.636	83.992	7.928	14.711
C <sub>sub</sub> (fF)	6.807	6.807	6.807	6.807	1.361	0.681
R <sub>sub</sub> (Ω)	45.833	45.833	45.833	45.833	229.167	458.333

### 13.17.4.3 Model Error Table

MIMCAP with and without underground metal fitting error between measurement and simulation are summarized in Table 13.17.4.3.1, 13.17.4.3.2, 13.17.4.3.3 and 13.17.4.3.4. For each device four Y-parameter fitting errors are separated with real part and imaginary part. According to the existing data of 1.5fF MiMcap with underground metal, we generate the 1.5fF MiMcap model without underground metal by using the substrate of UDC 1.5 fF MiMcap without underground metal. As for UDC 2.0fF MiMcap models with and without underground metal, they are generated on the basis of UDC 1.5fF MiMcap models with and without underground metal.

**Table 13.17.4.3.1: Fitting errors (Real and Imaginary) for MIMCAP with underground metal.**

W(μm)	4	10	25	50	100	50	100
L(μm)	4	10	25	50	100	10	10
Real(Y11)(%)	13.82	18.16	17.50	24.04	7.98	35.26	11.66
Real(Y21)(%)	6.87	20.46	17.27	24.69	7.25	34.71	10.88
Real(Y12)(%)	12.41	14.79	18.84	26.19	6.97	37.26	10.66
Real(Y22)(%)	10.34	16.27	18.52	26.82	6.24	36.46	9.90
Imag(Y11)(%)	0.20	0.11	0.70	2.96	6.29	3.40	7.55
Imag(Y21)(%)	0.40	0.14	0.79	3.23	6.65	3.85	6.88
Imag(Y12)(%)	0.88	0.26	0.82	3.24	6.53	3.91	6.99
Imag(Y22)(%)	0.28	0.29	0.85	3.52	6.86	4.15	6.30

**Table 13.17.4.3.2: Fitting errors (Real and Imaginary) for 2.0fF MIMCAP with underground metal.**

W(μm)	5	10	20	30	100	10	10
L(μm)	5	10	20	30	100	50	100
Real(Y11)(%)	3.82	18.56	23.93	17.82	16.70	9.67	18.37
Real(Y21)(%)	5.91	18.48	24.26	18.38	16.52	9.50	17.82
Real(Y12)(%)	7.04	16.63	25.56	18.61	16.18	9.40	17.69
Real(Y22)(%)	17.84	15.49	25.91	19.22	16.00	9.30	17.15
Imag(Y11)(%)	1.56	2.12	1.30	6.33	2.13	2.01	3.32
Imag(Y21)(%)	0.90	1.66	1.45	6.65	2.26	1.82	3.06
Imag(Y12)(%)	0.88	1.66	1.46	6.64	2.25	1.83	3.07
Imag(Y22)(%)	2.70	2.35	1.34	6.82	2.26	1.83	2.97

**Table 13.15.4.3.3: Fitting errors (Real and Imaginary) for UDC 1.5fF MIMCAP with underground metal.**

L(μm)	4	10	20	30	100	50	100
W(μm)	4	10	20	30	100	10	10
Real(Y11)(%)	48.51	11.49	17.15	20.73	22.68	28.04	7.40
Real(Y21)(%)	37.21	15.99	17.45	20.37	22.07	28.64	6.50
Real(Y12)(%)	38.06	14.81	17.67	20.36	21.75	29.06	6.27
Real(Y22)(%)	22.73	17.96	17.56	20.01	21.15	29.20	5.49
Imag(Y11)(%)	1.77	0.71	0.63	8.65	2.91	0.98	5.77
Imag(Y21)(%)	1.70	0.66	0.52	8.35	2.86	1.15	7.13
Imag(Y12)(%)	1.70	0.66	0.52	8.35	2.87	1.15	7.11
Imag(Y22)(%)	7.03	1.79	0.54	7.97	2.84	1.14	8.08

**Table 13.17.4.3.4: Fitting errors (Real and Imaginary) for UDC 1.5fF MIMCAP without underground metal.**

L(μm)	10	20	30	100	50	100
W(μm)	10	20	30	100	10	10
Real(Y11)(%)	10.87	20.21	16.99	8.02	24.62	24.99
Real(Y21)(%)	12.04	10.73	14.31	7.67	24.54	24.46
Real(Y12)(%)	11.52	13.19	18.16	7.57	25.04	24.26
Real(Y22)(%)	12.02	15.39	15.98	7.10	25.01	23.69
Imag(Y11)(%)	4.35	4.41	4.31	2.39	1.77	6.43
Imag(Y21)(%)	4.07	1.40	3.05	2.29	1.84	6.90
Imag(Y12)(%)	4.10	1.40	3.05	2.30	1.85	6.88
Imag(Y22)(%)	4.48	4.52	4.49	1.99	2.02	7.36

## 13.17.5 Corner Model Table

The skew parameters are listed below Table 13.17.5.1 for corner-case simulation.

Table 13.17.5.1: Corner Model Table for MIMCAP with and without underground metal.

Skew Parameter	SS	TT	FF
cm7_mimfac	1.08	1.0	0.926
rctm_mimfac	1.1	1.0	0.9
cmim_mimfac	1.1	1.0	0.9
cmim2p0_mimfac	1.15	1.0	0.85
cm5_mimfac	1.074	1.0	0.931
I_mimfac	1.0235	1.0	0.9762
rsub_mimfac	1.2	1.0	0.8
csub_mimfac	0.833	1.0	1.25

## 13.17.6 Temperature Effect Model

The temperature characteristics of capacitors are evaluated with  $20 \times 20 \mu\text{m}^2$ . The capacitance does not appear to change much with temperature ( $-40^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $125^\circ\text{C}$ ). However, the Q changes with temperature. It might be due to the temperature coefficient of the MIM resistance (TCR).

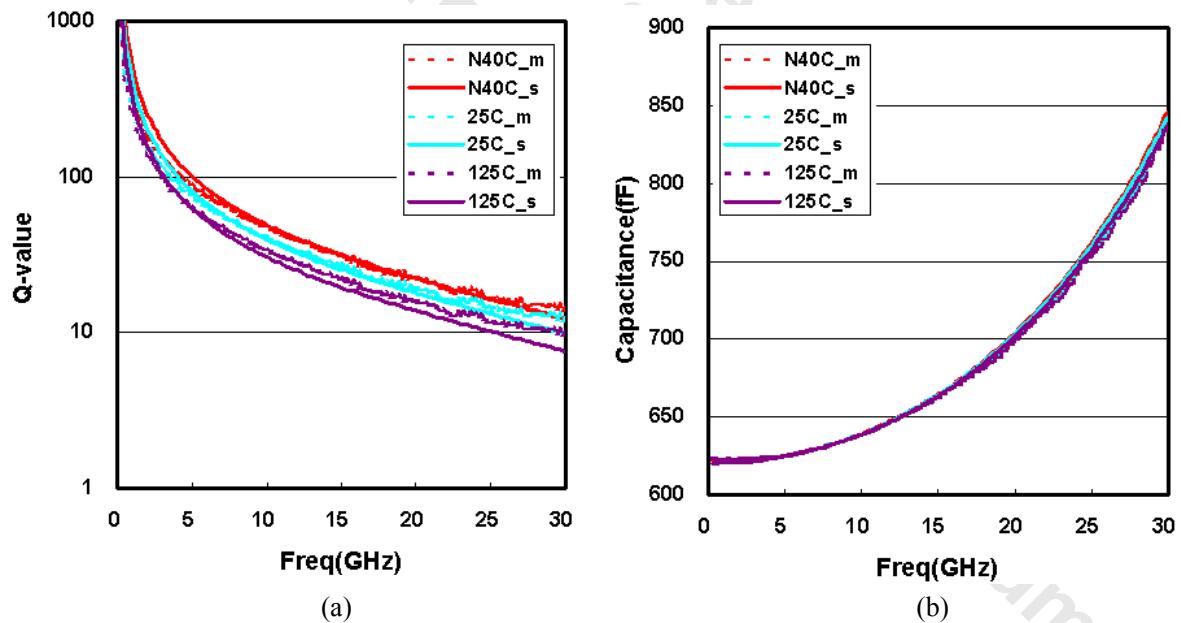


Fig. 13.17.6.1: MIM  $20 \times 20$  at  $125^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $-40^\circ\text{C}$  (a) Q , (b) C Plots

The TCR characteristics of capacitors are also evaluated with  $20 \times 20 \mu\text{m}^2$ . The resistance shows a linear dependence of the temperature ( $-40^\circ\text{C}$ ,  $25^\circ\text{C}$ ,  $125^\circ\text{C}$ ). The following functions have been implemented into the model for temperature effect simulation.

$$R_{top}(T) = R_{top} * (0.003 * (\text{temper} - 25) + 1)$$

$$R_{bot}(T) = R_{bot} * (0.003 * (\text{temper} - 25) + 1)$$

## 13.17.7 TCC and VCC

The VCC and TCC characteristics of capacitors are evaluated with  $20 \times 20 \times 12 \mu\text{m}^2$ . The capacitance shows a parabolic dependence of the DC bias voltage (-4V to 4V in steps of 0.5V) at  $25^\circ\text{C}$ , the  $V_{cc1} = -33.3 \text{ ppm/V}$ ,  $V_{cc2} = -29.2 \text{ ppm/V}^2$  for 1.5fF MiMCAP and the  $V_{cc1} = -10.14 \text{ ppm/V}$ ,  $V_{cc2} = -29.674 \text{ ppm/V}^2$  for 2.0fF MiMCAP. At 0 V bias different temperature, the  $T_{cc1}$  of the 1.5fF capacitors is  $-51.3 \text{ ppm/}^\circ\text{C}$   $T_{cc2} = -0.00 \text{ ppm/}^\circ\text{C}^2$  and the  $T_{cc1}$  of the 2.0fF capacitors is  $-11.89 \text{ ppm/}^\circ\text{C}$   $T_{cc2} = -0.004 \text{ ppm/}^\circ\text{C}^2$ . TCC and VCC characteristics of UDC MiMcap capacitors are close to the results of MiMcap capacitors, so that the value of TCC and VCC are the same in 1.5fF MiMcap or in 2.0fFMiMcap models.

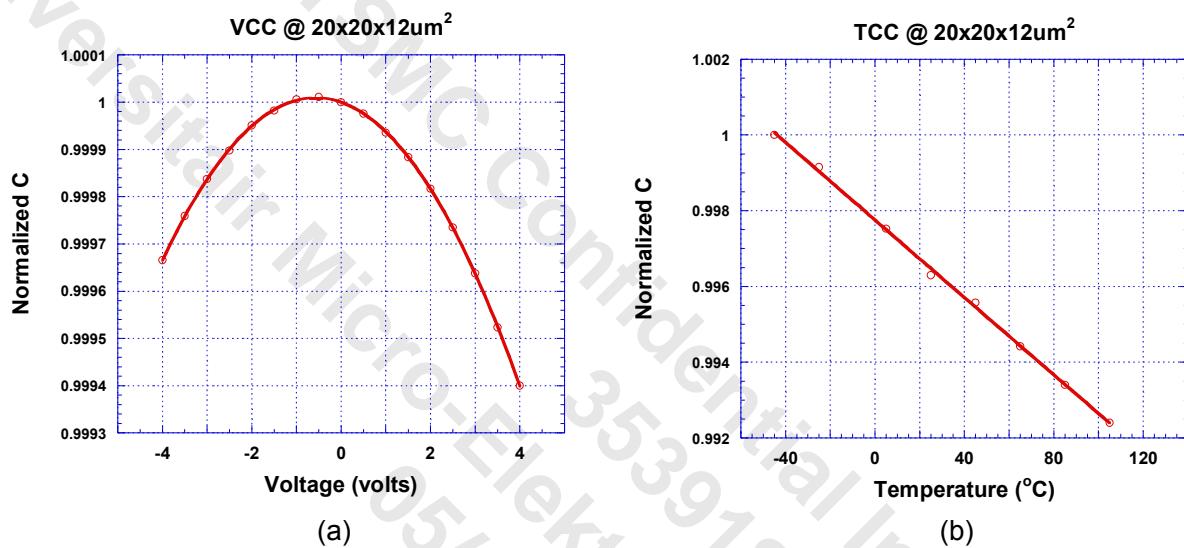


Fig. 13.17.7.1 (a) VCC , (b) TCC Plots of 1.5fF MIMCAP

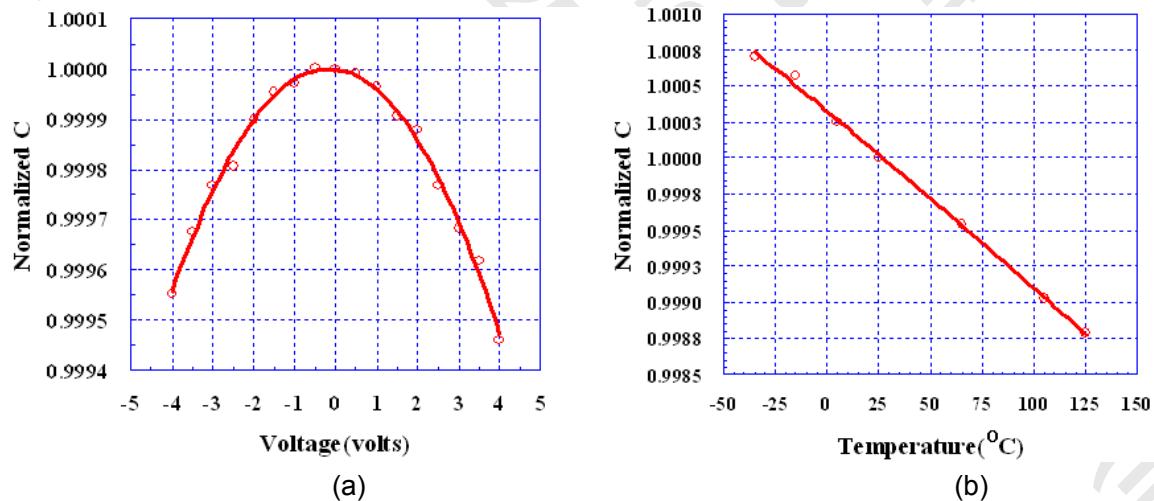


Fig. 13.17.7.2: (a) VCC , (b) TCC Plots of 2.0fF MIMCAP

1 Curve fitting of the measured C for VCC uses  $C(V) = C_0[1 + V_{cc1}(V) + V_{cc2}(V)^2]$ , where  $C_0$  is capacitance at 0V bias.

2 Curve fitting of the measured C for TCC uses  $C(T) = C(T_{nom})[1 + T_{cc1}(T - T_{nom}) + T_{cc2}(T - T_{nom})^2]$ , where  $T_{nom}$  is at  $25^\circ\text{C}$  and  $C(T_{nom})$  is capacitance at  $25^\circ\text{C}$ .

3 Measurements have been carried out using the HP 4284 LCR meter @100KHz.

## 13.17.8 Mismatch Model

The model for this technology has added the capability for mismatch analysis of an identical and closely spaced MIM pair. Random variations in Gaussian distribution of the total capacitance are included in the model to account for the mismatch performance. The designers will need to turn off (mismatchflag=0) or turn on (mismatchflag=1) in the macro model for nominal or Monte-Carlo analysis. The simulation results with the measured data are shown in Fig.13.17.8.1.

Statistical libraries for process (die to die ) variation are denoted by MC\_RFMIM and MC\_MIM for RF and baseband model respectively. The four sigma of the capacitance variation are 10% for the  $1.5\text{fF}/\mu\text{m}^2$  MIM and 15% for the  $2.0\text{fF}/\mu\text{m}^2$  MIM.

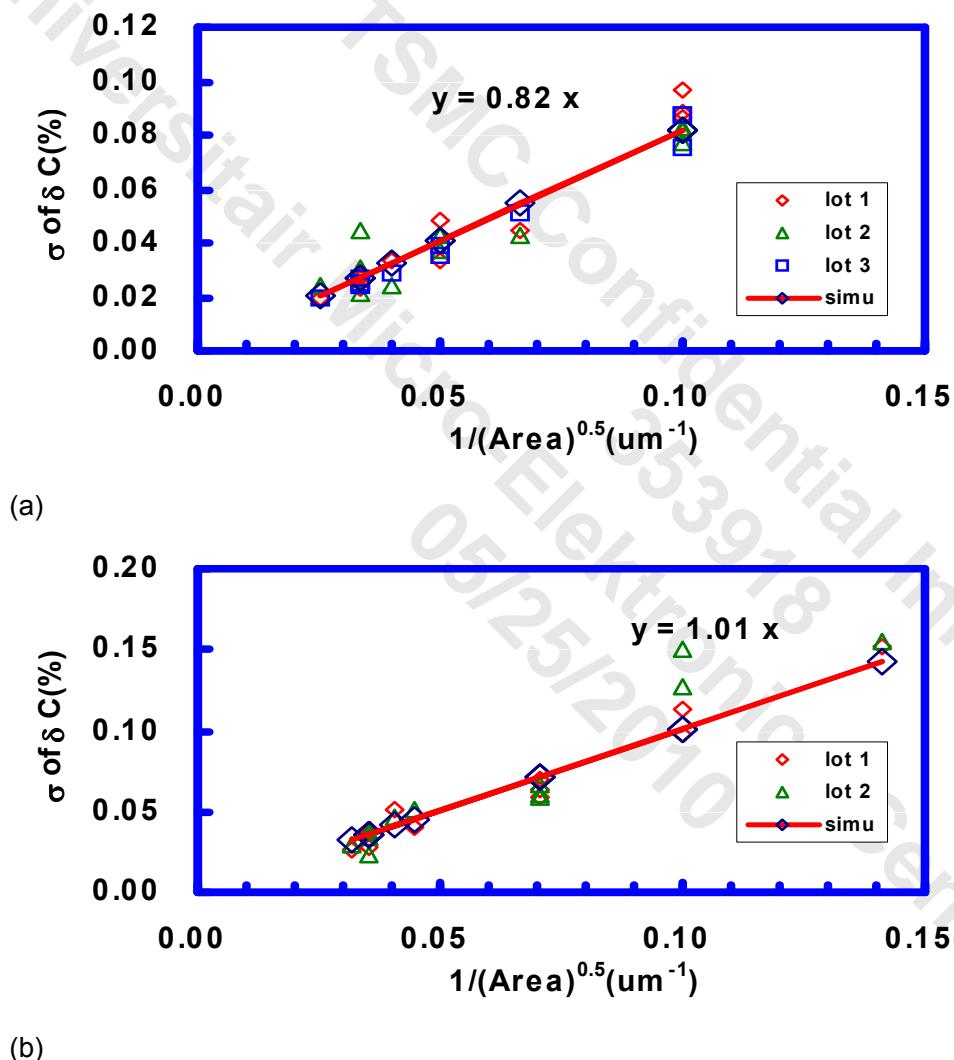


Fig. 13.17.8.1: Simulation results of 1000 Monte-Carlo random tests of  $\sigma 2^*(C_1 - C_2)/(C_1 + C_2)$  of the (a)  $1.5\text{fF}/\mu\text{m}^2$  MIM and (b)  $2.0\text{fF}/\mu\text{m}^2$  MIM.

## 13.18 RTMOM Capacitor Model

### 13.18.1 RF Model Usage Guide

Please refer to T-N90-CM-SP-001 for the baseband RTMOM. The rotative metal capacitor (RTMOM) with poly shield was modeled based on the two-port S-parameter measurement and Y-parameter fitting. NV, NH, spacing, and metal layer are the parameters of this scalable model, when its model range is list in the table 13.18.1.1. For this model, NV and NH are limited to be even number. The total layer number of metal is at least 3 layers stacked with ploy shield. Besides, designer can use “busflag” to decide the width of L-shape bus equals to 0.14um (busflag=0, default) or 0.23um (busflag=1).

Model	Model range
Valid NV number	6 ~ 288 (even fingers)
Valid NH number	6 ~ 288 (even fingers)
Valid spacing	0.14μm ~ 0.18μm
Valid width	0.14μm ~ 0.18μm
Start metal layer	M1,M2,M3,M4,M5
Stop metal layer	M3,M4,M5,M6,M7
TCC	from -40°C to 125°C
VCC	from -5V to 5V

Table 13.18.1.1: Detail ranges of the RF RTMOM model

### 13.18.2 RF Test Structure and Measurement Procedures

Layout of the RTMOM structures is as shown in Fig. 13.18.2.1. It is designed as a two-port network with poly shield connected to ground for RTMOM capacitor. Two-port S parameter was performed with frequency sweep from 200 MHz to 30.0 GHz. Open and Short test structure measurements are used as RF de-embedding for each RTMOM.

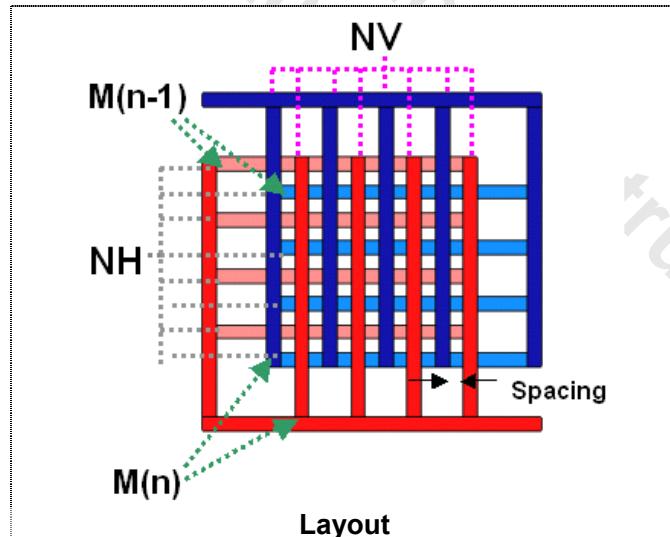


Fig. 13.18.2.1: Layout of RTMOM

### 13.18.3 RF Equivalent Circuit Model

The equivalent circuit model for the RTMOM with poly shield capacitor structure is shown in Fig. 13.18.3.1. Description of the equivalent circuit is summarized below:

The inter-metal dielectric Cmomin models the main element of the capacitor.

Ra and La are the parasitics existing in the electrode connected to port 1(a)

Rb and Lb are the parasitics existing in the electrode connected to port 2(b)

Cpa/Cpb of RTMOM represents the capacitance between metal and poly shield.

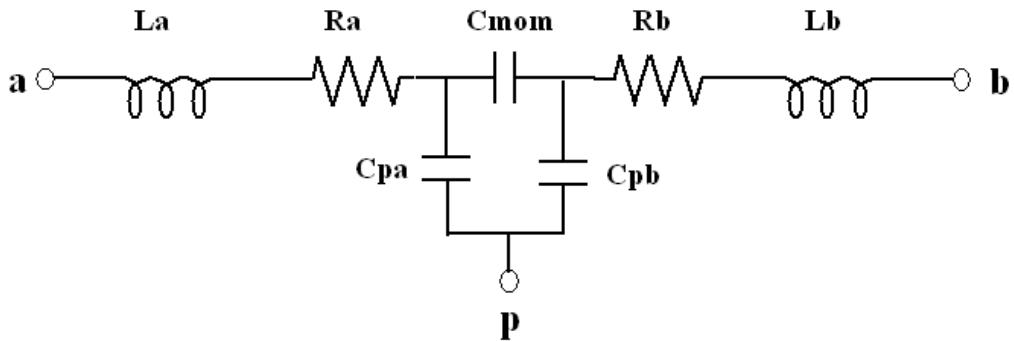


Fig. 13.18.3.1: Equivalent circuit of the RTMOM with poly shield structure

## 13.18.4 RF Model Details

### 13.18.4.1 Scaling Rule

The scaling equations for the various elements R, L and C are empirically determined and shown in Table 13.18.4.1.1.

Component	Scaling rule
$L_a$ (H)	total_I
$R_a$ ( $\Omega$ )	total_res·(0.0036·(temper-25)+1)
$C_{ab}$ (F)	(1+factmis)·(Cc1·Edg+Cf·FRI1+Ca·AREA+Cc2·FRI2)·1e-9·(1+(temper-25)·tcc1+(temper-25)·tcc2)·(1+vcc1·v(a1,b1)+vcc2·v(a1,b1)·v(a1,b1))
$C_{pa}$ (F)	(Ca_p·(Abm+Afm)+Cf_p·Pf+Cc_p·Pfb)·1e-9·(1+(temper-25)·tcc1+(temper-25)·tcc2)·(1+vcc1·v(a,p)+vcc2·v(a1,p)·v(a1,p))
$C_{pb}$ (F)	(Ca_p·(Abm+Afm)+Cf_p·Pf+Cc_p·Pfb)·1e-9·(1+(temper-25)·tcc1+(temper-25)·tcc2)·(1+vcc1·v(b,p)+vcc2·v(b1,p)·v(b1,p))
$R_b$ ( $\Omega$ )	total_res·(0.0036·(temper-25)+1)
$L_b$ (H)	total_I
where,	
layno	spm-stm+1
laym1	INT(layno/spm)
layodd	INT((layno+j1+j3+j5)/2)-laym1
layeven	INT((layno+j2+j4)/2)
r	0.82
dw	0.035u
ww	w-scale+dw
ss	s-scale-dw
wb	0.14u·(1-busflag)+0.23u·busflag+dw
sb	0.5u-dw
Inv	Nh·(ww+ss)-ss
Inh	nv·(ww+ss)-ss
tcc1	-12.5·1e-6
tcc2	0.0125·1e-6
vcc1	0.125·1e-6
vcc2	-1.125·1e-6
j1	(stm-2)·(stm-3)·(stm-4)·(stm-5)/(1-2)/(1-3)/(1-4)/(1-5)
j2	(stm-1)·(stm-3)·(stm-4)·(stm-5)/(2-1)/(2-3)/(2-4)/(2-5)
j3	(stm-1)·(stm-2)·(stm-4)·(stm-5)/(3-1)/(3-2)/(3-4)/(3-5)
j4	(stm-1)·(stm-2)·(stm-3)·(stm-5)/(4-1)/(4-2)/(4-3)/(4-5)
j5	(stm-1)·(stm-2)·(stm-3)·(stm-4)/(5-1)/(5-2)/(5-3)/(5-4)
Edg	((layodd+r·laym1)·(nv-1)·Inv+layeven·(nh-1)·Inh)
AREA	nv·nh/2·ww·(layno-1)
FRI1	(2·nh·nv·ww)·(layno-1)
FRI2	(layodd+r·laym1)·Inv·2+layeven·(Inh+sb)·2+((layodd+r·laym1)·nv·ww+layeven·nh·ww)+layno·wb·2
Abm	((Inh+(wb+sb)·2)+(Inv+sb))·wb/ww·((1-busflag)·(3·j1+9·j2+15·(j3+j4+j5))+busflag·(2.35·j1+5.9·j2+9.5·(j3+j4+j5)))
Afm	(j1+j3+j5)·(nv·(Inv+sb))/2+(j2+j4)·(nh·(Inh+sb))/2
Pf	(j1+j3+j5)·nv·(Inv+sb)+(j2+j4)·nh·(Inh+sb)+2·(Inv+Inh)+6·wb+6·sb
Pfb	j1·(Inv+2·wb+sb)·2.5
Cc1	((1.38287132687712E-06)/(w-scale·1e6)+(1.28434517185447E-02)/(s-scale·1e6)+(-9.51068922558549E-05)/(s-scale·1e6)/(w-scale·1e6)+(0.007890394118502))·1.078
Cc2	(2.89166666666667E-02)·2.4
Cf	((-1.14456610988729E-03)·(w-scale·1e6)+(3.40735779344344E-02)·(s-scale·1e6)+(7.75814036995283E-03)·(s-scale·1e6)·(w-scale·1e6)+(3.91043615388531E-04))·1
Ca	((8.55768320779471E-02)·(w-scale·1e6)+(3.42078406319888E-03)·(s-scale·1e6)+(1.72650608929306E-02)·(s-scale·1e6)·(w-scale·1e6)+(1.11117855154897E-03))·1
ca_p_a	(j1·(0.146172208111846)·0.810+j2·(3.64551632761436E-02)·0.630+j3·(1.95425271016389E-02)·0.500+j4·(1.33930640495099E-02)·0.500+j5·(1.03498029229406E-02)·0.500)
ca_p_b	(j1·(1.82779444326889E-03)·0.810+j2·(2.11074961039823E-03)·0.630+j3·(1.23920300340969E-03)·0.500+j4·(7.68410309899179E-04)·0.500+j5·(1.92831547168466E-04)·0.500)
ca_p_c	(j1·(-9.97536849903791E-03)·0.810+j2·(3.06827841451244E-03)·0.630+j3·(9.43716365687349E-04)·0.500+j4·(6.90602435701344E-04)·0.500+j5·(-7.68934658955753E-04)·0.500)

Component	Scaling rule
ca_p_d	$(j1 \cdot (-1.25553824723206E-04) \cdot 0.810 + j2 \cdot (3.50850668761436E-04) \cdot 0.630 + j3 \cdot (1.88525861386361E-04) \cdot 0.500 + j4 \cdot (1.33682599125244E-04) \cdot 0.500 + j5 \cdot (1.61196200083524E-04) \cdot 0.500)$
cf_p_a	$(j1 \cdot (-2.71509069214316E-03) \cdot 0.810 + j2 \cdot (-1.10200331192201E-03) \cdot 0.630 + j3 \cdot (1.26901394639261E-03) \cdot 0.500 + j4 \cdot (1.21673278546678E-03) \cdot 0.500 + j5 \cdot (2.45225891140367E-03) \cdot 0.500)$
cf_p_b	$(j1 \cdot (5.25249831756145E-02) \cdot 0.810 + j2 \cdot (0.016284884956133) \cdot 0.630 + j3 \cdot (1.12390047122562E-02) \cdot 0.500 + j4 \cdot (8.47435051396489E-03) \cdot 0.500 + j5 \cdot (8.50258208872684E-03) \cdot 0.500)$
cf_p_c	$(j1 \cdot (3.34537198611838E-02) \cdot 0.810 + j2 \cdot (6.38061261182805E-03) \cdot 0.630 + j3 \cdot (-7.77567185787758E-03) \cdot 0.500 + j4 \cdot (-4.80011322468783E-03) \cdot 0.500 + j5 \cdot (-8.88244754500573E-03) \cdot 0.500)$
cf_p_d	$(j1 \cdot (3.81877517951098E-03) \cdot 0.810 + j2 \cdot (2.32886849647634E-03) \cdot 0.630 + j3 \cdot (2.04615541648665E-03) \cdot 0.500 + j4 \cdot (2.01166504247318E-03) \cdot 0.500 + j5 \cdot (1.76558121828956E-03) \cdot 0.500)$
Ca_p	$(ca\_p\_a \cdot (w\cdot scale\cdot 1e6) + ca\_p\_b \cdot (s\cdot scale\cdot 1e6) + ca\_p\_c \cdot (s\cdot scale\cdot 1e6) \cdot (w\cdot scale\cdot 1e6) + ca\_p\_d \cdot 1)$
Cf_p	$(cf\_p\_a \cdot (w\cdot scale\cdot 1e6) + cf\_p\_b \cdot (s\cdot scale\cdot 1e6) + cf\_p\_c \cdot (s\cdot scale\cdot 1e6) \cdot (w\cdot scale\cdot 1e6) + cf\_p\_d \cdot 1)$
Cc_p	$(0.023)\cdot 1$
geo_fac	$1/sqrt((Cc1\cdot Edg\cdot 1e-9+Cf\cdot 1e-9\cdot FRI1+Ca\cdot 1e-9\cdot AREA+Cc2\cdot 1e-9\cdot FRI2)\cdot 1e15)$
mis	$0.54\cdot(((geo\_fac-0.029)^2+0.000000000000000001)^{0.5}+geo\_fac)+2.6\cdot(((geo\_fac-0.029)^2+0.0000000000000001)^{0.5}-geo\_fac)+0.12$
factmis	$mis/1.414/100\cdot mismatchflag$
length_nv	$nh\cdot(w+s)-s$
res_nv	$(length\_nv/w\cdot 0.072)+0.5\cdot 1e-6/w\cdot 0.072$
latres_nv	$(w+2\cdot s)/(0.14u\cdot(1\cdot busflag)+0.23u\cdot busflag)\cdot 0.072$
fin_nv	$nv/2$
totres_nv	$(latres\_nv/2+(fin\_nv/2-1)\cdot (fin\_nv-1)/(6\cdot fin\_nv/2)\cdot latres\_nv+res\_nv/(fin\_nv/2))/2$
allres_nv	$totres\_nv/(layodd+laym1)$
length_nh	$nv\cdot(w+s)-s$
res_nh	$(length\_nh/w\cdot 0.072)+0.5\cdot 1e-6/w\cdot 0.072$
latres_nh	$(w+2\cdot s)/(0.14u\cdot(1\cdot busflag)+0.23u\cdot busflag)\cdot 0.072$
fin_nh	$nh/2$
rend_nh	$(0.5\cdot 1e-6+w+s+length\_nh/2+0.5\cdot 1e-6)/(0.14u\cdot(1\cdot busflag)+0.23u\cdot busflag)\cdot 0.072$
totres_nh	$rend\_nh+(fin\_nh-1)\cdot (2\cdot fin\_nh-1)/(6\cdot fin\_nh)\cdot latres\_nh+res\_nh/fin\_nh$
allres_nh	$totres\_nh/layeven$
total_res_d14	$((1/(1/allres_nv+1/allres_nh))\cdot (((nv/nh\cdot (-0.00295421904051423)+(0.00665356748823694)/nv)+(nh/nv\cdot (-0.000362418857457649)+(0.928271687627286)/nh)+((1.05147609895631e-07)\cdot nv\cdot nh))/((0.077602644193527)\cdot w\cdot 1e6+(0.466628892310347)\cdot s\cdot 1e6+(0.177241753938233)\cdot (w\cdot 1e6)))$
total_res_d23	$((1/(1/allres_nv+1/allres_nh))\cdot (((nv/nh\cdot (-0.00265879713646281)+(0.00598821073941325)/nv)+(nh/nv\cdot (-0.000326176971711884)+(0.835444518864558)/nh)+((9.4632848906068E-08)\cdot nv\cdot nh))/((0.077602644193527)\cdot w\cdot 1e6+(0.466628892310347)\cdot s\cdot 1e6+(0.177241753938233)\cdot (w\cdot 1e6)))$
total_res	$(total\_res\_d14\cdot (1\cdot busflag)+total\_res\_d23\cdot busflag)$
I_nvnh	$((0.2\cdot (length\_nv\cdot 1e6)\cdot (\log10((length\_nv\cdot 1e6)/(length\_nh\cdot 1e6+0.22)))+1.19+0.022\cdot (length\_nh\cdot 1e6+0.22)/(length\_nv\cdot 1e6))+1.5))$
total_nvnh	$((0.1+(layno-1)\cdot (2\cdot layno-1)/(6\cdot layno)-0.1+I\_nvnh/layno))$
total_I_d14	$(((-0.00200723700664269)\cdot total\_nvnh^2+(0.107620716032798)\cdot total\_nvnh+(56.1120122581937)\cdot ((38.8095156996774)\cdot (layno)^{(0.00230072519205777)}\cdot ((w\cdot 1e6+s\cdot 1e6)^{(0.0064152117401132)}\cdot ((nv\cdot nh)^{(0.000129852603284219)})+(-2170.12789133465))\cdot 1e-12$
total_I_d23	$(((-0.00200723700664269)\cdot total\_nvnh^2+(0.107620716032798)\cdot total\_nvnh+(56.1120122581937)\cdot ((34.9285641297097)\cdot (layno)^{(0.00230072519205777)}\cdot ((w\cdot 1e6+s\cdot 1e6)^{(0.0064152117401132)}\cdot ((nv\cdot nh)^{(0.000129852603284219)})+(-1953.11510220118))\cdot 1e-12$
total_I	$(total\_I\_d14\cdot (1\cdot busflag)+total\_I\_d23\cdot busflag)$

Table 13.18.4.1.1: Sub-circuit elements for RTMOM.

### 13.18.4.2 Model Parameter

The values for equivalent circuit elements are shown in Table 13.18.4.2.1.

Nv	6	6	48	96	192	192	288	288	288	96	288
Nh	96	192	48	96	48	192	6	6	6	96	6
W(μm)	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.18	0.14	0.14	0.14
S(μm)	0.14	0.14	0.14	0.14	0.14	0.14	0.18	0.14	0.14	0.14	0.14
Stm	1	1	1	1	1	1	1	1	2	1	1
Spm	5	5	5	5	5	5	5	5	5	3	3
L <sub>a</sub> (pH)	11.65	22.84	4.76	7.72	4.02	13.04	4.14	4.14	1.35	8.95	0.36
R <sub>a</sub> (Ω)	1.13	1.26	0.40	0.49	0.79	0.80	1.52	1.37	1.97	0.74	2.03
R <sub>b</sub> (Ω)	1.13	1.26	0.40	0.49	0.79	0.80	1.52	1.37	1.97	0.74	2.03
L <sub>b</sub> (pH)	11.65	22.84	4.76	7.72	4.02	13.04	4.14	4.14	1.35	8.95	0.36

(a)

Nv	16	16	40	48	52	56	56	60	64	74	80	80	82	116	288
Nh	50	78	56	64	60	72	160	48	64	74	30	80	206	124	288
W(μm)	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
S(μm)	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
Stm	1	1	1	2	1	2	1	2	1	1	1	1	1	1	1
Spm	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
L <sub>a</sub> (pH)	5.05	7.59	4.98	5.41	5.09	5.95	12.53	3.85	5.21	5.76	2.96	6.09	15.02	8.51	16.14
R <sub>a</sub> (mΩ)	421.20	493.55	285.11	401.71	275.35	403.52	373.29	394.62	276.51	283.83	326.16	289.31	388.19	337.55	742.12
R <sub>b</sub> (mΩ)	421.20	493.55	285.11	401.71	275.35	403.52	373.29	394.62	276.51	283.83	326.16	289.31	388.19	337.55	742.12
L <sub>b</sub> (pH)	5.05	7.59	4.98	5.41	5.09	5.95	12.53	3.85	5.21	5.76	2.96	6.09	15.02	8.51	16.14

(b)

Table 13.18.4.2.1: Equivalent circuit parameters for RTMOM. (a) L-bus=0.14um, (b) L-bus=0.23um.

### 13.18.4.3 Model Error Table

RTMOM fitting errors between measurement and simulation are summarized in Table 13.18.4.3.1. For each device the capacitance and Q-value fitting errors are shown at 2.4GHz and 10GHz. Definition of fitting error CRMS is documented in section 10.

NV	6	6	48	96	192	192	288	288	288	96	288
NH	96	192	48	96	48	192	6	6	6	96	6
W (um)	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.18	0.14	0.14	0.14
S (um)	0.14	0.14	0.14	0.14	0.14	0.14	0.18	0.14	0.14	0.14	0.14
stm	1	1	1	1	1	1	1	1	2	1	1
spm	5	5	5	5	5	5	5	5	5	3	3
C <sub>RMS</sub> (%) *	1.2	1.0	0.3	2.0	5.3	3.1	1.2	0.2	2.1	2.0	4.2
C <sub>f=2.4GHz</sub> (%)	1.1	1.1	-0.5	0.4	-0.5	0.7	-1.6	-0.1	-1.8	-1.7	-3.7
C <sub>f=10GHz</sub> (%)	1.2	1.0	0.0	0.3	-1.8	18.6	-1.2	0.3	-1.9	-1.3	-4.0
Q <sub>f=2.4GHz</sub> (%)	8.4	-31.7	-7.1	-10.1	-7.3	3.1	0.2	-3.5	-9.3	-10.2	7.2
Q <sub>f=10GHz</sub> (%)	-23.3	-20.7	-2.1	-4.9	-4.5	1.3	-2.5	-1.2	-6.5	-7.9	5.3

(a)

NV	16	16	40	48	52	56	52	60	64	74	80	80	82	116	288
NH	50	78	56	64	60	72	160	48	64	74	30	80	206	124	288
W (um)	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
S (um)	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14	0.14
stm	1	1	1	2	1	2	1	2	1	1	1	1	1	1	1
spm	5	5	5	5	5	5	5	5	5	5	5	5	5	5	5
C <sub>RMS</sub> (%) *	0.1	0.3	0.7	0.8	1.3	2.0	1.1	0.9	1.1	1.6	0.4	2.5	1.0	0.9	7.8
C <sub>f=2.4GHz</sub> (%)	0.0	-0.1	0.0	-1.0	0.2	-1.2	0.9	-0.8	-0.5	-0.3	-0.4	-0.2	0.2	-0.2	3.1
C <sub>f=10GHz</sub> (%)	0.0	0.2	-0.1	-0.6	1.2	-1.3	1.2	-0.7	-0.4	-0.3	0.2	-0.5	-3.9	1.1	NA
Q <sub>f=2.4GHz</sub> (%)	-9.7	-11.0	-34.8	-19.4	-12.4	-19.5	-10.5	-13.6	-11.8	-16.0	-15.5	-22.0	-9.7	-4.9	15.8
Q <sub>f=10GHz</sub> (%)	17.0	-12.4	-5.0	-10.3	13.7	-9.0	10.3	-5.6	10.7	-7.6	-0.9	-11.2	26.3	7.8	NA

(b)

Table 13.18.4.3.1: Fitting errors for RTMOM. (a) L-bus=0.14um, (b) L-bus=0.23um

## 13.18.5 RF Corner Model Table

The skew parameters are listed below Table 13.18.5.1 for corner-case simulation.

Skew Parameter	SS	TT	FF
RTMOM_momfac	1.15	1	0.85
RTMOM_momfac2	1.4	1	0.6
l_momfac	1.0235	1	0.9762
r_momfac	1.3	1	0.7

Table 13.18.5.1: Corner Model Table for RTMOM.

## 13.18.6 RF Temperature Effect Model

The temperature characteristics of capacitors are evaluated with W/S=0.14/0.14 m, NV/NH=192/72 and stacked metal M2~M7. The capacitance does not appear to change much with temperature(-40°C, 25°C, 125°C). However, the Q changes with temperature. It might be due to the temperature coefficient of the RTMOM resistance (TCR).

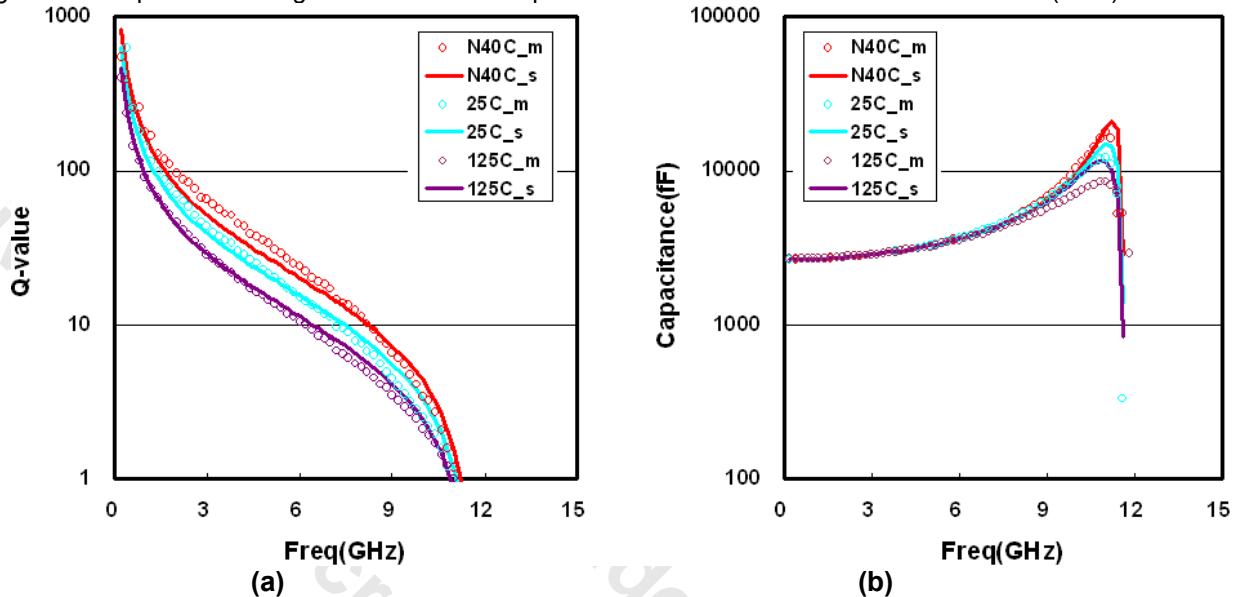


Fig. 13.18.6.1: RTMOM at 125°C , 25°C , -40°C (a) Q , (b) C Plots

The TCR characteristics of capacitors are also evaluated with W/S=0.14/0.14 m, NV/NH=192/72 and stacked metal M2~M7. The resistance shows a linear dependence of the temperature(-40°C, 25 °C, 125°C). The following functions have been implemented into the model for temperature effect simulation.

$$Ra(T)=Ra*(0.0036*(temper-25)+1)$$

$$Rb(T)=Rb*(0.0036*(temper-25)+1)$$

## 13.18.7 VCC and TCC

The VCC and TCC characteristics of capacitors are evaluated with W/S=0.14/0.14 m and NV/NH=144/288. The capacitance shows a parabolic dependence of the DC bias voltage(-5V to 5V in steps of 0.5V) at 25 °C, for its  $V_{cc1} = 0.125 \text{ ppm/V}$ , and  $V_{cc2} = -1.125 \text{ ppm/V}^2$ . At the bias 0V, with different temperature (-40°C to 125 °C), the  $T_{cc1}$  of the capacitors is  $-12.5 \text{ ppm/}^\circ\text{C}$ , where  $T_{cc2}$  is  $0.0125 \text{ ppm/}^\circ\text{C}^2$ .

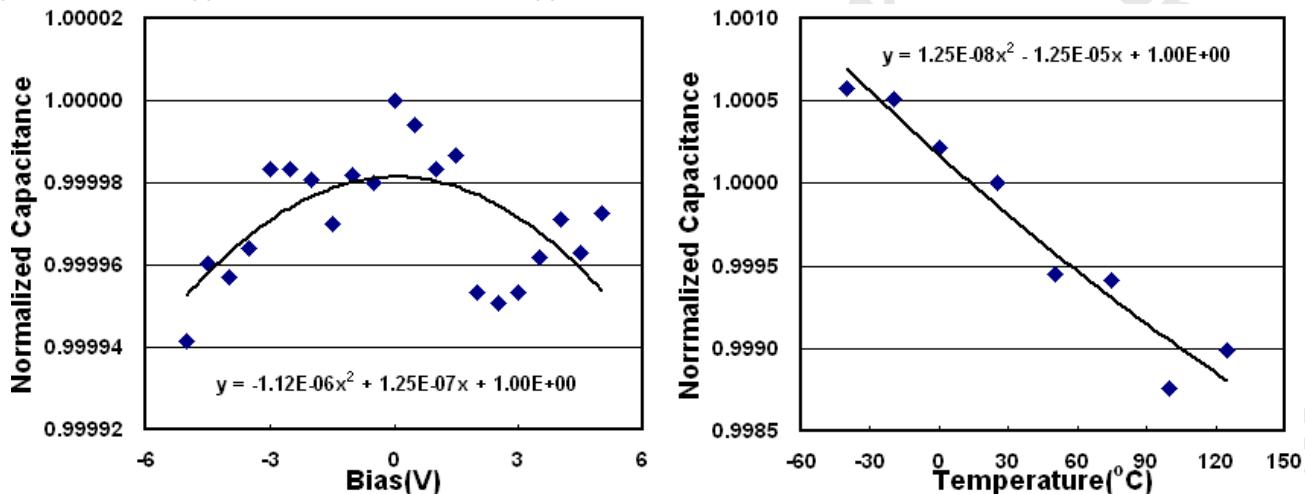


Fig. 13.18.7.1: (a) VCC, (b) TCC Plots of RTMOM

## 13.18.8 Mismatch Model

The model for this technology has added the capability for mismatch analysis of an identical and closely spaced RTMOM pair. Random variations in Gaussian distribution of the total capacitance are included in the model to account for the mismatch performance. The mismatch simulation results with the measured data are shown in Fig.8-5 for parallel RTMOM.

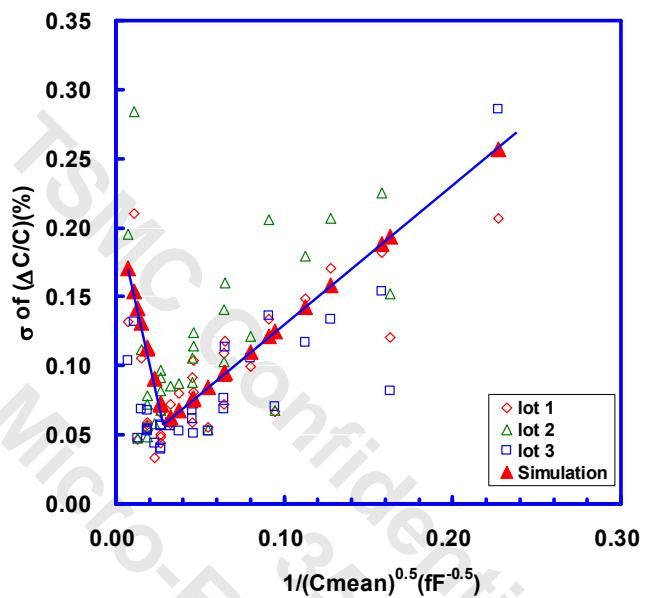


Fig. 13.18.8.1: Simulation results of 1000 Monte-Carlo random tests of  $\sigma_2(C_1 - C_2)/(C_1 + C_2)$  of parallel RTMOM.

## 13.19 Inductor Model

### 13.19.1 Model Usage Guide

Standard and symmetric octagonal spiral inductors using a thick Cu metal (physical thickness: 3.4um) were fabricated on top of P-substrate and modeled based on the two-port Y-parameter fitting. Three types of scalable inductor models, which are standard (STD), symmetric (SYM), and symmetric with center tap (SYMCT) have been included in this release. The detailed ranges of models are listed in Table 13.19.1.1.

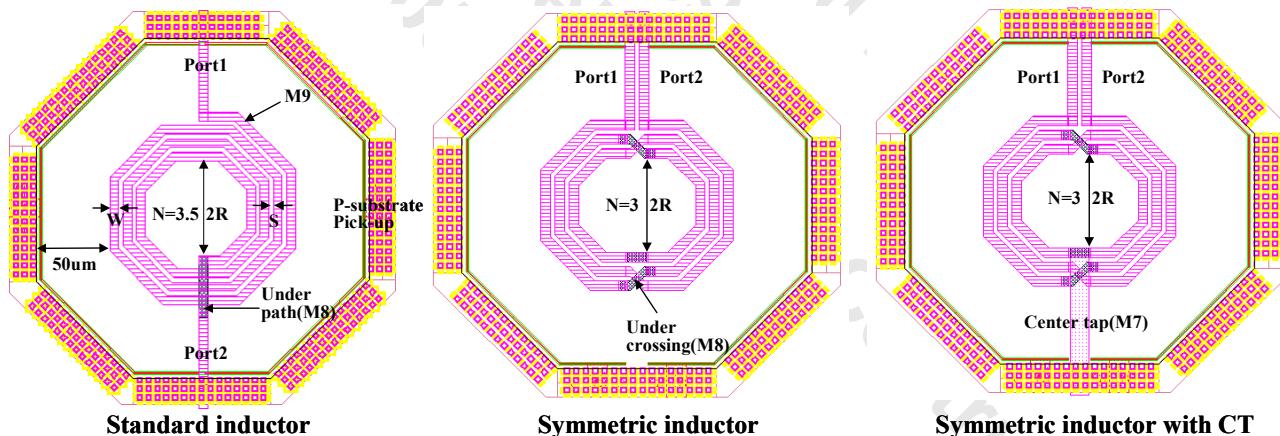
**Table 13.19.1.1: Detailed ranges of inductor models**

Specification	Standard Inductor				Symmetric Inductor				Symmetric Inductor with CT											
Inductance(nH)	0.22 ~ 11.2				0.12 ~ 12.9				0.12 ~ 12.9											
Fixed width(μm)	3	6	9	15	3	6	9	15	3	6	9	15								
Valid Turns(N)	0.5 ~ 5.5	0.5 ~ 5.5	0.5 ~ 5.5	0.5 ~ 5.5	1 ~ 6	1 ~ 6	1 ~ 6	1 ~ 6	1 ~ 5	1 ~ 5	1 ~ 5	1 ~ 5								
Valid Radius(R:μm)	1/4 turn increments				Integral turn increments				Odd turn increments											
Variable Metal Layer	15 ~ 90				15 ~ 90				15 ~ 90											
Valid Temperature	1P4M ~ 1P9M																			
Valid Frequency	-40°C ~ 125°C																			
	min(30GHz, Fsr)																			

The symmetric inductors can be used both in a single-ended operation and differential mode operation. No devices are allowed to be placed below the inductor, as their performance will be affected by the magnetic flux penetrating into the silicon substrate. Designers can change N (turns) and R (radius) to tune the L (inductance) value. For information regarding the inductor design, please refer to the thick metal rule of the chapter 4.

### 13.19.2 Test Structure and Measurement Procedures

The top views of different inductor layouts with the key design parameters are shown in Fig. 13.19.2.1.



**Fig. 13.19.2.1: Top views of inductor layouts.**

The key parameters of the inductor as depicted in the diagram are

- N: number of turns
- W: inductor track width
- S: spacing between tracks
- R: inner radius of inductor

### 13.19.3 Equivalent Circuit Model

A lumped RLC equivalent circuit representation of 2-port standard inductor is shown in Fig. 13.19.3.1. The values of each component are extracted through the fitting of the 2-port Y-parameters that are obtained after de-embedding the dummy open and through accordingly. Fig. 13.19.3.2 shows the equivalent circuit of a symmetric inductor with and without center-tap (dash-line).

The definitions of the parameters are,

- L1 (and L2): Inductor self-inductance
- M: Mutual inductance
- R1 (and R2): Metal series resistance
- C12: Coupling capacitance between port 1 and port 2
- Cox1 (Cox2 and Cox3): Oxide capacitance between the spiral and substrate
- Rsub1 (Rsub2 and Rsub3): Silicon substrate resistance
- Csub1 (Csub2 and Csub3): Silicon substrate capacitance
- Ls1 (and Ls2): Inductance to model the skin effect of the metal track
- Rs1 (and Rs2): Resistance to model the skin effect of the metal track
- R13 (and R32): Substrate coupling resistance
- C13 (and C32): Substrate coupling capacitance
- Lct: Inductance due to the center tap metal
- Rct: Resistance due to the center tap metal

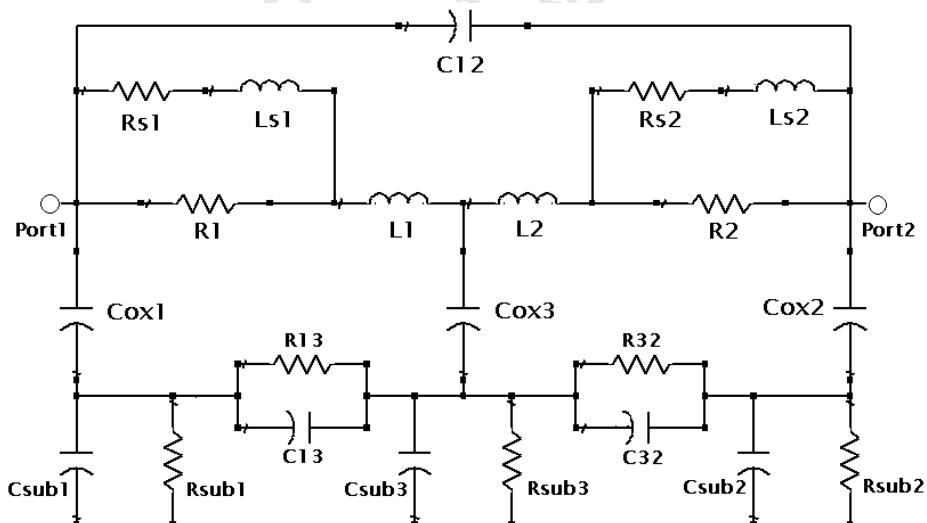


Fig. 13.19.3.1: Equivalent circuit of a standard inductor.

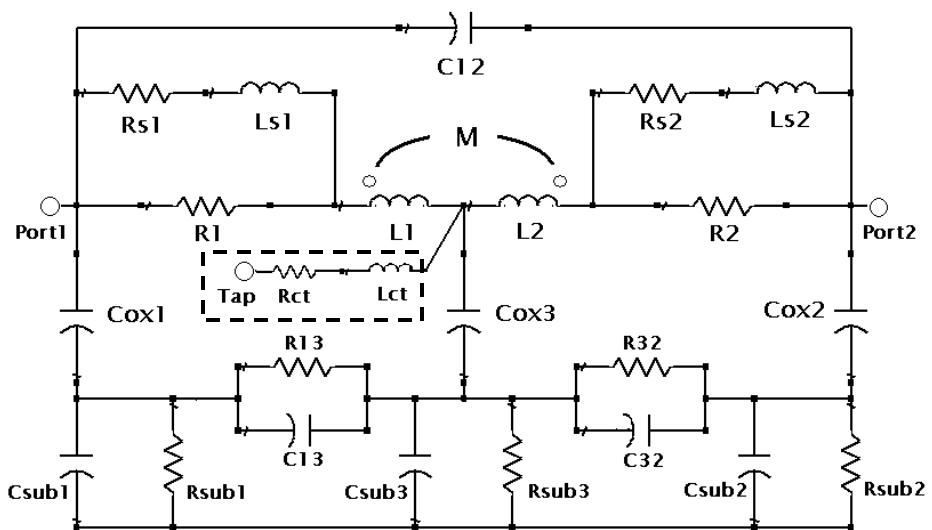


Fig. 13.19.3.2: Equivalent circuit of a symmetric inductor.

## 13.19.4 Model Details

The 2D scalable models are generated based on the procedure:

- Measure devices on Si-wafer
- Extract each parameter using  $\Pi$ -circuit
- Fit and fine-tune these parameters in terms of the fitting of Y-parameters, Q-value(Q), and inductance(L)
- Find and optimize a scalable equation, which is function of turns and radius, for each component of equivalent circuit.

Inductance as a function of number of turns (N) and radius (R) is modeled with the empirical equation below.

$$L1=L2=a \cdot N^b \cdot DA^c \cdot DO^d + e \cdot N^f + g$$

Where, a, b, c, d, e, f and g are fitting parameters, DO is outer diameter, DI is inner diameter and DA (average diameter) =  $(DO+DI)/2$ . Quality of the model is show in Fig. 13.19.4.4.

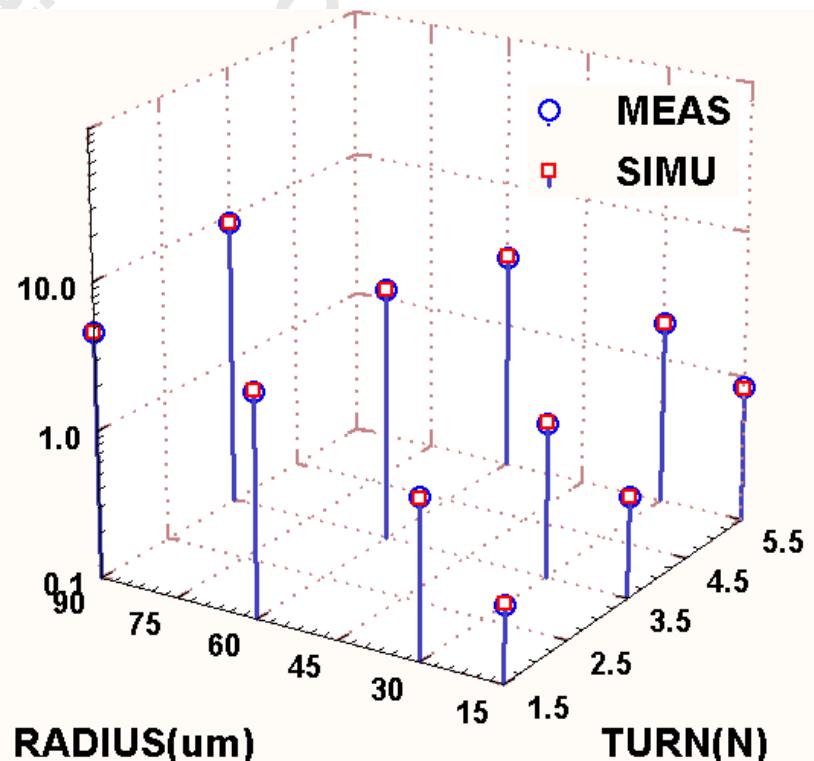


Fig. 13.19.4.4: Inductance (STD W=9  $\mu$ m) as a function of number of turns and radius @ 2.4GHz

The scaling formulae for other parameters with respect to N and DA are,

For standard inductor,

$$\begin{aligned}
 R1=R2 &= a*N*DA2+b*N+c*DA+d*N2+e \\
 Rs1=Rs2 &= a*N*DA2+b*N+c*DA+d*N2+e \\
 C12 &= a*N+b*N*DA+c*N2+d*DA2+e \\
 Cox1 &= a*N*DA+b \\
 Cox2 &= a*N*DA+b \\
 Cox3 &= Cox1+Cox2 \\
 Rsub1 &= a/(N*DA)+b/DA+c/N+d \\
 Rsub2 &= a/(N*DA)+b/DA+c/N+d \\
 Rsub3 &= Rsub1*Rsub2/(Rsub1+Rsub2) \\
 Csub1 &= 1.053e-11/Rsub1 \\
 Csub2 &= 1.053e-11/Rsub2 \\
 Csub3 &= Csub1+Csub2 \\
 R13 &= a*N/(spiral length) \\
 R32 &= a*N/(spiral length) \\
 C13 &= 1.053e-11/R13 \\
 C32 &= 1.053e-11/R32
 \end{aligned}$$

For symmetric inductor

$$K=a*Nb*DAc*DOd+e*Nf+g$$

For symmetric with center-tap

$$\begin{aligned}
 Lct &= a*N2+b*N+c \\
 Rct &= a*N+b
 \end{aligned}$$

$F_r$  is the resonance frequency of the inductor under single-end operation,  $Q_s(-\text{imag}Y_{11}/\text{real}Y_{11})$  is the Q-factor of the inductor under single-end operation,  $Q_d(\text{imag}Z_d/\text{real}Z_d)$  is the Q-factor of the inductor under differential mode operation and  $F_{dr}$  is the resonance frequency of the inductor under differential mode operation.

The differential mode one-port S-parameter  $S_d$  and differential mode input impedance  $Z_d$  are obtained by using the formulae below,

$$\begin{aligned}
 S_d &= \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2}, \\
 Z_d &= 2Z_o \left( \frac{1 + S_d}{1 - S_d} \right)
 \end{aligned}$$

where  $2Z_o$  is the differential system impedance, with  $Z_o$  assumed to be  $50\Omega$ .  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$  and  $S_{22}$  are the 2-port S-parameters of the single-ended mode inductor. All of  $S_{11}$ ,  $S_{12}$ ,  $S_{21}$ ,  $S_{22}$ , and  $S_{d11}$  were used in the parameter extraction

## 13.19.4.1 Standard inductor

### 13.19.4.1.1 Scaling Rule

Table 13.19.4.1.1.1: Sub-circuit elements for standard inductor with W=9  $\mu$  m.

Component	Scaling Rule
C <sub>12</sub> (F)	(c12_a·nr+c12_b·nr·da+c12_c·nr·nr+c12_d·da·da+c12_e)·1e-15
R <sub>1</sub> ( $\Omega$ )	(r1_a·nr·da·da+r1_b·nr+r1_c·da+r1_d·nr·nr+r1_e)·(0.0026·(temper-25)+1)
L <sub>1</sub> (H)	(l1_a·nr <sup>(l1_b)</sup> ·da <sup>(l1_c)</sup> ·do <sup>(l1_d)</sup> +l1_e·nr <sup>(l1_f)</sup> +l1_g)·1.0e-9
L <sub>2</sub> (H)	(l1_a·nr <sup>(l1_b)</sup> ·da <sup>(l1_c)</sup> ·do <sup>(l1_d)</sup> +l1_e·nr <sup>(l1_f)</sup> +l1_g)·1.0e-9
R <sub>2</sub> ( $\Omega$ )	(r1_a·nr·da·da+r1_b·nr+r1_c·da+r1_d·nr·nr+r1_e)·(0.0026·(temper-25)+1)
R <sub>s1</sub> ( $\Omega$ )	(rs_a·nr·da·da+rs_b·nr+rs_c·da+rs_d·nr·nr+rs_e)·((0.0026·(temper-25)+1) <sup>(0.5)</sup> )
L <sub>s1</sub> (H)	(ls_a·nr <sup>(ls_b)</sup> ·da <sup>(ls_c)</sup> ·do <sup>(ls_d)</sup> +ls_e·nr <sup>(ls_f)</sup> +ls_g)·1e-9
L <sub>s2</sub> (H)	(ls_a·nr <sup>(ls_b)</sup> ·da <sup>(ls_c)</sup> ·do <sup>(ls_d)</sup> +ls_e·nr <sup>(ls_f)</sup> +ls_g)·1e-9
R <sub>s2</sub> ( $\Omega$ )	(rs_a·nr·da·da+rs_b·nr+rs_c·da+rs_d·nr·nr+rs_e)·((0.0026·(temper-25)+1) <sup>(0.5)</sup> )
C <sub>ox1</sub> (F)	(cox_1)·((1/(12.503905+(1.7014125)·(lay-3)))/(0.0440289))·1e-15
C <sub>ox2</sub> (F)	(cox_2)·((1/(12.503905+(1.7014125)·(lay-3)))/(0.0440289))·1e-15
C <sub>ox3</sub> (F)	(cox_1+cox_2)·((1/(12.503905+(1.7014125)·(lay-3)))/(0.0440289))·1e-15
R <sub>sub13</sub> ( $\Omega$ )	(rsub_13)
R <sub>sub32</sub> ( $\Omega$ )	(rsub_32)
C <sub>sub13</sub> (F)	(csub_13)
C <sub>sub32</sub> (F)	(csub_32)
C <sub>sub1</sub> (F)	(csub_1)
C <sub>sub2</sub> (F)	(csub_2)
C <sub>sub3</sub> (F)	(csub_1+csub_2)
R <sub>sub1</sub> ( $\Omega$ )	(rsub_1)
R <sub>sub2</sub> ( $\Omega$ )	(rsub_2)
R <sub>sub3</sub> ( $\Omega$ )	(rsub_1·rsub_2/(rsub_1+rsub_2))
where,	
di	2·rad·1e6
do	2·(rad·1e6)+(int(nr+0.5)·(w·1e6+3)-3)+((int(nr)+1)·(w·1e6+3)-3)
da	(di+do)/2
c12_a	2.33864817
c12_b	0.001715054
c12_c	0.053531587
c12_d	0.000245546
c12_e	-1.460165781
r1_a	4.48E-06
r1_b	-0.05827335
r1_c	0.001228349
r1_d	0.063969073
r1_e	0.401067475
l1_a	0.00047619
l1_b	1.731275617
l1_c	2.228105758
l1_d	-1.034846428
l1_e	-20.942088
l1_f	0.000996
l1_g	21.02613
rs_a	3.36E-06
rs_b	-0.043705012
rs_c	0.000921262
rs_d	0.047976805

Component	Scaling Rule
rs_e	0.300800606
ls_a	0.049368924
ls_b	1.014977315
ls_c	0.452271083
ls_d	-0.173688549
ls_e	-0.134570189
ls_f	0.9324
ls_g	0.0124
cox1_a	0.05062799
cox1_b	6.439803165
cox2_a	9u-15u
cox2_b	7.051851648
rsub1_a	-2191.687531
rsub1_b	46788.72163
rsub1_c	309.5905447
rsub1_d	101.9150019
rsub2_a	-4006.35
rsub2_b	67284.87
rsub2_c	185.2727
rsub2_d	181.4429
rsub13_a	70
rsub32_a	80
cox_1	cox1_a·nr·da+cox1_b
cox_2	cox2_a·nr·da+cox2_b
rsub_1	(rsub1_a/(nr·da)+rsub1_b/da+rsub1_c/nr+rsub1_d)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
rsub_2	(rsub2_a/(nr·da)+rsub2_b/da+rsub2_c/nr+rsub2_d)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
rsub_13	(0.0000018·nr/((nr·da·3.31372+136)·7.25e-10)·rsub13_a)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
rsub_32	(0.0000018·nr/((nr·da·3.31372+136)·7.25e-10)·rsub32_a)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
csub_1	1.05315e-11/rsub_1
csub_2	1.05315e-11/rsub_2
csub_13	1.05315e-11/rsub_13
csub_32	1.05315e-11/rsub_32

### 13.19.4.1.2 Model Parameter

Table 13.19.4.1.2.1: Equivalent circuit parameters for standard inductor with W=9  $\mu$ m.

Nr	1.5	1.5	1.5	1.5	3.5	3.5	3.5	3.5	5.5	5.5	5.5
Rad( $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60
W( $\mu$ m)	9	9	9	9	9	9	9	9	9	9	9
Lay	9	9	9	9	9	9	9	9	9	9	9
C <sub>12</sub> (fF)	2.94	3.99	7.41	12.61	9.21	10.72	15.06	21.16	16.36	18.33	23.58
R <sub>1</sub> ( $\Omega$ )	0.538	0.601	0.764	0.976	1.161	1.283	1.61	2.051	2.379	2.584	3.128
L <sub>1</sub> (nH)	0.149	0.219	0.381	0.561	0.5	0.801	1.495	2.269	1.317	1.978	3.485
L <sub>2</sub> (nH)	0.149	0.219	0.381	0.561	0.5	0.801	1.495	2.269	1.317	1.978	3.485
R <sub>2</sub> ( $\Omega$ )	0.538	0.601	0.764	0.976	1.161	1.283	1.61	2.051	2.379	2.584	3.128
R <sub>s1</sub> ( $\Omega$ )	0.403	0.451	0.573	0.732	0.871	0.962	1.208	1.538	1.784	1.938	2.346
L <sub>s1</sub> (pH)	25.83	59.48	104.70	136.86	119.88	184.76	279.86	350.90	266.86	354.12	489.44
L <sub>s2</sub> (pH)	25.83	59.48	104.70	136.86	119.88	184.76	279.86	350.90	266.86	354.12	489.44
R <sub>s2</sub> ( $\Omega$ )	0.403	0.451	0.573	0.732	0.871	0.962	1.208	1.538	1.784	1.938	2.346
C <sub>ox1</sub> (fF)	10.31	12.59	17.15	21.70	19.73	25.05	35.68	46.31	34.01	42.36	59.07
C <sub>ox2</sub> (fF)	10.78	12.97	17.36	21.75	19.85	24.96	35.20	45.43	33.59	41.63	57.71
C <sub>ox3</sub> (fF)	21.09	25.56	34.51	43.45	39.58	50.01	70.88	91.74	67.60	83.99	116.78
R <sub>sub13</sub> ( $\Omega$ )	669.3	484.0	311.5	229.7	604.7	449.3	296.8	221.5	492.6	384.3	267.0
R <sub>sub32</sub> ( $\Omega$ )	764.9	553.1	356.0	262.5	691.1	513.5	339.2	253.2	563.0	439.2	305.1
C <sub>sub13</sub> (fF)	15.74	21.76	33.81	45.86	17.42	23.44	35.49	47.54	21.38	27.40	39.45
C <sub>sub32</sub> (fF)	13.77	19.04	29.58	40.12	15.24	20.51	31.05	41.59	18.71	23.98	34.52
C <sub>sub1</sub> (fF)	8.80	12.13	16.72	19.73	13.07	16.72	22.40	26.63	16.80	20.34	26.09
C <sub>sub2</sub> (fF)	6.7	9.551	13.799	16.812	9.435	12.185	16.579	19.933	11.868	14.406	18.565
C <sub>sub3</sub> (fF)	15.50	21.69	30.52	36.54	22.50	28.90	38.98	46.56	28.67	34.74	44.66
R <sub>sub1</sub> (K $\Omega$ )	1.197	0.868	0.63	0.534	0.806	0.63	0.47	0.396	0.627	0.518	0.404
R <sub>sub2</sub> (K $\Omega$ )	1.572	1.103	0.763	0.626	1.116	0.864	0.635	0.528	0.887	0.731	0.567
R <sub>sub3</sub> ( $\Omega$ )	679.6	485.7	345.1	288.2	468.0	364.4	270.2	226.2	367.3	303.1	235.8
											201.0

### 13.19.4.1.3 Model Error Table

Standard inductor fitting error between measurement and simulation are summarized in Table 13.19.4.1.3.1 to Table 13.19.4.1.3.4. For each device four Y-parameter fitting errors are separated with real part and imaginary part.

**Table 13.19.4.1.3.1: Fitting errors (Real and Imaginary) for standard inductor with W=3  $\mu$ m.**

N (turns)	1.5	1.5	1.5	1.5	3.5	3.5	3.5	3.5	4.5	4.5	4.5	4.5
R(radius in $\mu$ m)	16.5	31.5	61.5	91.5	16.5	31.5	61.5	91.5	16.5	31.5	61.5	91.5
Real(Y11)(%)	10.99	7.76	2.61	3.50	5.41	2.85	4.13	1.62	3.81	3.60	4.67	1.45
Real(Y21)(%)	10.97	7.73	2.59	3.53	5.41	2.82	4.01	1.45	3.82	3.50	4.51	0.85
Real(Y12)(%)	11.01	7.78	2.62	3.48	5.40	2.87	4.23	1.66	3.82	3.69	4.74	0.92
Real(Y22)(%)	10.98	7.75	2.61	3.52	5.40	2.84	4.11	1.58	3.82	3.59	4.66	1.43
Imag(Y11)(%)	7.09	3.83	2.04	3.47	4.12	2.09	3.68	1.54	4.55	4.01	4.62	1.50
Imag(Y21)(%)	7.04	3.81	2.07	3.76	4.05	2.08	3.61	1.51	4.48	3.94	4.54	1.45
Imag(Y12)(%)	7.05	3.81	2.08	3.76	4.05	2.07	3.68	1.56	4.48	4.02	4.59	1.50
Imag(Y22)(%)	7.08	3.82	2.05	3.48	4.22	2.20	3.68	1.59	4.73	4.11	4.67	1.72

**Table 13.19.4.1.3.2: Fitting errors (Real and Imaginary) for standard inductor with W=6  $\mu$ m.**

N (turns)	1.5	1.5	1.5	1.5	3.5	3.5	3.5	3.5	5.5	5.5	5.5
R(radius in $\mu$ m)	17.25	32.25	62.25	92.25	17.25	32.25	62.25	92.25	17.25	32.25	62.25
Real(Y11)(%)	22.74	13.80	11.39	12.64	13.67	7.82	4.70	5.82	22.06	14.20	10.91
Real(Y21)(%)	22.75	13.83	11.44	12.70	13.82	7.98	4.89	5.97	22.17	14.32	10.94
Real(Y12)(%)	22.73	13.78	11.35	12.58	13.53	7.68	4.54	5.62	22.07	14.15	10.50
Real(Y22)(%)	22.74	13.81	11.38	12.64	13.66	7.81	4.72	5.80	22.11	14.25	10.87
Imag(Y11)(%)	4.81	3.79	1.84	1.37	2.14	2.78	2.97	1.64	2.91	5.15	1.84
Imag(Y21)(%)	4.78	3.77	1.88	2.16	2.31	2.81	3.00	2.28	2.98	5.11	1.96
Imag(Y12)(%)	4.79	3.77	1.88	2.18	2.30	2.79	2.98	2.27	3.00	5.11	1.96
Imag(Y22)(%)	4.81	3.78	1.81	1.37	2.53	2.97	3.04	1.98	3.44	5.32	2.35

**Table 13.19.4.1.3.3: Fitting errors (Real and Imaginary) for standard inductor with W=9  $\mu$ m.**

N (turns)	1.5	1.5	1.5	1.5	3.5	3.5	3.5	3.5	5.5	5.5	5.5
R(radius in $\mu$ m)	18	33	63	93	18	33	63	93	18	33	63
Real(Y11)(%)	22.83	13.69	14.73	30.91	12.58	6.34	1.47	3.12	22.09	14.24	7.44
Real(Y21)(%)	22.92	13.79	14.85	35.92	12.78	6.47	1.62	2.96	22.45	14.55	6.92
Real(Y12)(%)	22.75	13.61	14.66	34.62	12.45	6.29	1.42	3.18	21.95	14.09	6.50
Real(Y22)(%)	22.84	13.71	14.76	30.83	12.59	6.35	1.55	3.14	22.11	14.30	7.74
Imag(Y11)(%)	4.84	3.36	2.83	1.63	2.43	1.86	1.13	0.61	6.19	2.11	0.87
Imag(Y21)(%)	4.82	3.36	2.86	2.05	2.66	1.94	1.19	0.98	6.24	2.31	1.46
Imag(Y12)(%)	4.83	3.37	2.87	2.06	2.65	1.96	1.20	1.00	6.22	2.29	1.47
Imag(Y22)(%)	4.84	3.37	2.83	1.68	2.81	2.23	1.41	1.15	6.40	2.72	2.40

**Table 13.19.4.1.3.4: Fitting errors (Real and Imaginary) for standard inductor with W=15  $\mu$ m.**

N (turns)	1.5	1.5	1.5	1.5	3.5	3.5	3.5	3.5	5.5	5.5	5.5
R(radius in $\mu$ m)	19.5	34.5	64.5	94.5	19.5	34.5	64.5	94.5	19.5	34.5	64.5
Real(Y11)(%)	16.93	17.59	17.60	10.42	3.89	5.40	2.86	3.52	30.98	17.45	15.00
Real(Y21)(%)	19.82	19.36	26.82	18.19	5.86	7.04	2.73	2.60	31.81	17.96	14.98
Real(Y12)(%)	19.56	18.74	25.95	17.21	5.65	6.60	2.68	2.76	31.13	17.43	14.69
Real(Y22)(%)	16.85	17.51	17.31	10.61	4.14	6.17	2.94	3.54	31.04	17.49	14.79
Imag(Y11)(%)	2.28	1.13	2.77	3.65	4.60	2.37	0.80	1.19	2.36	0.82	1.26
Imag(Y21)(%)	2.32	1.20	2.97	3.80	4.72	2.48	1.06	1.68	2.92	1.66	1.72
Imag(Y12)(%)	2.33	1.21	2.99	3.80	4.72	2.50	1.06	1.68	2.91	1.66	1.74
Imag(Y22)(%)	2.27	1.15	2.83	3.69	4.78	2.60	1.28	1.82	3.08	2.04	2.32

## 13.19.4.2 Symmetric inductor

### 13.19.4.2.1 Scaling Rule

Table 13.19.4.2.1.1: Sub-circuit elements for symmetric inductor with W=9  $\mu$ m.

Component	Scaling Rule
C <sub>12</sub> (F)	(c <sub>12_a</sub> ·nr+c <sub>12_b</sub> ·nr·da+c <sub>12_c</sub> ·nr·nr+c <sub>12_d</sub> ·da·da+c <sub>12_e</sub> )·1e-15
R <sub>1</sub> ( $\Omega$ )	(r <sub>1_a</sub> ·nr·da·da+r <sub>1_b</sub> ·nr+r <sub>1_c</sub> ·da+r <sub>1_d</sub> ·nr·nr+r <sub>1_e</sub> )·(0.0026·(temper-25)+1)
L <sub>1</sub> (H)	(l <sub>1_a</sub> ·nr <sup>(l<sub>1_b</sub>)</sup> ·da <sup>(l<sub>1_c</sub>)</sup> ·do <sup>(l<sub>1_d</sub>)</sup> +l <sub>1_e</sub> ·nr <sup>(l<sub>1_f</sub>)</sup> +l <sub>1_g</sub> )·1.0e-9
L <sub>2</sub> (H)	(l <sub>1_a</sub> ·nr <sup>(l<sub>1_b</sub>)</sup> ·da <sup>(l<sub>1_c</sub>)</sup> ·do <sup>(l<sub>1_d</sub>)</sup> +l <sub>1_e</sub> ·nr <sup>(l<sub>1_f</sub>)</sup> +l <sub>1_g</sub> )·1.0e-9
R <sub>2</sub> ( $\Omega$ )	(r <sub>1_a</sub> ·nr·da·da+r <sub>1_b</sub> ·nr+r <sub>1_c</sub> ·da+r <sub>1_d</sub> ·nr·nr+r <sub>1_e</sub> )·(0.0026·(temper-25)+1)
K <sub>12</sub>	(m <sub>a</sub> ·nr <sup>(m<sub>b</sub>)</sup> ·da <sup>(m<sub>c</sub>)</sup> ·do <sup>(m<sub>d</sub>)</sup> +m <sub>e</sub> ·nr <sup>(m<sub>f</sub>)</sup> +m <sub>g</sub> )
R <sub>s1</sub> ( $\Omega$ )	(rs <sub>a</sub> ·nr·da·da+rs <sub>b</sub> ·nr+rs <sub>c</sub> ·da+rs <sub>d</sub> ·nr·nr+rs <sub>e</sub> )·((0.0026·(temper-25)+1) <sup>(0.5)</sup> )
L <sub>s1</sub> (H)	(ls <sub>a</sub> ·nr <sup>(ls<sub>b</sub>)</sup> ·da <sup>(ls<sub>c</sub>)</sup> ·do <sup>(ls<sub>d</sub>)</sup> +ls <sub>e</sub> ·nr <sup>(ls<sub>f</sub>)</sup> +ls <sub>g</sub> )·1e-9
L <sub>s2</sub> (H)	(ls <sub>a</sub> ·nr <sup>(ls<sub>b</sub>)</sup> ·da <sup>(ls<sub>c</sub>)</sup> ·do <sup>(ls<sub>d</sub>)</sup> +ls <sub>e</sub> ·nr <sup>(ls<sub>f</sub>)</sup> +ls <sub>g</sub> )·1e-9
R <sub>s2</sub> ( $\Omega$ )	(rs <sub>a</sub> ·nr·da·da+rs <sub>b</sub> ·nr+rs <sub>c</sub> ·da+rs <sub>d</sub> ·nr·nr+rs <sub>e</sub> )·((0.0026·(temper-25)+1) <sup>(0.5)</sup> )
C <sub>ox1</sub> (F)	(cox <sub>1</sub> )·((1/(12.503905+(1.7014125)·(lay-3)))/(0.0440289))·1e-15
C <sub>ox2</sub> (F)	(cox <sub>2</sub> )·((1/(12.503905+(1.7014125)·(lay-3)))/(0.0440289))·1e-15
C <sub>ox3</sub> (F)	(cox <sub>1</sub> +cox <sub>2</sub> )·((1/(12.503905+(1.7014125)·(lay-3)))/(0.0440289))·1e-15
R <sub>sub13</sub> ( $\Omega$ )	(rsub <sub>13</sub> )
R <sub>sub32</sub> ( $\Omega$ )	(rsub <sub>13</sub> )
C <sub>sub13</sub> (F)	(csub <sub>13</sub> )
C <sub>sub32</sub> (F)	(csub <sub>13</sub> )
C <sub>sub1</sub> (F)	(csub <sub>1</sub> )
C <sub>sub2</sub> (F)	(csub <sub>2</sub> )
C <sub>sub3</sub> (F)	(csub <sub>1</sub> +csub <sub>2</sub> )
R <sub>sub1</sub> ( $\Omega$ )	(rsub <sub>1</sub> )
R <sub>sub2</sub> ( $\Omega$ )	(rsub <sub>2</sub> )
R <sub>sub3</sub> ( $\Omega$ )	(rsub <sub>1</sub> ·rsub <sub>2</sub> /(rsub <sub>1</sub> +rsub <sub>2</sub> ))
where,	
di	2·rad·1e6
do	2·rad·1e6+2·(nr·(w·1e6+3)-3)
da	(di+do)/2
c <sub>12_a</sub>	-3.487659166
c <sub>12_b</sub>	0.083894075
c <sub>12_c</sub>	0.802478617
c <sub>12_d</sub>	-0.000194149
c <sub>12_e</sub>	0.971886585
r <sub>1_a</sub>	3.72E-06
r <sub>1_b</sub>	0.462524363
r <sub>1_c</sub>	0.002126148
r <sub>1_d</sub>	-0.017932108
r <sub>1_e</sub>	-0.148010545
l <sub>1_a</sub>	0.000291748
l <sub>1_b</sub>	1.533019164
l <sub>1_c</sub>	1.655981779
l <sub>1_d</sub>	-0.442001746
l <sub>1_e</sub>	10.56951658
l <sub>1_f</sub>	0.000256121
l <sub>1_g</sub>	-10.53819606
m <sub>a</sub>	7.536628471
m <sub>b</sub>	0.027843479
m <sub>c</sub>	0.111597388

Component	Scaling Rule
m_d	-0.115535359
m_e	49.56343638
m_f	0.005308
m_g	-56.80037564
rs_a	2.97E-06
rs_b	0.370019491
rs_c	0.001700919
rs_d	-0.014345686
rs_e	-0.118408436
ls_a	0.000132859
ls_b	1.38665634
ls_c	-0.730000302
ls_d	1.775475653
ls_e	-0.018062932
ls_f	1.190352684
ls_g	0.021301163
cox_a	0.052971645
cox_b	7.953175098
rsub_a	-21611.17246
rsub_b	78889.80612
rsub_c	597.1862311
rsub_d	58.76995796
rsub13_a	30
cox_1	cox_a·nr·da+cox_b
cox_2	cox_a·nr·da+cox_b
rsub_1	(rsub_a/(nr·da)+rsub_b/da+rsub_c/nr+rsub_d)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
rsub_2	(rsub_a/(nr·da)+rsub_b/da+rsub_c/nr+rsub_d)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
rsub_13	(0.0000018·nr/((nr·da·3.31372+126)·7.25e-10)·rsub13_a)·(-0.0000114365·(temper-25)·(temper-25)+0.0045985091·(temper-25)+1)
csub_1	1.05315e-11/rsub_1
csub_2	1.05315e-11/rsub_2
csub_13	1.05315e-11/rsub_13

### 13.19.4.2.2 Model Parameter

Table 13.19.4.2.2.1: Equivalent circuit parameters for symmetric inductor with W=9  $\mu$ m.

Nr	1	1	1	1	3	3	3	3	5	5	5	5
Rad( $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
W( $\mu$ m)	9	9	9	9	9	9	9	9	9	9	9	9
Lay	9	9	9	9	9	9	9	9	9	9	9	9
C <sub>12</sub> (fF)	1.263	3.151	5.878	7.207	12.817	19.458	31.694	42.531	38.62	50.016	71.759	92.105
R <sub>1</sub> ( $\Omega$ )	0.385	0.461	0.633	0.831	1.256	1.372	1.664	2.037	2.042	2.219	2.675	3.264
L <sub>1</sub> (nH)	0.054	0.079	0.135	0.197	0.234	0.371	0.682	1.024	0.658	0.971	1.665	2.424
L <sub>2</sub> (nH)	0.054	0.079	0.135	0.197	0.234	0.371	0.682	1.024	0.658	0.971	1.665	2.424
R <sub>2</sub> ( $\Omega$ )	0.385	0.461	0.633	0.831	1.256	1.372	1.664	2.037	2.042	2.219	2.675	3.264
R <sub>s1</sub> ( $\Omega$ )	0.308	0.369	0.506	0.665	1.005	1.098	1.332	1.629	1.634	1.776	2.14	2.611
L <sub>s1</sub> (pH)	12.088	17.055	27.335	37.852	52.446	73.95	120.33	168.46	221.38	262.43	353.69	450.11
L <sub>s2</sub> (pH)	12.088	17.055	27.335	37.852	52.446	73.95	120.33	168.46	221.38	262.43	353.69	450.11
R <sub>s2</sub> ( $\Omega$ )	0.308	0.369	0.506	0.665	1.005	1.098	1.332	1.629	1.634	1.776	2.14	2.611
C <sub>ox1</sub> (fF)	10.019	11.608	14.787	17.965	17.965	22.732	32.267	41.802	30.996	38.942	54.833	70.724
C <sub>ox2</sub> (fF)	10.019	11.608	14.787	17.965	17.965	22.732	32.267	41.802	30.996	38.942	54.833	70.724
C <sub>ox3</sub> (fF)	20.038	23.216	29.573	35.93	35.93	45.464	64.534	83.604	61.992	77.883	109.67	141.45
R <sub>sub13</sub> ( $\Omega$ )	291.82	210.02	134.57	99.008	297.02	212.7	135.67	99.6	237.59	180.39	121.76	91.891
R <sub>sub32</sub> ( $\Omega$ )	291.82	210.02	134.57	99.008	297.02	212.7	135.67	99.6	237.59	180.39	121.76	91.891
C <sub>sub13</sub> (fF)	36.089	50.145	78.258	106.37	35.457	49.513	77.626	105.74	44.326	58.383	86.495	114.61
C <sub>sub32</sub> (fF)	36.089	50.145	78.258	106.37	35.457	49.513	77.626	105.74	44.326	58.383	86.495	114.61
C <sub>sub1</sub> (fF)	4.957	7.087	9.574	10.982	7.546	10.238	14.499	17.718	10.172	12.914	17.567	21.369
C <sub>sub2</sub> (fF)	4.957	7.087	9.574	10.982	7.546	10.238	14.499	17.718	10.172	12.914	17.567	21.369
C <sub>sub3</sub> (fF)	9.914	14.174	19.149	21.963	15.091	20.476	28.998	35.437	20.345	25.827	35.135	42.738
R <sub>sub1</sub> (K $\Omega$ )	2.125	1.486	1.1	0.959	1.396	1.029	0.726	0.594	1.035	0.816	0.599	0.493
R <sub>sub2</sub> (K $\Omega$ )	2.125	1.486	1.1	0.959	1.396	1.029	0.726	0.594	1.035	0.816	0.599	0.493
R <sub>sub3</sub> (K $\Omega$ )	1.062	0.743	0.55	0.48	0.698	0.514	0.363	0.297	0.518	0.408	0.3	0.246
K	0.016	0.071	0.099	0.106	0.335	0.423	0.501	0.536	0.495	0.577	0.666	0.713

### 13.19.4.2.3 Model Error Table

Symmetric inductor(SYM) fitting error between measurement and simulation are summarized in Table 13.19.4.2.3.1 to Table 13.19.4.2.3.4. For each device four Y-parameter fitting errors are separated with real part and imaginary part.

**Table 13.19.4.2.3.1: Fitting errors (Real and Imaginary) for symmetric inductor with W=3  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	15.89	13.26	11.00	16.06	12.35	3.43	0.68	1.91	5.50	1.61	1.70	4.67
Real(Y21)(%)	15.89	13.26	11.02	16.08	12.35	3.42	0.58	1.93	5.52	1.71	1.80	4.80
Real(Y12)(%)	15.90	13.26	11.00	16.06	12.35	3.44	0.58	1.84	5.51	1.58	1.73	4.67
Real(Y22)(%)	15.89	13.26	11.01	16.07	12.35	3.43	0.67	1.96	5.53	1.66	1.79	4.80
Imag(Y11)(%)	7.27	6.19	4.80	5.91	5.89	2.48	1.17	0.97	1.36	1.37	0.83	0.78
Imag(Y21)(%)	7.24	6.19	4.98	6.38	5.83	2.45	1.56	2.00	1.47	0.88	0.96	0.93
Imag(Y12)(%)	7.23	6.18	4.95	6.36	5.82	2.41	1.49	1.92	1.45	0.86	0.95	0.94
Imag(Y22)(%)	7.25	6.18	4.80	5.91	5.89	2.46	1.14	0.99	1.34	1.36	0.84	0.80

**Table 13.19.4.2.3.2: Fitting errors (Real and Imaginary) for symmetric inductor with W=6  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	43.33	32.69	22.76	20.63	11.86	11.57	15.74	16.41	13.32	11.45	12.65	13.86
Real(Y21)(%)	43.35	32.71	22.78	20.66	11.88	11.62	15.81	16.59	13.39	11.62	12.90	14.13
Real(Y12)(%)	43.32	32.69	22.74	20.62	11.84	11.53	15.70	16.36	13.28	11.35	12.62	13.86
Real(Y22)(%)	43.34	32.70	22.76	20.63	11.86	11.57	15.73	16.49	13.32	11.49	12.80	14.00
Imag(Y11)(%)	7.56	4.58	2.91	3.10	3.98	2.59	3.07	2.69	2.33	1.67	3.28	2.54
Imag(Y21)(%)	7.52	4.57	3.25	4.57	4.01	2.45	3.01	2.81	2.41	1.73	3.25	2.55
Imag(Y12)(%)	7.54	4.58	3.28	4.55	3.99	2.46	3.01	2.79	2.42	1.69	3.24	2.48
Imag(Y22)(%)	7.54	4.56	2.93	3.19	3.98	2.58	3.05	2.68	2.37	1.66	3.30	2.55

**Table 13.19.4.2.3.3: Fitting errors (Real and Imaginary) for symmetric inductor with W=9  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	47.81	35.87	32.67	33.56	27.33	26.48	14.84	20.06	27.12	19.12	9.10	8.46
Real(Y21)(%)	47.87	35.94	32.73	33.60	27.39	26.56	16.48	20.30	27.21	19.31	9.38	8.81
Real(Y12)(%)	47.76	35.81	32.61	33.54	27.29	26.44	16.06	20.01	27.13	19.09	9.07	8.51
Real(Y22)(%)	47.82	35.88	32.67	33.56	27.34	26.49	15.24	20.14	27.11	19.17	9.25	8.69
Imag(Y11)(%)	6.44	3.23	4.46	4.93	3.42	3.27	0.85	2.74	1.40	3.12	0.71	1.03
Imag(Y21)(%)	6.43	3.20	4.60	5.43	3.53	3.26	1.33	2.87	1.77	3.18	0.87	1.72
Imag(Y12)(%)	6.43	3.21	4.60	5.43	3.54	3.27	1.30	2.83	1.79	3.15	0.86	1.63
Imag(Y22)(%)	6.42	3.21	4.47	4.95	3.44	3.25	0.84	2.75	1.39	3.14	0.69	0.95

**Table 13.19.4.2.3.4: Fitting errors (Real and Imaginary) for symmetric inductor with W=15  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	41.45	36.31	26.45	30.08	23.19	24.08	24.65	21.78	22.24	24.76	9.53	2.27
Real(Y21)(%)	42.52	37.76	27.99	34.84	25.00	25.92	25.91	22.29	24.65	25.30	9.91	1.80
Real(Y12)(%)	42.52	37.78	27.97	34.50	24.53	25.28	25.28	21.77	24.11	24.86	9.54	1.61
Real(Y22)(%)	41.48	36.28	26.30	30.32	23.12	23.97	24.72	21.89	22.29	24.92	9.71	2.37
Imag(Y11)(%)	3.34	2.82	2.85	2.16	3.66	2.67	4.32	1.38	3.74	3.42	0.56	1.04
Imag(Y21)(%)	3.36	3.01	3.60	4.28	4.19	2.85	4.38	1.67	4.21	3.56	0.66	0.77
Imag(Y12)(%)	3.37	3.02	3.61	4.31	4.20	2.85	4.36	1.63	4.22	3.51	0.62	0.80
Imag(Y22)(%)	3.31	2.82	2.89	2.22	3.70	2.65	4.33	1.40	3.74	3.43	0.57	1.03

### 13.19.4.2.4 Model Error Table

Symmetric inductor with center tap (SYMCT) fitting error between measurement and simulation are summarized in Table 13.19.4.3.4.1 to Table 13.19.4.3.4.4. For each device four Y-parameter fitting errors are separated with real part and imaginary part.

**Table 13.19.4.2.4.1: Fitting errors (Real and Imaginary) for SYMCT inductor with W=3  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	17.75	9.81	17.01	16.62	9.56	5.87	4.71	0.98	5.55	3.11	2.85	5.72
Real(Y21)(%)	24.21	12.78	68.38	17.34	14.60	7.41	13.78	2.38	9.25	3.16	5.79	6.98
Real(Y12)(%)	24.47	12.93	68.05	17.38	14.75	7.41	13.57	2.45	9.29	3.17	5.84	7.01
Real(Y22)(%)	24.52	14.79	15.81	18.28	8.65	3.09	5.13	1.88	4.92	1.56	5.12	4.06
Imag(Y11)(%)	11.46	6.37	6.08	10.34	10.94	5.73	3.68	0.74	2.81	2.97	2.32	6.78
Imag(Y21)(%)	18.60	8.76	73.19	14.62	15.52	8.06	9.63	1.83	8.99	2.80	6.04	6.70
Imag(Y12)(%)	18.77	8.87	72.76	14.78	15.60	8.09	9.54	1.93	8.99	2.85	6.09	6.70
Imag(Y22)(%)	16.11	10.74	6.42	11.70	8.80	2.64	4.06	2.78	2.63	1.53	7.46	3.22

**Table 13.19.4.2.4.2: Fitting errors (Real and Imaginary) for SYMCT inductor with W=6  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	40.79	31.55	26.11	19.05	9.11	7.27	3.65	2.82	3.20	4.08	4.86	4.91
Real(Y21)(%)	46.36	36.13	28.88	20.05	17.08	25.68	11.55	18.00	20.28	14.33	11.38	11.63
Real(Y12)(%)	46.23	35.95	28.67	20.23	16.89	25.95	11.44	18.01	19.96	14.51	11.55	11.65
Real(Y22)(%)	39.03	29.40	24.78	23.63	10.88	6.57	2.40	2.43	1.36	1.89	3.97	5.60
Imag(Y11)(%)	14.45	8.78	7.28	8.70	3.54	6.49	5.91	5.45	3.51	3.26	3.60	5.94
Imag(Y21)(%)	16.23	8.65	7.59	12.22	5.37	5.97	6.81	8.96	7.76	8.21	7.72	9.00
Imag(Y12)(%)	16.21	8.60	7.60	12.38	5.48	6.09	6.99	9.10	7.91	8.40	7.85	8.96
Imag(Y22)(%)	13.90	8.14	7.02	11.96	6.37	5.52	3.54	8.43	4.36	5.88	5.19	4.46

**Table 13.19.4.2.4.3: Fitting errors (Real and Imaginary) for SYMCT inductor with W=9  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	48.96	37.75	27.43	40.71	22.53	14.92	6.96	4.75	2.13	2.72	0.86	1.53
Real(Y21)(%)	60.32	47.57	33.41	68.23	15.12	16.50	20.67	16.23	11.26	14.06	2.09	3.22
Real(Y12)(%)	60.50	47.32	32.84	68.11	15.27	16.49	20.46	16.37	11.38	13.93	2.21	3.27
Real(Y22)(%)	45.24	34.62	25.97	37.97	20.28	13.85	5.32	5.93	2.56	1.38	1.55	2.07
Imag(Y11)(%)	6.81	9.00	9.03	9.98	4.65	4.00	4.03	2.36	2.63	2.25	0.78	1.12
Imag(Y21)(%)	6.69	8.38	5.87	8.24	5.57	7.28	6.21	8.12	11.93	5.78	3.41	4.97
Imag(Y12)(%)	6.71	8.33	5.69	8.27	5.57	7.29	6.10	7.94	11.79	5.79	3.32	4.96
Imag(Y22)(%)	6.30	8.20	7.65	9.73	4.06	3.90	4.15	6.64	5.17	3.23	1.17	2.20

**Table 13.19.4.2.4.4: Fitting errors (Real and Imaginary) for SYMCT inductor with W=15  $\mu$  m.**

N (turns)	1	1	1	1	3	3	3	3	5	5	5	5
R(radius in $\mu$ m)	15	30	60	90	15	30	60	90	15	30	60	90
Real(Y11)(%)	37.36	38.39	44.88	40.83	18.34	7.09	2.98	1.55	6.93	8.00	12.16	13.98
Real(Y21)(%)	59.82	68.20	70.20	76.39	14.72	9.47	9.78	10.04	18.08	23.81	18.00	17.41
Real(Y12)(%)	59.70	68.55	70.17	76.90	15.09	9.31	9.76	10.17	18.10	23.93	18.12	17.40
Real(Y22)(%)	34.17	31.86	36.76	34.38	16.30	12.61	6.34	1.88	7.60	8.09	11.55	14.13
Imag(Y11)(%)	5.54	3.95	5.45	5.81	4.72	2.34	2.63	2.38	10.04	7.22	7.24	8.17
Imag(Y21)(%)	5.51	4.94	5.98	7.50	6.16	5.76	5.38	5.12	11.78	11.34	15.33	17.86
Imag(Y12)(%)	5.50	4.95	6.06	7.58	6.18	5.57	5.37	4.94	11.74	11.35	15.35	17.82
Imag(Y22)(%)	5.12	3.98	8.48	8.46	3.94	5.71	6.99	2.24	9.00	6.90	7.57	8.21

## 13.19.5 Corner Model Table

The skew parameters are listed below for corner-case simulation. The worst case is determined on the variation of Q-value. Users can use these parameters in the model file to generate the worst-case simulation.

**Table 13.19.5.1: Corner parameters for inductor model.**

Skew Parameter	SS	TT	FF
rm9_indfac	1.1	1.0	0.9
cm9_indfac	1.07	1.0	0.913
c12_indfac	1.081	1.0	0.926
rsub_indfac	1.2	1.0	0.8
csub_indfac	0.8333	1.0	1.25
I_indfac	1.0235	1.0	0.9762

## 13.19.6 Temperature Effect Model

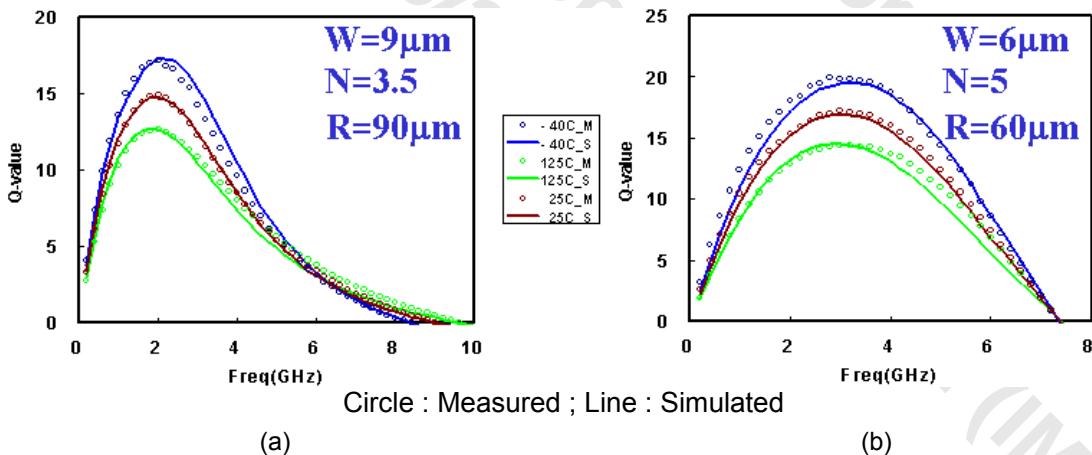
The temperature effect was analyzed through characterization of S-parameters. Two kinds of inductors (standard and symmetric inductor) were measured with three different temperatures (-40°C, 25°C, and 125°C) to characterize this effect. The following functions have been implemented into the model for temperature effect simulation.

$$R(T)=R*(0.0026*(temper-25)+1)$$

$$Rs(T)=Rs*(0.0026*(temper-25)+1)*0.5$$

$$Rsub(T)=Rsub*(-0.0000114*(temper-25)+0.0046*(temper-25)+1)$$

The variation of Q with different temperature depends upon two key factors: 1. Spiral metal(UTM) TCR 2. Substrate resistance TCR. The spiral metal has a positive TCR, which increases resistance in the inductor as the temperature is increasing. This effect decreases the Q-value. The substrate resistance also has a positive temperature coefficient. This effect enhances Q-value at high frequency. Fig. 13.19.6.1 shows the simulated and measured data for three different temperatures.



**Fig. 13.19.6.1: (a) Standard inductor (b) Symmetric inductor**

## 13.19.7 Variable metal layer Model

The variable metal layer model was characterized by three different back-end processes, which are four metal, seven metal and nine metal schemes. The following function has been implemented into the model for metal layer simulation.

$$\text{Cox}(\text{layer}) = \text{Cox}(\text{layer}=9) * [(1/(12.5039 + (1.7014 * (\text{layer}-3))) / (0.0444))]$$

The variation of Q with different metal layers (1P4M ~ 1P9M) is caused by the varying capacitance between the spiral and substrate. This increasing capacitance (Cox) causes Q-value to decrease. Fig. 13.19.7.1 shows the simulated and measured data for three different layers.

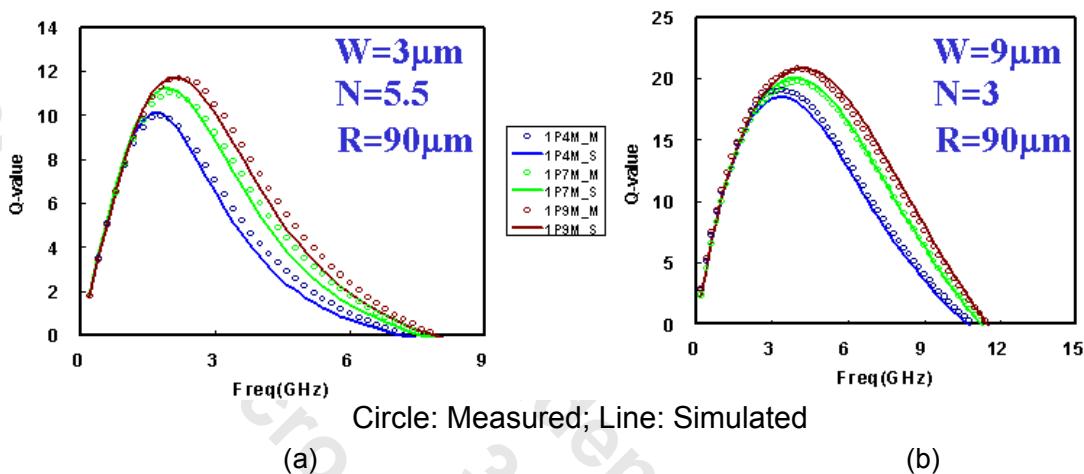


Fig. 13.19.7.1: (a) Standard inductor (b) Symmetric inductor

## 13.19.8 Statistical Model

In this version inductor provides statistical model and their corresponding corner models. Whenever the corners of inductor were provided, their statistical model was made accordingly based on PCA result. Statistical libraries for Monte-Carlo simulation are denoted by MC. RF models are labeled as "RFIND". For example, the library "TT\_RFIND" is for typical RF model; "MC\_RFIND" for statistical RF model. The simulation results with corner of inductor are shown in Fig.13.19.8.1.

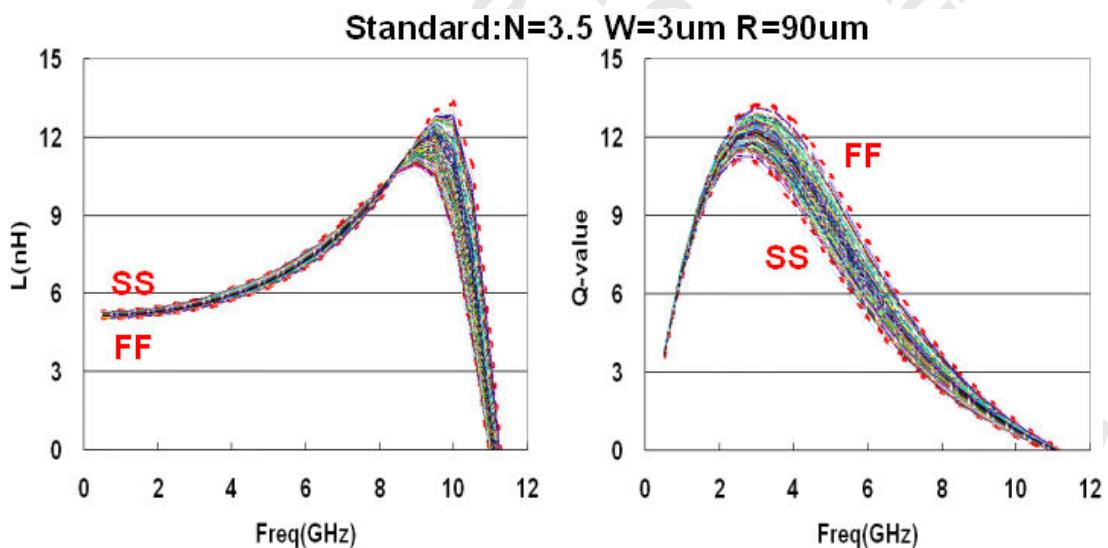


Fig. 13.19.8.1: Simulation results of 250 Monte-Carlo random tests.

# Appendix A Revision History

## A.1 T-N90-LO-DR-001 (Logic)

### A.1.1 From Version 0.1 to Version 0.2

From Version 0.1 to Version 0.2				
Rule	Sec. No.	Section Title	Revision Description	
1.		Title	Changes document title to "90nm Logic General Purpose 1P9M Salicide 1.0V/1.8V, 1.0V/2.5V, 1.0V/3.3V, 1.0V/1.8V/3.3V Design Rule"	
2.	G.3		Modifies G.3 rule wording to "Only shapes that are orthogonal or on a 45 degree angle are allowed."	
3.	0.1		Zigzag patterns (small): Modifies recommendation #10 wording to avoid small zigzag patterns (suggest $\geq$ half of minimum dimension of each layer for each segment of zigzag). Jogs (small): Modifies recommendation #10 wording to avoid small jogs (suggest $\geq$ half of minimum dimension of each layer).	
4.	0.1		Jogs (small): Modifies recommendation #10 wording to avoid small jogs (suggest $\geq$ half of minimum dimension of each layer).	
5.	0.3		Changes special layer "RHDMY" to "RH."	
6.	0.3		Changes special layer "DMSRM" to "SRM."	
7.	0.3		Changes special layer "ESD3DMY" to "ESD3."	
8.	0.3		Changes special layer "VARDMY" to "VAR"	
9.	0.3		Adds special layer RFDMY for RF application in mixed-signal circuits.	
10.	1.7		Adds two masking steps: One pre-doping masking step before poly using NP mask One P+ implantation masking step for 2.5V/3.3V I/O using P2V mask.	
11.	NW.S.2	2.11	NW	Modifies wording of the NW.S.2 N-Well rule to "Minimum space between two NW1V or two NW2V (NW3V) regions with the same potential. Merge if space is less than this value."
12.	NW.S.3	2.11	NW	Modifies wording of the NW.S.3 rule to "Minimum space between an NW1V and an NW2V (NW3V), two NW2V (NW3V) with different potentials, or a notch in a hot NW2V (NW3V) region. The maximum applied voltage is greater than 1.0V but less than or equal to 2.5V or 3.3V."
13.	NWR.R.1	2.1.2.1	NW	Modifies wording of the NWR.R.1 rule (NW resistor under OD) to "PP/NP/VTH_N/VTH_P/VTL_N/VTL_P overlapped NW resistor (within OD) region is not allowed."
14.	NWR.R.2	2.1.2.2	NW	Adds NWR.R.2 (NW resistor under STI) rule: "PP/NP/VTH_N/VTH_P/VTL_N/VTL_P overlapped NW resistor (within OD) region is not allowed"
15.	DNW.I.1	2.13	DNW	Modifies wording of DNW.I.1 rule to "DNW edge must be enclosed by NW."
16.	DNW.I.5	2.13	DNW	Deletes DNW.I.5 rule.
17.	NT_N	2.2	NT_N	Adds description for the NT_N section: "This layer is used for mask making, instead of process requirement. If using native NMOS devices in circuit design, please use this drawn layer with NW to generate P-well. This native NMOS device is based on [a] general purpose standard $v_t$ device. It cannot be applied to pure low $v_t$ designs."
18.	NT_N.W.2	2.2	NT_N	Changes NT_N.W.2 rule to 0.2 $\mu\text{m}$ from 0.25 $\mu\text{m}$ .
19.	NT_N.W.4	2.2	NT_N	Adds NT_N.W.4 rule for 1.8V native device gate length.
20.	NT_N.S.1	2.2	NT_N	Modifies NT_N.S.1 rule wording to "Minimum space between two NT_N regions."

## From Version 0.1 to Version 0.2

Rule	Sec. No.	Section Title	Revision Description
21. NT_N.W.5	2.2	NT_N	Adds NT_N.W.5 rule: Minimum OD width of native device [is] 0.5 $\mu\text{m}$ .
22. OD.S.1.2	2.3.1	OD	Adds OD.S.1.2 rule: "Minimum space between two ODs crossed by a common poly gate if at least one of the corresponding OD regions has a width > 0.23 $\mu\text{m}$ , and if a PO is crossing one of the ODs $\leq$ 0.16 $\mu\text{m}$ away from the other OD." 0.16 $\mu\text{m}$ .
23. OD.L.2	2.3.1	OD	Adds OD.L.2 rule: "Maximum OD length between 2 contacts and between one contact at the OD line end when OD width is $\leq$ 0.15 $\mu\text{m}$ ." 25 $\mu\text{m}$ .
24. OD.R.1	2.3.1	OD	Adds OD.R.1 rule: "OD must be fully covered by N+/P+ except for dummy OD."
25. OD	2.3.1	OD	Deletes recommendation for max. OD length between 2 contacts.
26. DOD	2.3.2	DOD	Adds wording "Dummy OD/PO gds layer data type is 1."
27. DOD.C.3	2.3.2	DOD	Deletes DOD.C.3 rule.
28. DOD.E.2	2.3.2	DOD	Deletes DOD.E.2 rule.
29. DOD.E.3	2.3.2	DOD	Deletes DOD.E.3 rule.
30. PO.W.1.1	2.4	PO	Changes PO.W.1.1 rule to 0.28 $\mu\text{m}$ from 0.3 $\mu\text{m}$ .
31. PO.W.2.1	2.4	PO	Changes PO.W.2.1 rule to 0.28 $\mu\text{m}$ from 0.3 $\mu\text{m}$ .
32. PO.W.1.2	2.4	PO	Changes PO.W.1.2 rule to 0.38 $\mu\text{m}$ from 0.4 $\mu\text{m}$ .
33. PO.W.2.2	2.4	PO	Changes PO.W.1.2 rule to 0.38 $\mu\text{m}$ from 0.4 $\mu\text{m}$ .
34. PO.C.1.1	2.4	PO	Adds PO.C.1.1 rule: "Minimum clearance from an L-shape OD to a related PO on the field oxide, where channel width is < 0.2 $\mu\text{m}$ . (It is strongly recommended to keep 0.1 $\mu\text{m}$ clearance for all OD width to obtain better performance.)" 0.10um.
35. PO.O.1.1	2.4	PO	Modifies wording of PO.O.1.1 rule to "Minimum overlap of a PO extended into field oxide (end-cap) when L-shape OD to PO clearance is < 0.1 $\mu\text{m}$ and OD width is $\geq$ 0.2 $\mu\text{m}$ ."
36. PO.L.1	2.4	PO	Adds PO.L.1 rule: "Maximum poly length between 2 contacts and between one contact at the poly line end when poly width is $\leq$ 0.13 $\mu\text{m}$ ." 25 $\mu\text{m}$ .
37. PO	2.4	PO	Deletes recommendation for max. PO length between 2 contacts.
38. VTH_N	2.5.1	VTH_N	Adds description to VTH_N rule: "VTH_N is only applied for 1.0V. It is not allowed in 1.8V/2.5V/3.3V."
39. VTH_N.W.1	2.5.1	VTH_N	Changes VTH_N.W.1 rule to 0.4 $\mu\text{m}$ from 0.28 $\mu\text{m}$ .
40. VTH_N.S.1	2.5.1	VTH_N	Changes VTH_N.S.1 rule to 0.24 $\mu\text{m}$ from 0.28 $\mu\text{m}$ .
41. VTH_N.E.2	2.5.1	VTH_N	Changes VTH_N.E.2 rule to 0.23 $\mu\text{m}$ from 0.29 $\mu\text{m}$ .
42. VTH_N.C.2	2.5.1	VTH_N	Changes VTH_N.C.2 rule to 0.23 $\mu\text{m}$ from 0.17 $\mu\text{m}$
43. VTH_N.A.1	2.5.1	VTH_N	Changes VTH_N.A.1 rule to 0.4 $\mu\text{m}^2$ from 0.122 $\mu\text{m}^2$ .
44. VTH_N.A.2	2.5.1	VTH_N	Changes VTH_N.A.2 rule to 0.4 $\mu\text{m}^2$ from 0.122 $\mu\text{m}^2$ .
45. VTH_N.C.3	2.5.1	VTH_N	Changes VTH_N.C.3 rule to 0.26 $\mu\text{m}$ from 0.2 $\mu\text{m}$ .
46. VTH_P	2.5.2	VTH_P	Adds description: "VTH_P is only applied for 1.0V. It is not allowed in 1.8V/2.5V/3.3V."
47. VTH_P.W.1	2.5.2	VTH_P	Changes rule to 0.4 $\mu\text{m}$ from 0.28 $\mu\text{m}$ .
48. VTH_P.S.1			Changes rule to 0.24 $\mu\text{m}$ from 0.28 $\mu\text{m}$ .
49. VTH_P.E.2	2.5.2	VTH_P	Changes rule to 0.23 $\mu\text{m}$ from 0.29 $\mu\text{m}$ .
50. VTH_P.C.2	2.5.2	VTH_P	Changes rule to 0.23 $\mu\text{m}$ from 0.17 $\mu\text{m}$ .
51. VTH_P.A.1	2.5.2	VTH_P	Changes rule to 0.4 $\mu\text{m}^2$ from 0.122 $\mu\text{m}^2$ .
52. VTH_P.A.2	2.5.2	VTH_P	Changes rule to 0.4 $\mu\text{m}^2$ from 0.122 $\mu\text{m}^2$ .
53. VTH_P.C.3	2.5.2	VTH_P	Changes rule to 0.26 $\mu\text{m}$ from 0.2 $\mu\text{m}$ .
54. VTL_N	2.5.3	VTL_N	Adds description: "VTL_N is only applied for 1.0V. It is not allowed in 1.8V/2.5V/3.3V."
55. VTL_N.W.1	2.5.3	VTL_N	Changes VTL_N.W.1 rule to 0.4 $\mu\text{m}$ from 0.28 $\mu\text{m}$ .
56. VTL_N.S.1	2.5.3	VTL_N	Changes VTL_N.S.1 rule to 0.24 $\mu\text{m}$ from 0.28 $\mu\text{m}$ .
57. VTL_N.E.2	2.5.3	VTL_N	Changes VTL_N.E.2 rule to 0.23 $\mu\text{m}$ from 0.29 $\mu\text{m}$ .
58. VTL_N.C.2	2.5.3	VTL_N	Changes VTL_N.C.2 rule to 0.23 $\mu\text{m}$ from 0.17 $\mu\text{m}$ .
59. VTL_N.A.1	2.5.3	VTL_N	Changes VTL_N.A.1 rule to 0.4 $\mu\text{m}^2$ from 0.122 $\mu\text{m}^2$ .
60. VTL_N.A.2	2.5.3	VTL_N	Changes VTL_N.A.2 rule to 0.4 $\mu\text{m}^2$ from 0.122 $\mu\text{m}^2$ .
61. VTL_N.C.3	2.5.3	VTL_N	Changes VTL_N.C.3 rule to 0.26 $\mu\text{m}$ from 0.2 $\mu\text{m}$ .

## From Version 0.1 to Version 0.2

Rule	Sec. No.	Section Title	Revision Description
62.	VTL_P	2.5.4	VTL_P
			Adds description: "VTL_P is only applied for 1.0V. It is not allowed in 1.8V/2.5V/3.3V."
63.	VTL_P.W.1	2.5.4	VTL_P
			Changes VTL_P.W.1 rule <b>to</b> 0.4 $\mu\text{m}$ <b>from</b> 0.28 $\mu\text{m}$ .
64.	VTL_P.S.1	2.5.4	VTL_P
			Changes VTL_P.S.1 rule <b>to</b> 0.24 $\mu\text{m}$ <b>from</b> 0.28 $\mu\text{m}$ .
65.	VTL_P.E.2	2.5.4	VTL_P
			Changes VTL_P.E.2 rule <b>to</b> 0.23 $\mu\text{m}$ <b>from</b> 0.29 $\mu\text{m}$ .
66.	VTL_P.C.2	2.5.4	VTL_P
			Changes VTL_P.C.2 rule <b>to</b> 0.23 $\mu\text{m}$ <b>from</b> 0.17 $\mu\text{m}$ .
67.	VTL_P.A.1	2.5.4	VTL_P
			Changes VTL_P.A.1 rule <b>to</b> 0.4 $\mu\text{m}^2$ <b>from</b> 0.122 $\mu\text{m}^2$ .
68.	VTL_P.A.2	2.5.4	VTL_P
			Changes VTL_P.A.2 rule to 0.4 $\mu\text{m}^2$ <b>from</b> 0.122 $\mu\text{m}^2$ .
69.	VTL_P.C.3	2.5.4	VTL_P
			Changes VTL_P.C.3 rule <b>to</b> 0.26 $\mu\text{m}$ <b>from</b> 0.2 $\mu\text{m}$ .
70.	PP.C.2	2.6.1	P + S/D I/I
			Modifies wording of PP.C.2 rule to "Minimum clearance from a PP inside N-well to a non-butted edge of N-well pick-up N+OD."
71.	PP.C.4	2.6.1	P + S/D I/I
			Modifies wording of PP.C.4 rule to "Minimum clearance from a PP edge on OD to a P-Channel PO gate."
72.	PP.C.6	2.6.1	P + S/D I/I
			Modifies wording of PP.C.6 rule to "Minimum clearance from a butted P+ to the related Poly gate if butting N+ OD extending 0 < J < 0.22 $\mu\text{m}$ in PW. When J = 0, please refer to OC.C.6."
73.	PP.R.1	2.6.1	P + S/D I/I
			Adds wording to PP.R.1 rule: "Dummy poly without implant is allowed."
74.	PP.R.3	2.6.1	P + S/D I/I
			Adds PP.R.3 rule: "OD must be covered by N+/P+ except for dummy OD."
75.	NP.C.2	2.6.2	N+ S/D I/I
			Modifies wording of NP.C.2 rule to "Minimum clearance from a NP inside P-well to a non-butted edge of P-well pick-up P+OD."
76.	NP.C.4	2.6.2	N+ S/D I/I
			Modifies wording of NP.C.4 rule to "Minimum clearance from a NP edge on OD to an N-Channel PO gate."
77.	NP.C.6	2.6.2	N+ S/D I/I
			Modifies wording of NP.C.6 rule to "Minimum clearance from a butted NP to the related Poly gate if butting P+ OD extending 0 < J < 0.22 $\mu\text{m}$ in NW. When J=0, please refer to OC.C.6."
78.	NP.R.1	2.6.2	N+ S/D I/I
			Adds wording to NP.R.1 rule: "Dummy poly without implant is allowed."
79.	NP.R.3	2.6.2	N+ S/D I/I
			Adds NP.R.3 rule: "OD must be fully covered by N+/P+ except for dummy OD."
80.	LDN.E.3	2.6.3	LDL Mask Logic Operation
			Adds LDN.E.3 rule.
81.	LDN.E.4,	2.6.3	LDL Mask Logic Operation
			Adds LDN.E.4 rule.
82.	LDP.E.3	2.6.3	LDP Mask Logic Operation
			Adds LDP.E.3 rule.
83.	LDP.E.4.	2.6.3	LDP Mask Logic Operation
			Adds LDP.E.4 rule.
84.	VT.E.1	2.6.3	VT Mask Logic Operation
			Adds VT.E.1 rule.
85.	VT.C.1	2.6.3	VT Mask Logic Operation
			Adds VT.C.1 rule.
86.	VT.E.2	2.6.3	VT Mask Logic Operation
			Adds VT.E.2 rule.
87.	CO.S.2	2.8	CO
			Modifies wording of CO.S.2 rule to "Minimum space between two CO within a contact array where there is at least a CO with equal or more than 3-neighboring CO."
88.	M1.S.2.1~5	2.9	MI
			Deletes wording of M1.S.2.1~5 rules: "The space inside metal hole is checked without parallel run length. Minimum metal hole length is 20 $\mu\text{m}$ ."
89.	M1.A.1	2.9	MI
			Changes M1.A.1 rule <b>to</b> 0.058 $\mu\text{m}^2$ <b>from</b> 0.059 $\mu\text{m}^2$ .
90.	M1.A.2	2.9	MI
			Modifies wording of M1.A.2 rule to "Minimum M1 enclosed area when M1 width is $\geq 0.12 \mu\text{m}$ " and changes rule <b>to</b> 0.2 $\mu\text{m}^2$ <b>from</b> 0.16 $\mu\text{m}^2$ .
91.	M1.A.2.1	2.9	MI
			Adds M1.A.2.1 rule: "Minimum M1 enclosed area when M1 width is $> 0.18 \mu\text{m}$ ." 0.8 $\mu\text{m}^2$ .
92.	M1.A.2.2	2.9	MI
			Adds M1.A.2.2 rule: "Minimum M1 enclosed area when M1 width is $> 0.15 \mu\text{m}$ ." 3.2 $\mu\text{m}^2$ .
93.	M1.A.2.3	2.9	MI
			Adds M1.A.2.3 rule: "Minimum M1 enclosed area when M1 width is $> 0.3 \mu\text{m}$ ." 7.2 $\mu\text{m}^2$ .

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Rule	Sec. No.	Section Title	Revision Description
94. M1.A.2.4	2.9	MI	Adds M1.A.2.4 rule: "Minimum M1 enclosed area when M1 width is > 4.5 $\mu\text{m}$ ." 20.2 $\mu\text{m}^2$ .
95. M1.A.2.5	2.9	MI	Adds M1.A.2.5 rule: "Minimum M1 enclosed area when M1 width is > 7.5 $\mu\text{m}$ ." 51.8 $\mu\text{m}^2$ .
96. M1.R.2	2.9	MI	Deletes M1.R.2 rule.
97. M1.S.5	2.9	MI	Modifies wording of M1.S.5 rule to "If 2 or more parallel metals are within the range of wide metal ( $W_n > 1.5\mu\text{m}$ ) spacing ( $S_n$ ), the spacing between these metals should be $\geq S_n$ . $W_n$ , $S_n$ are defined by M1.S.2.2 – M1.S.2.5."
98. M1.R.1	2.9	MI	Adds wording to M1.R.1 rule: "It is a must to use data type 1 for dummy metal to reduce DRC, OPC processing time (~50%) and errors."
99. M1	2.9	MI	Adds note: "Bond pad sizing up 2 $\mu\text{m}$ area don't need to check M1.A.2.1-5."
100. VIAx.R.4	2.10	VIAx	Changes wording of VIAx.R.4 rule to "At least 2 vias with space $\leq 0.29(S_1)$ , or at least 4 vias with space $\leq 0.57 \mu\text{m}$ ( $S_1'$ ) are required to connect $M_x$ to $M_{x+1}$ when one of these 2 metals have both length and width ( $W_1$ ) $> 0.42 \mu\text{m}$ ."
101. VIAx.R.5	2.10	VIAx	Changes wording of VIAx.R.5 rule to "At least 4 vias with space $\leq 0.29(S_2)$ , or at least 9 vias with space $\leq 0.77 \mu\text{m}$ ( $S_2'$ ) are required to connect $M_x$ to $M_{x+1}$ when one of these 2 metals have both length and width ( $W_1$ ) $> 0.98 \mu\text{m}$ ."
102. VIAx.S.2	2.10	VIAx	Changes wording of VIAx.S.2 rule to "Minimum space between VIAx to 3-neighboring VIAx or 4-neighboring VIAx."
103. Mx.S.2.1, 3 – 5	2.11	Mx	Deletes wording of Mx.S.2.1, 3-5 rules: "The space inside metal hole is checked without parallel run length. Minimum metal hole length is 20 $\mu\text{m}$ ."
104. Mx.S.2.2	2.11	Mx	Changes the wording of the MxS.2.2 rule to "Minimum space between two parallel metal lines with one or both metal line whose width is larger than 1.50 ( $W_2$ ) $\mu\text{m}$ and the parallel length is larger than 1.5 ( $L_2$ ) $\mu\text{m}$ ."
105. MxA.2	2.11	Mx	Modifies wording of MxA.2 to "Minimum $M_x$ enclosed area when $M_x$ width is $\geq 0.14 \mu\text{m}$ ."
106. MxA.2.1	2.11	Mx	Add MxA.2.1 rule: "Minimum $M_x$ enclosed area when $M_x$ width is $> 0.21\mu\text{m}$ ." 0.8 $\mu\text{m}^2$ .
107. MxA.2.2	2.11	Mx	Adds MxA.2.2 rule: "Minimum $M_x$ enclosed area when $M_x$ width is > 1.5 $\mu\text{m}$ ." 3.2 $\mu\text{m}^2$ .
108. MxA.2.3	2.11	Mx	Adds MxA.2.3 rule: "Minimum $M_x$ enclosed area when $M_x$ width is > 3 $\mu\text{m}$ ." 7.2 $\mu\text{m}^2$ .
109. MxA.2.4	2.11	Mx	Adds MxA.2.4 rule: "Minimum $M_x$ enclosed area when $M_x$ width is > 4.5 $\mu\text{m}$ ." 20.2 $\mu\text{m}^2$ .
110. MxA.2.5	2.11	Mx	Adds MxA.2.5 rule: "Minimum $M_x$ enclosed area when $M_x$ width is > 7.5 $\mu\text{m}$ ." 51.8 $\mu\text{m}^2$ .
111. M9.R.2	2.11	Mx	Deletes M9.R.2 rule.
112. M9.S.5	2.11	Mx	Modifies wording of M9.S.5 to "If 2 or more parallel metals are within the range of wide metal ( $W_n > 1.5 \mu\text{m}$ ) spacing ( $S_n$ ), the spacing between these metals should be $\geq S_n$ . $W_n$ , $S_n$ are defined by Mx.S.2.2 – Mx.S.2.5."
113. M9.R.1	2.11	Mx	Adds wording to M9.R.1 rule: "It is a must to use data type 1 for dummy metal to reduce DRC, OPC processing time (~50%) and errors."
114. Mx	2.11	Mx	Adds note: "Bond pad sizing up 2 $\mu\text{m}$ area don't need to check Mx.A.2.1-5."
115. VIA8.R.4	2.12	VIA8 Rule	Changes wording of VIA8.R.4 rule to "At least 2 VIA8(VIA7) with space $\leq 1.7 \mu\text{m}$ are required to connect $M_8(M_7)$ to $M_9(M_8)$ when one of these 2 metals have both length and width $> 1.8 \mu\text{m}$ ."
116. VIA8.S.2	2.12	VIA8 Rule	Changes wording of VIA8.S.2 rule to "Minimum space between VIA8 (VIA7) to 3-neighboring VIA8 (VIA7) or 4-neighboring VIA8 (VIA7)."
117. M9.S.2.2, 3, 4	2.13	Metal-9 Rule	Deletes wording of M9.S.2.2, 3, 4 rules: "The space inside metal hole is checked without parallel run length. Minimum metal hole length is 20 $\mu\text{m}$ ."

## From Version 0.1 to Version 0.2

Rule	Sec. No.	Section Title	Revision Description
118. M9.S.2.1	2.13	Metal-9 Rule	Changes the wording of M9.S.2.1 rule to "Minimum space between two parallel metal lines with one or both metal line whose width is larger than 1.50 (W1) $\mu\text{m}$ and the parallel length is larger than 1.5 (L1) $\mu\text{m}$ ."
119. M9.A.2	2.13	Metal-9 Rule	Modifies wording of M9.A.2 rule to "Minimum M9 enclosed area when M9 width is = 0.42 $\mu\text{m}$ ."
120. M9.A.2.1	2.13	Metal-9 Rule	Adds M9.A.2.1 rule: "Minimum M9 enclosed area when M9 width is > 0.42um." 0.8um <sup>2</sup> ."
121. M9.A.2.2	2.13	Metal-9 Rule	Adds M9.A.2.2 rule: "Minimum M9 enclosed area when M9 width is > 1.5 $\mu\text{m}$ ." 3.2 $\mu\text{m}^2$ ."
122. M9.A.2.3	2.13	Metal-9 Rule	Adds M9.A.2.3 rule: "Minimum M9 enclosed area when M9 width is > 3 $\mu\text{m}$ ." 7.2 $\mu\text{m}^2$ ."
123. M9.A.2.4	2.13	Metal-9 Rule	Adds M9.A.2.4 rule: "Minimum M9 enclosed area when M9 width is > 4.5 $\mu\text{m}$ ." 20.2 $\mu\text{m}^2$ ."
124. M9.A.2.5	2.13	Metal-9 Rule	Adds M9.A.2.5 rule: "Minimum M9 enclosed area when M9 width is > 7.5 $\mu\text{m}$ ." 51.8 $\mu\text{m}^2$ ."
125. M9.R.2	2.13	Metal-9 Rule	Deletes M9.R.2 rule.
126. M9.S.5	2.13	Metal-9 Rule	Modifies wording of M9.S.5 rule to "If 2 or more parallel metals are within the range of wide metal (Wn > 1.5um) spacing (Sn), the spacing between these metals should be >= Sn. Wn, Sn are defined by M9.S.2.1 – M9.S.2.4"
127. M9.R.1	2.13	Metal-9 Rule	Modifies wording of M9.R.1 rule to "Metal density range over any 100 $\mu\text{m}$ x 100 $\mu\text{m}$ area (checked by stepping in 50 $\mu\text{m}$ increments). M9 (topmost metal layer) bond pad area is excluded from density check. Dummy pattern is required for those with M9 density less than 20 %. TSMC's recommended dummy pattern is 2 $\mu\text{m}$ x 2 $\mu\text{m}$ , space 2 $\mu\text{m}$ either between 2 dummy metals or between dummy metal and interconnect metal. It is a must to use data type 1 for dummy metal to reduce DRC, OPC processing time (~50%) and errors."
128. M9.R.1.1	2.13	Metal-9 Rule	Modifies the wording of M9.R.n.1 rule: "Maximum M9 (M8) density over any 500 $\mu\text{m}$ x 500 $\mu\text{m}$ area (checked by stepping in 250um increments). Bond pad area is excluded from density check."
129. M9	2.13	Metal-9 Rule	Adds note: "Bond pad sizing up 2 $\mu\text{m}$ area don't need to check M9.A.2.1-5."
130.	2.16	SRAM Rule	Adds Section 2.16.
131.	2.18	Chip Corner Stress Relief Pattern	Adds Section 2.18.
132.	2.19	Seal-Ring Rule	Adds Section 2.19.
133.	2.20	Antenna rules	Modifies all antenna rules.
134.	2.21	Latch-up Prevention Guideline	Renames rule no.
135. LUP.4	2.21	Latch-up Prevention Guideline	Changes wording of LUP.4 rule to "The minimum space between OD of IO buffer (transistor connected to IO pad) and OD in internal circuit (core) where it follows latch-up rule 3." Changes rule to 50 $\mu\text{m}$ .
136. LUP.5	2.21	Latch-up Prevention Guideline	Changes wording of LUP.5 rule to "Any periphery circuit or core circuit, which are within the 50 $\mu\text{m}$ (C in Fig. 2), should follow the I/O buffer rule (latch-up rule 1 and rule 2). The suggested NMOS and PMOS placement in IO and periphery please refer Fig. 2."
137.	2.23	I/O ESD Protection Circuit Design and Layout Guideline	Renames rule no. Adds 1.8V I/O device rules.
138. ESD.11	2.23	I/O ESD Protection Circuit Design and Layout Guideline	Changes 3.3V poly gate length to 0.38 $\mu\text{m}$ and 2.5V to 0.28 $\mu\text{m}$ .

## A.1.2 From Version 0.2 to Version 0.3

From Version 0.2 to 0.3				
Rule	Sec. No.	Section Title	Revision Description	
1.	0.1 Part 1	Recommendation	<ul style="list-style-type: none"> <li>Deletes one item: "For better poly CD uniformity consideration: Certain forbidden pitch should be avoided. Please contact tsmc for details."</li> <li>Adds one item as # 8: "It is strongly recommended NOT to use thin oxide for de-coupling capacitor with the gate directly tied to power/ground. It is recommended to connect the gate to power/ground through a resistor or other tie-up/tie-down circuitry. Please also be aware of thin oxide gate leakage level."</li> <li>Modifies item #10 description and table for current density spec.</li> </ul>	
2.	0.5 Part V	Package Related Design Rule Documents	Adds "Package Related Design Rule documents" section.	
3.	1.1	Device Truth Table	<ul style="list-style-type: none"> <li>Changes layer OD3 to OD_18.</li> <li>Changes layer OD2 to OD_25 or OD_33.</li> </ul>	
4.	1.1	Device Truth Table	<ul style="list-style-type: none"> <li>Adds HSL device in device truth table.</li> </ul>	
5.	1.3	Reserved Mask Name	<ul style="list-style-type: none"> <li>Adds five optional mask sets, including HSL, PW3 (TGO_HS), NW3(TGO_HS), N3V(TGO_HS), and P3V(TGO_HS).</li> <li>Deletes one mask of NW3(TGO).</li> </ul>	
6.	1.7	Cad Layer Definition	Adds "CAD Layer Definition" section.	
7.	1.8	Key Process Sequence	<ul style="list-style-type: none"> <li>Adds five optional processes, including:           <ul style="list-style-type: none"> <li>HSL</li> <li>PW3 (TGO_HS)</li> <li>NW3(TGO_HS)</li> <li>N3V(TGO_HS)</li> <li>P3V(TGO_HS).</li> </ul> </li> <li>Deletes NW3(TGO) process.</li> </ul>	
8.	NWR.O.1	2.1.2.1	NW under STI	Modifies wording of NWR.O.1 rule <b>from</b> "Minimum overlap of RPO to NP inside NW" <b>to</b> "Minimum overlap of RPO to NP."
9.	NWR.O.2	2.1.2.1	NW under STI	<ul style="list-style-type: none"> <li>Modifies the definition of the NOR.O.2 rule: definition overlap to extension.</li> <li>Changes the Rule name NWR.E.6.</li> </ul>
10.		2.1.2.1	NW under STI	Adds recommendation: "It is strongly recommended to have NW Resistor $\geq$ 5 squares."
11.	DNW.C.1	2.13	DNW	Changes DNW.C.1 rule <b>to</b> 3.3 $\mu\text{m}$ <b>from</b> 3.5 $\mu\text{m}$ .
12.	OD	2.3.1	Thin Oxide Rule	Changes the OD width for 1.8V/2.5V <b>to</b> 0.4 $\mu\text{m}$ <b>from</b> 0.3 $\mu\text{m}$ .
13.	OD	2.3.1	Thin Oxide Rule	Adds note: "It is strongly suggested to limit the max. OD width to < 100 $\mu\text{m}$ for better CMP uniformity and CD control."
14.	OD.S.1.2	2.3.1	Thin Oxide Rule	Changes wording of OD.S.1.2 rule to "Minimum space between two ODs with a parallel length $\geq$ 0.3 $\mu\text{m}$ (L) and at least one of the corresponding OD regions has width $>$ 0.23 $\mu\text{m}$ (W): (a) if crossed by a common PO, or (b) if PO is crossing one of the ODs. Rule applies up to a distance of 0.16 $\mu\text{m}$ away from the Gate."
15.	OD.L.2	2.3.1	Thin Oxide Rule	Adds wording to OD.L.2 rule: "It is strongly suggested to limit the max interconnect OD length to < 10 $\mu\text{m}$ and as short as possible to ensure better resistance control."
16.	DOD	2.3.2	Dummy OD/PO Rule	Modifies Dummy OD rules and guidelines.
17.	DPO	2.3.2	Dummy OD/PO Rule	Modifies Dummy PO rules and guidelines.

From Version 0.2 to 0.3			
Rule	Sec. No.	Section Title	Revision Description
18.	OD2	2.3.3	Thick Oxide Rule <ul style="list-style-type: none"> <li>The OD_33 layer (CAD layer: 15) is used for 3.3V gate oxide area.</li> <li>The OD_25 layer (CAD layer: 41) is used for 2.5V gate oxide area.</li> <li>The OD_18 layer (CAD layer: 16) is used for 1.8V gate oxide area.</li> </ul>
19.	OD2	2.3.3	Thick Oxide Rule <p>Adds note: "OD2 refers to any thick oxide device, i.e. OD2=OD_18 or OD_25 or OD_33."</p>
20.	OD2.C.4	2.3.3	Thick Oxide Rule <p>Adds OD2.C.4 rule: "Minimum clearance between an OD_33 and an OD_18 is 0.62 µm. Align if space is less than this value."</p>
21.	OD2.R.1	2.3.3	Thick Oxide Rule <p>Adds OD2.R.1 rule: "OD_33 and OD_25 cannot be used on the same die. OD_18 and OD_25 cannot be used on the same die."</p>
22.	OD3	2.3.4	OD3 Rules <ul style="list-style-type: none"> <li>Deletes the "OD3 Rules" section.</li> <li>Deletes the reference to "OD3" in other sections.</li> </ul>
23.	HSL	2.3.4	HSL Rules <p>Adds "HSL Rules" section.</p>
24.	PO.S.6	2.4	Poly Rule <p>Adds PO.S.6 rule: "The min. space between Poly spacing covered by RPO &gt; 0.25 µm. (See PO.S.6.)"</p>
25.	PO.S.5	2.4	Poly Rule <p>Changes PO.S.5 rule to 0.19 µm from 0.22 µm.</p>
26.	PO.W.5	2.4	Poly Rule <p>Changes PO.W.5 rule to 0.19 µm from 0.16 µm.</p>
27.	PO.L.1	2.4	Poly Rule <p>Adds wording to PO.L.1 rule: "It is strongly suggested to limit the max interconnect PO length to &lt; 10 µm and as short as possible to ensure better resistance control."</p>
28.		2.4.2	OD/Poly Resistor Guideline <p>Changes RHDMY to RH.</p>
29.		2.4.2	OD/Poly Resistor Guideline <p>Deletes "It is strongly recommended that contacts to pickup OD/poly resistor should be a single column."</p>
30.	PP.C.6	2.6.1	P+ S/D I/I Rule <p>Changes wording of PP.C.6 rule from "Minimum clearance from a butted P+ OD to the related Poly gate if butting N+ extending 0 &lt; J &lt; 0.22 µm in PW. When J = 0, please refer to OD.C.6." to " Minimum clearance from a butted P+ OD to the related Poly gate if butting N+ OD extending 0 &lt; J &lt; 0.22 µm in PW. When J = 0, please refer to OD.C.6."</p>
31.	PP.E.2	2.6.1	P+ S/D I/I Rule <p>Adds wording to PP.E.2 rule: "It is strongly suggested to use 0.13 µm extension when P+OD space to NW is smaller than 0.22 µm."</p>
32.	PP.A.3	2.6.1	P+ S/D I/I Rule <p>Adds rule PP.A.3: Minimum area of P+ OD butted to a N+ OD is 0.04 µm<sup>2</sup>.</p>
33.	NP.C.6	2.6.2	N+ S/D I/I Rule <p>Changes wording of NP.C.6 rule from "Minimum clearance from a butted N+ OD to the related Poly gate if butting N+ extending 0 &lt; J &lt; 0.22 µm in PW. When J = 0, please refer to OD.C.6." to " Minimum clearance from a butted N+ OD to the related Poly gate if butting P+ OD extending 0 &lt; J &lt; 0.22 µm in NW. When J = 0, please refer to OD.C.6."</p>
34.	NP.E.2	2.6.2	N+ S/D I/I Rule <p>Adds wording to NP.E.2 rule: "It is strongly suggested to use 0.13 µm extension when N+OD space to NW is smaller than 0.22 µm."</p>
35.	NP.A.3	2.6.2	N+ S/D I/I Rule <p>Adds NP.A.3 rule: Minimum area of N+ OD butted to a P+ OD is 0.04 µm<sup>2</sup>.</p>
36.	LDN.03	2.63	Rules for LDD Mask Logical operation <p>Deletes LDN.03 rule: "Minimum overlap between NP and OD3."</p>
37.	LDP.03	2.63	Rules for LDD Mask Logical operation <p>Deletes LDP.03 rule: "Minimum overlap between PP and OD3."</p>
38.	CO	2.8	Contact Rule <p>Adds notes: <ul style="list-style-type: none"> <li>"It is strongly suggested to put multiple and symmetrical source/drain contacts to minimize source/drain series resistance."</li> <li>"It is strongly suggested to put PO contacts to gate as close as possible to minimize voltage drop due to long poly line."</li> </ul> </p>

## From Version 0.2 to 0.3

Rule	Sec. No.	Section Title	Revision Description
39.	CO.E.1.1	2.8	Contact Rule Adds wording to CO.E.1.1 rule: "It is strongly suggested to use $\geq 0.07 \mu\text{m}$ to have tighter Rc control."
40.	CO.E.1.2	2.8	Contact Rule Adds wording to CO.E.1.2 rule: "It is strongly suggested to use $\geq 0.07 \mu\text{m}$ to have tighter Rc control."
41.	CO.E.2.1	2.8	Contact Rule Adds wording to CO.E.2.1 rule: "It is strongly suggested to use $\geq 0.07 \mu\text{m}$ to have tighter Rc control."
42.	CO.E.2.2	2.8	Contact Rule Adds wording to CO.E.2 rule: "It is strongly suggested to use $\geq 0.07 \mu\text{m}$ to have tighter Rc control."
43.	M1.A.2.1	2.9	Metal-1 Rule Fixes typo in M1.A.2.1 rule: "0,18" $\rightarrow$ "0.18."
44.	M1.S.5	2.9	Metal-1 Rule Relaxes M1.S.5 rule to allow width < parallel run length. (DRC)
45.	Mx.S.5	2.11	Metal-2 to Metal-7 Rule Relaxes Mx.S.5 to allow width < parallel run length. (DRC)
46.	M.9.S.5	2.13	Metal-8, 9 Rule Relaxes M9.S.5 to allow width < parallel run length. (DRC)
47.	M1.E.2	2.9	Metal-1 Rule Modifies wording of M1.E.2 rule from "It is strongly recommended to use bigger metal end-of-line extension whenever possible for better yield and reliability." to "It is strongly recommended to use bigger metal end-of-line extension $\geq 0.07 \mu\text{m}$ whenever possible for better yield and reliability."
48.	M1.R.1	2.9	Metal-1 Rule Modifies wording of M1.R.1 rule from "Dummy pattern is required for those with M1 density less than 20 %. TSMC's recommended dummy pattern is $2 \mu\text{m} \times 2 \mu\text{m}$ , space $2 \mu\text{m}$ either between 2 dummy metals or between dummy metal and interconnect metal. It is a must to use data type 1 for dummy metal to reduce DRC, OPC processing time (~50%) and errors." to "Please see section 2.13.1 for detail dummy metal rules."
49.	VIAx.S.2	2.10	VIA-1 to VIA-6 Rule Modifies wording of VIAx.S.2 rule from "Minimum space between VIAx to 3-neighboring VIAx or 4-neighboring VIAx." to "Minimum space between VIAx to $\geq 3$ -neighboring VIAx."
50.	VIAx.E.2	2.10	VIA-1 to VIA-6 Rule Adds wording to VIAx.E.2 rule: "It is strongly recommended to use bigger metal end-of-line extension $\geq 0.08 \mu\text{m}$ whenever possible for better yield and reliability."
51.	VIAx.R.4.1	2.10	VIA-1 to VIA-6 Rule Changes wording of VIAx.R.4.1 rule from "More than 1 VIAx are required to connect to Mx and Mx+1 when Mx has H $> 20 \mu\text{m}$ , and W3 $> 1 \mu\text{m}$ , where connected length is defined as smaller than 5 $\mu\text{m}$ ( $L < 5 \mu\text{m}$ ) of the large metal area on a metal tab of Mx." to "At least 2 VIAx must be used for a connection that is $< 5 \mu\text{m}$ ( $L$ ) away from a metal plate of with height $> 20 \mu\text{m}$ (H) and width $> 3 \mu\text{m}$ (W3)"
52.	Mx.A.2.1	2.11	Metal-2 to Metal-7 Rule Fixes typo in Mx.A.2.1 rule: "0,21" $\rightarrow$ "0.21."
53.	Mx.E.2	2.11	Metal-2 to Metal-7 Rule Modifies wording of Mx.E.2 word from "It is strongly recommended to use bigger metal end-of-line extension whenever possible for better yield and reliability." to "It is strongly recommended to use bigger metal end-of-line extension $\geq 0.08 \mu\text{m}$ whenever possible for better yield and reliability."
54.	Mx.R.1	2.11	Metal-2 to Metal-7 Rule Modifies wording of Mx.R.1 rule from "Dummy pattern is required for those with Mx density less than 20 %. TSMC's recommended dummy pattern is $2 \mu\text{m} \times 2 \mu\text{m}$ , space $2 \mu\text{m}$ either between 2 dummy metals or between dummy metal and interconnect metal. It is a must to use data type 1 for dummy metal to reduce DRC, OPC processing time (~50%) and errors." to "Please see section 2.13.1 for detail dummy metal rules."
55.	VIA8.S.2	2.12	VIA-7, 8 Rule Modifies wording of VIA8.S.2 rule from "Minimum space between VIA8 (VIA7) to 3-neighboring VIA8 (VIA7) or 4-neighboring VIA8 (VIA7)." to "Minimum space between VIA8 (VIA7) to $\geq 3$ -neighboring VIA8 (VIA7)."

## From Version 0.2 to 0.3

Rule	Sec. No.	Section Title	Revision Description
56.	VIA8.E.2	2.12	VIA-7, 8 Rule  Modifies wording of VIA8.E.2 rule from "Minimum extension of M8 (M7) end-of-line beyond VIA8 (VIA7). For VIA8 (VIA7) located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and another side can follow VIA8.E.1" and changes rule <b>from</b> 0.09 µm <b>to</b> 0.08 µm.
57.	VIA8.E.3	2.12	VIA-7, 8 Rule  Deletes VIA8.E.3 rule and graph.
58.	VIA8.E.1	2.12	VIA-7, 8 Rule  Modifies wording of VIA8.E.1 rule: "Minimum extension of M8 (M7) beyond VIA8 (VIA7)."
59.	VIA8.E.0	2.12	VIA-7, 8 Rule  Modifies wording of VIA8.E.0 rule: "VIA8 (VIA7) extension is defined by VIA8.E.1 & VIA8.E.2."
60.	VIA8.R.4.1	2.12	VIA-7, 8 Rule  Changes wording of VIA8.R.4.1 rule <b>from</b> "More than 1 VIA8 (VIA7) are required to connect to M8(M7) and M9(M8) when M8(M7) has H>20 µm, and W3 >1 µm, where connected length is defined as smaller than 5 um (L< 5 um) of the large metal area on a metal tab of M8(M7)." <b>to</b> "At least 2 VIA8 (VIA7) must be used for a connection that is < 5 um (L) away from a metal plate of with height > 20 um (H) and width > 3 um ."
61.	VIA8.E.2	2.12	VIA-7, 8 Rule  Fixes typo in VIA8.E.2 rule: "VIAx.E.1" →"VIA8.E.1."
62.	M9.E.2	2.13	Metal-8, 9 Rule  Modifies the wording of the M9.E.2 rule to "Minimum extension of M9(M8) end-of-line beyond VIA8(VIA7). For VIA8 (VIA7) located at the 90 degree corner, at least one side of metal extension must be treated as end-of-line and another side can follow M9.E.1 (It is strongly recommended to use bigger metal end-of-line extension whenever possible for better yield and reliability.)" and rule change form 0.09 µm to 0.08 µm
63.	M9.R.1	2.13	Metal-8, 9 Rule  Changes the M9.R.1 rule: High density to 80%.
64.	M9.R.1	2.13	Metal-8, 9 Rule  Modifies the wording of the M9.R.1 rule <b>from</b> "Dummy pattern is required for those with M9 (M8) density less than 20 %. tsmc's recommended dummy pattern is 2 µm x 2 µm, space 2 µm either between 2 dummy metals or between dummy metal and interconnect metal. It is a must to use data type 1 for dummy metal to reduce DRC, OPC processing time (~50%) and errors." <b>to</b> "Please see section 2.13.1 for detail dummy metal rules."
65.	DMx	2.13.1	Dummy Metal Rule  Adds Dummy Metal Rule (DMx x=1,2,3,4,5,6,7,8,9)
66.		2.14	Current Density (EM) Specification  Updates "Current Density (EM) Specification" section.
67.		2.19	Seal Ring Rule  Updates "Seal-Ring Rule" section.
68.		2.20	Antenna Rules  Updates "Antenna Rules" section.
69.		2.23	I/O ESD Protection Circuit Design and Layout Guideline  Updates "I/O ESD Protection Circuit Design and Layout Guideline" section.

## A.1.3 From Version 0.3 to Version 1.0

From Version 0.3 to Version 1.0				
Rule	Sec. No.	Section Title	Revision Description	
1.	0.4	Special Layer summary	Adds SDI layer and LOGO layer in the summary table.	
2.	0.5	Dummy OD/POLY/Metal Filling Guideline	Adds "Dummy OD/POLY/Metal Filling Guideline" section.	
3.	1.2	Technology Family	Adds "Technology Family" section.	
4.	1.21	Power Supply	Adds "Power Supply" section.	
5.	1.3	Device Truth Table	Modifies "Device Truth Table" section: <ul style="list-style-type: none"> <li>• Separate to G, LP, HS process.</li> <li>• Deletes HSL device in device truth table.</li> <li>• Adds VTUHN and VTUHP devices in LP process.</li> </ul>	
6.	1.5	Reserved Mask Names	<ul style="list-style-type: none"> <li>• Deletes five Mask Names including:               <ul style="list-style-type: none"> <li>◦ HSL</li> <li>◦ PW3 (TGO_HS)</li> <li>◦ NW3 (TGO_HS)</li> <li>◦ N3V (TGO_HS)</li> <li>◦ P3V (TGO_HS)</li> </ul> </li> <li>• Adds two mask names: VTUH_N and VTUH_P.</li> </ul>	
7.	1.9	CAD Layer Definition	Deletes HSL CAD layer.	
8.	1.9	CAD Layer Definition	Adds VTUH_N AND VTUH_P CAD layers.	
9.	1.10	Key Process Sequence	<ul style="list-style-type: none"> <li>• Deletes five optional processes, including:               <ul style="list-style-type: none"> <li>◦ HSL</li> <li>◦ PW3 (TGO_HS)</li> <li>◦ NW3(TGO_HS)</li> <li>◦ N3V(TGO_HS)</li> <li>◦ P3V(TGO_HS)</li> </ul> </li> <li>• Adds two optional processes, including VTUH_N and VTUH_P device processes.</li> </ul>	
10.	NW.S.1		Modifies the operation voltage from 1.0V to 1.2V	
11.	NW.S.3		Modifies the operation voltage from 1.0V to 1.2V	
12.	NT_N.W.2		Modifies the operation voltage from 1.0V to 1.2V	
13.	OD.W.1.1		Modifies the operation voltage from 1.0V to 1.2V	
14.	OD.W.1.2		Modifies the operation voltage from 1.0V to 1.2V	
15.	OD.S.1		Modifies the operation voltage from 1.0V to 1.2V	
16.	OD.S.1.1		Modifies the operation voltage from 1.0V to 1.2V	
17.	PO.W.1		Modifies the operation voltage from 1.0V to 1.2V	
18.	PO.W.2		Modifies the operation voltage from 1.0V to 1.2V	
19.	PO.S.2		Modifies the operation voltage from 1.0V to 1.2V	
20.	VTH_N.W.2		Modifies the operation voltage from 1.0V to 1.2V	
21.	VTH_P.W.2		Modifies the operation voltage from 1.0V to 1.2V	
22.	VTL_N.W.2		Modifies the operation voltage from 1.0V to 1.2V	
23.	VTL_P.W.2		Modifies the operation voltage from 1.0V to 1.2V	
24.			Re-organizes rule numbers according to category.	
25.			Lists recommendations in a separate line.	
26.	2.1	Well Rule	Adds recommendation: “* It is strongly recommended to have all well must connect to contact/metal, floating well is not suggested.”	
27.	2.1.2	NW Resistor Layout Rule	<ul style="list-style-type: none"> <li>• Changes wording from “NW resistor layout guideline” to “NW resistor layout rule”.</li> <li>• Modifies Fig.2 NWDMY need to align NP.</li> </ul>	
28.	NW.R.O.1	2.1.2	NW Resistor Layout Rule	Mini overlap of RPO to NP: Adds recommendation to NW.R.O.1 rule: “It is recommendation to use fixed number 0.4 µm”

From Version 0.3 to Version 1.0			
Rule	Sec. No.	Section Title	Revision Description
29.	2.3.1	OD Rule	Deletes the fig and illustration of "It is suggested to avoid long narrow strip type of OD (L > 50 µm and W < 2 µm) which encloses STI sharp polygon inside. Minimum STI width inside is 0.36 µm."
30.	2.3.2.1	Dummy OD Rule.	<ul style="list-style-type: none"> <li>Modifies the description 1: DOC no."T-N90-LO-LE-003" to "T-N90-LO-LE-005 and T-N90-LO-LE-006."</li> <li>Modifies the description 2 wording <b>from</b> "When any one of these following layouts is revised, customer needs to evaluate the impact on OD masks carefully: a. Poly/ DPO(dummy Poly) b. NW/ ODBLK/ POBLK /NWDMY/ FW/ LMARK/ CB." <b>to</b> "When any one of these following layouts is revised, customer needs to evaluate the impact on OD masks carefully: a. Poly/ DPO(dummy Poly) b. NW/ ODBLK/ POBLK /NWDMY/ FW/ LMARK/LOGO."</li> <li>Modifies the description 3 wording <b>from</b> "Add ODBLK to include d. LOGO and e. Pad metal area for high frequency" <b>to</b> "If items a-d are specified in the gds2 file, TSMC on-line utility can handle these layers. Therefore, they can be excluded from ODBLK."</li> <li>Adds description 5: "Please refer to Chapter 0.5 'Dummy Pattern Guideline' for detail guideline of 'Blockage layer drawing,' 'Dummy pattern filling' and 'Mask revision.'"</li> </ul>
31.	DOD.C.1	2.3.2.1 Dummy OD Rule	Modifies the DOD.C.1 rule: "Minimum clearance of DOD to OD. DOD overlapped OD is not allowed." From 2 µm to 1.5 µm.
32.	DOD.C.2	2.3.2.1 Dummy OD Rule	Modifies the DOD.C.2 rule: "Minimum clearance of DOD to Poly. DOD overlapped Poly is not allowed." From 2 µm to 1.5 µm.
33.	DOD.C.9	2.3.2.1 Dummy OD Rule	Adds DOD.C.9 rule: "Minimum clearance of DOD to LOGO is 0 µm. DOD overlapped LOGO is not allowed."
34.	DOD.C.10	2.3.2.1 Dummy OD Rule	Adds DOD.C.10 rule: "Minimum clearance of DOD to INDDMY is 1.2 µm". DOD overlapped INDDMY is not allowed.
35.	DOD.R.1	2.3.2.1 Dummy OD Rule	<ul style="list-style-type: none"> <li>Modifies the DOD.R.1 rule <b>from</b> "Minimum (OD OR DOD) density over any 150 µm x 150 µm area (checked by stepping in 75 µm increments)." <b>to</b> "Minimum (OD OR DOD) density over any 150um x 150um area (checked by stepping in 75 µm increments)."</li> <li>Keeps density rule 20%.</li> </ul>
36.	DOD.R.1.1	2.3.2.1 Dummy OD Rule	<ul style="list-style-type: none"> <li>Modifies the DOD.R.1.1 rule <b>from</b> "Maximum (OD OR DOD) density over any 500 µm x 500 µm area (checked by stepping in 250um increments)." <b>to</b> "Maximum (OD OR DOD) density over any 150 µm x 150 µm area on core region (without OD2 and checked by stepping in 75 µm increments)."</li> <li>Keeps density rule 20%.</li> </ul>
37.	DOD.R.1.2	2.3.2.1 Dummy OD Rule	<ul style="list-style-type: none"> <li>Adds DOD.R.1.2 rule: "Maximum (OD OR DOD) density over any 150 µm x 150 µm area on I/O region (With OD2 and checked by stepping in 75 µm increments)."</li> <li>Rule is 90%</li> </ul>
38.	DOD.R.3	2.3.2.1 Dummy OD Rule	Modifies wording of DOD.R.3 rule <b>from</b> "For density check, DOD.R.1/DOD.R.1.1/DOD.R.1.2, these 3 regions can be excluded: 1. (CB sizing 2) for RF product 2. NWDMY/FW/LMARK as default3. Chip corner stress relief area if seal-ring & stress relief pattern added by TSMC." <b>to</b> "For density check, DOD.R.1/DOD.R.1.1/DOD.R.1.2, these 2 regions can be excluded: 1. ODBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default 2. Chip corner stress relief area if seal-ring and stress relief pattern added by TSMC."
39.	DOD.R.4	2.3.2.1 Dummy OD Rule	<ul style="list-style-type: none"> <li>Adds DOD.R.4 rule: "Minimum OD density in ODBLK over any 150 µm x 150 µm area. (checked by stepping in 75 µm increments).</li> <li>Rule is 20%.</li> </ul>
40.	DOD.R.4.1	2.3.2.1 Dummy OD Rule	<ul style="list-style-type: none"> <li>Adds DOD.R.4.1 rule: "Minimum OD density in ODBLK over any 150 µm x 150 µm area. (checked by stepping in 75 µm increments).</li> <li>Rule is 80%.</li> </ul>
41.	DOD.R.4.2	2.3.2.1 Dummy OD Rule	<ul style="list-style-type: none"> <li>Adds DOD.R.4.2 rule: "Maximum OD density in ODBLK over any 150 µm x 150 µm area on I/O region. (With OD2 and checked by stepping in 75 µm increments).</li> <li>Rule is 90%.</li> </ul>
42.	DOD.R.1	2.3.2.1 Dummy OD Rule	For density check, DOD.R.1, the following region can be excluded: ODBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default.
43.	DOD.R.2	2.3.2.1 Dummy OD Rule	For density check, DOD.R.2, the following region can be excluded: ODBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default.

From Version 0.3 to Version 1.0				
Rule	Sec. No.	Section Title	Revision Description	
44.	DOD.R.4	2.3.2.1	Dummy OD Rule	For density check, DOD.R.4, the following region can be excluded: ODBLK/NWDMY/FW/LMARK/LOGO/INDDMY as default.
45.	DPO	2.3.2.2	Dummy PO Rule	Modifies wording of description 2 (Dummy PO rule) <b>from</b> "When any one of these following layouts is revised, customer needs to evaluate the impact on PO masks carefully a.OD/ DOD (Dummy OD) b.POBLK/ FW/ LMARK/CB" <b>to</b> "When any one of these following layouts is revised, customer needs to evaluate the impact on PO masks carefully a. OD/ DOD (Dummy OD) b. POBLK/ FW/ LMARK/LOGO/INDDMY."
46.	DPO	2.3.2.2	Dummy PO Rule	Modifies description 1 wording (Dummy PO Rule) <b>from</b> DOC no: T-N90-LO-LE-003 <b>to</b> "T-N90-LO-LE-005 and T-N90-LO-LE-006."
47.	DPO	2.3.2.2	Dummy PO Rule	Adds description 3 wording (Dummy PO Rule): "Auto-fill DPO can be excluded from a block layer (POBLK, CAD layer no. 150;20) drawn by customer. We suggest POBLK to include, a. Fuse window/LMARK b. Inductor (INDDMY) c. LOGO d. Pad metal area for high frequency e. Sensitive circuits, as SRAM sensitive functional blocks and bit cell arrays, Analog/RF circuit (DAC/ADC, PLL).....etc. Adding DPO inside of sensitive circuits by customer manually is required to gain better process window and electrical performance. If items a~c are specified in the gds2 file, TSMC's on-line utility can handle these layers. Therefore, they can be excluded from POBLK."
48.	DPO	2.3.2.2	Dummy PO Rule	Adds description 5 wording (Dummy PO Rule): "Please refer to Chapter 0.5 'Dummy Pattern Guideline' for detail guideline of 'Blockage layer drawing', 'Dummy pattern filling' and 'Mask revision.'"
49.	DPO.C.1	2.3.2.2	Dummy PO Rule	Modifies DPO.C.1 rule: "Minimum clearance of DPO to OD. DPO overlapped OD is not allowed." <b>From</b> 2 $\mu\text{m}$ <b>to</b> 1.5 $\mu\text{m}$ .
50.	DPO.C.2	2.3.2.2	Dummy PO Rule	Modifies DPO.C.2 rule: "Minimum clearance of DPO to Poly. DPO overlapped Poly is not allowed." <b>From</b> 2 $\mu\text{m}$ <b>to</b> 1.5 $\mu\text{m}$ .
51.	DPO.C.11	2.3.2.2	Dummy PO Rule	Adds DPO.C.11 rule: "Minimum clearance of DPO to LOGO is 0 $\mu\text{m}$ . DPO overlapped LOGO is not allowed."
52.	DPO.C.12	2.3.2.2	Dummy PO Rule	Adds DPO.C.12 rule: "Minimum clearance of DPO to INDDMY is 1.5 $\mu\text{m}$ . DPO overlapped INDDMY is not allowed."
53.		2.3.4	High speed Low Leakage device (HSL) Rule	Deletes "High speed Low Leakage device (HSL) Rule section."
54.		2.4	Poly Rule	Adds a recommendation: "It is recommended to limit the max gate (Poly under OD) area to 400 $\mu\text{m}^2$ ".
55.		2.4.1	Phase shift Rules for High Performance Option	Deletes "Phase shift Rules for High Performance Option" section.
56.		2.5.5	Ultra High Vt NMOS Implant Rule	Adds "Ultra High Vt NMOS Implant Rule" section.
57.		2.5.6	Ultra High Vt PMOS Implant Rule	Adds "Ultra High Vt PMOS Implant Rule" section.
58.	RPO.C.4	2.7	RPO Rule	Adds recommendation to RPO.C.4 rule: "It is recommended the minimum clearance of RPO to related OD is 0.3 $\mu\text{m}$ when RPO width >10 $\mu\text{m}$ ."
59.	RPO.C.5	2.7	RPO Rule	Adds recommendation to RPO.C.5 rule: "It is recommended the minimum extension of RPO to poly resistor on field oxide is 0.3 $\mu\text{m}$ when RPO width > 10 $\mu\text{m}$ ."
60.		2.9	Metal -1 Rule.	Adds recommendation to Line-end/Extension illustration figure: "For product yield concern, fig. a is preferred."
61.	Viax.R.4	2.10	Via-1 to Via-6 Rule	Changes wording of Viax.R.4 rule <b>from</b> "At least 2 vias with space $\leq 0.29(\text{S1})$ , or at least 4 vias with space $\leq 0.57 \mu\text{m}(\text{S1}')$ are required to connect M <sub>x</sub> and M <sub>x+1</sub> when one of these 2 metals have width (W <sub>1</sub> ) > 0.42 $\mu\text{m}$ ." <b>to</b> "At least 2 vias with space $\leq 0.29(\text{S1})$ , or at least 4 vias with space $\leq 0.57 \mu\text{m}(\text{S1}')$ are required to connect M <sub>x</sub> and M <sub>x+1</sub> when one of these 2 metals have width and length (W <sub>1</sub> ) > 0.42 $\mu\text{m}$ ."
62.	Viax.R.5	2.10	Via-1 to Via-6 Rule	Changes wording of VIAx.R.5 rule <b>from</b> "At least 4 vias with space $\leq 0.29(\text{S2})$ , or at least 9 vias with space $\leq 0.77 \mu\text{m}(\text{S2}')$ are required to connect M <sub>x</sub> and M <sub>x+1</sub> when one of these 2 metals have width (W <sub>2</sub> ) > 0.98 $\mu\text{m}$ ." <b>to</b> "At least 4 vias with space $\leq 0.29(\text{S2})$ , or at least 9 vias with space $\leq 0.77 \mu\text{m}(\text{S2}')$ are required to connect M <sub>x</sub> and M <sub>x+1</sub> when one of these 2 metals have width and length (W <sub>2</sub> ) > 0.98 $\mu\text{m}$ ."

From Version 0.3 to Version 1.0			
Rule	Sec. No.	Section Title	Revision Description
63.	2.11	Metal-2 to Metal-7 Rule	Adds recommendation to Line-end/ Extension illustration figure: "For product yield concern, fig. a is preferred."
64.	VIA8.R.4	2.12 Via-7,8 Rule	Changes wording of VIA8.R.4 rule <b>from</b> "At least 2 VIA8 (VIA7) with space $\leq 1.7 \mu\text{m}$ are required to connect M8 (M7) and M9 (M8) when one of these 2 metals have width $> 1.8 \mu\text{m}$ ." <b>to</b> "At least 2 VIA8 (VIA7) with space $\leq 1.7 \mu\text{m}$ are required to connect M8 (M7) and M9 (M8) when one of these 2 metals have width and length $> 1.8 \mu\text{m}$ ."
65.	2.13	Metal-8, 9 Rule	Adds recommendation to Line-end/ Extension illustration figure: "For product yield concern, fig. a is preferred."
66.	2.13.1	Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Modifies the description 1 wording <b>from</b> "In order to improve metal CMP process window, every product must be filled by DMx as default." <b>to</b> "In order to improve metal CMP process window, filling dummy metal is required."
67.	2.13.1	Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Modifies the description 2 wording <b>from</b> "DOC no.:T-N90-LO-LE-003" <b>to</b> "T-N90-LO-LE-003 for CALIBRE and T-N90-LO-LE-004 for HERCULES."
68.	2.13.1	Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Adds description 6: "Please refer to Chapter 0.5 'Dummy Pattern Guideline' for detailed guideline of 'Blockage layer drawing', 'Dummy pattern filling' and 'Mask revision.'"
69.	DMx.1.1	2.13.1 Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	<ul style="list-style-type: none"> <li>• Adds DMx.1.1 rule: "Minimum clearance of DMx to LOGO edge, DMx overlapped LOGO edge is not allowed."</li> <li>• Rule is 0 <math>\mu\text{m}</math>.</li> </ul>
70.	DMx.C.6	2.13.1 Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Modifies wording of CMxC.6 rule <b>from</b> "DMx is must. DMx must be an individual CAD layer (data type 1 as default, such as 31;1 for DM1) to save mask making cycle time." <b>to</b> "DMx must be an individual CAD layer (data type 1 as default, such as 31;1 for DM1) to save mask making cycle time."
71.	DMx.C.7	2.13.1 Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Adds DMx.C.7 rule: "Minimum clearance from DMx to INDDMY edge is 18 $\mu\text{m}$ . DMx overlapped INDDMY is not allowed."
72.	DMx.C.8	2.13.1 Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Adds DMx.C.8 rule: "Minimum clearance from DMx to CBM edge is 1.5 $\mu\text{m}$ . DMx overlapped CBM is not allowed."
73.	DMX.R.1	2.13.1 Dummy Metal Rule (DMx, x=1,2,3,4,5,6,7,8,9)	Changes wording of DMX.R.1 rule <b>from</b> "Metal (Mx OR DMx) density range over any 100 $\mu\text{m} \times 100 \mu\text{m}$ area (checked by stepping in 50 $\mu\text{m}$ increments). The local density check would exclude the below regions: a. DMxEXCL/FW/LMARK b. Chip corner stress relief area if seal-ring and stress relief pattern added by TSMC." <b>to</b> "Metal (Mx OR DMx) density range over any 100 $\mu\text{m} \times 100 \mu\text{m}$ area (checked by stepping in 50 $\mu\text{m}$ increments). The local density check would exclude the below regions: a. DMxEXCL/FW/LMARK/LOGO/INDDMY. b. Chip corner stress relief area if seal-ring and stress relief pattern added by TSMC c. CBM of MIM capacitor would be excluded from the density check on below one metal layer. For example, if MIM capacitor placed between M9 and M8, then M8 density check would exclude CBM region."
74.	2.14	Product Labels and Logo Rule	Adds "Product Labels and Logo Rule" section.
75.	2.15	Current Density (EM) Specification	Adds Metal I peak rule and Poly resistor current density rule.
76.	2.16	Metal Fuse Rule	Changes description to "Please refer to Document no.: T-000-LO-DR-004."
77.	2.17	SRAM Rule	Merges Section 2.22 "Dummy layouts for Embedded SRAM" into "SRAM Rule" section.
78.	2.20	Seal-Ring Rule	Changes the schematic diagram for dual passivation process.
79.	A.R.7	2.21 Antenna Rules	Modifies A.R.7 rule typo <b>from</b> "on OD2" <b>to</b> "for cumulative layers"
80.	ESD.24	2.23 I/O ESD Protection Circuit Design and Layout Guideline	Modifies wording of ESD.24 rule <b>from</b> "Except 1.0V/1.8V $V_{dd}/V_{ss}$ power protection, RPO of 2.5V and 3.3 V $V_{dd}/V_{ss}$ (Ncs in Fig.4 and Fig.8), the RPO should fully cover drain/source and the poly gate on top of channel." <b>to</b> "Except 1.0V/1.8V $V_{dd}/V_{ss}$ power protection, RPO of 2.5V and 3.3 V $V_{dd}/V_{ss}$ (Ncs in Fig.4 and Fig.8), the RPO should cover drain side and the poly gate on top of channel."
81.		2.23 I/O ESD Protection Circuit Design and Layout Guideline	Modifies Fig. 7.

## A.1.4 From Version 1.0 to Version 1.1

<b>From Version 1.0 to Version 1.1</b> (The rule code, section no, section title, and revision description are based on Version 1.0.)			
Rule	Sec. No.	Section Title	Revision Description
1.	0.0	General Rule	Deletes "General Rule" section.
2.	1	Introduction	Restructures "Introduction" section.
3.	1	Technology Overview	Restructures "Technology Overview" section.
4.	1	Layout Information	Restructures "Layout Information" section.
5.	2	Layout Rule Description	Restructures "Layout Rule Description" section.
6.	DNW.E.2	Deep N-Well Rule	Deletes DNW.E.2 rule.
7.	DNW.S.3	Deep N-Well Rule	Inserts DNW.S.3 rule from OD.C.8. This is an insert of the rule, not an add.
8.	OD.W.3	OD Rule	Combines OD.W.1.1 rule and OD.W.1.2 rule to OD.W.3 rule: "Width of MOS (> 1.2V to ≤ 3.3V)."
9.	OD.C.1.1	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
10.	OD.C.2	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
11.	OD.C.2.1	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
12.	OD.C.2.2	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
13.	OD.C.3	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
14.	OD.C.4	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
15.	OD.C.4.1	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
16.	OD.C.4.2	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
17.	OD.C.5	OD Rule	Moves rules (OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, and OD.C.5) to NW section. These rules are not cancelled.
18.	OD.C.6	OD Rule	Deletes OD.C.6 rule. (This rule is not canceled. It is defined in the rules in sections 2.19 PP and 2.20 NP.)
19.	OD.C.7	OD Rule	Deletes OD.C.7 rule. (This rule is not canceled. It is defined in the rules in sections 2.19 PP and 2.20 NP.)
20.	OD.C.8	OD Rule	Moves OD.C.8 rule to DNW.S.3. This rule is not cancelled.
21.	NW.S.5	NW Rule	Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
22.	NW.S.6	NW Rule	Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.

**From Version 1.0 to Version 1.1**  
**(The rule code, section no, section title, and revision description are based on Version 1.0.)**

Rule	Sec. No.	Section Title	Revision Description
23.	NW.S.7	2.1	NW Rule  Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
24.	NW.S.7®	2.1	NW Rule  Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
25.	NW.EN.1	2.1	NW Rule  Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
26.	NW.EN.2	2.1	NW Rule  Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
27.	NW.EN.3	2.1	NW Rule  Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
28.	NW.EN.3®	2.1	NW Rule  Inserts rules (NW.S.5, NW.S.6, NW.S.7, NW.S.7®, NW.EN.1, NW.EN.2, NW.EN.3, NW.EN.3®) and originals from OD.C.1. OD.C.1.1, OD.C.2, OD.C.2.1, OD.C.2.2, OD.C.3, OD.C.4, OD.C.4.1, OD.C.4.2, OD.C.5. The rules are inserted, not added.
29.	NWROD.W.1	2.1	NWROD Rule  Inserts NWROD.W.1 and original from NW.W.2. This is an insert, not an add.
30.	NWR.C.2	2.1	NWROD Rule  Deletes the rule number description NWR.C.2. Only note the rule value in illustration fig.
31.	NWRSTI.W.1	2.1	NWRSTI Rule  Inserts NWRSTI.W.1 and original from NW.W.2. This is an insert, not an add.
32.	NT_N.I.5	2.2	NT_N Rule  Deletes the NT_N.I.5 rule: "A bent Po region is not allowed to put in an NT_N region."
33.	PO.W.3	2.4	POLY Rule  Combines the PO.W.3 rule ("Minimum width of a PO for interconnect) with the PO.W.1 rule ("(Min) Width."
34.	PO.W.1	2.4	POLY Rule  Combines the PO.W.3 rule ("Minimum width of a PO for interconnect) with the PO.W.1 rule ("(Min) Width."
35.	PO.C.2®	2.4	POLY Rule  Modifies the rule <b>from</b> 0.28 µm <b>to</b> 0.23 µm.
36.	VTH_N.I.2	2.5	VTH_N Rule  Deletes the VTH_N.I.2 rule: "A P+ region is not allowed to put in a VTH_N region except PW pickup."
37.	VTH_N.S.3	2.5	VTH_N Rule  Modifies the VTH_N.S.3 rule: "Space to gate in S/D direction." <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
38.	VTH_N.S.2	2.5	VTH_N Rule  Combines VTH_N.S.2 and VTH_N.S.3 into VTH_N.S.2 rule "Space to gate" 0.22 µm
39.	VTH_N.S.3	2.5	VTH_N Rule  Combines the VTH_N.S.2 and VTH_N.S.3 rules into the VTH_N.S.2 rule "Space to gate" 0.22 µm.
40.	VTH_N.EX.1	2.5	VTH_N Rule  Modifies the VTH_N.EX.1 rule: "Extension on gate in S/D direction." <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
41.	VTH_N.EN.1	2.5	VTH_N Rule  Combines the VTH_N.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTH_N.EX.2 rule ("Extension on gate in S/D direction" 0.22 µm) to the VTH_N.EN.1 rule ("Enclosure on gate." 0.22 µm.)
42.	VTH_N.EX.1	2.5	VTH_N Rule  Combines the VTH_N.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTH_N.EX.2 rule ("Extension on gate in S/D direction" 0.22 µm) to the VTH_N.EN.1 rule ("Enclosure on gate." 0.22 µm.)

**From Version 1.0 to Version 1.1**  
**(The rule code, section no, section title, and revision description are based on Version 1.0.)**

Rule	Sec. No.	Section Title	Revision Description
43.	VTH_N.EX.2	2.5	VTH_N Rule  Combines the VTH_N.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTH_N.EX.2 rule ("Extension on gate in S/D direction" 0.22 µm) to the VTH_N.EN.1 rule ("Enclosure on gate." 0.22 µm.)
44.	VTH_N.W.2	2.5	VTH_N Rule  The VTH_N.W.2 rule is incorporated in the PO.W.1 rule.
45.	VTH_P.I.2	2.5	VTH_P rule  Deletes the VTH_P.I.2 rule: "A N+ region is not allowed to put in a VTH_P region except NW pickup."
46.	VTH_P.S.3	2.5	VTH_P rule  Modifies the VTH_P.S.3 rule: "Space to gate in S/D direction" from 0.23 µm to 0.22 µm.
47.	VTH_P.S.3	2.5	VTH_P rule  Combines the VTH_P.S.2 and VTH_P.S.3 rules to the VTH_P.S.2 rule: "Space to gate" 0.22 µm
48.	VTH_P.S.2	2.5	VTH_P rule  Combines the VTH_P.S.2 and VTH_P.S.3 rules to the VTH_P.S.2 rule: "Space to gate" 0.22 µm
49.	VTH_P.EX.1	2.5	VTH_P rule  Modifies the VTH_P.EX.1 rule: "Extension on gate in S/D direction" <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
50.	VTH_P.EN.1	2.5	VTH_P rule  Combines the VTH_P.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTH_P.EX.2 rule ("Extension on gate in S/D direction" 0.22 µm) to the VTH_P.EN.1 rule ("Enclosure on gate." 0.22 µm.)
51.	VTH_P.EX.1	2.5	VTH_P Rule  Combines the VTH_P.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTH_P.EX.2 rule ("Extension on gate in S/D direction" 0.22 µm) to the VTH_P.EN.1rule ("Enclosure on gate." 0.22 µm.)
52.	VTH_P.EX.2	2.5	VTH_P Rule  Combines the VTH_P.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTH_P.EX.2 rule ("Extension on gate in S/D direction" 0.22 µm) to the VTH_P.EN.1rule ("Enclosure on gate." 0.22 µm.)
53.	VTH_P.W.2	2.5	VTH_P Rule  Integrates the VTH_P.W.2 into the PO.W.1 rule.
54.	VTL_N.I.2	2.5	VTL_N Rule  Deletes the VTL_N.I.2 rule: "A P+ region is not allowed to put in a VTL_N region except PW pickup."
55.	VTL_N.S.3	2.5	VTL_N Rule  Modifies the VTL_N.S.3 rule: "Space to gate in S/D direction." <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
56.	VTL_N.S.2	2.5	VTL_N Rule  Combines the VTL_N.S.2 rule and VTL_N.S.3 rule to VTL_N.S.2: "Space to gate." 0.22 µm.
57.	VTL_N.EX.1	2.5	VTL_N Rule  Modifies the VTL_N.EX.1 rule: "Extension on gate in S/D direction." <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
58.	VTL_N.EN.1	2.5	VTL_N Rule  Combines the VTL_N.EX.1 rule ("Extension on gate in S/D direction." 0.22 µm) and the VTL_N.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm.) to the VTL_N.EN.1 rule ("Enclosure on gate." 0.22 µm.).
59.	VTL_N.EX.1	2.5	VTL_N Rule  Combines the VTL_N.EX.1 rule ("Extension on gate in S/D direction." 0.22 µm) and the VTL_N.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm.) to the VTL_N.EN.1 rule ("Enclosure on gate." 0.22 µm.).
60.	VTL_N.EX.2	2.5	VTL_N Rule  Combines the VTL_N.EX.1 rule ("Extension on gate in S/D direction." 0.22 µm) and the VTL_N.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm.) to the VTL_N.EN.1 rule ("Enclosure on gate." 0.22 µm.).
61.	VTL_N.W.2	2.5	VTL_N Rule  Combines the VTL_N.W.2 rule to the PO.W.1 rule.
62.	VTL_P.I.2	2.5	VTL_P Rule  Deletes the VTL_P.I.2 rule: "A N+ region is not allowed to put in a VTL_P region except NW pickup."
63.	VTL_P.S.3	2.5	VTL_P Rule  Modifies the VTL_P.S.3 rule: "Space to gate in S/D direction." <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
64.	VTL_P.S.2	2.5	VTL_P Rule  Combines VTL_P.S.2 and VTL_P.S.3 to VTL_P.S.2 "Space to gate." 0.22 µm.
65.	VTL_P.EX.1	2.5	VTL_P Rule  Modifies the VTL_P.EX.1 rule: "Extension on gate in S/D direction." <b>from</b> 0.23 µm <b>to</b> 0.22 µm.
66.	VTL_P.EN.1	2.5	VTL_P Rule  Combines the VTL_P.EX.1 rule ("Extension on gate in S/D direction." 0.22 µm) and the VTL_P.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm) to the VTL_P.EN.1 rule ("Enclosure on gate." 0.22 µm).

**From Version 1.0 to Version 1.1**  
**(The rule code, section no, section title, and revision description are based on Version 1.0.)**

Rule	Sec. No.	Section Title	Revision Description
67.	VTL_P.EX.1	2.5	VTL_P Rule Combines the VTL_P.EX.1 rule ("Extension on gate in S/D direction." 0.22 µm) and the VTL_P.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm) to the VTL_P.EN.1 rule ("Enclosure on gate." 0.22 µm).
68.	VTL_P.EX.2	2.5	VTL_P Rule Combines the VTL_P.EX.1 rule ("Extension on gate in S/D direction." 0.22 µm) and the VTL_P.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm) to the VTL_P.EN.1 rule ("Enclosure on gate." 0.22 µm).
69.	VTL_P.W.2	2.5	VTL_P Rule Combines the VTL_P.W.2 rule to the PO.W.1 rule.
70.	VTUH_N.I.2	2.5	VTUH_N Rule Deletes the VTUH_N.I.2 rule: "A P+ region is not allowed to put in a VTUH_N region except PW pickup."
71.	VTUH_N.S.3	2.5	VTUH_N Rule Modifies the VTUH_N.S.3 rule: "Space to gate in S/D direction" from 0.23 µm to 0.22 µm.
72.	VTUH_N.S.2	2.5	VTUH_N Rule Combines the VTUH_N.S.2 and VTUH_N.S.3 rules to the VTUH_N.S.2 rule: "Space to gate." 0.22 µm.
73.	VTUH_N.EX.1	2.5	VTUH_N Rule Modifies the VTUH_N.EX.1 rule: "Extension on gate in S/D direction." from 0.23 µm to 0.22 µm.
74.	VTUH_N.EN.1	2.5	VTUH_N Rule Combines the VTUH_N.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTUH_N.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm) to the VTUH_N.EN.1 rule ("Enclosure on gate." 0.22 µm.).
75.	VTUH_N.EX.1	2.5	VTUH_N Rule Combines the VTUH_N.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTUH_N.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm) to the VTUH_N.EN.1 rule ("Enclosure on gate." 0.22 µm.).
76.	VTUH_N.EX.2	2.5	VTUH_N Rule Combines the VTUH_N.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTUH_N.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm) to the VTUH_N.EN.1 rule ("Enclosure on gate." 0.22 µm.).
77.	VTL_N.W.2	2.5	VTUH_N Rule Combines the VTL_N.W.2 rule to the PO.W.1 rule.
78.	VTUH_P.I.2	2.5	VTUH_P Rule Deletes the VTUH_P.I.2 rule: "A N+ region is not allowed to put in a VTUH_P region except NW pickup."
79.	VTUH_P.S.3	2.5	VTUH_P Rule Modifies the VTUH_P.S.3 rule: "Space to gate in S/D direction." from 0.23 µm to 0.22 µm.
80.	VTUH_P.S.3	2.5	VTUH_P Rule Combines the VTUH_P.S.2 and VTUH_P.S.3 rules to the VTUH_P.S.2 rule: "Space to gate." 0.22 µm.
81.	VTUH_P.S.2	2.5	VTUH_P Rule Combines the VTUH_P.S.2 and VTUH_P.S.3 rules to the VTUH_P.S.2 rule: "Space to gate." 0.22 µm.
82.	VTUH_P.EX.1	2.5	VTUH_P Rule Modifies the VTUH_P.EX.1 rule: "Extension on gate in S/D direction." from 0.23 µm to 0.22 µm.
83.	VTUH_P.EN.1	2.5	VTUH_P Rule Combines the VTUH_P.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTUH_P.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm.) to the VTUH_P.EN.1 rule ("Enclosure on gate." 0.22 µm.).
84.	VTUH_P.EX.1	2.5	VTUH_P Rule Combines the VTUH_P.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTUH_P.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm.) to the VTUH_P.EN.1 rule ("Enclosure on gate." 0.22 µm.).
85.	VTUH_P.EX.2	2.5	VTUH_P Rule Combines the VTUH_P.EX.1 rule ("Extension on gate in S/D direction" 0.22 µm) and the VTUH_P.EX.2 rule ("Extension on gate in S/D direction." 0.22 µm.) to the VTUH_P.EN.1 rule ("Enclosure on gate." 0.22 µm.).
86.	VTUH_P.W.2	2.5	VTUH_P Rule Combines the VTUH_P.W.2 rule to the PO.W.1 rule.
87.	PP.E.3	2.6	PP Rule Deletes the PP.E.3 rule: "Minimum extension of a PP along the edge of a butted diffusion P+OD/N+OD." 0 µm.
88.	NP.E.3	2.6	NP Rule Deletes the NP.E.3 rule: "Minimum extension of a NP along the edge of a butted diffusion P+OD/N+OD." 0 µm.
89.	RPO.Ex.1	2.7	RPO Rule Combines the RPO.C.5 rule and the RPO.C.4 rule to the RPO.Ex.1 rule.
90.	CO.S.2	2.8	CO Rule Adds 3-neighboring definition with CO (< 0.18 µm distance) in the description.

From Version 1.0 to Version 1.1 (The rule code, section no, section title, and revision description are based on Version 1.0.)			
Rule	Sec. No.	Section Title	Revision Description
91.	CO.C.1	2.8	CO Rule Modifies the CO.C.1 rule: "Minimum clearance from a CO on OD to a PO gate of 1.0V devices" <b>from 0.08 µm to 0.07 µm.</b>
92.	CO.E.3®	2.8	CO Rule Deletes the CO.E.3® and CO.E.4® recommended value 0.07 µm: "It is strongly recommended to put contacts at both source side and butted well pickup side."
93.	CO.E.4®	2.8	CO Rule Deletes the CO.E.3® and CO.E.4® recommended value 0.07 µm: "It is strongly recommended to put contacts at both source side and butted well pickup side."
94.	M1.S.2.3	2.9	M1 Rule Deletes the M1.S.2.3 rule: "Minimum space (0.9 µm) between two parallel metal lines with one or both metal line whose width is larger than 3.00 (W3) µm and the parallel length is larger than 3.00 (L3) µm."
95.	M1.S.2.5	2.9	M1 Rule Deletes the M1.S.2.5 rule: "Minimum space (2.5 µm) between two parallel metal lines with one or both metal line whose width is larger than 7.50 (W5) µm and the parallel length is larger than 7.50 (L5) µm."
96.	M1.A.2.1	2.9	M1 Rule Deletes the M1.A.2.1 rule: "Minimum M1 enclosed area (0.8 µm) when M1 width is > 0.18 µm."
97.	M1.A.2.2	2.9	M1 Rule Deletes the M1.A.2.2 rule: "Minimum M1 enclosed area (3.2 µm) when M1 width is > 1.5 µm."
98.	M1.A.2.3	2.9	M1 Rule Deletes the M1.A.2.3 rule: "Minimum M1 enclosed area (7.2 µm) when M1 width is > 3.8 µm."
99.	M1.A.2.4	2.9	M1 Rule Deletes the M1.A.2.4 rule: "Minimum M1 enclosed area (20.2 µm) when M1 width is > 4.5 µm."
100.	M1.A.2.5	2.9	M1 Rule Deletes the M1.A.2.5 rule: "Minimum M1 enclosed area (51.8 µm) when M1 width is > 7.5 µm."
101.	M1.R.1	2.9	M1 Rule Modifies the M1.R.1 rule: "Metal density range over any 100 µm x 100 µm area" the lower bound <b>from "≥ 20%" to "≥ 15%"</b>
102.	M1.R.1.1	2.9	M1 Rule Deletes the M1.R.1.1 rule: "Maximum M1 density (65%) over any 500 µm x 500 µm area. (checked by stepping in 250 µm increments)."
103.	M1.DN.2	2.9	M1 Rule Adds the M1.DN.2 rule: "Maximum metal density (90%) over any 20 µm x 20 µm area (checked by stepping in 10 µm increments)."
104.	M1.S.5	2.9	M1 Rule Deletes the M1.S.5 rule.
105.	VIAx.S.2	2.10	VIAx Rule Adds 3-neighboring definition with VIAx (< 0.19 µm distance) in the description.
106.	VIAx.R.4	2.10	VIAx Rule Adds the VIAx.R.4 rule: "At least 2 vias must be used to connect Mx and Mx+1 for a connection that is distance < 1 µm (D) away from a metal plate when Mx of with length > 0.7 µm (L) and width > 0.7 µm (W). (It is allowed to use 1 VIAx for a connection that is > 1 µm (D) away from a Mx metal plate with length > 0.7 µm (L) and width > 0.7 µm (W).)"
107.	VIAx.R.5	2.10	VIAx Rule Adds the VIAx.R.5 rule: "At least 2 vias must be used to connect Mx and Mx+1 for a connection that is distance < 2 µm (D) away from a metal plate when Mx of with length > 2 µm (L) and width > 2 µm (W). (It is allowed to use 1 VIAx for a connection that is > 2 µm (D) away from a Mx metal plate with length > 2 µm (L) and width > 2 µm (W).)"
108.	VIAx.R.6	2.10	VIAx Rule Modifies the VIAx.R.6 rule: "At least 2 vias must be used for a connection that is < 5 µm (L) away from a metal plate of with length > 10 µm (L) and width > 3 µm (W3). (It is allowed to use 1 VIAx for a connection that is > 5 µm (D) away from a metal plate (either Mx or Mx+1) with length > 10 µm (L) and width > 3 µm (W).)"
109.		2.10	Recommendation For Redundant Via Adds "Recommendation For Redundant Via" section.

**From Version 1.0 to Version 1.1**  
**(The rule code, section no, section title, and revision description are based on Version 1.0.)**

Rule	Sec. No.	Section Title	Revision Description
110.	Mx.S.2.3	2.11	METALx Rule  Deletes the Mx.S.2.3 rule: "Minimum space (0.9 µm) between two parallel metal lines with one or both metal line whose width is larger than 3.00 (W3) µm and the parallel length is larger than 3.00 (L3) µm."
111.	Mx.S.2.5	2.11	METALx Rule  Deletes the Mx.S.2.5 rule: "Minimum space (1.5 µm) between two parallel metal lines with one or both metal line whose width is larger than 7.50 (W5) µm and the parallel length is larger than 7.50 (L5) µm."
112.	Mx.A.2.1	2.11	METALx Rule  Deletes the Mx.A.2.1 rule: "Minimum Mx enclosed area (0.8 um2) when Mx width is > 0.21µm."
113.	Mx.A.2.2	2.11	METALx Rule  Deletes the Mx.A.2.2 rule: "Minimum Mx enclosed area (3.2 um2) when Mx width is > 1.5 µm."
114.	Mx.A.2.3	2.11	METALx Rule  Deletes the Mx.A.2.3 rule: "Minimum Mx enclosed area (7.2 um2) when Mx width is > 3 µm."
115.	Mx.A.2.4	2.11	METALx Rule  Deletes the Mx.A.2.4 rule: "Minimum Mx enclosed area (20.2 um2) when Mx width is > 4.5 µm."
116.	Mx.A.2.5	2.11	METALx Rule  Deletes the Mx.A.2.5 rule: "Minimum Mx enclosed area (51.8 um2) when Mx width is > 7.5 µm."
117.	Mx.R.1	2.11	METALx Rule  Modifies the Mx.R.1 rule: "Metal density range over any 100 µm x 100 µm area" the lower bound <b>from "≥ 20%" to "≥ 15%"</b>
118.	Mx.R.1.1	2.11	METALx Rule  Deletes the Mx.R.1.1 rule: "Maximum Mx density (65%) over any 500 µm x 500 µm area. (checked by stepping in 250 µm increments)."
119.	Mx.DN.2	2.11	METALx Rule  Adds the Mx.DN.2 rule: "Maximum metal density (90%) over any 20 µm x 20 µm area (checked by stepping in 10 µm increments)."
120.	Mx.S.5	2.11	METALx Rule  Deletes the Mx.S.5 rule.
121.	VIAn.S.2	2.12	Large Via (VIAn) Rule  Adds 3-neighboring definition with VIAn (< 0.56 µm distance) in the description.
122.	VIAn.R.3	2.12	Large Via (VIAn) Rule  Modifies the Vian.R.3 rule: "At least 2 VIAn must be used for a connection that is distance < 5 µm (D) away from a metal plate of with length > 10 µm (L) and width > 3 µm (W). (It is allowed to use 1 VIAn for a connection that is > 5 µm (D) away from a metal plate (either Mn or Mn-1) with length > 10 µm (L) and width > 3 µm (W).)"
123.	M9.E.2®	2.13	Thick Metal (Mn) Rule  Deletes the M9.E.2® rule: "It is strongly recommended to use bigger metal end-of-line extension whenever possible for better yield and reliability."
124.	M9.S.2.2	2.13	Thick Metal (Mn) Rule  Deletes the M9.S.2.2 rule: "Minimum space (0.9 µm)between two parallel metal lines with one or both metal line whose width is larger than 3.00 (W2) µm and the parallel length is larger than 3.00 (L2)"
125.	M9.S.2.4	2.13	Thick Metal (Mn) Rule  Deletes the M9.S.2.4 rule: "Minimum space (2.5 µm)between two parallel metal lines with one or both metal line whose width is larger than 7.50 (W4) um and the parallel length is larger than 7.50 (L4) µm."
126.	M9.A.2.1	2.13	Thick Metal (Mn) Rule  Deletes the M9.A.2.1 rule: "Minimum M9 (M8) enclosed area (0.8 µm) when M9 (M8) width is > 0.42 µm."
127.	M9.A.2.2	2.13	Thick Metal (Mn) Rule  Deletes the M9.A.2.2 rule: "Minimum M9 (M8) enclosed area (3.2 µm) when M9 (M8) width is > 1.5 µm."
128.	M9.A.2.3	2.13	Thick Metal (Mn) Rule  Deletes the M9.A.2.3 rule: "Minimum M9 (M8) enclosed area (7.2 µm) when M9 (M8) width is > 3 µm."
129.	M9.A.2.4	2.13	Thick Metal (Mn) Rule  Deletes the M9.A.2.4 rule: "Minimum M9 (M8) enclosed area (20.2 µm)when M9 (M8) width is > 4.5 µm."
130.	M9.A.2.5	2.13	Thick Metal (Mn) Rule  Deletes the M9.A.2.5 rule: "Minimum M9 (M8) enclosed area (51.8 µm) when M9 (M8) width is > 7.5 µm."
131.	M9.R.1.1	2.13	Thick Metal (Mn) Rule  Deletes the M9.R.1.1 rule: "Maximum M9 (M8) density 65% over any 500 µm x 500 µm area. (checked by stepping in 250 µm increments). Bond pad area is excluded from density check."

<b>From Version 1.0 to Version 1.1</b> <b>(The rule code, section no, section title, and revision description are based on Version 1.0.)</b>			
<b>Rule</b>	<b>Sec. No.</b>	<b>Section Title</b>	<b>Revision Description</b>
132.	Mn.DN.2	2.13	Thick Metal (Mn) Rule  Adds the Mn.DN.2 rule: "Maximum metal density (90%) over any 20 µm x 20 µm area (checked by stepping in 10 µm increments)."
133.	M9.S.5	2.13	Thick Metal (Mn) Rule  Deletes the M9.S.5 rule.
134.	DMx.W.2	2.13	Dummy Metal Rule  Modifies the DMx.W.2 rule: "Maximum width and length of DMx pattern" <b>from 6 µm to 3 µm</b> .
135.	DMx.DN.1	2.13	Dummy Metal Rule  Modifies the DMx.DN.1 rule: "{Mx OR DMx} density range over any 100 µm x 100 µm area (checked by stepping in 50 µm increments)." for Mn/M9T ≥ 15% (from 20% to 15%).
136.	DMx.R.2	2.13	Dummy Metal Rule  Modifies the DMx.DN.2 rule: "Metal density range inside DMxEXCL over any 100 µm x 100 µm area (checked by stepping in 50um increments)." <b>for Mn/M9T is ≥ 15%</b> (from 20% to 15%).
137.	DMx.S.1	2.13	Dummy Metal Rule  Modifies the DMx.S.1 rule: "Space to Mx (Overlap is not allowed)." <b>from 1.5 µm to 0.6 µm</b> .
138.	LOG.R.1	2.14	LOGO Rule  Combines the LOG.R.1~R.9 rules and the LOG.R.11 rule to the LOG.R.1 rule.
139.			Adds "Design for manufacturing (DFM)" section.
140.			Adds "Layout Guidelines for Yield Enhancement" section.
141.		Recommended rule (R-Rule) Summary	Adds "Recommended rule (R-Rule) Summary" section.
142.		Layout guideline for Analog Circuit	Adds "Layout guideline for Analog Circuit" section.
143.		2.15 Current Density (EM) Specification	<ul style="list-style-type: none"> <li>Modifies table of Jmax vs temp de-rating factor.</li> <li>Modifies CO EM Jmax <b>from 0.101 mA/CO to 0.294 mA/CO</b>.</li> <li>Adds Poly Jmax guideline.</li> </ul>
144.		2.15 Current density (EM) specification	Modifies VIAx EM Jmax <b>from 0.093 mA/via to 0.189 mA/via</b> .
145.		2.22 Latch- up prevention guideline	Modifies "Latch- up prevention guideline" section.
146.	LUP.4	2.22 Latch- up prevention guideline	Modifies the rule of I/O buffer space to circuit <b>from 50 µm to 20 µm</b> (LUP.5 in Version 1.1)
147.		2.23 Layout Guide line for latch up and ESD I/O	Modifies "Layout Guideline for latch up and ESD I/O" section.
148.		2.23 I/O ESD protection circuit design and layout guideline	Modifies "I/O ESD protection circuit design and layout guideline" section.
149.	ESD.8	2.23 I/O ESD protection circuit design and layout guideline	Modifies wording of ESD.8 rule to <ul style="list-style-type: none"> <li>A. Except ESD device, the space between 2 device ODs needs to be larger than or equal to 2.4 µm if the following conditions are both met: <ul style="list-style-type: none"> <li>A-1: N+OD to N+OD in PWell, or P+OD to P+OD in Nwell</li> <li>A-2: 2 ODs connected to different pads.</li> </ul> </li> <li>B. Guideline A can be waived if these 2 ODs are separated completely by a different type of OD (pick-up)."</li> </ul>
150.		2.23 I/O ESD protection circuit design and layout guideline	Modifies the numbering of tables and the rule sequence. Please refer to the rule code mapping table of ESD.
151.		2.23 I/O ESD protection circuit design and layout guideline	Merges ESD.29 rule "ESD3 is required for 5V tolerance" in Version 1.0 to ESD.30 in Version 1.1.
152.		2.23 I/O ESD protection circuit design and layout guideline	Merges ESD.25 and ESD.32 rules in Version 1.0 to ESD.30 in Version 1.1.
153.		2.23 I/O ESD protection circuit design and layout guideline	Adds a new rule description for ESD.41 in Version 1.1.

<b>From Version 1.0 to Version 1.1</b> <b>(The rule code, section no, section title, and revision description are based on Version 1.0.)</b>			
<b>Rule</b>	<b>Sec. No.</b>	<b>Section Title</b>	<b>Revision Description</b>
154.	2.23	I/O ESD protection circuit design and layout guideline	Modifies wording of ESD.24 and the graph of Figure 7.2.9 with RPO fully cover. Modifies Figure 7.2.10 without RPO covered.
155.	ESD.21	I/O ESD protection circuit design and layout guideline	Modifies the rule “The minimum width of RPO on the drain side (X) and RPO edge to OD edge (Y) for 3.3V, 2.5V, and 1.0V PMOS used as an I/O device” <b>from</b> 1.95 $\mu\text{m}$ <b>to</b> 1.5 $\mu\text{m}$ (ESD.28 in Version 1.1)
156.		Appendix	Adds “Appendix” section.
157.		Rule Number Mapping table	Adds “ Rule Number Mapping table” section.
158.	0.6	Revision History	Adds “Revision History” section.

## A.1.5 From Version 1.1 to Version 1.2

<b>From Version 1.1 to Version 1.2</b> (The rule code, section no, section title, and revision description are based on Version 1.1.)			
Rule	Sec. No.	Section Title	Revision Description
1.	1.2	Reference Documentation	Merges wire bond and flip chip related rules. Modifies Figure 1.3.1.
2.	3	General Layout Information	Deletes high speed and adds high performance device truth table. Revises related wordings.
3.	3.8	General Layout Recommendation	Deletes this section. Parts of this section are moved to section 6.1.2.
4. G1	3.6	Design Geometry Restriction	Adds more words regarding layer 186;4.
5.	4.3	Definition of Layout Geometrical Terminology	Adds the graph definitions of Cut, Parallel Run Length, Size up, Size down, and Butted.
6. DNW.S.3	4.5	Layout Rules and Guidelines	Modifies the rule from 0.32 to 1.82 and modifies the rule description.
7. DNW.R.5®	4.5	Layout Rules and Guidelines	Modifies as guideline DNW.R.5g.
8. OD.S.2	4.5	Layout Rules and Guidelines	Modifies the rule description.
9. OD.S.3	4.5	Layout Rules and Guidelines	Modifies the arrow from OD to gate of the figure.
10. OD.S.5	4.5	Layout Rules and Guidelines	Adds one graph for this rule.
11. OD.W.1®	4.5	Layout Rules and Guidelines	Deletes OD.W.1®
12. OD.DN.2 & OD.DN.3	4.5	Layout Rules and Guidelines	Adds notes to explain the so called "outside OD2".
13. OD.L.2®	4.5	Layout Rules and Guidelines	Modifies as guideline OD.L.2g.
14. NW.S.7®	4.5	Layout Rules and Guidelines	Deletes.
15. NW.EN.3®	4.5	Layout Rules and Guidelines	Deletes.
16. NW.R.1®	4.5	Layout Rules and Guidelines	Modifies as guideline NW.R.1g.
17. NT_N.S.2	4.5	Layout Rules and Guidelines	Modifies the rule description.
18.	4.5	Layout Rules and Guidelines	Delete the figures of PO.S.6®, PO.S.2®, and PO.EX.2®.
19. PO.L.1®	4.5	Layout Rules and Guidelines	Modifies as guideline PO.L.1g.
20. VT*_.R.1	4.5	Layout Rules and Guidelines	Modifies PW as N+ACTIVE and NW as P+ACTIVE in rule descriptions.
21. PP.EX.2®	4.5	Layout Rules and Guidelines	Deletes.
22. NP.EX.2®	4.5	Layout Rules and Guidelines	Deletes.
23. CO.S.3	4.5	Layout Rules and Guidelines	Adds the wording "[space can be $\geq 0.058 \mu\text{m}$ inside SRAM word line decoder covered by layer 186;4]"
24. CO.EN.2®	4.5	Layout Rules and Guidelines	Modifies the rule number CO.EN.2® as CO.EN.3®
25. CO.S.6®	4.5	Layout Rules and Guidelines	Modifies as guideline CO.S.6g.
26. CO.R.1®	4.5	Layout Rules and Guidelines	Modifies as guideline CO.R.1g.
27. CO.R.5®	4.5	Layout Rules and Guidelines	Modifies as guideline CO.R.5g.

**From Version 1.1 to Version 1.2**  
**(The rule code, section no, section title, and revision description are based on Version 1.1.)**

Rule	Sec. No.	Section Title	Revision Description
28.	CO.R.6®	4.5	Layout Rules and Guidelines Modifies as guideline CO.R.6g.
29.		4.5	Layout Rules and Guidelines Adds guidelines CO.R.7g, VIAx.R.10g, and VIAn.R.6g.
30.	VIAx.R.9®	4.5	Layout Rules and Guidelines Modifies as guideline VIAx.R.9g.
31.		4.5	Section 4.5.26 Modifies the figures and contents.
32.		4.5	Layout Rules and Guidelines Corrects typos in VIA1~6 of Figure a in section 4.5.34.
33.		4.5	Layout Rules and Guidelines Modifies the table notes of section 4.5.35.
34.	DOD.W.1	5.1	DOD Rules Modifies the rule from 2.0 to 0.5.
35.	DOD.S.1	5.1	DOD Rules Modifies the rule from 1.1 to 0.4.
36.	DOD.S.2	5.1	DOD Rules Modifies the rule from 1.5 to 0.6.
37.	DOD.S.3	5.1	DOD Rules Modifies the rule from 1.5 to 0.6.
38.	DOD.S.4	5.1	DOD Rules Modifies the rule as guideline DOD.S.4g.
39.	DOD.S.8	5.1	DOD Rules Modifies the rule from 1.2 to 0.6.
40.	DOD.EN.2	5.1	DOD Rules Modifies the rule from 2.5 to 0.6.
41.	DPO.W.1	5.2	DPO Rules Modifies the rule from 0.5 to 0.4.
42.	DPO.S.2	5.2	DPO Rules Modifies the rule from 1.5 to 0.2.
43.	DPO.S.3	5.2	DPO Rules Modifies the rule from 1.5 to 0.5.
44.	DPO.S.4	5.2	DPO Rules Modifies the rule as guideline DPO.S.4g.
45.	DPO.EN.1	5.2	DPO Rules Modifies the rule from 2.5 to 0.6.
46.	DPO.S.7	5.2	DPO Rules Deletes.
47.	DPO.A.1	5.2	DPO Rules Deletes.
48.		5.2	DPO Rules Adds the guideline DPO.R.4g.
49.	DMx.S.6	5.3	DM Rules Modifies the rule as guideline DMx.S.6g.
50.	DMx.W.1®	5.3	DM Rules Modifies the rule as guideline DMx.W.1g. Modifies the table of Recommended DMx size.
51.		6.1	Layout Guidelines for Yield Enhancement Modifies section 6.1.2.1. Adds section 6.1.2.2 and 6.1.2.3.
52.		6.2	R-rule Summary Re-formats the entire section. R rules are separated as three groups.
53.		6.4	Mechanical and Thermal Guidelines for FCBGA Adds the section.
54.		7.1	Layout Guidelines for Latch-up Prevention Modifies Figure 7.1.1
55.		7.2	Layout Guidelines for Latch-up Prevention Modifies Table 7.2.3.
56.		7.2	Layout Guidelines for Latch-up Prevention Corrects the typo of ESD.44 from $\geq$ to $\leq$ .
57.		7.2	Section 7.2.7 Modifies the referred document from T-013-MM-RP-018 to T-013-MM-RP-014.

## A.1.6 From Version 1.2 to Version 1.3

From Version 1.2 to Version 1.3			
Rule	Sec. No.	Section Title	Revision Description
1.	1.1	Overview	Delete mask bias reference document.
2.	1.2	Reference Documents	Add reference documents for Reference Flow, DRC deck, dummy pattern generation utility, DFM utility, SPICE, LVS, and SRAM.
3.	2.1.1	Front-End Features	<ul style="list-style-type: none"> <li>• Add the description: Native devices with dual gate oxide and triple gate oxide applications</li> <li>• Add the table: SRAM cells in different process</li> <li>• Add the description: MOS varactor provides 1.0V/1.2V/2.5V/3.3V NMOS-in-NW capacitor structure.</li> </ul>
4.	2.2	Devices	<ul style="list-style-type: none"> <li>• Delete UHVT in LP process and add LVT in LP process</li> <li>• Add table note for table 2.2.1 and add the table 2.2.2</li> </ul>
5.	2.3	Power Supply ....	Add the over-drive voltage
6.	3.1	Mask Names ....	<ul style="list-style-type: none"> <li>• Add the description for P1V/N1V and SEALRING.</li> <li>• Separate the Mask table to G/GT/LP, respectively. And add the column, reference layer in logical operation</li> <li>• Add the table 3.1.4: Mask Name/ ID/ Grade/ Type, OPC, and PSM for CLN90G/GT/LP</li> </ul>
7.	3.1.1	Derived Mask Layers	Delete
8.	3.3	Special Recognition CAD Layer Summary	<ul style="list-style-type: none"> <li>• Delete HOTWL</li> <li>• Add the description in the SEALRING: This layer is a must for tape out of VIAx, if either customers add sealring by themselves or metal fuse is used.</li> <li>• Modify the description in the 186;4: SRAM periphery DRC layer can only be used in the word decoder of TSMC SRAM (0.99um^2 and 1.15um^2). This layer is only to waive CO.S.3 and G.1. And the SRAM must be reviewed by TSMC's R&amp;D and PE even if customer uses TSMC cell.</li> <li>• Add PSPO layer</li> </ul>
9.	3.4	Device Truth Tables	Delete UHVT in LP process and add LVT in LP process
10.	3.5	Mask Requirement .....	Correct some typo and separate the Mask application to G/GT/LP, respectively.
11.	OPC.R.1®	OPC Recommendations	Add the recommendation rule
12.	OPC.R.2g <sup>U</sup>	OPC Recommendations	Add the guideline
13.	3.6.2	OPC Recommendations	<ul style="list-style-type: none"> <li>• Add Figure 3.6.2: Simulation contour for the layout with and without small jog/zigzag.</li> <li>• Add Figure 3.6.3 avoid small zigzag</li> </ul>
14.	4.1	Layout Rule Conventions	<ul style="list-style-type: none"> <li>• Add the description: A registered symbol "<sup>U</sup>" is marked after the rule number as the rule is not checked by DRC.</li> </ul>
15.	4.3	Definition of Layout Geometrical Terminology	<ul style="list-style-type: none"> <li>• Add the figure of Guard ring.</li> </ul>
16.	DNW.R.5g	DNW Rules	Delete
17.	OD.S.2	OD Rules	Change "OD space inside OD2 [ACTIVE extension on OD2 without gate is not allowed.]" to "Space of {OD AND OD2} *It is recommended to avoid using minimum OD space, 0.14um, at OD interact with OD2 layout style for low leakage concern."
18.	OD.DN.3	OD Rules	Modify the description: "OD.DN.3 must be followed before ODBLK defined. This rule is only applied while the area (checking window AND ODBLK) >=5625um^2."

From Version 1.2 to Version 1.3			
Rule	Sec. No.	Section Title	Revision Description
19.	OD.DN.2/ OD.DN.3	4.5.2	OD Rules  Add the description: These rules are applied while the area (checking window - the above excluded region) >=5625um^2.
20.	DOD.R.1	4.5.2	OD Rules  Also put DOD.R.1 in OD rules for reference
21.	NW.W.2	4.5.3	NW Rules  Delete
22.	PO.EX.2®	4.5.8	PO Rules  Add the description: (full and symmetrical contact placement are recommended at both source and drain side), especially for the device width > 2μm.
23.	PO.DN.2	4.5.8	PO Rules  Add the rule
24.	DPO.R.1	4.5.8	PO Rules  Also put DPO.R.1 in PO rules for reference
25.		4.5.11	LVT_N Rules [G/GT]  Add the description: G process (1.0V device) uses VTL_N mask to process LVT device. GT process (1.2V device) uses logic operation by shrinking PO gate dimension to process LVT device. It is not allowed in 1.8V, 2.5V, and 3.3V devices.
26.		4.5.12	LVT_P Rules [G/GT]  Add the description: G process (1.0V device) uses VTL_P mask to process LVT device. GT process (1.2V device) uses logic operation by shrinking PO gate dimension to process LVT device. It is not allowed in 1.8V, 2.5V, and 3.3V devices.
27.		4.5.13	LVT Rules [LP]  Add the section
28.		4.5.18	Layout Rules for LDD Mask Logical Operations  Add the description: In DRC deck, we use proper sizing to reduce DRC false error.
29.	VT.EX.1	4.5.18	Layout Rules for LDD Mask Logical Operations  Delete
30.	RPO.EX.3	4.5.19	RPO rules  Change the recommended RPO.EX.1® to rule RPO.EX.3
31.		4.5.20	OD and Poly Resistor Guidelines  ● Refine the guidelines and provide the rule code ● Modify the width/length from 2/10 to 0.4/0.8 for OD/PO resistor. ● Provide the table of the resistance performance and variation with sampled width/legnth
32.		4.5.21	MOS Varactor Rules  Add the section
33.	CO.W.2	4.5.22	CO Rules  Add the rule
34.	CO.R.6g <sup>U</sup>	4.5.22	CO Rules  Add the description: especially for the device width >2 μm
35.	M1.S.2	4.5.23	M1 Rules  Relax the codition of M1 width from 0.18 μm to 0.3 μm
36.	M1.EN.3®	4.5.23	M1 Rules  Add the recommended rule
37.	DM1.R.1	4.5.23	M1 Rules  Also put DM1.R.1 in M1 rules for reference
38.	VIAx.W.2	4.5.24	VIAx Rules  Add the rule
39.	VIAx.S.3®	4.5.24	VIAx Rules  Add the recommended rule
40.	VIAx.EN.1®	4.5.24	VIAx Rules  Add the recommended rule
41.	VIAx.R.8®	4.5.24	VIAx Rules  Change the rule VIAx.R.8 to the recommended VIAx.R.8®
42.	Mx.EN.1®	4.5.25	Mx Rules  Add the recommended rule
43.	DMx.R.1	4.5.25	Mx Rules  Also put DMx.R.1 in Mx rules for reference
44.	Mx.R.2g <sup>U</sup>	4.5.25	Mx Rules  Add the guideline
45.	VIAN.W.2	4.5.26	VIAN Rules  Add the rule
46.	DMn.R.1	4.5.27	Mn Rules  Also put DMn.R.1 in Mn rules for reference
47.	Mn.R.2g <sup>U</sup>	4.5.27	Mn Rules  Add the guideline
48.		4.5.28	Via Layout Recommendations  Modifies the figures and contents.
49.		4.5.29	Product Labels and Logo Rules  Add the description: To protect the product labels and process uniformity consideration, do not use circuits in the LOGO demarcated regions.

From Version 1.2 to Version 1.3				
Rule	Sec. No.	Section Title	Revision Description	
50.	4.5.30	SRAM Rules	<ul style="list-style-type: none"> <li>Refine the rule and provide the rule code</li> <li>Provide TSMC's SRAM summary in SRAM.R.4<sup>U</sup></li> <li>Add the rule SRAM.R.7<sup>U</sup></li> <li>Add the description in SRAM.R.10g<sup>U</sup>: The overall Poly CD uniformity improvement is 0.5nm. The vertical and horizontal poly CD may have 2nm difference in worse case as the poly orientation is different.</li> <li>Move DNW.R.1g to SRAM.R.11.g<sup>U</sup></li> </ul>	
51.	SR.R.1	4.5.35	Seal Ring Rules	Add the rule
52.	CO.W.2	4.5.35	Seal Ring Rules	Also put CO.W.2 in Seal Ring Rules
53.	VIAx.W.2	4.5.35	Seal Ring Rules	Also put VIAx.W.2 in Seal Ring Rules
54.	VIAN.W.2	4.5.35	Seal Ring Rules	Also put VIAN.W.2 in Seal Ring Rules
55.	5.1	DOD Rules	<ul style="list-style-type: none"> <li>Add the description: In order to meet the extremely tight requirement in terms of process control for STI etch, polish as well as channel length definition (inter-level dielectric (ILD) planarization)</li> <li>Add the description: It is important to perform the utility on the whole chip GDS. It is dangerous to perform the utility only on the local density violation blocks in terms of the process requirement.</li> <li>Add the description: It is recommended to use filler cells with OD/PO to fill a large empty area in the standard-cell-based block during the P&amp;R stage. Current TSMC DOD/DPO utility is difficult to insert DOD shapes into a standard-cell placed area. For the better PO and OD CD control requirement, it is suggested to layout both OD and PO into filler cell (treat OD/PO as dummy filling, need to follow OD/PO and related rules, and use the GDS layer of OD/PO).</li> </ul>	
56.	OD.DN.3	5.1	DOD Rules	Modify the description: "OD.DN.3 must be followed before ODBLK defined. This rule is only applied while the area (checking window AND ODBLK) >=5625um^2."
57.	OD.DN.2/ OD.DN.3	5.1	DOD Rules	Add the description: These rules are applied while the area (checking window - the above excluded region) >=5625um^2.
58.	5.2	DPO Rules	<ul style="list-style-type: none"> <li>Add the description: Good Poly uniformity is required the key to meet the PO CD as well as circuit performance requirement. You must fill the DPO globally and uniformly</li> <li>Add the description: It is recommended to use filler cells with OD/PO to fill a large empty area in the standard-cell-based block during the P&amp;R stage. Current TSMC DOD/DPO utility is difficult to insert DOD shapes into a standard-cell placed area. For the better PO and OD CD control requirement, it is suggested to layout both OD and PO into filler cell (treat OD/PO as dummy filling, need to follow OD/PO and related rules, and use the GDS layer of OD/PO).</li> </ul>	
59.	PO.DN.2	5.2	DPO Rules	Also put PO.DN.2 in DPO Rules
60.	5.3	DMx Rules	<ul style="list-style-type: none"> <li>Add the description: In order to have an accurate interconnect RC for timing and power analysis, it is important to extract RC after dummy metal insertion, and extract RC with density based metal thickness variation feature enabled.</li> </ul>	
61.	DMx.W.1	5.3	DMx Rules	<ul style="list-style-type: none"> <li>Dimension from 0.4 to 0.32 for M1and Mx (thin metal)</li> <li>Dimension from 0.8 to 0.6 for Mn and MD (thick metal)</li> </ul>
62.	DMx.A.1	5.3	DMx Rules	<ul style="list-style-type: none"> <li>Area from 0.36 to 0.32 for M1and Mx (thin metal)</li> <li>Dimension from 0.8 to 0.6 for Mn and MD (thick metal)</li> </ul>
63.	Mx.DN.3	5.3	DMx Rules	Modify the description: DMxEXCL defined. This rule is only applied while the area (checking window AND DMXEXCL) >=2500um^2.
64.	Mx.DN.2/ Mx.DN.3	5.3	DMx Rules	Modify the description: These rules are applied while the area (checking window - the above excluded region) >=2500um^2.

From Version 1.2 to Version 1.3			
Rule	Sec. No.	Section Title	Revision Description
65.	DMx.W.1g <sup>U</sup>	5.3	DMx Rules
			<ul style="list-style-type: none"> <li>● Modify the dimension from 0.4x1~0.4x10/0.8 to 0.32x1~0.32x6/0.52 for Width x Length/Space in M1 and Mx</li> <li>● Modify the dimension from 0.8x1~0.8x10/1.6 to 0.6x1~0.6x10/1.08 for Width x Length/Space in Mn and MD</li> <li>● Modify the dimension from 1 to 0.61 for DMx to Mx space in M1 and Mx</li> <li>● Modify the dimension from 1.6 to 1.17 for DMx to Mx space in Mn and MD</li> </ul>
66.		5.4.2	Recommended Flow for Dummy Pattern Filling
			Add the section
67.		6.1.1	Layout Tips for Minimizing Critical Areas
			<ul style="list-style-type: none"> <li>● In item 1: Space out the wiring           <ul style="list-style-type: none"> <li>■ Add the description: either using Wire Spreading at P&amp;R stage or manually layout modification at cell level,</li> <li>■ Add the description: It can reduce the possibility of pattern short.</li> </ul> </li> <li>● In item 2: Reduce the probability of wiring shorts.           <ul style="list-style-type: none"> <li>■ Add the description: For long and parallel metal or poly lines use a larger space.</li> </ul> </li> </ul>
68.		6.1.1.2	Transistors
			<ul style="list-style-type: none"> <li>● In item 4: Modify the description to: The overall CD uniformity improvement is 0.5nm. The vertical and horizontal poly CD may have 2nm difference in worse case as the poly orientation is different.</li> <li>● Add item 6/7/8</li> </ul>
69.		6.1.2.3	Resistors
70.		6.2	DFM Rules and Guidelines Summary
			Add the description: Compliance checker is provided for DFM action-required (6.2.1) and recommended (6.2.2) rules. It is bundled in the TSMC logic DRC release package under the directory "DFM".
71.		6.2.1	Action-required
			Add the description: LPE is provided for action-required (6.2.1) DFM rules to get better precision in device parameters and simulation result. It is bundled in TSMC LVS release package under the directory "DFM".
72.	PO.EX.2®	6.2.1	Action-required
			<ul style="list-style-type: none"> <li>● Add the description: LPE model can support the simulation accuracy while channel width <math>\leq 2\mu m</math>.</li> <li>● Add the description: Full and symmetrical contact placement are recommended at both source and drain side, especially for the device width <math>&gt; 2\mu m</math>.</li> </ul>
73.	PO.S.5®/ PO.S.6®	6.2.1	Action-required
			Modify the typo from " $>0.2$ " to " $\geq 0.2$ "
74.	OPC.R.1®/ VAR.S.2®/ VAR.A.1®/ M1.EN.3®/ VIAx.S.3®/ VIAx.EN.1®/ VIAx.R.8®/ Mx.EN.1®	6.2.2	Recommended
			Add these recommended rules
75.	OPC.R.2g <sup>U</sup> / Mx.R.2g <sup>U</sup> / Mn.R.2g <sup>U</sup>	6.2.3	Guidelines
			Add these guidelines
76.		6.3	Layout Guidelines for Analog Circuits
			Add the description: Compliance checker is provided for DFM recommended Dimension for Analog Design (6.3.1). It is bundled in the TSMC logic DRC release package under the directory "DFM".
77.		6.3.1	Recommended Dimensions for Analog Designs
			Add the description: Besides section 6.2.1: Action-required, section 6.2.2: Recommended, and section 6.2.3: Guidelines, it is recommended additionally to use the following dimensions for analog designs.

From Version 1.2 to Version 1.3				
Rule	Sec. No.	Section Title	Revision Description	
78.	NW.R.2m / PO.EX.1m / PO.S.6.m / PO.S.5m / PO.EX.2m / POR.W.1m / POR.L.1m / RPO.S.3m	6.3.1	Recommended Dimensions for Analog Designs	Add the rule dimension for them
79.		6.3.2	Device Placement	<ul style="list-style-type: none"> <li>● Add item 12: Well proximity</li> <li>● Add item 13: Recommended to have an additional VSS (PW) guardring around the analog circuit block.</li> </ul>
80.	LUP.3g	7.1	Layout Guidelines for Latch-Up	Add the description: For only NMOS in the DNW [without the PMOS in NW overlapping with the DNW], there is no latch-up risk. The space from any point inside the source/drain OD area to the nearest pickup OD depends on the maximum allowed back bias.
81.	LUP.7	7.1	Layout Guidelines for Latch-Up	Delete
82.		7.2	I/O ESD Protection Circuit Design and Layout Guidelines	Replace "1.0V" by "1.2V/1.0V" in the section
83.	ESD.45g	7.2	I/O ESD Protection Circuit Design and Layout Guidelines	Add the guideline
84.		8	Reliability Rules and Models	<ul style="list-style-type: none"> <li>● Add the chapter</li> <li>● Move EM rule from section 4.5 to section 8.3 <ul style="list-style-type: none"> <li>■ Add section 8.3.1.8.2: AC Operation, Maximum Root-Mean-Square Current for LK Dielectrics (other metallization options)</li> <li>■ Add M9 I<sub>peak_DC</sub> current in section 8.3.1.9: AC Operation, PeakCurrent</li> </ul> </li> </ul>
85.		9	Electrical Parameters Summary	Add the chapter

## A.1.7 From Version 1.3 to Version 1.4

From Version 1.3 to Version 1.4			
Rule	Sec. No.	Section Title	Revision Description
1.		Title	Add "(G/ GT/ LP)" in the title
2.	1.1	Overview	Add 1.8V IO for N90 GT process
3.	1.2	Reference Documents	Add reference documents for, CLN80 rule, Latch up, Qualification report, Brief process flow, 2XTM rule and T-N90-CL-SP-028 in SPICE.
4.	1.3	Package Related Design Rule Documents	Remove this section
5.	1.3	Guidelines for Half Node Technologies (CLN80 only)	Add the section
6.	2.1.1	Front-End Features	<ul style="list-style-type: none"> <li>● Add 1.2V/1.8V in dual gate oxide</li> <li>● Add additional 1.8V application in NMOS-in-NW capacitor structure.</li> </ul>
7.	2.1.2	Back-End Features	<ul style="list-style-type: none"> <li>● Add the description, Low K (&lt;3.0) inter-metal dielectric for thin metal</li> <li>● Move the description of wire bond or flip chip terminals from section 1.3</li> </ul>
8.	2.2	Devices	<ul style="list-style-type: none"> <li>● Delete UHVT in LP process</li> </ul>
9.	2.3	Power Supply	Add 1.8V IO for N90 GT process
10.	3.1	Mask Names	<ul style="list-style-type: none"> <li>● Add DMx_O in the column of Reference Layer in Logical Operation of Mx in G/GT/LP process.</li> <li>● Add 1.2V/1.8V in formation in GT process</li> <li>● Delete UHVT in LP process</li> </ul>
11.	3.2	Dummy Pattern Fill CAD Layers	Add the information of the DMx_O
12.	3.3	Special Recognition CAD Layer Summary	<ul style="list-style-type: none"> <li>● Add RRuleRequire</li> <li>● Add RRuleRecommend</li> <li>● Add RruleAnalog</li> <li>● Add FILLER</li> </ul>
13.	3.4	Device Truth Tables	<ul style="list-style-type: none"> <li>● Add 1.8V/2.5V MOS Varactor in the G table</li> <li>● Add 2.5V MOS Varactor and delete UHVT in LP table.</li> <li>● Add 1.8V MOS and 1.8V MOS Varactor in the GT table</li> </ul>
14.	3.5	Mask Requirement	Delete UHVT
15.	G.4	Design Geometry Rules	Add the rule
16.	OPC.R.3®	OPC Recommendations and Guidelines	Add the recommendation rule
17.	3.7	Design Hierarchy Guidelines	<ul style="list-style-type: none"> <li>● Add Figure 3.7.1 Avoid redundant or excessive overlaps of polygons</li> </ul>
18.	4.2	Derived Geometries Used in Physical Design Rules	<ul style="list-style-type: none"> <li>● Add the definition of the chip edge</li> <li>● Add the definition of the assembly isolation</li> </ul>
19.	OD.DN.2/3	OD Rules	Change the DRC check from area $\geq 5625\text{um}^2$ to width $\geq 37.5\text{um}$ .
20.	4.5.2	OD Rules	Add the table notes
21.	OD.S.6®	OD Rules	Add the rule
22.	NWROD.O.2	NWROD Rules	Delete VTUH_N/VTUH_P in the rule.
23.	NWRSTI.O.1	NWRSTI	Delete VTUH_P in the rule.
24.	NT_N.EN.1	NT_N Rules	Modify the rule from =0.26 to 0.26~0.285 and add the description, "if the layout will be shrunk to be N80, you need to plot =0.285."
25.		OD2 Rules	Add the description, "Triple gate oxide is only for 1.0V/1.8V/3.3V of N90G process."
26.	OD2.EN.1	OD2 Rules	Add the description, "in S/D direction"

From Version 1.3 to Version 1.4			
Rule	Sec. No.	Section Title	Revision Description
27.	OD2.EX.3	4.5.7	OD2 Rules
28.	PO.S.10®	4.5.8	PO Rules
29.	PO.EX.2®	4.5.8	PO Rules
30.	PO.DN.2	4.5.8	PO Rules
31.	DPO.R.1	4.5.8	PO Rules
32.		4.5.8	PO Rules
33.	VTH_N.S.3	4.5.9	VTH_N Rules
34.	VTH_N.R.1	4.5.9	VTH_N Rules
35.	VTH_P.S.3	4.5.10	VTH_P Rules
36.	VTH_P.R.1	4.5.10	VTH_P Rules
37.	VTL_N.S.3	4.5.11	VTL_N Rules
38.	VTL_N.R.1	4.5.11	VTL_N Rules
39.	VTL_P.S.3	4.5.12	VTL_P Rules
40.	VTL_P.R.1	4.5.12	VTL_P Rules
41.	PSPO.R.1	4.5.13	LVT Rules [LP]
42.			Delete VTUH_N in the rule
43.			Delete VTUH_P in the rule
44.	RES.8g	4.5.18	OD and Poly Resistor Guidelines
45.	RES.9g	4.5.18	OD and Poly Resistor Guidelines
46.		4.5.18	OD and Poly Resistor Guidelines
47.	VAR.EN.2	4.5.19	VAR Rules
48.	VAR.R.2	4.5.19	VAR Rules
49.	VAR.R.5	4.5.19	VAR Rules
50.	M1.S.6®	4.5.21	M1 Rules
51.	M1.DN.1	4.5.21	M1 Rules
52.	M1.DN.3	4.5.21	M1 Rules
53.	M1.DN.3®	4.5.21	M1 Rules
54.		4.5.21	M1 Rules
55.	Mx.W.4®	4.5.23	Mx Rules
56.	Mx.S.6®	4.5.23	Mx Rules
57.	Mx.DN.1	4.5.23	Mx Rules
58.	Mx.DN.3	4.5.23	Mx Rules
59.	Mx.DN.3®	4.5.23	Mx Rules
60.	Mx.R.3®	4.5.23	Mx Rules
61.		4.5.23	Mx Rules
62.	Mn.W.3®	4.5.25	Mn Rules
63.	Mn.DN.1	4.5.25	Mn Rules
64.	Mn.DN.3	4.5.25	Mn Rules
65.		4.5.25	Mn Rules
66.	SRAM.R.12	4.5.28	SRAM Rules
67.	SRAM.R.13	4.5.28	SRAM Rules
68.	SR.S.1	4.5.33	Seal Ring Rules
69.	A.R.5	4.5.34	Antenna Rules

From Version 1.3 to Version 1.4			
Rule	Sec. No.	Section Title	Revision Description
70.	OD.DN.2/3	5.1	DOD Rules
			<ul style="list-style-type: none"> <li>Change ((checking window NOT the item 3) from area <math>\geq 5625</math> to width <math>\geq 37.5</math> in OD.DN.2).</li> <li>Change ((checking window AND ODBLK) NOT the above excluded region) from area <math>\geq 5625</math> to width <math>\geq 37.5</math> in OD.DN.3).</li> </ul>
71.	PO.DN.2	5.4	DPO Rules
			<ul style="list-style-type: none"> <li>Add the description: The rule is applied while width of (checking window NOT item 2) <math>\geq 5\mu m</math></li> </ul>
72.		5.3	DMx Rules
			Add item 3 about DMx_O description
73.	Mx.DN.1/3	5.3	DMx Rules
			<ul style="list-style-type: none"> <li>Modify the checking window from 100x100 to 50x50 in 15%/20% check.</li> <li>Mx.DN.1 <math>\geq 15\% / 20\%</math> rule is applied while the width of (checking window NOT item 3) <math>\geq 12.5\mu m</math>.</li> <li>Mx.DN.1 <math>\leq 70\% / 80\%</math> rule is applied while the width of (checking window NOT item 3) <math>\geq 25\mu m</math>.</li> <li>Mx.DN.3 <math>\geq 15\% / 20\%</math> rule is only applied while the width of ((checking window AND DMxEXCL) NOT item 3) <math>\geq 12.5\mu m</math>.</li> <li>Mx.DN.3 <math>\leq 70\% / 80\%</math> rule is only applied while the width of ((checking window AND DMxEXCL) NOT item 3) <math>\geq 25\mu m</math>.</li> </ul>
74.	Mx.DN.3®	5.3	DMx Rules
			Add the recommendation
75.	Mx.DN.2	5.3	DMx Rules
			Add the description: The rule is applied while width of (checking window NOT Bond pad) $\geq 5\mu m$
76.	Mx.R.3®	5.3	DMx Rules
			Add the recommendation
77.		6.1.2.1	Transistors
			<ul style="list-style-type: none"> <li>Add item 4: Pay attention to the unexpected leakage current from floating gate.</li> </ul>
78.		6.1.2.1.1	Improvement of poly CD uniformity
			Add the section
79.		6.1.3	Electrical Wiring
			<ul style="list-style-type: none"> <li>Add item 2: During IP/marco design, it is important to put certain density margin to avoid the possibility of high density violations (Mx.DN.1, Mx.DN.2, Mx.DN.3) during placement. It may have unexpected violation during the IP/marco placement due to the environment, even if the IP/marco already pass the high density rule check. Therefore, you need to carefully design the dimension of the width/space for wide metal (eg, power/ground bus), under the proper high density limit.</li> <li>Add item 4: Maintain uniform metal density to minimize wire sheet resistance variation and maximize the associated photo process window. Target the local density to the middle range of the specification, avoiding the two extreme ends.</li> <li>Add item 5: Need dummy insertion in the library/IP/Macro blockage area</li> </ul>
80.		6.2	DFM Rules Recommendations and Guidelines Summary
			Add the description: The following 2 methods can specify the region to run DFM recommendations in DFM DRC deck. Please also refer to the "UserGuide" in the DFM deck.
81.	OPC.R.3®	6.2.3	Recommended
82.	OD.S.6®	6.2.3	Recommended
83.	PO.S.10®	6.2.3	Recommended
84.	M1.S.6®	6.2.3	Recommended
85.	M1.DN.3®	6.2.3	Recommended
86.	Mx.W.4®	6.2.3	Recommended
87.	Mx.S.6®	6.2.3	Recommended
88.	Mx.DN.3®	6.2.3	Recommended
89.	Mx.R.3®	6.2.3	Recommended
90.	Mn.W.3®	6.2.3	Recommended
91.	NWROD.R.1g	6.2.4	Guidelines
92.	CO.R.7g	6.2.4	Guidelines

From Version 1.3 to Version 1.4				
Rule	Sec. No.	Section Title	Revision Description	
93.	6.3	Layout Guidelines for Analog Circuits	Add the description: The following 2 methods can specify the region to run DFM recommendations in DFM DRC deck. Please also refer to the "UserGuide" in the DFM deck.	
94.	6.3.2.2	Device Placement	Add item 14: Avoid passivation opening, including both wire bond and flip chip, on the top of matching pairs Add item 15: Avoid placing the matching pairs at the chip corner and chip edge.	
95. \ ESD.35g	7.2.4	ESD Guidelines	Change the rule dimension from 20 to 10	
96. ESD.46g	7.2.4	ESD Guidelines	Add the guideline	
97. ESD.47g	7.2.4	ESD Guidelines	Add the guideline and figure 7.2.15	
98.	8.5	e-Reliability model system introduction	Add the section	
99.	9	Electrical Parameters Summary	Add the 1.2V/1.8V GT SPICE related information	
100.	Appendix B	Rule Mapping Table	Delete the section	

## A.1.8 From Version 1.4 to Version 1.5

From Version 1.4 to Version 1.5			
Rule	Sec. No.	Section Title	Revision Description
1.	1.2	Reference Documentation	Add MM/RF rule, 1T MIM rules, AP fuse rule, 2XTM qualification report, 2XTM SPICE,
2.	2.1.2	Back-End Features	Add 2XTM information
3.	2.4	Cross-section	Add 2XTM cross-section
4.	2.5	Metallization Options	Add 2XTM metallization and metal numbers of 3XTM or 2XTM for wirebond and flip chip
5.	3.1	Mask Informtaion, Key Process Sequence, and CAD Layers	<ul style="list-style-type: none"> <li>● Add option 2: Wire bond, filp chip with AP RDL (AP-MD) in table 3.1.1/3.1.2/3.1.3</li> <li>● 2XTM and AP-MD information in table 3.1.4</li> </ul>
6.	3.3	Special Recognition CAD Layer Summary	Add CDUDMY, BJTDY
7.	3.4.1	General Purpose (G): 1.0V Core Design	Change 0 to 1 in RPO layer for BJT device
8.	3.4.2	Low Power (LP): 1.2V Core Design	Change 0 to 1 in RPO layer for BJT device
9.	3.4.3	High Performance (GT): 1.2V Core Design	Change 0 to 1 in RPO layer for BJT device
10.	3.6.2	OPC Recommendations and Guidelines	Delete “Avoid redundant or excessive overlaps of polygons from two, or more than two, different cells or cell placements. For example, avoid forming a straight line from numerous cell placements, with each one contributing a little piece. Refer to the “Design Hierarchy Guidelines” section in this chapter. (Figure 3.7.1)”
11.	3.7	Design Hierarchy Guidelines	Delete “Avoid redundant or excessive overlaps of polygons from two, or more than two, different cells or cell placements. (See figure 3.7.1)For example, avoid forming a straight line from numerous cell placements, with each one contributing a little piece.”
12.	DNW.S.3	4.5.1	Modify “Space to N+ACTIVE” to “Space to “N+ACTIVE (DNW cut N+ACTIVE is not allowed)”
13.	DNW.S.4	4.5.1	Modify “RW space to RW with different potential” to “RW space to {RW OR PW} with different potential”
14.	DNW.S.5	4.5.1	Modify “RW space to {RW interact with OD2} with different potential” to “{RW OR PW} space to {RW interact with OD2} with different potential”
15.	DNW.S.6®	4.5.1	Add the recommendation
16.	DNW.EN.1®	4.5.1	Change DNW.EN.1 to DNW.EN.1®
17.	DNW.EN.2	4.5.1	Add the rule
18.	DNW.EN.3®	4.5.1	Add the recommendation
19.	DNW.R.1	4.5.1	Remove the rule
20.	DNW.R.2	4.5.1	Remove the rule
21.	DNW.R.4 <sup>U</sup>	4.5.1	Modify “{NW interact with DNW} must be at the same potential” to “(1) DNW and {NW interact with same DNW} must bias at same potential.(2) {NWs interact with same DNW} must bias at same potential”
22.	OD.W.1®	4.5.2	Add the description ”..... for CMP uniformity”
23.	OD.W.2®	4.5.2	Add the description ”..... for stable Isat (avoid corner rounding effect)”
24.	OD.S.1®	4.5.2	Add the description ”..... to reduce short possibility caused by partical”
25.	OD.L.2g <sup>U</sup>	4.5.2	Add the description ”..... to avoid high Rs of salicidation”
26.	NW.R.1g <sup>U</sup>	4.5.3	Add the description ”..... to avoid unstable device performance”

From Version 1.4 to Version 1.5			
Rule	Sec. No.	Section Title	Revision Description
27.	NWROD.R.1®	4.5.4	NWROD rules  Change NWROD.R.1g to NWROD.R.1® and modify "Recommend resistor length/width $\geq 5$ " to "Recommend resistor length (L) $\geq 20\mu m$ , and square number (length (L) / width (A)) $\geq 5$ for SPICE model accuracy. DRC can not check square number"
28.	NWRSTI.R.1®	4.5.5	NWRSTI rules  Add the recommendation
29.	NT_N.W.2.1	4.5.6	NT_N rules  Add the rule
30.	OD2.R.2 <sup>U</sup>	4.5.7	OD2 rules  Add the rule and change the related picture
31.	PO.S.1®	4.5.8	PO rules  Add the description "... to reduce short possibility caused by partical"
32.	PO.S.2®	4.5.8	PO rules  Add the description "... to avoid Isat degradation"
33.	PO.S.5®	4.5.8	PO rules  Add the description "... for stable Isat (avoid corner rounding effect)"
34.	PO.S.6®	4.5.8	PO rules  Add the description "... for stable Isat (avoid corner rounding effect)"
35.	PO.EX.2®	4.5.8	PO rules  Add the description "... to avoid Isat degradation"
36.	PO.EX.4®	4.5.8	PO rules  Add the recommendation
37.	PO.EX.5®	4.5.8	PO rules  Add the recommendation
38.	PO.L.1g <sup>U</sup>	4.5.8	PO rules  Add the description "... to avoid high Rs of salicidation"
39.	CO.EN.1®	4.5.20	CO rules  Add the description "... to avoid high Rc"
40.	CO.EN.3®	4.5.20	CO rules  Add the description "... to avoid high Rc"
41.	CO.S.6g <sup>U</sup>	4.5.20	CO rules  Add the description "... to avoid high Rs"
42.	CO.R.1g <sup>U</sup>	4.5.20	CO rules  Add the description "... f to avoid high Rs"
43.	CO.R.5g <sup>U</sup>	4.5.20	CO rules  Add the description "... to avoid high Rc"
44.	CO.R.6g <sup>U</sup>	4.5.20	CO rules  Add the description "... for SPICE accuracy"
45.	M1.EN.2®	4.5.21	M1 rules  Add the description "... to avoid high Rc"
46.	M1.EN.3®	4.5.21	M1 rules  Add the description "... to avoid high Rc"
47.	M1.DN.3®	4.5.21	M1 rules  Add the description "... for CMP uniformity"
48.	VIAx.EN.1®	4.5.22	VIAx rules  Add the description "... to avoid high Rc"
49.	VIAx.EN.2®	4.5.22	VIAx rules  Add the description "... to avoid high Rc"
50.	VIAx.R.2	4.5.22	VIAx rules  Add the wording "... , or at least nine VIAx with space $\leq 0.77 \mu m$ (S1")..."
51.	VIAx.R.3	4.5.22	VIAx rules  Modify M2 from 0.98 to 1.14
52.	VIAx.R.8®	4.5.22	VIAx rules  Add the description "... to avoid high Rc"
53.	VIAx.R.9g <sup>U</sup>	4.5.22	VIAx rules  Add the description "... to avoid high Rc ...."
54.	Mx.W.4®	4.5.23	Mx rules  Add the description "... for CMP uniformity"
55.	Mx.EN.1®	4.5.23	Mx rules  Add the description "... to avoid high Rc"
56.	Mx.EN.2®	4.5.23	Mx rules  Add the description "... to avoid high Rc"
57.	Mx.DN.3®	4.5.23	Mx rules  Add the description "... for CMP uniformity"
58.	Mx.DN.4®	4.5.23	Mx rules  Change Mx.R.3® to Mx.DN.3® and add the description "... for CMP uniformity ...."
59.	VIAN.R.5g <sup>U</sup>	4.5.24	VIAN rules (3XTM)  Add the description "... to avoid high Rc ...."
60.	Mn.W.3®	4.5.25	Mn rules (3XTM)  Add the description "... for CMP uniformity"
61.		4.5.26	VIAy rules (2XTM)  Add the section
62.		4.5.27	My rules (2XTM)  Add the section
63.		4.5.33.1	Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns  Add the section and modify/add the 6 seal ring GDS
64.	CSR.R.1	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules  Add L-mark seal ring
65.	CSR.S.2	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules  Change VIA1~6 to VIAx
66.	CSR.S.3	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules  Change VIAn to VIAn or VIAy

From Version 1.4 to Version 1.5			
Rule	Sec. No.	Section Title	Revision Description
67.	CSR.R.3 <sup>U</sup>	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Change (CO/VIAx, VIA <sub>n</sub> ) to (CO/VIAx, VIA <sub>n</sub> /VIAy)
68.	CSR.W.1	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
69.	CSR.L.1	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
70.	CSR.EN.4	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
71.	CSR.EN.5	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
72.	CSR.W.2	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
73.	CSR.W.3	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
74.	CSR.EN.6	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
75.	CSR.EN.7	4.5.33.2	Chip Corner Stress Relief Pattern (CSR) Layout Rules Add the rule for L-mark seal ring
76.		4.5.33.3.2	L-mark Seal-ring Corner Add the section
77.	VIAy.W.2	4.5.34	Seal Ring Layout Rules Add the rule
78.		4.5.34	Seal Ring Layout Rules ● Add 2XTM information in the Figure a. ● Add 371/383/306/309 information in the Figure b.
79.		4.5.34	CDU (Critical Dimension Uniformity) Rules Add the section
80.		Chapter 5	Layout Rules, Recommendations, and Guidelines for Analog Circuits Add the chapter 5
81.		Chapter 6	Dummy Pattern Rule and Filling Guideline Move the chapter from 5 to 6
82.	DOD.S.7.0	6.1	DOD rules Add the rule
83.	DOD.S.7.1	6.1	DOD rules Add the rule
84.	DOD.DN.2/3	6.1	DOD rules Modify them to the following wording with 20%/80%/90% rule: ● (CB sizing 2) for high speed/RF products for 20% rule. ● NWDMY/FW/LMARK/LOGO/INDDMY for 20% rule ● Chip corner stress relief and seal ring, and assembly isolation for 20%/80%/90% rule
85.	DOD.R.3	6.1	DOD rules Delete "A 45 degree shape is not allowed."
86.	DPO.S.6.0	6.2	DPO rules Add the rule
87.	DPO.S.6.1	6.2	DPO rules Add the rule
88.	DPO.R.3	6.2	DPO rules Delete "A 45 degree shape is not allowed."
89.		6.3	DMx rules Add 2XTM information

From Version 1.4 to Version 1.5				
Rule	Sec. No.	Section Title	Revision Description	
90.	DMx.S.5.0	6.3	DMx rules	Add the rule
91.	DMx.S.5.1	6.3	DMx rules	Add the rule
92.	DMx.DN.1/3	6.3	DMx rules	<p>Modify them to the following wording with 15%/20%/70%/80% rule:</p> <ul style="list-style-type: none"> <li>● FW/ LOGO/INDDMY for 15%/20% rules</li> <li>● LAMRK for 15%/20%/80% rules</li> <li>● Chip corner stress relief area and seal ring, and assembly isolation for 15% / 20%/70%/80% rule</li> <li>● CBM of MIM capacitor for 15%/20% rules</li> </ul>
93.	Mx.DN.2	6.3	DMx rules	Exclude LMARK check in the rule
94.	DMx.R.3	6.3	DMx rules	Delete "A 45 degree shape is not allowed."
95.	Chapter 7	Design For Manufacturing (DFM)	Move the chapter from 6 to 7	
96.		Guidelines for Low Power Designs	Add the section	
97.	7.2	DFM Recommendations and Guidelines Summary	Add 2 excluded cell option to run DFM check: ExclCellsForRRuleRequired and ExclCellsForRRuleRecommended	
98.		Action-Required Rules	Change title from Action-required to Action-Required Rules	
99.	7.2.1	Recommendations	Change title from Recommended to Recommendations	
100.		Recommendations	Move OD.W.2® from Action-Required Rules to Recommendations	
101.	DNW.S.6®	7.2.2	Recommendations	Add the recommendation
102.	DNW.EN.1®	7.2.2	Recommendations	Add the recommendation
103.	DNW.EN.3®	7.2.2	Recommendations	Add the recommendation
104.	NWRD.R.1®	7.2.2	Recommendations	Add the recommendation
105.	NWRD.R.1®	7.2.2	Recommendations	Add the recommendation
106.	PO.EX.4®	7.2.2	Recommendations	Add the recommendation
107.	PO.EX.5®	7.2.2	Recommendations	Add the recommendation
108.	VIAy.EN.1®	7.2.2	Recommendations	Add the recommendation
109.	VIAy.EN.2®	7.2.2	Recommendations	Add the recommendation
110.	My.W.4®	7.2.2	Recommendations	Add the recommendation
111.	My.S.6®	7.2.2	Recommendations	Add the recommendation
112.	My.EN.1®	7.2.2	Recommendations	Add the recommendation
113.	My.EN.2®	7.2.2	Recommendations	Add the recommendation
114.	VIAy.R.10g <sup>U</sup>	7.2.3	Guidelines	Add the guideline
115.	VIAy.R.9g <sup>U</sup>	7.2.3	Guidelines	Add the guideline
116.	My.R.2g <sup>U</sup>	7.2.3	Guidelines	Add the guideline

From Version 1.4 to Version 1.5				
Rule	Sec. No.	Section Title	Revision Description	
117.		Chapter 7	Layout Guidelines for Analog Circuit	Move the section to Chapter 5
118.		Chapter 8	Layout Guidelines for Latch-Up and I/O ESD	Move the chapter from 7 to 8
119.	ESD.43g <sup>U</sup>	8.2.4	ESD Guidelines	Modify minimum Via number from 300 to 100
120.		Chapter 9	Reliability Rules and Models	Move the chapter from 8 to 9
121.		9.3.1	Current Density (EM)	Add 2XTM and AP RDL information
122.		9.4	Product Early Failure Rate Screening Guidelines	Add the section
123.		Chapter 10	Electrical Parameters Summary	<ul style="list-style-type: none"> <li>● Move the chapter from 9 to 10</li> <li>● Add 2XTM information</li> <li>● Update the device parameters of LP native device</li> </ul>

## A.1.9 From Version 1.5 to Version 2.0

From Version 1.5 to Version 2.0				
Rule	Sec. No.	Section Title	Revision Description	
1.	1.2	Reference Documentation	Modify the table 1.2.1	
2.	1.3	Guidelines for Half Node Technologies (CLN80 only)	Add item 4/5	
3.	2.1.1	Front-End Features	Add SRAM information for UHD/DP in LP	
4.	2.5	Metalization Options	Add W/S and Mask layers in table 2.5.1/2.5.1	
5.	3.1	Mask Informtaion, Key Process Sequence, and CAD Layers	<ul style="list-style-type: none"> <li>Remove 1.0V/1.8V in 131 maks.in table 3.1.1</li> <li>Modify the 6 options of FBEOL in the tables 3.1.1/3.1.2/3.1.3</li> </ul>	
6.	3.3	Special Recognition CAD Layer Summary	Add Ncap_NTN, MOMDMY_1, MOMDMY_2, MOMDMY_3, MOMDMY_4, MOMDMY_5, MOMDMY_6, MOMDMY_7, MOMDMY_8, MOMDMY_9, MOMDMY_AP, RTMOMDMY, POFUSE, IO_buffer	
7.	G.5g <sup>U</sup>	Design Geometry Rules	Add the guideline	
8.	3.6.2	OPC Recommendations and Guidelines	<p>Add the description, “Use a well-organized, hierarchical layout structure.</p> <p>Avoid redundant or excessive overlaps of polygons from two, or more than two, different cells or cell placements. For example, avoid forming a straight line from numerous cell placements, with each one contributing a little piece. Refer to the “Design Hierarchy Guidelines” section in this chapter”</p>	
9.	4.3	Definition of Layout Geometrical Terminology	Add Channel width, Channel length, Vertex,	
10.	DNW.S.6®	DNW Rules	Remove the recommendation	
11.	DNW.EN.3®	DNW Rules	Remove the recommendation	
12.	DNW.R.5g <sup>U</sup>	DNW Rules	Add the guideline	
13.	OD.W.1	OD Rules	Remove the recommendation	
14.	OD.W.4	OD Rules	Add the description, “Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)”	
15.	OD.L.2	OD Rules	Change “[OD width is ≤ 0.15 μm]” to “[OD width is < 0.15 μm]”	
16.	NWROD.R.2g <sup>U</sup>	NWROD Rules	Add the guideline	
17.	NWROD.R.3g <sup>U</sup>	NWROD Rules	Add the guideline	
18.	NWRSTI.R.2g <sup>U</sup>	NWRSTI Rules	Add the guideline	
19.	NWRSTI.R.3g <sup>U</sup>	NWRSTI Rules	Add the guideline	
20.	NT_N.R.2	NT_N Rules	Change “P+OD” to “P+Gate”	
21.	OD2.W.2®	OD2 Rules	Add the recommendation	
22.	OD2.S.2	OD2 Rules	Modify the rule description from “Space to ACTIVE” to “Space to {ACTIVE OR GATE}”	
23.	OD2.S.5®	OD2 Rules	Add the recommendation	
24.	OD2.S.6®	OD2 Rules	Add the recommendation	
25.	OD2.S.7®	OD2 Rules	Add the recommendation	
26.	PO.W.4	PO Rules	Add the description, “Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)”	
27.	PO.S.10®	PO Rules	Remove the recommendation	
28.	PO.EX.4®	PO Rules	Remove the recommendation	
29.	PO.EX.5®	PO Rules	Remove the recommendation	

From Version 1.5 to Version 2.0			
Rule	Sec. No.	Section Title	Revision Description
30.	PO.L.1	4.5.8	PO Rules Modify the description, "Maximum PO length between two contacts, as well as between one contact and the PO line end when the PO width is < 0.13 $\mu\text{m}$ ." to Maximum PO length between two contacts without gate, as well as the length from any point inside PO gate to nearest CO, when the PO width is < 0.13 $\mu\text{m}$ ."
31.	PO.R.4	4.5.8	PO Rules Add the description, "and RTMOM region(RTMOMDMY, CAD layer:155;21)."
32.	PO.R.5 g <sup>U</sup>	4.5.8	PO Rules Add the guideline
33.	VTH_N.R.2	4.5.9	VTH_N Rules Add the rule
34.	VTH_N.R.3	4.5.9	VTH_N Rules Add the rule
35.	VTH_P.R.2	4.5.10	VTH_P Rules Add the rule
36.	VTH_P.R.3	4.5.10	VTH_P Rules Add the rule
37.	VTL_N.R.2	4.5.11	VTL_N Rules Add the rule
38.	VTL_N.R.3	4.5.11	VTL_N Rules Add the rule
39.	VTL_P.R.2	4.5.12	VTL_P Rules Add the rule
40.	VTL_P.R.3	4.5.12	VTL_P Rules Add the rule
41.	RES.10.g	4.5.18	OD and Poly Resistor Guidelines Add the guideline
42.	RES.11.g	4.5.18	OD and Poly Resistor Guidelines Add the guideline
43.	RES.12.g	4.5.18	OD and Poly Resistor Guidelines Add the guideline
44.	RES.13.g	4.5.18	OD and Poly Resistor Guidelines Add the guideline
45.	RES.14.g	4.5.18	OD and Poly Resistor Guidelines Add the guideline
46.	RES.15.g <sup>U</sup>	4.5.18	OD and Poly Resistor Guidelines Add the guideline
47.	RES.16.g <sup>U</sup>	4.5.18	OD and Poly Resistor Guidelines Add the guideline
48.	VAR.S.2®	4.5.19	VAR Rules Remove the recommendation
49.	CO.R.5g <sup>U</sup>	4.5.20	CO Rules Add the description, " 1. Recommended to use double CO or more on the resistor connection. 2. Double CO on Poly gate to reduce the probability of high Rc 3. Recommend putting multiple and symmetrical source/drain CO for SPICE simulation accuracy. 4. For large transistor, limit the number of source/drain CO: have the number of CO necessary for the current, and then spread them all over the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle)"
50.	CO.R.6g <sup>U</sup>	4.5.20	CO Rules Merge the guideline to CO.R.5g <sup>U</sup>
51.	M1.W.2	4.5.21	M1 Rules Add the description, "Please make sure the vertex of 45 degree pattern is on 5nm grid (refer to the guideline, G.5g <sup>U</sup> , in section 3.6)"
52.	M1.S.4	4.5.21	M1 Rules Add the description, 'Note: When M1 width > 9um is used, please take care of the M1.DN.2 rule by using larger space. For example, if two M1 with width 12um and space 1.5um, it will get 92.5% density violation on M1.DN.2; either enlarger the M1 space (like 2um) or reduce the M1 width (like 9um) to meet M1.DN.2."
53.	M1.S.6®	4.5.21	M1 Rules Add the description, "e.g. enlarge the metal width $\geq 0.35$ for the guard ring design."
54.	VIAx.S.3®	4.5.22	VIAx Rules Remove the recommendation
55.	VIAx.EN.0	4.5.22	VIAx Rules Add the rule
56.	VIAx.EN.0®	4.5.22	VIAx Rules Add the recommendation
57.	VIAx.EN.1	4.5.22	VIAx Rules Modify from " by Mx" to "by Mx or M1"
58.	VIAx.EN.1®	4.5.22	VIAx Rules Modify from " by Mx" to "by Mx or M1"
59.	VIAx.EN.2	4.5.22	VIAx Rules Modify from " by Mx" to "by Mx or M1"
60.	VIAx.EN.2®	4.5.22	VIAx Rules Modify from " by Mx" to "by Mx or M1"

From Version 1.5 to Version 2.0			
Rule	Sec. No.	Section Title	Revision Description
61.	VIAx.EN.3	4.5.22	VIAx Rules
62.	VIAx.R.11	4.5.22	VIAx Rules
63.	Mx.W.2	4.5.23	Mx Rules
64.	Mx.S.4	4.5.23	Mx Rules
65.	Mx.S.6®	4.5.23	Mx Rules
66.	Mx.EN.0	4.5.23	Mx Rules
67.	Mx.EN.0®	4.5.23	Mx Rules
68.	Mx.EN.3	4.5.23	Mx Rules
69.	VIAx.EN.1	4.5.24	VIAx Rules
70.	VIAx.EN.2	4.5.24	VIAx Rules
71.	Mn.S.3	4.5.25	Mn Rules
72.	Mn.R.2g <sup>U</sup>	4.5.25	Mn Rules
73.	VIAy.EN.0®	4.5.26	VIAy Rules
74.	VIAy.EN.1	4.5.26	VIAy Rules
75.	VIAy.EN.1®	4.5.26	VIAy Rules
76.	VIAy.EN.2	4.5.26	VIAy Rules
77.	VIAy.EN.2®	4.5.26	VIAy Rules
78.	My.W.2	4.5.27	My Rules
79.	My.S.4	4.5.27	My Rules
80.	My.S.6®	4.5.27	My Rules
81.	My.EN.0®	4.5.27	My Rules
82.		4.5.28	MOM Rules
83.		4.5.29	Via Layout Recommendations
84.	LOGO.O.1	4.5.30	Product Labels and Logo Rules
85.	LOGO.R.2	4.5.30	Product Labels and Logo Rules
86.	A.R.6	4.5.37	Antenna Rules
87.		4.5.37	Antenna Rules
88.		5.2	WPE
89.	AN.R.33mg <sup>U</sup>	5.4.1	General Guidelines
90.	AN.R.34mg <sup>U</sup>	5.4.1	General Guidelines
91.	AN.R.35mg <sup>U</sup>	5.4.1	General Guidelines
92.	DNW.S.6m	5.4.2	MOS Rules and Recommendations and Guidelines

From Version 1.5 to Version 2.0				
Rule	Sec. No.	Section Title	Revision Description	
93.	DNW.EN.3m	5.4.2	MOS Rules and Recommendations and Guidelines	Remove the rule
94.	OD.W.2m	5.4.2	MOS Rules and Recommendations and Guidelines	Remove the rule
95.	PO.EX.2mg <sup>U</sup>	5.4.2	MOS Rules and Recommendations and Guidelines	Change the rule to guideline
96.	AN.R.44mg <sup>U</sup>	5.4.2	MOS Rules and Recommendations and Guidelines	Add the guideline
97.	AN.R.36mg <sup>U</sup>	5.4.5	Capacitor Guidelines	Add the guideline
98.	AN.R.37mg <sup>U</sup>	5.4.5	Capacitor Guidelines	Add the guideline
99.	AN.R.38mg <sup>U</sup>	5.5.2	Matching Rules and Guidelines	Add the guideline
100.	AN.R.10mg <sup>U</sup>	5.5.2	Matching Rules and Guidelines	Modify the description from "Pay attention to the associated routing layout of the matching pair." to "Pay attention to the associated routing layout, as well as the associated pattern density, of the matching pair, to minimize the Rs difference."
101.	AN.R.12mg <sup>U</sup>	5.5.2	Matching Rules and Guidelines	Add the description, "Current mirror and"
102.	AN.R.39mg <sup>U</sup>	5.5.2	Matching Rules and Guidelines	Add the guideline
103.	AN.R.17mg <sup>U</sup>	5.5.3	Electrical Performance Rules and Guidelines	Add the description, "unsilicided"
104.	AN.R.40mg <sup>U</sup>	5.5.3	Electrical Performance Rules and Guidelines	Add the guideline
105.	AN.R.24mg <sup>U</sup>	5.5.4.1	Power and Ground	Add the description, "(width>1um)"
106.		5.6	Burn-in Guidelines for Analog Circuits	Add the section
107.	DOD.EN.1	6.1	DOD Rules	Add the description, "(fully outside is allowed)"
108.		7.1.2.1.1	Improvement of poly CD uniformity	Remove FILLER, 181.
109.		7.2	DFM Recommendations and Guidelines Summary	Add the description, "DFM does not have to comply to the advisory/recommendation value completely. Any change even by one grid helps."
110.		7.2.4	Grouping Table of DFM Action-Required Rules, Recommendations and Guidelines	Add the section
111.		7.4	MFU Optimization kit	Add the section
112.	LUP.2g	8.1	Layout Guidelines for Latch-Up Prevention	Modify the rule value from 15 to 10
113.	LUP.5g	8.1	Layout Guidelines for Latch-Up Prevention	Change DRC-unchecked item to DRC-checked item
114.	ESD.38g <sup>U</sup>	8.2.4	ESD Guidelines	Remove the guideline
115.		9.3.1.2.1	General	Update the table of section 9.3.1.2.1
116.		9.3.1.2.2	Dependence of metal length (length<20mm)	Add the section
117.		9.3.1.4	Dependence of Via array on DC current (Tj = 110°C)	Add the section
118.		9.3.1.10	Poly Current Density Guidelines	Add the description, "at a junction temperature of 110°C. This density is calculated using 0.1% point of measurement data at a 5% resistance increase after 100K hours of continuous operation."

From Version 1.5 to Version 2.0			
Rule	Sec. No.	Section Title	Revision Description
119.	9.3.2.2	Maximum DC Current for AP RDL Metal (AP-MD) Lines ( $T_j = 110^\circ\text{C}$ )	Modify the typo for AP-RDL $I_{max}$ from "2.02.7" to "2.7"
120.	9.3.2.3	Maximum DC Current for CB Vias (CB-VD) ( $T_j = 110^\circ\text{C}$ )	Modify the typo for CB-VD $I_{max}$ from "7294" to "7"
121.	9.4.3	Soft Error Rate	Add the section
122.	10	Electrical Parameters Summary	<ul style="list-style-type: none"> <li>● Update the electrical parameters summary based on T-N90-LO-SP-001 from V1.3 to V1.5</li> <li>● Update the electrical parameters summary based on T-N90-LO-SP-002 from V1.4 to V1.6</li> <li>● Update the electrical parameters summary based on T-N90-LO-SP-003 from V1.3 to V1.5</li> <li>● Update the electrical parameters summary based on T-N90-CL-SP-005 from V1.3 to V1.5</li> <li>● Update the electrical parameters summary based on T-N90-CL-SP-028 from V1.0 to V1.2</li> <li>● Update the electrical parameters summary based on T-N90-CL-SP-013 from V1.1 to V1.3</li> <li>● Update the electrical parameters summary based on T-N90-LO-SP-008 from V1.2 to V1.3</li> <li>● Update the electrical parameters summary based on T-N90-LO-SP-009 from V1.2 to V1.3</li> </ul>

## A.1.10 From Version 2.0 to Version 2.1

From Version 2.0 to Version 2.1			
Rule	Sec. No.	Section Title	Revision Description
1.			Merge T-N90-CM-DR-001( MS_RF rule, V1.1), T-000-CL-DR-002( PAD rule, V1.4), T-N80-CL-DR-001(N80 rule, V1.1), and T-N80-CM-DR-001( MS_RF rule, V1.0) into T-N90-LO-DR-001(Logic rule, V2.1)
2.		Title	Add CLN80: GC/ GT/ HS/ LP, CMN90: G/ GT/ LP, CMN80: GC, in the title
3.	1.1	Overview	Add CLN80: GC/ GT/ HS/ LP, CMN90: G/ GT/ LP, CMN80: GC
4.	1.2	Reference Documentation	Modifies Table 1.2.1
	1.3	Guidelines for Half Node Technologies (CLN80 only)	Removed
5.	2.1.1	Front-End Features	<ol style="list-style-type: none"> <li>1. Add the description "substrate resistivity of 8-12 Ω-cm"</li> <li>2. Add CLN80: GC/ GT/ HS/ LP, CMN90: G/ GT/ LP, CMN80: GC</li> <li>3. Update SRAM information</li> <li>4. Add NW resistor information</li> </ol>
6.	2.1.2	Back-End Features	<ol style="list-style-type: none"> <li>1. Add UTM information</li> <li>2. Add information of MOM, MiM, Inductor</li> <li>3. Add the descriptor, “ TSMC N80 generation does not support inductor devices.”</li> <li>4. Add electrical fuse information</li> </ol>
7.	2.2	Devices	<ol style="list-style-type: none"> <li>1. Add information of MOM, MiM, Inductor</li> <li>2. Add CLN80, CMN90, CMN80</li> </ol>
8.	2.3	Power Supply and Operation Temperature Ranges	Add CLN80, CMN90, CMN80
9.	2.4	Cross section	Add Cross section for MIM with/without UTM
	2.5	Metallization Options	<ol style="list-style-type: none"> <li>1. Add information of CLN80, CMN90, CMN80 metal/ Via</li> <li>2. Add table 2.5.5-9</li> <li>3. Add UTM in table 2.5.8</li> </ol>
10.	3.1	Mask Information, Key Process Sequence, and CAD Layers	<ol style="list-style-type: none"> <li>1. Add item 7, “In the table of section 3.1, “ * ” means optional mask. “ # ” means non-design level mask which is no need to draw (or design) this layer. This non-design level mask is generated by logical operation from other drawn layers..”</li> <li>2. Add the table 3.1.8-9</li> <li>3. Add the column, Non-design level mask, in table 3.1.10</li> </ol>
11.	3.4	Special Recognition CAD Layer Summary	<ol style="list-style-type: none"> <li>1. Modify Ncap_NTN,</li> <li>2. Add SRAMDMY_PE, DPSRM, LUPWDMY, RruleGuideline, excludeRRuleRequire, excludeRRuleRecommended, excludeRRuleAnalog, excludeRRuleGuideline.</li> <li>3. Copy Ms_RF related layers from T-N65-CM-DR-001</li> <li>4. Copy WBDMY from T-000-CL-DR-002.</li> <li>5. Remove ESD1DMY and ESD2DMY.</li> </ol>

## From Version 2.0 to Version 2.1

Rule	Sec. No.	Section Title	Revision Description
12.	3.5	Device Truth Tables	1. Add CLN80GC 2. Add CLN80GT 3. Add CLN80HS 4. Add CLN80LP 5. Add CMN90 6. Add CMN80
13.	3.5	Mask Requirement for Device options (High/STD/Low VT)	Add N80: GC/ GT/ HS/ LP
14.	OPC.R.2g	3.7.2	OPC Recommendations and Guidelines
15.		4.2.2	Special Definition
16.		4.4	Minimum Pitches
17.		4.5	CLN90 (Logic) Layout Rules and Guidelines
18.	DNW.R.5g	4.5.1.	DNW Rules  1. change it to DRC checkable 2. Add the description, DRC can flag RW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.
19.	NW.R.1g	4.5.3	NW Rules  1. Change it to DRC checkable 2. Add the description, DRC can flag both NW is not with CO in NPOD and PW is not with CO in PPOD, but DRC can not flag STRAP is not connected to Vdd/Vss.
20.	NWROD.R.2g <sup>U</sup>	4.5.4	NWROD Rules
21.	NWROD.R.3g	4.5.4	NWROD Rules  1. Change it to DRC checkable 2. Add the description, DRC can flag {NWDMY AND NW} is not a rectangle.
22.	NWRSTI.R.2g <sup>U</sup>	4.5.5	NWRSTI Rules
23.	NWRSTI.R.3g	4.5.5	NWRSTI Rules  1. Change it to DRC checkable 2. Add the description, DRC can flag {NWDMY AND NW} is not a rectangle.
24.	NT_N.R.3	4.5.6	NT_N Rules  Add the description " You have to draw a NCAP_NTN layer to cover the NMOS capacitors. The NCAP_NTN enclosure of OD have to be $\geq$ 0um. DRC also flags NCAP_NTN and OD outside of the NCAP_NTN in the same NT_N."
25.	PO.L.1	4.5.8	PO Rules  Add the description "except RTMOM region (RTMOMDMY, CAD layer:155;21)."
26.	PO.R.8	4.5.8	Add this rule
27.	RES.1g <sup>U</sup> RES.3g <sup>U</sup> RES.4g <sup>U</sup> RES.6g <sup>U</sup> RES.7g <sup>U</sup> RES.15g <sup>U</sup>	4.5.18	OD and Poly Resistor Recommendations and Guidelines
28.	RES.5g	4.5.18	OD and Poly Resistor Recommendations and Guidelines  Move it to RES.5m®
29.	CO.S.6g	4.5.20	CO Rules  1. Change it to DRC checkable 2. Add the description, DRC can flag if the STRAP is butted on source, one of STRAP and source is without CO.

## From Version 2.0 to Version 2.1

Rule	Sec. No.	Section Title	Revision Description
30.	CO.S.5g	4.5.20	CO Rules  1. Modify item 4 to, If it is hard to increase the CO to gate spacing (CO.S.3®) for the large transistor, limit the number of source/drain CO: to have the necessary CO number for the current, and then distribute the CO evenly on the Source/Drain area. If possible, also increase the CO to gate spacing (to reduce the short possibility by particle) 2. Change it to DRC checkable 3. Add the description, DRC can flag single CO.
31.	VIAx.EN.1®	4.5.22	VIAx Rules  Add this description “[VIA1 count <=2 in the region of (M1 AND M2) or VIAx count <=2 in the region of (Mx and Mx+1)]”
32.	VIAx.EN.2®	4.5.22	VIAx Rules  Add this description “[VIA1 count <=2 in the region of (M1 AND M2) or VIAx count <=2 in the region of (Mx and Mx+1)]”
33.	VIAx.R.9g	4.5.22	VIAx Rules  1. Change it to DRC checkable 2. Add the description, “DRC can flag single via.”
34.	Mx.EN.1®	4.5.23	Mx Rules  Add this description “[VIAx-1 count <=2 in the region of (Mx-1 AND Mx)]”
35.	Mx.EN.2®	4.5.23	Mx Rules  Add this description “[VIAx-1 count <=2 in the region of (Mx-1 AND Mx)]”
36.	VIAx.R.5g	4.5.24	VIAx Rules  1. Change it to DRC checkable 2. Add the description, “DRC can flag single via.”
37.	VIAy.EN.1®	4.5.26	VIAy Rules  Add this description “[VIAy count <=2 in the region of (Mx AND My+1) or VIAy count <=2 in the region of (My AND My+1)]”
38.	VIAy.EN.2®	4.5.26	VIAy Rules  Add this description “[VIAy count <=2 in the region of (Mx AND My+1) or VIAy count <=2 in the region of (My AND My+1)]”
39.	VIAy.R.9g	4.5.26	VIAy Rules  1. Change it to DRC checkable 2. Add the description, “DRC can flag single via.”
40.	My.EN.1®	4.5.27	My Rules  Add this description “[VIAy-1 count <=2 in the region of (Mx AND My) or VIAy count <=2 in the region of (My AND My+1)]”
41.	My.EN.2®	4.5.27	My Rules  Add this description “[VIAy-1 count <=2 in the region of (Mx AND My) or VIAy count <=2 in the region of (My AND My+1)]”
42.	SRAM.R.3 <sup>U</sup>	4.5.31	SRAM Rules  Modify the description from 2M to 4M. Modify the reference document from T-N90-CL-RP-001 to T-000-CL-RP-002.
43.	SRAM.R.4 <sup>U</sup>	4.5.31	SRAM Rules  Move the table to Table 4.5.31.1 and 4.5.31.2
44.	SRAM.R.14g <sup>U</sup>	4.5.31	SRAM Rules  Add this guideline.
45.	SR.S.1.1	4.5.34	Seal Ring Layout Rules  Add this rule
46.		4.5.36	Antenna Rules  Change diode to protection OD.
47.		4.6	CMN90 (Mixed Singnal, RF) Layout Rules and Guidelines  Add this section (merged from T-N90-CM-DR-001)
48.	A.R.MIM.9	4.6.6.2	Antenna Effect Prevention Layout Rules  Add this rule
49.		4.6.9	The Chip Corner Stress Relief Pattern (CSR) and Seal Ring Rules for UTM  Change GDS from N90SR_3XTM_L-mark_UTM_2007.gds to N90SR_3XTM_L-mark_UTM_20080402.gds. It is to copy CB(43;0) for CB2(86;0) because CB2(86;0) is missing in the UCDSRN90V1_UTM9 cell.
50.		5	Wire Bond, Flip Chip and Interconnection Design Rules  Add this chapter (merged from T-000-CL-DR-002)

## From Version 2.0 to Version 2.1

Rule	Sec. No.	Section Title	Revision Description	
51.	6	N80 Design Information	Add this chapter (merged from T-N80-CL-DR-001 and T-N80-CM-DR-001)	
52.	7.2	WPE	<p>1. Add item 1.</p> <p>2. Modify item: SPICE model has included the WPE effect. Users need to input SC in the netlist to activate these new features. During post-simulation LPE will automatically extract the SC from layout, and add the extracted SC to the netlist, then activate the model properly. (SC is the distance between gate to Well edge, please refer to the Appendix in the SPICE document). Not only NW layout but also OD2 layout will impact WPE calculation. Please refer to the 4 WPE recommendations in this section and the Figure 7.2.1.</p> <p>3. Add Figure 7.2.1</p> <p>4. Add Figure 7.2.2</p>	
53.	AN.R.44mg <sup>U</sup>	7.4.2	MOS Recommendations and Guidelines	Add this guideline
54.	RES.5m®	7.4.4	Resistor Rules and Recommendations	Add this recommendation
55.	AN.R.36mg <sup>U</sup>	7.4.5	Capacitor Guidelines	Change it to "It is recommended not to use a very long channel device in the design. In order to ensure the channel relaxation time of the MOS capacitor (excluding varactor) is enough to build up charge to the steady state, it is recommended to use proper channel length at the high operation frequency range. The operating frequency shall be below $0.2 * gm / Cgate$ , where gm is the transconductance of the transistor and Cgate is the gate-oxide capacitance."
56.	AN.R.25mg <sup>U</sup>	7.5.4.1	Power and Ground	Add the description, and also for the analog and digital circuits. (Figure 7.5.15).
57.	Mx.DN.1	8.3	DMx Rules	Change the excluded region from INDDMY to (INDDMY SIZING 18)
58.	Mx.DN.3	8.3	DMx Rules	Change the excluded region from INDDMY to (INDDMY SIZING 18)
59.	Mx.DN.3®	8.3	DMx Rules	Change the excluded region from INDDMY to (INDDMY SIZING 18)
60.	CTM.W.1®	9.2.2	Recommendations	Add this recommendation (merged from T-N90-CM-DR-001)
61.	UTM.EN.3®	9.2.2	Recommendations	Add this recommendation (merged from T-N90-CM-DR-001)
62.	UTM.DN.5®	9.2.2	Recommendations	Add this recommendation (merged from T-N90-CM-DR-001)
63.	CB.W.4® <sup>U</sup>	9.2.2	Recommendations	Add this recommendation (merged from T-000-CL-DR-002)
64.	AP.W.2® <sup>U</sup>	9.2.2	Recommendations	Add this recommendation (merged from T-000-CL-DR-002)
65.	UBM.S.4®	9.2.2	Recommendations	Add this recommendation (merged from T-000-CL-DR-002)
66.	UBM.EN.1®	9.2.2	Recommendations	Add this recommendation (merged from T-000-CL-DR-002)
67.	UBM.A.1®	9.2.2	Recommendations	Add this recommendation (merged from T-000-CL-DR-002)
68.	UBM.DN.1®	9.2.2	Recommendations	Add this recommendation (merged from T-000-CL-DR-002)

From Version 2.0 to Version 2.1			
Rule	Sec. No.	Section Title	Revision Description
69.	UBM.DN.3®	9.2.2	Recommendations
70.	UBM.R.6® <sup>U</sup>	9.2.2	Recommendations
71.	BP.R.2®	9.2.2	Recommendations
72.	UBM.R.7®	9.2.2	Recommendations
73.	VIA.R.8g <sup>U</sup>	9.2.3	Guidelines
74.	UTM.R.1g <sup>U</sup>	9.2.3	Guidelines
75.	UTM.R.9g <sup>U</sup>	9.2.3	Guidelines
76.	UBM.R.4g <sup>U</sup>	9.2.3	Guidelines
77.	UBM.R.5g <sup>U</sup>	9.2.3	Guidelines
78.		9.3	Mechanical and Thermal Guidelines for FCBGA
79.		9.4	GDA die size optimization kit
80.		10.1.1	Latch-up Introduction
81.		10.1.2.1	Special Definition in Latch-up Prevention
82.		10.1.2.2	Latch-up Dummy Layers Summary
83.		10.1.2.3	Layout Rules and Guidelines for Latch-up Prevention 1. Modify this section from Guidelines for Latch-up Prevention 2. Modify it from LUP.3 to LUP.6 3. Modify it from LUP.1/2/4/5/6/8/9 to LUP.1/2/3/4/5/7/8/9
84.		10.1.3	Test Specification and Requirements
85.		10.2.1	ESD introduction
86.		10.2.2	TSMC IO ESD layout style introduction
87.		10.2.3	ESD Dummy Layers Summary
88.		10.2.4	ESD circuits Definition
89.		10.2.5	Requirements for ESD Implant Masks
90.		10.2.6	ESD Guidelines 1. Modify this section from ESD Guidelines 2. Add ESD.WARN.1, ESD.WARN.2 3. Modify it from ESD.1-47 to ESD.1-57
91.		10.2.7	Tips for the Power Bus
92.		10.2.8	ESD test methodology
93.		11.3.1	Guidelines for Stress Migration(SM)
94.		11.3.2	Guidelines for Low-k Dielectric Integrity
95.		11.3.3.2	Maximum DC Current for Metal Lines, contact and Vias ( $T_j = 110^\circ\text{C}$ )
96.		11.3.3.4	Dependence of Via array/ Contact array on DC current ( $T_j = 110^\circ\text{C}$ )
97.		11.3.3.5	DC Operation, Required Number of Vias

From Version 2.0 to Version 2.1			
Rule	Sec. No.	Section Title	Revision Description
98.	11.3.4	N80 DC Current Density (EM) Specifications	Add this section (merged from T-N80-CL-DR-001)
99.	11.3.5.3	Root-Mean-Square Current	Add Mu information
100.	12	Electrical Parameters Summary	Add CLN80: GC/ GT/ HS/ LP, CMN90: G/ GT/ LP, CMN80: GC

## A.1.11 From Version 2.1 to Version 2.2

From Version 2.1 to Version 2.2			
Rule	Sec. No.	Section Title	Revision Description
1.			Merge T-N90-CR-DR-001(SBD rule, V1.0), T-N90-CL-DR-017 (ULVt rule, V1.0), T-N85-CL-DR-001(N85 rule, V1.0) into T-N90-LO-DR-001(Logic rule, V2.2)
2.	Title		Add CLN85: G/LP, CMN85: G/LP in the title
3.	1.1	Overview	Add CLN85: G/LP, CMN85: G/LP
4.	1.2	Reference Documentation	Modifies Table 1.2.1
5.	2.1.1	Front-End Features	Add N85 SRAM cells in different process
6.	2.1.2	Back-End Features	1. Add AP-MD information
7.	2.2	Devices	1. Modify table 2.2.1 2. Add CLN85/CMN85 into table notes
8.	2.3	Power Supply and Operation Temperature Ranges	1. Modify table 2.3.1 2. Add CLN85, CMN85 3. Add maximum power supply voltage
9.	2.5	Metallization Options	1. Modify table 2.5.1, table 2.5.2 2. Add CLN85, CMN85, AP-MD, RV 3. Modify the CLN90 Vx value from 01.5 to 0.15 4. Modify table 2.5.3~2.5.9 to add RV and AP-MD
10.	3.1	Mask Information, Key Process Sequence, and CAD Layers	1. Add ULVT_N/ULVT_P into table 3.1.3 (Merge from T-N90-CL-DR-017) 2. Add table 3.1.4~5/ 3.1.11, modify table 3.1.13 (merge from T-N85-CL-DR-001)
11.	3.3	Special Recognition CAD Layer Summary	1. Add CTMDMY(drawing 1), RFDMY(drawing 1), SBDDMY, VDDDMY, VSSDMY, M1(pin)~ MD(pin), DMDEXCL 2. Modify WBDMY CAD layer to 183;0
12.	3.4	Device Truth Tables	1. Add ULVt_N/P into CLN90LP, and SBD into CMN90 2. Add sections for CLN85G, CLN85LP, CMN85
13.	3.5	Mask Requirements for Device Options (High/STD/Low VT)	1. Add Ultra Low Vt into table 3.5.1 2. Add table 3.5.2 (merge from T-N85-CL-DR-001)
14.	G.1	Design Geometry Rules	Add the description, DRC will not flag UBM/CBD/PM/CB2/PM2/PPI layers when vertexes of polygon are larger than 100.
15.	3.6.1.1	DBU guideline	Add
16.	OPC.R.1®	OPC Recommendations and Guidelines	Add the description "The OPC layers: OD, PO....".
17.	DNW.S.2	Deep N-Well (DNW) Layout Rules (MASK ID:119) [Optional]	Add the description " with different potential"
18.	DNW.EN.1®	Deep N-Well (DNW) Layout Rules (MASK ID:119) [Optional]	Add the description "Except SBDDMY region"
19.	OD.R.1	Gate Oxide and Diffusion (OD) Layout Rules (Mask ID: 120)	Add the description "SBDDMY region"
20.	NW.S.3	N-Well (NW) Layout Rules	Add the description " with different potentials"
21.	NWRD.R.4 NWRD.R.5 NWRD.R.6 NWRD.R.7	N-Well Resistor Within OD (NWRD) Layout Rules	Add
22.	4.5.6	Native Device (NT_N) Layout Rules	Remove the description "A Native NMOS device is based on a standard Vt process. It cannot be applied to pure low Vt designs."
23.	PO.R.5g <sup>U</sup>	Poly (PO) Layout Rules (Mask ID: 130)	Remove
24.	4.5.13	Ultra Low Vt NMOS (ULVT_N) Layout Rules (Mask ID: 11R)	Add (merge from T-N90-CL-DR-017 and T-N85-CL-DR-001)
25.	4.5.14	Ultra Low Vt PMOS (ULVTP) Layout Rules	Add (merge from T-N90-CL-DR-017 and T-N85-CL-DR-001)

From Version 2.1 to Version 2.2			
Rule	Sec. No.	Section Title	Revision Description
		(Mask ID: 11Q)	
26.	PP.EX.1	4.5.16 P+ Source/Drain Ion Implantation (PP) Layout Rules (Mask ID: 197)	Add the description "except SBDDMY region"
27.	PP.R.3	4.5.16 P+ Source/Drain Ion Implantation (PP) Layout Rules (Mask ID: 197)	Add the description "SBDDMY region"
28.	NP.R.3	4.5.17 N+ Source/Drain Ion Implantation (NP) Rules (Mask ID: 198)	Add the description "SBDDMY region"
29.		4.5.18 Layout Rules for LDD Mask Logical Operations	Remove the warning description "recommendations"
30.	RES.8	4.5.20 OD and Poly Resistor Guidelines	Add
31.	RES.11 RES.12	4.5.20 OD and Poly Resistor Guidelines	Change the guidelines to rules
32.	CO.S.6	4.5.22 Contact (CO) Layout Rules (Mask ID: 156)	Add the description "except SBDDMY region"
33.	MOM.R.1g <sup>U</sup>	4.5.30 MOM Layout Rules	Remove
34.		4.5.30.1 RTMOM (Rotated Metal Oxide Metal) Capacitor Guidelines	1. Remove figure 4.5.30.1.1 2. Add description for item 1
35.		4.5.33 SRAM Rules	Add the table 4.5.33.2
36.		4.5.35.1 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	1. Add the description "TSMC offers new sealring structures in WLCSP...". 2. Add the description "Mask combination CB (mask ID: 107)/ AP (mask ID: 307)/ CB (mask ID: 107) is not allowed for WLCSP process"
37.	CSR.EN.4 CSR.EN.4.1 CSR.EN.5 CSR.EN.5.1	4.5.35.2 Chip Corner Stress Relief Pattern (CSR) Layout Rules	1. Add the description "Except WLCSP sealring region" 2. Add the rule for WLCSP sealring 3. Add the description "Except WLCSP sealring region" 4. Add the rule for WLCSP sealring 5. Add the figure of chip corner stress relief pattern for WLCSP
38.	SR.S.1	4.5.36 Seal Ring Layout Rules	Modify the description for non-WLCSP seal ring and for WLCSP seal ring
39.	SR.S.1.1	4.5.36 Seal Ring Layout Rules	Add the description "Except WLCSP sealring region"
40.	SR.EN.1	4.5.36 Seal Ring Layout Rules	Add
41.		4.5.36 Seal Ring Layout Rules	1. Add cross-sectional view of WLCSP sealring 2. Add the mask information for WLCSP layers
42.	A.R.10~13	4.5.38 Antenna Effect Prevention (A) Layout Rules	Merge from 5.1.2.6.3 Antenna Effect Prevention (A) Layout Rules for RV and AP-MD.
43.	Mx.DN.5 Mx.R.3g <sup>U</sup>	4.6.2 Capacitor Bottom Metal (CBM) Layout Rules (Mask ID: 183)	Add
44.		4.6.6.1.2 MIM Structure Recognition Methodology	Add this section
45.		4.6.6.1.3 Check Methods	Change the figures of (j), (o), (p) from balanced to unbalanced
46.	A.R.MIM.1 A.R.MIM.2 A.R.MIM.3 A.R.MIM.4 A.R.MIM.5 A.R.MIM.9	4.6.6.2 Antenna Effect Prevention Layout Rules	1. Modify the rules' description to cumulative metal top area and AP-MD sidewall area 2. Add the description "Both A.R.MIM.2 and A.R.MIM.3...." 3. Modify the description to cumulative both VIA and RV 4. Add the description "Both A.R.MIM.4 and A.R.MIM.5...." 5. Remove the wording of A.R.MIM.9 "structures in figure (j),(o),(p) are also not allowed."
47.	A.R.MIM.6 A.R.MIM.7	4.6.6.2 Antenna Effect Prevention Layout Rules	1. Merge into A.R.MIM.4 2. Merge into A.R.MIM.5
48.		4.6.9 Schottky Barrier Diode (SBD) Layout Rules	Add (merge form T-N90-CR-DR-001)
49.		4.6.10 The Chip Corner Stress Relief Pattern (CSR) and Seal Ring Rules for UTM	Add the description "Sample GDS file for 3XTM L-mark seal-ring corner of WLCSP.."
50.		4.6.10.1 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	Add the sample GDS file of WLCSP

From Version 2.1 to Version 2.2			
Rule	Sec. No.	Section Title	Revision Description
51.	CSR.EN.5 CSR.EN.5.1	4.6.10.1 Guidelines for Placing Chip Corner Stress Relief (CSR) Patterns	1. Add the description "Except WLCSP sealring region" 2. Add this rule for WLCSP 3. Add the figure in the section 4.6.10.1.2
52.	SR.EN.1	4.6.10.2 Seal Ring Layout Rules for UTM	1. Add this rule 2. Add the cross-sectional view of WLCSP seal ring
53.		5 Wire Bond, Flip Chip and Interconnection Design Rules	1. Add the warning information 2. Add the description for 14.5K and 28K of AP-MD thickness 3. Add the description for lead-free bump design rule, please consult with tsmc.
54.	CBVIAx.R.4	5.1.2.3 Pad Structure Rules	Modify the description to "at square metal crossing region with width equal to CBMx.W.2 in pad area" from "at metal crossing in pad area"
55.		5.1.2.5 Wire Bond Non-shrinkable Rules for the N85	Add this section (merge from T-N85-CL-DR-001)
56.	AP.W.2 <sup>U</sup>	5.1.2.7.2 AP-MD Layout Rules	Change the rule value from 15 to 10
57.	RV.R.1	5.1.2.7.1 RV Layout Rules (CB VIA hole)	Add the description "Except WLCSP seal ring region"
58.	AP.S.1.1	5.1.2.7.2 AP-MD Layout Rules	Add the description "Except spacing in the same polygon"
59.	AP.R.1 <sup>U</sup>	5.1.2.7.2 AP-MD Layout Rules	Add the wording "Need to add polyimide layer for wirebond using AP-MD routing for die size >= 100mm <sup>2</sup> "
60.		Antenna Effect Prevention (A) Layout Rules for RV and AP-MD.	Remove (merge into 4.5.38 Antenna Effect Prevention (A) Layout Rules)
61.		5.2 Layout Rules for EU/HL Flip Chip	1. Modify the title to add "EU/HL" 2. Remove the wording of LF: lead free 3. Add the description "For lead free application, please refer to LF design rule"
62.		5.2.1 Recommendations for EU/HL Flip Chip	Add the description of item 14 "If you are going to design a new product....."
63.		5.2.2 Under Bump Metallurgy (UBM) Rules	Add the description "For lead-free bump design rule, please consult with tsmc"
64.	UBM.DN.1	5.2.2 Under Bump Metallurgy (UBM) Rules	Modify the rule value to 10% from 2.5%
65.	UBM.DN.1 <sup>®</sup>	5.2.2 Under Bump Metallurgy (UBM) Rules	Remove (merge into UBM.DN.1)
66.	UBM.DN.2	5.2.2 Under Bump Metallurgy (UBM) Rules	Remove (merge into UBM.DN.1)
67.	UBM.DN.3	5.2.2 Under Bump Metallurgy (UBM) Rules	Remove the description "for the die sizing > = 169mm <sup>2</sup> "
68.	UBM.DN.3 <sup>®</sup>	5.2.2 Under Bump Metallurgy (UBM) Rules	Remove (merge into UBM.DN.3)
69.	UBM.R.5	5.2.2 Under Bump Metallurgy (UBM) Rules	1. Change the " <sup>U</sup> " to the rule and modify the description 2. Add the Note for LF application 3. Add the schematic diagram
70.		5.2.3 Flip Chip Rules	1. Add N85 wording 2. Remove the description "Ground-up (with CBD) ...." due to repeat
71.	BP.EN.5	5.2.3.2 Bump Pad Structure Rules	Add the description "without AP RDL/ with AP RDL..."
72.		5.2.3.2 Bump Pad Structure Rules	Add the description "For lead free application, please refer to LF design rule"
73.		5.2.3.3 Polyimide (PM) Rules for EU/HL Flip Chip	1. Modify the title to add "EU/HL" 2. Add the description "Polyimide is must for LF application....."
74.		5.2.3.4 Flip Chip Non-shrinkable Rules for the N85	1. Add this section (merge from T-N85-CL-DR-001) 2. Modify BP.EN.4 to add "without PM"
75.	BP.EN.5	5.2.3.5 Flip Chip Non-shrinkable Rules for the N80	Add the description "without AP RDL/ with AP RDL..."
76.		5.2.3.6 Redistribution Metal Layout Rules	Add the AP-MD 28K into the table of redistribution metal
77.	RV.R.1	5.2.3.7.1 RV Layout Rules (Passivation-1 VIA Hole)	Add the description "Except WLCSP seal ring region"
78.	AP.W.2 <sup>U</sup>	5.2.3.7.2 AP-MD Layout Rules	Change the rule value from 15 to 10
79.		6 N85 Design Information	Add this chapter (merge from T-N85-CL-DR-001)

From Version 2.1 to Version 2.2			
Rule	Sec. No.	Section Title	Revision Description
80.	BP.EN.4	6.2.2.1	Non-shrinkable Rules Modify BP.EN.4 to add " without PM"
81.	BP.EN.5	7.2.3.1	Non-shrinkable Rules Add the description " without AP RDL/ with AP RDL..."
82.		7.5	Design Flow For Tape-Out Modify this section
83.	DMx.S.8	9.3	Dummy Metal (DM) Rules Modify the rule value from 18 to 2.5 (follow the value of N65)
84.	DMx_O.R.1	9.3	Dummy Metal (DM) Rules Add
85.	AP.W.2® <sup>U</sup>	10.2.2	Recommendations Change the rule value from 15 to 10
86.		10.2.2	Recommendations Add the description " For lead free application, please refer to LF design rule"
87.	PO.R.5g <sup>U</sup>	10.2.3	Guidelines Remove
88.		11.1.1	Latch-up Introduction Update figures 11.1.3~11.1.6
89.		11.1.2.3	DRC methodology for Latch-up Rules Add this section
90.		11.2.6.7	CDM Protection for Cross Domain Interface Add this section
91.		11.2.7	Tips for the Power Modify the description
92.		11.2.7.1	Approach 1 Modify the description
93.		12.2	Front-End Process Reliability Rules and Models 1. Add N85 reliability informations 2. Add the description for guidelines for negative bias temperature instability (NBTI) 3. Add the description for failure mechanism of NBTI
94.		12.3	Back-End Process Reliability Rules 1. Add N85 DC current density (EM) Specifications 2. Modify N80 DC current density (EM) Specifications
95.		12.3.7	Maximum DC Current for AP RDL Metal (AP-MD) Lines ( $T_j = 110^\circ\text{C}$ ) Add the $I_{max}$ DC current for AP RDL 28K Å.
96.		12.3.8	N90/N85/N80 AP RDL AC Operation 1. Add $I_{rms}$ for AP RDL 28K Å. 2. Add the description " The $I_{peak}$ rule for AP RDL is 58mA/um for RDL thickness = 14.5K Å." 3. Add the description " The $I_{peak}$ rule for AP RDL is 112mA/um for RDL thickness = 28.0K Å."
97.		13	Electrical Parameters Summary Modify this section and add the key parameters of MOS transistors

## A.2 Revision History of T-N90-CM-DR-001 (MS\_RF)

### A.2.1 Version 0.1

#### A.2.1.1 New

	New Rule (Version 0.1)	Impact Description
	Version 0.1	Only include MIM and UTM design rule

### A.2.2 From version 0.1 to version 1.0

From Version 0.1 to Version 1.0 (The rule code, section no, section title, and revision description are based on Version 0.1.)			
Rule	Sec. No.	Section Title	Revision Description
	1.3.1		Allow MIM directly with UTM.
	2.2.1	Metallization Option Tables	More flexible metal scheme. 1.TM 2.UTM 3.TM+TM 4.TM+UTM
CTM.S.3	4.5.1	Capacitor Top Metal (CTM) Layout Rules (182)	Space change to 0.54.
CBM.S.2	4.5.2	Capacitor Bottom Metal (CBM) Layout Rules (183)	Space change to 0.54.
CBM.W.3	4.5.2	Capacitor Bottom Metal (CBM) Layout Rules (183)	Mcap width 0.84 in CTMDMY
CMB.S.3	4.5.2	Capacitor Bottom Metal (CBM) Layout Rules (183)	Mcap space0.84 in CTMDMY
CBM.W.5	4.5.2	Capacitor Bottom Metal (CBM) Layout Rules (183)	UTMcap width 2.0 in CTMDMY
CMB.S.7	4.5.2	Capacitor Bottom Metal (CBM) Layout Rules (183)	UTMcap space 2.0 in CTMDMY
UTM.W.3	4.5.3	Ultra Thick Metal (UTM) Layout Rules (389)	Allow metal max width in INDDMY
UTM.R.4	4.5.3	Ultra Thick Metal (UTM) Layout Rules (389)	Modify the description of pick up ring
	4.5.4	The Chip Corner Stress Relief Pattern (CSR) and Seal Ring Rules for the UTM Process	Add CSR and seal ring rule
	4.5.4.1	The Chip Corner Stress Relief (CSR) Pattern for UTM	Add CSR and seal ring rule
	4.5.4.2	Seal Ring Layout Rules for UTM9	Add CSR and seal ring rule

## A.2.3 Rules Mapping Table From ver. 1.0 to ver. 1.1

Ver. 1.0	Ver. 1.1
<b>CTM Rules</b>	
CTM.W.1	CTM.W.1
	CTM.W.1®
CTM.W.2	CTM.W.2
CTM.S.1	CTM.S.1
	CTM.R.4
CTM.R.3 <sup>U</sup>	Remove
<b>CBM Rules</b>	
CBM.W.1	CBM.W.1
CBM.W.2	CBM.W.2
CBM.S.1	CBM.S.1.1
CBM.S.5	CBM.S.2
CBM.S.6	CBM.S.1.2
	CBM.EN.1
CBM.EN.2	CBM.EN.2
CBM.R.2	CBM.R.2
<b>UTM Rules</b>	
UTM.W.1	UTM.W.1
CBM.W.5	
UTM.W.2	UTM.W.2
UTM.W.3	UTM.W.3
UTM.S.1	UTM.S.1
UTM.S.2	UTM.S.2
UTM.S.3	Remove
UTM.EN.1	UTM.EN.1
UTM.EN.2	UTM.EN.2
UTM.R.1	UTM.EN.3®
UTM.A.1	UTM.A.1
UTM.A.2	UTM.A.2
UTM.R.2	UTM.R.2
UTM.R.3	UTM.R.3
UTM.R.4	UTM.R.4
UTM.W.4	UTM.W.4
UTM.R.6	UTM.R.6 <sup>U</sup>
	UTM.R.8

Ver. 1.0	Ver. 1.1
<b>UTM Rules</b>	
UTM.DN.1	UTM.DN.1
UTM.DN.2	UTM.DN.2
UTM.DN.3	UTM.DN.3
CBM.DN.1	UTM.DN.4
CBM.DN.2	
	UTM.DN.5®
	UTM.R.1g <sup>U</sup>
	UTM.R.9g <sup>U</sup>
<b>VIA n rules</b>	
CTM.S.2	VIA n.S.3
CTM.S.3	VIA n.S.4
CBM.S.2	VIA n.S.5
CTM.EN.1	VIA n.EN.3
CBM.EN.1	VIA n.EN.4
UTM.EN.3	VIA n.EN.5
CBM.R.1	VIA n.R.7
UTM.R.5	VIA n.R.9
CTM.R.2®	VIA n.R.8g <sup>U</sup>
<b>Mn Rules</b>	
CBM.W.3	Mn.W.4
CBM.S.3	Mn.S.4
CBM.S.4	Mn.S.5
CBM.EN.3	Mn.EN.3
CBM.DN.1	Mn.DN.5
CBM.DN.2	
<b>MIM Antenna Rules</b>	
	A.R.MIM.1
	A.R.MIM.2
	A.R.MIM.3
	A.R.MIM.4
	A.R.MIM.5
	A.R.MIM.6
	A.R.MIM.7
	A.R.MIM.8

Ver. 1.0	Ver. 1.1
<b>CSR Rules</b>	
CSR.R.1	CSR.R.1
CSR.R.2	CSR.R.2
CSR.R.3	CSR.R.3
CSR.S.1	CSR.S.1
CSR.EN.1 <sup>U</sup>	CSR.EN.1 <sup>U</sup>
CSR.S.2	CSR.S.2
CSR.EN.2 <sup>U</sup>	CSR.EN.2 <sup>U</sup>
CSR.S.3	CSR.S.3
CSR.EN.3 <sup>U</sup>	CSR.EN.3 <sup>U</sup>
CSR.R.4	CSR.R.4
	CSR.W.1
	CSR.L.1
	CSR.EN.4
	CSR.EN.5
	CSR.W.2
	CSR.W.3
	CSR.EN.6
	CSR.EN.7

## A.3 Revision History of T-N80-CL-DR-001 (N80 logic)

### A.3.1 From Version 0.1 to Version 0.2

Rule No.	From Version 0.1 to Version 0.2		
	Section		Revision Description
	No.	Title	
1.	1.1	OVERVIEW	Remove CLN90G shrink to CLN80GT. CLN90G should shrink to CLN80G in future
2.	1.2	Related Design Rule Manuals and Documents	N80 dummy patterns generation utility is obsolete and replaced by the most updated N90 utility. Dummy OD/PO generation utility: T-N80-CL-DR-001-C2 is obsoleted and replaced by T-N90-LO-DR-001-C2. Dummy Mx generation utility: T-N80-CL-DR-001-C3 is obsoleted and replaced by T-N90-LO-DR-001-C3. Add SPICE, SRAM, Latch-up and Brief process flow documents.
3.	1.3.2/2.4	1.3.2 SRAM Design Specifications 2.4 Special Recognition CAD Layer Summary	Rename SRAMDMY (186;1) to AMDMY_PE(186;1)
4.	1.3.2/4.1	1.3.2 SRAM Design Specifications 4.1 How to shrink the existing CLN90 design	Add “Fuse circuit must .....CLN80 IP circuit”.
5.	2.1/2.3 /2.5.1 /2.6	2.1 Devices 2.3 Reserved mask name and ID, Key process sequence, and CAD layer 2.5.1 CLN80GT (1.2V Core Design) 2.6 Mask Requirements for Device Options (High/Std Vt)	Remove VTUH_N and VTUH_P mask for process flow table and Ultra high Vt N/PMOS from device truth table. Because CLN80GT does not provide ultra high Vt.
6.	2.3	Reserved mask name and ID, Key process sequence, and CAD layer	Rename OD2 CAD layer from “15” to “41”
7.	OD.W.3	Non-shrinkable Layout Rules	Delete; this rule is allowed to shrink.
8.	M1.A.2	Non-shrinkable Layout Rules	Delete; this rule is allowed to shrink.
9.	Mx.A.2	Non-shrinkable Layout Rules	Delete; this rule is allowed to shrink.
10.	DOD/DPO /DMx rules	3.2.2.3 Dummy pattern (DOD/DPO/DMx) rules	Delete; these dummy rules are allowed to shrink.
11.	OD_DECAP Rules	3.3 Core Decoupling Capacitor (OD_DECAP) Layout Rules (For CLN80HS only)	Add Core Decoupling Capacitor (OD_DECAP) Rules for CLN80HS only
12.	CB.W.2	3.2.3 Pad Rule for Wire Bond	1. Add non-shrinkable rule for stagger pad(60um)2.Delete non-shrinkable rule(CB.W.2) of 55um pitch single in-line pad and allow to shrink.
13.	UBM.S.1	3.2.4 Flip Chip Bump Rules	Relax from 66um to 55um
14.	UBM.S.3	3.2.4 Flip Chip Bump Rules	Relax from 99um to 88um
15.		3.1 General Logic Design Specifications	Add one item of “Dummy OD/PO/Mx (DOD/DPO/DMx) patterns and rules are shrinkable.”
16.		4.1 How to shrink the existing CLN90 design	Add one item of “Dummy OD/PO/Mx (DOD/DPO/DMx) patterns and rules are shrinkable.”
17.			
18.		4.1 How to shrink the existing CLN90 design	Modify Fig. 4.1.
19.		4.2 How to prepare a new design of CLN80	Modify Fig. 4.2
20.		4.4 Layout checking and post simulation	Modify Fig. 4.4

## A.3.2 Version 0.2 to Version 1.0

From Version 0.2 to Version 1.0			
Rule	Sec. No.	Section Title	Revision Description
101.  Release CLN80GC/LP		Title	Add "(GC/ GT/HS/LP)" in the title
		1.1 Overview	Add CLN80GC and CLN80LP process introduction
		1.3.2 SRAM Design Specification	Update UHD and DP SRAM for CLN80GC and SP SRAM for CLN80LP.
		2.1 Device	Update 1.0V/3.3V for CLN80GC, 1.2/2.5V for CLN80LP and Low Vt device for CLN80HS
		2.2 Power Supply and Operation Temperature	Update thickness 1.0V/3.3V for CLN80GC and 1.2V/2.5V for CLN80LP
		2.3 Reserved mask name and ID, Key process sequence, and CAD layer	Add Table 2.3.1 for CLN80GC and Table 2.3.4 for CLN80LP
		2.5 Device Truth Table	Add Table 2.5.2 for CLN80GC and Table 2.5.5 for CLN80LP
		2.6 Mask Requirement for Device Options (High/STD/Low Vt)	Add Table 2.6.1 for CLN80GC and Table 2.6.4 for CLN80LP. Update Table 2.6.3 with "STD+Low Vt" option
102.	Release 2XTM for CLN80	3.2.2.3	Stress Migration and Wide Metal Spacing Rules Adjustment
		Chapter 5	Electrical Parameter Summary
103.	NT_N.W.2.2	3.2.2.1	New native device rules for CLN80HS
104.	NT_N.W.2.3		3.3V IO channel length is non-shrinkable (CLN80GC)
105.	PO.W.3		New rule to avoid the device degradation due to PO/OD rounding
106.	PO.S.2.1		Remove and follow CO.EN.3® of N90
107.	PO.A.3		Remove and follow M1.EN.2® of N90
108.	CO.EN.3®	3.2.2.2	Remove and follow M1.EN.3® of N90
109.	M1.EN.2®		Remove and follow VIAx.EN.2® of N90
110.	M1.EN.3®		Remove and follow Mx.EN.2® of N90
111.	VIAx.EN.2®		Remove and follow Mx.EN.2® of N90
112.	Mx.EN.2®		Remove and follow CO.EN.3® of N90
113.	M1.S.2.1	3.2.2.3	New rule to avoid the DRC false alarm on 10% size-up circuit
114.	Mx.S.2.1		Refine 50 & 55um single-in-line and 60um staggered pad and align with wire bond pad rule (T-000-CL-DR-002)
115.	CB.W.1	3.2.3	Add CB.W.2= 66um as the 55um single in line and 60um stagger pad. But it is same with N90 pad rule.
116.	CB.W.2		Refine 50 & 55um single-in-line and 60um staggered pad and align with wire bond pad rule (T-000-CL-DR-002)
117.	CB.S.1		Refine the design flow by replacing a new figure.
118.	Figure 4.1	4.1	Refine the design flow by replacing a new figure.
119.	Figure 4.2	4.2	Refine the design flow by replacing a new figure.
120.		Chapter 5	Update the electrical parameters of CLN80GC/GT/HS/LP

## A.3.3 Version 1.0 to Version 1.1

From Version 1.0 to Version 1.1			
Rule	Sec. No.	Section Title	Revision Description
1.	1.1	Overview	<ul style="list-style-type: none"> <li>• Add 2.5V option for CLN80GC.</li> <li>• Add the description, "Capacitor and Varactor for CLN80HS"</li> </ul>
2.	1.3.1	General Logic Design Specifications	Add the description, "It's recommended to use 1 nm design grid on 110% size-up IP layout to minimize the device layout mismatch due to data truncation or grid snapping....." and "For newly developed IP, if a compatible design for both CLN90 and CLN80 is preferred, please consider the following guidelines besides non-shrinkable rules....."
3.	2.2	Power Supply and Operation Temperature Ranges	Add 2.5V option for CLN80GC.
4.	2.3	Reserved mask name and ID, Key process sequence, and CAD layer	Add the warning message, "Warning: Tsmc will evaluate the necessity of PO mask revision if you only have OD mask revision."
5.			Add 30A mask
6.	2.5.1	CLN80GC (1.0V Core Design)	Add 2.5V option
7.	2.5.3	CLN80HS (1.05V Core Design)	Delete 1.05V Varactor
8. NT_N.W.2	3.2.2.1	Non-shrinkable rule	Delete the wording, GC.
9. NT_N.W.2.2			Add the wording, GC. So, channel length of CLN80GC core native device from 0.22 to 0.5 due to the change of NT_N.W.2 and NT_N.W.2.2.
10. NT_N.W.3			Add the wording, 3.3V
11. PO.S.2.1			Delete the rule
12. PO.A.3			Delete the rule
13. VAR.R.6			Add the rule
14.	3.2.4.1	Non-shrinkable rule	Add the warning message for bump pitch 150~175um and UBM width 80um.
15.	3.2.6	AP Metal Fuse Rules	Add the section
16.	3.3	Core Decoupling Capacitor (OD_DECAP) Layout Rules (For CLN80HS only)	Add the description, "A second choice is provided for the Core MOS capacitor by using OD_DECAP for lower leakage performance requirement."
17. OD_DECAP. W.2			Add the rule.
18.	3.4	Current Density (EM) Specifications	Add 2XTM DC EM information
19.	3.4.2.2	Dependence of metal length (length<20mm)	Add the section
20.	3.4.2.4	Dependence of Via array on DC current ( $T_j = 110^\circ C$ )	Add the section
21.	3.2.6	AP Metal Fuse Rules	Add the section from T-000-CL-DR-005.
22.	4.1	How to shrink the existing CLN90 design	Add the description, "It's recommended to use 1 nm design grid on 110% size-up IP layout to minimize the device layout mismatch due to the data truncation or grid snapping."
23.	4.3	110% size-up	Re-write the section
24.	4.4.1	SPICE Guidelines	Provide some examples for "Contact-to-poly parasitics" and "Macro Model Resistor & Capacitor (or Varactor)"
25.	4.4.2	RC Extraction Guidelines	Update figure 4.5 layout extraction flow
26.	Chapter 5	Electrical Parameter Summary	<ul style="list-style-type: none"> <li>• Update the related information of T-N80-CL-SP-001 from V1.0 to V1.1</li> <li>• Update the related information of T-N80-CL-SP-005 from V0.1 to V1.0</li> <li>• Add the related information of T-N80-CL-SP-014 V0.1</li> <li>• Add the related information of T-N80-CL-SP-015 V0.1</li> </ul>

## A.4 Revision History of T-000-CL-DR-002 (Pad)

### A.4.1 Change from Each Document to Version 1.0

#### A.4.1.1 Merged from Design Rule Documents

Version 2.0 includes rules that were merged from the following Design Rule documents:

- T-000-LO-DR-001: TSMC AL BOND PAD DESIGN RULE FOR WIRE BOND (Ver.2.3)
- T-000-LO-DR-004: TSMC CU BOND PAD DESIGN RULE FOR WIRE BOND (Ver.0.3)
- T-000-FC-DR-001: TSMC FLIP CHIP BOND PAD DESIGN RULE FOR AL PAD (Ver.2.1)
- T-000-FC-DR-002: TSMC FLIP CHIP BOND PAD DESIGN RULE FOR CU PAD (Ver.1.2)
- T-000-LO-DR-002: REDISTRIBUTION FOR SOLDER BUMP DESIGN RULE (Ver.0.4)
- T-000-FC-DR-003: TSMC POST PASSIVATION INTERCONNECTION (PPI) FOR SOLDER BUMP DESIGN RULE (Ver.0.2)
- T-000-LO-DR-005: TSMC CMOS LOGIC GENERAL PURPOSE COPPER INTERCONNECTION DESIGN RULE FOR FLIP CHIP (Ver.0.1)
- T-000-FC-DR-004: TSMC AL INTERCONNECT DESIGN RULE FOR FLIP CHIP (0.15/0.18/0.22/0.25UM) (Ver.0.1)

#### A.4.1.2 Rule Changes from Pre-merged Document to this Version 1.0 Merged Document

##### T-000-LO-DR-001 (Ver.2.3)

Rule	Revision
CB	Added CB structure rules of CL022 (via and metal rules)
CB.EN.1	Revised CB.EN.1 from M1/M2 to M1~Mtop-3.
CB.R.1	Changed the pattern of notch (50 µm pitch) and the length of probing area from 60 µm to 50 µm.
CB.W.1	Changed 48 µm to 43 µm for BGA and from 53 µm to 48 µm for non-BGA.
CB.W.3	<ul style="list-style-type: none"> <li>• Changed M1/M2 to M1~Mtop-3 and 50.</li> <li>• Added 50 µm for 80 µm pitch staggered.</li> </ul>
Double bonds	Added wording that double bonds are for QFP only.
Pitch (50 µm)	Merged 50 µm pitch rules (43 µm* 80 µm) with the CB rule for BGA.
PM.R.3	Revised PM.R.3 and removed the PM logical operation.
Staggered	Changed inner/out tier of staggered to inner/outer pad.
Tri-Tier	Changed first/second/third tier of Tri-Tier to inner/middle/outer pad.

##### T-000-LO-DR-004 (Ver.0.3)

Rule	Revision
CB.EN.1	Revised CB.EN.1 from M1/M2 to M2~Mtop-3.
CB.R.1/CB.W.3	Added rules.
CB.S.1	Add CB.S.1= 9 µm for 50µm and 55µm pitch
CB.W.1	Add CB.W.1= 46 µm of 55µm pitch for all packages and = 41 µm of 50µm pitch for BGA only.
CBVIAT.EN.2	Revised CBVIAT.EN.2 from Mtop-1 to Mtop-1/Mtop (for CL013) and Mtop-2/Mtop-1/Mtop for (CN90).
Staggered	Revised from inner/outer tier of staggered to inner/outer pad. Added rules for pitch staggered (70 µm).
Tri-Tier	Added rules for pitch tri-tier (80 µm).

**T-000-FC-DR-001 (Ver2.0)**

<b>Rule</b>	<b>Revision</b>
BP.EN.3	Revised BP.EN.3 from 2 µm to 12 µm.
UBM.R.2	Revised the wording for UBM.R.2.
UBM.DN.1	Added rule.
UBM.EN.3	Revised UBM.EN.3 from 160 µm (from the center of the scribe lane) to 100 µm (from the chip edge).

**T-000-FC-DR-002 (Ver.1.2)**

<b>Rule</b>	<b>Revision</b>
BP.S.3/BP.S.4	Removed space between two AP (BP.S.3 and BP.S.4).
UBM.DN.1	Added rule.
UBM.EN.3	Revised UBM.EN.3 from 160 µm (from the center of the scribe lane) to 100 µm (from the chip edge).
UBM.R.2	Revised the wording for UBM.R.2.

**T-000-LO-DR-002 (Ver.0.4)**

<b>Rule</b>	<b>Revision</b>
Rule writing style	Revised the rule writing style to refer to the top VIA and the top metal rule of each generation's design rule.
VIAD.R.2 (A1)	Revised VIAD.R.2 (A1) from 400 to 200.

**T-000-FC-DR-003 (Ver0.2)**

<b>Rule</b>	<b>Revision</b>
Application process	Revised the application process from both Cu and Al processes to the Al process only.
CB.S.4	Added rule.

**T-000-LO-DR-005 (Ver.1.0)**

<b>Rule</b>	<b>Revision</b>
BP.R.7	Removed rule BP.R.7.
UBM.EN.1	Revised UBM.EN.1 from 120 µm (space to center of scribe lane) to 100 µm (enclosure by chip edge).

**T-000-FC-DR-004 (Ver.0.1)**

<b>Rule</b>	<b>Revision</b>
BP.R.7	Removed rule BP.R.7.
BP.R.9	Revised BP.R.9 from 170 µm (space to center of scribe lane) to 110 µm (space to chip edge).
UBM.EN.1	Revised UBM.EN.1 from 120 µm (space to center of scribe lane) to 100 µm (enclosure by chip edge).

## A.4.2 Change from Version 1.0 to 1.1

### New

	New rules (Version 1.0 to 1.1)	Description
1	New bump pad pitch rules (150~175μm) for Al and Cu process	Add new rules of UBM, CBD, PM, bump diameter, and bump height for 150 ~ 175μm pitch
2	BP.EN.4 for Al process	Add this rule of "PM enclosure by CBD region"
3	Mechanical and Thermal guidelines for FCBGA	Add new packaging guideline for CL013 and beyond technologies.
4	1.1 OVERVIEW	Add the wordings of " The pad pitch and packaging technology ..."
5	2.2 Flip Chip Guideline	Add " 3. For bump pad pitch selection:..."
6	2.5 Non-shrinkable Guidelines for Shrinkage Technologies	For easier use by the designer who wants to use the TSMC shrinkage technologies
7	PM.W.2	Add this rule for the polyimide window opening on non-CB region
8	4.7 Non-shrinkable Rule For Shrinkable Technologies	For easier use by the designer who wants to use the TSMC shrinkage technologies
9	Add the seal ring cross section on section 4.6.1 and section 4.6.2	Insert the MD/PPI layer into the seal ring cross-section

### Modified

	Modified rules (Version 1.0 to 1.1)	Description
1	UBM.P.1	Modify from 175μm to 150μm
2	CB.W.2	Modify from "width" to "length"
3	BP.W.4	Add "... under UBM area"
4	The bump height and diameter in Table1 & Table2	Simplify the bump height and diameter information
5	BP.EN.2 for Al process	Add the description "without polyimide process only"
6	CB.EN.1	Remark this rule at section 4.4.2.
7	2.3 Redistribution Interconnection Guidelines 4. I/O ESD protection recommendations:	Modify "The minimum bus line width is 20μm." to The minimum total bus line width is 20μm.
8	1.1 OVERVIEW	Modify the wordings of "is only applied..." to "is verified by..."
9	Modify the description using "Mil" unit	Add "μm" in front of "Mil"
10	PM.W.1	Specify this rule using on PM opening on CB region.
11	PPI.S.3	Relax from 30μm to 5μm
12	Modify CB.EN.1 for Cu process	Relax this rule from 2μm to 1.5μm
13	BP.EN.2	Add".... (Without Polyimide process only)"
14	Modify "*" mark for DRC can't check	Change from "#" to "U"

### Deleted

	Deleted rule (Version 1.0 to 1.1)	Description
1	60 μm pitch for single in-line Cu pad	Delete the rules of this pitch due to no impact on TSMC IO library.

## A.4.3 Change from Version 1.1 to 1.2

### New

	New rules (Version 1.1 to 1.2)	Description
1.	Add CLN65 relative wire bond and flip chip design rules	1. Wire bond pad structure need have new rules. 2. Flip chip rules are same with CLN90 low-K
2	#CB.S.3 <sup>t</sup>	Space of the different pad geometries [(Single to Stagger), (Single to Tri-tier) or (Stagger to Tri-tier)]
3	CB.W.1/CB.S.1 for dual passivation	Relax CB.W.1/CB.S.1 to 44/6um(50um pitch) and 49/6um (60um pitch) for dual passivation only
4	60um pitch staggered rule	CB.W.1/CB.W.2/CB.S.1=50/66/10um .CB.W.1/CB.S.1 will be set as non-shrinkable.
5	UBM.S.4®	Recommended maximum space between two UBM
6	UBM.R.5	At least one bump has to be placed near, and as close as possible, to the chip corner.
7	UBM.R.5®	It's recommended not to place the IO bump pads on 2 <sup>nd</sup> and 3 <sup>rd</sup> row on bump array corners, but instead to put Vss, Vdd or dummy bump pads.
8	UBM.EN.1g	Recommended enclosure by chip edge (Maximum)
9	UBM.R.4g	<p>It is recommended not to put any bump on the top of SRAM area and the matching pairs.</p> <p>The circuits should be located at a minimum distance of 60 µm from the bump pad's PM or CBD edge.</p> <p>It's also recommended to consider UBM.S.4® at the same time.</p> <p>If bump over SRAM area is needed, it's recommended to use the ultra-low alpha particle materials during the bump and assembly processes (solder bump, under-fill, pre-solder bump...) to avoid high Soft Error Rate (SER).</p> <p>TSMC uses ultra-low alpha particle materials in the solder bump process.</p> <p>If a customer couldn't meet UBM.S.4® and UBM.R.4g at the same time, you can consult TSMC for layout suggestion.</p>
10	#BP.S.1 <sup>t</sup>	PM space to AP-MD [PM on AP is prohibited, except UBM region and seal ring] (CL013 FSG with AI PPI)
11	BP.EN.8 <sup>t</sup>	PM enclosure by UBM (CL013 FSG with AI PPI)
12	BP.R.1 <sup>t</sup>	CB2 on AP-MD for interconnection is prohibited [except UBM and sealring]
13	CB-VD and AP-MD rules for AI PPI for CL013/CLN90 Cu process flip chip design	
	CB.W.1	Width (maximum =minimum) {Not inside seal ring}
	CB.S.1	Space
	CB.EN.1	Enclosure by MT {Not inside seal ring}
	CB.R.1	A 45-degree rotated CB-VD is prohibited
	AP.W.1	Width {Interconnection only} {Not inside UBM or seal ring}
	AP.S.1	Space
	AP.S.2	Space to FW
	AP.S.3	Space to LMARK
	AP.S.4	Space to CB2/PM
	AP.EN.1	Enclosure of CB-VD {Not inside seal ring}
	AP.DN.1	AP density across full chip
14	Add Sec. 2.1 wire bond guideline item 2	Pad Geometries selection
15	Add Sec. 2.1 wire bond guideline item 3	Pad pitch and size.
16	Add Sec. 2.2 Flip chip guideline item 6	Add new Polyimide guideline

**Modified**

	<b>Modified rules (Version 1.1 to 1.2)</b>	<b>Description</b>
1	#UBM.S.1 <sup>t</sup>	Space to metal fuse protection ring (change from 60 to 50um)
2	UBM.S.3 <sup>t</sup>	Space to L target (for Cu process only) (change from 90 to 80um)
3	Non-shrinkable rule of CB.W.2 of 55um pitch single	Change from 72u.6um to 66um.
4	Non-shrinkable of UBM.S.1	Change from 66 to 55um
5	Non-shrinkable of UBM.S.3	Change form 99 to 88um
6	Sec. 2.2 Flip chip guideline item 7	Modify this process sequence table and add AI PPI(AP-MD)
7	Sec. 2.2 Flip chip guideline item 9	Modify the alpha particle sensitive area and forbidden SRAM area ,except use ultra-low alpha particle material

## A.4.4 Change from Version 1.2 to 1.3

From Version 1.2 to Version 1.3			
Rule	Sec. No.	Section Title	Revision Description
Consolidate C015/C018 (T-000-CL-DR-001) and C013 CUP design rule (T-013-CL-DR-005)	2.1.2	Circuit Under Pad (CUP) Recommendations	Recommendations for CUP
	3.2	Special Recognition CAD Layers	Add WBDMY to cover CUP pad
	4.4	Pad Pitch Rules for Wire Bond	Add CUP relative descriptions in the current rules (CB.W.3/CB.S.2/CB.EN.1)
	4.6.2	Circuit Under Pad (CUP) Pad structure rules (for C015/C018 only)	Merge all rules from T-000-CL-DR-001
	4.7.2	Circuit Under Pad (CUP) Pad structure rules (for C013 only)	Merge all rules from T-013-CL-DR-005
Add RV and AP-MD rule for C013/N90/N65 wire bond application	3.1	Mask Information, Process Sequence and CAD layers	Add the process sequence of AP-MD with dual passivation scheme on C013 and below technologies
	3.2	Special Recognition CAD Layers	Add RV, AP-MD and CB2 for AP RDL application
	4.4	Pad Pitch Rules for Wire Bond	Add AP-MD and CB2 relative descriptions in the current rules (CB.W.1/CB.W.2/CB.W.3/CB.S.1 /CB.S.2/CB.EN.1/CB.R.1)
	4.7	Wire Bond Pad Structure Rules for Cu Process	Add AP-MD and CB2 relative descriptions in the current rules (CB.R.5/CB.R.6/CBVIAx.R.3/ CBVIAx.R.3.1)
	4.8	RV And AP-MD Layout Rules for Wire Bond	Add RV and AP-MD rules for wire bond
	5.2	Polyimide Window (PM) Rules for Flip Chip	Add AP-MD and CB2 relative descriptions in PM.W.2
Item 5: Required bumping testing flow	2.2	Recommendations for Flip Chip Application	Change "Suggested bumping and testing flow... to "Required bumping and testing flow..."
Mask layer, Process Sequence Table	3.1	Mask Information, Process Sequence and CAD layers	Modify the table and separate the tables of "Al process," "C013 single passivation," C013/CN90 dual passivation," and "CN65 dual passivation"
60um pitch staggered pad rules	4.4	Pad Pitch Rules for Wire Bond	CN90/CN65 dual passivation and Al process single passivation share the same rules and separated with C013.
70um and 80um pitch staggered pad rules	4.4	Pad Pitch Rules for Wire Bond	Change to become the recommended rules
PM.R.1/PM.R.2	4.5	Polyimide Window (PM) Rules for Wire Bond	Add "(Al process only)"
CBVIAx.R.1	4.6.1	Wire Bond Pad Structures Rules For Al Process	Modify the description to except the regions of CBVIAx.R.1.1
CBVIAx.R.1.1	4.6.1	Wire Bond Pad Structures Rules For Al Process	Add this new rule for "Ratio of total exposure area of {VIA1~VIAtop-2 INSIDE CB} to CB area (In the inter row pad of staggered and the inter/middle row pad of Tri-tier)"
CBVIAx.R.3	4.7.1	Wire Bond Pad Structures Rules For Al Process	Modify the description to except the regions of CBVIAx.R.3.1
CBVIAx.R.3.1	4.7.1	Wire Bond Pad Structures Rules For Al Process	Add this new rule for "Ratio of total exposure area of {VIA1~VIAtop-2 INSIDE CB} to CB area (In the inter row pad of staggered and the inter/middle row pad of Tri-tier)"
CN90(2XTM)/CN65(2XTM)/CN65(VIAY) rules	4.7.1	Wire Bond Pad Structures Rules For Al Process	Add new rules for CN90(2XTM)/CN65(2XTM)/ CN65 (VIAY) processes
UBM.R.3	5.1	Under Bump Metallurgy (UBM) Rules	Add the required layers for the bump ball structure of different processes
UBM.R.5®	5.1	Under Bump Metallurgy (UBM) Rules	Rename to UBM.R.5g

From Version 1.2 to Version 1.3			
Rule	Sec. No.	Section Title	Revision Description
UBM.R.6®	5.1	Under Bump Metallurgy (UBM) Rules	New guideline for the size ratio of UBM/Pre-Solder Bump SRO (=C/S) and BGA SRO/Board Pad (=T/O) = 1.0~1.1
UBM.EN.1g	5.1	Under Bump Metallurgy (UBM) Rules	Rename to UBM.EN.1®
BP.S.1	5.4	Bump Pad Structure Rules For Cu Process	Deleted this rule and replaced by AP.S.4
BP.EN.7	5.4	Bump Pad Structure Rules For Cu Process	Relax the number from 15um to 2um.
BP.EN.8	5.4	Bump Pad Structure Rules For Cu Process	Deleted this rule due to Single pass+PM scheme is prohibited for AP RDL process
Rename all rules	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Rename CB.W.5/CB.S.3/CB.S.4/CB.EN.3 to RV.W.2/RV.S.1/RV.S.2/RV.EN.2
RV.W.2	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Relax from >=25um to =5um
RV.S.1	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Relax from >=15um to >=3um
RV.S.2	5.5.2.1	RV Layout Rules (Passivation-1 VIA hole)	Relax from >=9um to >=0um
Rename all rules	5.5.3.1	RV Layout Rules (Passivation-1 VIA hole)	Rename CB.W.1/CB.S.1/CB.EN.1/CB.R.1 to RV.W.1/RV.S.1/RV.EN.1/RV.R.1
RV.S.2	5.5.3.1	RV Layout Rules (Passivation-1 VIA hole)	New rule
RV.R.3	5.5.3.1	RV Layout Rules (Passivation-1 VIA hole)	New rule
AP.W.1	5.5.3.2	AP-MD Layout Rules	Add CBD, CB2, and FW(AP) in the rule description
AP.S.2/AP.S.3/AP.S.4	5.5.3.2	AP-MD Layout Rules	Add “ overlapping is prohibited in the rule description
AP.EN.1	5.5.3.2	AP-MD Layout Rules	Modify CB-VD to RV
AP.DN.1	5.5.3.2	AP-MD Layout Rules	Relax the maximum density from 60% to 70%
A.R.10/A.R.11/A.R.12/A.R.13	4.8.3 5.5.3	Layout Rules for RV and AP-MD	Add new rules Cu process.

## A.4.4.1 Rule Number Mapping Table (from Version 1.2 to 1.3):

<b>Consolidate from T-000-CL-DR-001 Ver1.2</b>		
<b>T-000-CL-DR-001</b>	<b>Version1.3</b>	<b>Note</b>
CB.EN.1	CUPCB.EN.1	No rule change
CB.R.3	CUPCB.R.1	No rule change
CBVIAT.EN.2	CUPVIAT.EN.1	No rule change
CBVIAT.W.2	CUPVIAT.W.1	No rule change
CBVIAT.W.3	CUPVIAT.W.2	No rule change
CBVIAT.S.3	CUPVIAT.S.1	No rule change
CBVIAT.S.4	CUPVIAT.S.2	No rule change
CBVIAT.DN.1	CUPVIAT.DN.1	No rule change
CBVIAT.R.2	CUPVIAT.R.1	No rule change
<b>Consolidate from T-013-CL-DR-005 Ver.1.2</b>		
<b>T-013-CL-DR-005</b>	<b>Version1.3</b>	<b>Note</b>
CB.EN.3	CUPCB.EN.2	No rule change
CB.EN.4	CUPCB.EN.3	No rule change
CB.EN.5	CUPCB.EN.4	No rule change
CB.EN.6	CUPCB.EN.5	No rule change
CB.W.5	CUPCB.W.1	Change from =5um to >=5um
CB.R.3 <sup>u</sup>	CUPCB.R.2 <sup>u</sup>	No rule change
CB.R.4	CUPCB.R.3	No rule change
CB.R.5	CUPCB.R.4	No rule change
CB.R.6 <sup>u</sup>	CUPCB.R.5 <sup>u</sup>	Remove the constraint of "It's prohibited to place CUP chip and non-CUP pad in the same chip"
CB.R.7	CUPCB.R.6	No rule change
CBVIAT.W.1	CUPVIAT.W.3	No rule change
CBVIAT.S.1	CUPVIAT.S.3	No rule change
CBVIAT.S.2	CUPVIAT.S.4	No rule change
CBVIAT.S.3	CUPVIAT.S.5	No rule change
CBVIAT.EN.1	CUPVIAT.EN.2	No rule change
CBVIAT.R.1	CUPVIAT.R.2	No rule change
CBVIAT.R.2	-	Remove
<b>Rename the RV rules in section 5.5.2</b>		
<b>Version1.2</b>	<b>Version1.3</b>	<b>Note</b>
CB.W.5**	RV.W.2	Change from 25um to 5um
CB.S.3**	RV.S.1	Change from 15um to 3um
CB.S.4	RV.S.2	Change from 9um to 0um
CB.EN.3	RV.EN.2	
<b>Rename the RV rules in section 5.5.3</b>		
<b>Version1.2</b>	<b>Version1.3</b>	<b>Note</b>
CB.W.1	RV.W.1	No rule change
CB.S.1	RV.S.1	No rule change
-	RV.S.2	New rule
CB.EN.1	RV.EN.1	No rule change
CB.R.1	RV.R.1	No rule change
-	RV.R.3	New rule

## A.4.5 Change from Version 1.3 to 1.4

From Version 1.3 to Version 1.4			
Rule	Sec. No.	Section Title	Revision Description
Consolidate N90/N65 CUP design rule (T-N90-CL-DR-009)	2.4	Special Recognition CAD Layers	Add WBDMY to cover CUP pad
	3.3.3	Pad Pitch Rules for Wire Bond	Add CUP relative descriptions in the current rules (CB.W.3/CB.S.2/CB.EN.1)
	3.3.4.2.2	Circuit Under Pad (CUP) Pad structure rules (for N65/N90)	Merge all rules from T-N90-CL-DR-009
A.R.10/A.R.11/A.R.12	3.3.7.3	Antenna Effect Prevention (A) Layout Rules for RV and AP-MD	Change antenna rules with core and I/O devices and modify the A.R.12 parameter numbers
UBM.EN.1	4.2	Under Bump Metallurgy (UBM) Rules	Change rule number from 100um to 80um.
UBM.EN.1®	4.2	Under Bump Metallurgy (UBM) Rules	New rule for placing UBM uniform.
UBM.EN.2	4.2	Under Bump Metallurgy (UBM) Rules	New rule for placing UBM uniform.
UBM.EN.3	4.2	Under Bump Metallurgy (UBM) Rules	New rule for preventing iso bump.
UBM.EN.3®	4.2	Under Bump Metallurgy (UBM) Rules	New rule for preventing iso bump.
UBM.R.6® <sup>u</sup>	4.2	Under Bump Metallurgy (UBM) Rules	Change rule number from 1.0~1.1 to 0.95~1.05
UBM.EN.2	4.3.5	Flip Chip non-shrinkable Rules for the Half Node Technologies	Change rule number from 2.3 to 2.2
BP.EN.5	4.3.5	Flip Chip non-shrinkable Rules for the Half Node Technologies	Change rule number from 11.2 to 11

### A.4.5.1 Rule Number Mapping Table (from Version 1.3 to 1.4):

Consolidate from T-N90-CL-DR-009 Ver.1.2		
T-N90-CL-DR-009	Version1.4	Note
CB.EN.3	CUPCB.EN.6	No rule change
CB.EN.4	CUPCB.EN.7	No rule change
CB.R.3 <sup>u</sup>	CUPCB.EN.7 <sup>u</sup>	No rule change
CB.R.6 <sup>u</sup>	CUPCB.EN.8 <sup>u</sup>	No rule change
CB.R.7	CUPCB.R.7	No rule change
CBVIAT.W.1	CUPVIAT.W.1	No rule change
CBVIAT.S.1	CUPVIAT.S.1	No rule change
CBVIAT.EN.1	CUPVIAT.EN.1	No rule change
CBVIAT.DN.1	CUPVIAT.DN.1	No rule change
CBVIAT.DN.2	CUPVIAT.DN.2	No rule change

## A.5 Revision History of T-N85-CL-DR-001 (N85)

### A.5.1 From Version 0.1 to Version 0.2

From Version 0.1 to Version 0.2			
Rule	Sec. No.	Section Title	Revision Description
1.		Title	Add MS
2.	1.1	Overview	<ul style="list-style-type: none"> <li>1. Add 1.8V, 2.5V, 1.8V/3.3V IO device for CLN85G</li> <li>2. Add 2.5V IO device for CLN85LP</li> <li>3. Add CMN85 process</li> </ul>
3.	1.3.2	SRAM Design Specifications	Add the table for N85 SRAM cells in different process
4.	2.1	Devices	Update the table for Available Vt/ MOM/ MIM/ Inductor in each technology
5.	2.2	Power Supply and Operation Temperature Ranges	<ul style="list-style-type: none"> <li>1. Add 1.8V, 2.5V, 1.8V/3.3V IO device for CLN85G</li> <li>2. Add 2.5V IO device for CLN85LP</li> <li>3. Add CMN85 process</li> </ul>
6.	2.3	Metalization Options	Add My, UTM, MiM
7.	2.4	Mask Information, Key Process Sequence, and CAD Layers	Add this section
8.	2.5	Device Truth Tables	Add this section
9.	2.6	Mask Requirement for Device options (High/STD/Low VT)	Add this section
10.	3.3	Ultra Low Vt NMOS (ULVT_N) Layout Rules (Mask ID: 11R)	Add this section
11.	3.4	Ultra Low Vt PMOS (ULVT_P) Layout Rules (Mask ID: 11Q)	Add this section

## A.6 Revision History of T-N90-CL-DR-017 (N90 ULVt)

### A.6.1 From Version 0.1 to Version 1.0

From Version 0.1 to Version 1.0			
Rule	Sec. No.	Section Title	Revision Description
		Title	Remove N85.
	1.2	Reference Documentation	Add this section
	1.3	Mask Information, Key Process Sequence, and CAD Layers	Add this section
	1.4	Device Truth Tables	Add this section
	1.5	Mask Requirement for Device options (High/STD/Low VT)	Add this section

## A.6.2 From Version 0.2 to Version 1.0

From Version 0.1 to Version 0.2			
Rule	Sec. No.	Section Title	Revision Description
1.	1.2	Related Design Rule Manuals And Documents	Update reference documents summary table 1.2.1
2.	1.1	Overview	Delete the CMN85G offering for 1.8V IO device and triple-gate oxide process.
3.	2.1	Devices	Delete the Ultra low Vt device for CMN85LP
4.	2.2	Power Supply and Operation Temperature Ranges	Delete the 1.8V and 1.8V/ 3.3V IO devices for CMN85LP
5.	3.3	Ultra Low Vt NMOS (ULVT_N) Layout Rules (Mask ID: 11R)	Change "N85LP" to "CLN85LP"
6.	3.4	Ultra Low Vt PMOS (ULVT_P) Layout Rules (Mask ID: 11Q)	Change "N85LP" to "CLN85LP"
7.	4.1.3	Dummy Insertion	Add this section
8.	4.3	Legacy IP porting	Add this section
9.	4.4.5	Dummy Insertion	Add this section
10.	Chapter 5	Reliability Rules and Models	Add this chapter