

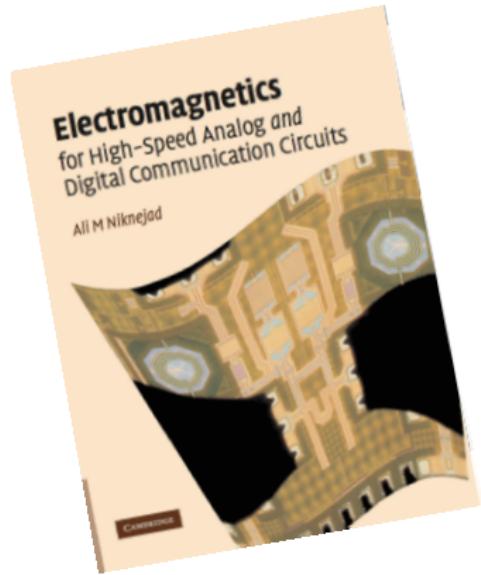
Passive Devices for Communication Integrated Circuits

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Outline

- Part I: Motivation
- Part II: Inductors
- Part III: Transformers
- Part IV: E/M Coupling
- Part V: mm-Wave Passives (if time permits)



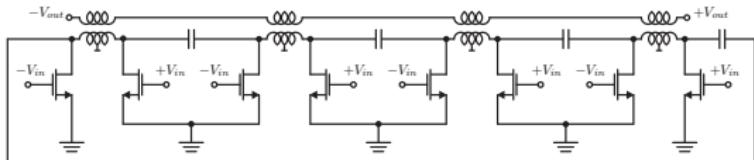
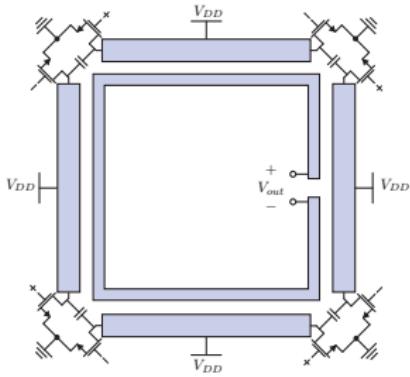
Motivation

- Why am [are] I [you] here?

Passive Devices

- Equally important as active devices at RF/microwave frequencies
- Quality factor of resonators determines phase noise (key spec for high data rate communication)
- Transistor requires matching in order to obtain
 - Maximum gain
 - Low noise
 - High power
- Lack of “ground plane” in CMOS requires careful design of return paths and AC bypass capacitors

Innovations in IC's



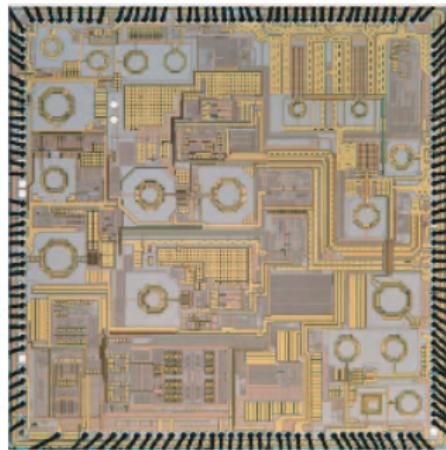
- Some of the best ideas in the past 10 years have come from custom passive devices which were not in the "library"
 - Examples: DAT, tapered resonator, artificial dielectric transmission lines (slow wave and meta-material structures)
Ref: [Aoki]

Why should “designers” be involved?

- They know their circuits best and can make the best decisions. There are many solutions to a give problem with competing trade-offs. Without knowing the trade-offs, it's hard to make a decision in a vacuum.
 - The designer should be aware of the layout of the passive elements to be sure that “what you see is what you get”.
 - The routing and area constraints in a design may favor one topology over another
- Library is often limited to a small discrete set of structures
 - Many new innovations come from structures not in the library

Other Good Reasons...

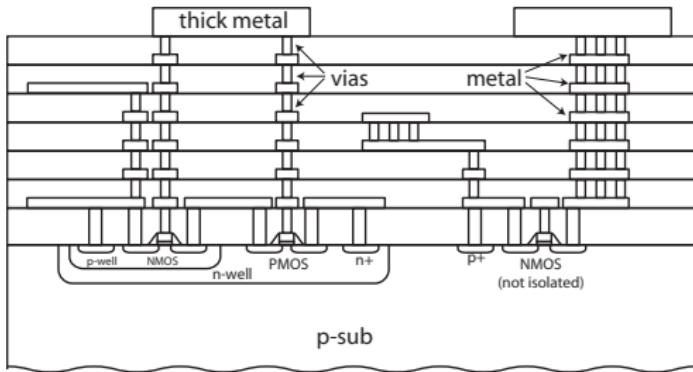
- In the era of highly integrated transceivers, coupling is a huge issue and good layout and planning can help a great deal
 - Where to put grounds, bypass, differential signals, shielding, transmission lines, passive device orientation, substrate taps, wells, etc.
- Faster design cycle (can quickly estimate the impact of a layout choice on the circuit performance)
- Role of modeling engineer:
Validate design, provide technology files, provide framework, and help with especially difficult and challenging cases



Typical RF Library

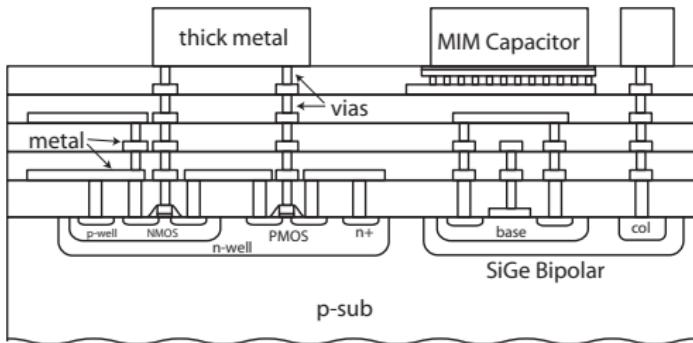
- Building blocks:
 - Lumped inductors
 - Transformers
 - Coupling capacitors
 - Transmission lines ($> 10\text{GHz}$)
 - CMOS Transistor (MOS varactor)
- Issues:
 - Layout (fill, slotting)
 - Modeling (broadband models for SPICE)
 - Measurements (esp high Q structures, sensitive to contact resistance)

Typical CMOS IC Process



- For passive devices, the most important things are (in order of importance):
 - Metal conductivity, distance to substrate, substrate conductivity
 - Other important considerations include a triple-well (or deep nwell) for isolation
- Top one or two layers are usually thicker

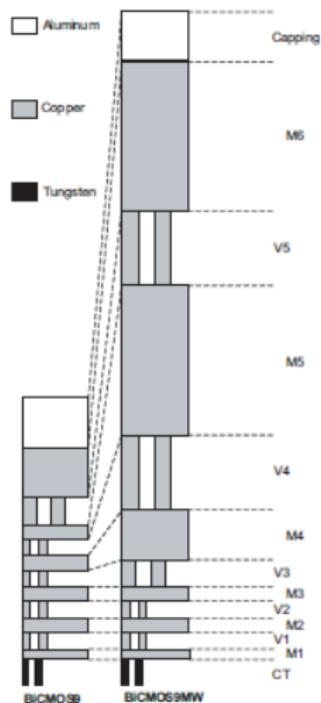
Typical SiGe Process



- SiGe processes are optimized for RF applications and as such they usually offer many “goodies” when it comes to passives
- There are usually 1-2 very thick metal layers ($> 3\mu\text{m}$)
- The distance to substrate for these layers is also much larger than CMOS, as high as $12\mu\text{m}$
- MIM capacitors are also usually included.

Technology Stack-Up (Back-End)

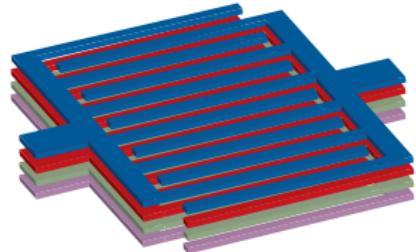
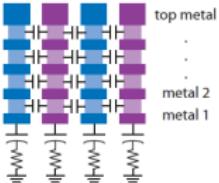
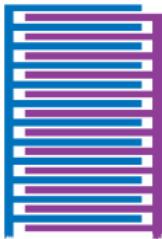
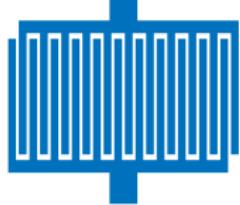
- Modern CMOS (< 90nm) processes have nine or more metal layers
 - The switch to copper was a boon to passive devices. Not only is it less resistive, but it also can handle much higher currents.
 - Unfortunately, more metals usually means thinner metals and dielectrics
 - Ultra-thick layers are available as an option
 - Re-distribution layers (RDL) or Al capping layers is now commonly available, but the current density in these lines is much lower
- Dielectrics are now very complicated, with a complex stack-up of low-K and high-K materials. This makes simulation more complicated,



Substrate Conductivity

- Substrate conductivity is very important if it's above a certain threshold.
- Current injected into the substrate through displacement current can be shielded or controlled through careful placement of substrate taps.
- Current induced magnetically, eddy currents, are (nearly) impossible to shield for an inductor and can cause substantial loss if the substrate is conductive
- Today most technologies use a relatively resistive substrate (10 ohm-cm), and eddy currents are not much of a concern
- Many processes cover the surface with n-well or p-well automatically. Therefore it's very important to use a "well block" layer underneath the inductors to prevent highly conductive layers from underneath the structure.

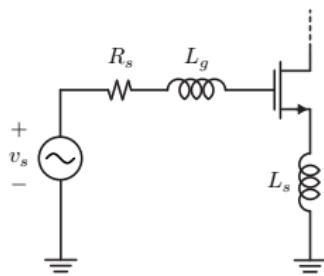
Scaling Helps and Hurts



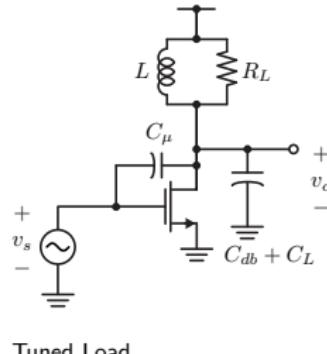
- Can build very high density caps
- Cu and thick metal stacks were very exciting (130nm, 90nm)
- Metals are getting thinner (low K)
- Inductors and T-lines are getting worse

Inductors

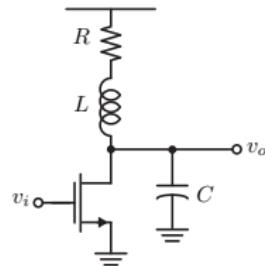
Common Applications for Inductors



Impedance Matching



Tuned Load

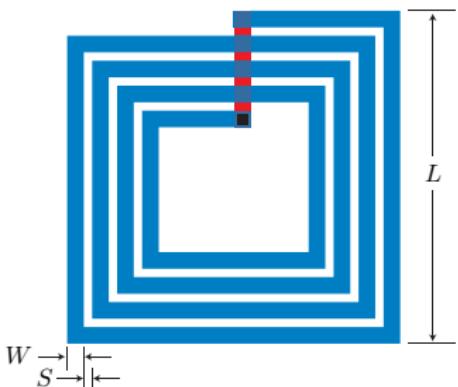


Shunt-Peaking Load

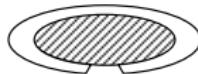
- Tune out capacitance (form resonant tank)
 - Higher frequency of operation – not bandwidth
 - Lower drive power by Q of network
 - Provide filtering
- Matching networks (almost the same thing)
 - Provide higher power, higher efficiency, higher power gain, or lower noise figure

Inductor Performance Metrics

- Spiral geometry defined by
 - Outer length / width (L)
 - Conductor width (W)
 - Conductor spacing (S)
 - Number of turns (N)
- For a given area (A) and metal/oxide/substrate layers, we wish to select the best (or desired)
 - Quality factor (Q)
 - Inductance (L)
 - $Q \cdot L$ product
 - Self-Resonance Frequency (SRF)
 - Parasitic Capacitance (C_{sub} , C_{ox} , C_c)



Inductance



external flux Ψ_{ext}



internal flux Ψ_{int}



total flux $\Psi = \Psi_{int} + \Psi_{ext}$

$$L_{DC} = \frac{\Psi_{ext} + \Psi_{int}}{I}$$

$$L_{\infty} = \frac{\Psi_{ext}}{I}$$

- Why does it vary with frequency?
- First of all, the variation is typically small (< 10%). The reason is that most of the flux is actually outside of the conductors.
- At high frequency, due to skin effect, the fields in the conductors are cancelled and so the inductance decreases.
- Much higher variation in effective inductance is due to capacitance and mutual coupling to other structures (eddy currents)

Quality Factor Definition

$$P = \frac{1}{2} \oint_S \mathbf{E} \times \mathbf{H}^* \cdot d\mathbf{s} = P_I + 2j\omega(W_m - W_e)$$

$$Q = \frac{W_{stored}}{W_{loss}} = \frac{W_{stored}}{W_{loss,1} + W_{loss,2} + \dots}$$

$$\frac{1}{Q} = \frac{W_{loss,1} + W_{loss,2} + \dots}{W_{stored}} = \frac{1}{Q_1} + \frac{1}{Q_2} + \dots$$

$$Q = 2\pi \frac{|W_m| + |W_e|}{P_\ell \times T} = \omega \frac{|W_m| + |W_e|}{P_\ell}$$

$$Q = \omega \frac{|W_m| + |W_e|}{P_\ell} = \omega \frac{W_m^{peak}}{P_\ell} = \omega \frac{W_e^{peak}}{P_\ell} = \frac{\omega L}{R} = \frac{1}{\omega CR} = \frac{X}{R}$$

- Be careful if you're defining Q based on net energy stored (inductive – capacitive) versus total energy stored.
- In resonance, by definition, the net energy is half inductive and half capacitive and the sum is equal to the peak of each
- For a simple RLC tank, the result is the familiar result

LC Matching Network Loss

- The power loss of integrated matching networks is important.
- The insertion loss can be derived by making some simple approximations
- The final result implies that we should minimize our circuit Q factor and maximize the component Q_c

$$IL = \frac{1}{1 + \frac{Q}{Q_c}}$$

$$P_{in} = P_L + P_{diss}$$

$$IL = \frac{P_L}{P_{in}} = \frac{P_L}{P_L + P_{diss}} = \frac{1}{1 + \frac{P_{diss}}{P_L}}$$

$$W_m = \frac{1}{4} L i_s^2 = \frac{1}{4} \frac{v_s^2}{4R_S^2} L$$

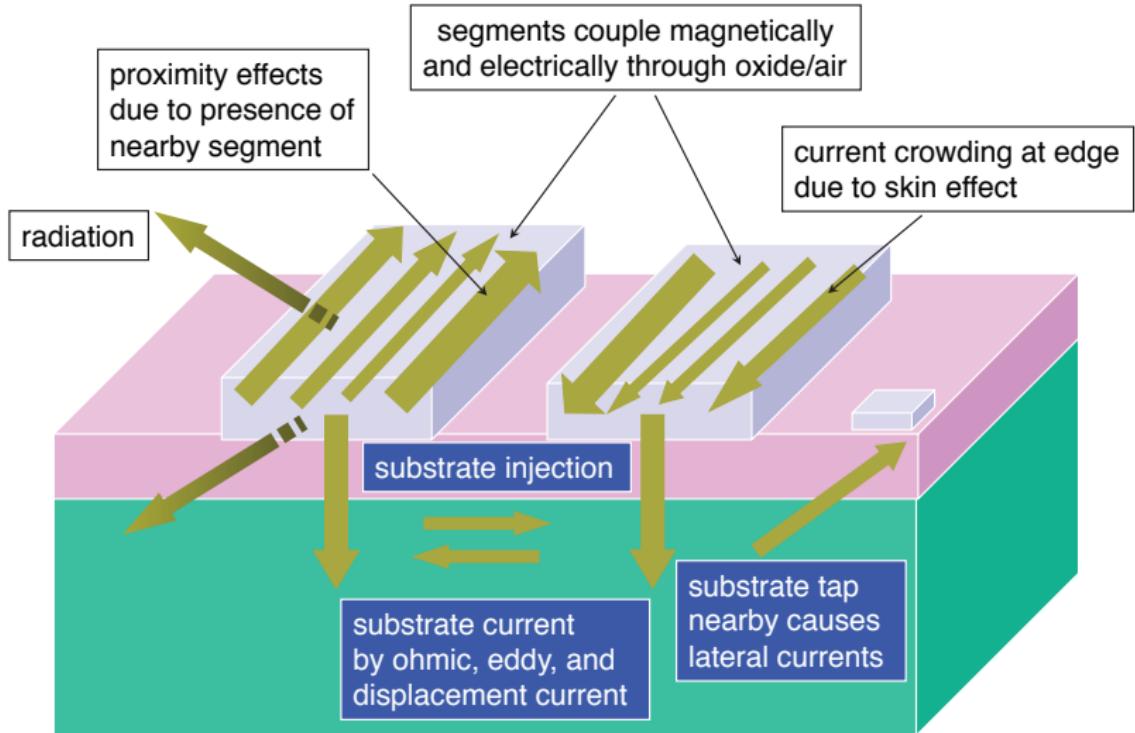
$$\omega_0 \times W_m = \frac{1}{4} \frac{v_s^2}{4R_S} \frac{\omega_0 L}{R_S} = \frac{1}{2} \frac{v_s^2}{8R_S} Q = \frac{1}{2} P_L \times$$

$$P_L = \frac{v_s^2}{2R_S} = \frac{v_s^2}{4 \cdot 2 \cdot R_S} = \frac{v_s^2}{8R_S}$$

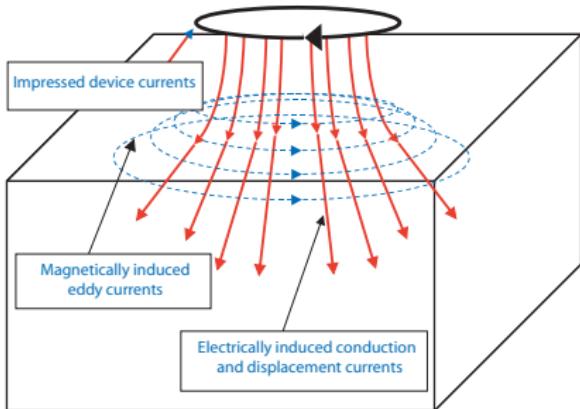
$$\omega_0 (W_m + W_e) = Q \times P_L$$

$$P_{diss} = \frac{P_L \cdot Q}{Q_c}$$

Overview of Loss Mechanisms

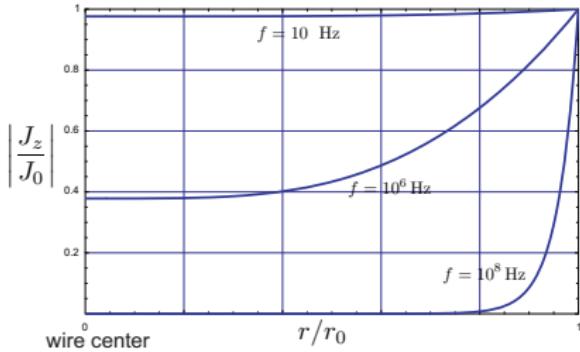
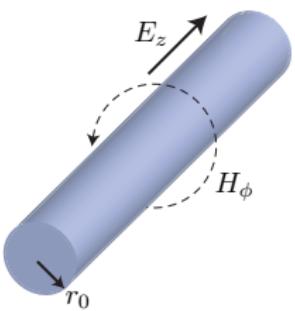


Substrate Loss Mechanisms



- Electrically induced currents flow if the potential in the loop (or spiral) is higher than the substrate. This current flows to ground through the substrate and is a major loss mechanism.
- When a current flows through a loop (or spiral), magnetic fields that penetrate the substrate induce eddy currents which flow in the opposite direction (Lenz' Law). If the substrate is sufficiently resistive ($\sim\text{ohm}\cdot\text{cm}$), this form of loss is small

Metal Conductive Losses



- At low frequencies, the current is uniform and DC loss dominates
- Even at moderately high frequencies ($\sim \text{GHz}$), the skin depth becomes comparable to wire cross-sectional dimensions and non-uniform current flows

Skin Depth of Common Materials

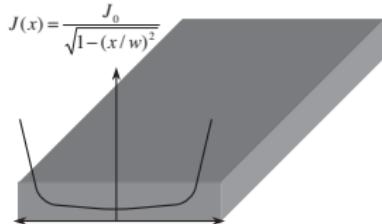
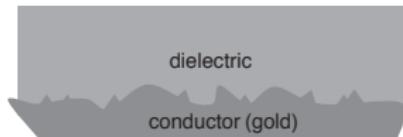
Material	Conductivity (S/m)	Skin Depth (μ)		
		100 MHz	1 GHz	10 GHz
Copper	5.80×10^7	6.6	2.1	0.66
Aluminum	3.72×10^7	8.2	2.6	0.82
Gold	4.44×10^7	7.6	2.4	0.76
Silver	6.17×10^7	6.4	2.0	0.64
Brass	1.57×10^7	12.7	4.0	1.27

- Microwave designers sometimes make a surface impedance approximation and turn conductors into sheets
- Clearly this is not valid for a typical CMOS process since the width and thickness is on the order of the skin depth
- It's important to realize that the skin-effect occurs around the periphery of the wire with concentration at the edges.
- The round wire can be solved analytically but the rectangular wire requires approximations.

Resistance of a Rectangular Wire

- In rectangular conductors, current flows near the outer edges. The exact current distribution is difficult to obtain in closed form.
- Due to surface roughness, the AC resistance is higher than expected. Current flows near surface and the travel distance is increased. There are empirical equations for the AC resistance due to surface roughness (need RMS value of roughness)

$$R' = R(1 + K)$$
$$K = \left(1 - 1.33e^{\frac{-r}{.8\delta}} + 0.33e^{\frac{-r}{.2\delta}} \right)$$

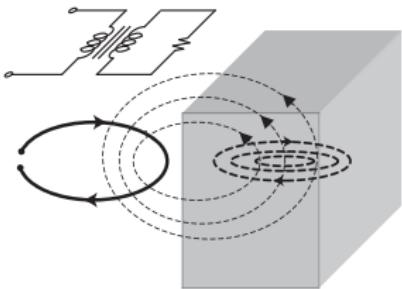
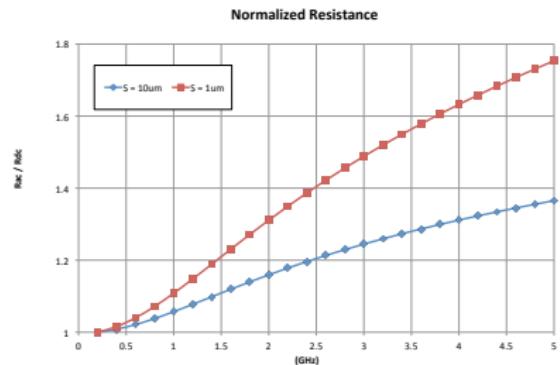
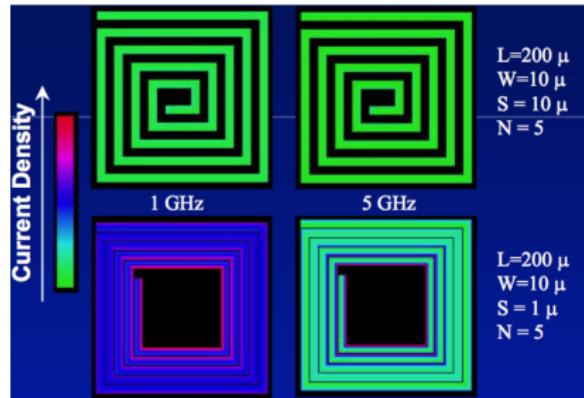


$$R = \frac{I}{\sigma wt} \left[\frac{0.43093x_w}{1 + 0.041 \left(\frac{w}{t} \right)^{1.19}} + \frac{1.1147 + 1.2868x_w}{1.2296 + 1.287x_w^3} + 0.0035 \left(\frac{w}{t} - 1 \right)^{1.8} \right]$$

where $x_w = \sqrt{2f\sigma\mu wt} \geq 2.5$ and for $x_w < 2.5$

$$R = \frac{I}{\sigma wt} \left[1 + 0.0122x_w^{3+0.01x_w^2} \right]$$

Skin-Effect and Proximity Effect



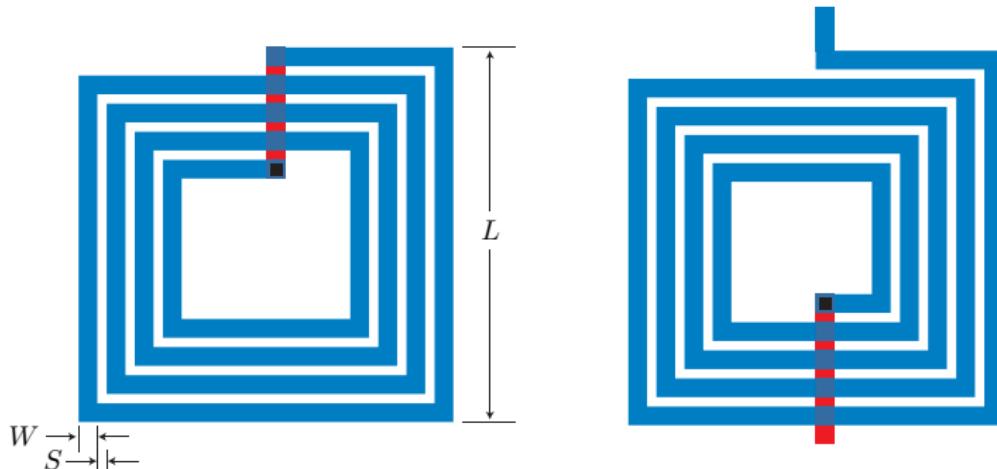
- Any conductor in proximity to the current will experience eddy currents. This is the case for the substrate but also for adjacent metal layers.
- This is why currents flow on the edges nearest each other.

Note: Wires carrying DC currents repel each other! Why do the currents "attract" each other here?

Inductor Layout Choices

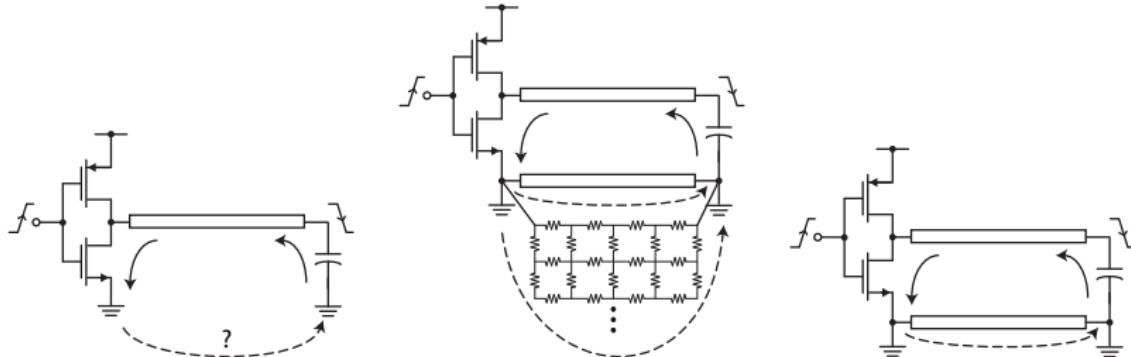
- A designer faces a myriad of questions when choosing an inductor topology:
 - Two-port or one-port ?
 - Symmetry needed?
 - Mirror or translational?
 - Center tap?
 - Shielding?
 - Rectangular or square?
 - Spirals? Concentric rings? Square spiral? Circular?
 - Multi-layer choices:
 - Shunt or Series Connection?
 - Tapering?

Two-Port versus One-Port



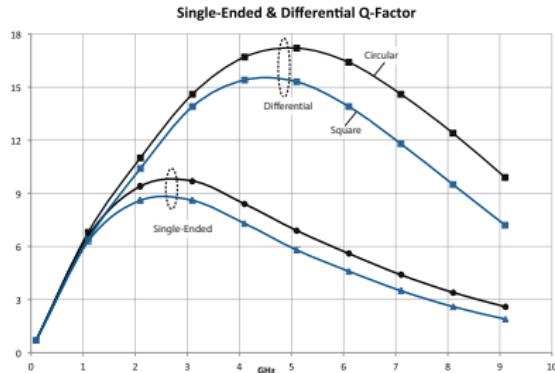
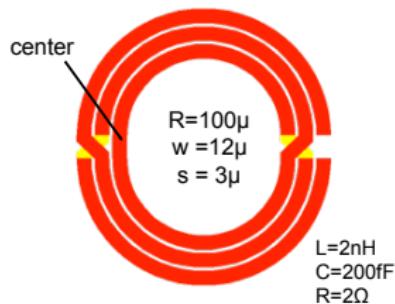
- The circuit layout has a big impact on the choice of a one-port or two-port inductor.
- In a one-port inductor, the loop is closed and well defined and so is the inductance. Both leads come to a common point (for instance to the gate-source of a transistor to tune out its cap)
- A two-port inductor is more dangerous because it's only a partial inductance. The return current is yet to be defined !

Return Currents



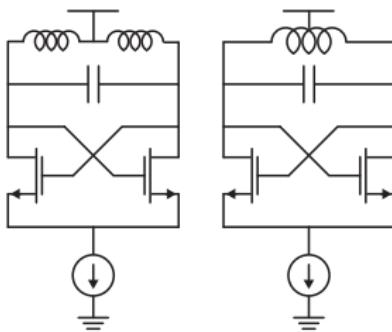
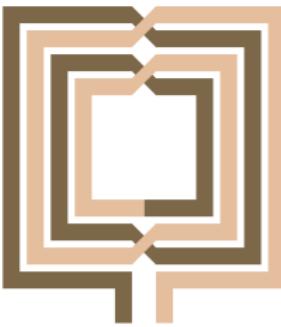
- Inductance is defined for a closed loop. The statement “the inductance of a wire” is meaningless unless one is speaking of *partial* inductance.
- In the above example, how much inductance does the wire have?
 - It depends on where the ground *return current* flows.
 - If it flows in a well defined metal ground, it can be computed accurately. But if there are substrate taps nearby, it can also partially flow through the substrate !
 - The partial inductance assumes return currents at infinity (or far enough)

Differential versus Single-Ended



- An inductor can be driven single-ended (ground one end) or differentially. The performance is markedly different for a differential mode excitation, especially if substrate loss dominates
- Note that if we ground one side, we see roughly L and C . If we drive it differentially, we see L and $C/2$ as the ground capacitors appear in series.
- From a T-line perspective, the SRF is $\lambda/4$ for a shorted line and $\lambda/2$ for an open line. The SRF is doubled!

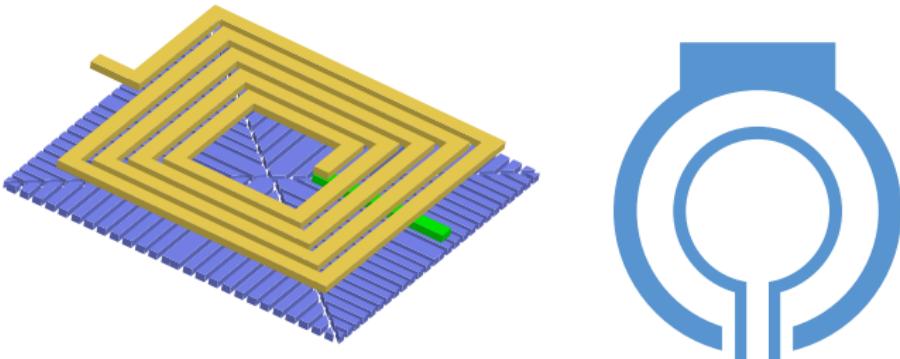
Symmetric Spirals



$$L = 2(L+M) = 2L(1+k) \quad L = 2(L + M) \approx 2L$$

- In a fully differential circuit, we would like to keep things as symmetric as possible to reject common mode noise.
- We can employ two separate inductors or we can use a center tapped inductor. Note that the center tapped inductor has a symmetric point that can be grounded (or biased) and it will occupy less area.
- Area savings occur due to the mutual inductance

Shielding



- Shielding was popularized by T. Lee and P. Yue as a means of improving the Q factor [Yue].
- The shield is patterned to avoid eddy currents and it's constructed in the lowest metal or poly.
- IBM researchers have proposed a "halo" shield which gives nearly the same benefits without hurting the SRF. [Bur]
- Note that we are shielding electric fields, not magnetic fields.
- A solid shield would actually shield the magnetic fields, but the inductance of the structure would also disappear!

Shielding Math

$$R_{low} \approx R_{sub}$$

$$C_{low} \approx Q_c^2 C_s$$

Low Q_c case, no shield is necessary if parallel resistance is larger than tank resistance. Substrate capacitance very small.

$$R_p = (1 + Q_c^2) R_{sub}$$

$$C_p = \frac{Q_c^2}{1 + Q_c^2} C_s$$

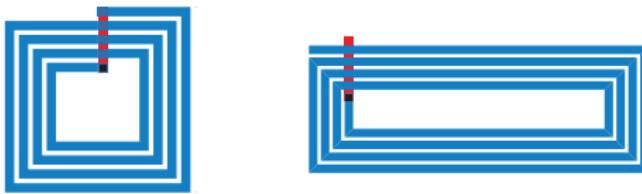
$$R_{hi} \approx Q_c^2 R_{sub}$$

$$C_{hi} \approx C_s$$

Shielding helps if capacitor Q is boosted enough to increase shunt resistance above tank resistance. But SRF is lowered.

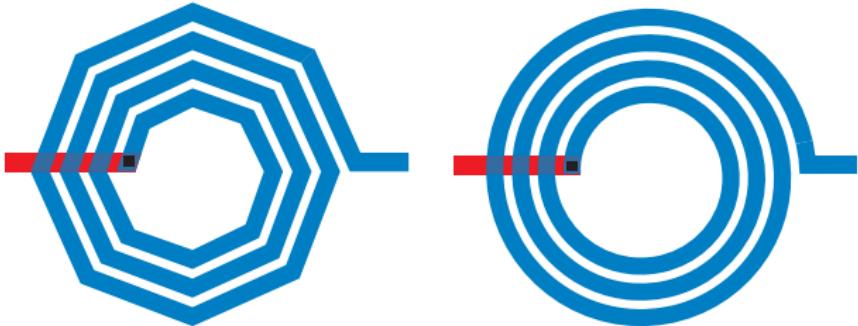
- Shielding changes the value of R in series of C . This helps because it moves one away from the optimal value of R , which by the maximum power transfer theorem is equal to the reactance of C .
- With a shield one moves away from the “optimally bad” value to a much lower value. Unfortunately this also lowers the SRF .
- Often if the substrate taps are placed correctly, a sufficiently large value of R can be obtained with the same benefits and much higher SRF .

Rectangular versus Square



- Square is the optimal layout for quality factor.
- To see this, consider the positive mutual coupling and negative mutual coupling that occurs in a spiral.
- In a square, each half sees the same balanced $+/-$ coupling, whereas in a rectangle, the longer half contributes much less inductance due to flux cancellation.

Circle versus Square



- Circles are better than squares since for a given area (inductance) they have a smaller periphery (resistance).
- A polygon with more than eight sides does a good job in approximating the circular spiral performance.
- The difference in Q is small, $\sim 10\%$.
- The difference is quite small, and in practice a square inductor utilizes the area better (higher inductance), and fits into the layout more easily.

Multi-Layer Shunt

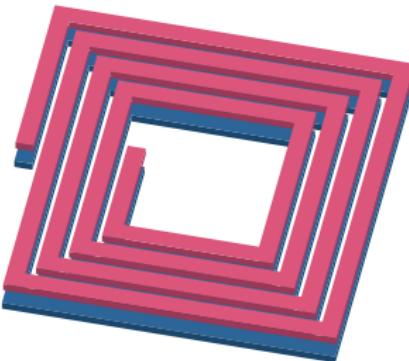
$$V = (I_1 s L_1 + I_2 s M)$$

$$V = (I_2 s L_2 + I_1 s M)$$

$$I = I_1 + I_2$$

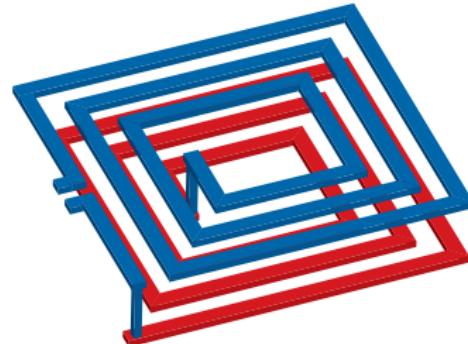
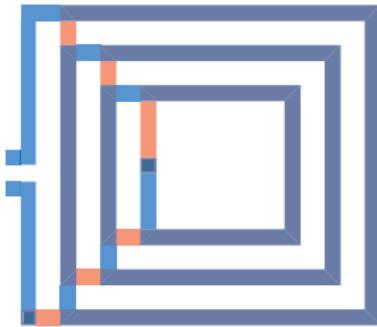
$$L = \frac{L_1 L_2 - M^2}{L_1 + L_2 - 2M}$$

$$L = \frac{L(1 - k^2)}{2(1 - k)} = \frac{L}{2}(1 + k)$$



- Add layers in parallel to lower the conductive losses.
- This is effective at lower frequencies where loss is dominated by conductive (not substrate) losses.
- Notice that the inductance of the structure remains roughly the same (due to mutual coupling $k \sim 0.7 - 0.8$) whereas the resistance drops.

Multi-Layer Series

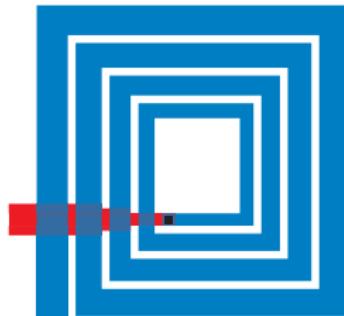


$$L = L_1 + L_2 + M_{12} + M_{21} = 2L + 2M \approx 4L$$

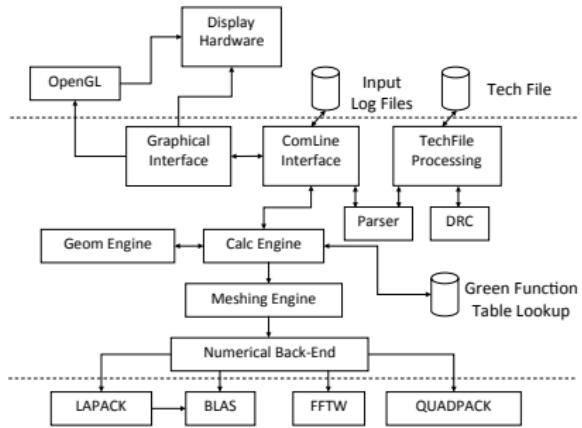
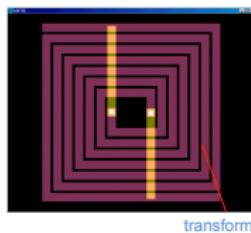
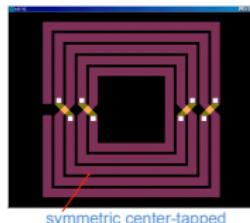
- When many metal layers are available, inductors can be stacked on top of each other oriented properly so that the flux adds.
- The inductance boost can be quite high and approach N^2 increase with number of turns (assuming $k \sim 1$).
- The downside is that lower metal layers usually have higher resistance, they are closer to the substrate, and that interwinding capacitance is a large factor. *SRF* is lowered considerably.

Tapering

- In a spiral structure, the outer turns contribute the most inductance (largest area) and suffer the least from proximity effects.
- The inner turns, though, contribute less inductance and also have very high eddy currents due to the build-up of the magnetic fields.
 - Researchers propose “hollow” inductors for this reason to eliminate the extra loss (current constriction in inner turns).
 - Alternatively, the metal width of inner turns can be reduced substantially since the current is already flowing in a small fraction of width.
 - If the structure is dominated by conductive losses, this helps ~20%.



Simulation of Inductors: ASITIC



- Solve inductance and capacitance problem separately using quasi-static assumptions.
- Assumes currents in segments non-uniform but flowing in direction of segment.
- Substrate is handled through Green functions (no need to mesh substrate).
- Very fast simulation times (seconds to minutes). Uses fast matrix and FFT engines

ASITIC Library Generation

- ASITIC can be used to generate a library of inductors
- Output can be imported into spreadsheet for selection

```
ASITIC> sweep
Sweep filename? sq_sweep1.txt ← Filename for output
Spiral Name? a
Enter electrical constraints:
Frequency? (GHz) 2.4 ← Operating Frequency
Desired range of inductance(nH) (e.g. 2 2.5):1 10 ← Desired inductance
Minimum desired Q (e.g. 5):4 ← range and Q
Enter geometric constraints:
Min/Inc/Max Length or Radius (e.g. 50 10 100)? 125 25 250 ← Geometric constraints
Min/Inc/Max Spacing? (e.g. .5 .5 5) 1 1 1
Metal layer? mtop
Metal layer? mt
Exit metal layer? ml
Number of sides (e.g. 4 for square, or > 4 for polygon spirals)? 4
maxL = 3125.00, maxT = 1.16, maxW = 1.16 (lambda = 62500.00, delta
= 1.45)
1: L = 125.000000, W = 10.000000, S = 1.000000, N = 1.000000
Warning: Could not open data file at frequency = 2.40. Tried
using . as path.
Computing FFTs...
46: L = 125.000000, W = 15.000000, S = 1.000000, N = 3.750000
```

On a modern workstation, this took three minutes to run (642 spirals simulated)

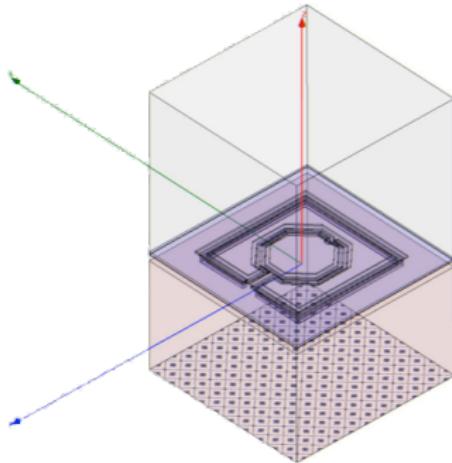
Example Results from Library

Length	W	S	N	L (nH)	R	Q1
225	13	1	3.25	3.34	2.56	15.1
225	10	1	3.00	3.40	2.59	15.2
175	10	1	4.50	3.43	3.67	11.5
225	15	1	4.00	3.44	3.41	12.1
200	13	1	4.25	3.46	3.53	11.9
200	10	1	3.50	3.46	2.81	14.3
175	10	1	4.75	3.55	3.96	11.1

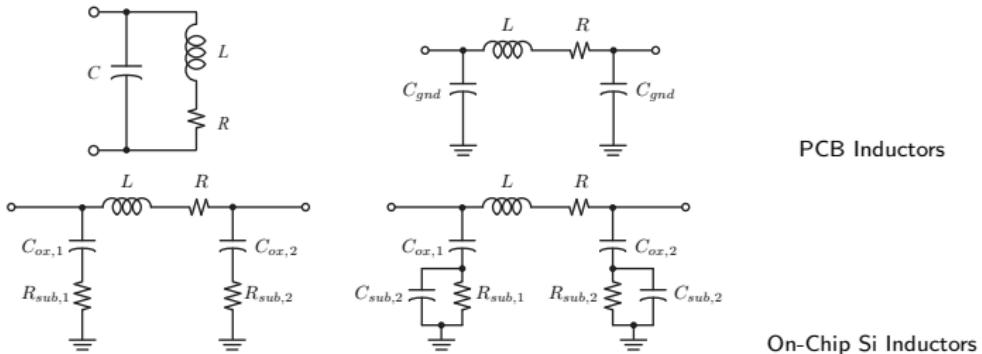
- In this case we sorted the output by the inductance value and then by the quality factor.
- As you can see, for a 3-4 nH inductor, you can realize $Q \sim [11, 15]$, mostly by trading off area
- In certain applications, you would prefer different number of turns (1-port versus 2-port). A 2-port inductor has to make half turns $N = x.5$.

Simulation of Inductors: HFSS

- HFSS is a finite element solver and it has to mesh the entire problem space. This means that simulations run much slower than a method of moment solver
- Convergence criteria should be selected carefully.
- Port definitions very confusing and ultimately pose some problems.
Grounding is related to the ports since the substrate is not a good ground plane.
(we'll come back to this point)

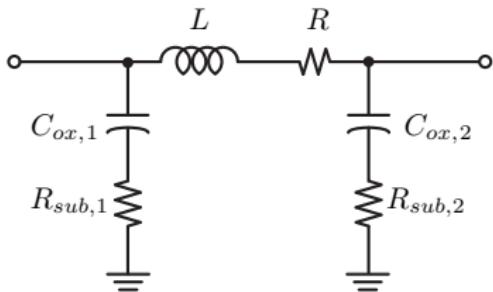


Simple Inductor Modeling



- In certain situations (AC analysis), the scattering parameters from EM simulation or measurements can be used directly
- It's much more convenient (and insightful) if an equivalent circuit model is available.
- For an air core inductor, you just need LCR to capture first resonance. The same is true for inductors on a low loss PCB.
- The key difference for on-chip spirals is to include the electrically induced substrate losses.

The π -Model



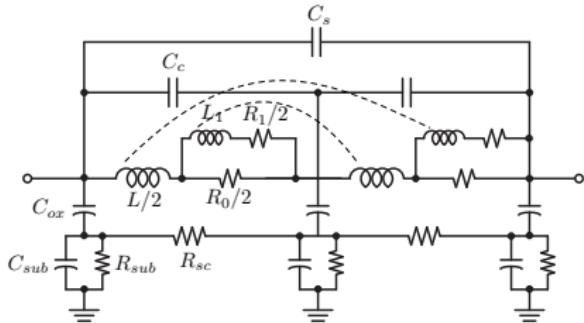
$$R + j\omega L = \frac{-1}{Y_{12}}$$

$$(R + j\omega L) \parallel \left(R_{s,1} + \frac{1}{j\omega C_{s,1}} \right) = Y_{11}$$

$$(R + j\omega L) \parallel \left(R_{s,2} + \frac{1}{j\omega C_{s,2}} \right) = Y_{22}$$

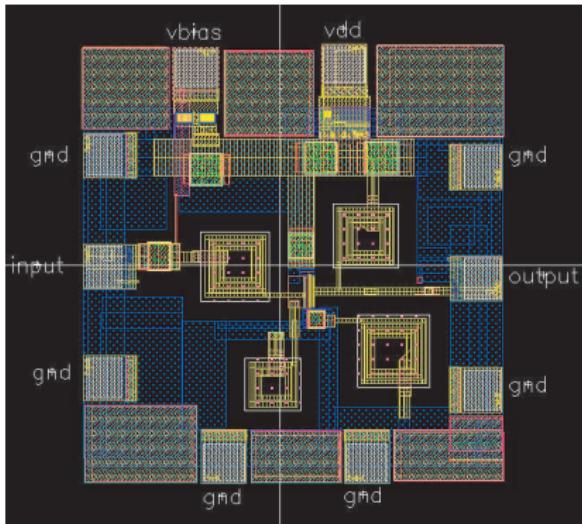
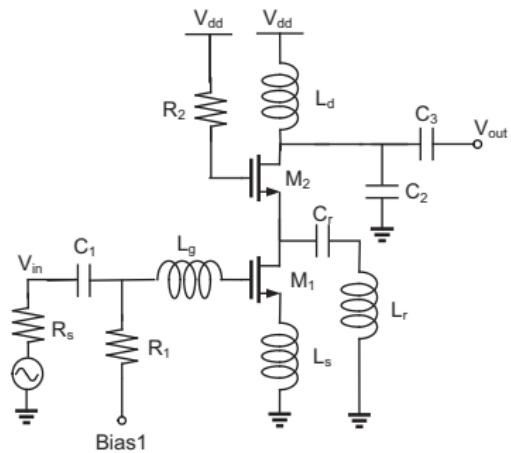
- The two-port parameters of a structure have a one-to-one correspondence with the π equivalent circuit model (at only one frequency)
- The nominal values of L , R , and C can be quickly calculated and used in a narrowband design.
- This is a useful “sanity check” to ensure that the two-port data actually represents an inductor.

Complex Models



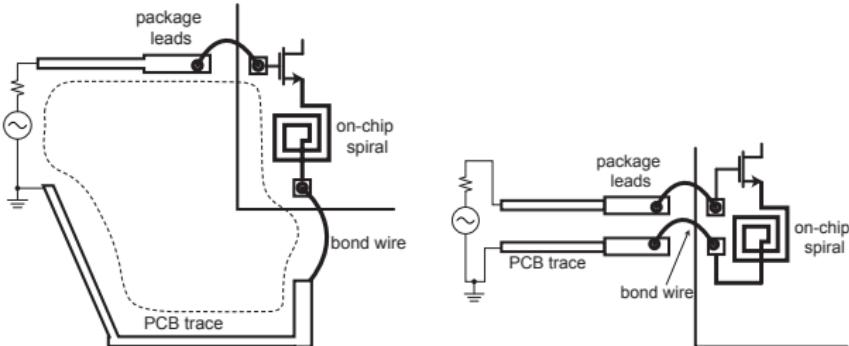
- Higher accuracy requires a multi-section model to capture some distributed effects.
- Skin effect and proximity effect can be modeled using this approach [Cao]
- The equivalent circuit includes interwinding capacitance, substrate coupling, and winding to winding mutual inductance.
- While it is possible to calculate these values, they are often only used as a starting point in an optimization to obtain the best fit.

Inductance: Post Layout



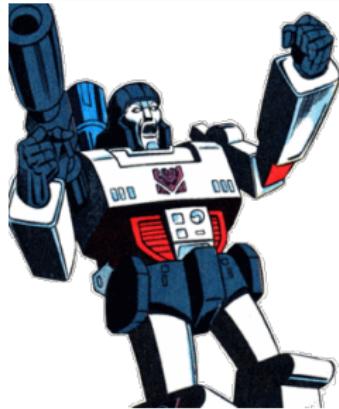
- What is the “inductance”
 - Partial Inductance
 - Ground return currents
- Coupling and shielding (later)
- Common mode rejection (breaking symmetry)

Inductance: Going Off-Chip



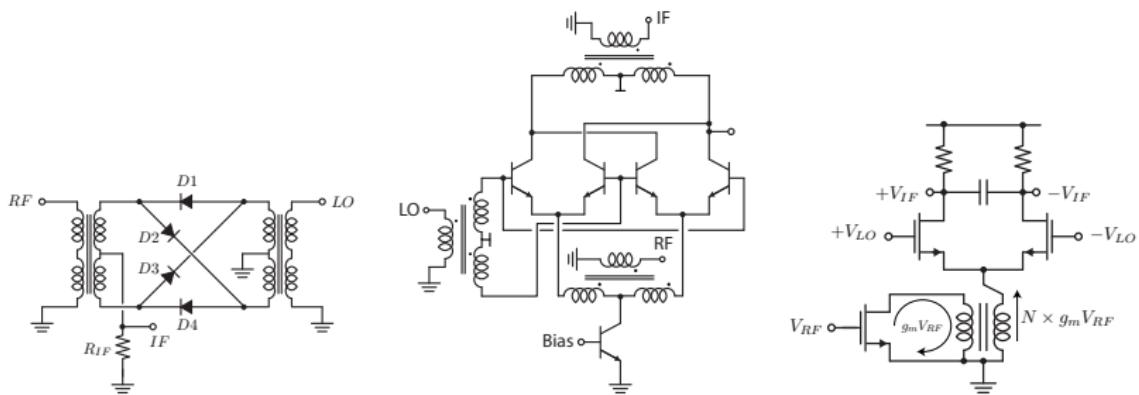
- Inductance is defined by a loop. Part of the induced emf is dropped across the source-ground connection, and the other part contributes to gate inductance. Note that the return path off-chip contributes a significant fraction of the inductance, requires care to simulate, and coordination with the board design.
- In the second design, the off-chip path is minimized by tightening the loop. The return current partially cancels the flux and lowers the inductance too (bond-wire, trace), forming a transmission line.

Transformers



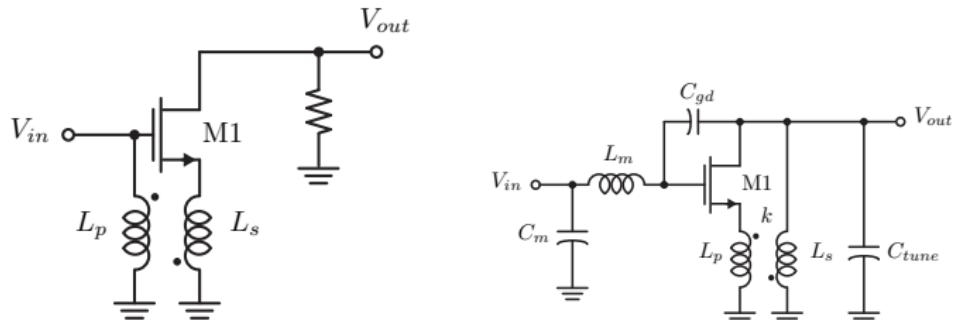
- More than meets the eye...

Applications of Transformers: Mixers



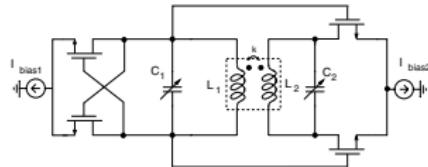
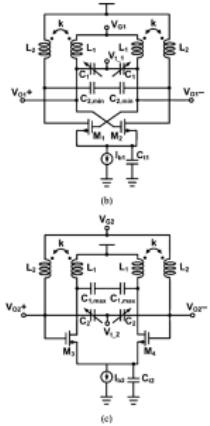
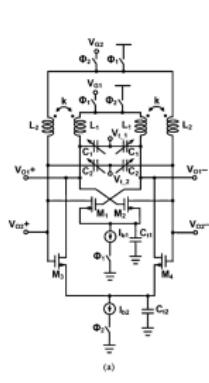
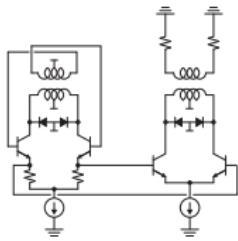
- Transformers widely used in mixers
- Useful for combining LO and RF signals and providing isolation
- Useful for generating fully balanced signals for optimal mixer performance

Low Noise and Wideband LNA



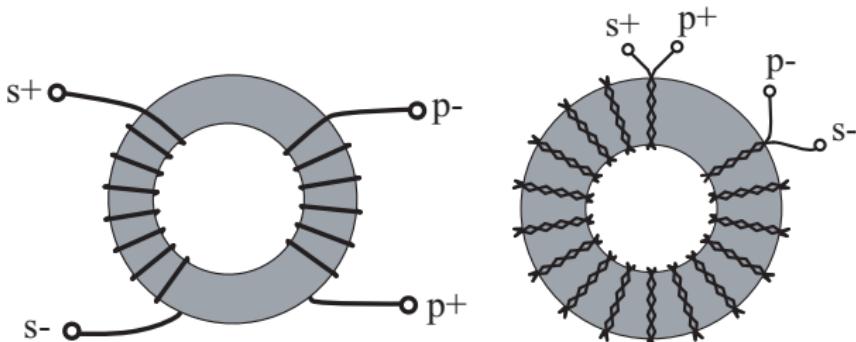
- Used for feedback and matching in [Long1]. A 0.9-dB noise figure LNA from 5-6 GHz demonstrated in $0.18\mu\text{m}$ CMOS.
- Can be used for gain boosting and broadband matching. The transformer presents a scaled $1/g_m$ impedance to the source.
- In [Long2] an LNA with 3-10 GHz bandwidth and excellent performance is demonstrated in 130nm CMOS.

Transformers in Wideband VCOs

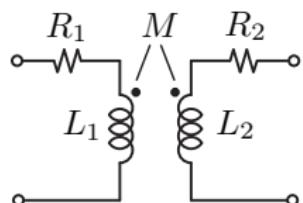


- In bipolar cross-coupled VCOs, the base current is an issue. A transformer solves this problem nicely.
- In another application, the two resonant modes of the transformer are exploited to create very wide tuning VCOs [Bevil].

Lumped Transformers



- At low frequencies, a magnetic core boosts the inductance and concentrates the flux.
- At high frequency, we rely on spatial proximity to create a high coupling factor.



Transformer Specifications and Metrics

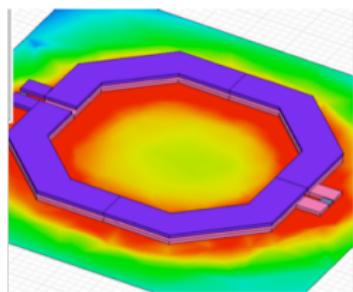
- Inductance L (primary and secondary winding).
 - Sets location of zero in transfer function.
 - Tuned transformer or broadband transformer?
- Coupling Factor k
 - Leakage inductance.
- Quality Factor Q
 - Of each winding individually.
- Winding Resistance R
 - Sets the insertion loss at low frequencies. Prevents one from using too large a winding (for good low frequency cut-off)
- IL_{min}
 - Minimum insertion loss of structure when bi-conjugately matched.
 - Bandwidth under biconjugate match at one point?

Unique Properties of Transformers

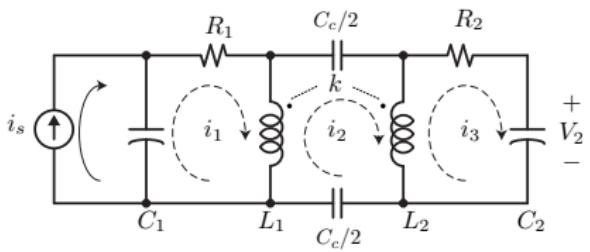
- Lower magnetic flux compared to an inductor. See next slide.
- Impedance matching occurs automatically.
- Low loss independent of matching ratio (unlike an LC network).
- DC isolation / biasing, extremely convenient for circuits.
- Transmission line transformers can extend frequency range of operation.
- Common mode rejection crucial for circuits living in a “dirty” environment. Also good for stability.
- Broadband operation due to inherent low Q . See next slides.

Lower Magnetic Flux

- Because the induced currents flow in a direction opposite the primary currents, they tend to cancel the flux of the primary.
- This means that the flux is much lower and occurs mainly between the windings.
- This helps to reduce eddy current losses but more importantly it also means fewer stray fields minimizes coupling to nearby structures.
- Transformers can be packed more tightly as a result.



Transformer Resonance



$$\omega^+ = \frac{1}{C(L + M)} = \frac{1}{LC(1 + k)}$$
$$\omega^- = \frac{1}{C(L - M)} = \frac{1}{LC(1 - k)}$$

- Transformers have two resonant modes – resonance and anti-resonance.
- In the resonant mode, the currents flow in phase and reinforce the magnetic field. The effective inductance is boosted and the coupling capacitance does not play a role.
- In anti-resonance mode, the currents flow in opposite phase and reduce the magnetic field. The coupling capacitor now plays an important role.

Broadband/Low Q Structure

- Consider the impedance looking into a transformer with a load resistance:

$$V_2 = -I_2 R = sM I_1 + sL_2 I_2 \rightarrow I_2 = \frac{-sM}{sL_2 + R} I_1$$

$$V_1 = sL_1 I_1 + sM I_2 = \left(sL_1 - \frac{s^2 M^2}{sL_2 + R} \right) I_1$$

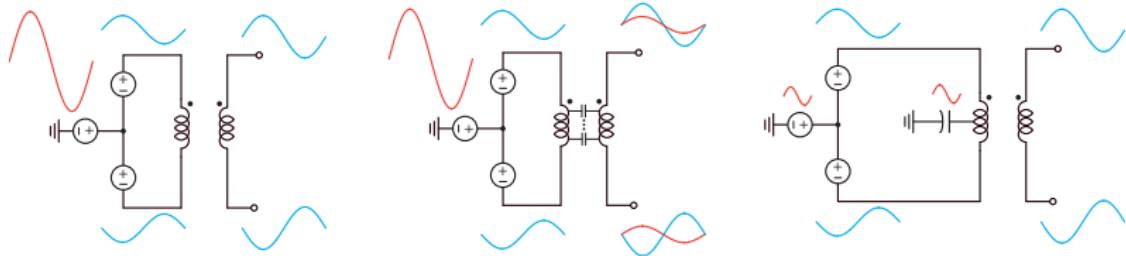
$$Z_{in} = sL_1 - \frac{s^2 M^2}{sL_2 + R} \approx sL_1 - \frac{sM^2}{L_2} \left(1 - \frac{R}{sL_2} \right)$$

$$Z_{in} = sL_1 \left(1 - \frac{M^2}{L_1 L_2} \right) + \frac{M^2}{L_2^2} R$$

$$Z_{in} = sL_1(1 - k^2) + N^2 R$$

- As expected, the load is transformed but the imaginary part is also small if coupling factor is close to unity. The structure stores very little energy.

Common Mode Rejection



- Common mode signals are rejected by an ideal transformer. For a signal to be transferred to the secondary, current has to flow through the primary winding.
- Note that common-mode signals will flow through the center-tapped node and therefore good bypass should be supplied there.
- A real transformer has capacitance from winding to winding and thus can couple common-mode signals, although they are rejected very well below the self-resonance frequency.

Transformer Matching / Loss

- The insertion loss of a transformer can be calculated from the maximum power gain (bi-conjugate match)
- For a simple transformer, the maximum gain is a function of only the winding Q factors and the magnetic coupling factor (k)
- It's independent of the matching ratio!

$$K = \frac{2\Re(Z_{11})\Re(Z_{22}) - \Re(Z_{12}Z_{21})}{|Z_{12}Z_{21}|}$$

$$Z = \begin{pmatrix} R_p + j\omega L_p & j\omega M \\ j\omega M & R_s + j\omega L_s \end{pmatrix}$$

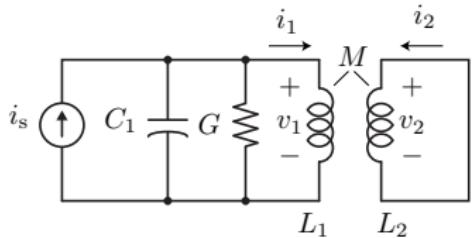
$$G_{max} = \frac{Y_{21}}{Y_{12}} \left(K - \sqrt{K^2 - 1} \right)$$

$$K = \frac{2R_p R_s + \omega^2 M^2}{\omega^2 M^2}$$

$$= \frac{2R_p R_s}{\omega^2 M^2} + 1 = \frac{2}{k^2 Q_p Q_s} + 1$$

$$G_{max}(Q, k) = 1 + \frac{2}{Q_p Q_s k^2} - 2 \sqrt{\frac{1}{Q_p^2 Q_s^2 k^4 + \frac{1}{Q_p Q_s k^2}}}$$

Tuned Transformer



$$v_2 = 0 = j\omega Mi_1 + j\omega L_2 i_2$$

$$\frac{i_2}{i_1} = -\frac{M}{L_2} = -k \sqrt{\frac{L_1}{L_2}}$$

$$i_1 = i_s - Gv_1 - j\omega C_1 v_1 = i_s - (G + j\omega C_1)(j\omega Mi_2 + j\omega L_1 i_1)$$

$$i_1 = i_s - (G + j\omega C_1)j\omega L_1(1 - k^2)$$

$$i_s = i_1(1 - \omega^2 L_1 C_1 (1 - k^2) + j\omega L_1 G)$$

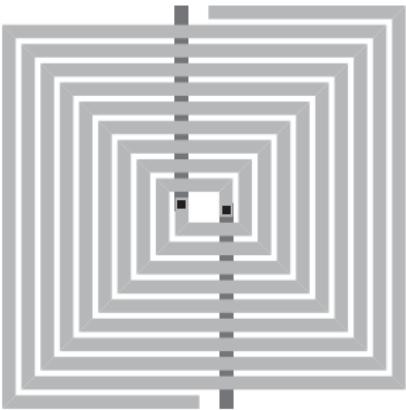
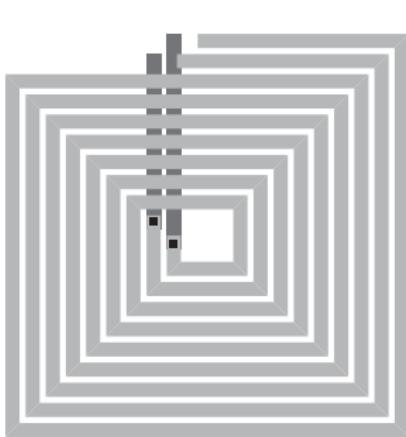
$$\omega_0 = 1 / \sqrt{L_1 C_1 (1 - k^2)} \rightarrow i_1 = i_s \frac{R}{j\omega L_1} = -jQ i_s$$

- Often the transformer is used as a tuned circuit. The properties are a bit different since there is a resonant current boost. If both input and output are tuned, we can split the poles to create a broadband response.

Problems in Real Transformers

- Coupling factor k is not unity. In fact, the coupling factor can be as low as 0.5 - 0.8 for typical layouts.
 - The consequence of this is that there is always a leakage inductance associated with the structure (which can be tuned out ... but then it's more narrowband).
- Winding inductance L
 - Cannot make it too large since it will have low Q (high resistance), which means large insertion loss.
- Self-resonant frequency (SRF)
 - A large inductance will also cause the structure to self-resonate earlier.
 - Note that self-resonance is also determined by interwinding capacitance, which is something we often neglect in an inductor.

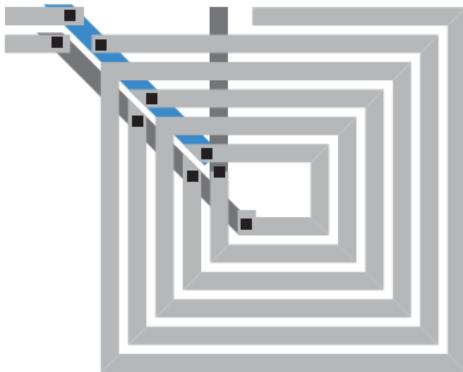
Planar 1:1 Layout Styles



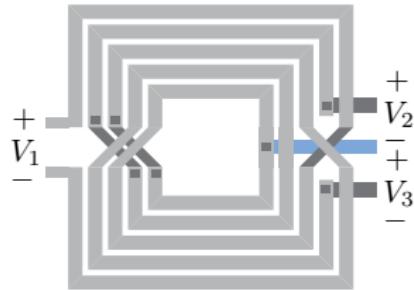
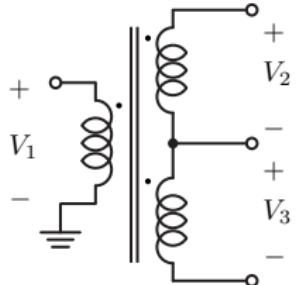
- This is the bifilar layout style. The first version is asymmetric, and the input/output ports are near each other.
- The second version is fully symmetric and the input/output are isolated.
- In each case, if the secondary winding is removed, the primary is just a spiral inductor. The secondary winding is interwoven alongside the primary to maximize the coupling.
- Lateral structures have k factors of about 0.6 - 0.7.

Planar N:1 Layout

- In most situations, we would like to use a non unity turns ratio for impedance matching.
- While the inductance of the secondary can be varied by the width and spacing of the conductors, it is only a weak function of these parameters. It's a much stronger function of the area and number of turns.
- In the layout above, the primary has 3 turns and the secondary has 3 parallel turns, in effect 1 turn. The turns ratio is approximately 3:1
- Since the current transforms in the opposite way, it's good to increase the width of the lower turns side. In this layout this occurs automatically.

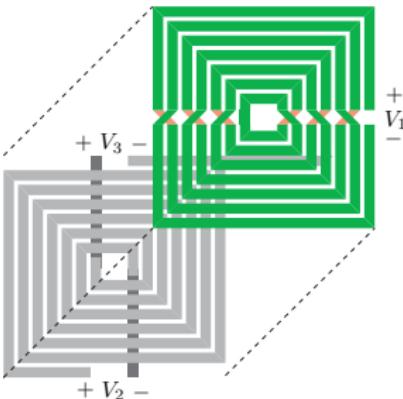


Baluns



- An ideal balun converts a single-ended signal into a fully differential signal. The output signal is fully balanced without any common-mode.
- The center tap is a convenient location to bias the secondary side of the transformer.
- A symmetric spiral inductor is a good starting point for the balun. Two symmetric spirals can be wound together and the center tap is grounded on one side.
- Capacitive coupling can introduce unwanted common mode signals to the output.

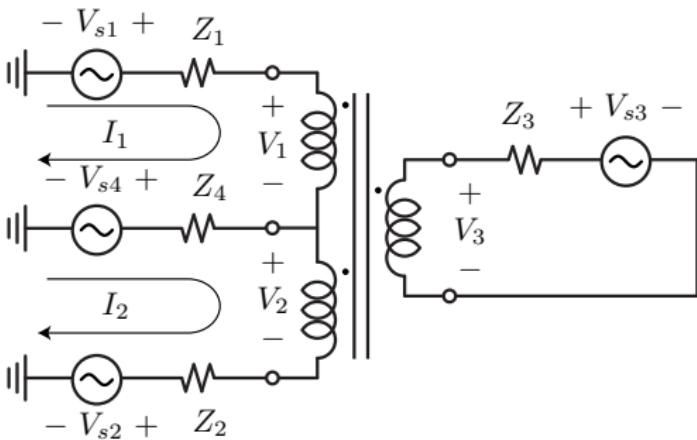
3D Structures



- Given the plethora of metal layers, you are only limited by your imagination when it comes to laying out transformers.
- In this example a symmetric spiral is put on top of a non-symmetric transformer forming a 3-port circuit. The top port can be used as a balanced port and the bottom two can be used to inject single-ended signals.
- The signal V_1 is proportional to the difference between V_3 and V_2 .

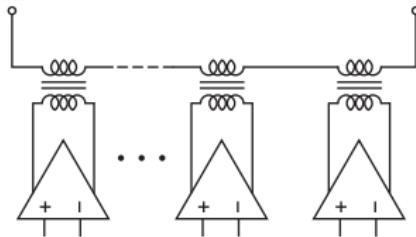
Hybrid Structure

$$Z_1 = Z_2 = Z$$
$$Z_3 = \frac{Z_4}{N^2} = \frac{Z^*}{2N^2}$$

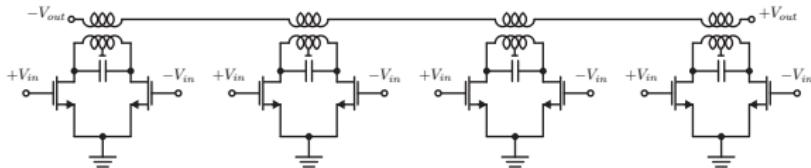


- A hybrid is a four port device that can be matched at all ports and provide isolation between the ports.
- For instance V_{s3} is proportional to the difference of V_{s1} and V_{s2} whereas V_{s4} is proportional to the sum
- Ports 3 and 4 are isolated as are ports 1 and 2.

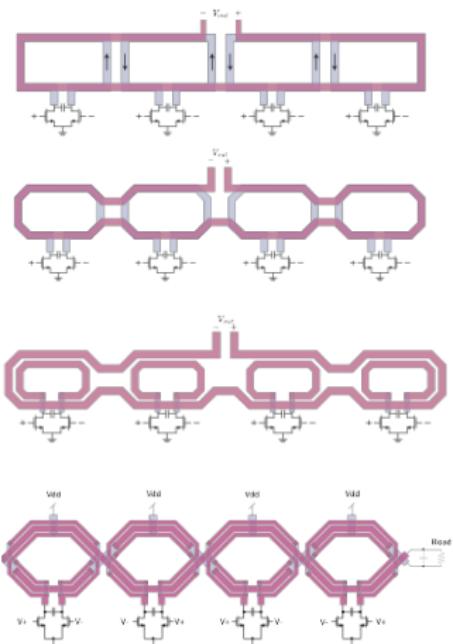
Voltage Combiners



- The voltage at the output is the sum of the voltages of all the driver stages.
- The coils are 1:1 and so each driver sees the total load power, but only $1/N$ the load voltage. This means the drivers see an impedance smaller by $1/N$.
- Since impedance matching and power combining is occurring through this structure, it can be used to boost the power of low-voltage drivers.



Layout of Transformer Combiner



Straightforward implementation suffers from flux cancellation

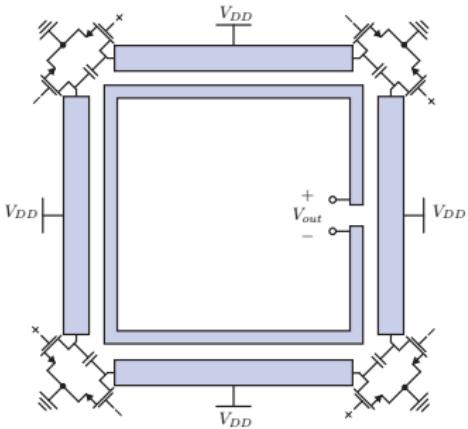
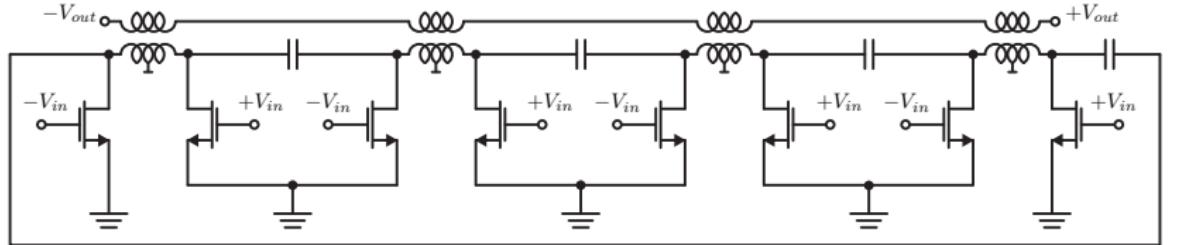
Coils spaced out and oval shape to minimize flux loss.

In a lateral version (one thick metal only), the loops are no longer 1:1 and current constriction occurs, increasing the loss.

A figure-eight structure has symmetric 1:1 turns, two-sided coupling and thus more uniform current, and a natural way to connect the loops.

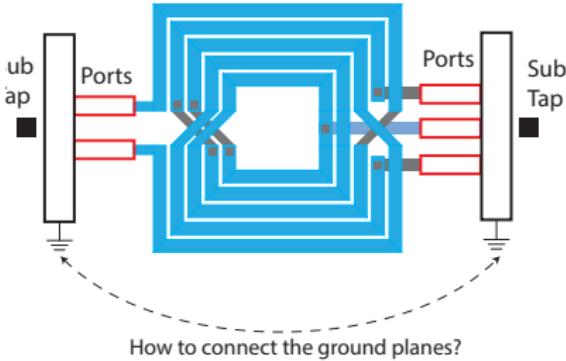
Distributed Active Transformer (DAT)

- Exploit differential operation to form virtual grounds.
- Drive each winding differentially, but ensure that neighbor winding is cross-differential as well. This means that the center of each conductor is a virtual ground.
- Extra leads are eliminated, improving loss of structure.



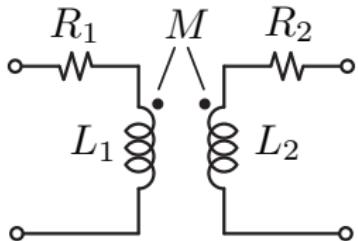
Simulation Issues

- Grounding the ports is always an issue. If the input and output windings are not nearby, then a ground path needs to be established to allow common mode signals to flow.



- Instead of guessing where the ground path should be, use the real circuit layout to establish this. This includes the ground plane and substrate contacts.
- Simulate the structure as a 4-port rather than a 2-port. This way you will capture both even and odd modes (common mode signals and differential signals)
- The center tap is important to simulate. Make it a 5-port (or 6) simulation if your structure uses the center tap.

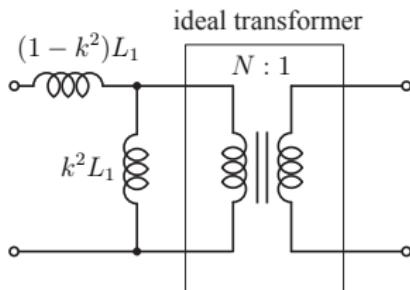
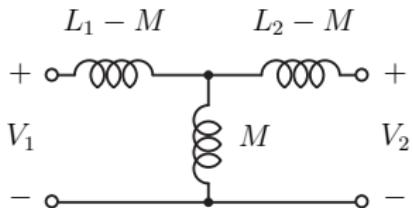
Transformer Narrowband Model



$$Z = \begin{pmatrix} R_p + j\omega L_p & j\omega M \\ j\omega M & R_s + j\omega L_s \end{pmatrix}$$

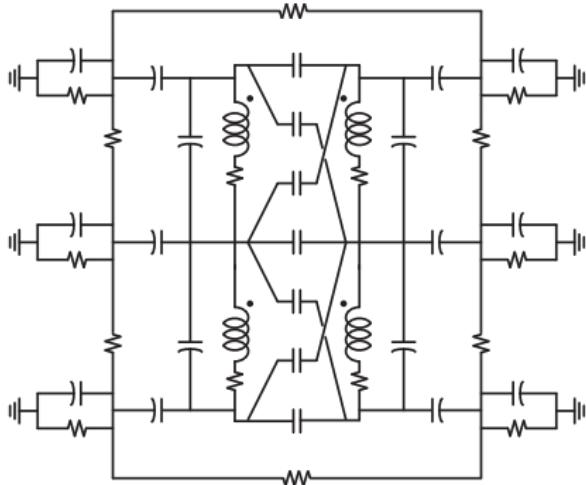
- At a fixed frequency, the two-port parameters of the structure have a one-to-one equivalence with the following circuit model.
- This model is useful to check to make sure the two-port parameters from a long simulation actually make sense. Do the winding inductances and coupling factors add up?
- If a multi-port winding is simulated, the circuit simulation can be used to appropriately ground / leave open other ports and to extract two port parameters.
- If the real part of Z_{12} is not zero, this is a good sign that capacitive coupling is occurring.

Modeling for Hand Analysis



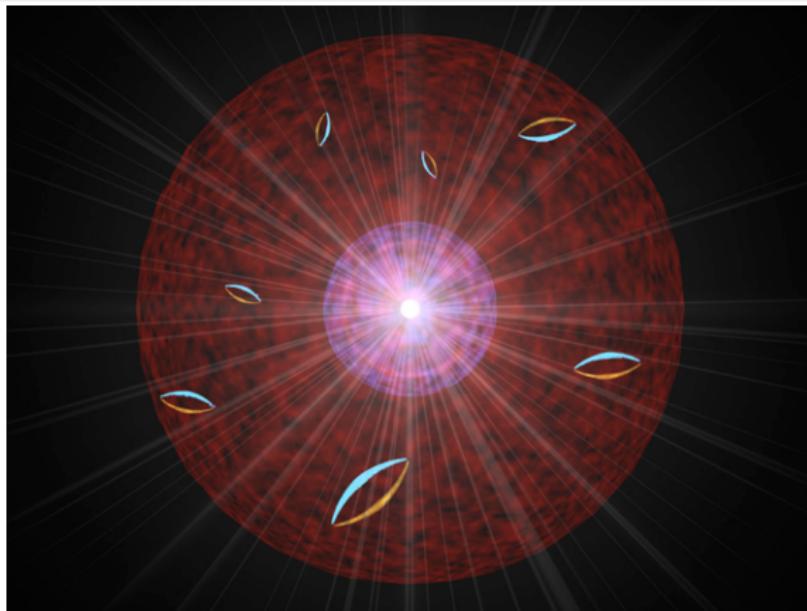
- Coupled inductors can be represented as a T-network, or an ideal transformer with parasitics
- Notice that even if the coupling factor $k = 1$, there is still inductance in the model. This is true because a transformer cannot work with DC currents.
- If the inductance of the winding is large enough, it can be neglected at AC frequencies.

Computer Modeling



- Similar to inductor modeling but add important coupling terms
- Symmetric 2π model
- $R - L$ network models frequency-dependent loss
- Winding capacitance for SRF
- Asymmetric substrate network

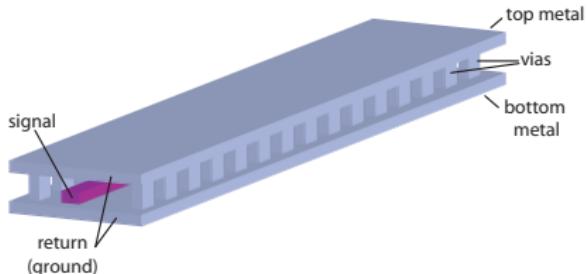
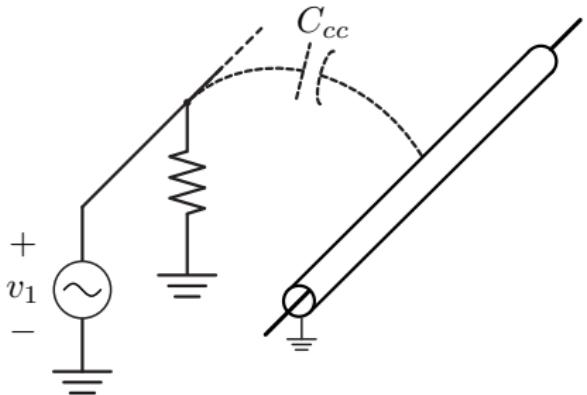
E/M Coupling



- You are not alone.

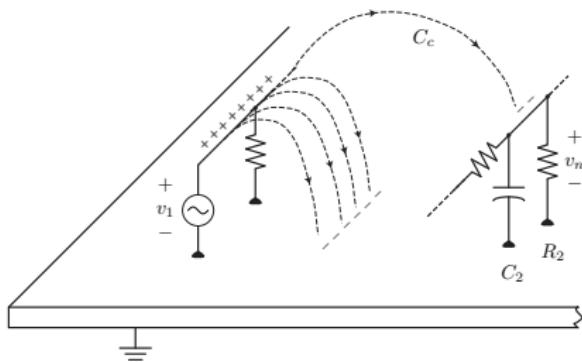
Source: <http://www.physics.purdue.edu/topaz/research/electron.gif>

Electrical Coupling

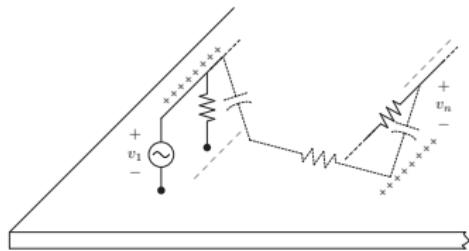


- Perhaps the easiest form of coupling to understand.
- Capacitive coupling between lines causes voltage coupling to occur. Keep things separated or use shields. Make sure “shield” is grounded (ground inductance?)
- Be careful of high impedance lines that easily pickup noise

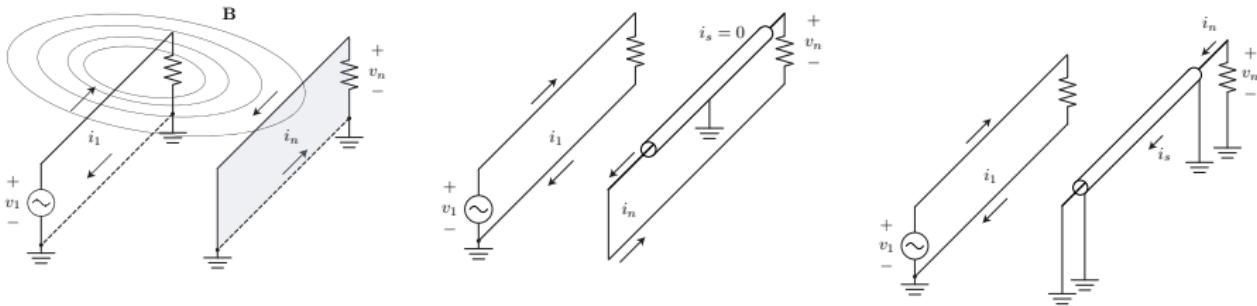
Ground Plane



- A ground plane can help a great deal since stray fields are minimized.
- Note that if the ground plane is floating, then it may increase the coupling between distant points!

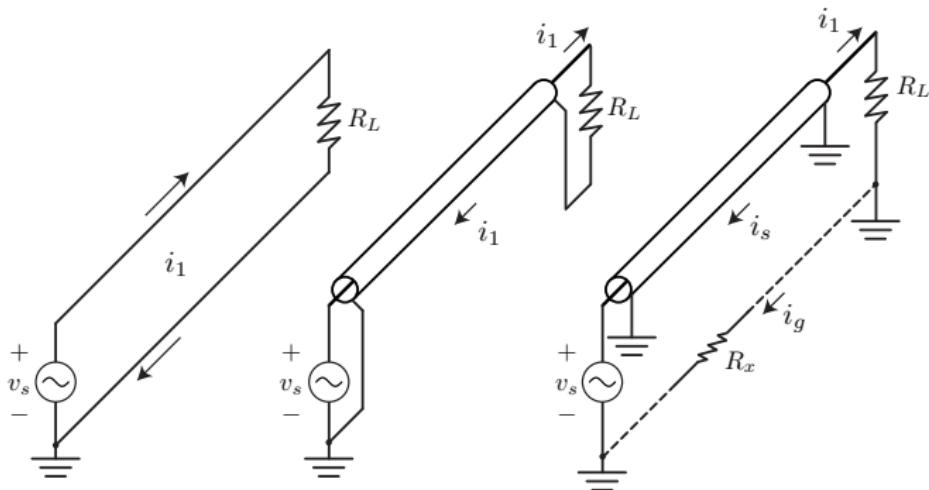


Magnetic Coupling



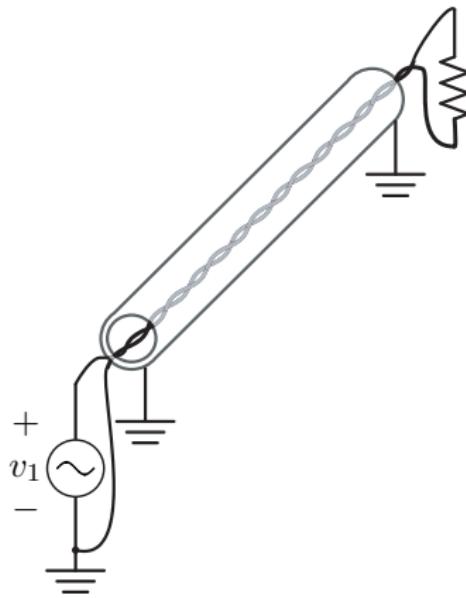
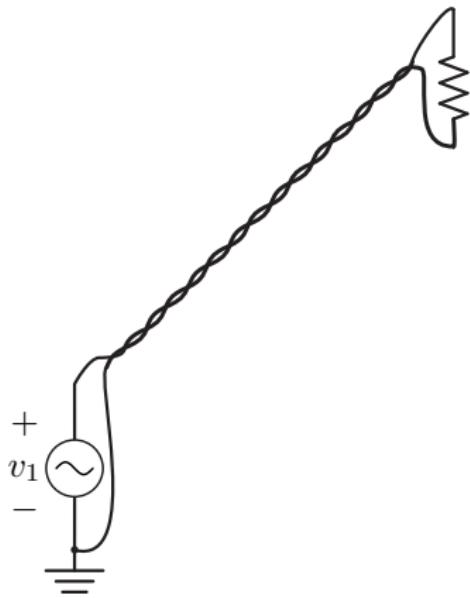
- To completely understand the amount of magnetic coupling, you must define the loops in the circuit.
- If you use a shield grounded at only one point, there is actually no magnetic shielding at all!
- Both points need to be grounded so that current can flow through the shield rather than through the conductor.
- Notice that the shield current is canceling the magnetic field of the aggressor.

Controlling the Return Current



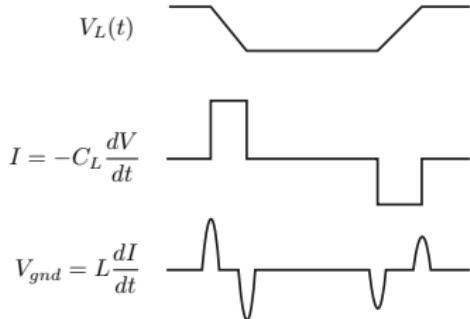
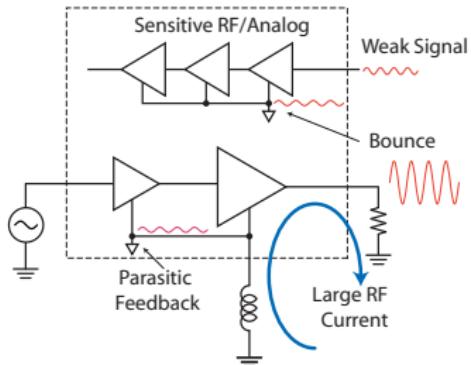
- If you explicitly define the path of the return current, then you are doing a much better job in confining the loop of the current.
- For instance, return currents may flow through the substrate or ground plane and cause unwanted (increased) coupling (since they span a larger area).

Twisted Pairs



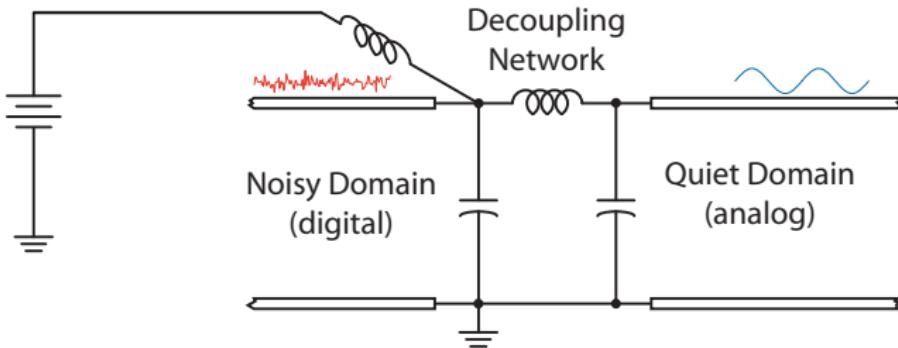
- If wires are twisted together, not only is the area of the loop minimized, but also the interference fields are canceled since successive loops have different orientations.
- A shielded twisted pair gives very good isolation.

Ground Bounce



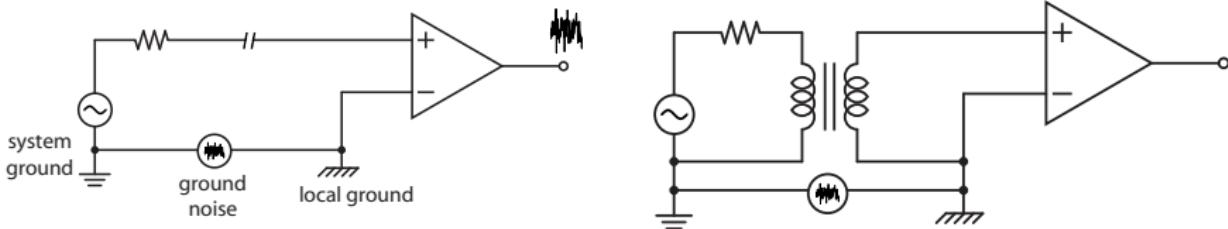
- Ground bounce (and supply bounce) is a reality in every circuit.
- Due to finite supply/ground inductance, any time current is drawn from the supply, there is finite ripple.
- If circuits are properly reference to the on-chip supply, then the bypass capacitance can help a great deal.

Separating Supply Domains

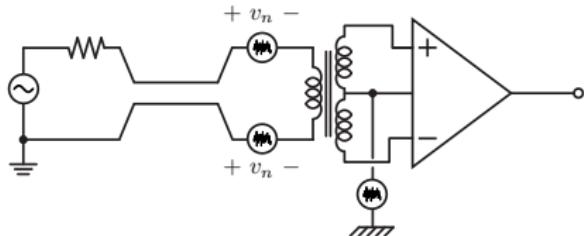


- Using separate “clean” and “dirty” supplies (aka digital and analog) can help a great deal.
- On the board, these supply domains should be decoupled since ultimately they go to the same supply (battery).
- Watch out for resonance frequencies of the decoupling network.

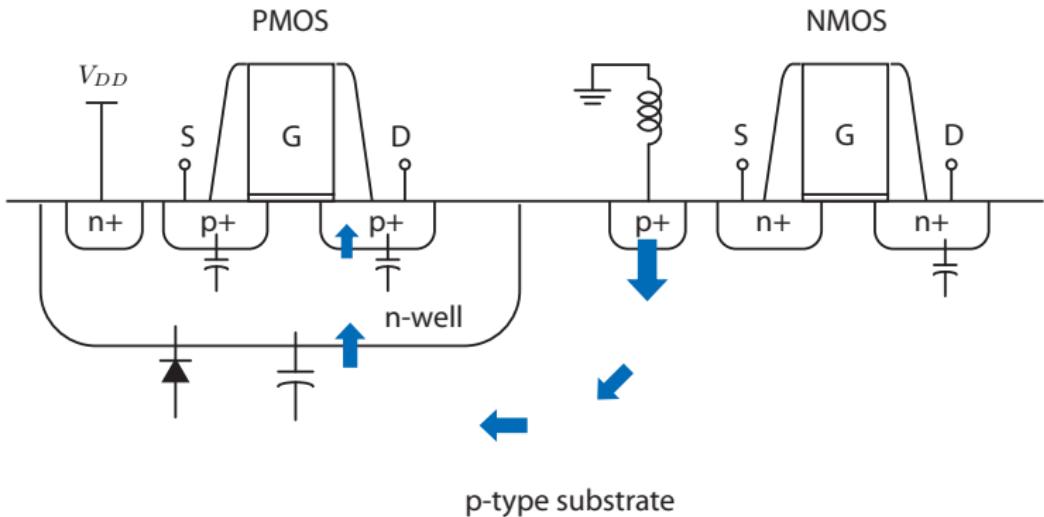
Rejecting Supply Bounce



- The on-chip ground is noisy and so this causes noise at the output of the first amplifier.
- The second amplifier uses a transformer to reject the noise.
- A true fully balanced or differential circuit is the best choice at rejecting these sources of noise.



Substrate Noise



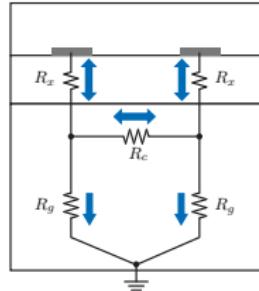
- Transistors inject noise into the substrate. Using a triple well or deep n-well process helps to reduce this noise.
 - Inductors/transformers and other large passive devices also inject noise into the substrate capacitively.

Substrate Conductance Matters

SiO_2	$t \sim 10\ \mu$
$\rho \sim 1\ \Omega \cdot \text{cm}$	$t \sim 1\ \mu$
Si bulk	
$\rho \sim 10\ \Omega \cdot \text{cm}$	$t \sim 700\ \mu$

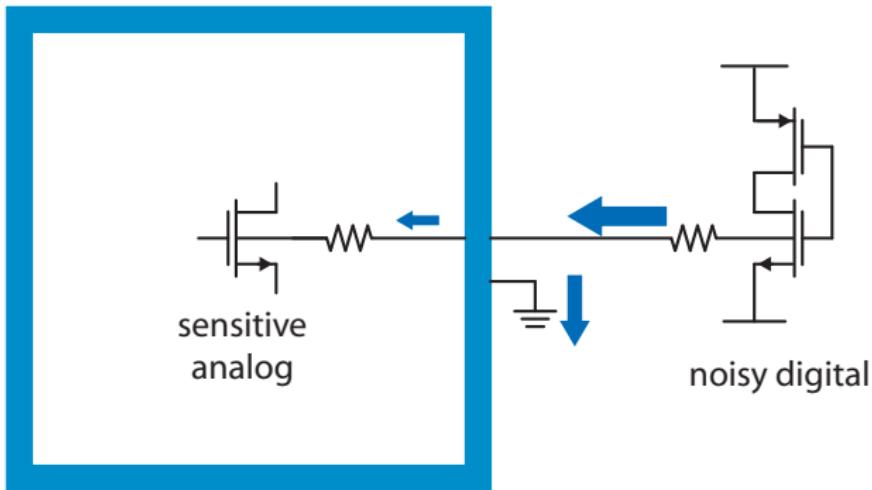
SiO_2	$\rho \sim 10\ \Omega \cdot \text{cm}$
Si bulk	$\rho \sim 10^{-4}\ \Omega \cdot \text{cm}$

$\epsilon = 3.9$	SiO_2
$\epsilon = 11.9$	
Si bulk	
$\rho \sim 10^4\ \Omega \cdot \text{cm}$	



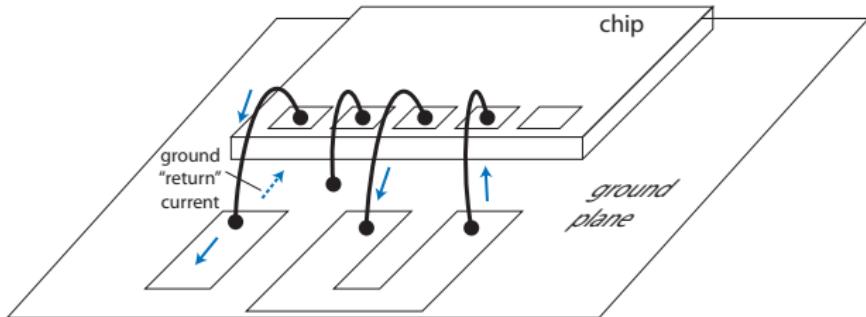
- The amount of coupling can be represented by the above equivalent circuit.
- In a lightly doped substrate, the coupling decreases with distance.
- In a heavily doped substrate, the substrate acts like a ground plane and couples everything. The coupling is nearly independent of distance.

Guard Ring



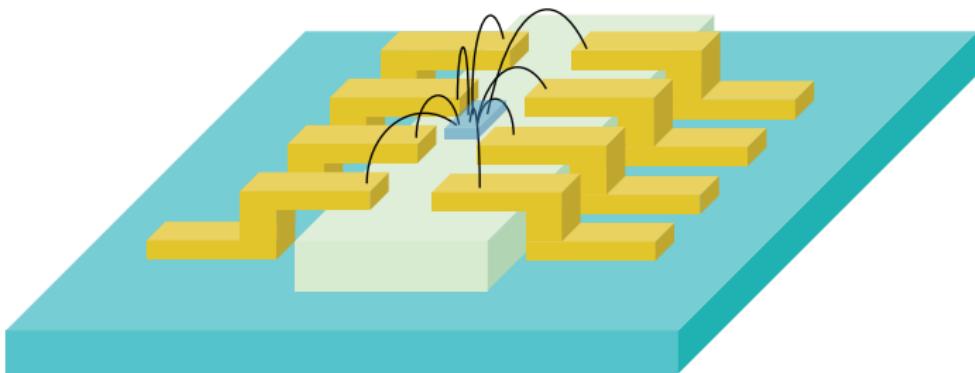
- Guard rings are commonly used to isolate structures.
- Keep in mind that these “rings” are not very deep and current can flow underneath these structures.
- Also, make sure these structures are really grounded! Ground inductance can make a big difference.

Package Coupling



- The coupling is often dominated by the package inductance and capacitance.
- Floorplan early to avoid problems. Orthogonal paths help to minimize coupling.
- Downbonds (if available) reduce inductance to ground.
- Remember that the inductance of a bondwire is meaningless until the full path for current flow is determined. Design the ground and PCB leads carefully.

Package and Board Level Parasitics



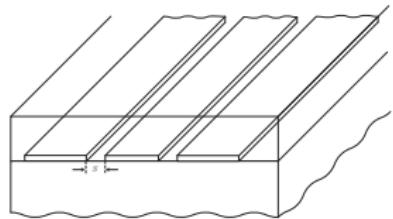
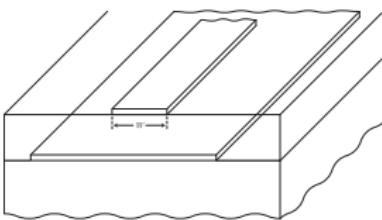
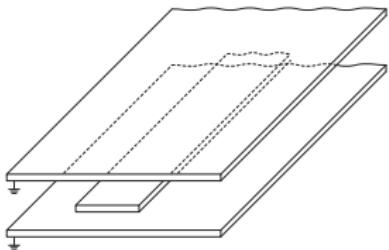
- Important to model package parasitics for RF signals going off-chip
- Package often limits isolation in circuits (accurate coupling)
- Co-simulation of chip + package + board difficult due to change of problem scale
- Higher frequency packages use flip-chip technology
- Many passive elements can be placed into package or board

mm-Wave Passives

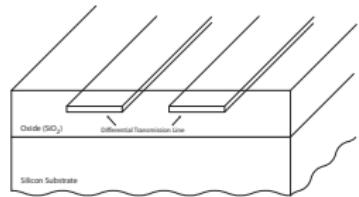
Lumped or Distributed?



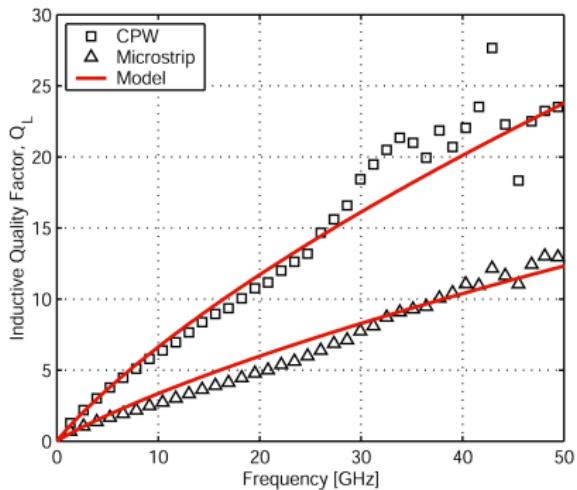
Transmission Lines



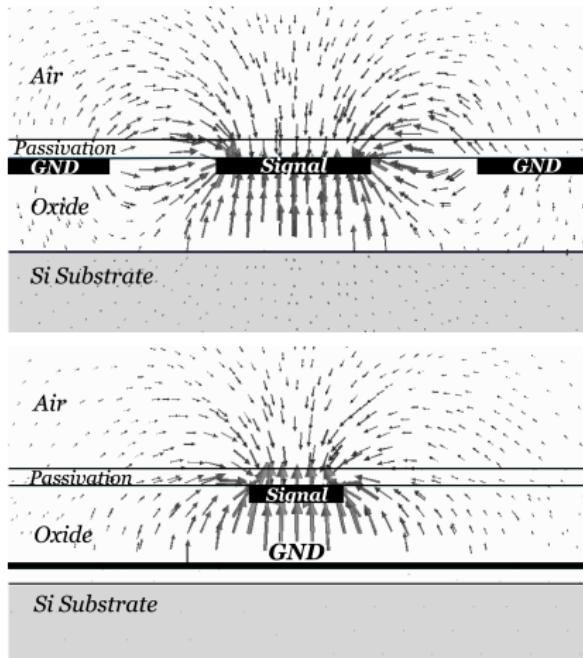
- Balanced versus unbalanced
- IC compatible (planar): stripline, microstrip, co-planar, co-planar stripline – balanced (differential)
- Metrics: Z_0 , loss, propagation constant
- Modes of propagation: TEM, TE, TM



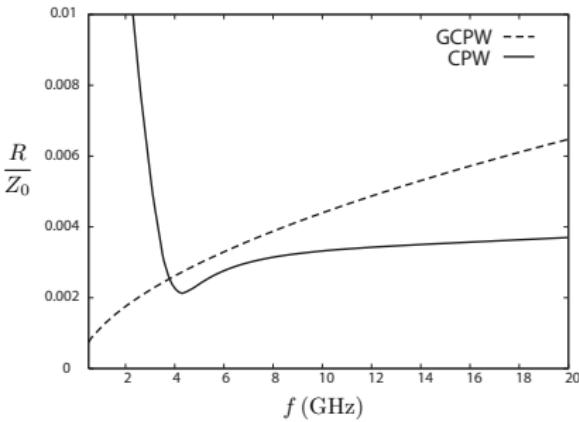
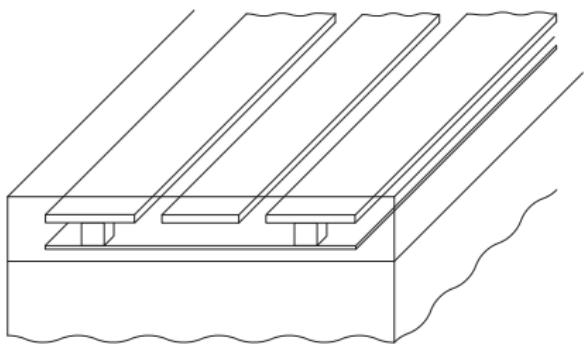
CPW versus Microstrip



- Microstrip shields fields from substrate but has higher conductor losses
- CPW can realize higher Q inductors needed for tuning out device capacitance

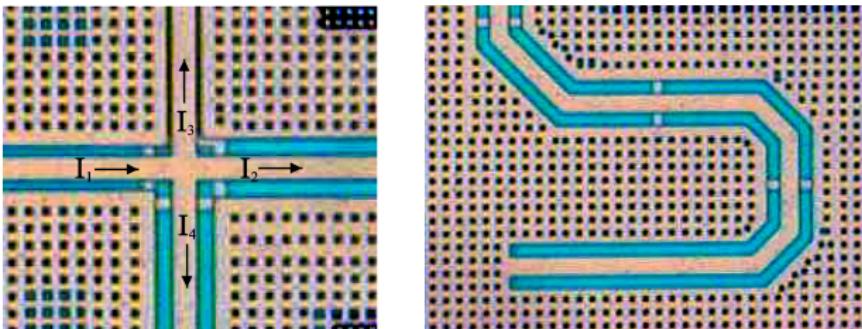


CPW versus GCPW



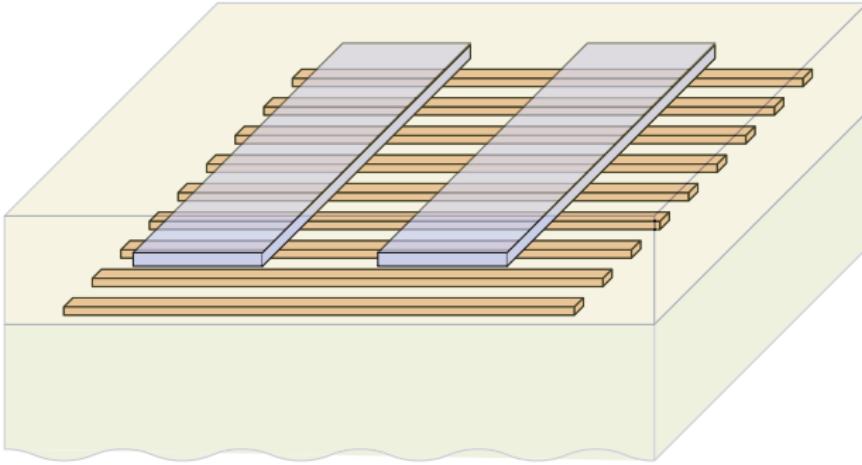
- Grounded co-planar has lower Z_0 but seems better due to shielding capability.
- In this simulation we see that at high frequencies, the CPW is lower loss (resistance per unit length) since the current flow in the GCPW is non-uniform and can flow under the line (less thick metal) at high frequencies forming a microstrip mode.

Co-Planar Waveguide Layout



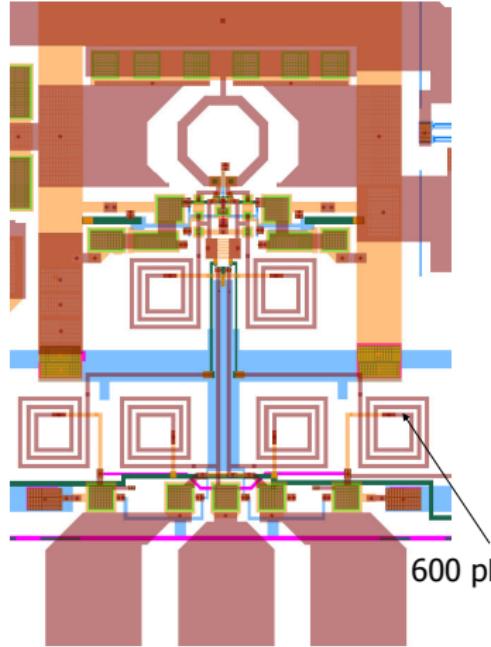
- Bridges suppress odd-mode propagation
 - Keep ground currents balanced
 - Advantage of the multi-layer metallization in CMOS
- Signal-to-ground spacing
 - Used to set Z_0
 - Helps confine EM fields
 - Effects of bends are reduced

Slow Wave T-Lines

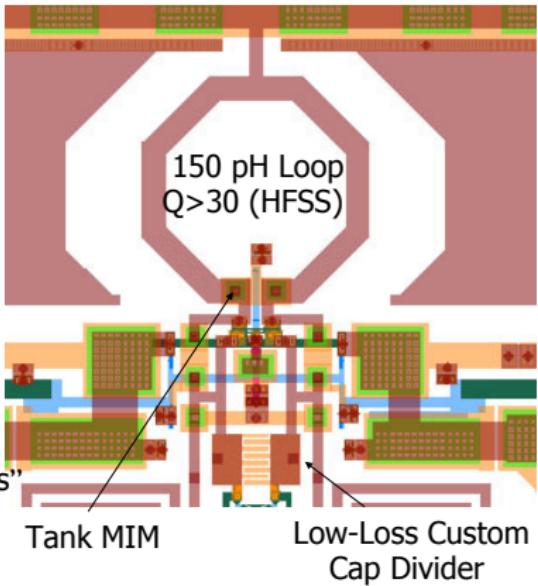


- Can use multiple metal layers to improve performance.
- Slow wave structures have an artificial dielectric that increases the capacitance per unit length without altering the inductance per unit length.
- This results in a “slow wave” structure which saves Si area and potentially lower loss.

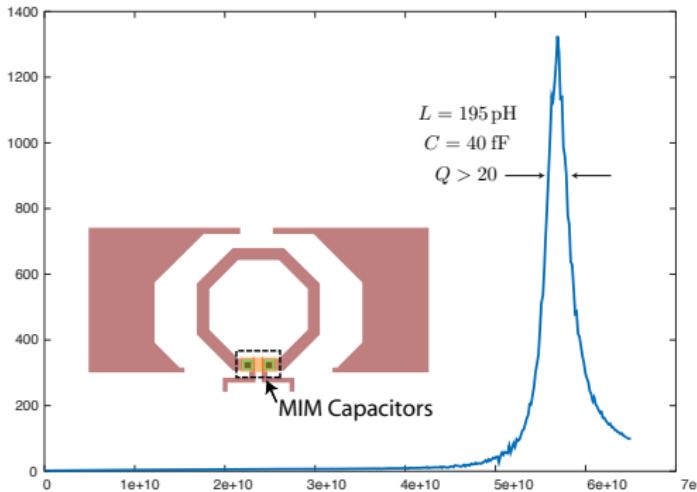
Lumped LC Tank Resonator



Low Loss MIM Cap and Inductor Ring
Tightly Coupled for Low Loss



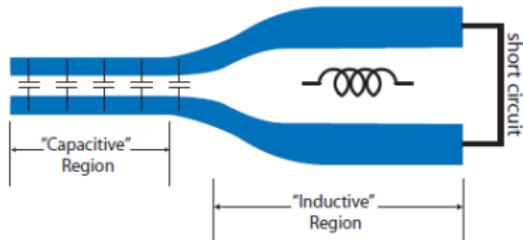
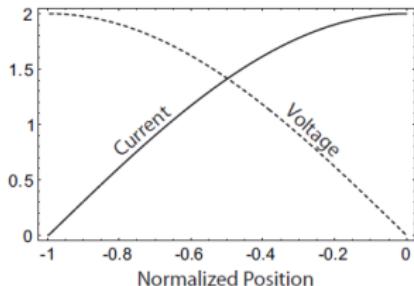
Inductor or T-Line?



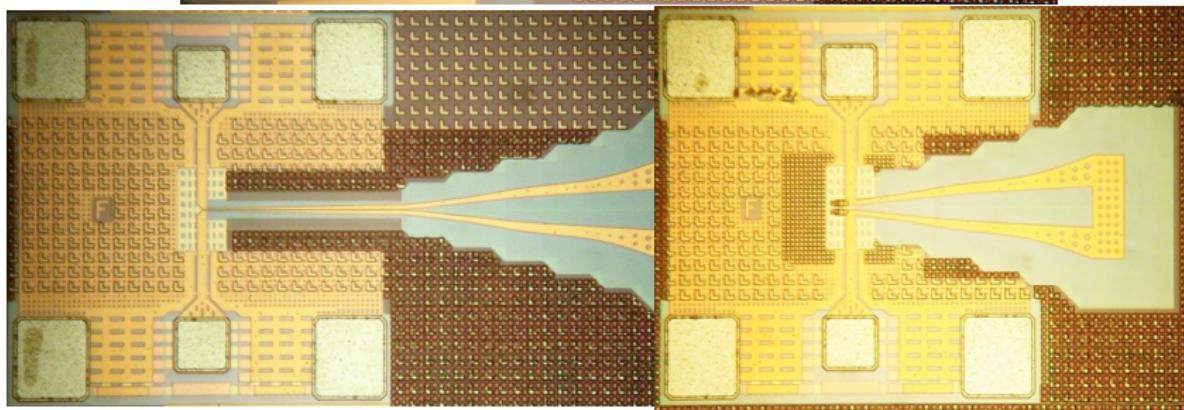
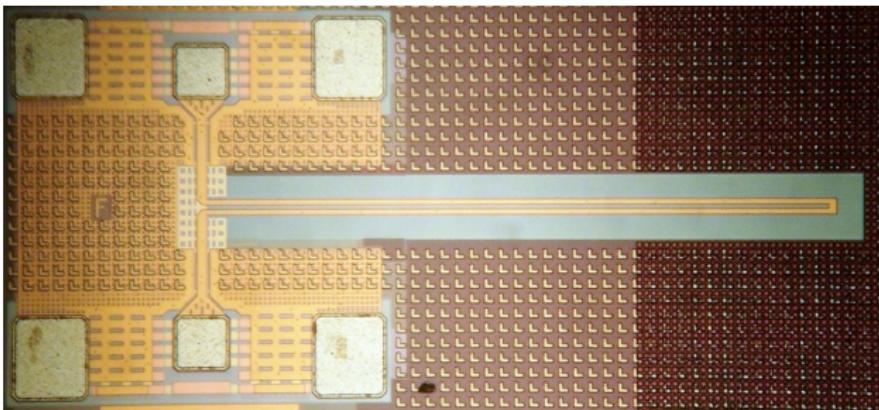
- LC resonators have good Q factor . . . varactors are problematic above 40GHz
- High Z_0 quarter wave resonators \rightarrow loop inductors?

Optimal Taper Profile

- Andress and Ham [And] showed that a tapered resonator has improved Q
- Assumed a constant Z_0 line. What if you remove this constraint?
- Result looks like an LC tank!

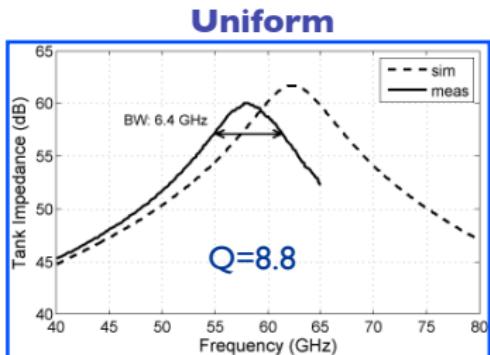


Resonator Layouts in 90nm CMOS

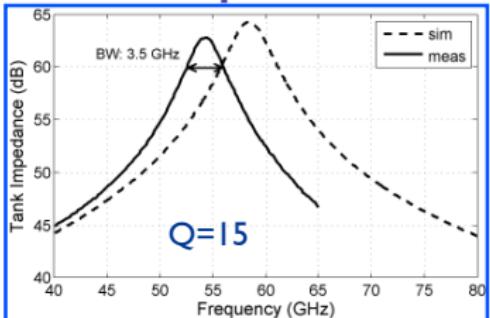


Resonator Meas vs. Simulation

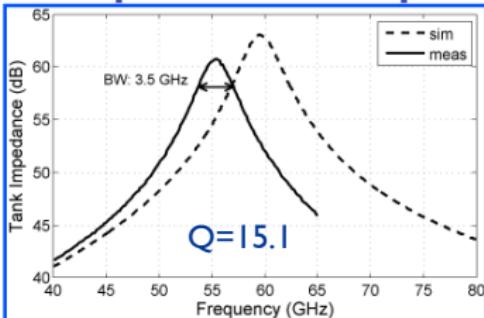
70% improvement



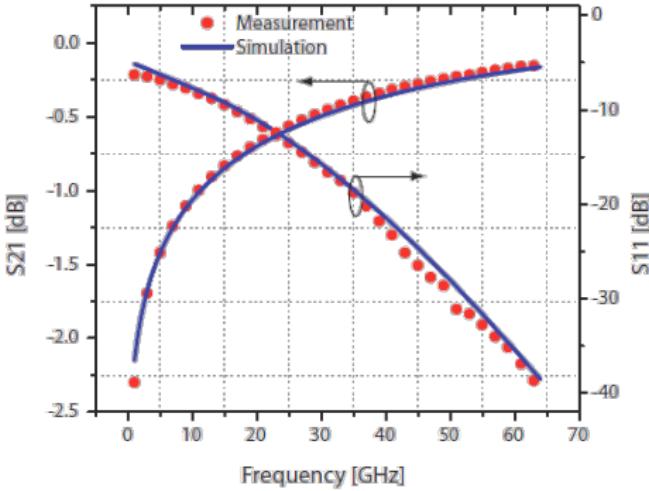
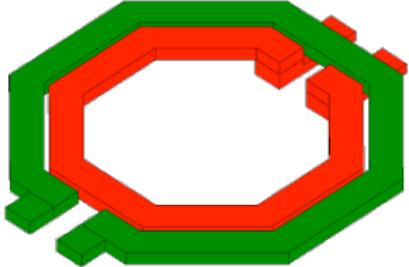
Tapered



Cap-loaded Half-taper

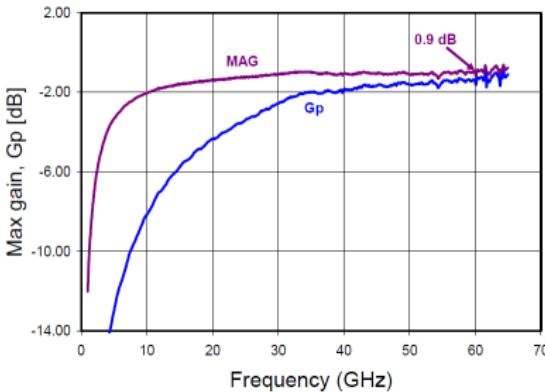
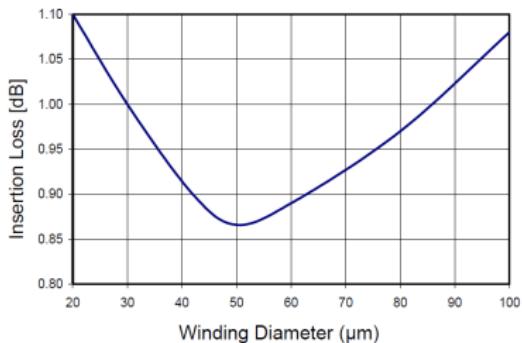


Transformers Scale to mm-Waves



- Isolation, impedance matching, biasing ...
- Good insertion loss
- Compact layout compared to T-lines

Transformer Design



- Optimal dimension to minimize insertion loss (IL) found by sweeping a geometry. Can fit a model of a differential transmission line (use even and odd mode impedances) to speed up design [Chow].
- For a particular design, the source or load impedance may be fixed (for example in an LNA or PA, or an inter-stage match where one side is optimized for noise or power). In this case G_p and G_a can be plotted to optimize performance. More on this later.

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