## 12.9 A Fully Integrated 6W Wireless Power Receiver Operating at 6.78MHz with Magnetic Resonance Coupling

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Wireless power transfer (WPT) systems are becoming ubiquitous with applications in powering medical implants and a range of portable consumer electronic devices such as smart phones and wearable devices. Wireless power transferring methods can be classified into two types: inductive and resonant. For the resonant type, wider-range power transfer is possible, and multiple devices with different power requirements can be charged at the same time. The Alliance for Wireless Power (A4WP) has chosen the 6.78MHz ISM band as the power-transfer frequency [1]. At 6.78MHz, the associated switching loss is an order of magnitude larger than that in a typical wireless receiver based on an inductive coupling, with a carrier frequency of around 200kHz. Besides the two fundamental aspects of switching frequency and power, there is a third important parameter, notably the higher input voltage range needed for the 'loosely coupled' resonant type, which is 25V maximum for this work. Ref. [2] appears to be one of few works that can be entirely related to the current work, targeting the same application. However, it does not integrate the most critical parts of the receiver, such as the AC-DC rectifier. Other works in the same frequency range are either limited to low-power applications [3] or the AC-DC rectifier is a stand-alone chip [4-5].

In this paper, a fully integrated 6W resonant-type 6.78MHz wireless power receiver including a high-efficiency on-chip AC-DC rectifier, is described. Figure 12.9.1 shows the simplified block diagram of the receiver IC. The received AC power is converted into DC voltage $V_{rect}$ by the AC-DC rectifier, and then linear regulator $LDO_1$ generates the 5V output voltage $V_{LDO1}$ for internal supply. The companion out-of-band communication chip is powered by two linear regulators $LDO_2$ and $LDO_3$. The output of the rectifier $V_{rect}$ is regulated to 5V output voltage $V_{chg}$ by the buck converter for battery charging. If the rectifier output $V_{rect}$ reaches the target value, a 2-way power switch changes the input voltage of the linear regulators $LDO_2$ and $LDO_3$ from $V_{LDO1}$ to $V_{chg}$ in order to maximize the system efficiency. For simplicity, other functional blocks such as a 12b SAR-ADC, protection circuits, NTC temperature-sensing circuit, logic functions and one-time-programmable memory, etc., are not shown here.

Even a small timing mismatch can be a cause of substantial efficiency degradation for a fully active AC-DC rectifier operating in the 6.78MHz or 13.56MHz ISM band frequency [6]. The AC-DC rectifier structure of this work is selected based on comparative analyses with the fully active rectifier structures. The focus is on the efficiency, simplicity and robustness on PVT variations. Figure 12.9.2 shows the implemented AC-DC rectifier details. It is composed of two on-chip Schottky diodes D1 and D2 for the high side stage, and of two NMOS transistors $M_5$ and $M_6$ for the low side stage driven by common-gate drivers $M_1$ and $M_2$, respectively. The Schottky diode optimized for this application is implemented without any additional mask layer. LDMOS transistors $M_5$ and $M_6$ are automatically turned on and off depending on the polarity of the received AC input voltage. To illustrate the operation of the AC-DC rectifier more clearly, the associated waveforms are also shown in the same figure. To reduce the associated switching losses of the NMOS transistors, gate voltages $V_{L1}$ and $V_{L2}$ of the MOS transistors are limited to $V_{L5R}$-$V_{th1}$ and $V_{L5R}$-$V_{th2}$, by the operation of the linear regulator $V_{L5R}$ and common-gate transistors $M_1$ and $M_2$. The gate capacitances of $M_5$ and $M_6$ act as a part of the LC tank [6]. Hence, there are only small ohmic losses from parasitic resistances in the related current paths and the switching loss is minimized. In this structure, there is no start-up problem as in fully active rectifiers. The peak efficiency of the AC-DC converter is 92.8%. Considering the 6W maximum power level with 25V maximum input voltage range at a frequency of 6.78MHz, the above efficiency number is the result of an optimal trade-off between switching and conduction losses. NMOS transistors $M_3$ and $M_4$ for over-voltage protection (OVP) activate the de-tuning capacitors $C_2$ and $C_3$ to shift the resonance frequency and thus to reduce the received AC power under over-voltage conditions of the $V_{rect}$.

Figure 12.9.3 shows the DC-DC switching regulator details. It steps down the rectifier output voltage $V_{rect}$ to a regulated 5V DC voltage $V_{chg}$. An average current-mode control (ACMC) is applied to achieve precise load-current control as well as the output-voltage regulation. The advantages of ACMC over the traditional peak current-mode control (PCMC) are enhanced noise immunity, no requirement for slope-compensation, excellent voltage and current regulation, and fine behaviour in both continuous and discontinuous inductor current modes. These advantages make the architecture more suitable for such an application in which the input is provided by an AC-DC rectifier. The output voltage of the converter is dynamically scalable within a 4.2-to-5.8V window with 200mV resolution, and the output current limit also can be controlled dynamically from 0.5 to 1.2A with 100mA steps. The power switch sizing and the gate driver design focuses on minimizing the power loss. A pulse skip mode control strategy is also implemented for better light load efficiency. Over 91% efficiency is achieved over full-load current conditions. The auxiliary blocks including control logic for power-on sequence (soft-start), current limiter, and zero current detector for light load operation are also illustrated in the diagram.

In the same figure, the average current sensor is also shown. The current-sensing resistor is implemented with an on-chip metal layer resistor without requiring any external component. This current sensor is used also for rectifier output current and DC-DC output current sensing. To ensure proper operation for all the operation scenarios, it is designed to work over the full range of $V_{chg}$ from 0 to 6V. The structure is a symmetrical "over-the-top" feedback amplifier, in which two operational trans-resistance amplifiers (OTRA) together with a MOS pass-device form a loop that guarantees that the current over the output resistor is a scaled version of the current over the sense resistor. A 2-way switch selects automatically the high-side or the low-side output to be used by the system.

The wireless power receiver is fabricated in a 0.13μm BCD process, and the die area is 14.44mm$^2$. It is a monolithic solution compatible with A4WP standard and shows up to 84.6% efficiency. Figure 12.9.4 shows the measured waveforms and Fig. 12.9.5 shows the measured efficiency plot of the wireless power receiver as a function of rectified voltage $V_{rect}$ and load current $I_{OUT}$ of buck converter. The efficiency is optimized around $V_{rect}$ = 10V and the maximum efficiency of the receiver is 84.6% at $V_{rect}$ = 10V and $I_{OUT}$ = 0.6A. Figure 12.9.6 shows a comparison table with wireless power receivers working in the ISM bands (6.78 or 13.56MHz) presented in the literature. Even with higher input voltage range of 25V and 6W power level, the power density figure of merit is superior to that of the other implementations. The chip micrograph is shown in Fig. 12.9.7.

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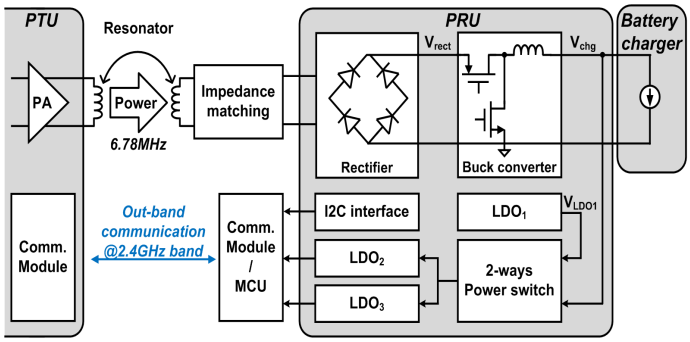


Figure 12.9.1: Block diagram of the wireless power-transfer system.

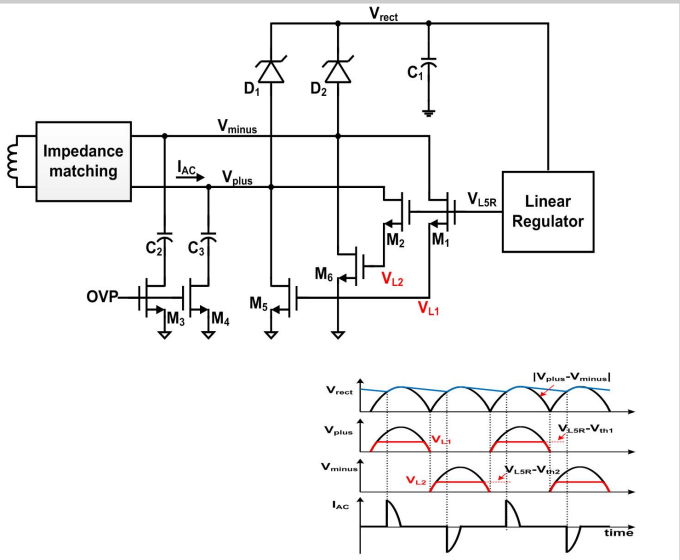


Figure 12.9.2: Schematic diagram and timing diagram of the AC-DC rectifier.

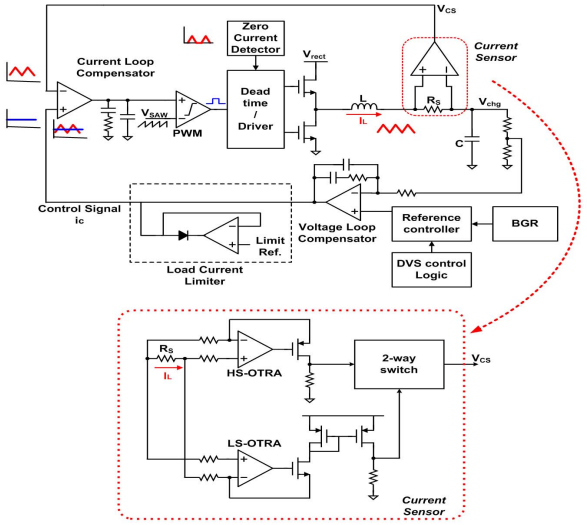


Figure 12.9.3: The DC-DC converter block diagram with the associated average current sensor.

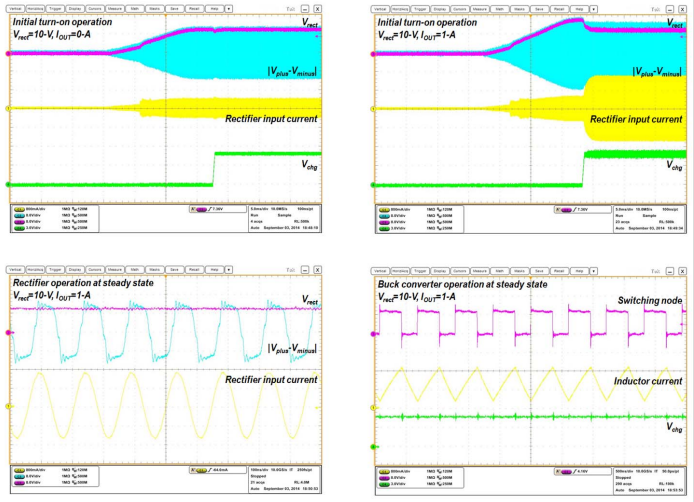


Figure 12.9.4: Measured waveforms.

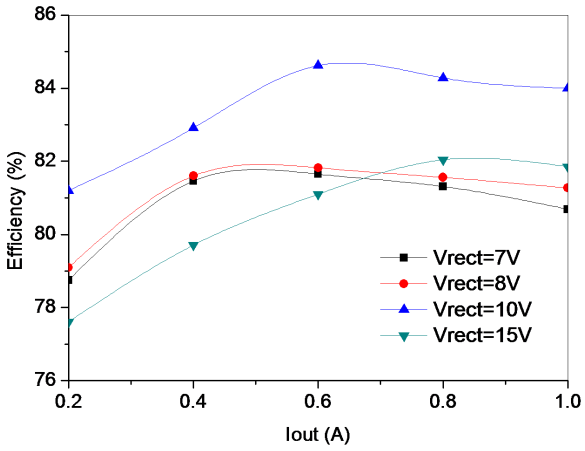


Figure 12.9.5: Measured efficiency as a function of rectified voltage and load current.

| | This work | [2] | [3] | [4] | [5] |
|---|---|---|---|---|---|
| Receiver structure | Rectifier + Buck | 3R | Voltage 2x / Rect. | Active rect. | Boost/Active rect. |
| Coil type | Resonant | Resonant | Resonant | Inductive | Resonant |
| Max input voltage | 25V | 20V | 3.1V | 1.8V | 20V |
| Max Output Power | 6W | 6W | 37mW | 6W | 1W |
| Carrier | 6.78MHz | 6.78MHz | 13.56MHz | 150MHz | 6.78MHz |
| Regulation responsible | TX & RX | RX | RX | RX | TX & RX |
| Receiver Efficiency | 84.6% | 86% | Not rated (<77%) | 17% | Not rated (>50%) |
| Rectifier efficiency | 92.8% | 92.4% | 77% | Not rated | Not rated |
| Fully Integrated | Yes | No | Yes | Yes | Multi-chip |
| Distance | 6mm | | | 0.05-0.32mm | 1mm |
| Area | 14.44mm$^2$ | N/A | ~0.6mm$^2$ | 25mm$^2$ | 12.5mm$^2$ |
| AW4P Compatible | Yes | Yes | No | No | No |
| Power density | 415mW/mm$^2$ | N/A | 61mW/mm$^2$ | 240mW/mm$^2$ | 80mW/mm$^2$ |
| Process | BCD 0.13µm | BCD 0.35µm | CMOS 0.5µm | CMOS 0.18µm | CMOS 0.18µm |

Figure 12.9.6: Performance comparison table with state of the art.

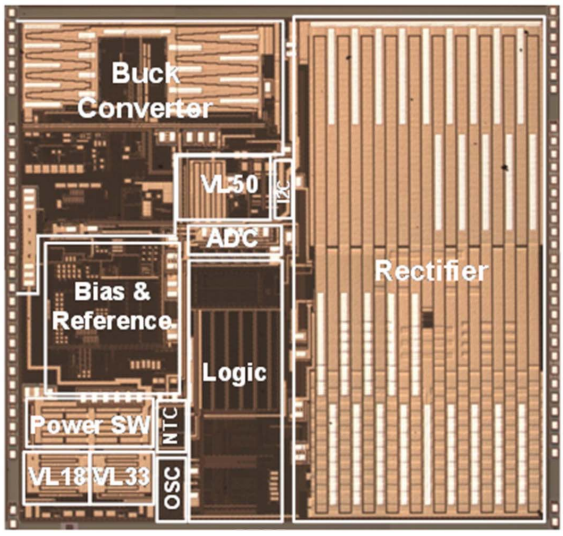


**Figure 12.9.7: Microphotograph of the implemented wireless power receiver chip.**


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