CMOS Inductor Performance Estimation using Z- and S-parameters

Maria Drakaki
Dept. of Electronics
Educational Institute of Thessaloniki
Thessaloniki, Greece
drakaki@el.teithe.gr

Alkis A. Hatzopoulos
Dept. of Electrical and Computer Engineering
Aristotle University of Thessaloniki
Thessaloniki, Greece
alkis@vergina.eng.auth.gr

Stylianos Siskos
Electronics Laboratory, Dept. of Physics
Aristotle University of Thessaloniki
Thessaloniki, Greece
siskos@physics.auth.gr

***Abstract*— A comparison is made between model parameter calculation equations of RF CMOS inductors. Model parameters can be extracted from different equations using as variables either Y-, Z-parameters depending on the circuit configuration of the inductor or S-parameters. Results are based on on-wafer RF S-parameter measurements of a fabricated inductor. Differences appear between results obtained with calculation equations based on Z- and S-parameters, extracted for a differentially driven inductor. Therefore, care must be taken by the designers when evaluating an integrated inductor performance to comprehend the technological and operating environment of the device and to choose the corresponding formulas accordingly.**

I. INTRODUCTION

Accurate device models are required for RFIC circuit design. This is especially true for RF CMOS technologies due to the low resistivity silicon substrate. Integrated inductors are basic components of RFIC circuits. Model parameters that measure the performance of integrated inductors are the inductance, series resistance, and quality factor. Parameter extraction is based on a device model, such as the nine-element model [1]. On-wafer scattering parameter measurements are necessary for device model validation. S-parameter measurements are taken using a Vector Network Analyzer along with a set of Ground-Signal-Ground (GSG) or Ground-Signal (GS) probes. De-embedded S-parameters are converted to Y- and Z-parameters in order to be used for model parameter extraction.

Depending on the inductor configuration in the circuit different calculation equations are used to extract the model parameters. An equation using the Y_{11}-parameter as a variable, as well as an equation using the input reflection coefficient, Γ_{in}, defined from single-ended S-parameters, are used when the inductor is single-ended (grounded). An equation using the differential impedance Z_{dd} [2] as a variable, as well as an equation using a differential S-parameter [3], S_{dd}, is used when the inductor is differentially driven. Differential S-parameters have been defined in [4] to be used in differential networks. In [5] the quality factor is calculated in terms of two-port S-parameters and the load reflection coefficient derived using a complex power approach.

In this work a comparison is made between the different calculation equations used in each inductor configuration in order to check their equivalency. The nine-element model for the inductor is taken as the device model for the purposes of this analysis. Results are based on de-embedded Y-, Z-, and S-parameters calculated from on-wafer S-parameter measurements taken on a test chip. Comparison between results obtained for the differentially driven inductor show differences depending on whether the equation is based on the Z_{dd} variable or the S_{dd} variable. Calculation equations using the Y_{11}-parameter or the S-parameters as variables produce the same results for the single-ended inductor. A comparison is made between different quality factor definitions including the definition in [5]. In the following a theoretical analysis of model parameter extraction methods is given in section II. In section III results extracted from experimental data with the different evaluation methods are presented, followed by an analysis of the results. Finally, conclusions are given in section IV.

II. THEORETICAL ANALYSIS

A. *Single-ended Inductor*

A general two-port network is shown in Fig. 1a. A π-type equivalent circuit shown in Fig. 1b is used to calculate the model parameters of the single-ended inductor, assuming the nine-element model as the inductor model. Since the second port is grounded in this case, the input admittance of the circuit is equal to Y_{11}.

1-4244-0921-7/07 $25.00 © 2007 IEEE.

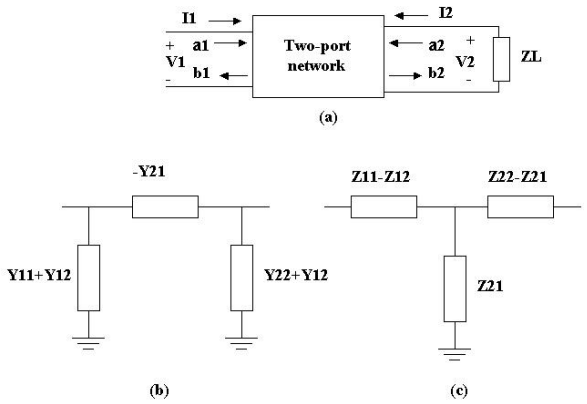

Fig. 1. (a) A general two-port network. (b) A π-type equivalent circuit. (c) A T-type equivalent circuit.

Inductance, L_{Y11}, series resistance, R_{Y11}, and quality factor, Q_{Y11} are calculated in terms of the Y_{11} parameter as

$$L_{Y11} = \frac{1}{2\pi f}\,\mathrm{imag}\left(1/Y_{11}\right). \tag{1}$$

$$R_{Y11} = \mathrm{real}\left(1/Y_{11}\right). \tag{2}$$

$$Q_{Y11} = \frac{imag\left(1/Y_{11}\right)}{real\left(1/Y_{11}\right)}. \tag{3}$$

A different parameter extraction equation can be derived using the input reflection coefficient Γ_{in}

$$\Gamma_{in} = S_{11} + \frac{S_{12}S_{21}\Gamma_L}{1 - S_{22}\Gamma_L} = S_{11} - \frac{S_{12}S_{21}}{1 + S_{22}}. \tag{4}$$

$$Z_{in,se} = Zo\,\frac{1+\Gamma_{in}}{1-\Gamma_{in}} = \frac{(1+S_{11})(1+S_{22}) - S_{12}S_{21}}{(1-S_{11})(1+S_{22}) + S_{12}S_{21}} = \frac{1}{Y_{11}} \tag{5}$$

where Γ_L is the load reflection coefficient. Γ_L=-1 for the single-ended inductor. $Z_{in,se}$ is the input impedance. The right hand side of (5) is obtained by using the conversion relation between Y- and S-parameters [6]. Z_o is the characteristic port impedance (typically 50 Ω).

The inductance, series resistance, and quality factor are then defined in terms of S-parameters as

$$L_{s,se} = \frac{1}{2\pi f}\,\mathrm{imag}(Z_{in,se}). \tag{6}$$

$$R_{s,se} = \mathrm{real}(Z_{in,se}). \tag{7}$$

$$Q_{s,se} = \frac{\mathrm{imag}(Z_{in,se})}{\mathrm{real}(Z_{in,se})}. \tag{8}$$

Taking into account (5), L_{Y11}, R_{Y11}, and Q_{Y11} are equivalent to $L_{s,se}$, $R_{s,se}$, and $Q_{s,se}$ respectively.

B. Differentially Driven Inductor

A T-type equivalent circuit for the inductor is used in this case as shown in Fig. 1c. Differential and common mode voltages (V_d, V_c) and currents (I_d, I_c) are defined from single-ended voltages and currents (Fig. 1a), as

$$V_d = V_1 - V_2,\; I_d = \frac{I_1 - I_2}{2}. \tag{9}$$

$$V_c = \frac{V_1 + V_2}{2},\; I_c = I_1 + I_2.$$

$$V_d = Z_{dc}I_c + Z_{dd}I_d. \tag{10}$$

$$V_c = Z_{cc}I_c + Z_{cd}I_d.$$

A differential impedance $Z_{dd,z}$ is defined from (10) as [7]

$$Z_{dd,z} = Z_{dd} = \left.\frac{V_d}{I_d}\right|_{I_c=0} = Z_{11} + Z_{22} - Z_{12} - Z_{21}. \tag{11}$$

Inductance, series resistance, and quality factor are then defined in terms of the differential impedance $Z_{dd,z}$ as

$$L_{Zdd,z} = \frac{1}{2\pi f}\,\mathrm{imag}(Z_{dd,z}). \tag{12}$$

$$R_{Zdd,z} = \mathrm{real}(Z_{dd,z}). \tag{13}$$

$$Q_{Zdd,z} = \frac{\mathrm{imag}(Z_{dd,z})}{\mathrm{real}(Z_{dd,z})}. \tag{14}$$

Single-ended voltages and currents have been defined in terms of incident and reflected power waves as

$$V_1 = \sqrt{Z_o}\,(a_1 + b_1),\; V_2 = \sqrt{Z_o}\,(a_2 + b_2).$$

$$I_1 = \frac{a_1 - b_1}{\sqrt{Z_o}},\; I_2 = \frac{a_2 - b_2}{\sqrt{Z_o}}. \tag{15}$$

where a_n, b_n are the incident and reflected power waves of port n, respectively.

Using (9) and (15) the condition I_c=0 in (11) is equivalent to

$$I_c = 0 \Rightarrow I_1 = -I_2 \Rightarrow a_1 + a_2 = b_1 + b_2. \tag{16}$$

Single-ended S-parameters are defined in terms of incident and reflected power waves from

$$b_1 = S_{11}a_1 + S_{12}a_2.$$

$$b_2 = S_{21}a_1 + S_{21}a_2. \tag{17}$$

Using (15), (16), and (17), the differential impedance in (11) can be written in terms of incident and reflected power waves as

$$Z_{dd,z} = Z_o\,\frac{a_1 + b_1 - a_2 - b_2}{a_1 - b_1}. \tag{18}$$

Another definition of model parameters can be derived in terms of differential S-parameters. Differential and common mode S-parameters have been defined in [4] as

$$b_d = S_{dc}a_c + S_{dd}a_d. \tag{19}$$

$$b_c = S_{cc}a_c + S_{cd}a_d.$$

where differential and common mode incident (a_d, a_c) and

reflected power waves (b_d, b_c) are defined from single-ended power waves as

$$a_c = \frac{a_1 + a_2}{\sqrt{2}}, a_d = \frac{a_1 - a_2}{\sqrt{2}}. \qquad (20)$$
$$b_c = \frac{b_1 + b_2}{\sqrt{2}}, b_d = \frac{b_1 - b_2}{\sqrt{2}}.$$

A differential S-parameter, S_{dd}, is defined from (19) as

$$S_{dd} = \left.\frac{b_d}{a_d}\right|_{a_c=0} = \left.\frac{b_2 - b_1}{a_2 - a_1}\right|_{a_c=0} = \left.\frac{b_1 - b_2}{2a_1}\right|_{a_c=0} \qquad (21)$$
$$= \frac{S_{11} + S_{22} - S_{12} - S_{21}}{2}.$$

Using (20), the condition a_c=0 in (21) is equivalent to

$$a_c = 0 \Rightarrow a_1 = -a_2. \qquad (22)$$

The right hand side in (21) has emerged taking into account (17) and (22).

A differential impedance, $Z_{dd,s}$ has been defined in terms of the differential S-parameters in [4] as

$$Z_{dd,s} = 2Z_o \frac{1 + S_{dd}}{1 - S_{dd}}. \qquad (23)$$

Using (21), (23) can be written in terms of power waves and S-parameters as

$$Z_{dd,s} = 2Z_o \frac{2a_1 + b_1 - b_2}{2a_1 - b_1 + b_2} = \qquad (24)$$
$$2Z_o \frac{2 + S_{11} + S_{22} - S_{12} - S_{12}}{2 - S_{11} - S_{22} + S_{12} + S_{21}}.$$

Inductance, series resistance, and quality factor are then defined in terms of the differential impedance $Z_{dd,s}$ from equations of the form of (12)-(14).

Comparing equations (18) and (24) in terms of power waves, it can be seen that they are not equivalent. The two definitions for the differential impedance lead to different results. They become equivalent when the conditions (16) and (22) are both valid. In that case

$$a_c = b_c = 0 \Rightarrow \left\{\begin{matrix} a_1 = -a_2 \\ b_1 = -b_2 \end{matrix}\right\} \Rightarrow \left\{\begin{matrix} V_1 = -V_2 \\ I_1 = -I_2 \end{matrix}\right\}. \qquad (25)$$

which leads to the following relation for $Z_{dd,z}$ and $Z_{dd,s}$

$$Z_{dd,s} = Z_{dd,z} = 2Z_o \frac{1 + S_{11} - S_{12}}{1 - S_{11} + S_{12}}. \qquad (26)$$

III. RESULTS AND DISCUSSION

The device under test (DUT) was a 3.75 turn square spiral inductor fabricated in AMIS 0.7 μm CMOS DM1P n-well technology. On wafer RF S-parameter measurements have been taken using a HP8510 Vector Network Analyzer and 150 μm pitch Picoprobe Ground-Signal-Ground probes in a frequency range from 1 to 15 GHz. A Line-Reflect-Match (LRM) calibration of the system performed on an impedance standard substrate calibrated the measurements up to the probe tips. An off-line calibration (de-embedding) was performed next to remove probe pad and metal interconnect line parasitic elements [8].

Figs. 2, 3, and 4 show the inductance, resistance and quality factor, respectively, calculated using the $Z_{dd,z}$, ((11)), and $Z_{dd,s}$ ((24)) differential impedances.

Fig. 5 shows quality factors for various load reflection coefficients calculated using the S-parameter based quality factor definition in [5] (eqs. (7) and (8) in [5]), the quality factor calculated using the $Z_{dd,s}$ for the differential configuration and the quality factor calculated using the $Z_{in,se}$ for the single-ended configuration.

As it is shown in Figs. 2, 3, and 4, there are differences at high frequencies of the extracted model parameters depending on whether the $Z_{dd,z}$ or $Z_{dd,s}$ differential impedance is used in the calculations. These differences are small for the DUT. Equation (16) (condition for the differential impedance $Z_{dd,z}$) implies that the same currents in magnitude (with 180° phase difference) flow to ports 1 and 2, so that there is no signal leakage to ground. The low resistivity silicon substrate causes signal leakage, an effect which is more obvious at high frequencies, as seen from Figs. 2, 3, and 4. This condition must be used with care, since it is mainly valid for SOI or GaAs technologies.

Fig. 5 shows that the quality factor calculated using the differential impedance is higher than the quality factors calculated for various load reflection coefficients using the definition in [5]. The quality factor for Γ_L=-1 (single-ended inductor condition) in [5] and the quality factor extracted using (8) for the single-ended inductor are equivalent. In [5] the quality factor has been derived using a complex power approach in terms of the two-port S-parameters and the load reflection coefficient. Fig. 5 shows that there is an

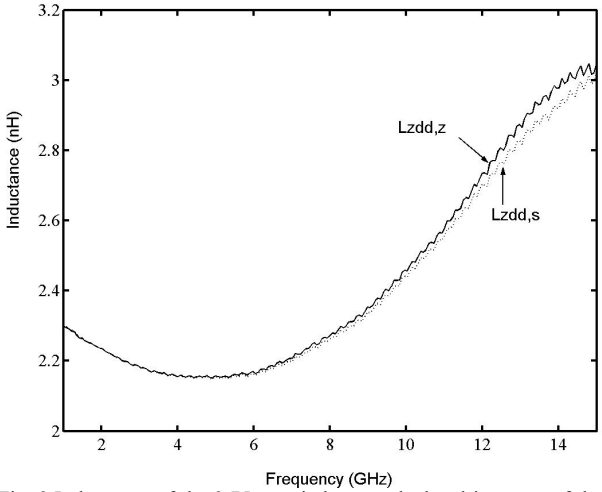

Fig. 2.Inductance of the 3.75 turn inductor calculated in terms of the $Z_{dd,z}$ (eq. (11)) and $Z_{dd,s}$ (eq. (24)) differential impedances.

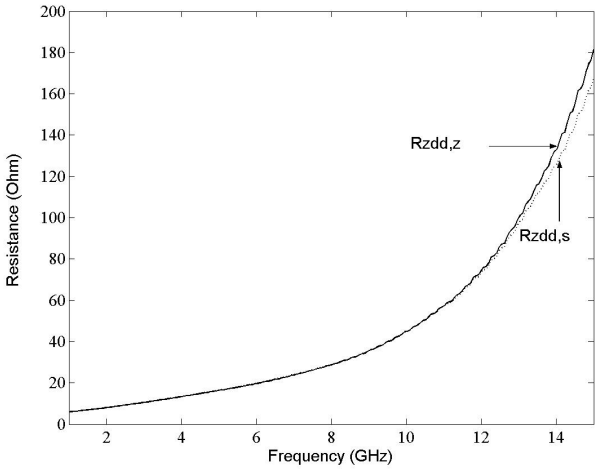

Fig. 3. Series resistance of the 3.75 turn inductor calculated in terms of the $Z_{dd,z}$ (eq. (11)) and $Z_{dd,s}$ (eq. (24)) differential impedances.

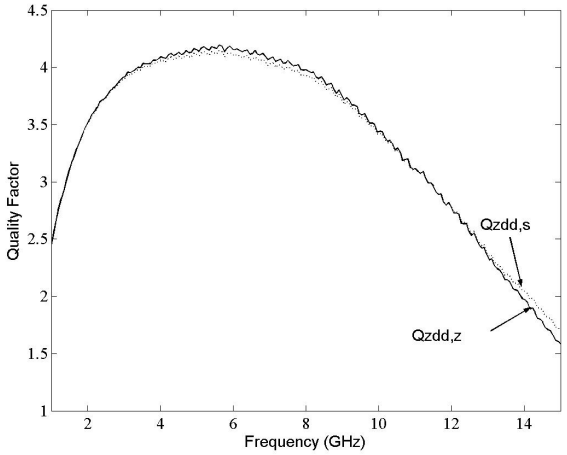

Fig. 4. Quality factor of the 3.75 turn inductor calculated in terms of the $Z_{dd,z}$. (eq. (11)) and $Z_{dd,s}$ (eq. (24)) differential impedances.

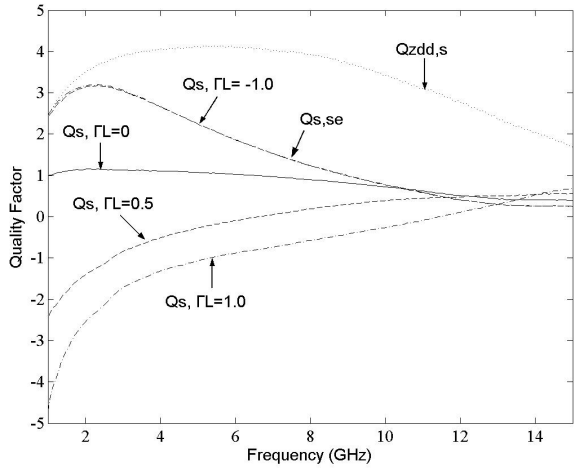

Fig. 5. Quality factor of the DUT calculated using the definition in [5] in terms of the load reflection coefficient (eqs. (7), (8) in [5]), the differential impedance $Z_{dd,s}$ (eq. (24)), and the single-ended impedance $Z_{in,se}$ (eq. 8)).

overestimation of the quality factor derived using the differential impedance as a variable whereas the same results are obtained for the quality factor derived using the definition in [5] and the single-ended impedance $Z_{in,se}$. The derivation of the quality factor definition in [5] is based on a one-port model, therefore the results shown for various load reflection coefficients must be interpreted with care.

IV. CONCLUSIONS

This paper presents a comparative evaluation of various performance estimations of integrated CMOS inductors. The calculation of L, R and Q for a specific fabricated inductor based on the same measured S-parameters is assessed, utilizing single-ended as well as differential models.

The calculation formulas utilized for single-ended inductor configuration (e.g. eq. (8) based on (5) and eqs. (7), (8) of [5] for Γ_L=-1) give the same results, as it can be observed, for example, for the quality factor Q in Fig. 5. However, small differences emerge when differential configuration is considered and Eq. (11) or (24) is applied. The condition under which the differential $Z_{dd,z}$ is derived is mainly valid for SOI or GaAs technologies or at low frequencies for CMOS technology. The quality factor calculated using the differential impedance $Z_{dd,s}$ or $Z_{dd,z}$ is higher than the quality factors calculated for various load reflection coefficients using the definition in [5].

Therefore, care must be taken by the designers when evaluating an integrated inductor performance to comprehend the technological and operating environment of the device and to choose the corresponding formulas accordingly.

REFERENCES

[1] C. P. Yue and S. Wong, "On chip spiral inductors with patterned ground shields for si-based RF ICs," in IEEE J. of Solid State Circuits, vol. 33, no. 5, pp. 743-752, May 1998.

[2] M. Danesh, J. Long, R. Hadaway, and D. Harame, "A Q-Factor Enhancement Technique for MMIC Inductors in Silicon Technology," in IEEE International Microwave and RFIC Symposium, Proceedings, pp. 217-220, June 1998.

[3] M. Danesh and J. R. Long, "Differentially driven symmetric microstrip inductors," in IEEE Trans. Microwave Theory Tech., vol. 50, no. 1, pp. 332-341, Jan. 2002.

[4] D. E. Bockelman, W. R. Eisenstadt, "Combined differential and common-mode scattering parameters: theory and simulation," in IEEE Trans. Microwave Theory Tech., vol. 43, no. 7, pp. 1530-1539, Jul. 1995.

[5] T-S Horng, K-C Peng, J-K Jau, and Y-S Tsai, "S-parameter formulation of quality factor in generalized two-port configuration," in IEEE Trans. Microwave Theory Tech., vol. 51, no. 11, pp. 2197-2202, Nov. 2003.

[6] D. M. Pozar, " Microwave Engineering," 2nd ed. New York:Wiley, 1997.

[7] M. Danesh, J. R. Long, R. Hadaway, and D. Harame, "A Q-factor enhancement technique for MMIC inductors," in Proc. IEEE MTTS and RFIC Symp., pp. 217-220, Apr. 1998.

[8] A. Hatzopoulos, S. Stefanou, G. Gielen, D. Schreurs, "Impact of parameter extraction methods on integrated inductor design," Proc. IEEE ISCAS Int. Symp. Circuits Systems, ISCAS 2006, May 2006, Greece.