UiO : Department of Informatics
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Wireless Power Receiving Unit

Analysis, design and implementation of inductive power receiving unit for wireless circuits

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Part I

Introduction and Background

Chapter 1

Introduction

1.1 Motivation

We start with the technology development trend in micorelectronics. The progress of different aspects of technology is discussed and compared with power/battery development. We end the chapter concluding the need for going cordless for suppling power for microelectronics.

1.1.1 Technology Trend

Size and weight : Lighter and tighter

Reduction in size and weight has been most dramatic that in course of some decades miniaturisation trend went from a room-sized fixed electronic into a wearable device. Most important milestone contributing for lighter and tighter devices is development of transistor in 1950s replacing large and bulky vacuum tubes, and development first IC in 1965 making it possible to integrated hundreds of transistors on a single silicon substrate of some square mm. Since then as stated by Moorse's law, IC size is continuously shrinking. A typical modern IC now consists of billions of transistors of some tens of nm feature size.

Operation: Multi-functional and fast

On the contrary to shrinking device size, integrated functionality and device speed is increasing proportionally. The introduction of SoCs created of new dawn of multi-functionality IC by integrating many electronic components and/or systems on a single silicon substrate. Similarly multi-core CPU with parallel programmed instruction significantly increased work payload as stated by Amdahl's law. Similarly recent developments in IoT has introduced whole new dimension on multifunctionality by connecting many devices to a same local network or the internet[2].

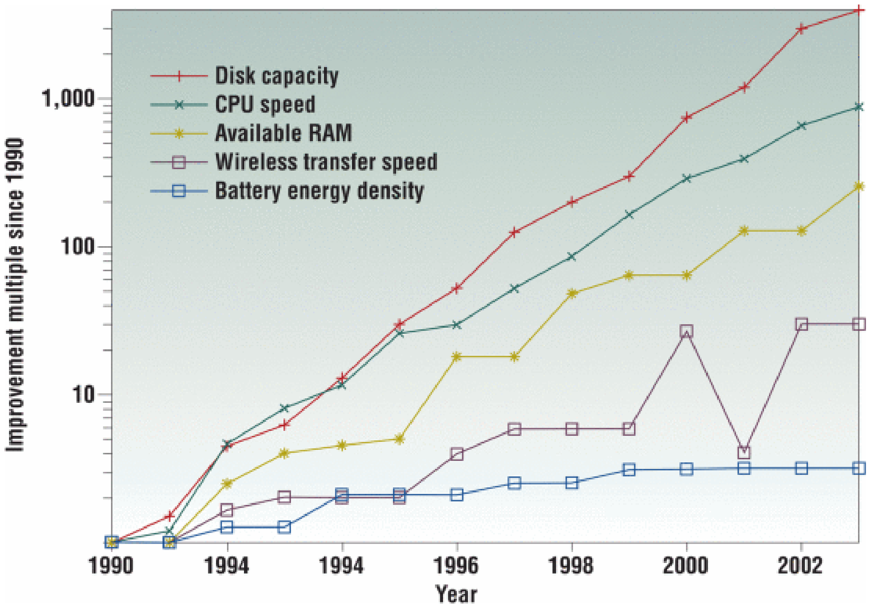


Figure 1.1: Mobile performance development trend [1]

Power consumption: Low-power

In terms of power consumption, though power density has increased due to increased transistor density and speed, power consumption per transistor and energy per operation, EOP, has significantly reduced. It is due to gradual shrinking in feature size and decrease in supply voltage. Similarly there has been a lot progress in LP design introducing new power optimal design techniques both at logic/circuit level and architecture level. Lately run time power optimisation technique by tracing realtime work load like dynamic voltage scaling and switching between different operation modes (sleep, nap, doze and active) have been popularly used to reduce power consumption[3].

Power supply: Cut the cord

In spite of dramatic technological advancement, battery technology has not evolve equally as good, see figure 1.1. It is not like there has been no progress in battery technology at all. There has been a lot improvements like increased volumetric energy density thereby reducing size, increased gravimetric energy density thereby reducing weight, reduced self discharge thereby increasing life time and increased charged cycle thereby increasing reuse.[CITE]. Today Li-ion has better choice for powering devices because of it better combined above mentioned characteristics and hence used excessively in portable and wearable devices.

But use of battery in todays' portable and wearable devices is constraining the overall developement of devices [CITE]. Batteries contribute significant proportion of total weight and size of the device. They supply limited power which means require regular recharge and in the long run need replacement. During recharge either device or batterly has to be physically connected to power outlet.

A power source technology with high power density which perpetually and wirelessly power devices could eliminate all the above problems and challenges mentioned above. But how far have we gone to achieve this? In the next chapter, we will discussed the techniques of energy harvesting and wireless power transfer studied and implemented so far. Bluetooth Low Energy, BLE is taken as a reference device to drive and a power harvesting circuit is designed and implememted for BLE.

1.2 Thesis outline

all chapter summary

Chapter 2

Background

2.1 Energy Harvesting

In this chapter, we discuss the options to elimanate or minimise the bottlenecks of battery used in portable and wearbale devices. We start with energy harvesting techniques and then wireless power transfer techniques.

There has been success in harvesting low power from ambient sources and a lot of effort and resources is being used for harvesting high power. As discussed earlier the technological advancement has given us low power electronics. These LP devices can now be powered solely by harvested energy, eventually making battery-less wirelessly powered electronic device a reality.

Energy harvesting system generally constitutes of energy source, transducer and power conditioning unit as shown in figure 2.1. Energy source can either be artificial like human walking or natural like sunlight. Transducer are devices which converts the energy from source which may be to electrical energy. And power conditioning unit process the harvested energy so that it can be used either to directly power a load or to store the energy.

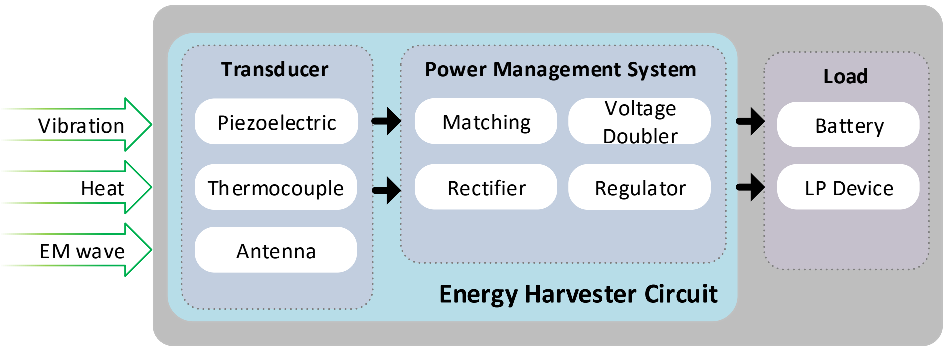


Figure 2.1: Functional block diagram of energy harvesting system

Depending upon the type of energy harvested from the surrounding environment, energy harvesting devices can be broadly classified into kinetic, electromagnetic and thermal energy sources[4]. These are briefly discussed below.

2.1.1 Kinetic energy harvesting

In kinetic energy harvesting, kinetic energy due to mechanical deformation of transducer is converted into electrical energy. Piezoelectrical material is good example of transducer for kinetic energy harvesting. Piezoelectrical materials are those which exhibit piezoelectric effect: when subjected to mechanical strain, it generates electrical charge proportional to applied strain. Strain is applied with either compression, slap or bending of the material.

2.1.2 Harvesting from Radiation

Electromagnetic energy harvesting is extraction of useful energy from ambient light or RF radiation. Solar energy harvesting is the most popular and widely successful EM energy harvesting for large scale energy generation. It makes use of semiconductor device called solar cells as transducer. These transducer converts incident light energy to electric energy due to photoelectric effect: when light is incident on semiconductor, electrons are emitted from the surface. Its application ranges from LP wrist watch to grid of photovoltaic system. The other popular example is harvesting from RF radiation, which are available almost everywhere in modern cities, to power RFIDs. In this technique, antenna or rectenna are used as transducer. However harvesting from RF radiation has been limited to very low power only.

2.1.3 Thermal energy harvesting

Similarly in thermal energy harvesting, thermal energy from any source in the environment is converted to useful electric energy. Thermopile is an example of thermal energy harvesting using thermocouples in series as transducer. Thermocouple is a electric device with two different conductors forming junctions. A thermocouple generates voltage proportional to temperature between junctions, known as Seeback effect. Connecting thermocouples in series increased the harvested voltage as in thermopile.

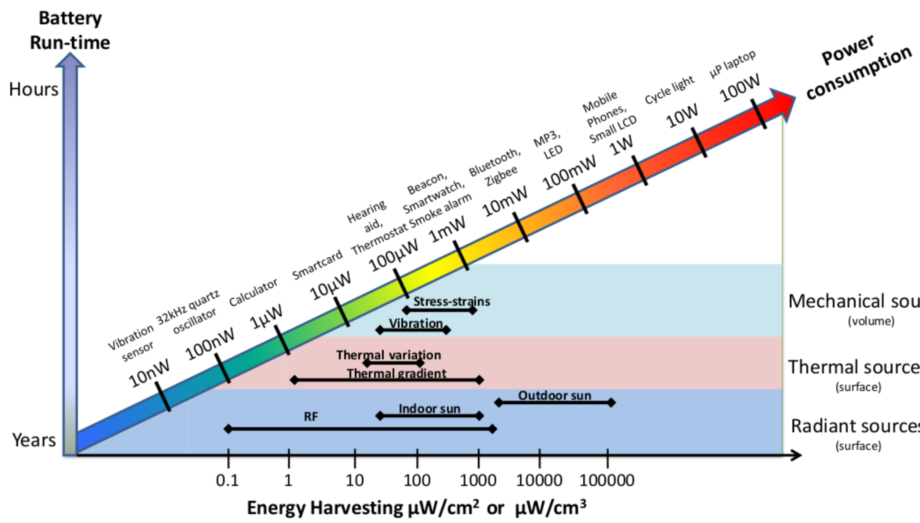


Figure 2.2: Power density of energy sources and consumption of electronic devices [5]

Figure 2.2 shows power density of different energy sources and power consumption of electronic devices. It is seem that the above discussed energy sources have a low power density which means very low power and some low power micro-electronic devices only have the privilege of integrating energy harvesting techniques so far. For most of the devices, the harvested power is not high enough to drive them yet. This means perpetual high density energy source is yet not realisiable for most of the devices. But what about wireless transfer of alreadry available power? We will discuss it ahead.

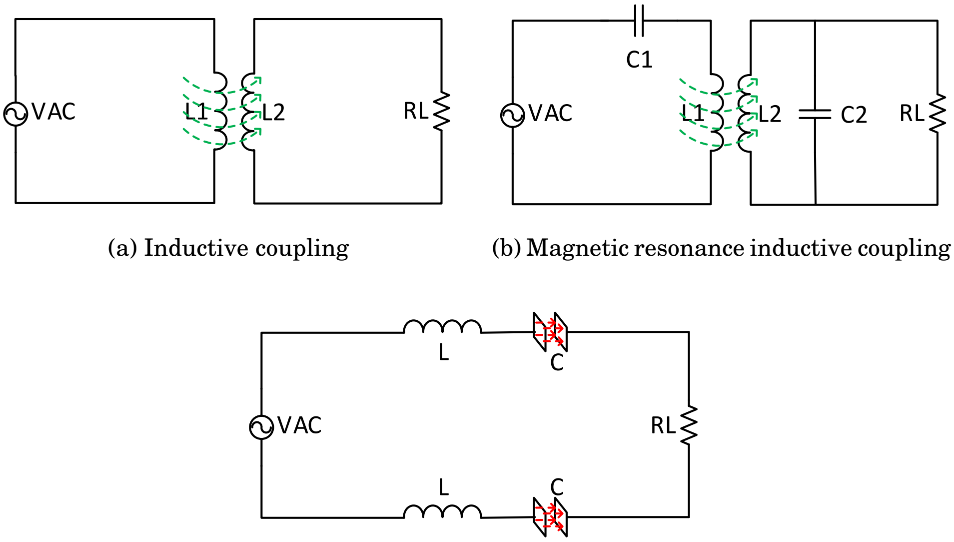
2.2 Wireless Power Transfer

As discussed earlier since the evolution of battery technology is not at par with rest of the development in microelectronic devices and energy harvesting techniques from natural sources has not yet evolved to high power density, wireless power transfer is by far best option to minimise challenges in battery powered devices.

Wireless power transfer is technique of cordlessly transferring electric energy across a air gap either to drive a load or to charge a battery. It eliminates the need of phycical power cables to recharge battery. and in the best case completely remove the battery. Wireless power transfer methods implemented today can be broadly classified into radiative and non-radiative power transfer on the basis of transfer distance which can be further sub-classified on the basis of power transfer principle [6] as discussed below.

2.2.1 Non-radiative wireless power transfer

Non radiative method of wireless power transfer based on magnetic field coupling between two coils within the distance of coil dimension. Since magnetic field diminishes rapidly after distance greater than radius of coil, assuming that distance is less than near field and far field boundary, $\lambda/2\pi$ [7, pp. 63], better coupling and hence power transfer can happen only within this short distance, and thus it is also called near field power transfer. Near field also means that radiative EM wave is not yet fully created and hence the name non-radiative WPT. As energy transfer in magnetic field is non radiative, it is safe even to transfer higher power as there is no RF exposure. This is one of the main reason of its widespread application today.



(a) Inductive coupling

(b) Magnetic resonance inductive coupling

(c) Capacitive coupling

Figure 2.3: Near-field coupling models

Inductive power transfer, IPT

IPT is based on electromagnetic induction between two coils. Electric energy is transferred by coupling of magnetic field from the primary to secondary coil. As stated by Faraday law of induction, alternating current flowing in primary coil generates varying magnetic filed which is when coupled with secondary coil includes voltage/current across the secondary coil.

In such conventional inductive coupling, larger air gap and difficulty in perfect alignment between the coils contribute to weak coupling, which directly translates into poor power transfer efficiency. This is why it is mostly used in LP devices and for short range in tens of mm transfer like RFIDs.

Magnetic resonance power transfer

The principle of magnetic resonance power transfer is same as IPT but with strong coupling between the coils. Instead of simple coil as in IPT, resonance is created at both primary and secondary coil at the same operating frequency. Such resonant IPT is often concisely called as Witricity, for wireless electricity and is less affected by coil misalignment and physical distance compared to conventional IPT [8]. A very key application of resonant IPT is that it can be used to simultaneously transfer/charge multiple power receivers from a single large source coil [9].

Because of it strong coupling between the coils, it can effectively transfer power for mid range in tens of cm. It is mostly used in wireless charging of medical implants and consumer electronics.

Capacitive power transfer, CPT

In capacitive power transfer, power transfer is done through capacitive coupling, use of E-field, between sending and receiving plates as transferring interface. For low power transfer, it is seen effective over IPT because of lower cost, smaller size and no shielding for EMI. However for higher power transfer is limited due to requirement of larger plate area and very close coupling [10].

2.2.2 Radiative wireless power transfer

Radiative power transfer used RF EM wave as a medium to deliver power. In contrary to near field, power is transferred through E-field of EM wave. The E-field can only develop after $\lambda/2\pi$ distance, at far field region, from the source [7, pp. 112], and energy can only be harvested in this far field region, it is called far field power transfer. However as EM wave is radiative and high power RF exposure has safety concerns on human.

Non-directive and directive radiative WPT

Radiative power transfer can be divided into directive and non-directive radiative power transfer. Non-directive power transfer is same as discussed in EM energy harvesting, where energy is harvested from isotropically radiated RF wave in the surrounding. Whereas in directive power transfer, dedicated transmitter antenna/antenna array is used to transmit EM wave to a particular direction of receiver antenna location. This is point to point far field transfer technique is also called energy beam-forming and has better transfer efficiency than non-directive method.

Health concerns as governed by FCC and IEEE safety regulation policy on human exposure has limited its used to low power harvesting over longer distance using RF wave. But, as RF wave is also information carrier wave in wireless communication, its capacity to transmit both data and power simultaneously is expected to introduce new application in wireless communication field [6].

2.2.3 WPT Applications

It is seen today that IPT and magnetic resonance IPT are mostly used because of easier implementation, lower cost, wide range power transfer capability. For high power transfer in order of kilowatt, IPT is mostly used in the field of industrial automation like automated material handling and industrial micro-robots and automotive like electric vehicle charging. Similarly both IPT and magnetic resonance IPT are used for transferring power medium power up-to tens of watt. Their typical uses have been in charging battery in medical equipments and consumers electronics. In case of microelectronics devices like medical implants, body sensors, pacemaker etc, magnetic resonance IPT is mostly used both to charge a battery or directly drive the device.

In context of radiative power transfer, non-directive technique is mostly used in low power sensors and implants. Because of the low power requirement, mostly omnipresent RF signals are used to harvest energy. This technique has been used in both perpetually supplying power like in body sensor which continuously monitor some activity or sporadically supplying power like in RFID and body implants which work only when required. [CITE] reports future application of microwave power transfer can be in SPS (Solar Power Satellite) system and SHARP (Stationary High Altitude Relay Platform). SPS uses satellite for harvesting solar energy in space and transfer that power to earth. Similarly SHARP is stationary charging station for unmanned aerial vehicles in stratosphere region by beaming power from earth.

2.2.4 Charger Standards

When wireless charging was introduced into consumer daily appliances, it was quickly realised the need of standard design protocols to maintain uniformity and avoid confusion for the manufacturers. Here are some mostly used standards in the market. All commercial standards discussed below use both IPT and resonant IPT techniques for char-

(a) Qualcomm EV charger

(b) Qualcomm mobile phone charger with foreign object detection feature

(c) IDT concept of wireless charging of bionic devices

Figure 2.4: Commercial application of wireless power transfer

ging, and have two elements: transmitter for transferring power and receiver device usually integrated into mobile, handheld or wearable devices. Both the transmitter and the receiver use the same control and management protocol in order to detect compatible electronic devices, exchange charging state information and control charging process.

Qi

Qi standard was introduced by Wireless Power Consortium in August 2008. It has standardised two categories of chargers: low power charger for mobile and music players and medium power charger. The power transfer was based on IPT and now is operating with magnetic resonance IPT too. Qi standard allow transmitter/charger to be either single fixed coil, single moving coil or array of coils. The transmitter coil type determines determines the positioning of the receiver, either guided or free. Qi charger also have foreign object detection feature [11]. Qi uses the same frequency for communication and power transfer, 80-300 KHz [12].

Figure 2.5: Qi

A4WP

A4WP is acronym for Alliance for Alliance for Wireless Power which has introduced another independent wireless charging protocol. It uses magnetic resonance IPT technique for power transfer. The main differences between A4WP from Qi are multiple device charging from a single charger, also called power transmitting unit, PTU and longer charging range. Similarly there are different category of PTUs from 1 to 5, most of them still on roadmap and supports wireless charging from low power to high power. A4WP used different frequency band for communication and power transfer, which are 2.4 GHz and 6.78 MHz respectively [13].

AirFuel Alliance

AirFuel Alliance is newly crated wireless charging standard buy merging Alliance for Alliance for Wireless Power, A4WP and Power Matters Alliance, PMA in 2015 with backing of major device manufacturers [14]. Like A4WP, PMA was IPT based independent wireless charging standard. AirFuel Alliance is believed to fight the market dominance of Qi standard. AirFuel is expecting to expand charging standard beyond consumer electronics to industrial, medical and military applications

[15].

2.3 This project

As mentioned in the last chapter, a typical microelectronics system, BLE, used extensively in all portable and wearable is taken as a reference load for this project. It requires 10 mA current from a supply of 1.8 V to drive BLE system. The purpose of this work will be to make a wireless power transfer system for cordlessly driving BLE or charging BLE battery. The target specification for this work is listed in table 2.1.

Figure 2.6: AirFuel

Table 2.1: Target specifications

Technology	TSMC 90nm 9M-1P
Chip area	TBA mm^2
Input AC voltage	2.5 Vp
Operating frequency	13.56 MHz
Maximum load	10 mA
Output DC voltage	1.8 V

Figure 2.7 is the functional block diagram of proposed implementation of wireless power transfer in this work. From the discussion in wireless power transfer section, it is seen that IPT is the best option for being mature, easy and safe implementation. Since tuning the IPT transfer link at the operating frequency increases the transfer effieiency, magnetic resonance link is designed for this work. The antennas are designed with the specifications provided by NORDIC. The power management system includes rectifier, LDO and reference and bias circuit. The biasing and reference circuit is designed solely for learning the design technique without much effort on the accuracy of the generated biases and references. So externally supplied bias and reference will be the secondary option.

The chapter ahead discusses the design, analysis and implementation of the functional blocks in figure 2.7 starting with rectifier. The physics behiend each block is less discussed, however the design choices and reasoning of choices will be clearly stated.

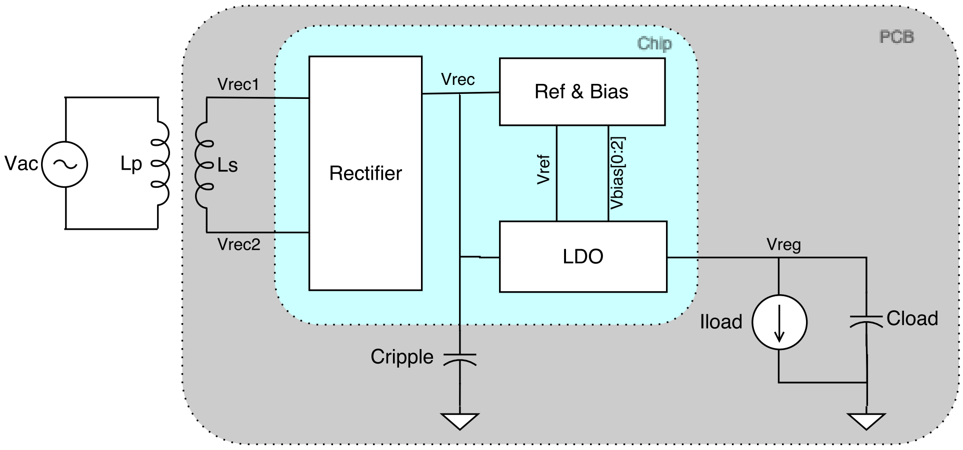


Figure 2.7: Block diagram of complete design

Part II

Component Design and Analysis

Chapter 3

Rectifier

3.1 Introduction

The most basic rectifier is conventional full wave bridge structure where the diodes are replaced by the diode connected MOS. devices in CMOS. technology. This topology though being simple to implement, has a major drawback. It requires at least twice the Vtn of a MOS device as there are two diode connected MOSes in the conduction path for each cycle of the input signal.

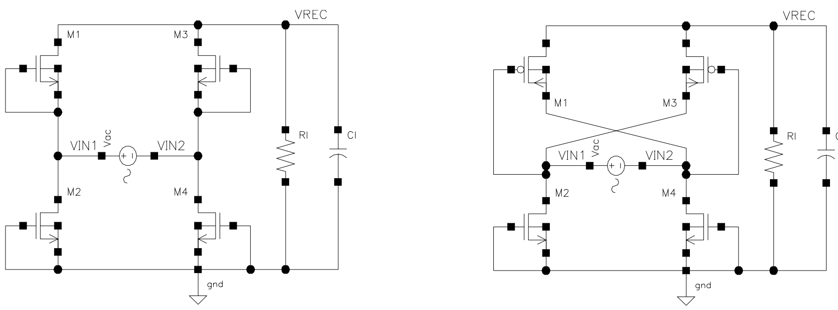
Gate cross coupled and fully gate cross coupled topologies are improvements over conventional full wave rectifier. In gate cross coupled rectifier, two diodes of conventional rectifier is replaced by two gate cross coupled MOSes working as switches where the voltage drop for every cycle is reduced to one threshold voltage. Similarly, in the fully gate cross coupled rectifier, all diodes are replaced by switches and hence the voltage drop is further reduced to twice the conduction drop only for every cycle. Even though this topology has least voltage drop, it suffers from the problem of reverse charge leakage because when the input ac amplitude is less than the output rectified voltage and the conducting pass devices are on simultaneously, current flows backward from output to input.

All the above discussed topology suffer from either large voltage drop or large power loss because of which their use are limited in low power and low voltage devices. The popular techniques for higher efficiency are using gate cross coupled rectifier along with passive or active circuitry for controlling other two pass devices. In passive rectifier, additional circuitry including bootstrap capacitor are used to reduce or eliminate threshold voltage one of which is discussed in this paper [16]. However, use of on-chip bootstrap capacitors limits it use where chip area and speed is of importance. On the other hand, in active rectifier, active circuitry is used control pass devices. The use of active circuitry increase both voltage conversion efficiency (VCE) and power conversion efficiency (PCE) because the pass devices are made to conduct in linear region and hence less conduction drop, and reverse current flow can be completely eliminated and hence less power loss. However active rectifier is not problem free either. The major issue is starting of the active circuit as there is no regulated supply at the start up.

3.2 Design

In this project, active rectifier is chosen, primarily for better VCE and PCE and secondarily to avoid the use large on chip capacitors. [17] and [18] have discussed same active rectifier topology with a slight difference in active circuitry. [17] has implemented comparator with compensating the delay of comparator's output falling whereas [18] has implemented comparator with compensating both the falling and the rising delay of comparator's output in expense of added circuit complexity and power consumption. [17] has been used here for its simple design.

Figure 3.1a, 3.1b and 3.2 is the CMOS implementation of conventional full wave bridge rectifier, gate cross coupled rectifier and proposed active rectifier in [17]. The problem with 3.1a and 3.1b has already been briefly mentioned above. Though 3.1b is significantly improvement over 3.1a , it is still not a favourable topology with respect to the design technology chosen. In the gate cross couple rectifier of 3.1b, the cross coupled pMOSes act as switches, so the only voltage drop across them is conduction drop due to channel resistance. However the other two nMOSes are diode connected, so they have at least Vtn drop across them which means $Vac \geq Vdc + Vtn$ for conduction.



(a) Conventional full wave bridge rectifier (b) Gate cross coupled full wave rectifier

Figure 3.1: Rectifier topologies: conventional and gate cross coupled

The proposed active circuit in 3.2 is improvement over 3.1b which eliminates Vtn drop required for conduction by replacing diode connected nMOS with devices controlled by active circuit as shown in figure 3.3. The active circuit is a four input comparator that turns on nMOSes fast when Vac > Vdc and turns off fast to avoid flow of current.

For the illustration of operation of comparator, consider the case when $Vin1 > Vin2$ i.e. $Vin1 > 0$ and $Vin2 < 0$. During this half cycle, comparator $D1$ output is low and turns off $Mn2$ and also, $Mp1$ is reversed biased and hence there is no path to flow current along $Mn2$ and $Mp1$. For simplicity, assume $Vac = Vin1 - Vin2$. When Vac reaches Vtp, $Mp3$ turns on which shorts $Vin1$ to $Vrec$. When $Vac > Vrec$, $D2$ output goes high, which turns on $Mn4$ and starts the conduction path for the first half cycle and starts charging Cl. When Vac reaches maximum, it starts to decrease and at $Vac < Vrec$, conduction stops as output of $D2$ is low and $Mn4$ is off. As Vac further decreases to below Vtp, $Mp3$ if off too. This way rectifier in 3.2 conducts during positive half cycle eliminating the Vtn drop seen in 3.1b. Now the only drop is the conduction drop due to channel resistance of two pass devices along the conduction path. This drop is much less because during conduction both the device are operating in the linear region with small resistance. The operation is similar for $Vin2 > Vin1$ where $Mn4$ and $Mp3$ are off and $Mn2$ and $Mp1$ conduct to charge Cl.

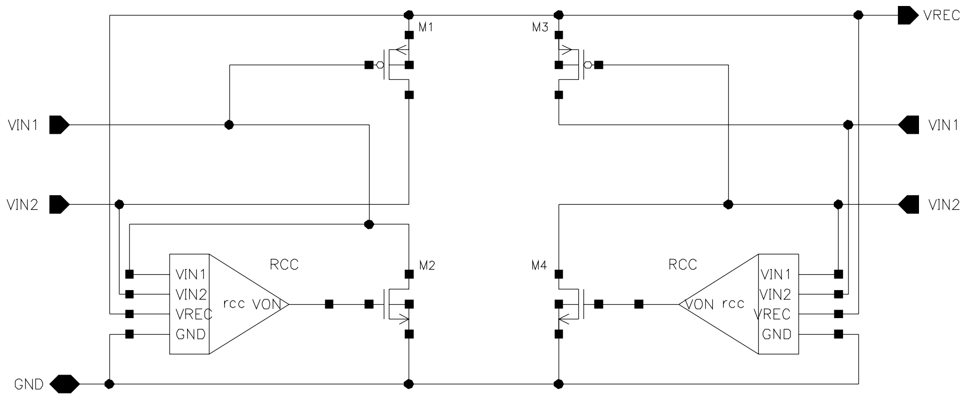


Figure 3.2: Gate cross coupled full wave active rectifer]

Figure 3.3 is the implementation of four input comparator $D2$ used in 3.2 as proposed in [17]. It is designed to self power and bias because no steady state supply is available at start up. $M1$, $M2$ and $M7$ monitors voltage across $Mn4$ i.e $Vin2 - Vgnd$ and $M3$, $M4$ and $M8$ monitors voltage across $Mp3$ ie $Vin1 - Vrec$. So when $Vin1 - Vrec > Vin2 - Vgnd$ which means $Vac > Vrec$, output of $D2$ is high and turns on $Mn4$ instantly. But when $Vac < Vrec$, the output of comparator is delayed to fall which causes $Mn4$ to conduct in reverse direction leading to significant reduction in power delivered to load. $M9$ is introduced in order to overcome this problem which adds offset currents to increase Van and Vpn faster, causing the output to decrease faster and turns off $Mn4$ before $Vac < Vrec$. This reverse current control technique compensates the comparator delay and increases the power efficiency of the rectifier.

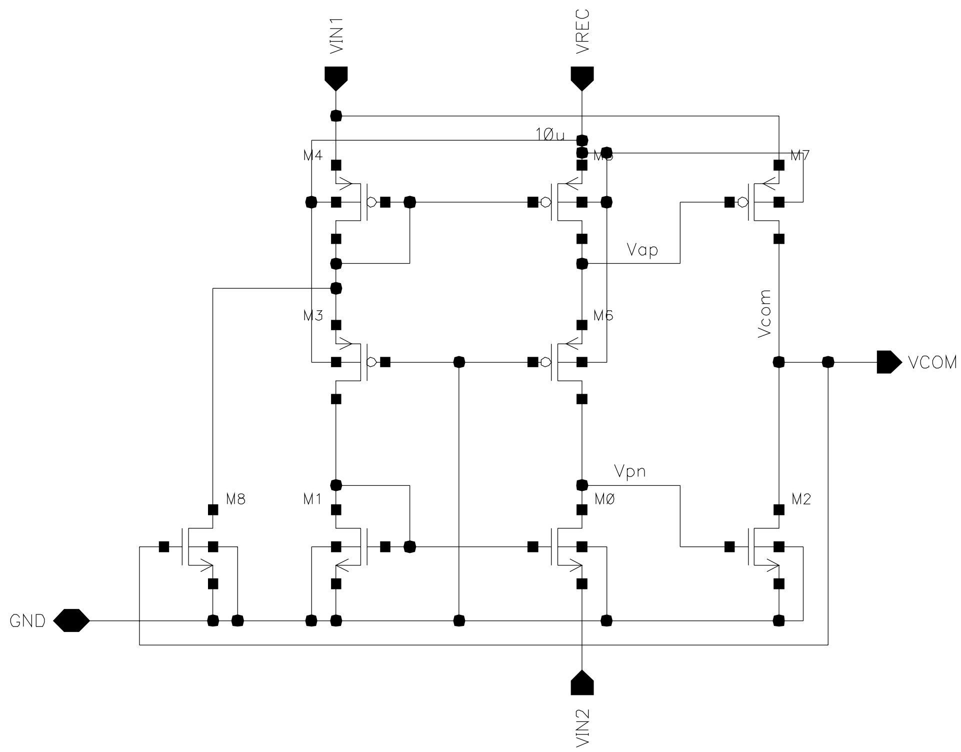


Figure 3.3: Comparator circuit, RCC

The design parameters for the rectifier is listed in table 3.1. The dimensions of the pass devices are first hand calculated by using square law current equation and devices parameters values given in the technology documents, and later optimised with simulation tool in order to make the rectifier to deliver the required current. Since nMOS does not have to have same device size as pMOS to deliver same current, optimal size ratio equation from [19] is used to find nMOS pass devices sizes. Thought maximum load for this work is 10 mA, It is always simulated with 1 mA extra load. This extra current is to account for the fact that RCC is self powered and LDO which will follow this rectifier will be powered by $Vrec$. Similarly, the value of ripple rejection capacitor is chosen 100nF. This size of filter capacitor is calculated from capacitor current-voltage relationship with the assumption of keeping peak to peak ripple voltage below 5 mV to deliver 11 mA current.

Table 3.1: Rectifier design parameters

Wn/Ln, Wp/Lp	720um/280nm, 1.2mm/280nm
Rectifier area	TBA mm^2
Operating frequency	13.56 MHz
Input ac magnitude	2.5 Vp
Load current	11 mA
Ripple rejection capacitor	100 nF

3.3 Simulation result

3.3.1 Transient performance

Figure 3.4 is the test bench setup for simulation of the rectifier. Figure 3.5 show the simulation results showing voltages at the input ac and output rectified DC voltages and current through rectifying MOSes. These waveforms clearly follows the working principle discussed above. Two important observations can be made from plots. First, the rectified output $Vrec$ is 2.2 V for Vpp ac input of 2.5 V for driving which means the voltage loss has been significantly reduced and the loss of around 300 mV yields to the conduction loss due the channel resistance. Secondly, the reverse current from output to input has been effectively eliminated as there is only positive current flowing to the load when all conducting devices are on.

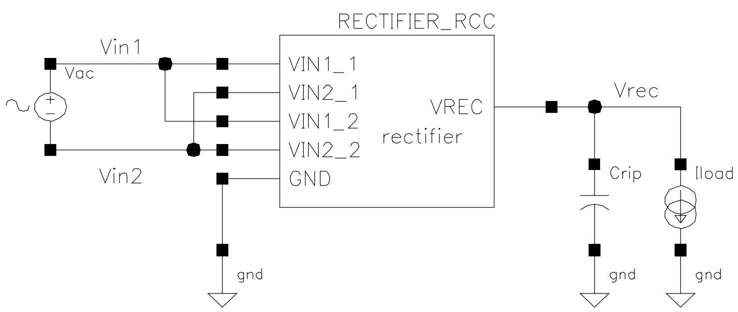


Figure 3.4: Testbench for rectifier

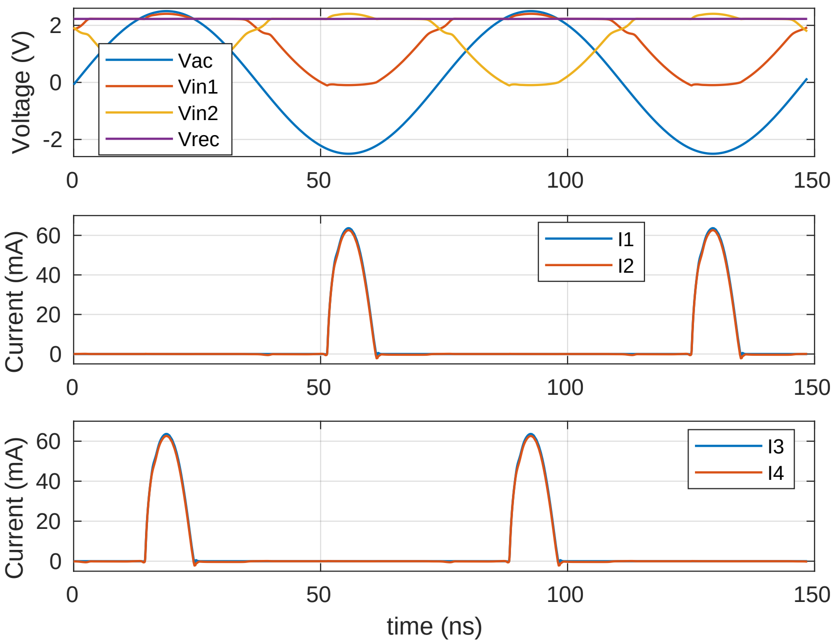


Figure 3.5: Voltage and current waveforms of the rectifier

Figure 3.6 presents both pre and post layout results of input voltages, $Vin1$ and $Vin2$ and output voltage, $Vrec$, for one cycle of ac input. The closer view of rectified output is shown in figure 3.7. The voltage drop of about 60 mV in layout result is accounted for the voltage drop due to the resistance of high current conduction path.

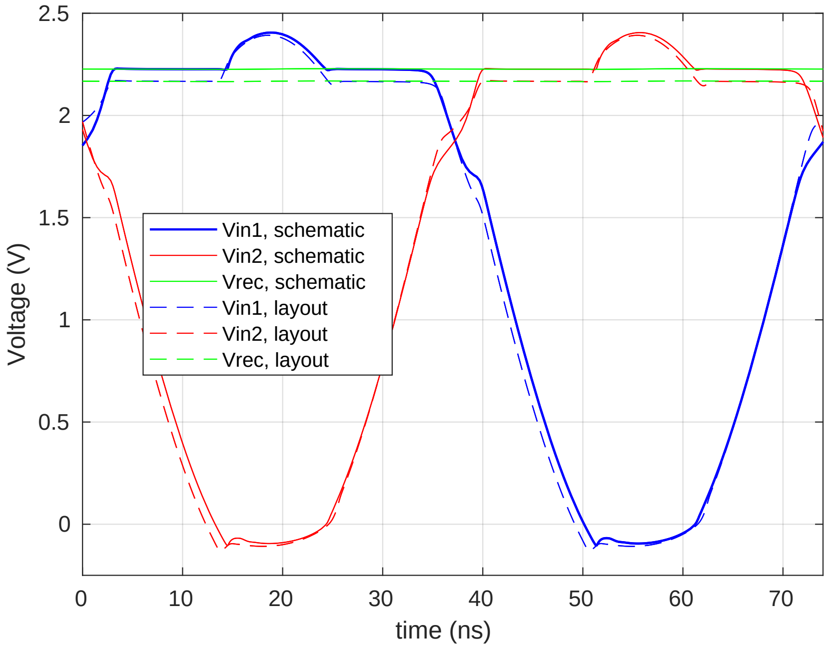


Figure 3.6: Voltages waveform for pre and post layout

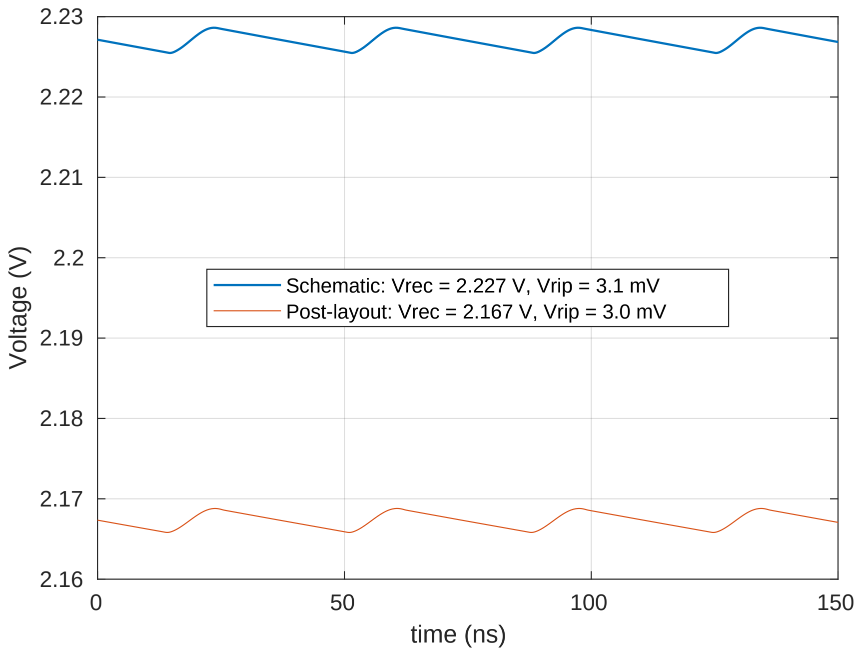


Figure 3.7: Rectified DC output for pre and post layout

3.3.2 DC performance

Similarly, figure 3.8 shows PCE, ratio of powered delivered to load to average power from the source and VCE, ratio of rectified DC, $Vrec$ to peak ac input, $|Vac|$ with respect to magnitude peak ac input signal. $|Vac|$ is gradually increased in peak magnitude in step of 50 mV and VCE and PCE is calculated for every step. The plot shows both PCE and VCE are very less for input ac amplitude less then 1.8 V. It can be explained by the fact that required bias current and gate drive voltage for RCC circuit are not achieved for smaller input. [INCLUDE POST LAYOUT RESULT TOO]

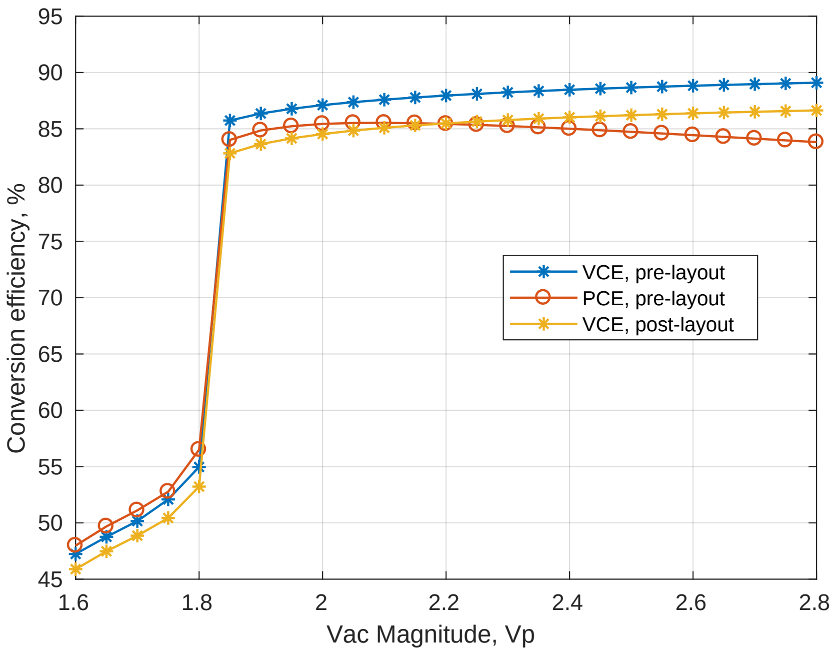


Figure 3.8: Voltage and power conversion efficiency

Table 3.2 comparatively summarises performance for pre and post layout result of the design. The layout design is attached in appendix. The layout is made symmetrical with four inputs, as seen in test bench figure 3.4, instead of two. This is done to make the current conducting path equal which result in equal drop in voltage when it reaches the rectifying MOSes. Simialarly the paths from the pad to the recitifier inputs are mask blocked for random metal fill to avoid inter layer coupling [WHY???]. The high current conduction routes are designed with wide parallel path of many higher level metal layers for reducing resistance in conduction path.

Table 3.2: Rectifier performance summary

	Schematic	**Post-layout**
Rectified DC	2.23 V	2.17 V
Ripple Vpp	3.1 mV	3 mV
Peak diode current	63.7 mA	-
PCE	84.5 %	-
VCE	88.6 %	86.2 %

Chapter 4

Low Dropout Regulator

4.1 Introduction

Voltage regulator follows the rectifier designed above in order to regulated the rectified voltage to 1.8 V and deliver maximum load current of 10 mA. Since the output from the active rectifier is 2.2 V and the required regulated voltage is 1.8 V, charge pump or SMPS of boost type is irrelevant here. Buck SMPS could be an option for voltage regulation but LDO is preferred for it better performance in terms of noise and faster settling of regulated voltage. [20].

Figure 4.1 shows a circuit of typical LDO with pMOS as pass element. As shown in the figure, the components includes an error amplifier (EA), a pass device (Mpass), a feedback circuit (R1 and R2) and load (C_{out} and I_{load}). A more general and complete LDO circuit also includes circuitry for generation of reference voltage and bias current/voltage. In this project it will be discussed separately later. The working principle of LDO is that the error amplifier compares the scaled down regulated voltage, Vdiv with Vref and regulates the internal resistance of the pass transistor such that the error, V_{ref} - V_{div} is least or zero ideally.

[21] and [22] are two examples of CMOS implementation of LDO. [21] has proposed bulk modulation technique for improving load regulation and stability of capacitor-less LDO. Similarly [22] has proposed techniques for increasing current efficiency of LDO especially at no or low load condition. Though the techniques discussed in these designs have not been used, they have given good insight into different design parameters of LDO.

4.2 Design

Figure 4.2 shows the CMOS implementation of LDO in this project. The components in this design include a folded cascode differential amplifier as error amplifier, pMOS buffer, pMOS pass device and feedback net-

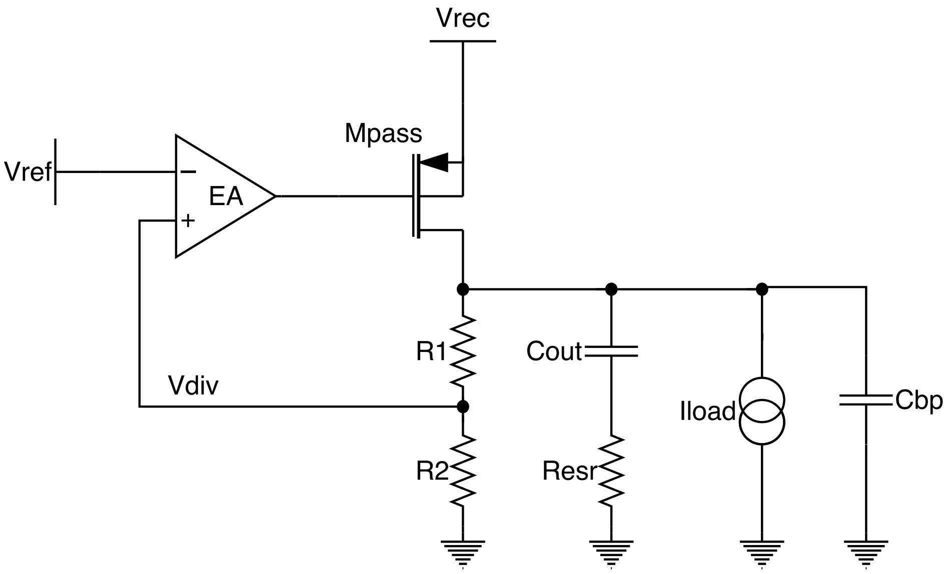


Figure 4.1: Generic LDO with pMOS pass device

work of resistors.

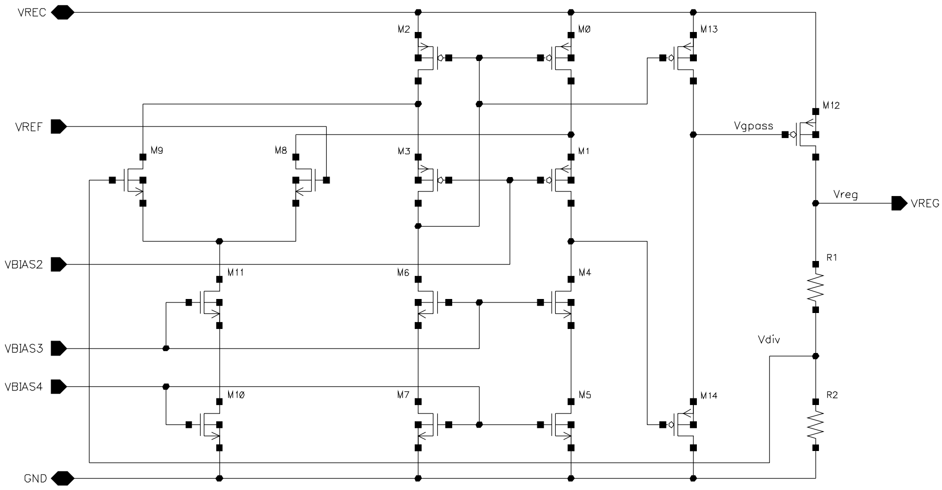


Figure 4.2: CMOS implemenation of LDO

As briefly mentioned above, the error amplifier amplifies the error i.e. difference in scaled regulated voltage, V_{div} and reference voltage, V_{ref}. It is known that an amplifier with higher open loop DC gain reduces the closed loop gain error and hence amplifier with higher gain is desired here which is turn increase the accuracy of regulated voltage, Vreg [21]. Typically error amplifier has gain $> 40dB$ which is not achieved with a single stage amplifier with this technology. Higher gain can be achieved by cascading multiple single stage but with increased difficulty in making the multistage amplifier stable. So for achieving higher DC gain and at the same time for stability convenience, folded cascode amplifier [23, pp. xx] is chosen.

Table 4.1: LDO design parameters

Pass device	pMOS
$(Wp/Lp)_{pass}$	540um/280nm
Input supply	>2.2 V
Error amplifier	folded cascode
Vbias2	1.1 V
Vbias3	0.88 V
Vbias4	0.68 V
Vref	1.17 V
C_{load}	> 5 µF
R_{esr}	> 0.5 Ω
Regulated output voltage	1.8 V
I_{load} max.	10 mA

The amplifier has a nMOS differential input stage, perferably for its higher mobility for achieving more gain. Reference voltage, V_{ref} will be bandgap voltage, 1.17 V, of silicon and thus ICMR for EA lies almost at half the supply voltage. This amplifier drives a pMOS buffer which is used to supply sufficient current to drive the large pass transistor. Moreover, pMOS as a buffer passes 1 better which means it can turn off the pass device completely and hence LDO regulates better at low load or no load condition. However for heavier load/larger load current, this pMOS buffer is not able to pull down the gate of pass device suffuiciently lower. This is overcome by making the pass device large enough to feed the required maximum load current.

The pass device is a pMOS transistor in this design. It is chosen because it has several advantages over it's counterparts like nMOS and BJT devices in terms of dropout voltage, quiescent current, input voltage, thermal response and noise[24]. Prominently, there are two factors that give pMOS edge over other devices; dropout voltage and quiescent current, when it comes to application in low power and low voltage devices. nMOS as a pass device requires a positive drive voltage with respect to output to operate. On the other hand, pMOS is driven by a negative signal with respect to input which means pMOS is preferable for a low input LDO. Similarly compared to BJTs, pMOS requires less headroom and less quiescent current to be driven[24], [25], which means low dropout and low power operation, typical requirement of today's micro devices' power supply.

However, pMOS as a pass device in LDO causes challenges in sta-

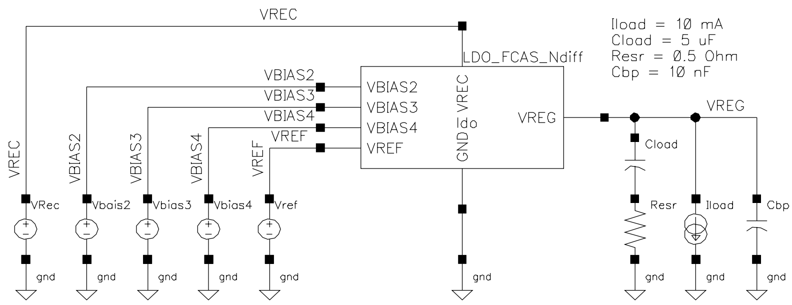


Figure 4.3: LDO testbench setup

bility. As mentioned above, LDO utilises a high gain feedback loop in order to provide a regulated output voltages independent of load current and in any system with feedback loop, the locations of poles and zeros determine stability of the system. In case of the pMOS LDO, the pass device is configured in a common source configuration. LDO with big output cap has a dominant pole pole at the output, which is a low frequency pole. The second pole is located at the gate of pass device because as mentioned earlier pMOS pass device is large and has a big parasitic capacitance. This second pole may be located closer to the dominant pole, resulting in significant reduction in phase margin (PM). Consequently, this may lead to instability of the LDO with pMOS pass device. Various methods have been implemented for ensuring the stability of the pMOS LDO. In this project, a large external capacitor, C_{load} in figure 4.1, is used for stabilising the system at the cost of additional settling time. When an external capacitor is used for designing a stable LDO, the minimum value of capacitance, C_{load} and minumum value of its equivalent series resistance (ESR), R_{esr} should be specified[25]. C_{load} determines the dominant pole of the LDO and R_{esr} in series with C_{load} introduces a left half plane zero below unity gain frequency, UGF of LDO in order to cancel out the non-dominant pole below UGF, producing a stable LDO system.

4.3 Simulation result

4.3.1 Transient response

Figure 4.4 is the transient simulations of the LDO which illustrates generation of regulated output voltage, $Vreg$ for both maximun load, 10 mA. For maximum load, it takes minimum 107 us to produce stable voltage. Since a large capacitor is used for stabilising LDO, it take longer time. Compared to schematic result, it takes 9 us extra time which can be accounted additional parasitic capacitance of interconnects at the output of LDO.

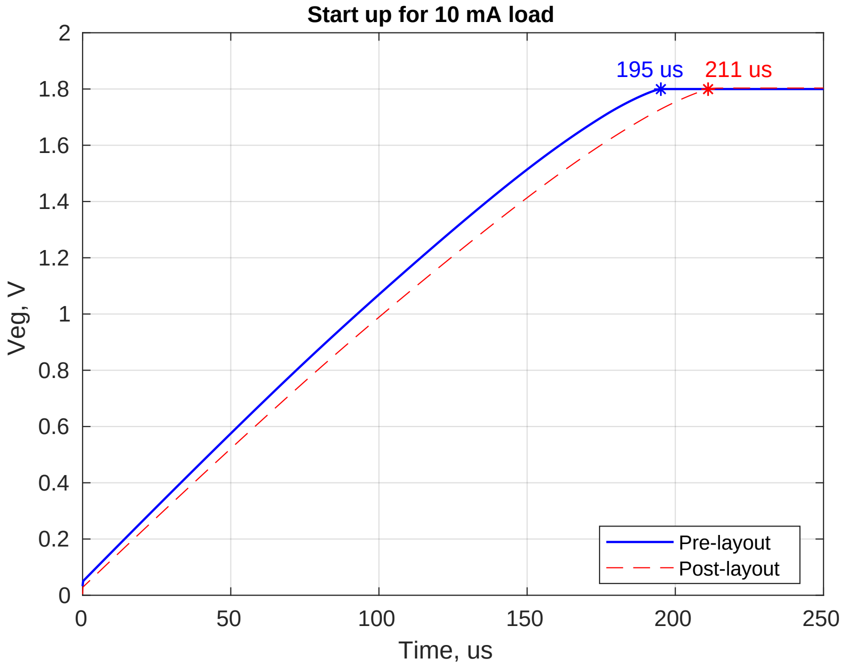


Figure 4.4: LDO transient simulation

Figure 4.5 and 4.6 show the transient response of LDO for line, $Vrec$ and load, $Iload$ variation. It gives information about how well and how fast regulated output settles for line and load variations. In figure 4.5 load is given as pulse varying from 10 uA to 10 mA with both falling and rising time of 1 ns keeping input supply constant to 2.2 V. Sudden increase in load causes the output voltage to drop. The error amplifier then takes some time adjusts the gate voltage of pass device to low to fully turn on the device. Likewise when the load suddenly drops to minimum, it causes the output voltage to increase. Again error amplifier adjust it back by increasing the gate voltage of pass device to turn it off. Similarly for line variation observation, input, $Vrec$ is pulsed from 2 V to 2.5 V with 1 ns rising and falling time keeping load current constant to 10 mA. Sudden increase in input voltage causes output to increase and vice-versa. As in load variation case, similar recovery pattern is seen. In both case of load and line regulation, the out put voltage is maintained quickly, less than 0.15 us. Both results from schematic and post layout have same transition behaviour except post layout result offset by 3.7 mV as explained in DC response section below.

Line regulation, change in regulated output voltage due to maximum change in input voltage and load regulation, change in output voltage due to maximum change in load current are calculated from values shown in respective plots and are listed in table 4.2.

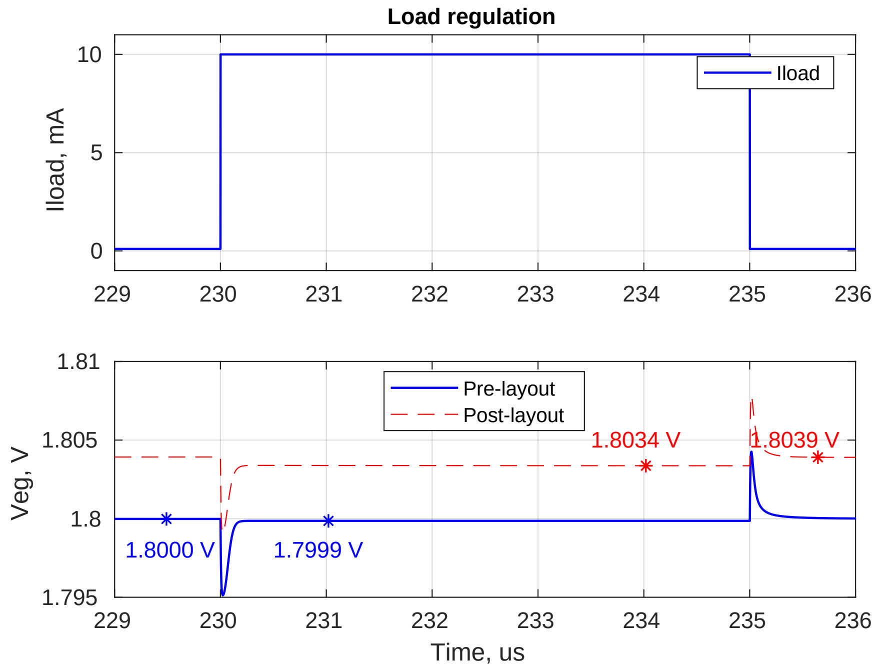


Figure 4.5: LDO step load regulation

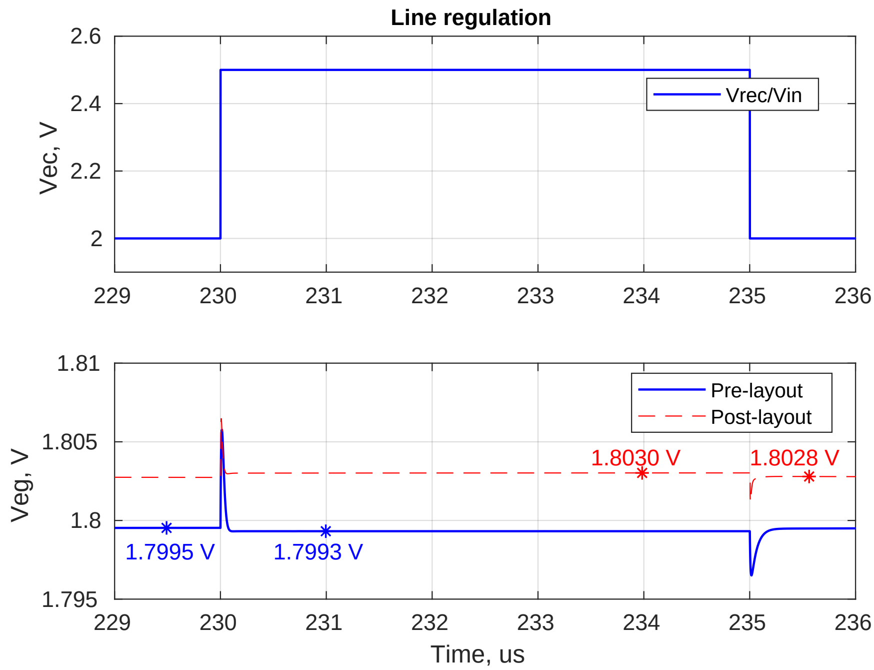


Figure 4.6: LDO step line regulation

4.3.2 DC response

Figure 4.7 and 4.8 show LDO response to input voltage, $Vrec$ sweep and output load, $Iload$ sweep. As seen in 4.7, the regulator is turned off for input below 1.85 V. Since the input is also the supply for the entire design, higher voltage is required for creating proper biasing of internal folded cascode error amplifier. However after turning on, it requires only 100 mV drop for proper regulation for maximum load and is even lesser for lighter load. This shows that minimum value of supply required for LDO to function properly is 1.95 V. In 4.8, it is seen that regulated output voltage for post layout simulation is 3.7 mV higher than for schematic. Since $Vreg = (1 + R1/R2) * Vref$, the mismatch in the resistors has resulted in slightly higher ratio, consequently increasing the close loop gain.

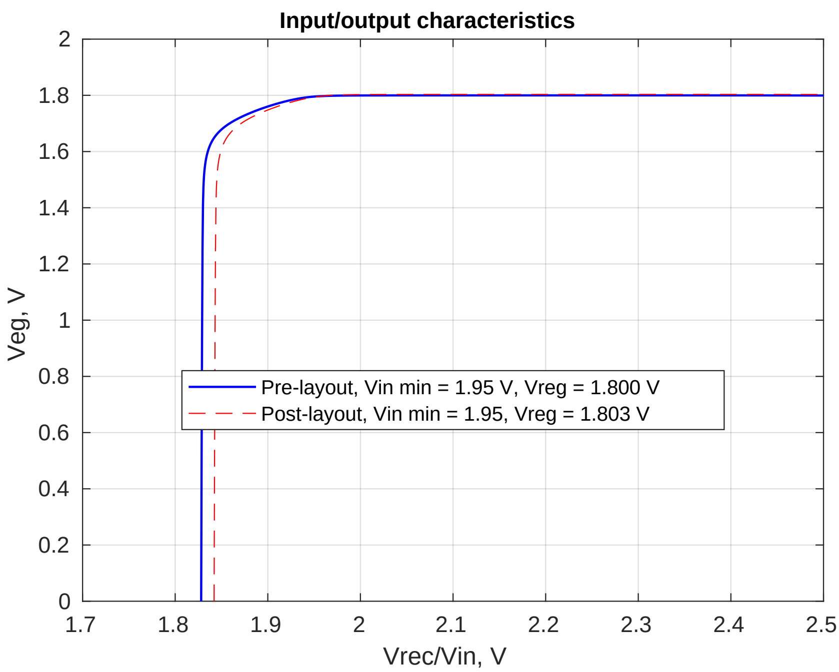


Figure 4.7: Regulated voltage with supply variation

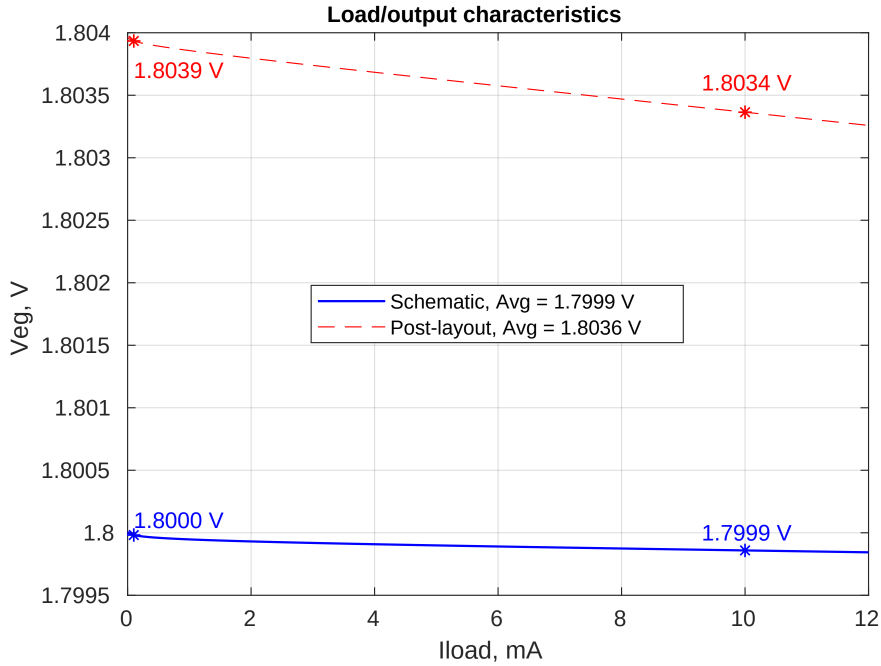


Figure 4.8: Regulated voltage with load variation

4.3.3 AC response

Figure 4.9 is open loop gain and phase margin of LDO without and with compensation. In the upper uncompensated bode plot, two poles below UGF are seen: the first one at 300 KHz due to output resistance of pass device and its parasitic capacitance, and the second one at 60 MHz due to buffer output resistance and gate capacitance of pass device. UGF is at 100 MHz. Due to these two poles both occurring below UGF, the PM fallen to -45°. For making the LDO stable, as discussed in the beginning, a capacitor, C_{load}, 2.5 uF with specific series equivalent resistance, R_{esr}, 0.8 Ω is used at the output. C_{load} and pass device output resistance creates the dominant pole at 1 KHz and R_{esr} and C_{load} creates a left half plane zero below UGF which cancels the non dominant pole. This eventually gives 75°PM and 30 dB GM.

Likewise figure 4.10 is the plot showing PSSR of this LDO. It can be seen that it has poor PSSR performance for frequency higher than 200 KHz. Low frequency noise like 50Hz supply ripple is effectively rejected. In this design 13.56 MHz ripple and its first harmonics is expected in the input of LDO because rectified output from rectifier operating at 13.56 MHz as input signal is used as supply and/or input for this LDO. Unfortunately, PSSR performance is worst around this frequencies. However the ripple rejection is still -36 dB at 13.56 MHz which is decent. As seen in figure 4.9, the open loop gain of LDO feedback circuit is 90 dB, which has contributed in achieving decent PSSR even at higher frequency[26]. This paper also discusses that UGF frequency corresponds to the roll off frequency of PSSR, which can also been seen by comparing plots 4.9 and 4.10. The stability technique in this design also gives adverse effect on PSSR performance as UGF is significantly lowered by large output capacitor.

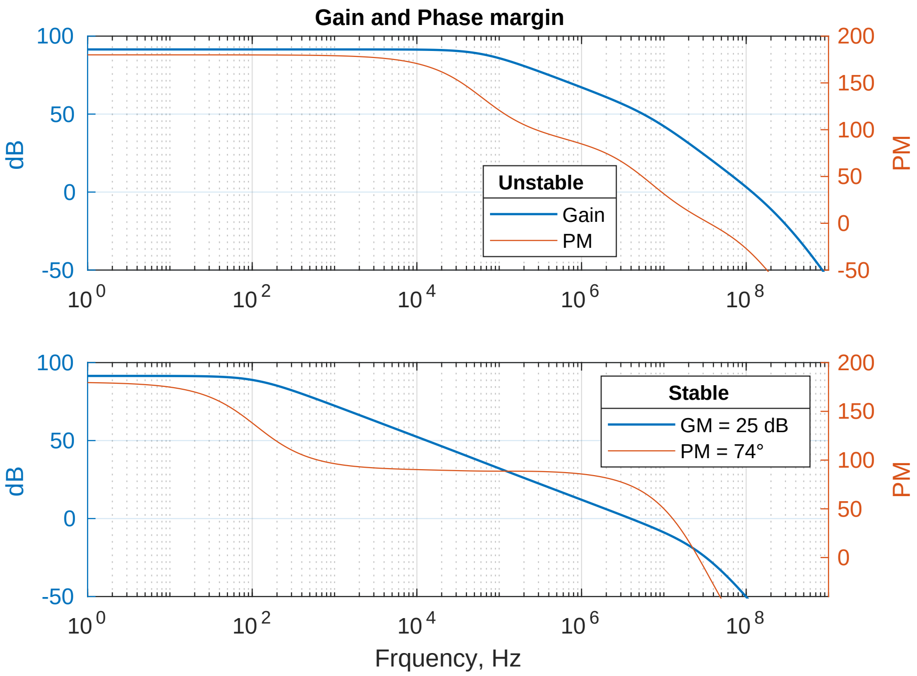


Figure 4.9: LDO stability before and after compensation

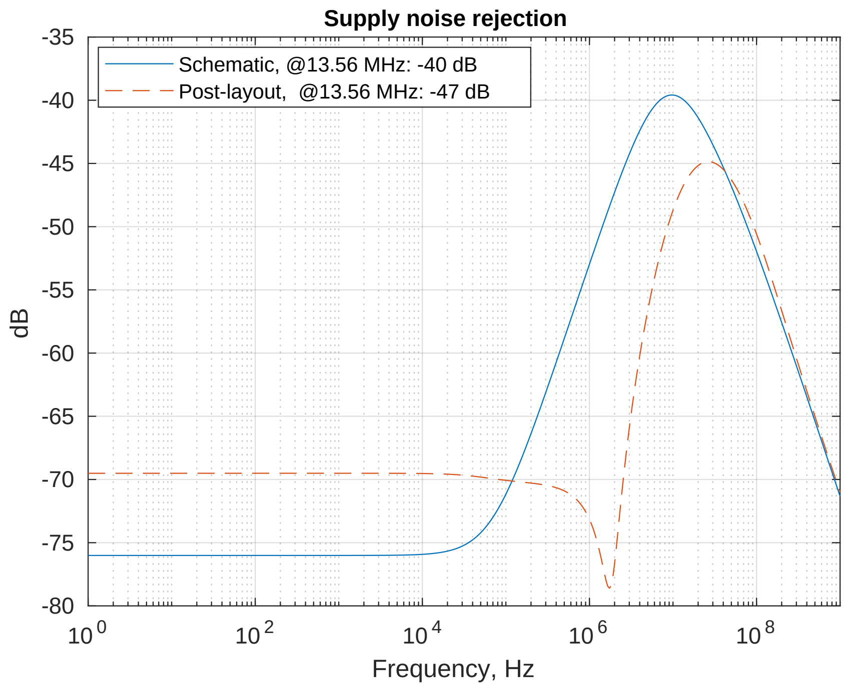


Figure 4.10: PSSR performance

Table 4.2 summaries the performance of LDO regulator discussed above. Power efficiency is calculated as power delivered to load to power consumed from the source. Quiescent current includes biasing currents for error amplifier, feedback resistors and buffer which is obtained by taking the difference of current drawn from the source and current delivered to the load. Both power efficiency and quiescent current is calculated for maximum load operation.

Table 4.2: LDO performance summary

	Schematic	**Post-layout**
PSSR	-36 dB @ 13.56 MHz	-59 dB @ 13.56 MH
Phase margin	75°	
Gain margin	30 dB	
Power efficiency	80.9 %	81 %
Quiescent current	105 uA	114 uA
Load regulation	17 uV/mA	53 uV/mA
Line regulation	435 uV/V	-1.162 mV/V

Chapter 5

Antenna Design

5.1 Introduction

All the components discussed above are part of any power management system which takes DC input from power line and creates regulated output as required. However, the objective here is to replace direct power line connection with wireless link. Since the intention is to just create a wireless power transfer link, the option which is easier to implement, convinent to operate and gives higher transfer efficiency is the primary choice here. And the literatures in wireless power transfer studies show inductive couling meets all these requirement.

Inductive coupling boils down to principle of electromagnetic induction. When alternating electirc current is passed through a coil, say primary, it generates alternating magnetic field. If another coil, say secondary, is placed in this changing magnetic field, alternating voltage/current is induced in the coil. In other word, power from primary coil is transferred wirelessly to secondary coil through magneic field and this is popularly known as inductive power transfer link. And this induced ac voltage is rectified and then used to power up the load.

The energy transfer efficiency between the coils depends on how much of the magnetic field generated by the primary is captured by the secondary coil. And the capture of magnetic field by the secondary coil in turn depends on shape and size of two coils, their separation and alignment. All these factors influencing the transfer efficiency collectively gives a quantity called coupling factor, k. A pefect inductive link has a coupling factor 1, which means all the magnetic flux genetated by primary is captured by secondary. However normally achieved coupling factor in practical inductive link is 0.3 and at best 0.5. So for better transfer of efficiency, some improvisation is done to the inductive link, so that efficiency is less affected by coil separation and alignment. This is done by tuning both the primary and secondary coil to same frequency i.e. creating resonance at some frequency so that coil coulpling is the strongest at that frequency. This method of creating better wireless energay transfer link is popuolarly known as magnetic resonance coupling.

In this project, first an antenna coil is designed and characterised. Then inductive link created using that antenna is studied and finally magnetic resonance technique is implemented to increase transfer efficiency at the operating frequency. The antenna dimensions are provided by Nordic Semiconductor which is one of their design already used in some application. Since having similar shape and size of antennas is important in gaining more transfer efficiency, the same antenna type is used as both primary and secondary coils.

5.2 Inductor model

Figure 5.1 is a lumped model of a planar antenna/coil/inductor made on a PCB. Rp, series DC resistance of wire and Cp, inter-winding self capacitance. These parasitics determine quality factor and self resonance frequency, SRF of the antenna. The quality factor is given as $Q = \omega L / Rp$ and SRF as $SRF = 1/(\sqrt{LCp})$, for this simple model.

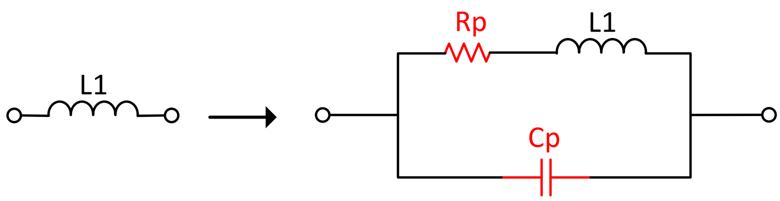
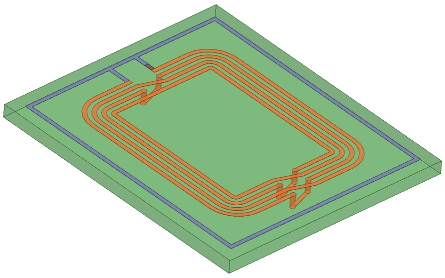


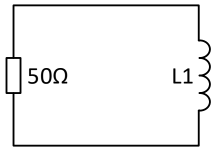
Figure 5.1: Real antenna model

For purpose of this work, with provided dimensions of the antenna, it is first modelled in HFSS as shown in figure 5.2a and its equivalent lumped circuit in figure 5.2b. It is important to note here that L1 in 5.2b is in fact 5.1. However, in the discussion ahead, these parasitics are not explicitly mentioned for the sake of simplicity because the parameter extraction will include these factors too and on the other hand the operating frequency here is much less than coil SRF. To realise a real antenna, physical parameters of materials used for making printed antenna on a PCB are also given for the model. After completing model, frequency sweep is done for extracting S parameter of the antenna which was eventually used to estimate self inductance of the modelled coil. The performance estimation of single antenna here and couple system later is based on formulas in [27]. In order to check and compare the estimated inductance value from the model, Modified Wheeler Formula, a mathematical approximation model described in [28] is used.

The qualities of antenna obtained from extracted S-parameter are listed in table 5.1. The table shows that modelled inductance value is less than mathematically approximated value. This difference can be explained with two things. Firstly, mathematical calculation assumed that the antenna is spiral and rectangular with sharp edge but the model has rounded edge. Secondly, during modelling besides dimensions of the coils, physical parameters of coil materials are also used but these are not considered for mathematical calculation.



(a) HFSS antenna model



(b) Equivalent schematic

Figure 5.2: Antenna model

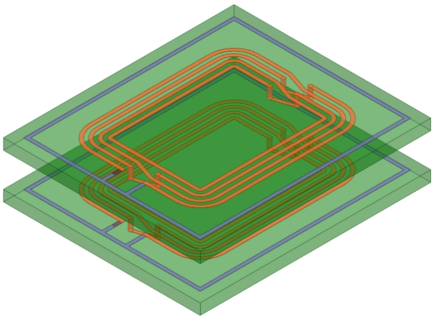
Table 5.1: Characterisation of antenna

	HFSS model	Modified Wheeler [28]
Self Inductance	448 nH	644 nH
SRF	125 MHz	
Quality factor		
Parasitic Resistance		
Parasitic Capacitancce		

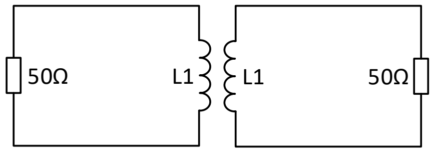
5.3 Inductive transfer link

In the next step, an inductive link is realised by using two antennas: one as primary and other as secondary, aligned one over other and separated by air gap as shown in figure 5.3a, equivalently shown as lumped schematic in figure 5.3b. Coupling system of these antennas is simulated for varying distance of magnetic field interaction to observe the difference in performance. The same procedure as used for single coil above, is used to extract self inductance of each coil, $L1$ and $L2$, mutual inductance of two coils, $L12$, coupling coefficient between the coils, k and quality factor, Q. The extracted values for coil separation of 1mm, 5mm and 10mm are listed in table 5.2 calculated at operating frequency of

13.56 MHz.



(a) HFSS coupling model



(b) Equivalent schematic

Figure 5.3: Antenna coupling model

Table 5.2: Coupling parameters for varying coils distance

Parameter	1 mm	5 mm	10 mm	mm
L1	-	-	-	nH
L2	-	-	-	nH
L12	-	-	-	nH
k	-	-	-	-
Q	-	-	-	-
SRF				

It is observed that $L1$ and $L2$ are same as in table 5.1 as it is the same coil used as primary and secondary. Similarly $L12$ and k, related as $L12 = k\sqrt(L1L2)$, are both decreasing with distance as expected. With increase in separation, less and less magnetic flux generated by primary coil is linked with the secondary, creating a loosley coupled inductive link.

The power transfer efficiency of the physical link created by coupled coils is very important. [CITE] states that efficiency depends k of coupling system and Q of coil and hence high k and high Q is always desirable and obviously coil optimisation is the most important part of coupling system design. [29] and [30] discusses some techniques to optimise transfer efficiency of inductive link: [29] about matching the load for better resonance whereas [30] about designing optimal coil geometry for higher Q. The former one compares the efficiency of general inductive coupling and conventional resonant coupling and their limitation in achieving higher efficiency. This eventually proposes optimal resonant load transformation which has better immunity to poor coupling and load variation. Likewise, the later one describes step by step iterative process of designing an antenna with optimal geometry for the given design constraints.

5.4 Magnetic resonance coupling

In this project, conventional magnetic resonance coupling as in is implemented to tune both primary and secondary to the power career frequency. The purpose here is to match the impedance of primary antenna to source impedance and secondary antenna of coupling system to load impedance in order to maximize the power tramsmission from the source to the load.

For the purpose of making a resonant inductive link, the S parameter of coupled antenna system in HFSS is exported to ADS in order to design matching networks using capacitors only. Impedance of primary antenna is matched to 50 Ω source resistance and impedance of secondary is matched to load impedance (50 Ω load or input impedance chip(?)) as shown in 5.4. $Cp1$, series capacitor and $Cp2$, shunt capacitor together with $L1$ created parallel resonant circuit at 13.56 MHz on the primary side and $Cs1$, shunt capacitor together with $L2$ creates the secondary resonant circuit at same operating frequency. Thus a pair of LC tank circuit is made tuned at same frequency. Such matching network is designed for all three coil separation distances as above, but resonant coupling system with 5 mm separation is taken as a typical example and presented here.

The reflection power loss, S11 and S22, at both primary and secondary terminal, power transfer gain, S21, from primary to secondary and Q-factors for both antennas before and after creating resonance are shown in figure 5.5, this and this.

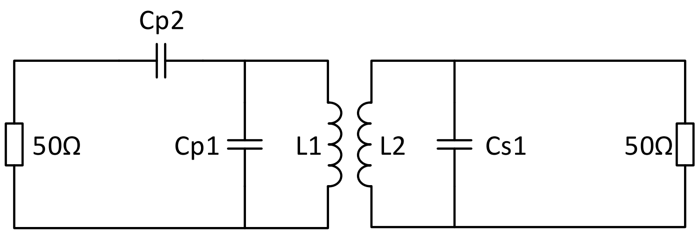


Figure 5.4: Resonant coupled inductive link

The performance of magnetic resonant coupling link designed in this work is summarises in table 5.3 below.

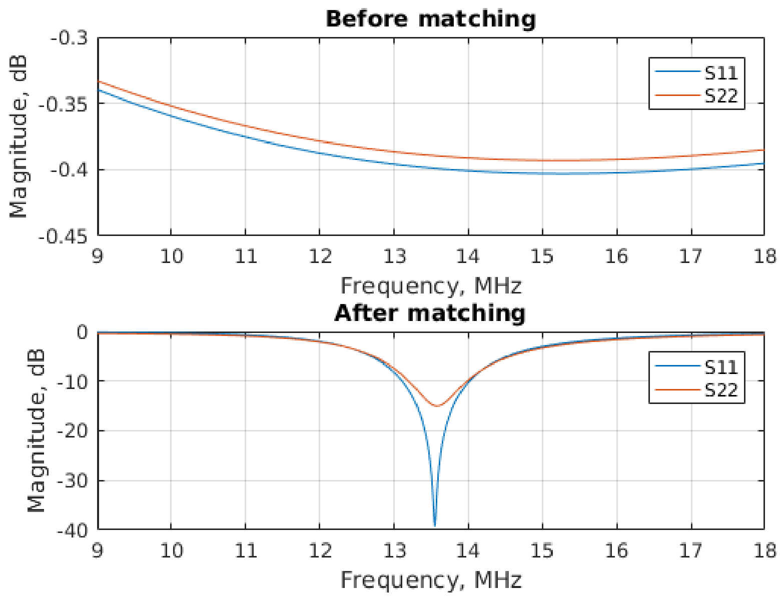


Figure 5.5: Power loss before and after matching

Table 5.3: Performance of resonant inductive link

$Cp1$ $Cp2$ and $Cs1$	
Resonant frequency	13.56 MHz
Primary reflection loss	
Secondary reflection loss	
Primary to secondary gaining	
Q-factor	

Part III

WPT System Design and Implementation

Chapter 6

Power Receiving Unit Design

6.1 Introduction

Wireless power transfer, WPT system always constitutes two main units: power transmitting unit, PTU and power receiving unit, PRU. Each unit comprises of resonator, power conditioner and control circuits as shown in figure 6.1. Both the resonators in PRU and PTU are tuned to operating frequency, which create a physical transfer link. Power conditioner circuit in PTU includes at least power amplifier and matching circuit, whereas in PRU, it includes matching circuit, rectifier and regulator. Similarly both these units have control block which facilitates transfer procedure and communication between these units. In this work, design and analysis of PRU is the main objective.

In figure 6.1 above, the block highlighted in blue is the PRU system in this design. Secondary coil, Rx is the receiver resonator, and rectifier and regulator is power conditioning block. The primary coil is driven by a power source and AC signal is generated at the secondary as discussed earlier in antenna design section. The rectifier then rectifies this AC signal to DC. The DC output of the rectifier is then fed to LDO to produce regulated DC output required to drive a load. The reference and biasing circuit generates required reference and biasing DC voltages for the LDO.

The PRU unit is broken down into two sub units for step wise analysis. As seen in the block diagram, it is functionally divided into Transfer Link and Power Management System (PMS). Firstly, PMS is simulated excluding the transfer link to characterise the performance of PMS. Secondly, the whole PRU system: PMS with transfer link created with coupled antenna, Tx and Rx, is simulated to observe the performance of whole PRU. Though it has already been told earlier, one important thing must be mentioned here again before going further. Even though reference and biasing circuit has been integrated into the PMS

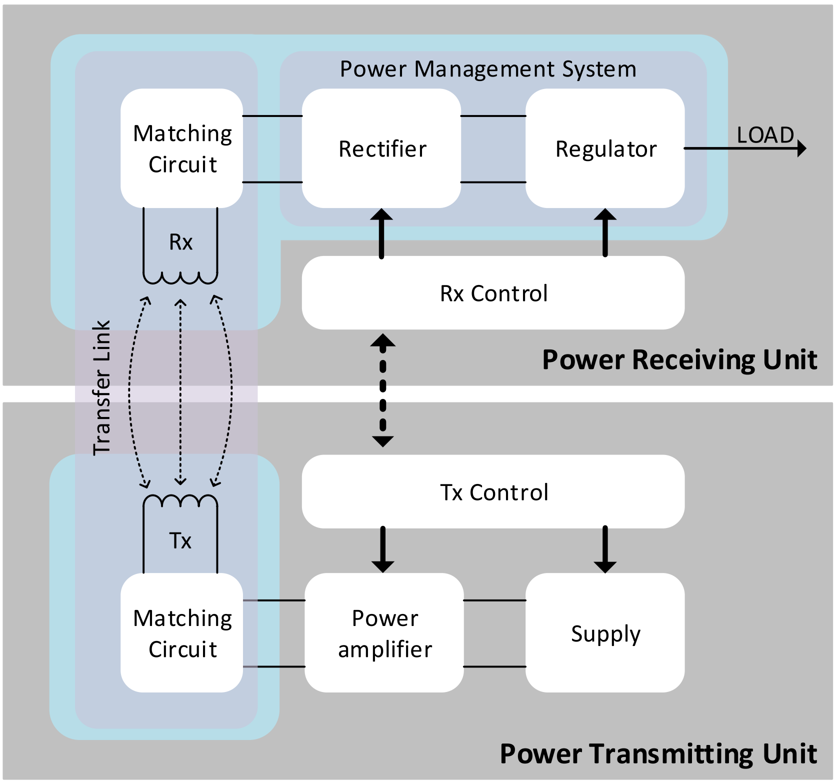


Figure 6.1: WPT block diagram

system, it has been designed with an option to override it externally. This externally supplied reference and biasing will be primarily used for the PRU system simulation. The result with on-system biases and reference will be explicitly noted when used.

6.2 Power Management System

Figure is the top level of PMS in this design. The purpose here is to see Vrec and Vreg outputs while driving maximum load. The voltage biases outputs to examine the performance of BGR circuit which is disable now with external control signal Vctl low. The test bench setup is a shown in figure .

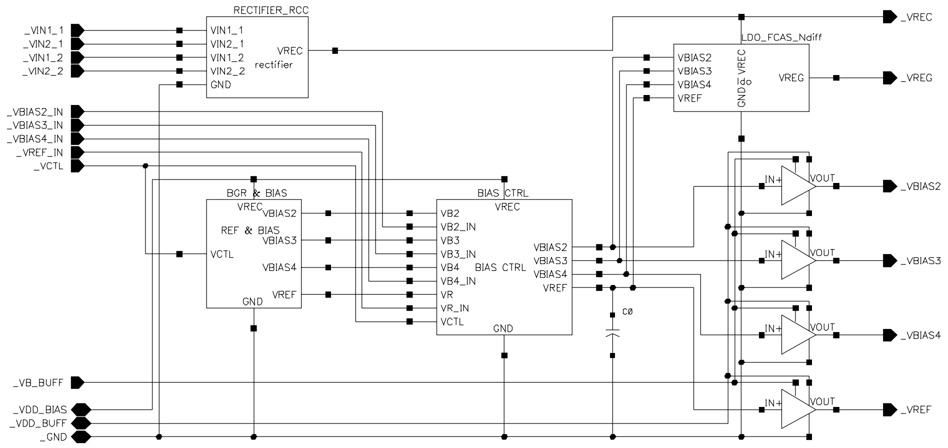


Figure 6.2: WPT PMS implementation

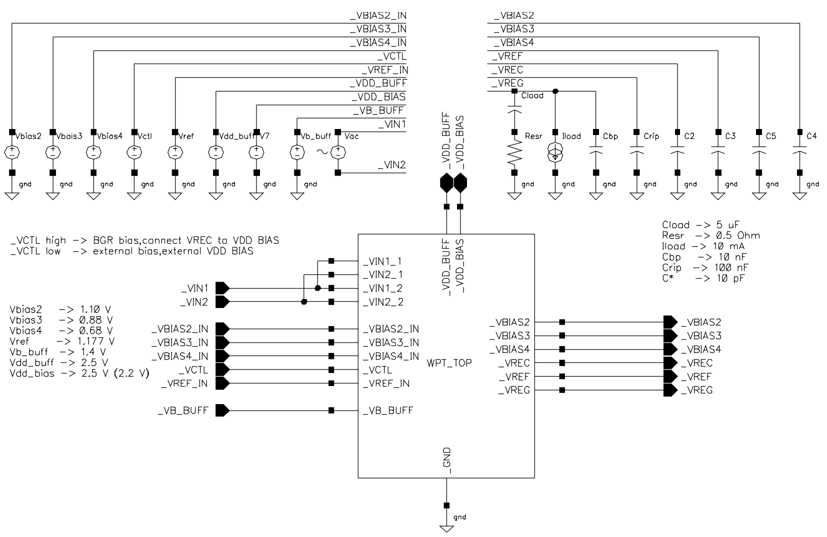


Figure 6.3: Test bench for PMS simulation

6.2.1 Transient Response

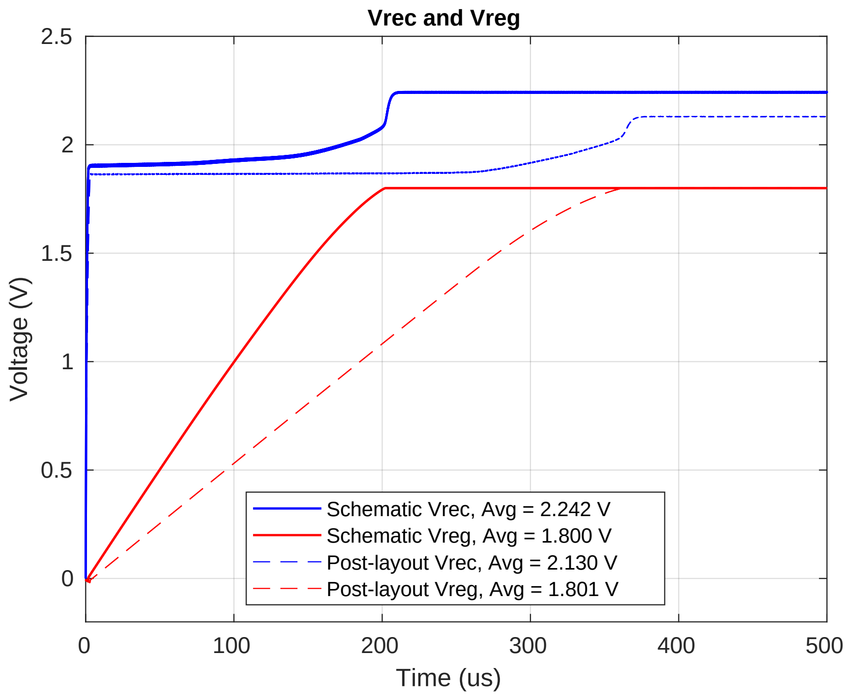


Figure 6.4: Transient Vrec and Vreg

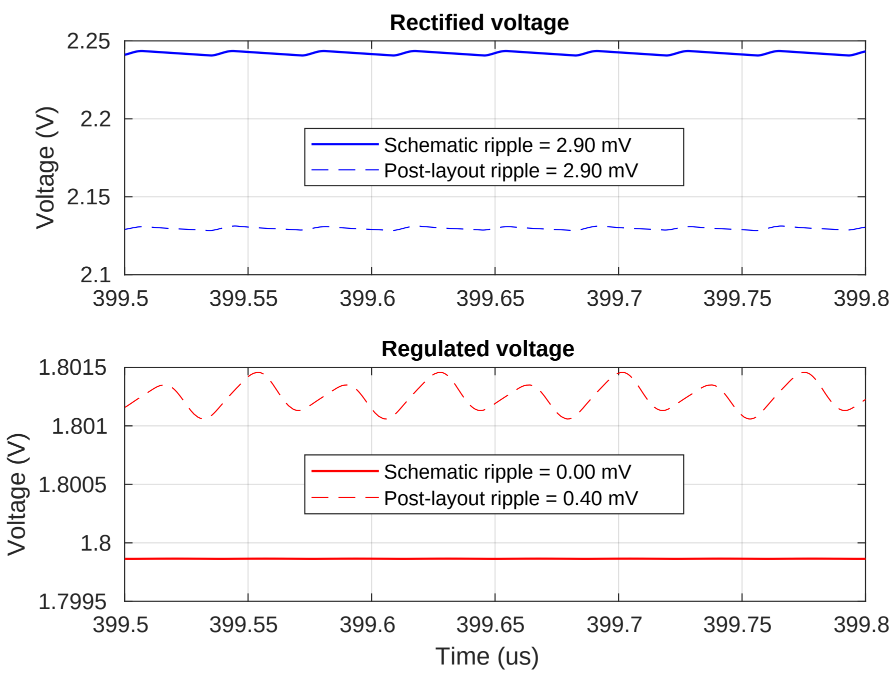


Figure 6.5: Ripple in Vrec and Vreg

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Acronyms

CMOS complementary metal-oxide-semiconductor

DC direct current

ESR equivalent series resistance

FCC Federal Communications Commission

GM gain margin

ICMR input common mode range

IEEE Institute of Electrical and Electronics Engineers

MOS metal-oxide-semiconductor

nMOS n-channel MOS

PCE power conversion efficiency

PM phase margin

pMOS p-channel MOS

PMS Power Management System

PRU Power Receiving Unit

PSSR power supply rejection ratio

PTU Power Transfer Unit

SMPS switch mode power supply

SRF self resonance frequency

UGF unity gain frequency

VCE voltage conversion efficiency

Vp peak voltage

Vpp peak to peak voltage

Vtn thresold voltage of n-channel MOS

Vtp thresold voltage of p-channel MOS

WPT Wireless Power Transfer