A 13.56 MHz Wireless Power Transfer System With Reconfigurable Resonant Regulating Rectifier and Wireless Power Control for Implantable Medical Devices

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***Abstract*—A 13.56 MHz wireless power transfer system with a 1X/2X reconfigurable resonant regulating (R^3) rectifier and wireless power control for biomedical implants is presented. Output voltage regulation is achieved through two mechanisms: 1) a local PWM loop at the secondary side controls the duty cycle of mode-switching of the rectifier between the 1X and 2X modes; and 2) a global control loop obtains the mode-switching information from the secondary side and send it back to the primary side through the wireless channel and adjusts the transmitter power of the primary coil to adapt to load and coupling variations. Two novel backscattering uplink techniques are proposed for fast and energy-efficient data feedback. The first is for general data transmission using Manchester code; and the second is for fast duty cycle feedback to cater for fast load-transient responses. Stability analysis of the entire system with the two control loops is also presented. The primary transmitter and the secondary R^3 rectifier are fabricated in 0.35 µm CMOS process with the digital control circuits implemented using FPGA. The measured maximum received power and receiver efficiency are 102 mW and 92.6%, respectively. For load transients, the overshoot and the undershoot are approximately 110 mV and the settling times are less than 130 µs.**

***Index Terms*—Implantable medical devices, reconfigurable resonant regulating rectifier, wireless power control, Wireless power transfer.**

I. Introduction

WIRELESS POWER TRANSFER (WPT) has been widely used in implantable medical devices (IMDs) such as retinal prostheses [1] and neural recording [2] to eliminate the use of the bulky battery. Real-time power transfer in the range of 10 mW to 100 mW [3] is required for different types of implants. For near-skin IMDs, WPT is based on inductive near-field coupling due to its high efficiency [4]. The basic WPT system consists of an external device and an internal implant as shown in Fig. 1. The power is transferred through two coupled coils: a primary coil and a secondary coil.

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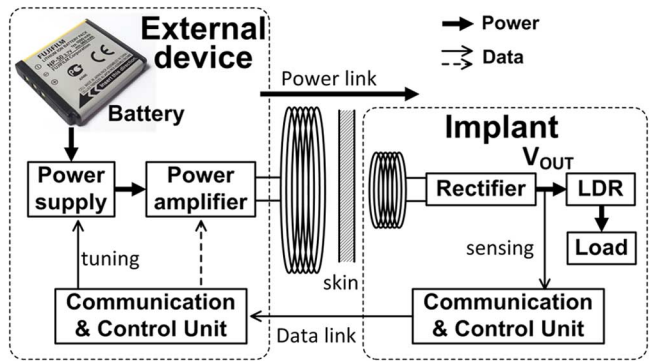

Fig. 1. Wireless power transfer (WPT) system for IMDs.

In the external device, the battery voltage is regulated by the DC supply module, which powers up the power amplifier (PA) that drives the primary coil to generate AC magnetic fluxes. In the implanted device, the coupled AC power is rectified into DC power, usually cascaded with a low dropout regulator (LDR) to generate a regulated voltage for the load. In actual IMD applications, the coil coupling varies with the distance and the alignment between the coils. The load may change with time depending on the application. Both coupling and load variations make the output voltage of the rectifier $V_{\rm OUT}$ unsteady. If there is no power control, the worst case scenario has to be designed for when the coupling distance is large, and use a high-enough transmission power to maintain $V_{\rm OUT}$ higher than the minimum required value $V_{\rm OUT,min}$. However, for cases with better coupling conditions, $V_{\rm OUT}$ will then be much higher than $V_{\rm OUT,min}$, and a large voltage drop across the LDR means poor receiver efficiency, with unnecessary power transmitted and absorbed by the body tissue, which accompanied by non-preferable heat dissipation, and leave a lower margin to reach the human tissue specific absorption rate (SAR) [5]. To implement power control, in addition to the forward power link, a separate reverse data link is required to regulate $V_{\rm OUT}$. $V_{\rm OUT}$ is sensed and sent back to the external device through a wireless uplink communication channel. The external device will then adjust the transmission power accordingly based on the received data [6]. The speed of this global control loop depends on the data rate of the uplink channel. In [7], a high carrier frequency is used to achieve a fast data uplink; however, an additional pair of data coils is needed

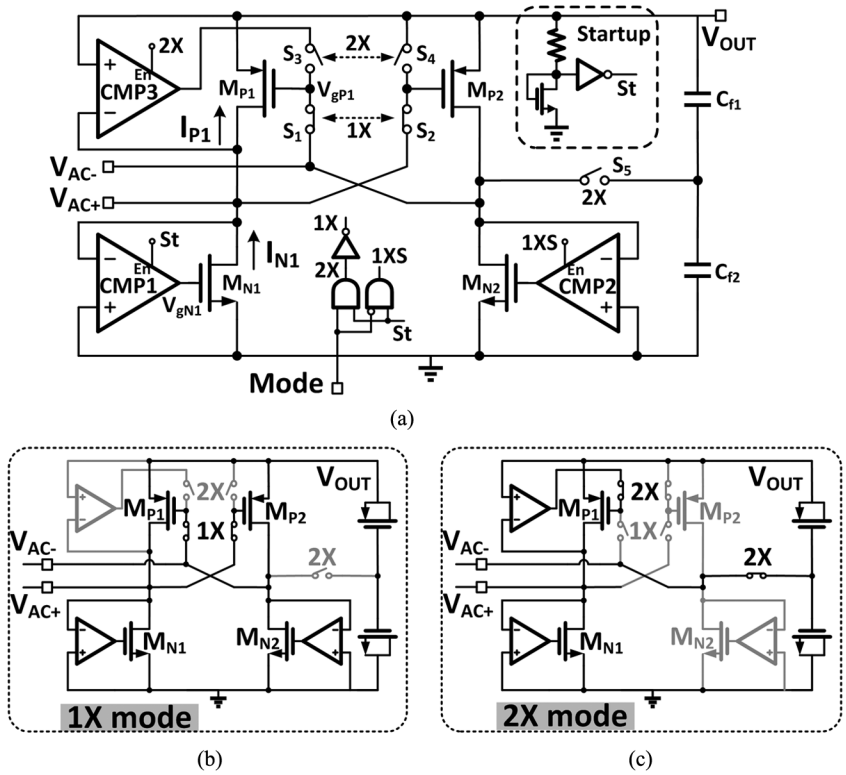

Fig. 2. (a) 1X/2X reconfigurable rectifier; (b) 1X mode; (c) 2X mode.

and the system complexity is increased. In [8], a high carrier frequency of 25 MHz is used. The data link is optimized for large bandwidth, and an independent power link is assumed to be present. Thus, an additional pair of data coils is still needed. In [9], $V_{\rm OUT}$ is regulated by the transmitter with feedback through a wire, which defeats the purpose of wireless power transfer.

Recently, rectifiers with reconfigurable output stage were proposed to upkeep the output voltage of the rectifier when the coupling conditions change. In [3], [10], 1X/2X reconfigurable rectifiers were proposed to step-up $V_{\rm OUT}$ when the two coils move apart. However, they do not have good $V_{\rm OUT}$ regulation, and an extra step-down converter such as a DC-DC converter or an LDR is required. In [11], a resonant regulating rectifier (3R) was used for $V_{\rm OUT}$ regulation. The 3R structure consists of a bridge rectifier and a step-down charge pump. The charge pump has two operating modes that result in two different output voltages. By switching between the two modes, the output voltage can be regulated through tuning the duty ratio of mode-switching. However, under extreme conditions, $V_{\rm OUT}$ cannot be regulated without increasing the transmitter power, and a global power control loop is needed. In [11], the transmitter power is controlled by a MCU and the information feedback is still through a wire.

In this work, we propose a reconfigurable resonant regulating rectifier ($\rm R^3$ rectifier) [12] that performs mode switching to regulate the output voltage $V_{\rm OUT}$, and employs a local control loop to adjusts the duty ratio D_0 of operating the $\rm R^3$ rectifier in the 2X mode (and $(1-D_0)$ in the 1X mode). In addition, to cater for large load and coupling variations, we propose an efficient data uplink channel to realize fast global wireless power control.

The rest of the paper is organized as follows. The design of the 1X/2X reconfigurable rectifier is presented in Section II. In Section III, a reconfigurable resonant regulating rectifier with local PWM control is proposed. In Section IV, two data backscattering methods are presented for energy-efficient data transmission and fast global power control. The overall WPT system will then be presented and the stability of the control loop be analyzed in Section V. Measurement results are presented and discussed in Section VI, followed by concluding remarks in Section VII.

II. 1X/2X Reconfigurable Rectifier

Before we discuss the operation of the reconfigurable resonant regulating rectifier, we first introduce the 1X/2X reconfigurable rectifier, the architecture of which is similar to that presented in [3], [10], but with a different circuit implementation.

A. 1X/2X Reconfigurable Rectifier Structure

The 1X/2X reconfigurable rectifier consists of five power switches ($M_{N1\sim2}$, $M_{P1\sim2}$ and S_5), three comparators ($CMP1 \sim 3$), two flying capacitors ($C_{f1\sim2}$) and a startup circuit as shown in Fig. 2(a). In normal operation, the startup signal St is high (St = '1'). This reconfigurable rectifier has two modes: the 1X mode and the 2X mode, depending on the on-off status of the switches $S_{1\sim5}$.

When *Mode* is '0', the 1X mode is activated. The switches S_1 and S_2 are turned on and the switches S_3, S_4 and S_5 are turned off. M_{P1} and M_{P2} are cross-connected with the gate of one transistor connected to the drain of the other. $CMP1$ and $CMP2$ are enabled, and $CMP3$ is disabled. M_{N1} and M_{N2}

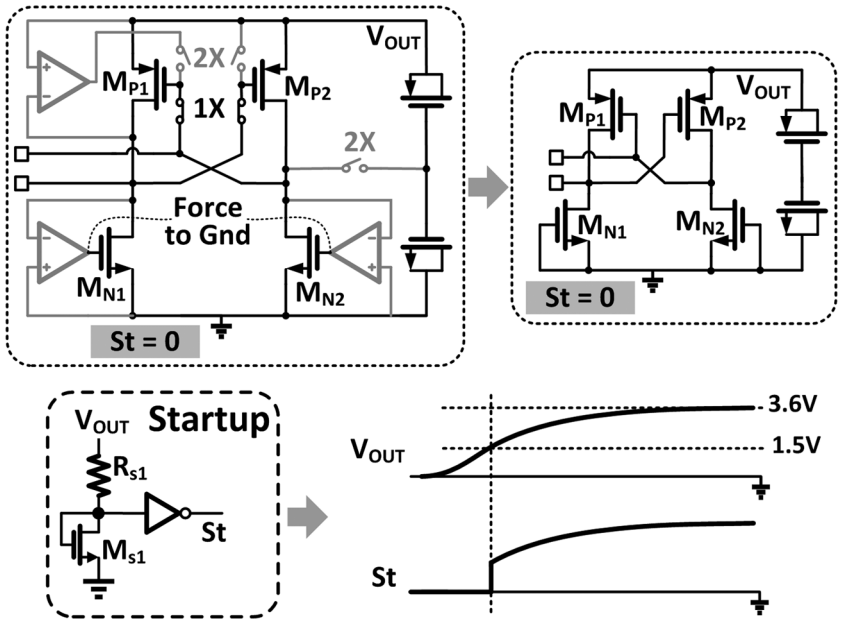

Fig. 3. Startup mode.

serve as active diodes. The equivalent structure of the 1X mode is a full-wave bridge rectifier as shown in Fig. 2(b).

When *Mode* is '1', the 2X mode is activated. S_1 and S_2 are turned off, and S_3, S_4 and S_5 are turned on. $CMP1$ and $CMP3$ are enabled, and $CMP2$ is disabled. M_{P1} and M_{N1} become active diodes. M_{N2} is turned off and M_{P2} is diode connected. In the steady state, V_{AC2} is clamped at $V_{\rm OUT}/2$, so M_{P2} is reverse-biased. The equivalent structure of the 2X mode is a voltage doubler made up of two half-wave rectifiers connected in series as shown in Fig. 2(c).

B. Startup Mode

The implant needs a startup circuit to steer away from the relaxed state. The startup circuit consists of a large resistor R_{s1} driving a diode-connected transistor M_{s1} with threshold voltage of 0.7 V, and an inverter powered up by $V_{\rm OUT}$ with inverter threshold voltage of 0.7 V when $V_{\rm OUT} = 1.5$ V. When $V_{\rm OUT} = 0$ V, the implant is in the startup mode, and $St =$ '0'. $CMP1{\sim}3$ are disabled. M_{P1} and M_{P2} are cross-connected with the gate of one transistor connected to the drain of the other. The gates of M_{N1} and M_{N2} are connected to ground, and the transistors become passive diodes. The four power transistors then form a full-wave passive bridge rectifier as shown in Fig. 3, and C_{f1} and C_{f2} are slowly charged up. When $V_{\rm OUT}$ is increased to around 1.5 V, St is then switched to become '1' and the rectifier is then working in the normal mode.

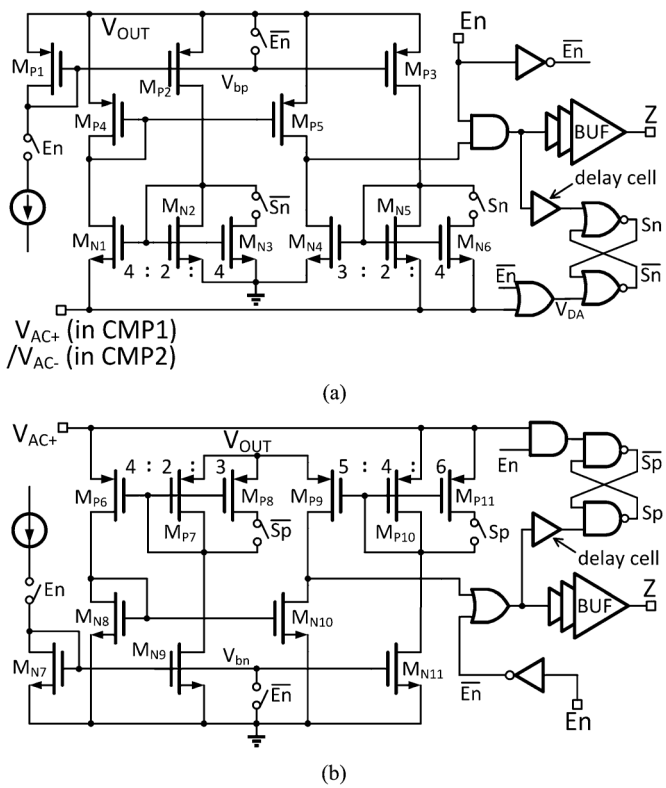

Fig. 4. (a) Structure of CMP1 & CMP2. (b) Structure of CMP3.

C. Switching-Delay Compensated Comparators

Comparators $CMP1$ and $CMP2$ are used to drive the NMOS power transistors of the active rectifier and they have the same structure as shown in Fig. 4(a). The comparator is activated when the enable signal En is high. The switches Sn and $\overline{Sn}$ control the input offset voltage of the comparator depending on the comparator output Z to compensate for the output switching delay [13], [14]. When Sn is low (and $\overline{Sn}$ is high), the size ratio of M_{N1}:$(M_{N2}+M_{N3})$ is 2:3, and that of M_{N4}:M_{N5} is 3:2, resulting in a negative input offset for the comparator. Conversely, when Sn is high (and $\overline{Sn}$ is low), the size ratio of M_{N1}:M_{N2} is 2:1, and that of M_{N4} : $(M_{N5}+M_{N6})$ is 1:2, resulting in a positive input offset. If Z is low, when V_{AC} increases to around $V_{\rm OUT}/2$, V_{DA} (the output voltage of the OR gate shown in Fig. 4) is changed from low to high as shown in Fig. 5(a) and Sn ($\overline{Sn}$) is switched from low (high)

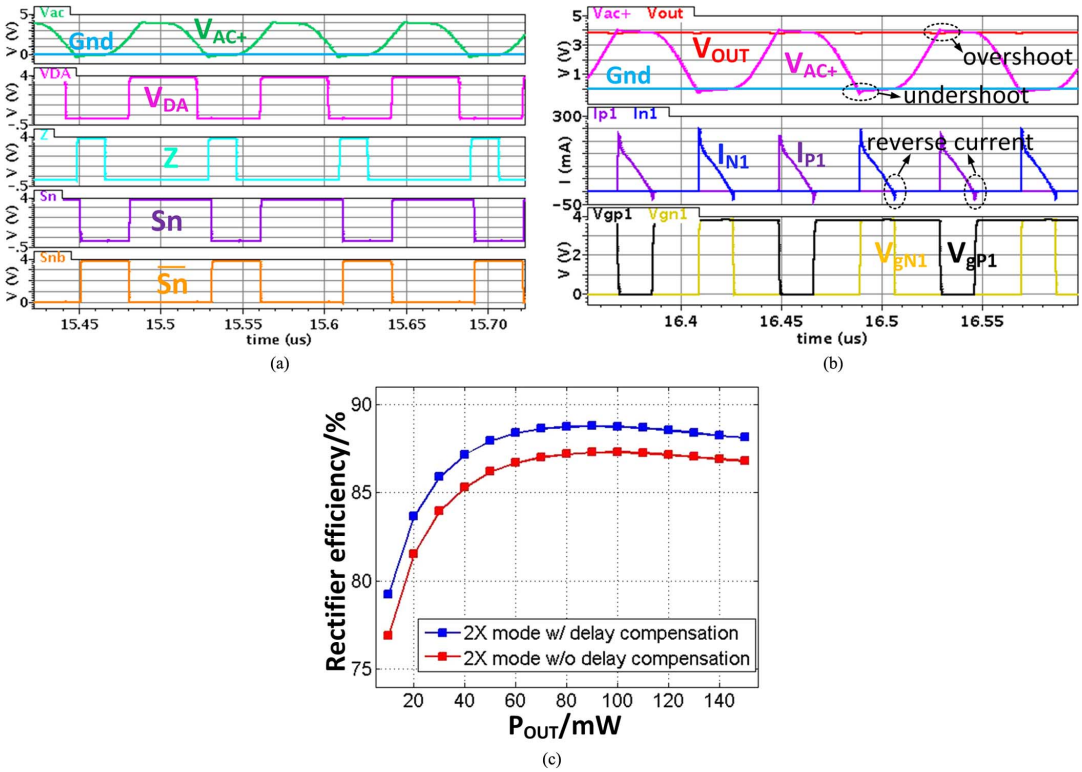

Fig. 5. (a) Operation waveforms of CMP1 (b) Operation waveforms of 1X/2X reconfigurable rectifier (c) Rectifier efficiency comparison between w/ and w/o delay compensation under 2X mode.

to high (low), and the comparator has a positive input offset voltage. When V_{AC} decreases and before it reaches zero, the comparator will respond to the positive input offset and the rising-edge delay of Z is compensated, which prevents voltage undershoot at V_{AC}. When Z is switched to high, Sn $(\overline{Sn})$ is switched to low (high) after the delay introduced by the delay cell and before the end of the conduction of the diode. The input offset voltage of the comparator becomes negative. When V_{AC} increases and before it reaches zero, the comparator starts to respond and the falling-edge delay of Z is compensated, and the reverse current is prevented. With the delays compensated by the introduced offset voltages, the efficiency of the rectifier is improved significantly. When En is low, all bias currents become zero and the comparator output Z is forced to be low. The comparator is disabled to save power.

Fig. 4(b) shows the schematic of the comparator $CMP3$ that is used to drive the PMOS power transistor. It is an up-down mirror image of that of $CMP1$ and $CMP2$. The operation principle is similar, but the transistor size ratios are different.

Simulation was performed to verify the effectiveness of the delay compensation method. A loading resistor of 200 Ω is used and $V_{\rm OUT}$ is set to be 3.6 V. The 1X/2X reconfigurable rectifier is configured in the 2X mode. The simulated waveforms of $CMP1$ are shown in Fig. 5(a). Fig. 5(b) shows the operation waveforms of the 1X/2X reconfigurable rectifier. With the offset-induced switching delay compensation, the overshoot and undershoot of V_{AC} as well as the reverse currents of M_{P1} (I_{P1}) and M_{N1} (I_{N1}) are small. Fig. 5(c) shows the efficiency of the rectifier with and without delay compensation under the 2X mode. For the latter, no offset is introduced into the comparators. Over a wide load range, the rectifier with switching-delay compensation has higher efficiency.

III. Proposed Reconfigurable Resonant Regulating Rectifier

Consider the input voltage V_{AC} with fixed amplitude. The 1X mode and the 2X mode of the reconfigurable rectifier will give different output voltages V_{1X} and V_{2X}, respectively, as shown in Fig. 6(a). If the rectifier is switched periodically between the two modes, $V_{\rm OUT}$ will settle at an intermediate voltage between V_{1X} and V_{2X} depending on the duty ratio D_0 defined as the portion of a mode-switching period for the rectifier to work in the 2X mode. The above PWM mechanism could be used to control $V_{\rm OUT}$, and thus we propose a reconfigurable resonant regulating (R^3) rectifier consisting of the 1X/2X reconfigurable rectifier regulated by a PWM controller, as shown in Fig. 6(b). The PWM controller senses $V_{\rm OUT}$ and compares it with the reference voltage $V_{\rm ref}$ by an error amplifier (EA). The output of EA (V_E) is then compared with the ramp signal by a comparator the output of which is sent to a D flip-flop (DFF). The clock signal of DFF is recovered from V_{AC} using a very small inverter. Mode switching is synchronized with the recovered clock to guarantee zero current switching (ZCS).

The R^3 rectifier could operate in the continuous mode (CM) or the discontinuous mode (DM) depending on the loading, as shown in Fig. 7. These modes are not to be confused with the continuous and discontinuous conduction modes (CCM and DCM) of a switching converter. In one switching cycle, I_{P1} and I_{N1} alternately charge the output capacitor, whether the rectifier is in the 1X mode or the 2X mode. Under heavy load

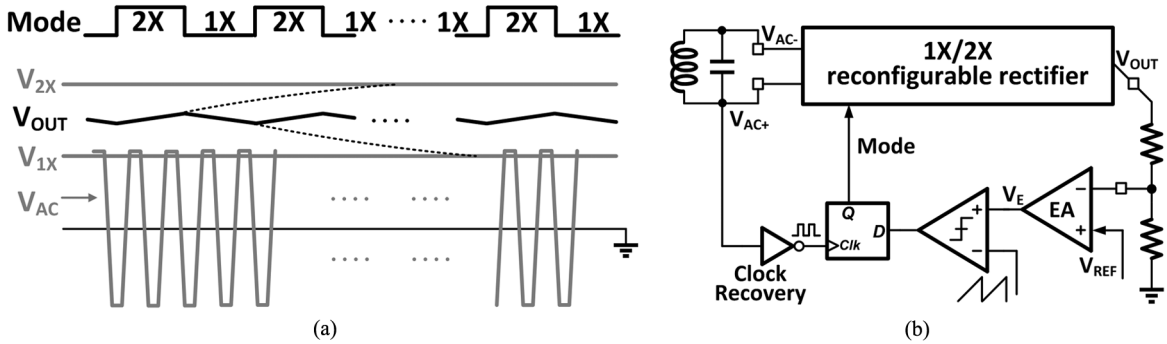

Fig. 6. (a) V_{OUT} regulation principle (b) Reconfigurable resonant regulating (R^3) rectifier.

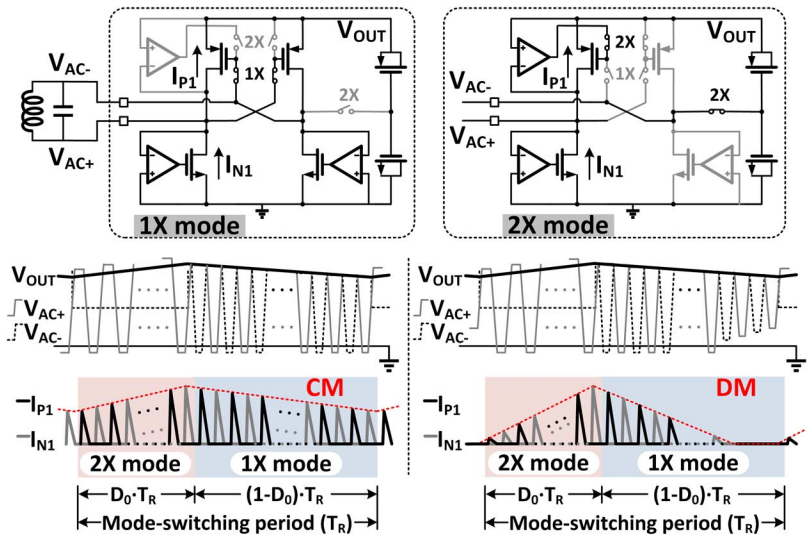

Fig. 7. Continuous mode (CM) & discontinuous mode (DM) of R^3 rectifier.

condition, the peaks of I_{P1} and I_{N1} are higher than zero, and the R^3 rectifier is said to work in continuous mode. Under light load condition, in each mode-switching period, the peaks of I_{P1} and I_{N1} will decrease to zero in the 1X mode. In such a case, the amplitude of $V_{AC+/-}$ is smaller than V_{OUT}, and there is no I_{P1} and I_{N1} to charge the output capacitor until the next mode-switching period starts, and this is discontinuous mode.

The proposed R^3 rectifier has several advantages over existing reconfigurable rectifiers. The 3R structure of [11] needs eight power components, while the R^3 rectifier has only five, making it more area-efficient and easier to be integrated on-chip. In the 3R structure, the maximum voltage is higher than $2V_{\mathrm{OUT}}$, while in the R^3 rectifier it is around V_{OUT}. Voltage stress of the devices is reduced and reliability is improved. Conversely, a lower voltage process may be used. In DM, the 3R rectifier is artificially disconnected from the load during the off time, resulting in abrupt boosting up of V_{OUT} that causes large voltage stress on the devices. An extra capacitor is also required at the input of the rectifier for voltage protection. In the R^3 rectifier, DM occurs when $V_{AC+/-}$ itself is smaller than V_{OUT} and no over-voltage protection issue arises.

IV. Data Uplink Communication Technique

In addition to the local PWM control loop, a global control loop through a wireless link is implemented to cater for large load and coupling variations, and it adjusts the transmitter power to vary the secondary input voltage V_{AC}. Fig. 8(a) shows the overall regulation control scheme. Fig. 8(b) shows the relationship of V_{1X} and V_{2X} with the load. The local PWM control loop (Rx loop) regulates V_{OUT} within $[V_{1X}, V_{2X}]$ that is denoted as Region 2 in Fig. 8(b). If the required output voltage $V_{\mathrm{OUT,req}}$ is located in either Region 1 or Region 3, the local loop is not able to regulate V_{OUT} to $V_{\mathrm{OUT,req}}$. A global control loop (Tx loop) is needed to increase (or decrease) the transmission power to move Region 2 up (or down) so that $V_{\mathrm{OUT,req}}$ is within Region 2 again. Indeed, whether $V_{\mathrm{OUT,req}}$ is within Region 2 is determined by the mode-switching duty ratio D_0 of the 2X mode. When D_0 increases, it means that $V_{\mathrm{OUT,req}}$ is closer to Region 3 and it will enter Region 3 when D_0 reaches 1. When D_0 decreases, $V_{\mathrm{OUT,req}}$ is closer to Region 1 and it will enter Region 1 when D_0 reaches 0. By feeding the digital equivalent of D_0 back to the transmitter, the global control loop knows which part of Region 2 that the R^3 rectifier is operating at and then issues the control action accordingly. Besides power control information, the status of the implant could be sent back periodically through this efficient data uplink communication channel.

Due to the size constraint of implant applications, a separate data communication channel is not preferred. Data backscattering through the power coupling coil is usually used for data

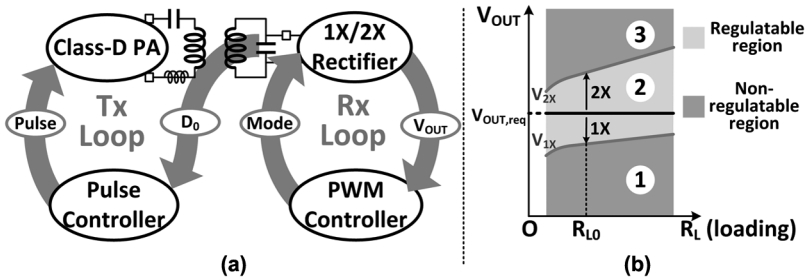

Fig. 8. Regulation region of R^3 rectifier.

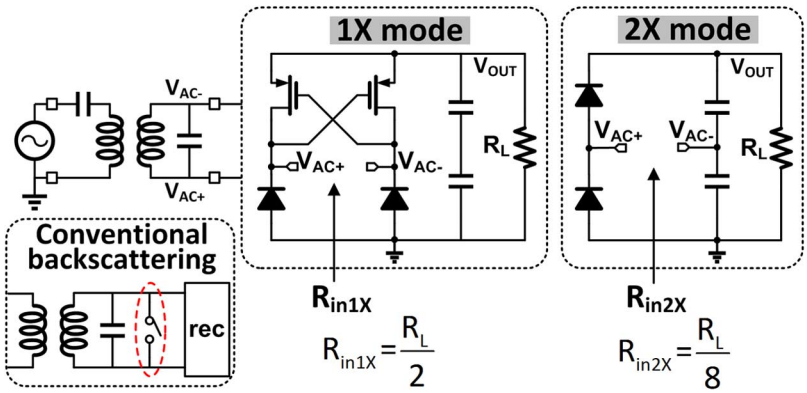

Fig. 9. Load shifting by mode switching in R^3 rectifier.

uplink communication [6], [15]. Backscattering is based on load shift, which is usually done by a data-controlled shunt switch as shown in Fig. 9 that interrupts power reception when the switch is turned on to short the secondary LC tank. The power transfer efficiency is degraded especially at high data rate, when the duty ratio of shorting the secondary LC tank is not negligible.

Now, assume all equivalent diodes of the proposed R^3 rectifier are ideal and the output capacitor is large. In the 1X mode it is configured as a full-wave bridge rectifier and the input resistance is $R_L/2$ [16]. In the 2X mode it is a voltage doubler and the input resistance is $R_L/8$ [16]. Mode switching results in load shift that could be used for backscattering. It has the advantages of continuous power reception, and is more energy-efficient, and the power transfer efficiency remains high even at high data rate. When compared to the conventional backscattering, the data link sensitivity of the proposed method is a little bit lower. The signal amplitude of the received data depends on the coupling and load conditions. The worst case occurs when the coupling is weak and the load current is heavy. The signal amplitude of the received data at the primary side is proportional to the load shift at the secondary side [16]. The conventional backscattering has a load shift between 0 and $R_L/2$ (assume that H-bridge rectifier is used). The proposed method has a load shift between $R_L/8$ (2X mode) and $R_L/2$ (1X mode), and the change in load is $3R_L/8$ [16]. When compared to the conventional backscattering, the received signal amplitude is reduced by 25%.

Mode switching of the R^3 rectifier induces an envelope shift of the primary coil voltage V_{L1} as shown in Fig. 10. A detection coil is used to sense V_{L1}, and is followed by a rectifier $Rec1$ to retrieve the envelope. The envelope is processed by a band-pass (BP) filter and a Schmitt comparator, and the mode-switching signal is obtained at *Data_Rx*.

The schematic of the data receiver is shown in Fig. 11. L_D is the detection coil and the coupling factor with the primary coil is constant. V_{L1} is scaled down and sensed across L_D. C_1 is a small capacitor used to stabilize the data receiver. The values of L_D and C_1 are chosen such that their resonant frequency is much higher than the carrier frequency of 13.56 MHz to avoid too much power absorption from the primary coil. $Rec1$ is a voltage doubler used to obtain the envelope. The BP filter is a second-order RC filter used to remove the DC offset and coupled noise at 13.56 MHz. Since the data is switching at the mode-switching frequency that is many times lower than the carrier frequency, it passes through the BP filter without attenuation. The resistor ladder provides the bias voltages for the BP filter and the Schmitt comparator. The output of the BP filter V_{Sig} is compared with $V+$ and $V-$ by the Schmitt comparator to recover the mode-switching signal at *Data_Rx*.

One issue is how to embed the data to be backscattered into the mode-switching waveform without changing it arbitrarily as it is used to regulate $V_{\rm OUT}$. Two methods are proposed next. The first is for general data transmission; and the second is for fast transmission of D_0, the duty ratio of the 2X mode.

A. Backscattering Data Using Phase Information of the Mode-Switching Waveform

In the R^3 rectifier, the duty ratio of the 2X mode is determined by $V_{\rm OUT}$ regulation and cannot be used to encode data. Instead, the phase of the mode-switching waveform can be considered. Fig. 12(b) shows our proposal of data encoding. Data '0' is encoded by the mode switching from 1X to 2X during one mode-switching cycle. Similarly, data '1' is encoded by the mode switching from 2X to 1X during one mode-switching cycle. In fact, the data is encoded into Manchester code based

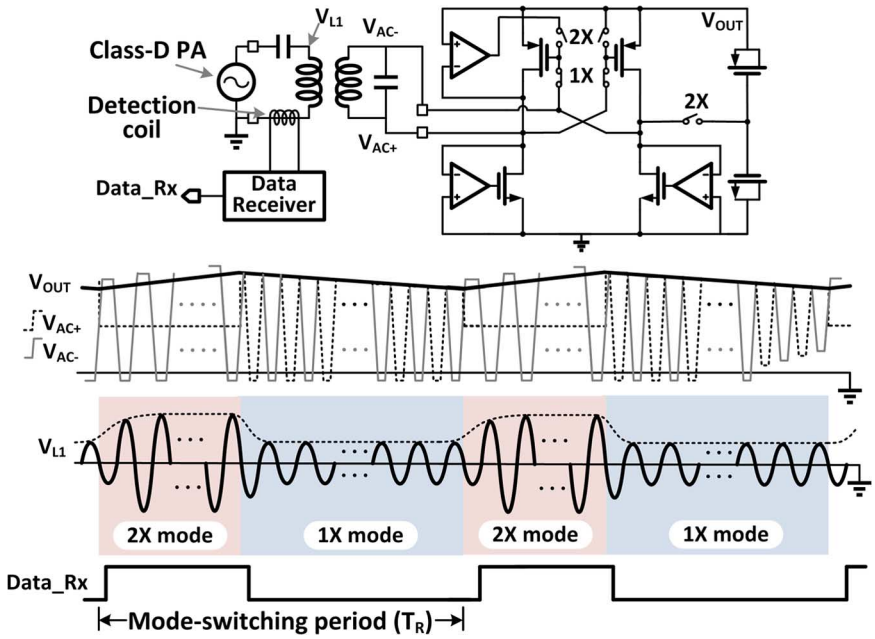

Fig. 10. Backscattering based on mode switching in R^3 rectifier.

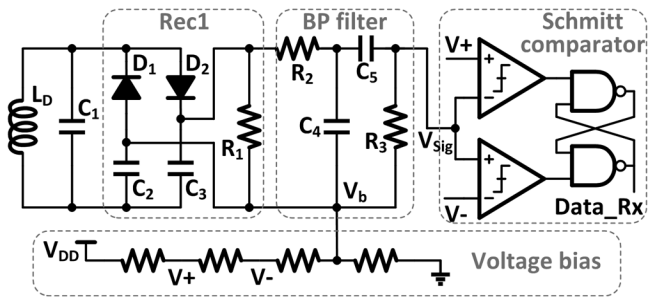

Fig. 11. Data receiver.

on mode switching, and it can be encoded independent of the value of D_0.

Manchester encoding is realized by a dual-mode ramp generator controlled by the data. If the data is '1', the ramp generator generates a trailing-edge ramp. By comparing this ramp with the output of the EA V_E, the rectifier is switched from 2X to 1X mode during the mode-switching cycle. If the data is '0', the ramp generator generates a leading-edge ramp and the rectifier is switched from 1X to 2X mode.

The data-controlled ramp generator is shown in Fig. 12(a). If *Data* is '1', $S+$ is ON and $S-$ is OFF. The current source I_2 and the switch M_P discharges and charges C_R respectively, and generates a trailing-edge ramp. If *Data* is '0', the roles of $S+$, I_2 and M_P are replaced by those of $S-$, I_1 and M_N, resulting in a leading-edge ramp. Comparing with the traditional load-switching based backscattering scheme, this ramp-based scheme backscatters the data to the primary side without affecting the local PWM control.

To decode the backscattered data at the primary side, we need to generate a reference clock *Clk_sample* to sample the data from the *Data_Rx* signal. *Clk_sample* is the delayed version of the rising clock of the mode-switching clock. However, the latter is not known at the primary side and during data backscattering, the phase of the rising edge of *Data_Rx* depends on the data and hence it cannot be directly used to obtain the mode-switching clock to track *Clk_sample*. To track *Clk_sample* from *Data_Rx*, we add a preamble word that consists of a string of '1' before sending the data. Since the preamble data is '1' and the rising edge of *Data_Rx* has a constant phase as shown in Fig. 12(c), the period of the ramping clock can also be obtained and *Clk_sample* can then be generated and tracked. To avoid *Clk_sample* from drifting over time, periodic preambles are added into the data streams. In doing so the uplink data rate is reduced. One way to mitigate *Clk_sample* drifting is to use a pre-determined period that is known to both the primary and the secondary sides. In the secondary side, the system clock is recovered from the power carrier clock (13.56 MHz in our case). A specific count of the system clock can then be used to trigger the $S+$ and $S-$ switching in the ramp generator and hence the mode-switching period is known. At the primary side, we only need to know the preamble word at the initiation of data transmission to recover the rising edge of *Data_Rx* to track *Clk_sample*. After that the same counts of the power carrier clock can be used to periodically generate *Clk_sample* without the need of adding periodic preamble.

B. Sending D_0 Through Backscattering

For the global control loop, only D_0 is needed to be sent back to the transmitter. The value of D_0 is encoded and backscattered to the primary side using the method presented in the previous sub-section. However, it will take many mode-switching cycles that affect the speed of the global control loop. Nevertheless, observe that the waveform of *Data_Rx* in Fig. 10 is very close to the waveform of *Mode*, and we may directly measure the duty ratio of *Data_Rx* at the primary side to obtain D_0 using a counter and the reference clock presented above. This method takes only one mode-switching cycle to transmit D_0 and is very fast. The accuracy is good enough for the global power control.

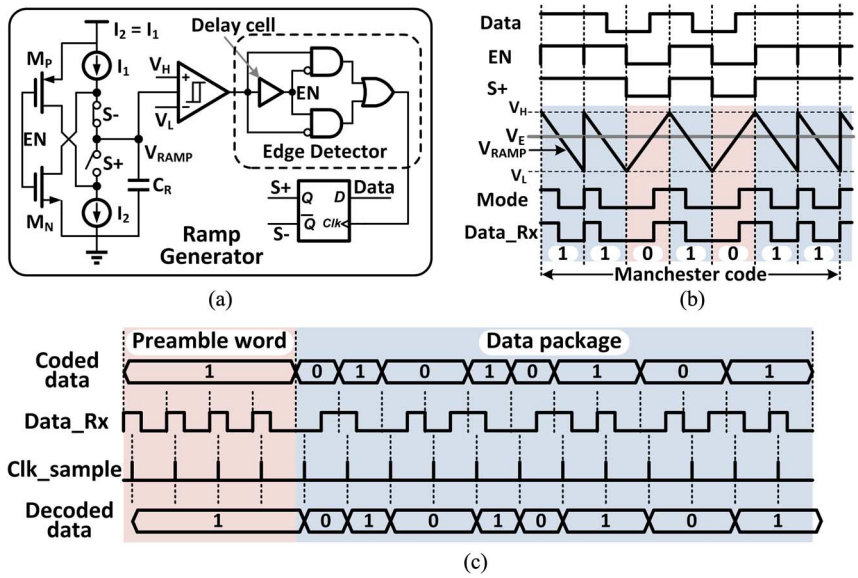

Fig. 12. (a) Data controlled ramp generator. (b) Manchester coding. (c) Data decoding.

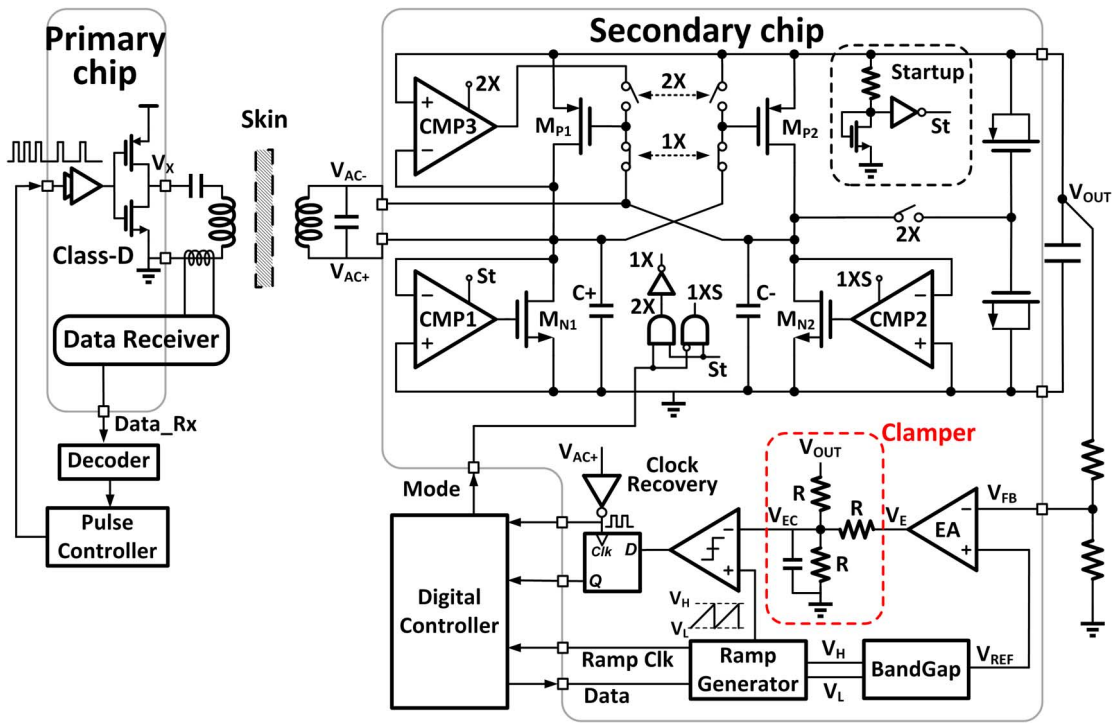

Fig. 13. Proposed wireless power transfer system.

V. Proposed WPT System

The wireless power transfer (WPT) system that employs the R^3 rectifier and the backscattering methods is shown in Fig. 13. The local PWM control loop of the R^3 rectifier not only regulates $V_{\rm OUT}$, but also backscatters D_0 to the primary side for the global control loop. According to the received D_0, the primary side regulates the transmission power using bang-bang control.

A. The 1X/2X Rectifier

Before analyzing the local loop, we first take a look at the characteristic of the 1X/2X rectifier using HSPICE simulation. The 1X/2X rectifier is driven by an ideal AC voltage source with $V_{AC} = 2.2$ V and an internal resistance of 5 Ω. $V_{\rm OUT}$ is obtained as a function of D_0, as shown in Fig. 14, with $R_L = 200\ \Omega$ and 1 kΩ, respectively. In this WPT system, D_0 is regulated to around 0.5. The voltage gain H_{D0} $(= \Delta V_{\rm OUT}/\Delta D_0)$ under this case is around 1.

At $V_{\rm OUT}$, the output pole $-p_L$ due to the loading resistor R_L and the output capacitor C_L is

$$p_L = \frac{1}{mR_LC_L} \tag{1}$$

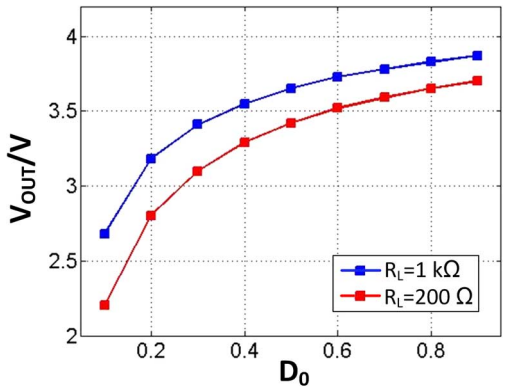

Fig. 14. $V_{\rm OUT}$ vs. D_0 of the 1X/2X rectifier.

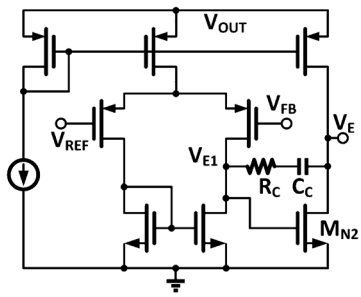

Fig. 15. The error amplifier (EA).

where mR_L $(0 < m < 1)$ is the equivalent load resistance correlated with D_0. With D_0 regulated to around 0.5, the coefficient m is almost constant. The transfer function $H_D(s)$ from D_0 to $V_{\rm OUT}$ is given by

$$H_D(s) = \frac{V_{\rm OUT}}{D_0} = \frac{H_{D0}}{1 + s/p_L}. \tag{2}$$

B. The Error Amplifier (EA)

The EA is a classic two-stage OTA as shown in Fig. 15. The compensator $A(s)$ is simply the EA with Miller capacitor C_C in series with the compensation resistor R_C. Now, the transconductance of M_{N2} is g_{m2}; the output resistance at V_{E1} is R_{E1}; and the loading resistor at V_E including the clamper is R_E. Standard derivation shows that $A(s)$ consists of one LHP zero $-z_1$ and two split poles $-p_1$ and $-p_h$. By designing p_h to be at negligibly high frequency, $A(s)$ is given by

$$A(s) = A_0 \cdot \frac{1 + s/z_1}{1 + s/p_1} \tag{3}$$

where the DC gain A_0, the LHP zero $-z_1$ and the dominant pole $-p_1$ are given by

$$A_0 \approx g_{m1} g_{m2} R_{E1} R_E \tag{4}$$

$$z_1 = \frac{1}{(R_C - 1/g_{m2})C_C} \approx \frac{1}{R_C C_C} \tag{5}$$

$$p_1 \approx \frac{1}{g_{m2} R_{E1} R_E C_C} \tag{6}$$

respectively. By neglecting the high-frequency pole $-p_h$, $A(s)$ realizes Type-II compensation.

C. The D_0 Clamper

The proposed backscattering methods are based on mode switching as discussed in Section IV, and as such D_0 can neither be as high as 100% nor as low as zero. Now, the voltage swing of the output of EA (V_E) is $[0, V_{\rm OUT}]$, and a clamper is added such that the voltage swing of V_{EC} is restricted to $[V_{\rm OUT}/3, 2V_{\rm OUT}/3]$. In designing the ramp generator for mode switching, the high threshold V_H should be higher than $2V_{\rm OUT}/3$ and the low threshold V_L should be lower than $V_{\rm OUT}/3$, and D_0 would then be clamped in a region that is larger than zero and smaller than 100%. The transfer function of the clamper $H_C(s)$ has a voltage gain of 1/3 and a pole $-p_C$ (at V_{EC}) that is located at a high frequency. Hence,

$$H_C(s) = \frac{1}{3(1 + s/p_C)}. \tag{7}$$

D. The Local Control Loop

By combining the results obtained in the previous two subsections, the transfer function $H_{FB}(s)$ from $V_{\rm OUT}$ to D_0 is

$$H_{FB}(s) = -A(s)H_C(s)/V_{\rm ramp} \tag{8}$$

where $V_{\rm ramp}$ $(= V_H - V_L)$ is the voltage excursion of the ramp signal. Therefore, the local control loop transfer function $T(s)$ is

$$\begin{aligned} T(s) &= -H_{FB}(s) \cdot H_D(s) \\ &= T_0 \cdot \frac{(1 + s/z_1)}{(1 + s/p_1)(1 + s/p_L)(1 + s/p_C)} \end{aligned} \tag{9}$$

where

$$T_0 = \frac{A_0 H_{D0}}{3V_{\rm ramp}}. \tag{10}$$

By designing the zero $-z_1$ to locate between $-p_1$ and $-p_L$, and $-p_C$ to be higher than the gain-bandwidth product of T(s) for adequate phase margin, Type-II compensation is achieved.

E. The Global Control Loop

The series-matched primary coil is driven by a Class-D power amplifier, and the output power is controlled by the pulse controller through switching-frequency modulation. The PA's output V_X is only switched at zero current for high efficiency, making the switching frequency of V_X cannot be controlled smoothly. The $\Sigma\Delta$ modulator in [9]is used to achieve smooth control of the average switching frequency of V_X. The backscattered D_0 is obtained by the data detector for the pulse controller to regulate the transmitter power. Bang-bang control is used and D_0 is regulated within the upper bound of 0.6 and the lower bound of 0.4. Only when D_0 is outside the two bounds should the global control loop be activated.

VI. Measurement Results

The power transmitter and receiver (except for the digital controllers) are fabricated in a 0.35 μm CMOS process. The die photo is shown in Fig. 16(a). The digital controller at the secondary side, the data decoder and the pulse controller at the primary side are implemented in FPGA. The primary, secondary

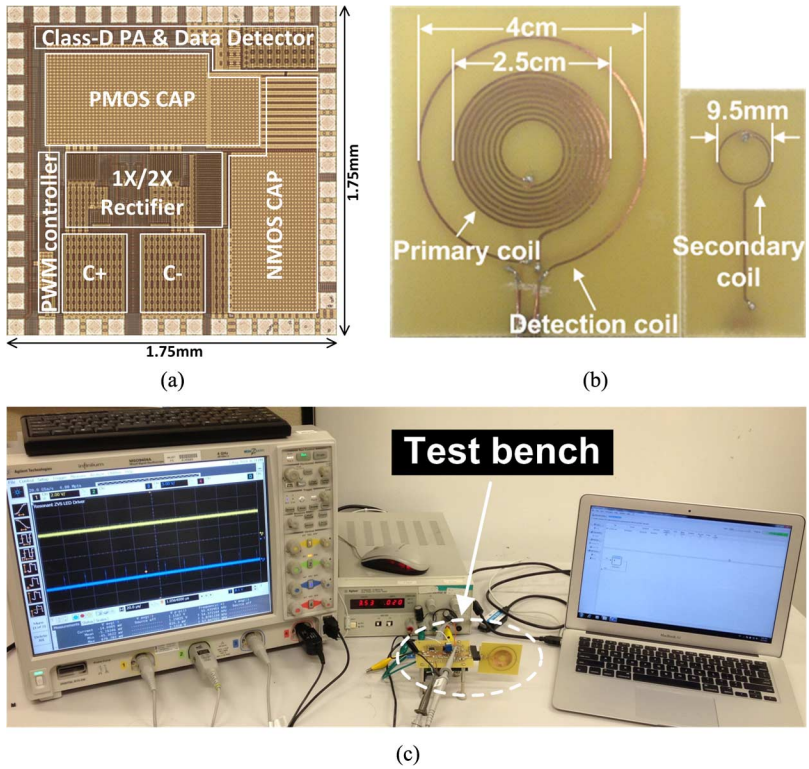

Fig. 16. (a) Die photo (b) Coils design (c) Testing setup.

TABLE I
COILS SPECIFICATION

Coils	Diameter	Inductance	Quality factor @13.56MHz
Primary coil	2.5cm	3.4 μH	61
Secondary coil	9.5mm	0.19 μH	29
Detection coil	4cm	0.42 μH	44

and detection coils are shown in Fig. 16(b). Table I summarizes the design parameters of the coils. The test setup is shown in Fig. 16(c).

The carrier frequency of the power link is 13.56 MHz. The mode-switching frequency was designed to be 500 kHz that was verified by simulation, which means that the uplink data rate can be up to 500 kbps. This data rate is comparable to the state-of-the-art conventional method [17]where an uplink data rate of 1.13 Mbs is reported. In [17], the power link and the data link share the same pair of coils that is similar to our approach. However, during the measurement of the fabricated chips, the output of the band-pass filter of the data receiver at the primary side was found to have some noise at 13.56 MHz, which is coupled from the primary coil. The noise degraded the BER and therefore a lower mode-switching frequency (56 kHz) was used to shift the band-pass filter response far away from 13.56 MHz in the spectrum. V_{OUT} is designed to be 3.6 V, and is used to drive a periodic current pulse signal into the eye tissue. The measured waveforms of V_{OUT}, V_{AC}, and the mode signals under CM and DM are shown in Fig. 17(a) and (b), respectively. When the output power P_{OUT} is 40 mW (heavy load), the R^3 rectifier works in continuous mode. The amplitude of $V_{AC+/-}$ is always larger than 3.6 V in the 1X mode. When P_{OUT} is 10 mW (light load), the R^3 rectifier works in discontinuous mode. The amplitude of $V_{AC+/-}$ is only larger than 3.6 V at the beginning of the 1X mode and then gradually becomes lower than 3.6 V in the rest of the 1X mode.

Fig. 17(c) shows how the backscattered data is encoded into Manchester code on the *Mode* signal and detected at the primary side by the data receiver without affecting V_{OUT} regulation. Fig. 17(d) shows the operation of the decoder. *Clk_sample* tracks the rising edge of *Data_Rx* in the preamble with a phase offset and is used to sample *Data_Rx* to obtain the correct data.

The operation of the local Rx PWM loop catered for small coupling variation is shown in Fig. 17(e). The load resistor R_L is 1 kΩ. When the coil distance changes from 1 cm to 0.75 cm, V_{OUT} is regulated at 3.6 V by the Rx loop through D_0 control. Observe that the duty ratio of the 2X mode (D_0) increases when the distance is changed from 0.75 cm to 1 cm. For a larger coupling variation both the global power control loop and the local Rx PWM loop have to be used, as shown in Fig. 17(f). R_L is still fixed at 1 kΩ. When the coil distance is changed from 1 cm to 2 cm, V_{OUT} cannot be regulated at 3.6 V by the Rx loop alone. The Tx loop helps regulating V_{OUT} by adjusting the transmission power through increasing the average switching frequency of the PA's output V_X.

Fig. 17(g) and (h) show the transient response under small load and large load changes, respectively. The coil distance is fixed at 1 cm. When the load power changes between 10 mW and 20 mW, V_{OUT} can be regulated at 3.6 V by the Rx loop alone, as shown in Fig. 17(g). The tracking time is 1 ms. Fig. 17(h) shows the load transients when the load changes between 10 mW and 60 mW. The coil distance is still fixed at 1 cm. Direct backscattering method is used to send D_0 for

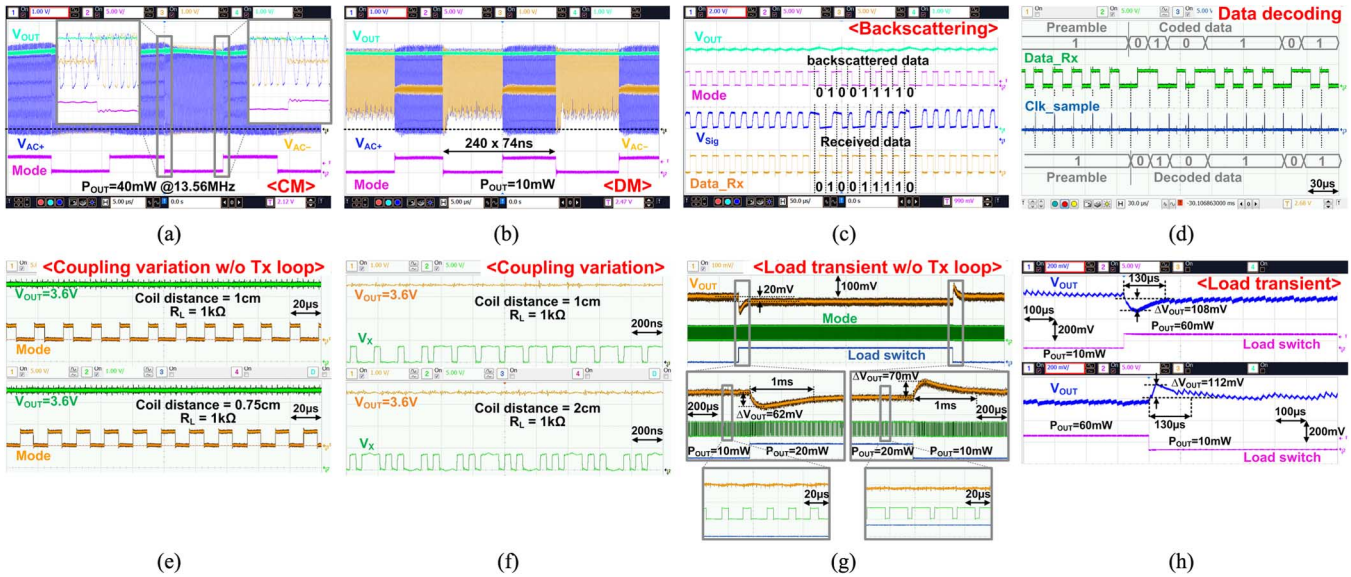

Fig. 17. Measured waveforms of (a) R^3 rectifier under CM, (b) R^3 rectifier under DM, (c) the data backscattering, (d) the data decoding, (e) the coupling variation effect with RX loop only, (f) the coupling variation with both TX and RX loop, (g) the load transient with RX loop only, and (h) the load transient with both TX and RX loop.

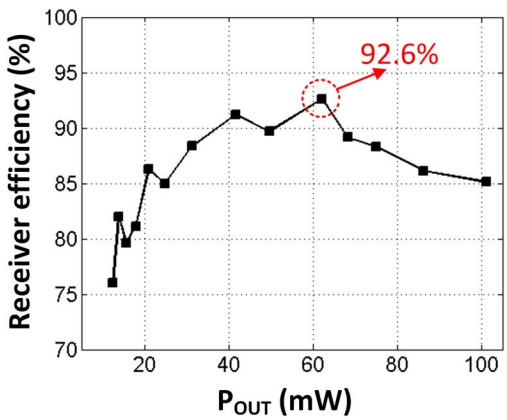

Fig. 18. Measured receiver efficiency.

TABLE II
COMPARISONS WITH PREVIOUS WORKS

	Lu [3] ISSCC13	Lee [10] TCAS-II12	Shinoda [9] ISSCC12	Choi [11] JSSC13	This work
Rx coil diam.	18mm	30mm	N/A	N/A	**9.5mm**
V_{OUT}	1.27~4V	3.1V	15V	5V	**3.6V**
$P_{OUT,Max}$	32mW	37mW	0.52W	6W	**102mW**
Power carrier Freq.	13.56MHz	13.56MHz	13.56MHz	6.78MHz	**13.56MHz**
Mode-switching Freq.	N/A	N/A	N/A	847.5kHz	**56.5kHz**
Regulation site	N/A	Rx	Tx	Rx	**Rx & Tx**
Data link	N/A	N/A	Wire	Wire	**Backscattering**
% Reg. [11]	N/A	33%	2.7%	3.3%	**3.1%**
Tracking time	N/A	N/A	30µs[1]	500µs	**130µs[2]**
Receiver eff.	84.2%	77%	N/A	86%	**92.6%**
Total eff.	N/A	N/A	50%	55%	**50%**
Process	CMOS 0.35µm	CMOS 0.5µm	HVCMOS 0.18µm	BCD 0.35µm	**CMOS 0.35µm**

1. Feedback is based on a wire 2. Feedback is based on wireless link

fast load-transient response. $V_{\rm OUT}$ cannot be regulated at 3.6 V by the Rx loop alone and the global control is also used for regulation. The overshoot and undershoot are around 110 mV and the settling time is less than 130 μs.

The measured receiver efficiency (the ratio of $P_{\rm OUT}$ to the input power of the rectifier) for different $P_{\rm OUT}$ ranging from 10 to 100 mW is summarized in Fig. 18. The power overhead of the PWM controller is included. In light load, the switching loss of the active diodes degrades the efficiency. In heavy load, the conduction loss of the active diodes degrades the efficiency. At $P_{\rm OUT} = 60$ mW, the maximum efficiency of 92.6% is achieved. At a coil distance of 0.3 cm and $P_{\rm OUT} = 60$ mW, the maximum total power transfer efficiency including the losses in the Class-D PA, the coupling coils and the receiver is 50%.

Table II summarizes the performance comparison with previous works. Our design has the smallest secondary coil, and our dual-loop control for $V_{\rm OUT}$ regulation achieves fast load-transient response. Moreover, the receiver efficiency is compared favorably with previous works.

VII. CONCLUSIONS

A 13.56 MHz wireless power transfer system with a R^3 rectifier and wireless power control for biomedical implants is presented. Output voltage regulation is achieved through two mechanisms: the local PWM loop at the secondary side controls the mode-switching duty cycle of the 2X mode (D_0); and the global power control loop adjusts the transmitter power of the primary coil according to the digitized D_0 fed back from the secondary side wirelessly, to adapt to large load and coupling variations. Two novel backscattering uplink techniques are proposed using the characteristics of mode switching of the R^3 rectifier for energy efficiency and fast load-transient responses. The measured maximum received power and receiver efficiency are 102 mW and 92.6%, respectively. For large load transients, the overshoot and the undershoot are less than 110 mV and the settling time is less than 130 μs.

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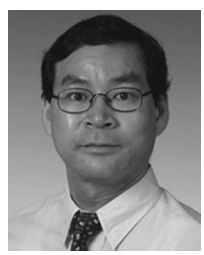

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