A CMOS Voltage Reference Based on Weighted Difference of Gate-Source Voltages between PMOS and NMOS Transistors for Low Dropout Regulators

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Abstract

A CMOS voltage reference, which takes advantage of weighted difference of the gate-source voltages between a PMOS and an NMOS transistor operating in saturation region, is presented in this paper. The reference has been implemented in a standard 0.6-μm CMOS process ($V_{thn} \approx |V_{thp}| \approx 0.9$ V@0 ^oC) and gives a temperature coefficient of not greater than 62 ppm/^oC from 0 to 100 ^oC without trimming, while consuming a maximum of 9.7 μA with a minimum supply of 1.4 V. The worst-case line regulation is ±0.17 %/V. The occupied chip area is 0.055 mm^2. The proposed reference has been applied to a 10-mA CMOS low dropout regulator, and a temperature coefficient of 94 ppm/^oC is achieved when the regulator delivers maximum load current.

1. Introduction

Voltage reference is an important building block in power converters. The specifications of a voltage reference such as temperature coefficient (TC) and line regulation (LR) directly affect the performance of the power converters. A bandgap voltage reference is generally used since, as shown in Table 1 [1], it has a low supply- and temperature-dependences.

However, CMOS technology remains the mainstream in circuit design due to its the relatively low fabrication cost and short turn-around period. It is expected that the whole system, including the voltage reference, can be implemented in CMOS technology. As a result, voltage references based on threshold voltage difference were proposed [2], [3]. This type of voltage reference is implemented by a pair MOS transistors with different values of threshold voltages, which are controlled by different levels of ion implantation. The temperature-dependence is highly affected by the process variations and bias current level. Moreover, the absolute value of these voltage references is based on the threshold voltages, and it is not as stable as the bandgap reference voltage of approximately 1.25 V. However, it is less important than the temperature-dependence since the absolute value can be compensated by system design [3]. Low dropout regulator, as shown in Fig. 1, is one of the applications in which the output voltage is defined by the resistive feedback network, and the output voltage can be easily adjusted by an appropriate resistor ratio.

Method	*Proposed CMOS reference*	Bandgap reference [1]	E-D reference [1]
Process	*CMOS*	BiCMOS	DMOS
Supply dependence	*±0.17% (max)*	±1%	±1%
Temperature dependence	*±0.31% (max)*	±0.4%	±1%

Table 1: Comparison of different type voltage references.

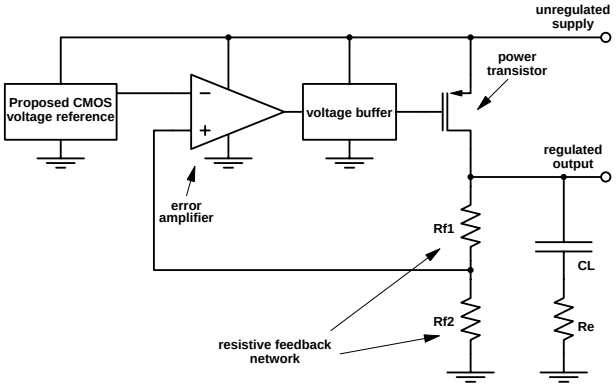

Fig. 1: Structure of a low dropout regulator.

In this paper, a voltage reference in a standard CMOS technology based on gate-source voltage difference between a PMOS and an NMOS transistor is presented. It is suitable for power converter applications. The main features of the proposed reference circuitry are: (i) use of standard MOS transistors to provide a low TC reference voltage without requiring additional process control, (ii) low sensitivity to bias current and hence a good TC and line regulation, and (iii) the precision on trimming is less than bandgap voltage reference.

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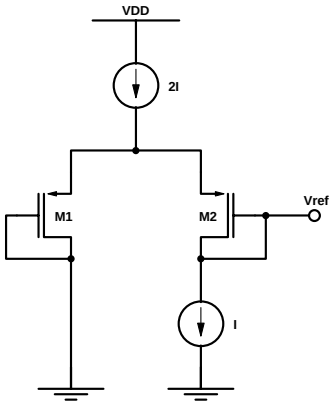

Fig. 2: Simplified structure of the voltage reference based on threshold voltage difference.

2. Brief Review on Voltage Reference Based on Threshold Voltage Difference

The simplified structure of a voltage reference generated by threshold voltage difference is shown in Fig. 2. Both the transistors are PMOS transistors (similar structure can be implemented by NMOS transistors). M_1 has a larger threshold voltage than M_2, and this is available in multi-threshold-voltage technologies. The reference voltage (V_{ref}) is given by [2]

$$V_{ref} = |V_{GS1}| - |V_{GS2}| = \left(|V_{thp1}| - |V_{thp2}|\right) + \sqrt{I}\left(\sqrt{\frac{1}{K_1}} - \sqrt{\frac{1}{K_2}}\right) \quad (1)$$

where K_1 and K_2 are the transconductance parameter of M_1 and M_2, respectively. As stated in [2], the bias current and mobility are temperature-dependent, and a complete cancellation on the temperature effect is difficult to achieve. Thus, a low bias current is generally used, and the expression of the reference voltage is simplified to

$$V_{ref} \approx |V_{thp1}| - |V_{thp2}| \quad (2)$$

A good process control makes the TCs of the threshold voltages of M_1 and M_2 close to each other, and a low TC reference voltage can be obtained.

From the above discussion, it is concluded that the voltage reference requires: (i) extra fabrication steps to implement multi-threshold-voltage devices, (ii) a good process control to make TCs of the threshold voltages of M_1 and M_2 close to each other, and (iii) preferably, a supply- and temperature-insensitive low-magnitude bias current to improve the TC and line regulation.

3. Proposed CMOS Voltage Reference

The proposed CMOS voltage reference is shown in Fig. 3. The circuit is formed by three parts: (i) a low-voltage bias circuit (M_1-M_4 and R_B), (ii) a start-up circuit

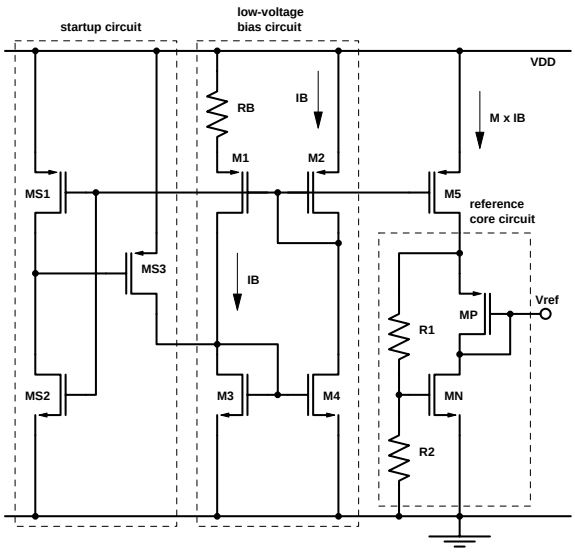

Fig. 3: The proposed CMOS voltage reference.

(M_{S1}-M_{S3}), and (iii) the reference core circuit (M_P, M_N, R_1 and R_2). By choosing a long channel length to eliminate the channel modulation effect and biasing the transistors in saturation region, the generated bias current at T_o = 0 °C is given by

$$I_B(T) = \frac{2}{\mu_p(T) C_{ox} R_B{}^2}\left[\frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}}\right]^2 = \frac{2}{\mu_p(T_o) C_{ox} R_B{}^2}\left[\frac{1}{\sqrt{\left(\frac{W}{L}\right)_2}} - \frac{1}{\sqrt{\left(\frac{W}{L}\right)_1}}\right]^2 \left(\frac{T}{T_o}\right)^{\beta_{\mu p}} = I_B(T_o)\left(\frac{T}{T_o}\right)^{\beta_{\mu p}} \quad (3)$$

where μ_p, C_{ox}, $\beta_{\mu p}$ and W/L are the mobility, the capacitance of gate oxide, mobility exponent [4] and channel width to channel length ratio, respectively. With the current mirror M_5, the injected current to the reference core circuitry is M times of I_B.

Assuming that the current flowing through R_1 and R_2 is negligible, the bias current to M_P and M_N is also M times of I_B. The reference voltage is given by

$$V_{ref} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{GSn} - |V_{GSp}| \quad (4)$$

A key design condition is that both M_P and M_N are biased deep in saturation region. Therefore, the gate-source voltage is governed by the fundamental equation of MOS transistors in saturation region. The temperature dependence of the reference voltage is therefore obtained by differentiating (4) with respect to the temperature. It is given by (5)

$$\frac{\partial V_{ref}}{\partial T} = \left(1+\frac{R_1}{R_2}\right)\frac{\partial V_{GSn}}{\partial T} - \frac{\partial |V_{GSp}|}{\partial T}$$
$$= \left[-\left(1+\frac{R_1}{R_2}\right)\beta_{vthn} + \beta_{vthp}\right] + \frac{\beta_{\mu p}}{T_o}\sqrt{\frac{2MI_B(T_o)}{\mu_p(T_o)C_{ox}\left(\frac{W}{L}\right)_p}} \times \left[\left(1+\frac{R_1}{R_2}\right)\left(\frac{1}{2}+\frac{\beta_{\mu n}}{2\beta_{\mu p}}\right)\sqrt{\frac{\mu_p(T_o)\left(\frac{W}{L}\right)_p}{\mu_n(T_o)\left(\frac{W}{L}\right)_n}}\left(\frac{T}{T_o}\right)^{\frac{\beta_{\mu p}+\beta_{\mu n}-2}{2}} - \left(\frac{T}{T_o}\right)^{\beta_{\mu p}-1}\right] \quad (5)$$

where β_{vthp} and β_{vthn} are the TCs of the threshold voltages of PMOS and NMOS transistors, respectively, and $\beta_{\mu p}$ and $\beta_{\mu n}$ are the mobility exponents of PMOS and NMOS transistors, respectively [4].

From (5), temperature-dependence of the proposed voltage reference is governed by a linear term and a high-order term. In order to obtain $\left.\frac{\partial V_{ref}}{\partial T}\right|_{T=T_r} = 0$ at room temperature (where T_r is room temperature), the linear term is set to zero by the resistor ratio, which is given by

$$\frac{R_1}{R_2} = \frac{\beta_{vthp}}{\beta_{vthn}} - 1 \quad (6)$$

and the high-order term is set to zero at $T = T_r$ by the transistor size ratio, which is given by

$$\frac{\left(\frac{W}{L}\right)_p}{\left(\frac{W}{L}\right)_n} = \frac{\frac{\mu_n(T_o)}{\mu_p(T_o)}\left(\frac{T_r}{T_o}\right)^{\beta_{\mu p}-\beta_{\mu n}}}{\left(\frac{\beta_{vthp}}{\beta_{vthn}}\right)^2\left(\frac{1}{2}+\frac{\beta_{\mu n}}{2\beta_{\mu p}}\right)^2} \quad (7)$$

Since the temperature-dependence of the threshold voltage is not exactly linear and a complete cancellation of the temperature-dependence of μ_p and μ_n cannot be achieved in the whole temperature range, there is non-linear residue appearing on the reference voltage.

The above analysis is based on the first-order equations of MOS transistors operating in saturation region. The conditions stated in (6) and (7) are independent of the magnitude of bias current. However, if the bias current decreases, M_N and M_P may leave saturation region and enter weak inversion region. Thus, a minimum supply voltage must be fulfilled in order to avoid the current source M_5 being forced to operate in triode region.

The sensitivity of the TC of the reference voltage on the variation of R_1 to R_2 ratio (due to doping gradient and non-optimized layout) is reduced. Considering the resistor ratio in (6) is increased by a small amount, a negative TC appears in the first term due to incomplete compensation of β_{vthp} and β_{vthn}. However, a positive TC created by the mobility terms in the second term compensates the effect. The phenomenon is similar when the ratio is decreased by a small amount. Due to this effect, the sensitivity of the reference circuit on the resistor ratio is reduced, and thus the resolution of the trimming circuit can be reduced substantially. Since β_{vthp}, β_{vthn}, $\beta_{\mu p}$ and $\beta_{\mu n}$ can be modelled accurately and are stable from run to run and lot to lot by a certain extent, no trimming is required to achieve an acceptable range of TC.

The minimum supply voltage should be considered at the lowest operation temperature as V_{thn} and $|V_{thp}|$ are maximum at that temperature. Since both M_N and M_P operate in saturation region, it is suggested to set V_{GSn} and $|V_{GSp}|$ larger than their threshold voltages by at least 100 mV [5]. Thus, the minimum supply voltage (V_{smin}) is given by

$$V_{s\min} = \left(1+\frac{R_1}{R_2}\right)\cdot V_{GSn}@0^oC + \left|V_{DS5(sat)}\right| \quad (8)$$

It is possible for the proposed CMOS voltage reference to operate in sub-1-V supply if a CMOS technology with low threshold voltage devices (< 0.65 V@0 ^oC) is used.

4. Experimental Results

The proposed voltage reference shown in Fig. 3 was successfully implemented in AMS (Austria Miko Systeme International AG, Austria) 0.6-μm CMOS process ($V_{thn} \approx |V_{thp}| \approx$ 0.9 V@0 ^oC). It can be implemented in other CMOS processes with changes on the resistor ratio and the transistors size ratio. Optional high resistive poly resistor (about 1.2 kΩ/sq.) is used to reduce the chip area. The micrograph is shown in Fig. 4, and the occupied chip area is 0.055 mm^2, which is much smaller than the conventional bandgap reference due to the absence of parasitic vertical BJT in the design.

A total of 11 samples from two consecutive runs were measured, and Table II summarizes the performance. The minimum supply voltage is 1.4 V, and it can be reduced if lower threshold voltage devices are used. The maximum supply current is 9.7 μA at 100 ^oC. Of all the samples, the worst-case line regulation is ±0.17%/V. A minimum TC of 2.7 ppm/^oC is achieved, and the worst-case TC is 62 ppm/^oC. Fig. 5 shows a sample with TC of about 24 ppm/^oC at 1.4-V, 2-V and 3-V supply. An intentional variation on the resistor ratio by +6.23% is preformed and is shown in Fig. 6. The change on the TC is only from 24 to 50 ppm/^oC. This experimental result verifies the theoretical analysis on the low sensitivity of the proposed CMOS voltage reference on the resistor ratio.

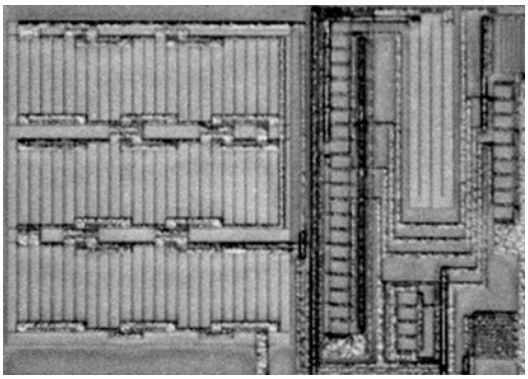

Fig. 4: Micrograph of the proposed CMOS voltage reference.

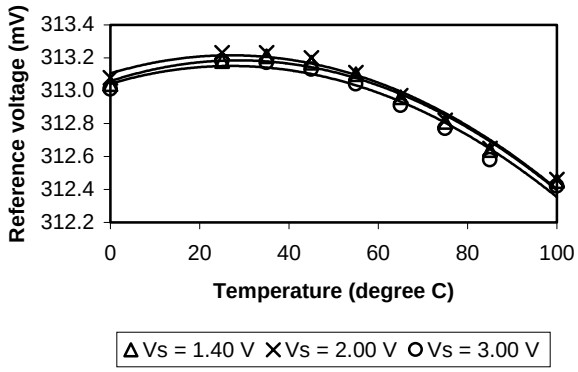

Fig. 5: TCs (nominal) of the proposed CMOS voltage reference at different supply voltages.

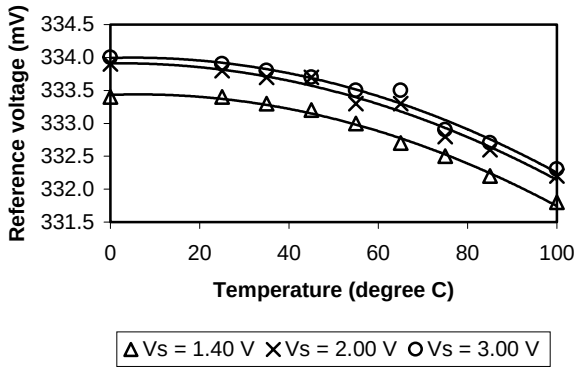

Fig. 6: TCs (resistor ratio off by +6.23%) of the proposed CMOS voltage reference at different supply voltages.

The proposed CMOS voltage reference is applied to a 10-mA low dropout regulator to demonstrate its application on power converter. A proposed voltage reference with TC of 59 ppm/^{o}C is used to provide the reference voltage to the regulator, and the regulator has a TC of 94 ppm/^{o}C when it delivers maximum load current. The increase in TC at the output of the regulator is due to the temperature-dependent offset voltage generated in the error amplifier of the regulator.

Supply voltage	1.4 to 3 V
Supply current	9.7 μA (max)
Reference voltage	302.24±12 mV
TC (0 to 100 ^{o}C)	62 ppm/^{o}C (max)
Line regulation	±0.17 %/V (max)

Table II: Performance of the proposed CMOS voltage reference (a total of 11 samples in two consecutive runs were measured).

5. Comparison with Existing Voltage References

A comparison of the proposed CMOS voltage reference on temperature- and supply-dependences with bandgap reference and enhancement-depletion MOS reference is shown in Table I. From the comparison, it is experimentally proven that the proposed voltage reference provides a comparable performance on temperature-dependence and a better performance on supply-dependence.

6. Conclusion

A voltage reference, which is compatible in standard CMOS, has been presented. The circuit uses MOS transistors operating in saturation region and resistors only. Both theoretical analysis and experimental results show that the sensitivity on the resistor ratio is low. The temperature-dependence and line regulation are good, and its performance is suitable for power converter applications. In addition, the application of the proposed voltage reference is demonstrated by a low dropout regulator.

7. References

[1] T. Kawahara, T. Kobayashi, Y. Jyouno, S.-I. Sacki, N. Miyamoto, T. Adachi, M. Kato, A. Sato, J. Yugami, H. Kume and K. Kimura, "Bit-Line Clamped Sensing Multiplex and Accurate High Voltage Generator for Quarter-Micron Flash Memories," *IEEE Journal of Solid-State Circuits*, vol. 31, pp.1590-1599, Nov. 1996.

[2] B.-S. Song and P. R. Gray, "Threshold-Voltage Temperature Drift in Ion-Implanted MOS Transistors", *IEEE Journal of Solid-State Circuits*, vol. SC-17, pp. 291-298, Apr. 1982.

[3] H.-J. Song and C.-K. Kim, "A Temperature-Stabilized SOI Voltage Reference Based on Threshold Voltage Difference Between Enhancement and Depletion NMOSFET's," *IEEE Journal of Solid-State Circuits*, vol. 28, pp. 671-677, June 1993.

[4] *0.6-μm CMOS CUP Process Parameter*, Document #: 9933011, Revision B, Austria Mikro Systeme International AG, Austria.

[5] R. L. Geiger, P. E. Allen and N. R. Strader, *VLSI Design Techniques for Analog and Digital Circuits*, 1st edition, Singapore: McGraw-Hill, 1990.