Investigation of Different Width Size of Transistor on Internal Resistance and Output Power in CMOS Rectifier Using Two PMOS and NMOS

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***Abstract*— This paper presents the simulation studies on different width size of PMOS and NMOS on internal resistance and output power in CMOS rectifier. This investigation focuses on the internal resistance of the MOSFET and output power in the rectifier. The proposed CMOS rectifier considered the PMOS carrier mobility by increasing the width size of transistors rapidly. This simulation is done using CADENCE simulation software. The best configuration of CMOS rectifier is selected based on the total internal resistance and output power of the CMOS rectifier.**

Keywords—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

The needs of DC supply voltage are increasing exponentially by time. The DC supply plays as an important role in energy scavenging system, radio frequency identification (RFID), and antenna[1]–[6]. The input voltage from the environment is accumulated and converted using rectifier block. The conventional rectifier has a disadvantage of high voltage drop in the converter since it has high internal resistance. Then, researchers find a way to replace the converter using Schottky-diode and CMOS technology which have lower voltage drop in the converter compared to the previous design[7], [8]. However, Schottky-diode did not compatible with the CMOS technologies therefore did not suited CMOS implementations [9]. So, all the researchers work on the CMOS rectifier for the applications that have low input voltage[9], [10]. In the converter design, it consist PMOS and NMOS transistors. The transistors have different carrier mobility. The mobility of carriers in the channel is one of the fundamental parameters of MOSFET operation. The carrier mobility determines the current drive, the transconductance, and the speed of the transistor[11]. Many researchers do hard works to improve the mobility problem in PMOS[11]–[15]. However, for the CMOS rectifier circuit, the design have similar width size of transistors for PMOS and NMOS. There are no consideration of carrier mobility in PMOS in the CMOS rectifier. This paper presented the variation of design using similar topologies (two PMOS and NMOS).

II. TYPICAL CMOS RECTIFIER

Typical CMOS rectifier is based on the conventional rectifier shown in Figure 1. CMOS consist of PMOS and NMOS can create the virtual diode based on their structured. In CMOS rectifier, as shown in Figure 3 the circuit consist of two PMOS (M1 and M3) and two NMOS (M2 and M4). In previous work, the CMOS rectifier is designed with the similar width size of transistors for PMOS and NMOS which is at 750µm [12-14]. For each positive and negative cycle two transistor will turn on (PMOS and NMOS) that is shows in Figure 4 and 5. For positive cycle, M1 and M4 is turn on while M2 and M3 will turn on in negative cycle. The main issue highlighted in this paper is the size of PMOS and NMOS which should not be in the same size regarding to the different carrier mobility for both type of MOSFET[13], [15].

The design configuration of CMOS rectifier will be discussed and presented in the next section.

III. PROPOSED CMOS RECTIFIER

The drive current capability for PMOS and NMOS is different. The electron in NMOS is lighter thus make the higher mobility compared to PMOS[13]. In previous design, CMOS rectifier is design with the same width size of transistors for PMOS and NMOS[1], [5], [16]–[18]. The proposed CMOS rectifier consists of PMOS and NMOS. In this paper, the mobility of PMOS is tolerated in CMOS rectifier. The pattern of resistance and output power are taken by varying the width size of transistors. The width size of PMOS is increased to have lower internal resistance in the transistor and to overcome the low mobility in PMOS. It will increase the performance of CMOS rectifier that is presented in the result. Section IV will explain the configuration design of CMOS rectifier in details.

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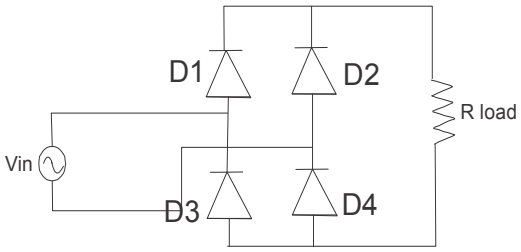

Fig. 1. Conventional AC/DC converter

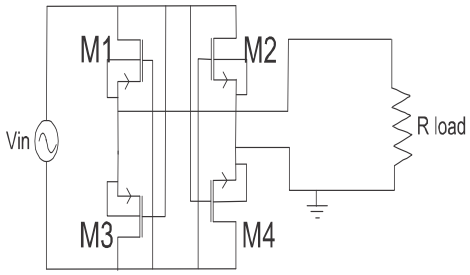

Fig. 2. Circuit of CMOS Rectifier

IV. Computer Simulation Model

In this section, there are two types of analysis which are the analysis on the internal resistance and the analysis to observe the output power of the CMOS rectifier. The simulation is done using CADENCE simulation software. The input voltage is set to $1V_p$ and load is set to $2k\Omega$.

A. Analysis of different design configuration of transistors on internal resistance in CMOS rectifier.

In this analysis, CMOS rectifier is designed in two different analyses. The focused on this design is to determine the internal resistance of the converter which is the resistance in PMOS and NMOS. The first analysis set the width size for all transistors to be similar. The designs are varied from small, medium and large width sizes. It is represented by design 1, 2, and 3. For second analysis, the width size of PMOS transistor is varied to improve the drive current in the circuit. The PMOS width size is enlarged to 1100µm and 1500µm (design 4 and 5) while the NMOS size is set at 750µm.

B. Analysis on the width size of transistors to the output power in CMOS rectifier

This analysis focused on the output power occurred from the converter. Two different design configurations are analyzed. For the first design configuration, the width size of PMOS and NMOS is set to be similar. The width size of the transistors is varied from 10µm to 1200µm. In the second design configurations, the width size of PMOS is varied from 800µm to 1500µm while the width size of NMOS is set at 750 µm. The second analysis is done to observe the variations of output power when the drive current is improved. These two analyses are done to get the profile of output power by the CMOS rectifier.

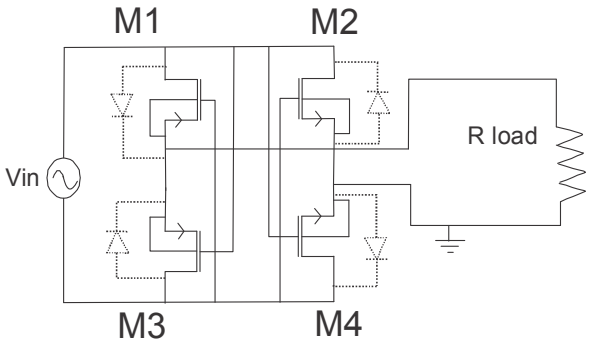

Fig. 3. Circuit of CMOS Rectifier with virtual diode

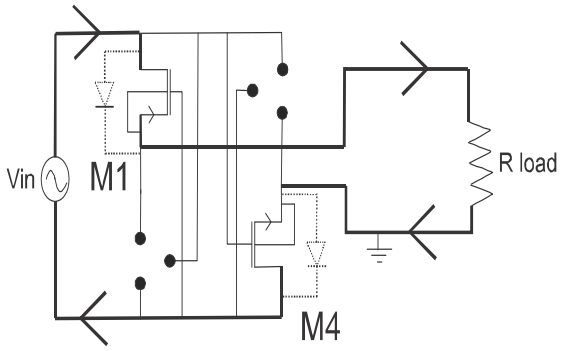

Fig. 4. Simplified circuit for positive cycle in CMOS Rectifier

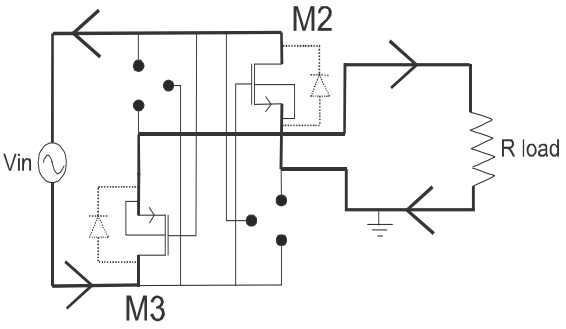

Fig. 5. Simplified circuit for negative cycle in CMOS Rectifier

V. RESULT AND DISCUSSION

For every cycle (positive and negative cycle) of the input voltage, the PMOS and NMOS will represented as a diode which have the internal resistance. The simplified circuit for the PMOS and NMOS transistor is shown in Figure 6. In analysis A, the result for five design is shown in Table I. Design 1 to 3 shows the design for the similar width size of the transistors. Design 4 and 5 shows the PMOS width size that is enlarged. For the analysis of similar width size of transistors, design 3 have the total resistance at 7.60 Ω and for the study of enlarging the PMOS width size, design 5 have the total resistance at 4.60 Ω compared to 5.80 Ω for design 4. It prove that the width size is one of the factor that effect the internal resistance in the transistors. The larger the width size of the transistor make the bigger current to go through to the transistor thus have the small value of the resistance. In design 4 and 5, the PMOS width size is set to be larger than NMOS width size to consider the low mobility of the PMOS. The PMOS width size from design 5 is designed twice from the NMOS width size. The design overcome the problem of lesser mobility in PMOS hence improves drive capability of PMOS. Figure 7 shows the graph plotted for the total resistance in analysis A.

In Analysis B, the performance of the CMOS rectifier is determined by finding the output power of the circuit. The analysis is done for the similar width size of the transistor which is shown in Table II and illustrated in Figure 8. The other analysis is the analysis which have the width size of PMOS larger than NMOS. This design configuration considered the low mobility of holes occurred in PMOS transistor compare to the electron occurs in NMOS. The result is shown in Table III and Figure 9. The output power is constant for designs 1000µ/750µ to 1500µ/750µ at 4.898x10-4 W. This is because it already achieved the current stability through the transistors in CMOS rectifier.

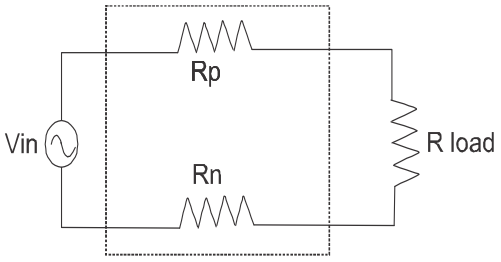

Fig. 6. Internal resistance for positive and negative cycle in CMOS rectifier

TABLE I. THE INTERNAL RESISTANCE FOR ANALYSIS A

Design	Design of CMOS rectifier (PMOS/NMOS)	Total Resistance(Ω)
1	4µ/4µ	1570.00
2	50µ/50µ	107.00
3	750µ/750µ	7.60
4	1100µ/750µ	5.80
5	1500µ/750µ	4.60

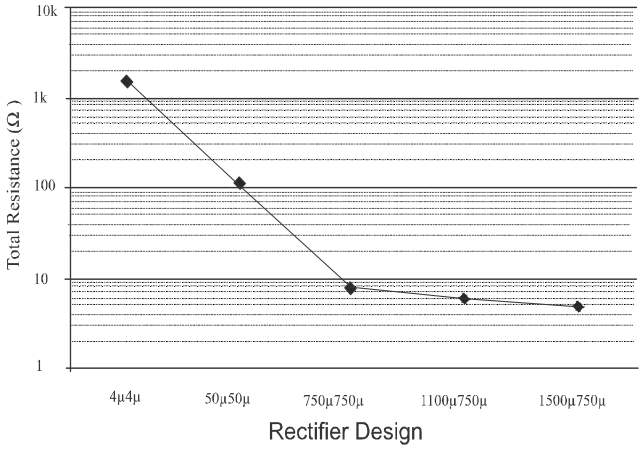

Fig. 7. Internal resistance for positive and negative cycle in CMOS rectifier

TABLE II. THE OUTPUT POWER FOR ANALYSIS B (FOR SIMILAR WIDTH SIZE OF TRANSISTORS)

Rectifier design	Power ($x10^{-4}$ W)	Rectifier design	Power ($x10^{-4}$ W)
10µ/10µ	2.98	300µ/300µ	4.85
20µ/20µ	3.82	400µ/400µ	4.89
30µ/30µ	4.15	500µ/500µ	4.94
40µ/40µ	4.32	600µ/600µ	4.95
50µ/50µ	4.44	700µ/700µ	4.92
60µ/60µ	4.52	750µ/750µ	4.92
70µ/70µ	4.54	800µ/800µ	4.91
80µ/80µ	4.61	900µ/900µ	4.91
90µ/90µ	4.69	1000µ/1000µ	4.91
100µ/100µ	4.68	1100µ/1100µ	4.91
200µ/200µ	4.80	1200µ/1200µ	4.92

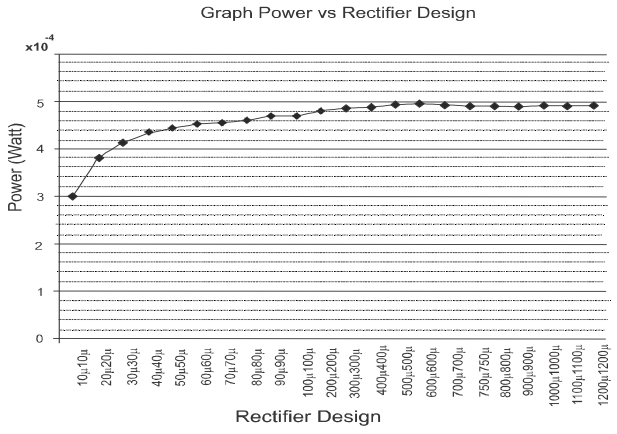

Fig. 8. Internal resistance for each cycle in CMOS rectifier

TABLE III. THE OUTPUT POWER FOR ANALYSIS B (WIDTH SIZE OF PMOS IS LARGER AND NMOS AT 750 μM)

Rectifier design	Power ($x10^{-4}$ W)
800μ/750μ	4.886
900μ/750μ	4.896
1000μ/750μ	4.898
1100μ/750μ	4.898
1300μ/750μ	4.898
1500μ/750μ	4.898

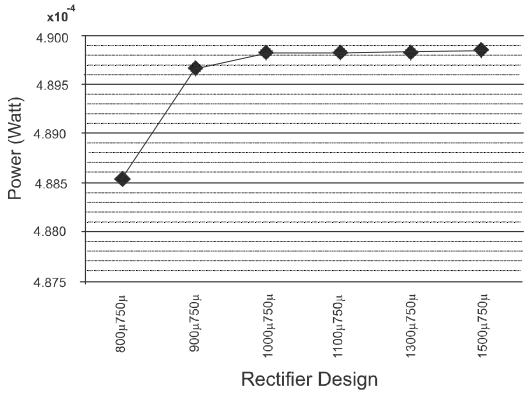

Fig. 9. Output power for analysis B for width size of PMOS larger than NMOS in CMOS Rectifier

VI. CONCLUSION

The analyses are to determine the low internal resistance and the performance of the CMOS rectifier. Based on the analyses from analysis A and B the design that has lowest total resistance is design 5 that is 4.60 Ω. The design configuration for design 5 is 1500μm of PMOS and 750μm of NMOS. For the output power in CMOS rectifier, four designs are discussed in analysis B, have the same output power performance (1000μ/750μ, 1100μ/750μ, 1300μ750μ and 1500μ/750μ) which is 4.898 x10-4 W. Design 5 is chose as the best circuit design since it has low internal resistance and optimum output performance of CMOS rectifier. This design mitigate the low PMOS mobility problem which is need to be larger than NMOS size.

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REFERENCES

[1] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation techniques," in 2009 IEEE 8th International Conference on ASIC, 2009, pp. 549–552.

[2] M. Ebrahimian, K. El-Sankary, and E. El-Masry, "Enhanced RF to DC CMOS rectifier with capacitor-bootstrapped transistor." pp. 1655–1658, 2010.

[3] D. Karolak, T. Taris, Y. Deval, J.-B. Begueret, and A. Mariano, "Design comparison of low-power rectifiers dedicated to RF energy harvesting," in 2012 19th IEEE International Conference on Electronics, Circuits, and Systems (ICECS 2012), 2012, pp. 524–527.

[4] A. Virattiya, B. Knobnob, and M. Kumngern, "CMOS precision full-wave and half-wave rectifier," in 2011 IEEE International Conference on Computer Science and Automation Engineering, 2011, vol. 4, pp. 556–559.

[5] Yuan Rao and D. P. Arnold, "An Input-Powered Vibrational Energy Harvesting Interface Circuit With Zero Standby Power," vol. 26, no. 12. pp. 3524–3533, 2011.

[6] G.-C. Lin, M.-W. Lee, and Y.-C. Hsu, "An AC-DC rectifier for RF energy harvesting system," in 2012 Asia Pacific Microwave Conference Proceedings, 2012, pp. 1052–1054.

[7] Q. Ma, M. R. Haider, and Y. Massoud, "Low-loss rectifier for RF powering of implantable biosensing devices," in WAMICON 2012 IEEE Wireless & Microwave Technology Conference, 2012, pp. 1–4.

[8] Xi-Ning Wang, Li-wu Yang, Ting-Huang Lee, Jian-Kun Su, Bin Zhu, and Xiao-Fang Yao, "RF modeling of integrated RF CMOS Schottky diodes for rectifier designs," in 2008 9th International Conference on Solid-State and Integrated-Circuit Technology, 2008, pp. 305–308.

[9] A. S. Bakhtiar, M. S. Jalali, and S. Mirabbasi, "A high-efficiency CMOS rectifier for low-power RFID tags," in 2010 IEEE International Conference on RFID (IEEE RFID 2010), 2010, pp. 83–88.

[10] M. Zargham and P. G. Gulak, "High-efficiency CMOS rectifier for fully integrated mW wireless power transfer," in 2012 IEEE International Symposium on Circuits and Systems, 2012, pp. 2869–2872.

[11] B. Watson, "Enhancement of PMOS device performance with poly-SiGe gate," IEEE Electron Device Lett., vol. 20, no. 5, pp. 232–234, May 1999.

[12] S. a. Campbell and P. Andersen, "CMOS mobility degradation coefficients at low temperatures," IEE Proc. I Solid State Electron Devices, vol. 135, no. 1, p. 17, 1988.

[13] a. S. Zoolfakar and a. Ahmad, "Holes mobility enhancement using strained silicon, SiGe technology," 2009 5th Int. Colloq. Signal Process. Its Appl., vol. 2, pp. 346–349, Mar. 2009.

[14] E. X. Wang, P. Matagne, L. Shifren, B. Obradovic, R. Kotlyar, S. Cea, M. Stettler, and M. D. Giles, "Physics of Hole Transport in Strained Silicon MOSFET Inversion Layers," IEEE Trans. Electron Devices, vol. 53, no. 8, pp. 1840–1851, Aug. 2006.

[15] F. Lime, "Investigation of electron and hole mobilities in," no. Fig 2, pp. 247–250.

[16] Yuan Rao and D. P. Arnold, "An input-powered active AC/DC converter with zero standby power for energy harvesting applications." pp. 4441–4446, 2010.

[17] K. Kotani, T. Bando, and Y. Sasaki, "Photovoltaic-assisted CMOS rectifier circuit for synergistic energy harvesting from ambient radio wave," in 2012 IEEE Asian Solid State Circuits Conference (A-SSCC), 2012, pp. 329–332.

[18] K. Kotani and T. Ito, "High efficiency CMOS rectifier circuits for UHF RFIDs using Vth cancellation techniques," in 2009 IEEE 8th International Conference on ASIC, 2009, pp. 549–552.