An Energy-Efficient Implantable Transponder for Biomedical Piezo-Resistance Pressure Sensors

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***Abstract*— An implantable transponder with wireless link for biomedical applications is presented. The application specific integrated circuit (ASIC) is energy optimized for a Wheatstone configured piezoresistive pressure sensor. The system takes advantage of an extremely low duty cycle reducing significantly the energy consumption. A net differential input swing voltage is obtained from only a single resistive sensor branch by interchanging the sensor supply polarity alternately. The ASIC was fabricated in TSMC 90 nm CMOS process with an area of 0.37 mm^2. The transponder is powered by a 13.56 MHz radio frequency signal and performs sensor signal amplification, analog to digital conversion and uplink data transmission through load shift keying within 96 μs every 5 min. This results in a total energy consumption for the complete system on the implant side of 12.5 nJ per sample for a resolution of 7.03 effective bits.**

***Index Terms*— Glucose sensor, piezoresistive pressure sensor, readout circuit, transponder chip, LSK, wireless, telemetry.**

I. Introduction

PRESSURE sensors have been commonly used in biomedical applications (clinical care) to monitor patient's pathologies such as intra-cranial pressure in neurosurgery, glaucoma intraocular pressure, blood glucose concentration and air pressure in respiratory diseases [1]. With the advance of down-scale CMOS technology, the size of complete smart sensor systems, including both the sensor and the conditioning circuitry, has been reduced significantly. This trend opens the possibility to implant the sensor system in human body for long term health care monitoring [2], [3]. A miniature biosensor implant such as, for example a transponder under the skin could improve life quality and potentially the life expectancy of millions of patients worldwide.

A conceptual illustration of a biosensor micro-implant transponder is shown in Fig. 1. It includes an RF coil antenna for power and data transmission, a biosensor and an ASIC implementing the sensor interface, including analog to digital conversion and data transmission circuitry.

Literature shows that resistance-to-frequency converters are dominant in piezoresistive pressure sensor interfaces because of circuit simplicity and high linearity [5]–[9]. Even though these systems require only relatively simple, and power conservative, current-to-frequency converters, they still need to be powered on for multiple pulse cycles in order to obtain an average frequency signal with sufficient precision. In addition, if the external reader uses a counter to translate the received data form into a binary number, transmitting the pulses may affect the accuracy due to jitter induced to the pulse timing by ambient and quantization noise. Moreover, the frequency output is not a digital output, not allowing a secure communication, and it is why a readout circuit with fully digital output is required and presented in [1] and [10]–[12]. Integrating resistance-to-frequency converters in sensor interfaces, allows these systems to achieve high resolution and high linearity with the tradeoff of consuming large power thus, not suitable for implant applications. Another factor contributing for an increase in power consumption is the fact that piezoresistive sensors are also the most "power hungry" components in complete sensor systems. Hence, it is (worth) taking into account the sensors' power consumption in wireless implant sensor systems.

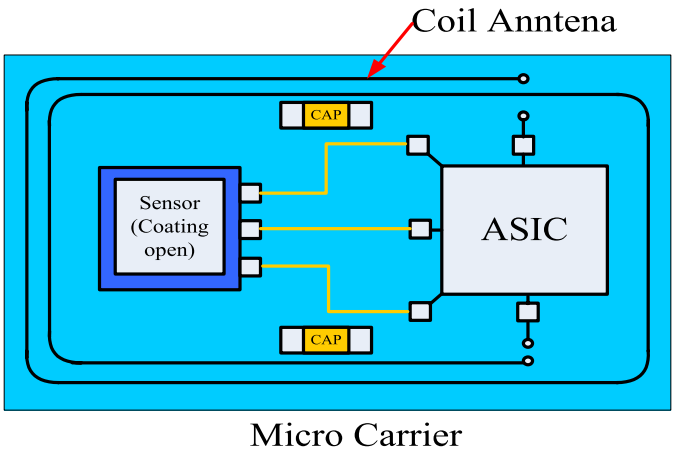

Fig. 1. Conceptual view of the sensor implant modified from [4].

For some biomedical applications, the main biological signals that need to be monitored in patients such as glucose concentration, intraocular pressure etc., change slowly and it is more interesting to retrieve information about a signal trend than an accurate absolute value. This allows the health care monitoring systems for such applications to avoid monitoring the signal sampling continuously. In fact, these systems only need to sample the signal once every ten minutes [3], [13], [14]. The requirement of low sampling rates allows these systems to save energy consumption substantially by

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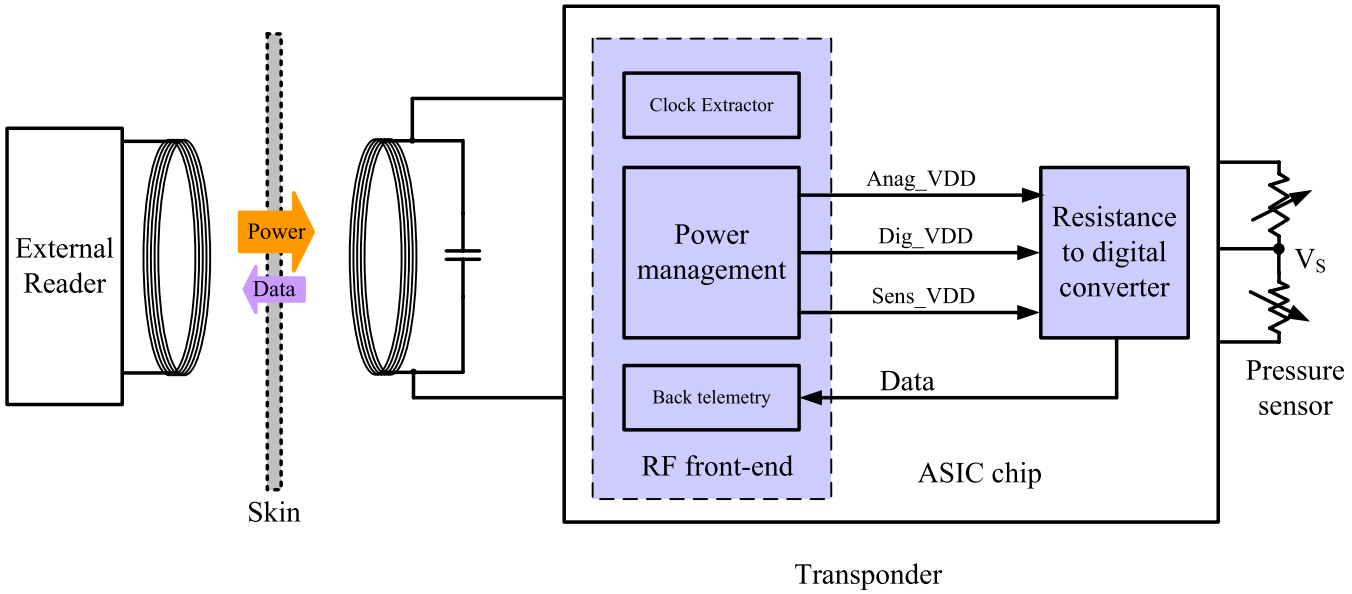

Fig. 2. System block diagram of the sensor.

going into a sleep mode between samples. This translates in a low duty cycle scheme that can help to prolong the life time of the battery on the reader side.

This paper is an extension of the conference paper [15] and provides further results of the full system on the implant side including characterized measurement results with a piezoresistive pressure sensor. There are two distinct characteristic features of the implant system: in the first instance, it is used only a single resistive branch of the sensor's Wheatstone bridge, reducing the current into the sensor by half. The same input voltage swing to the readout circuitry is maintained, as if it was established a differential connection (using both resistive branches on the Wheatstone bridge), by alternately changing the polarity of the sensor's power supply. This method not only reduces the complexity of the sensor's connection but also suppresses 1/f noise since this approach constitutes a correlated double sampling (CDB) of the same sensor node [16]. Secondly, we employ a full analog-to-digital converter (ADC) on chip to achieve fast data conversion and transmission thus, short periods of wireless power transmission and, consequently, much less energy per sample when comparing with a resistance-to-frequency approach. The content of this paper is divided according to: section II that has a detailed description of the sensor and the design constraints of the proposed system such as power management and readout circuitry. Section III contains the measurement results, and Section IV, the conclusion and a comparison in performance with other published work.

II. System Implementation

A generic representation of the system's block diagram is shown in Fig. 2. The power from the external reader and the data from the integrated transponder are transferred through a pair of inductively coupled coils with a 13.56 MHz RF carrier. The induced RF signal at the secondary coil is converted to an unregulated DC signal by a two-stage cross-coupled rectifier. Three voltage regulators produce three clean power signals for

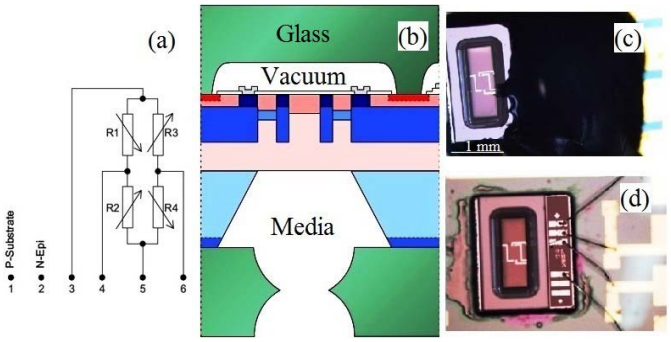

Fig. 3. (a) Electrical circuit diagram for the SW415-2 pressure sensor. (b) Schematic view of a SW4 pressure sensor cross-section. (c) Glob top epoxy covering/insulating the gold wires. (d) Wire bonding between the pressure sensor and the cooper on the PCB.

powering the circuitry in the transponder. The readout circuit senses, amplifies and converts a small signal from the sensor into a serial digital code. This information is transmitted to the external reader by LSK. A clock extractor provides a low frequency clock from the input RF signal for controlling the operation of the readout circuitry.

A. Sensor Assembling

The SW415-2 piezoresistive absolute pressure sensor [17], fabricated by Sensonor AS, consists of a Wheatstone bridge resistor with 4 variable resistors, Fig. 3, with a bridge resistance of 12 KΩ and a sensitivity of 64 mV/bar, at 5 V supply, with a maximum pressure of 2 bar. The sensor is highly compatible with different media sources since the media accesses from the backside and the piezoresistors do not come in direct contact with the environment.

A printed circuit board (PCB) with outputs connecting to sensor pins 3, 4 and 6 was fabricated. A 1×1 mm hole was made on the PCB and the pressure sensor was attached to the PCB with a two component epoxy (Araldite 2020, Huntsman, UK) and cured for 24 hours at Room Temperature (RT). Araldite 2020 has a low viscosity avoiding the epoxy to spread

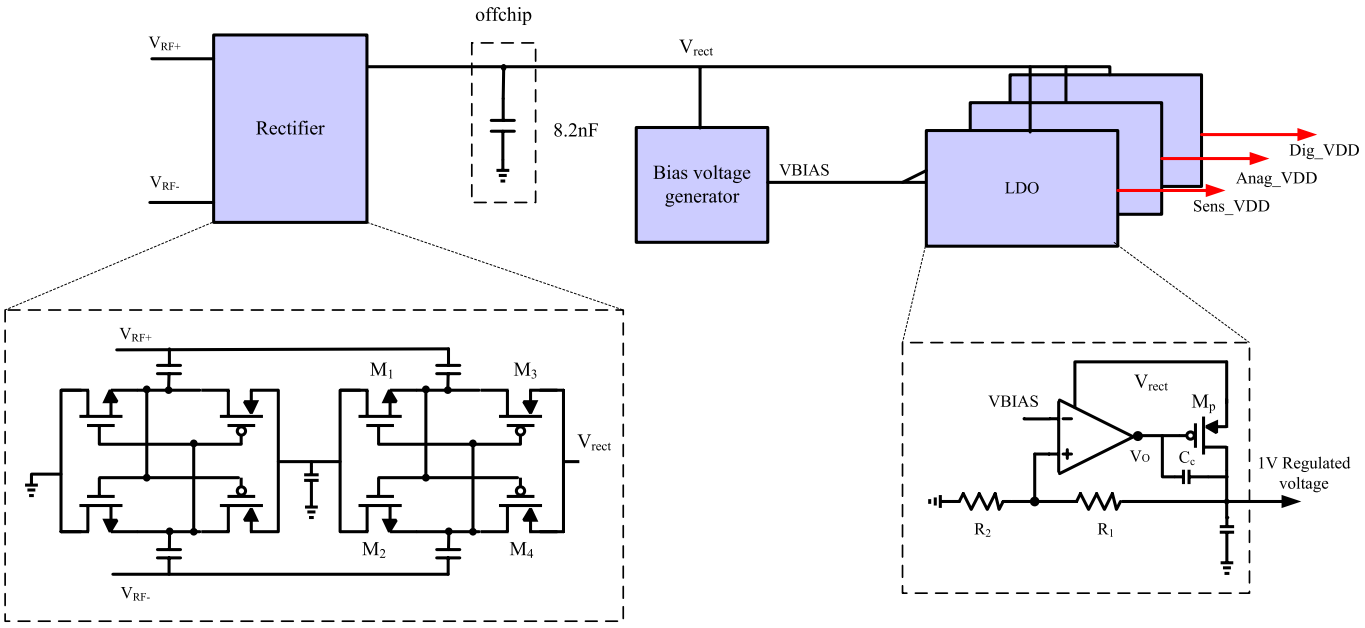

Fig. 4. Power management architecture.

towards the hole and covering the media access (air) to the sensor's diaphragm. An Acetal copolymer inlet was glued to the back of the PCB (with Araldite 2020) with the pressure sensor's media access point in the center, for connecting a tube with origin on a pneumatic/hydraulic hand-pump (DPI 104, GE Druck, UK) equipped with a digital pressure indicator in order to apply a known calibrated pressure. The wire bonding between the pressure sensor and the PCB was made by using a semi-auto wire bonder (Delvotic 5610, F&K, Austria). A gold wire of $\phi 25$ μm diameter was used to make a ball bond on the end of each connection. On the PCB bonds a silver conductive epoxy was used to ensure a good conductivity/bonding and a glob top epoxy (T7139T7139, EPO-TEK, USA) was deposited on the wires, and cured for 4 hours at 80 °C, in order to protect the wires and avoid short-circuits when handling the sensor.

B. RF Front-End

1) Power Management: The structure of the power management is shown in Fig. 4. A two-stage differential cross-coupled rectifier is used for converting the induced RF signal into a DC signal [18], [19]. This structure achieves high efficiency in UHF RFIDs applications, but we also have found that it works efficiently at a frequency of 13.56 MHz. In this structure, the full differential RF voltage swing is utilized to dynamically bias the gates of the transistors in order to achieve a high power conversion efficiency. In the forward phase, the gate-source voltage (V_{gs}) of, for example, transistor M_3 reaches approximately the positive peak-to-peak amplitude of the RF signal, reducing substantially the drop-on voltage (to approximately drain to source voltage V_{ds} of a transistor in triode condition). In the reverse phase, V_{gs} is pulled back to a negative value, significantly reducing the reverse leakage current. The high frequency component at the output voltage is then filtered out by an off-chip capacitor. The selection of this capacitor value is a constrain between a desired short powering-up time and sufficient energy stored on the capacitor before on-chip peripherals start drawing current. The measured results show that the rectifier achieves 40% power conversion efficiency (PCE) and 1.25 V output DC voltage with a load resistor of 8.2 KΩ at a 0.8V peak-to-peak RF input signal.

The DC output voltage from the rectifier varies with the strength of the induced RF signal and the loading current of the readout circuitry. Therefore, three low-dropout regulators (LDO) are designed to provide three separate, stable 1 V power supply signals for the sensor, the analog and the digital circuits. This separation suppresses the noise coupling effect from switching noise of the digital to the other sensitive circuitry. Because these voltage regulators should tolerate high DC voltages from the rectifier, thick gate-oxide transistors with a nominal supply voltage of 2.5 V are used instead of standard transistors. Since the transponder is intended to be implanted into human body, the working temperature of the chip is held constant thus, avoiding the use of a bandgap reference circuit [20]. Instead, a reference voltage generator based on [21] is designed to provide a 0.7 V bias voltage, V_{BIAS}, working at body temperature (37°C) (Fig. 4). Since the peak current drawn from the sensor is about 150 μA, the size of the PMOS transistor M_P in the sensor voltage regulator must be sufficiently large to provide enough current at low drop-on drain-to-source voltage. The size of the M_P is 40 μm/0.28 μm for the sensor voltage regulator and 10 μm/0.28 μm for the two other voltage regulators. The feedback voltage, which is $\frac{3}{4}$ of the output voltage, is generated by a resistive voltage divider. The values of R_1 and R_2 are 250 KΩ, and 750 KΩ, respectively.

2) Back Telemetry: For a modest data rate requirement, LSK is often preferred for back telemetry. In this technique, the reflected impedance on the primary coil at the external reader is modulated with the serial data stream in the transponder side [22]. The modulated information is then sensed by a resistor on the primary coil. In addition, the same coil is shared for both power, and data, link for low complexity. For these

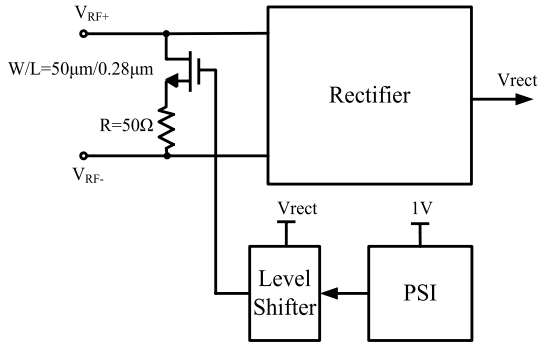

Fig. 5. Back telemetry.

reasons, LSK is also used here. The schematic of our LSK circuit is shown is Fig. 5. An NMOS transistor and a resistor in series are connected between two terminals of the coil. The serial data chain switches the NMOS transistor on and off, changing the load impedance on the secondary coil and, in turn, the reflected impedance on the primary coil [23]. This results in a change in the voltage on the primary coil and the transmitted data can be recovered by a simple envelope detector at the external reader. The serial resistor determines the load impedance modulation strength on the secondary coil. An off-chip resistor of 50 Ω is chosen to create 50% modulation strength and offer flexible testing.

3) Clock Extractor: The induced 13.56 MHz RF signal from the secondary coil is strengthened and divided into a 26.6 KHz clock signal for the readout circuitry and a 423.7 KHz clock signal for the parallel to serial interface (PSI) by the clock extractor. A 26.6 KHz clock signal extracted by a 512 ratio programmable frequency divider from the the RF signal determines the period of 18.8 μs for each operating phase of the readout circuit.

C. Resistance to Digital Converter

The sensor's resistance variation is sensed, and amplified, by a switched-capacitor (SC) amplifier in which correlated double sampling (CDS) is utilized to eliminate circuit's offset. The output voltage from the SC amplifier is then converted into a digital output code by a following single-slope ADC. The conversion process is divided into three phases: resetting, amplifying and converting. A branch of the Wheatstone bridge sensor is connected to the RDC as shown in Fig. 6. The resistive sensor branch is modeled by two differential sensing resistors $\mathrm{R}+\Delta\mathrm{R}$, and $\mathrm{R}-\Delta\mathrm{R}$, where ΔR corresponds to the resistance change which is proportional to the pressure change.

In the resetting phase ($\phi_1 = 0$), the sensor is powered up by connecting two switches S_0 and S_0' to power supply (VDD), and ground (GND), respectively. The input voltage of the SC amplifier in the first phase is determined as $V_S[1] = V_{DD}\frac{\Delta R}{R}$. At the same time, S_3 connects the input, and output, of the subthreshold inverter together settling on its switching threshold V_{off} which may differ slightly from zero reference V_{CM}. This voltage offset is stored on capacitor C_2. Since the inverter's transistors have a high threshold voltage (0.7 V for NMOS and 0.8 V for PMOS), both NMOS, and PMOS, are biased in the subthreshold region providing a high DC gain and consuming a small DC current. There is a trade-off between the power consumption and the response time of the subthreshold inverter. Since the power-on time of the system is critical, a relatively fast response is obtained by a relatively large aspect ratio of 25 μm/0.5 μm and 45 μm/0.5 μm for NMOS, and PMOS, devices respectively, drawing a current of 1.3 μA. The total charge stored on node V_G in this phase is calculated as

$$Q_1 = (V_{off} - V_S[1])C_1 + V_{off}C_2 \tag{1}$$

In the amplifying phase, the feedback loop S_3 is opened and the right hand side of C_2 is switched from V_{CM} to the output node, autozeroing the amplifier [24]. The two switches S_0, and S_0', are flipped to connect to VDD, and GND, respectively. The input voltage in this phase is $V_S[2] = -V_{DD}\frac{\Delta R}{R}$. The switch S_3 is opened to disconnect V_G and V_{out} while the switch S_2 is closed to connect the right hand side plate of C_2 to the output of the inverter. The total charge stored on node V_G in this phase is

$$Q_2 = (V_{off} - V_S[2])C_1 + (V_{off} - V_{out})C_2 \tag{2}$$

where V_{out} is the output voltage of the inverter at the end of the amplifying phase (it is assumed that the open loop gain is high enough for the feedback loop to maintain the voltage V_{off} on node V_G). Switch S_4 is closed connecting V_{out} to node V_H. By charge conservation in the now floating node V_G, Q_1 must be the same as Q_2 resulting in the following output voltage at the end of the amplifying phase:

$$V_{out} = V_{DD}\frac{\Delta R}{R}\frac{C_1}{C_2}\left(1 - \frac{C_1 + C_2}{C_2 A_v}\right) \tag{3}$$

Equation (3) shows the calculated output voltage equivalent to the output voltage of a SC amplifier with the differential input of a Wheatstone bridge. The limited open loop gain A_v of the inverter causes a gain error $(1/1 + (C_1 + C_2/C_2A_v))$. This gain error is a deterministic error and can be improved in post signal processing. Besides, the sensor itself will also require calibration on the reader side, so this gain error is not a major drawback and will be compensated for by system calibration. Due to CDS, the offset voltage and low frequency noise components at the input of the inverter are eliminated.

In the conversion phase, both the sensor and SC amplifier are powered down to save power [not explicitly shown in Fig. 6(a)]. Switch S_5 is closed and C_h is discharged by a constant current I_{disch} down to the threshold voltage of the comparator. The zero reference V_{CM} can be tuned to match with this threshold voltage. During this discharge time, the counter counts the number of clock cycles from an on-chip oscillator. The binary output code from the counter is, thus, proportional to the variation of the sensor's resistance:

$$\begin{aligned} D_{out} &= \frac{V_{out}C_h f_{OSC}}{I_{dis}} \\ &= V_{DD}\frac{\Delta R}{R}\frac{C_1}{C_2}C_h f_{OSC} I_{dis}\left(1 - \frac{C_1 + C_2}{C_2 A_v}\right) \end{aligned} \tag{4}$$

where f_{OSC} is the frequency of the oscillator. Equation (4) shows that the digital output code is linearly proportional to the resistance change of the sensor. As a chosen trade-off between power consumption, noise, and digital output code

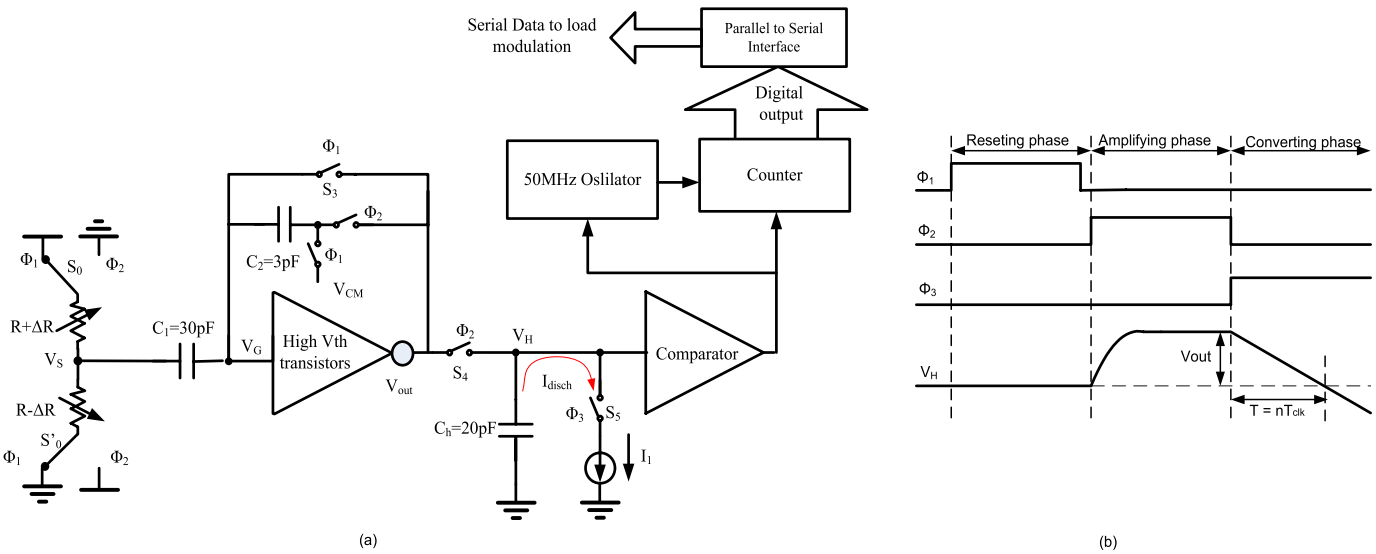

Fig. 6. (a) Resistance to digital converter. (b) Timing diagram [15].

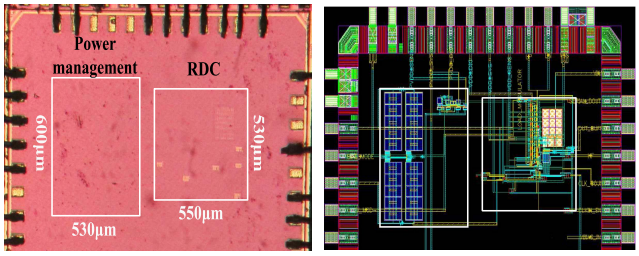

Fig. 7. Chip photograph.

range, I_{disch} and f_{OSC} are designed at 500 nA and 50 MHz respectively. Each of the three phases takes 18.8 μs including some safety margin for values to settle.

III. Measurement Results

The ASIC chip has been designed and fabricated in a 90 nm CMOS technology. The chip photograph is shown in Fig. 7. The details of the circuits are masked by dummy filling in the fabricating process and only MIM capacitors on the top metal layer are visible. Therefore a layout figure is provided on the right. The die area for the readout circuitry, and the power management circuitry, are 0.12 mm^2, and 0.25 mm^2, respectively without area optimization.

To characterize the function of the transponder chip output to the pressure sensor, the sensor PCB was connected to the chip test board. The applied pressure from the PV411A pneumatic/hydraulic hand-pump is recorded by a digital pressure indicator (DPI 104, GE Druck, UK). The digital output code from the chip is recorded and saved to the internal memory of an oscilloscope (DSO 6034, Agilent Technologies, USA) for offline data processing. Fig. 8 shows the relation between the sensor's pressure and the output code from the on-chip ADC. The output code ranged from 120 to 332 when the pressure was changed from 0 to 2 bar with a 0.1 bar increment. The offset code derives mainly from the offset voltage of the comparator in the RDC which can be eliminated by post-signal processing on the reader side. To calculate the resolution of

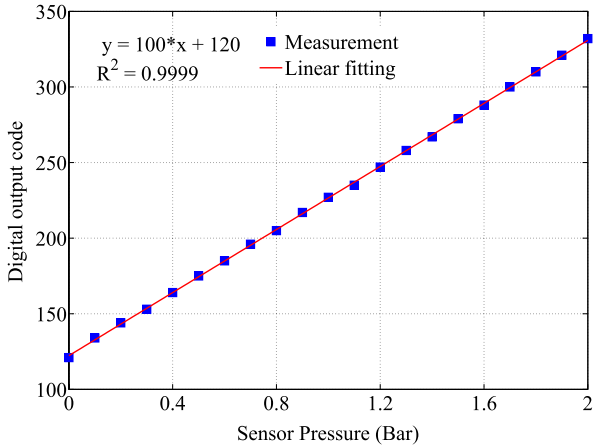

Fig. 8. Output code versus piezoresistor value.

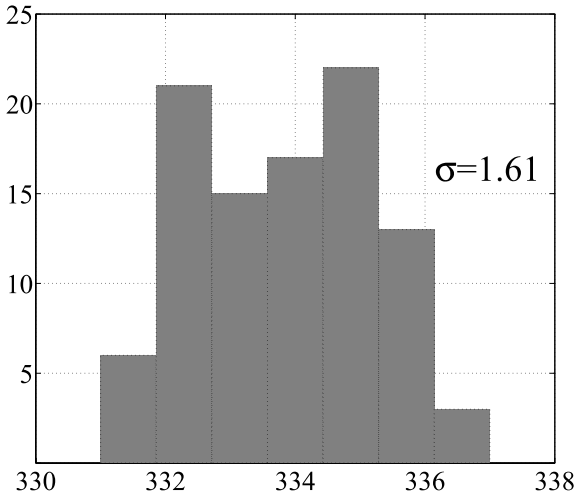

Fig. 9. Histogram of output code.

the readout circuitry, a batch of 100 samples at the saturated value output code (when the applied pressure is 2 bar) are recorded for processing. A histogram of the samples as shown in Fig. 9 provides a standard deviation of 1.61. This results in a resolution of 7.03 effective bits.

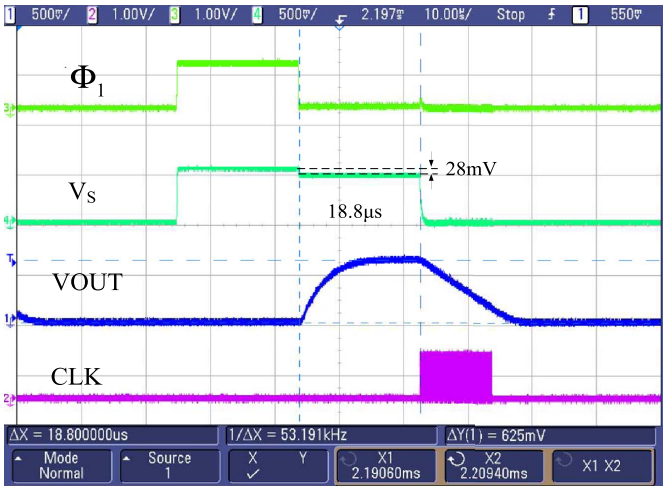

Fig. 10. Measurement result of the readout circuit.

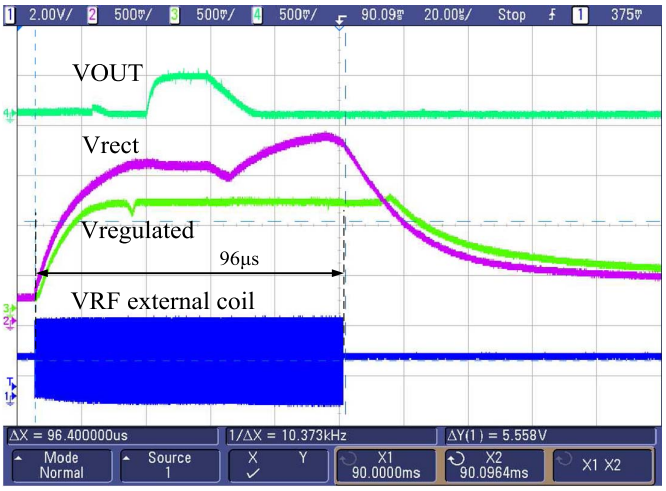

Fig. 11. Start-up behavior of the system.

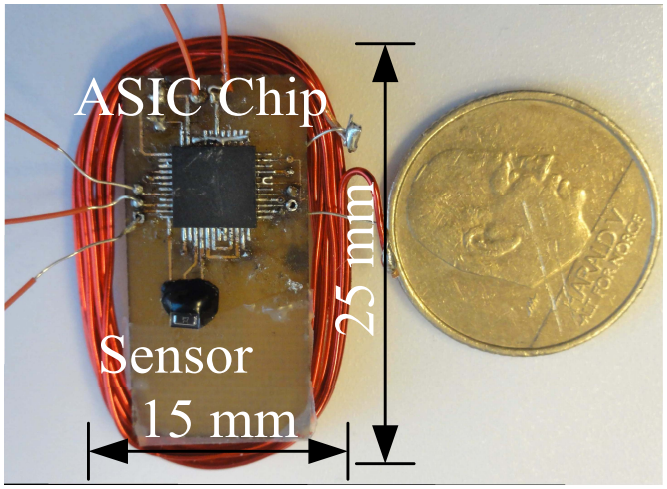

Fig. 12. Macro prototype of the pressure sensor implantable transponder.

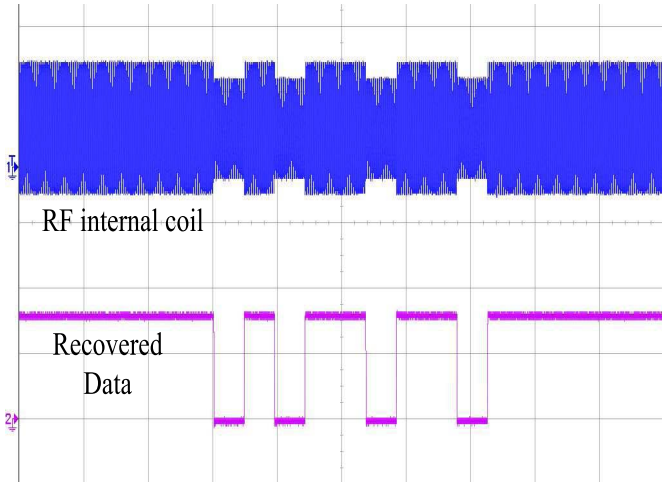

Fig. 13. Uplink data transmission measurement at 1 cm distance.

Fig. 10 shows the waveforms of interesting nodes of the RDC at the saturated condition of the ADC from the oscilloscope. The input voltage swing is approximately 28 mV when the sensor is supplied by a 1 V "clean" voltage from the on-chip LDO regulator. The on-chip oscillator feeds a 46 MHz clock signal which is slightly different from the simulated value to the counter during the maximum discharging time of 7.3 μs.

The macro-prototype of the transponder is shown in Fig. 12. A basic inductive link with two spiral coils on the external reader and transponder has been implemented exclusively for functional testing of the back telemetry and power transfer. Optimizing such links for biomedical implants has already been covered extensively by previous work [26]–[28]. To investigate the start-up behavior of the system, the external reader powers a burst-mode 13.56 MHz sinusoidal signal to the transponder. The start-up response of the system is shown in Fig. 11. The rectifier needs 20 μs to charge a 8.2 nF off-chip capacitor up to 1.25 V DC voltage. The output voltage of the LDO regulator starts being regulated at 1V after 30 μs. Assuming that 30 μs is reserved for 10 bit data transmission after conversion, the total active time of the system is approximately 96 μs.

Fig. 13 shows the waveforms of the RF signal on the internal coil and the recovered data from the external reader at a data

TABLE I
PERFORMANCE SUMARY

Transponder	
Transponder size	15 mm × 25 mm
Sensor range	0-2 bar@ 6000 ± 76.7 Ω
Resolution	7.03 bit
Technology	90 nm CMOS
Regulated supply voltage	1 V
Averaged power consumption ASIC chip Sensor	52 μW@96μs active time 19.5 μW@96μs active time 83.3 μW@37.6μs active time
Energy per sample	12.5 nJ
Telemetry Link	
Carrier frequency	13.56 MHz
Modulation scheme	LSK
Data rate	42.37 K bit/s
External coil	1.3 μH
Transponder coil	12 μH

TABLE II
PERFORMANCE COMPARISON OF BIOMEDICAL IMPLANTABLE PRESSURE SENSOR SYSTEM

Publication	[16], [25]	[6]	[7]	[11]	[12]	This work
CMOS technology	90 nm	0.35 μm	N/A	0.7 μm	0.13 μm	90 nm
Output signal	frequency	frequency	frequency	digital	digital	digital
Resolution	7.8 bit	8.5 bit	N/A	20 bit	10.4 bit	7.03 bit
Power consumption	1.7 μW	15 mW	42.75 mW	1.35 mW	224.5 μW	52 μW
Measurement time	1 s	100 ms	36 ms	170 ms	50μs	96 μs
Energy per sample	1.7 μJ	1.5 mJ	1.54 mJ	229.5 μJ	11.2 nJ	5 nJ

rate of 42.37 KHz. A frequency divider with 32 dividing ratio generates a clock signal from the 13.56 MHz RF input signal for the PSI block. The serial modulated data is then read by the external reader whith the maximum reading distance of 1 cm through the air. The distance can be further extended by optimizing the inductor coils design and increasing the modulation depth of the signal on the internal coil.

The performance of the transponder is shown in Table I. With the averaged power consumption of 52 μW during one sample period of 96 μs, the total energy consumption per sample is 5 nJ. Taking into account the 40% PCE of the rectifier, the total energy consumption of the complete system, on the implant side, is 12.5 nJ per sample. The performance comparison of our transponder with recent work is shown in Table II. Since the implant system can perform full analog-to-digital conversion on-chip before data transmission, instead of sending frequency information as a series of pulses for a long period, the transponder requires a very short power-on period for each sample, and consumes much less energy per sample.

IV. CONCLUSION

It has been presented a macro-prototype of an implantable transponder which has been energy-optimized for the power consuming bridge resistive pressure sensor. The ASIC chip has been designed and fabricated in TSMC 90 nm CMOS technology and it has been characterized with a commercial piezoresistive pressure sensor. By reducing the power-on time of the sensor, and performing full analog-to-digital conversion for true digital code transmission, this transponder consumes only 12.5 nJ per sample. This method is significantly useful in biomedical applications where the patient's physical properties change slowly such as glucose concentration, intraocular pressure, etc. As an example, one can assume a single sample every 5 minutes and a complete cut-off of the power in between each sampling period, which is the case for glucose monitoring [3], the system will run on only 41.6 pW. If one includes a three order of magnitude margin for losses due to power-up overhead of the transmitter (reader side) and limited wireless power transfer efficiency, the power consumption will not figure in the power budget of a battery driven reader.

In practice, the physical size of the transponder can be further reduced by attaching the bare die and bonding its pads onto the PCB. The secondary coil can be miniaturized and implemented on the PCB for low complexity. The ultra low-energy characteristics of this transponder make it suitable for integration with power harvesting systems from ambient sources. One could again consider to expand the implant power budget by adding more functionalities and features, such as other sensor modalities, local storage and simple processing capability. This would allow not only to move some functions from the reader to the implant but also for the implant to operate in the absence of a reader. This would reduce the communication bandwidth even more, together with the power consumption of the reader itself.

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