Effective Capacitive Power Transfer

Michael P. Theodoridis

***Abstract*—Capacitive power transfer (CPT) systems have up to date been used for very low power delivery due to a number of limitations. A fundamental treatment of the problem is carried out and a CPT system is presented that achieves many times higher power throughput into low-impedance loads than traditional systems with the same interface capacitance and frequency of operation and with reasonable ratings for the switching devices. The development and analysis of the system is based well on the parameters of the capacitive interface and a design procedure is provided. The validity of the concept has been verified by an experimental CPT system that delivered more than 25 W through a combined interface capacitance of 100 pF, at an operating frequency of only 1 MHz, with efficiency exceeding 80%.**

***Index Terms*—Capacitive power transfer (CPT), contactless charging, contactless power transfer.**

I. Introduction

CAPACITIVE power transfer (CPT) is a potentially convenient method of delivering power without wires, with the use of capacitive plates. Its small system volume and profile, especially on the power-receiving side, means that it can be used for small-size applications such as biomedical implants [1], medical applications [2], or in charging of space-confined systems such as robots [3] or mobile devices [4], etc. Its design flexibility and low cost make it ideal for power delivery in reconfigurable and moving systems, such as catoms [5], robot arms, and latches [6], and in-track-moving systems [7]. Inductive power transfer (IPT), that is magnetic coupling between coils, seems to offer higher power transfer than CPT. However, IPT systems require a magnetic core in order to provide good coupling and in some cases shielding in order to prevent EMI. With increasing operating frequency, CPT may compete IPT, as the former can offer equally good galvanic isolation and does not require a costly, high-frequency rated magnetic core. Still, CPT has not been used in high-power systems as it suffers from limited power delivery and/or low efficiency.

Fig. 1 shows the topology used in all CPT systems up to date. An inverter is used to produce ac voltage and feed current through the capacitive interface and into the load. The capacitance of typical interfaces is in the order of a few hundred picofarads, and in order to feed substantial level of current through the interface, its high reactance is compensated by either a passive (inductive) [1]–[8] or, very rarely, an active

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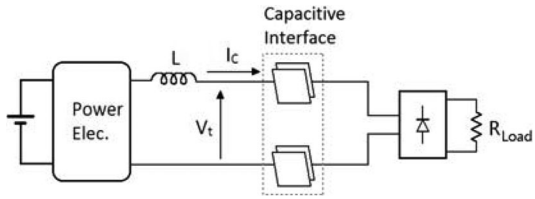

Fig. 1. Typical topology for CPT.

(negative capacitor) [9] element. There are a number of limitations which compromise the design of such systems.

The power that may be transferred through an interface such as this is

$$P_o = V_t I_C \cos(\varphi) \tag{1}$$

where V_t is the voltage across the terminals and φ is the angle between this voltage and the interface current I_C

$$\varphi = \tan^{-1}\left(-\frac{1}{\omega C R_e}\right) \tag{2}$$

$$I_C = \frac{V_t}{\sqrt{(1/\omega^2 C^2) + R_e^2}} \tag{3}$$

where R_e is the equivalent resistance of the load reflected at the input of the rectifier, not very different from R_{Load}.

At the same time, each capacitive element experiences a voltage stress equal to

$$V_C = \frac{I_C}{\omega C} \tag{4}$$

where C is the capacitance of each interface element.

Equations (1)–(4) connect the power throughput with all the critical parameters of the interface and the load characteristics. The capacitance C formed by the plates will have a maximum allowable voltage V_C and so will the voltage across the terminals, V_t. Designs in the past, [2]–[4], [8], [9], have not considered the terminal voltage although, if a reliable practical application is involved, this voltage is very critical.

In space-confined applications (see Fig. 2) and in order to maximize the power transfer, the area is used to the maximum so as to achieve high capacitance values. Therefore, the distance allowed between the capacitive terminals is very small and a maximum terminal voltage limit applies. Furthermore, with the frequencies of operation often exceeding 1 MHz, and with the terminal voltage usually reaching fractions of or even 1 kV—that is due to resonance with the inductor—there is a serious issue of electromagnetic interference (EMI). Finally, again due to the previous reasons, even the casing material between the terminal plates is subject to conducting high-frequency currents and experiencing losses. Therefore, the terminal voltage must be accounted for and rated in the vast majority of applications.

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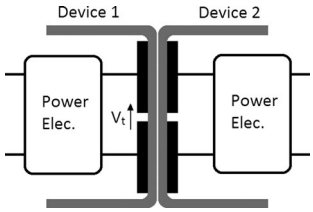

Fig. 2. Typical capacitive interface between devices. The voltage between the terminal plates V_t is also a critical parameter.

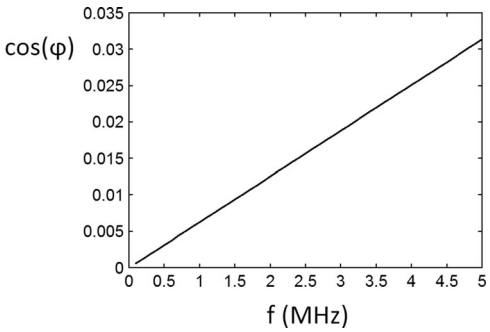

Fig. 3. Variation of cos(φ) with frequency for a typical CPT topology.

Equation (1), then, indicates that in order to have effective power transfer with the aforementioned system with reasonable terminal voltage and current, cos(φ) is required to be high. However, due to the typically low values of interface capacitance, the power factor of this topology is extremely low.

Fig. 3 shows the variation of cos(φ) with frequency for a typical CPT topology, where $R_e = 10\ \Omega$ and $C = 100$ pF. With the low values achieved even at high frequencies, the transfer of power is essentially based on the generation of very high V_t and I_C. V_t is limited due to reason explained previously but I_C is also limited. The interface current is limited to the point where the interface capacitor is subject to dielectric breakdown, due to the development of high voltage across it [see (4)]. This also means that, since the interface has to conduct the full-load current, low-impedance loads are prohibitive for such systems. At the same time, the inductance required to compensate the relatively small interface capacitance is quite large, which, combined with the fact that it also conducts the full-load current, imposes significant requirements on its rating/size if losses are to be kept low. The operation of these systems can be partly relieved by these problems only when the load resistance is in the order of kilohm, rendering the CPT method unsuitable for typical low-voltage applications.

Due to the above, CPT systems have until now exhibited limited output power and/or efficiency. In [4], an output power of 3.7 W is attainable with 63 pF of total (the series combination of the two plate capacitors) interface capacitance, with an efficiency of 80%, at 4 MHz. In [3], an output power of around 22 W is attainable with, however, 13 900 pF (13.9 nF) of total interface capacitance and with an efficiency of 47%, at 220 kHz.

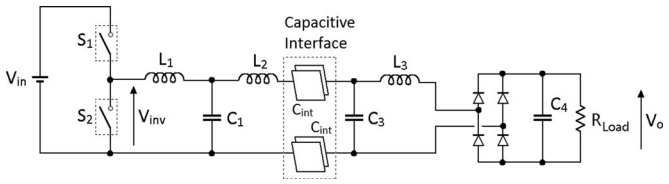

Fig. 4. Proposed CPT system.

The proposed CPT system overcomes the aforementioned limitations by 1) achieving higher values of cos(φ) and 2) by reduction of the current flowing through the interface with respect to the load current. This is done at the expense of higher circuit complexity. The experimental CPT system built with the proposed topology delivered more than 25 W through a combined interface capacitance of only 100 pF, at only 1 MHz and with an efficiency of 80%. The experiment was used as a means of validation of the analysis and it is expected that many times higher output power can be achieved.

II. Proposed System

Fig. 4 shows the proposed system. It is composed of a half-bridge (or alternatively full-bridge) inverter, three resonant inductors, two resonant capacitors, the capacitive interface and a current-fed rectifier.

Fig. 4 shows the components as they are to be placed in a practical application. However, since some of the components serve double purposes, Fig. 5 will be used to analyze the operation of the system.

Fig. 5 shows the topology of Fig. 4, rearranged so that it may be analyzed. The circuit has been divided into three networks, N_1–N_3. The series combination of the two interface capacitances has been replaced by C_2. C_1 and L_2 have been divided into two parts, as these components serve two purposes.

The second network is in effect equal to a short circuit, as L_{2a} acts as a compensating element for C_2. The third network N_3 is an *LLC* network that performs the two major functions connected to the power transfer capabilities of the system.

The first function performed by the *LLC* network is the increase of the power factor, cos(φ), where φ is the angle between the capacitive interface terminal voltage V_t and the interface current I_{C2} [see Fig. 6(a)]. It must be noticed here that L_{2b} is in practice on the power-sending side of the system in order to minimize the space of the power-receiving side. In effect, it is not all the *LLC* network that performs the rise of cos(φ) but part of it, in conjunction with C_2. R_e is the equivalent resistance of the load with the rectifier. Fig. 6(b) shows the power factor [see (5)], of the proposed system for the same component values as for Fig. 3 and for typical values of the involved parameters ($Q = 10$, $k = 10$). It is evident that the proposed system achieves over ten times higher power factor than traditional system arrangements.

$$\varphi = -\frac{A(Q^2 + k + 1) + B}{AkQ} \tag{5}$$

where

$$A = kR_e\omega C_2 Q \tag{6}$$

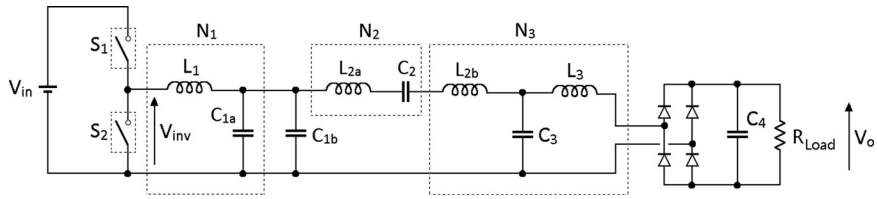

Fig. 5. Proposed CPT system of Fig. 4, rearranged for analysis.

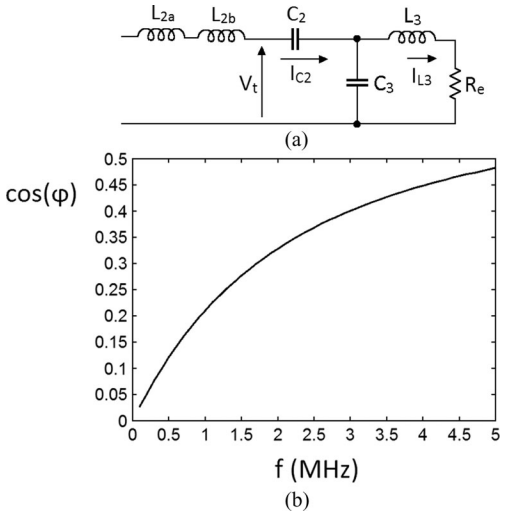

Fig. 6. Proposed CPT system achieves high power factor.

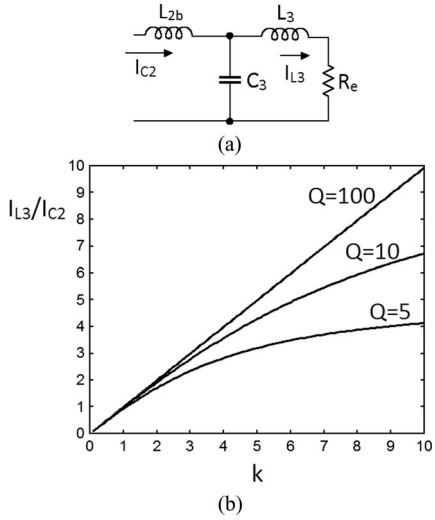

Fig. 7. Current amplification property of the *LLC* network.

$$B = Q^2 + k^2 + 2k + 1 \tag{7}$$

$$k = \frac{L_{2b}}{L_3} \tag{8}$$

$$Q = \frac{\omega L_3}{R_e} \tag{9}$$

$$\omega = \frac{1}{\sqrt{L_{\text{comb}} C_3}} \tag{10}$$

$$L_{\text{comb}} = \frac{L_{2b} L_3}{L_{2b} + L_3} \tag{11}$$

and, as known for current-fed rectifiers

$$R_e = R_{\text{Load}} \frac{8}{\pi^2}. \tag{12}$$

The second function performed by the *LLC* network is the load current multiplication. Fig. 7(a) shows again the *LLC* network, this time with the inductor on the power-receiving side. This is done for clarity and does not affect the analysis as the current through L_{2b} is the same as that of the capacitive interface I_{C2}. It is found that the ratio of load current to interface current is dependent on two parameters of the *LLC* network [see (13)]. Fig. 7(b) was generated for a range of these parameters and shows that the current ratio under typical conditions ($Q = 10$, $k = 10$) can be higher than 5

$$\frac{I_{L3}}{I_{C2}} = kQ \sqrt{\frac{1}{Q^2 + k^2 + 2k + 1}}. \tag{13}$$

The high load-current is now conducted only by the several times smaller resonant inductor L_3. L_{2b} is added to the compensating inductor and can be as large as the latter, but the current they both conduct is typically five to ten times lower than the load current. Since the inductor size and losses are dependent on I^2 ($0.5LI^2$ and I^2R, respectively), a great reduction in both is achieved.

The introduction of the *LLC* system raises the total impedance as it would be "seen" from a low-voltage inverter output. For this reason, L_1 and C_{1a} have been employed in order to match this impedance (of N_2 and N_3) to the inverter output impedance. Here again, the high output current of the inverter is conducted only by the relatively small resonant inductor L_1. The second part of C_1, i.e., C_{1b}, is used only to compensate the reactive part of the total impedance of N_2 and N_3 and therefore make this impedance appear as purely resistive. This greatly simplifies the design of N_1. This capacitor is many times smaller than C_{1a}.

N_1 and C_{1b} are not needed in the case of high supply voltage V_{in} in which case the output impedance of the inverter can directly match the circuit impedance. A transformer may also be used to raise the voltage. The most complicated case, that is using N_1 and C_{1b}, is considered here for the design procedure.

With the two aforementioned functions performed by the *LLC* network, and the complementary functions of the other components, the advantage of the proposed system in achieving high-power throughput for any given capacitive interface is fairly evident. The increased power factor and the load current multiplication mean that more power can be interfaced with

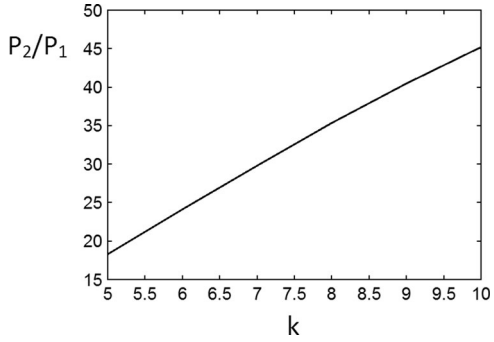

Fig. 8. Power transfer capability between the proposed and traditional system for fixed V_C/V_{C2}.

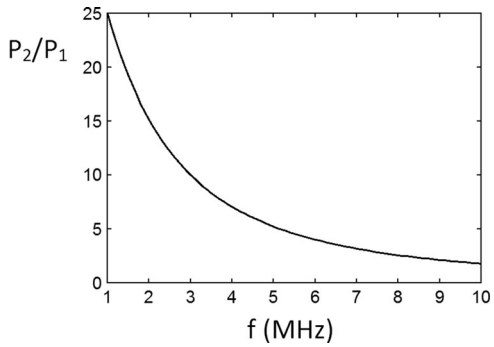

Fig. 9. Power transfer capability between the proposed and traditional system for fixed V_t.

lower terminal and capacitor voltages and with much lower current rating for the compensating inductor. For a comparison between the two systems, a capacitive interface may be considered with $\frac{1}{2}C = C_2 = 100$ pF and a load with $R_e = 10\,\Omega$. There are two ways to compare the systems, depending on whether the terminal voltage is judged to be critical or not. The first way is by neglecting the terminal voltage and assuming that with both systems, at any same frequency, the maximum interface capacitor voltage is reached, i.e., the same maximum interface current is conducted. Fig. 8 shows that in this case, due to the current multiplication, the power transfer achieved by the proposed system, P_2, is many times higher than that achieved by the traditional system, P_1. The second way to compare the systems is by assuming that the same maximum terminal voltage must be kept. In this case, the power comparison depends on the frequency of operation. Fig. 9 shows that the proposed system, due to better interface power factor, is capable of transferring higher power, especially at low frequencies ($k = 10$ here). Even at 10 MHz, where the interface impedance has reduced dramatically, the propose system delivers twice as much power to the load. Furthermore, Fig. 10 shows that, for the same case, the interface current of the proposed system, I_{C2}, is many times lower than that of the traditional system, I_C, therefore resulting in a system with much lower conduction/magnetic losses, interface capacitor voltage, and component rating.

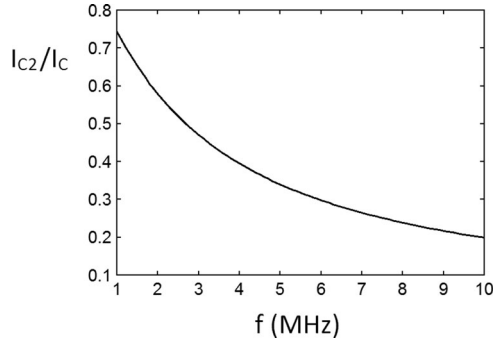

Fig. 10. Interface current advantage of the proposed over traditional system for fixed V_t.

Furthermore, the power-receiving end of the system occupies little volume since L_3, the most space-occupying component of all, is expected to have low value of inductance. Then, using a resonant inverter with zero-voltage switching (ZVS) and a current-fed rectifier means that the switching losses of the active power devices and the diodes are significantly minimized. ZVS can be achieved with a very small deviation above the system resonant frequency, which places the inverter output current at an appropriate phase with its output voltage, with the current not varying significantly in amplitude than when at exact resonance. Finally, the active switching devices need only to withstand the supply voltage and conduct a reasonable level of current, while the diodes need only to withstand the output voltage and conduct the output current.

III. Design Procedure

The design of the proposed system is based on an iterative process, as the circuit is described by high-order equations and a concise solution is unavailable. Known data for the design are the input requirement $V_{\rm in}$, the output requirements $R_{\rm Load}$ and P_o, and the capacitive interface characteristics, C_2, $V_{C2\_\max}$, and $V_{t\_\max}$. The frequency of operation is also a known requirement. As mentioned, the system can provide the required throughput power at any frequency. The frequency affects only the energy stored in the various reactive components, and eventually their size, and the various losses. The selection of frequency must be made upon the best compromise between system volume (decreases with increased frequency) and losses due to switching and conduction (both increase with increasing frequency, assuming component parasitic resistance and skin effect). This process cannot be the subject of the presented design as it also relates to the selection of switching devices and type of reactive components, making a general design guideline unrealistic. The aim of the presented design procedure is, for a given frequency, to provide solution for the values of the system components such that the system volume and component conductions losses are minimal. It has been found that the increase in the quality factor of N_3, Q, increases the size of the components, while its decrease causes deviations from the assumption of sinusoidal resonance. A good compromise between the two opposing effects is to keep Q at a typical value of around 10.

The design iterations are performed with the variation of two key parameters, V_t and k, until three conditions are met. The first condition is that the required power transfer is achieved

$$P_o = V_t I_{C2} \cos(\varphi) \tag{14}$$

where

$$I_{C2} = \frac{V_t}{Z_{CLC}} \tag{15}$$

$$Z_{CLC} = \sqrt{\frac{A^2(Q^2+1) + 2A(Q+k+1) + B}{\omega^2 C_2^2 B}} \tag{16}$$

[note: CLC stands for the network at the right of the V_t symbol in Fig. 6(a)—φ is found from (5)].

The second condition is that the interface capacitor voltage does not exceed its maximum [see (17)]. The same applies for V_t but it is already taken into account in the range of its variation in the iteration process

$$V_{C2} = \frac{I_{C2}}{\omega C_2} < V_{C2\_\max}. \tag{17}$$

There are many V_t–k combinations which can satisfy (14) and (17) simultaneously. From all the combinations, only the one that results in the lowest maximum stored energy E [see (18)] in the inductive components is chosen

$$E = \frac{1}{2} L_2 {I_{C2}}^2 + \frac{1}{2} L_3^2 {I_{L3}}^2 \tag{18}$$

where L_3 is found directly from (9) and I_{L3} is connected to I_o (known from root of P_o/R_{Load}) through the rectifier conversion ratio

$$I_{L3} = I_o \frac{\pi}{2\sqrt{2}} \tag{19}$$

and

$$L_2 = L_{2a} + L_{2b} \tag{20}$$

$$L_{2a} = \frac{1}{\omega^2 C_2} \tag{21}$$

where L_{2b} is found from (8).

The energy stored in the capacitors needs not be taken into account as the most space-occupying components are the inductors. L_1 is not considered, because, as mentioned, it is a component that may be omitted, depending on design. Furthermore, its stored energy follows the trend of the other two inductors.

Once the optimum values of V_t and k have been determined, the values of the rest of the components may be found as follows.

C_3 is calculated from (10) and (11). The value of the compensating capacitor was found by means of numerical calculations to depend solely on the inductor ratio under all conditions

$$C_{1b} = \frac{C_3}{k}. \tag{22}$$

The calculation of the values for the components of N_1 is based on the fact that the network converts the output voltage of the inverter V_{inv} to the required voltage across C_1 so that the total impedance of N_2 and N_3 conducts I_{C2}. Since N_2 is a short circuit at resonance, the impedance of N_2 and N_3 as "seen" from C_1 is equal to the impedance of the *LLC* network, i.e., of L_{2b}, L_3, C_3, and R_e. Therefore

$$V_{C1} = I_{C2} Z_{LLC} \tag{23}$$

where I_{C2} is found by (15) and the impedance of the *LLC* network and its phase angle are

$$Z_{LLC} = Q R_e k^2 \sqrt{\frac{1}{Q^2 + k^2 + 2k + 1}} \tag{24}$$

$$\psi = \tan^{-1}\left(\frac{k+1}{Q}\right). \tag{25}$$

Then, Q', the quality factor of N_1, is found. It is equal to the conversion ratio of N_1

$$\frac{V_{C1}}{V_{\mathrm{inv}}} = Q' \tag{26}$$

and

$$V_{\mathrm{inv}} = V_{\mathrm{in}} \frac{2}{\pi}. \tag{27}$$

Finally

$$L_1 = \frac{R_e'}{Q'\omega} \tag{28}$$

$$C_{1a} = \frac{1}{\omega^2 L_1} \tag{29}$$

where R_e' is the effective resistance of the *LLC* network as "seen" from C_{1a}, that is before the compensating capacitor C_{1b}:

$$R_e' = \frac{V_{C1}}{I_{C2}\cos(\psi)}. \tag{30}$$

The following pseudocode listing presents the algorithm used to design the system.

```
Set values for V_in, R_Load, P_o, C_2, V_C2_max, and V_t_max
Set ω and Q
For V_t = 0 to V_t_max
        For k = 1 to 30
                If (14) and (17) hold true within 1%
                Calculate E from (18) and store it along
                with values of V_t, V_C2 and k
                Else continue with stepping parameters
        End of k loop
End of V_t loop
From table of stored values of E, find minimum value and
corresponding V_t, V_C2, and k
Calculate components using (5)–(12) and (14)–(30)
```

Fig. 11 shows algorithm-generated results based on a case study for an interface with $V_{t\_\max} = 700$ V, $V_{C2\_\max} = 500$ V, $C_2 = 100$ pF, and a load of $R_{\mathrm{Load}} = 10\ \Omega$, for a range of operating frequencies.

For a typical range of frequencies, it is shown that the total inductor stored energy reduces with increasing frequency and increases with output power, as expected. The inductor ratio k remains unaffected by the output power and decreases with increasing frequency. It seems that the ratio of terminal to capacitor voltage increases with frequency; however, the capacitor

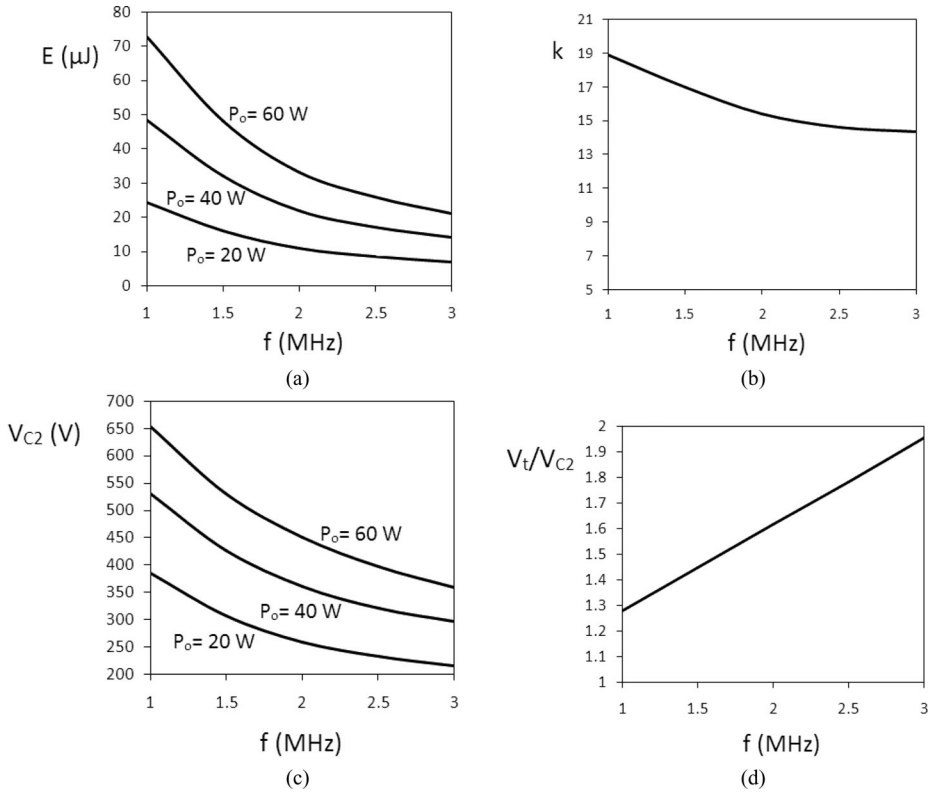

Fig. 11. Results from the design algorithm for a case study.

voltage alone reduces with increasing frequency. For a certain output power, the minimum design frequency must, therefore, be such that neither $V_{t\_\max}$ or $V_{C2\_\max}$ are exceeded. For example, if the output power is required to be 40 W, then the system must be operated above 1.15 MHz (where V_{C2} reaches 500 V). From then on, the frequency can be chosen to be at any higher value up to the point where the switching and conduction losses compromise the efficiency of the system.

To compare these results with the results from the typical system in Fig. 1, for the same capacitive interface and load (R_{Load}) as above, for 1 MHz and maximum terminal voltage of 490 V [see Fig. 11(c)], the presented system can output 20 W while the system in Fig. 1 can output 0.83 W. Even if the terminal voltage level was to be neglected, then for the typical system to reach 20 W (by large increase of the terminal voltage), the interface capacitor would have to sustain 2.5 kV, while the compensating inductor would have to be highly overrated or it would suffer significant losses due to conducting the full load-current. With the presented system, the compensating inductor (and the similar size $L_{2\mathrm{b}}$) will conduct a current that is 8.5 times lower than the load current [see (12)] with $Q = 10$ and $k = 10$.

Despite the complicated structure, the proposed system exhibits good controllability/tolerance against the variation of critical components, such as the interface capacitance, and the variation of the load. Although the study of the response of the system to these disturbances lies beyond the scope of this paper, relevant experimental results are presented in the following section.

IV. Experimental Validation

The experiment was set up with the target to deliver power to a mini laptop computer through a capacitive interface of 100 pF. The interface was made of square copper boards with a plate distance that dictated a V_{C2_max} of around 500 V. Since there was no real restriction, the maximum terminal voltage was chosen by convention to be 700 V. The output voltage was targeted for 19 V, as most laptops require, and the load resistance was set to 10 Ω, typical for a mini laptop. The operating frequency was chosen to be 1 MHz; a few runs of the design algorithm showed that the interface-related voltages were at that frequency safely lower than the maximum (also shown in Fig. 11(c) and (d) for around 40 W). The input voltage was chosen to be 24 V so as to verify the matching capabilities of N_1. The design algorithm gave the component and parameter values listed in Table I. The switching devices used were the STP30NF10 MOSFETs and the B540C diodes. The capacitors used were all of the silvered-mica type so as to ensure stability.

As seen from Table I, the system delivered 26.5 W at 16.3 V with efficiency slightly higher than 80%, while the capacitive interface-related voltages were within less than 2% of the calculated ones. The frequency was set 10 kHz higher than the resonant frequency so that a small phase difference between inverter output voltage and current was possible and ZVS was achieved (see Fig. 12). The losses were mainly comprised of the switching losses of the MOSFETs, the diode conduction losses, and the conduction/magnetic losses of L_2, which should ideally

TABLE I
DESIGN INPUT AND OUTPUT DATA AND EXPERIMENTAL RESULTS

Input Data	Calculated Values	Experimental Results
R_{Load}= 10 Ω	L_1= 15.31 μH	P_{in}= 32.9 W
P_o= 36 W	C_{1a}= 1.65 nF	P_o= 26.5 W
V_o= 19 V	C_{1b}= 110.8 pF	V_o= 16.3 V
V_{in}= 24 V	L_{2a}= 253.3 μH	
Q= 10	L_{2b}= 240.8 μH	
f= 1 MHz	C_3= 2.07 nF	f= 1.01 MHz
C_2= 100 pF	L_3= 12.89 μH	
V_{t_max}= 700 V	V_t= 507 V	V_t= 511 V
V_{C2_max}= 500 V	V_{C2}= 393 V	V_{C2}= 387 V

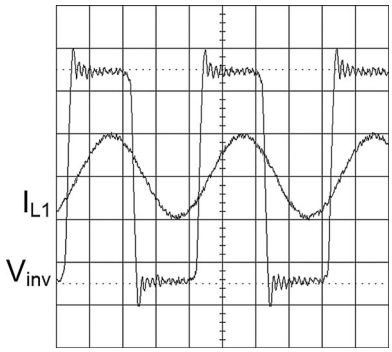

Fig. 12. Inverter output waveforms. $V_{\rm inv}$: 5 V/div, $I_{L\,1}$: 5 A/div, 250 ns/div.

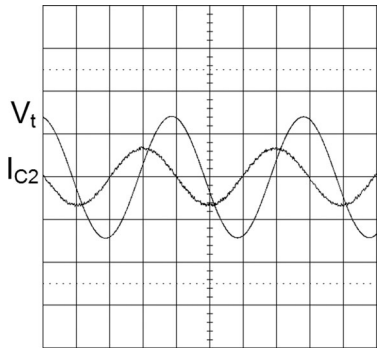

Fig. 13. Terminal voltage and current. V_t: 500 V/div, $I_{C\,2}$: 0.5 A/div, 250 ns/div.

have been made of Litz wire and very low loss core. Fig. 13 shows the angle φ of the capacitive interface being around 75°, close to the predicted 73°. Finally, Fig. 14 shows the currents of the interface and of inductor L_3; the ratio between the two is around 7.3, instead of the expected 8.5. Pspice simulations have verified that this deviation, as well as part of the output voltage deviation, is attributed to the operation of the circuit slightly above resonance. This effect may be compensated for by introducing an empirical coefficient within the design process or by introducing a ZVS-related function as a further constraint.

As regards the tolerance of the system to component variation and its controllability, another two experiments were performed. A 10% reduction in interface capacitance was imposed and the result was that, in order to restore the output voltage, a frequency increase of only 2.5% was required. The maximum achievable output voltage after restoration was around 2.5% lower than before the capacitance reduction, and the efficiency dropped to 76.5%. As regards control from the primary side components, it appears that, despite the involvement of several variables, load disturbances appear in the inverter output current with a fairly good gain. An increase of the load resistance by 10% resulted in an inverter output current increase of 9.2%. That was due to the increase of the impedance "seen" by C_{1a}, meaning increase in the quality factor of N_1 and, therefore, increase in the resonant current.

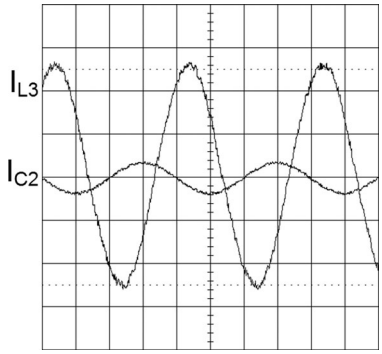

Fig. 14. Terminal and resonant tank current. $I_{L\,3}$, $I_{C\,2}$: 1 A/div, 250 ns/div.

V. CONCLUSION

A fundamental treatment of the transfer of power by means of a capacitive interface has shown that traditional CPT systems suffer from low power factor and high conduction/magnetic losses on the compensating inductor. The proposed system drastically increases the power factor at the interface and achieves multiplication of the load current with respect to the interface current, therefore significantly reducing the voltage stresses of the interface and the conduction/magnetic losses of the compensating inductor. Several times higher output power is achieved without the need to increase the frequency of operation. The proposed design algorithm ensures minimization of the system size and compliance with the voltage ratings of the interface. The validity of the analysis was verified by a prototype system which delivered several times higher output than traditional systems with the same capacitive interface characteristics and operating frequency.

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