ENG-326

0.35 um CMOS C35 30V Module Design Rules

Revision #: 6.0

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Table of Contents

1 Introduction 3
1.1 Revision 3
1.2 Process Family 3
1.3 Available Circuit Elements - Required Modules 3
1.4 Related Documents 4
2 General 5
2.1 Definitions 5
3 Layer Overview 6
3.1 CMOS Core Module 6
3.2 Isolated PTUB Module 6
4 Layer Rules 7
4.1 CMOS Core Module 7
4.1.1 FIDEF 7
4.2 Isolated PTUB Module 7
4.2.1 PFIMP 7
5 Element Rules 8
5.1 Transistors 8
5.1.1 NMOS18T 8
5.1.2 NMOS30M 9
5.1.3 PMOSD30M 10
6 Support 11
7 Copyright 11

1 Introduction

1.1 Revision

Revision	Date	Changes	Affected pages
1.0	2007-08	First version of design rule specification	1-8
2.0	2008-07	Change NLDD, NMOS30M, S1NWPW Add NMOS30T	1-10
3.0	2008-11	Delete NMOS30T Add NMOS18T	1-10
4.0	2010-01	Delete FIMP, NLDD, NLDD50	3-9
5.0	2012-05	Add isolated PTUB module, PFIMP, PMOSD30M	3, 5-7, 10
6.0	2012-10	Change PMOSD30M Add element revisions	8-10

Note: This document is a supplement to the document
“0.35 um CMOS C35 Design Rules” Eng - 183.

1.2 Process Family

See document “0.35 um C35 CMOS Design Rules” Eng - 183

1.3 Available Circuit Elements - Required Modules

Transistor	CMOS core	5V Gate	Isolated PTUB
NMOS30M	x	x	
NMOS18T	x		
PMOSD30M	x	x	x

1.4 Related Documents

Description	Document Number
0.35 um CMOS C35 30V Module Process Parameters	ENG-327
0.35 um CMOS C35 Design Rules	ENG-183
0.35 um CMOS C35 RF SPICE Models	ENG-188
0.35 um CMOS C35 Noise Parameters	ENG-189
0.35 um CMOS Matching Parameters	ENG-228
0.35 um ESD Design Rules	ENG-236

Note: All data represent drawn dimensions. Graphical illustrations are not to scale.

2 General

2.1 Definitions

Process Layers

PFIMP (PW): isolated p-tub layer

Definition Layers

Notes: These layers are not used in chip production.
They are necessary for design tools, e.g. design rule check.

HVDEF (HV): high voltage definition layer, text layer with high voltage element names
FIDEF (PW): field implant definition layer

Elements

NMOS18T: high voltage n-channel MOSFET with thin-oxide
NMOS30M: high voltage n-channel MOSFET with mid-oxide
PMOSD30M: high voltage p-channel MOSFET with mid-oxide (butted contacts)

3 Layer Overview

3.1 CMOS Core Module

Definition Layers

Name	GDS2 Layer / Datatype	Description
HVDEF	13 / 0	high voltage definition
FIDEF	62 / 29	FIMP definition

3.2 Isolated PTUB Module

Drawn Process Layers

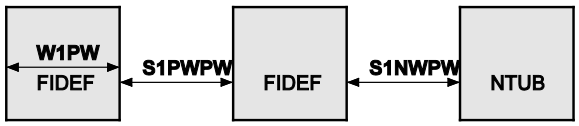
Name	GDS2 Layer / Datatype	Width [um]	Spacing [um]
PFIMP	12 / 0	0.8	1

4 Layer Rules

4.1 CMOS Core Module

4.1.1 FIDEF

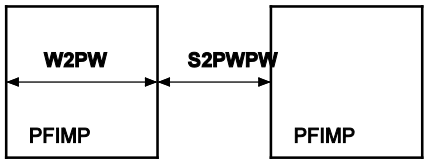
Rule	Description	Value [um]
W1PW	Minimum FIDEF width	1.7
S1PWPW	Minimum FIDEF spacing	1
S1NWPW	Minimum FIDEF to NTUB spacing	6.5



4.2 Isolated PTUB Module

4.2.1 PFIMP

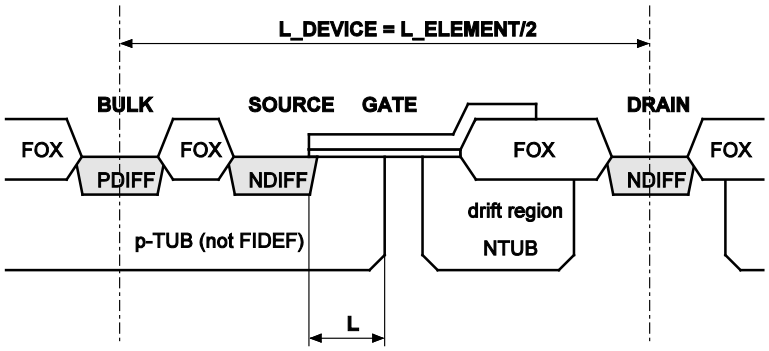
Rule	Description	Value [um]
W2PW	Minimum PFIMP width	0.8
S2PWPW	Minimum PFIMP spacing	1
PWR002	(PFIMP and not (HVDEF or SFCDEF)) is not allowed	



5 Element Rules

5.1 Transistors

5.1.1 NMOS18T

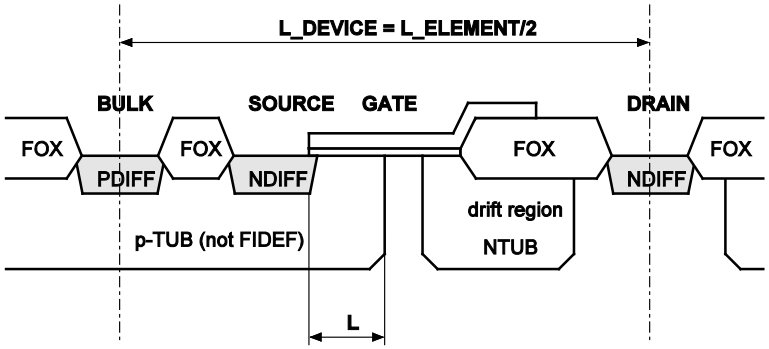


Rule	Description	Value [um]
NMOS18T_REV	NMOS18T revision	2
NMOS18T_L	Minimum channel length	0.5
NMOS18T_W2	Minimum channel width / 2	5

Symbol	Description	Value [um]
NMOS18T_L_DEVICE	Minimum device length	L+5.75
NMOS18T_L_ELEMENT	Minimum element pitch	2L+11.5

Note: The layout is predefined. Only W and L may be changed.

5.1.2 NMOS30M

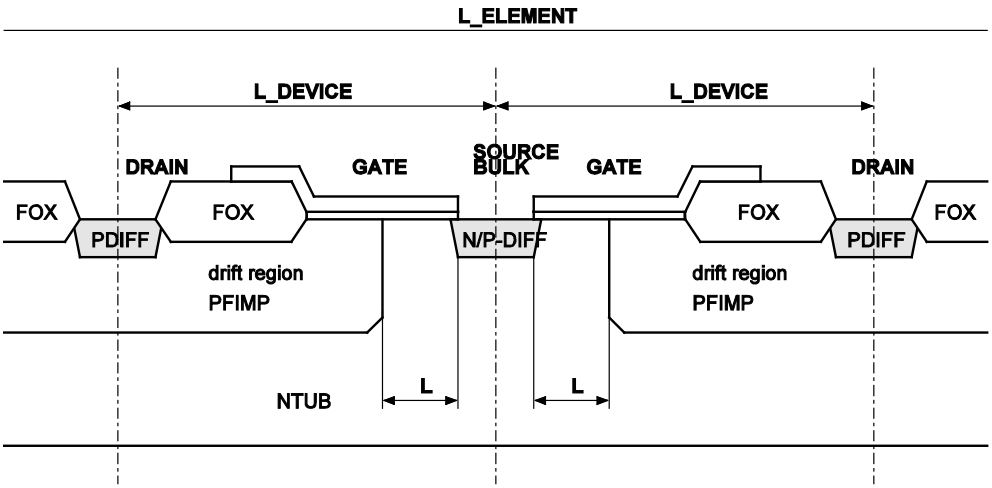


Rule	Description	Value [um]
NMOS30M_REV	NMOS30M revision	3
NMOS30M_L	Minimum channel length	0.5
NMOS30M_W2	Minimum channel width / 2	5

Symbol	Description	Value [um]
NMOS30M_L_DEVICE	Minimum device length	L+5.65
NMOS30M_L_ELEMENT	Minimum element pitch	2L+11.3

Note: The layout is predefined. Only W and L may be changed.

5.1.3 PMOSD30M



Rule	Description	Value [um]
PMOSD30M_REV	PMOSD30M revision	2
PMOSD30M_L	Minimum channel length	0.6
PMOSD30M_W2	Minimum channel width / N W2 = 1 + k * 1.8 (k = 3,4,5,...)	6.4
PMOSD30M_R1	BULK and SOURCE must be connected with MET1	

Symbol	Description	Value [um]
PMOSD30M_L_DEVICE	Minimum device length	L+4.1
PMOSD30M_L_ELEMENT	Minimum element pitch	4L+26.3

Note: The layout is predefined. Only W and L may be changed.
Allowed configurations: B-S-G-D-G-S-B, B-S-G-D-G-SB-G-D-G-S-B,....

6 Support

For questions on process parameters please refer to:

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