Voltage References and Biasing

1.0 Introduction

In this set of notes, we take up the study of an important topic: How to generate voltages and currents that are relatively independent of supply voltage and/or temperature. Because CMOS offers relatively limited options for realizing bias circuits, we'll see that some of the most useful biasing idioms are actually those based on bipolar circuits. A parasitic bipolar device exists in every CMOS technology, and may be used in a bandgap voltage reference, for example. Even though the characteristics of parasitic transistors are far from ideal, the performance of bias circuits made with such devices is frequently vastly superior to that of "pure" CMOS bias circuits.

In what follows, it is worthwhile to keep in mind that any voltage we produce must depend on some collection of parameters that ultimately have the dimensions of a voltage (such as kT/q, for example). Similarly, any current we produce must depend on parameters that ultimately have the dimensions of current (such as V/R). Although seemingly obvious and trivial statements, we'll see that they are extremely useful guides for the design of stable references.

2.0 Review of Behavior of Diodes

While the voltage across a forward-biased diode is relatively insensitive to current because of the logarithmic dependence of diode current on diode voltage, its variation with temperature is significant. To understand the precise nature of the temperature dependence, recall that the diode voltage may be expressed as:

$$V_D = nV_T ln\left(\frac{I_D}{I_S}\right) \tag{1}$$

where V_T is the thermal voltage, kT/q, and n, the ideality factor, is typically between 1 and 1.5 in diodes. A transistor's V_{BE} conforms more closely to the "ideal diode law" than do ordinary diodes, so we will assign n a unity value in all that follows.

It is frequently inferred incorrectly from Eqn.1 that V_D has a positive temperature coefficient (TC) because of its proportionality to V_T. The fly in the ointment is that I_D itself has an exponential temperature dependence, and this alters the situation considerably. To clarify matters, consider the following quasi-empirical expression for I_S:

$$I_S = I_0 exp\left(-\frac{V_{G0}}{V_T}\right) \tag{2}$$

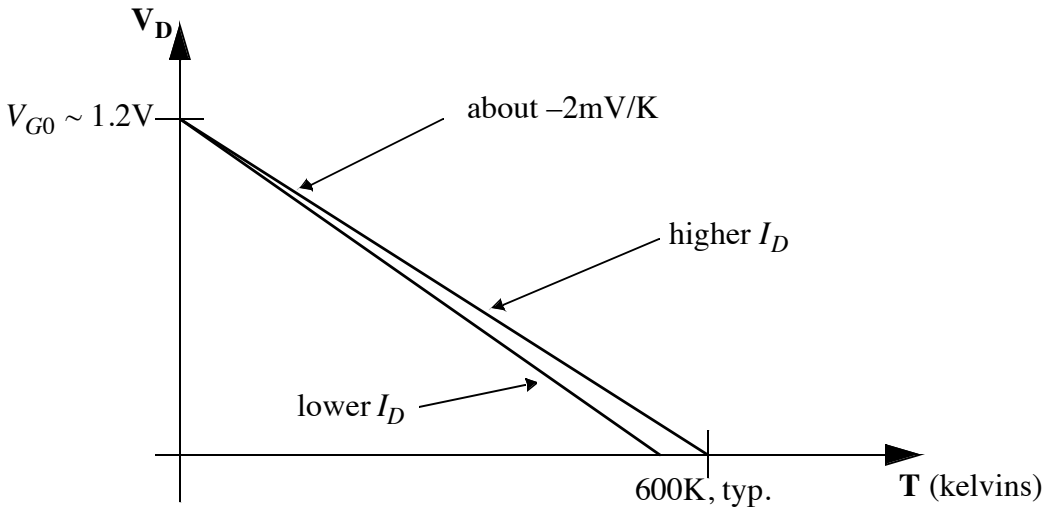
where I_O is some process- and geometry-dependent current[1] (I_0 is typically around 20 orders of magnitude larger than I_S at room temperature, so I_0 is much larger than typical values of I_D), and V_{G0} is the bandgap voltage (about 1.2 volts) extrapolated to absolute zero.

Using this detailed expression for I_S, we can expand the equation for V_D as follows:[2]

$$V_D = V_{GO} - V_T ln\left(\frac{I_0}{I_D}\right) \tag{3}$$

Thus, we see that the junction voltage decreases (linearly if I_0 were constant) from a value of V_{G0}, as seen in the following plot of V_D *vs*. temperature at constant diode current:

FIGURE 1. Approximate behavior of V_D *vs*. temperature



Note that this equation tells us that V_D *always* equals V_{G0} at absolute zero.[3] Furthermore it's easy to see that, if I_0 were constant, the temperature coefficient at any temperature is simply

$$\frac{dV_D}{dT} = -\frac{V_{G0} - V_D}{T} \quad . \tag{4}$$

1. It also depends weakly on temperature, but we'll defer a detailed discussion about the behavior of I_0 until the section on bandgap voltage references.

2. The minus sign is not an error. Just remember that the argument of the log here is typically much larger than unity.

3. Again, this value is an extrapolated one. It must be stressed that the behavior of real junctions at both extremes of temperature will differ from that shown; the equations presented lose validity at extremely cold temperatures (say, <100K) because of carrier freeze-out (i.e., failure of dopants to ionize) and because of bandgap variation with temperature, and at high temperatures (>450-500K) because the silicon goes intrinsic.

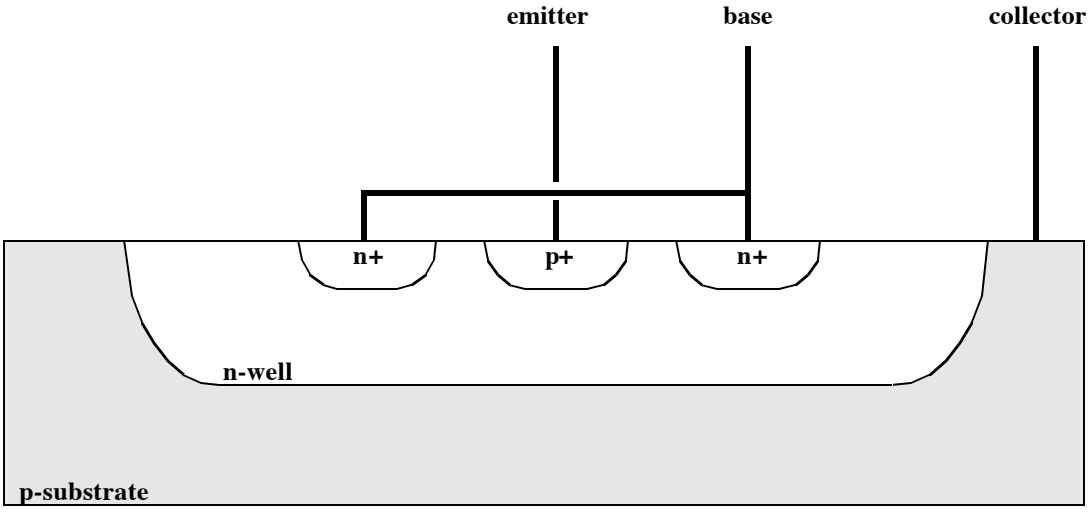
With the assumption of constant I_0, the temperature coefficient is independent of temperature and equal to about –2mV/K. This linearly decreasing behavior is known as CTAT, for "complementary to absolute temperature." Note that the voltage does depend (logarithmically) on diode current, so the temperature coefficient also depends somewhat on the diode current, with lower currents associated with higher temperature coefficients.

Although a V_D-based reference can provide an output that depends very little on supply voltage, the CTAT behavior may or may not be acceptable, depending on the application. However, we shall see that the CTAT behavior of a V_D is particularly valuable for use in a class of references based on the bandgap voltage V_{G0}. We'll take up the detailed study of bandgap references in Section5.0.

3.0 Diodes and Bipolar Transistors in CMOS Technology

The most flexible option for realizing diodes and bipolar transistors in standard CMOS technology derives from the parasitic substrate pnp transistor available in *n*-well processes. The p+ source/drain diffusions serve as the emitter, the *n*-well as the base, and the substrate as the collector:

FIGURE 2. Parasitic substrate PNP in *n*-well CMOS (not drawn to scale)



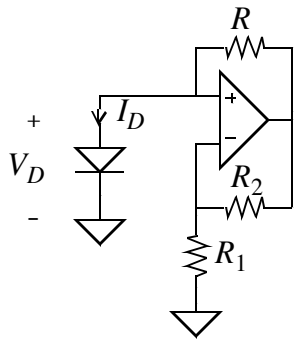
In applications where it is important to reduce series base resistance, it is advisable to surround completely the emitter with n+ diffusions placed as close to the emitter as the design rules allow, as suggested by Fig.2.

Just as its counterpart in inexpensive bipolar processes, the substrate pnp in CMOS technology can only be used in circuits that allow the collector to be at substrate potential. Fortunately, there are numerous circuits that satisfy this condition. For example, a simple voltage "reference" can be constructed with this device connected as a grounded diode, in which the emitter is the anode, and the cathode is the base and collector (substrate) tied together.

4.0 Supply-Independent Bias Circuits

To minimize sensitivity to power supply variations, it is desirable to derive the bias currents for reference voltages from the reference voltages themselves, rather than directly from the power supply. Although it may seem a violation of some fundamental law (the "no free lunch" principle), it is possible to arrange for this condition. To illustrate how one may accomplish this feat, consider the following circuit:

FIGURE 3. Self-biased reference



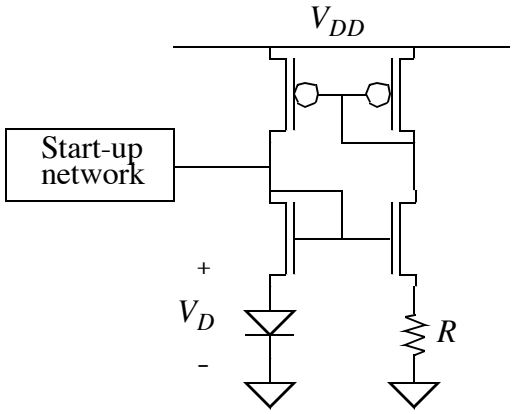
$$I_D = \frac{V_D\left(\frac{R_2}{R_1}\right)}{R}$$

As you can see, the current through the diode depends on the diode voltage itself, rather than on the supply voltage. This technique thus provides excellent supply-voltage independence.

An important practical note is that a start-up network is always necessary in self-biased circuits because there are two states, one which is stable in the conventional sense, and another in which all currents are zero.[4] The start-up network guarantees that the circuit gets out of the undesired metastable state.

Most practical implementations of the self-biased circuit dispense with the op-amp:

FIGURE 4. Self-biased reference



$$I_D = \frac{V_D}{R}$$

4. Even though the all-zero state is metastable, practical circuits are found in this state a maddeningly large portion of the time. A start-up network is therefore mandatory for reliable operation.

The PMOS mirror[5] enforces equality of the NMOS drain currents, and hence that of the NMOS V_{GS}'s. Thus, the diode voltage appears across R; the corresponding current is the same in both halves of the mirror and is therefore the bias current of the diode itself. Thus, as in the op-amp version of this circuit, the diode provides its own bias current.

The self-biased circuit of Fig.4 is quite versatile. It should be clear that the diode may be replaced by a variety of elements. For example, a diode-connected MOSFET would produce a bias current of V_{GS}/R, or a zener diode (if available) could be used instead. As we'll see in the next section, the self-biased circuit is particularly useful in realizing bandgap voltage references in CMOS technology.

5.0 The Bandgap Voltage Reference

Since IC technology directly offers no reference voltages that are inherently constant, the only practical option is two combine two voltages with precisely complementary temperature behavior. Thus, the general recipe for making temperature-independent references is to add a voltage that goes up with temperature to one that goes down with temperature. If the two slopes are equal in magnitude but opposite in sign, the sum will be independent of temperature.

Without question, the most elegant realization of this idea is the bandgap voltage reference, for it produces an output voltage that is traceable to fundamental constants, and therefore is relatively insensitive to process, temperature and supply variations.

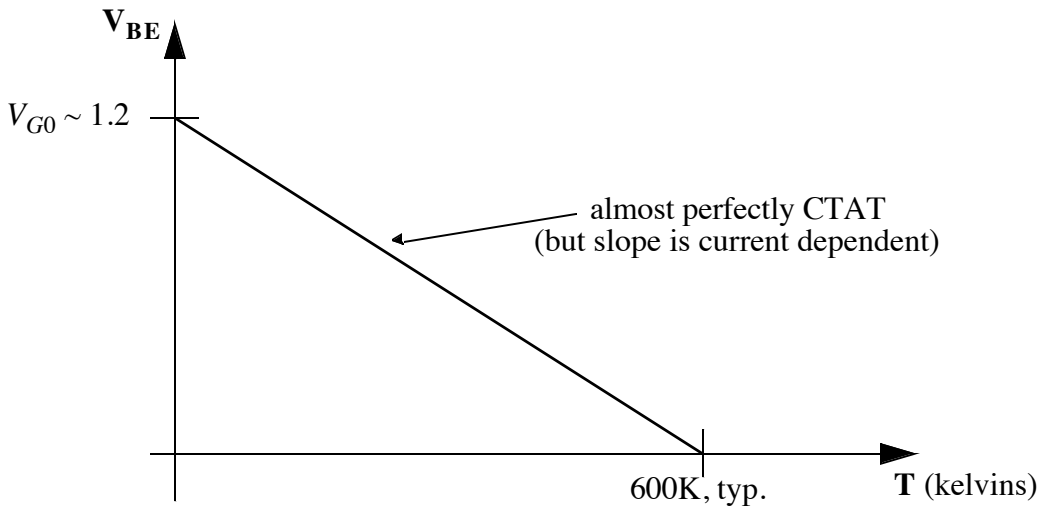
The first widely used bandgap voltage reference was designed by Bob Widlar in the 1970s, in the hugely popular and revolutionary LM309 5-volt regulator IC from National Semiconductor. It was the first reference whose initial accuracy was good enough to eliminate the requirement for adjustment by the end user. Thus, only three terminals were needed (allowing use of inexpensive transistor packages), making this part as easy to use as one could hope.

To understand quantitatively how bandgap references work, we need to re-examine the detailed behavior of junction voltage with temperature. Since transistor junctions exhibit more nearly ideal characteristics than ordinary diodes, we will assume bandgap implementations that use transistors. A plot of V_{BE} vs. temperature is repeated here for convenience:[6]

5. Better mirrors would almost always be used in practice; simple ones are shown to reduce schematic clutter.

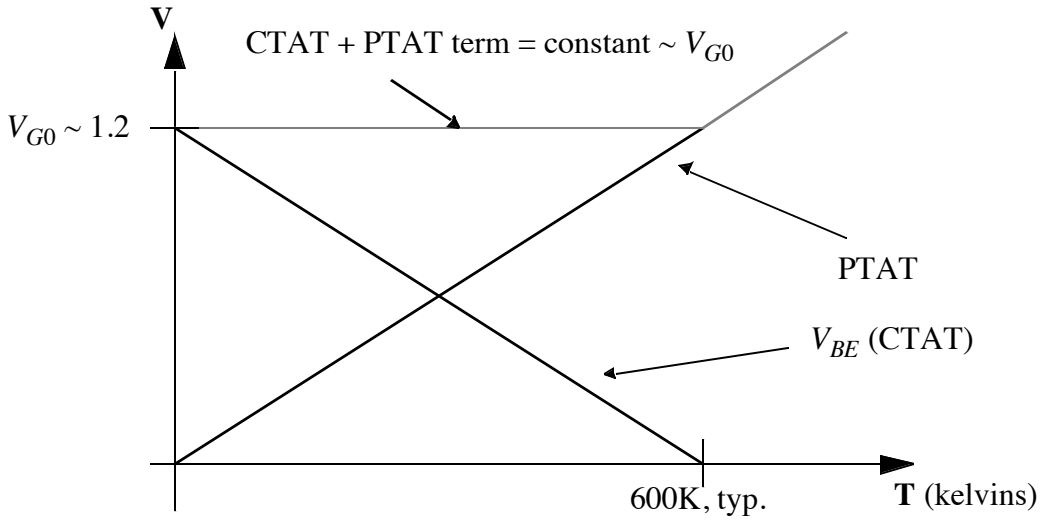
6. Again, keep in mind that this plot of V_{BE} is a slight fiction because we have neglected the small curvature caused by the weak temperature dependence of I_0. The correction is second-order, and we will take care of this little detail shortly.

FIGURE 5. V_{BE} *vs.* temperature



Recall that V_{BE} is nearly perfectly CTAT (i.e., it goes down almost linearly with temperature). Now suppose we add to this CTAT V_{BE} a voltage that is perfectly proportional to absolute temperature (PTAT). If we choose the slope of the PTAT term equal in magnitude to that of the CTAT term, the sum will be independent of temperature:

FIGURE 6. Illustration of bandgap reference principle



We see that something funny happens above about 600K, but the fact that the principle fails at temperatures high enough to melt lead is rarely a practical concern.

Note that the addition of a PTAT and CTAT voltage in the proper ratio yields an output equal to the bandgap voltage (extrapolated to 0K), independent of temperature. Stated another way, if we adjust the PTAT component to make the output voltage equal to V_{G0} at *any* temperature, the output voltage will equal V_{G0} at *all* temperatures, at least in this slightly simplified picture.

At this point, it's natural to consider how one obtains a PTAT voltage, since this whole concept relies on having one around. Let's start with the familiar equation for V_{BE}:

$$V_{BE} = V_T ln\left(\frac{I_C}{I_S}\right) \tag{5}$$

Using this expression, we can readily compute the *difference* in two base-emitter voltages for identical transistors operating at two different values of collector current (or, more generally, for transistors made in the same process, operating at two different values of collector current density):

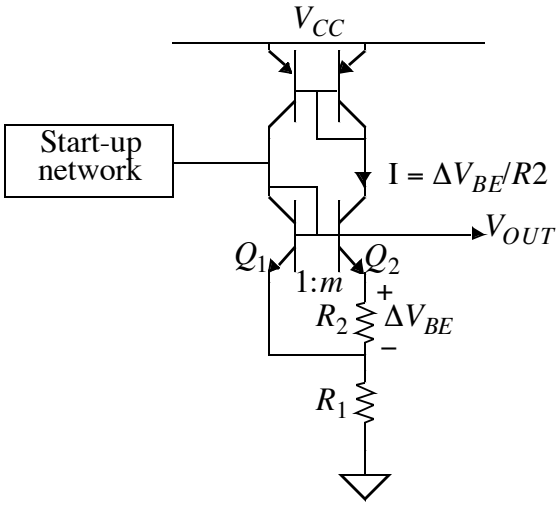
$$\Delta V_{BE} = V_{BE2} - V_{BE1} = V_T ln\left(\frac{J_{C2}}{J_{C1}}\right) \tag{6}$$

The misleading I_S term drops out, so we can conclude confidently that ΔV_{BE} truly is PTAT if the collector current densities are in a fixed ratio. Thus, while each V_{BE} is nearly CTAT, the *difference* between two V_{BE}'s is perfectly PTAT.

5.1 Classic Bandgap Reference

Now that we've got all the ingredients, all that remains is to sum the CTAT V_{BE} term with the right amount of PTAT ΔV_{BE}. While one could imagine a large number of methods for doing so, the Brokaw cell is a particularly elegant (and accurate) implementation of the bandgap reference. The classic bipolar implementation is shown in the following figure (again, basic mirrors are shown for simplicity's sake); we'll modify this circuit shortly for implementation in CMOS technology:

FIGURE 7. Classic Brokaw bandgap reference circuit



As we shall see, the output voltage is the sum of a PTAT voltage and a V_{BE}. Here, Q_1 and Q_2 operate at a fixed current density ratio of m (typically 8, because it lays out nicely) set, for example, by ratioing the effective emitter areas. Now, by KVL, the voltage across R_2 is

the difference in V_{BE}'s of Q_1 and Q_2, and is therefore PTAT and equal to $V_T \ln m$. Assuming that R_2's TC is negligibly small, the current through it will also be PTAT. Furthermore, the current through R_1 is simply twice that through R_2 since the two collector currents are equal.[7] Therefore, the voltage drop across the entire resistor string is purely PTAT. Finally, the output voltage is just this PTAT voltage plus the V_{BE} of Q_2, as advertised. With proper choice of R_1 and R_2, the output voltage will have zero TC. As a free bonus, a PTAT voltage is available at the emitters of Q_1 and Q_2, providing thermometer outputs.

Design Example:

To carry out a detailed design, we need some process-specific device data. As a particular example, suppose we go to the lab and find that $V_{BE} = 0.65\text{V}$ @ 300K and 100μA for a transistor of Q_2's size. Furthermore, let $m = 8$. This choice of m[8] sets ΔV_{BE} =53.8mV (a number comfortably larger than any offsets that we expect) @ 300K. Since we definitely know the value of V_{BE} at 100μA, a prudent choice for the collector currents would be this value of 100μA, and this choice then fixes the value of $R_2 = \Delta V_{BE}/100\mu\text{A} = 538\,\Omega$. Now, since we want the output voltage to be 1.2 volts, the drop across R_1 must be $1.2 - V_{BE} - \Delta V_{BE} = 0.496\text{V}$. Finally noting that the current through R_1 is twice that through R_2, we conclude that we should choose $R_1 = 0.496\text{V}/200\mu\text{A} = 2.48\text{k}\Omega$, completing the design.

You may have noticed that the collector currents in the Brokaw cell are not constant (in fact, they are PTAT if we assume that the resistors have zero TC). To see why this does not invalidate all we've done so far (in fact, it is beneficial), it is now time to take care of a few details, namely, those involving the temperature dependency of I_0.

A quasi-empirical expression for I_0 is

$$I_0 = A_e B T^r \tag{7}$$

where A_e is the emitter area, B is a process-dependent constant, T is the absolute temperature and r is a process-dependent quantity we'll call the curvature coefficient. For the relatively deep, diffused emitters of older bipolar processes, r typically has a value between 2 and 3, while for the shallow, implanted (and very heavily doped[9]) diffusions that are more common in modern CMOS and high-speed bipolar processes, r can range from 4 to 6. Your mileage may vary, so don't undertake a detailed design without first characterizing the junctions in your process.

With this equation for I_0, we can express V_{BE} as follows:

7. We are neglecting errors due to device mismatch, nonzero base currents and finite Early voltage.

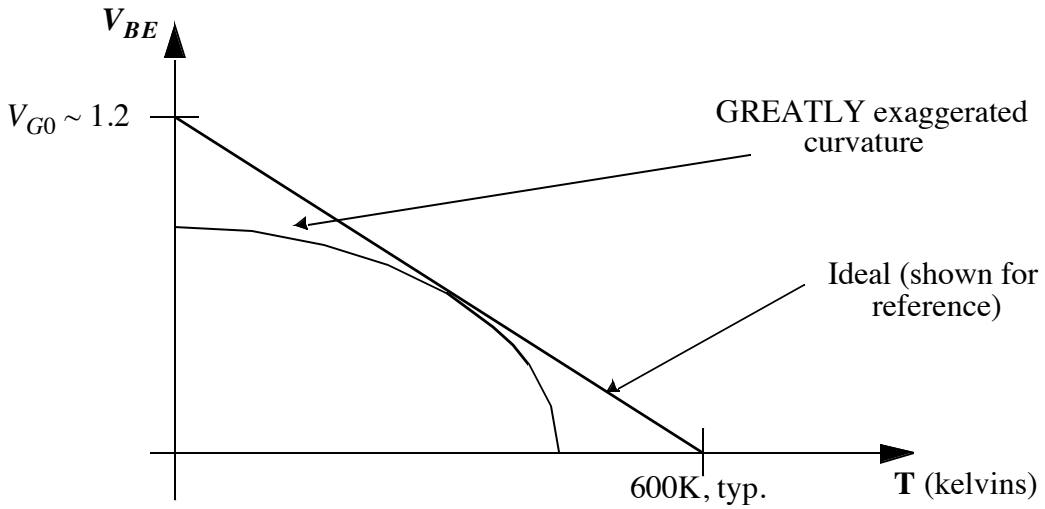
8. It is important that Q2 be laid out as eight instances of Q1 to guarantee that Q2 behaves as eight paralleled devices of Q1's size. If Q1 is placed at the center of a common-centroid arrangement, errors due to process variation will be minimized.

9. Bandgap narrowing and nonlinearity in the heavily doped emitters are probably responsible for the high values of r.

$$V_{BE} = V_{G0} - V_T ln\left(\frac{A_e B T^r}{I_C}\right) \tag{8}$$

Plotting as before, we can see why it is reasonable to call the parameter *r* the curvature coefficient (aside from the euphonious alliteration):

FIGURE 8. V_{BE} *vs.* temperature



Because the argument of the log is not quite independent of *T*, the temperature coefficient of V_{BE} is not quite constant, leading to a small departure from CTAT behavior for V_{BE}. Additionally, we've seen at least one implementation of a bandgap reference in which the collector current is also not constant. So, let's compute the actual TC that results if, in addition to the temperature dependence of I_0, we also consider a collector current that varies as the *n*th power of *T*:

$$\frac{dV_{BE}}{dT} = \frac{d}{dT}\left[V_T ln\left(\frac{CT^n}{A_e B T^r}\right)\right] = \frac{d}{dT}\left[V_T ln\left(\frac{C}{A_e B T^{r-n}}\right)\right] \tag{9}$$

so that

$$\frac{dV_{BE}}{dT} = \frac{k}{q}\left[ln\left(\frac{C}{A_e B T^{r-n}}\right) - (r-n)\right] \tag{10}$$

which we may re-write in a somewhat lower entropy form, as in Section2.0:

$$\frac{dV_{BE}}{dT} = -\frac{[V_{G0} - V_{BE} + (r-n)V_T]}{T} \tag{11}$$

Note that the curvature term disappears if $r = n$, and we're left with the same expression for the temperature coefficient as derived earlier. In the Brokaw cell, $n = 1$ to a good approximation (depending on the temperature coefficient of the resistors), which reduces the effect of, but does not cancel, r (remember, r is typically a minimum of 2, and can range up to about 6). Graphically, think of the increasing collector current with temperature as straightening out the V_{BE} curve.

The next question is, how does the curvature term affect the bandgap reference itself? The most expedient answer comes from deriving the condition for net zero TC. Suppose we call GV_T the PTAT component that we add to V_{BE}, where G is a constant to be found. Then, the TC of the PTAT component may be written as GV_T/T and the condition for zero TC is therefore

$$\frac{dV_{BE}}{dT} + \frac{GV_T}{T} = 0 \rightarrow G = \frac{[V_{G0} - V_{BE} + (r-n)V_T]}{V_T} \tag{12}$$

which corresponds to an output voltage of

$$V_{OUT}\big|_{TC=0} = V_{BE} + GV_T = V_{G0} + (r-n)V_T \tag{13}$$

This last equation depends on V_T and therefore implies that the output voltage cannot have zero TC at all temperatures; the best we can do is achieve zero TC at one temperature. Furthermore, to achieve this zero TC condition at that one temperature, we need to adjust the output to a voltage *higher* than V_{G0} by an amount equal to $(r - n)V_T$. Fortunately, this correction term is relatively small, typically amounting to just tens of mV out of a total that is greater than a volt. Hence, the output only has to be trimmed to a value a few percent greater than V_{G0} at the temperature where zero TC is desired (generally the center of the operating temperature range).

At this point, we'd like to quantify the errors that are caused by the curvature. Unfortunately, while the equations we've developed so far are valuable for design, they aren't quite suitable for analysis.To derive one that is, let us choose the factor m so that the output voltage has zero TC at some temperature we'll call T_R (for the reference temperature). Throughout, we'll use the subscript R to denote a variable's value at this reference temperature. With this notational convention, we may express V_{OUT} as follows:

$$V_{OUT}(T) = V_{G0} + \frac{T}{T_R}(r-n)V_{TR} - \frac{T}{T_R}(r-n)V_{TR}ln\left(\frac{T}{T_R}\right) \tag{14}$$

or, as some prefer:

$$V_{OUT}(T) = V_{G0} + \frac{T}{T_R}(r-n)V_{TR}\left[1 - ln\left(\frac{T}{T_R}\right)\right] \tag{15}$$

Note that this equation has the right limiting behavior: when $T = T_R$, it yields the output voltage corresponding to the zero TC condition. Also note that, if we were able to arrange

for the collector currents to vary as T^n with $n = r$, the output voltage would have zero TC at all temperatures if V_{OUT} were adjusted to a value V_{G0} at any temperature. This last observation is at the core of many efforts to synthesize curvature-corrected bandgap references.

Even without elaborate curvature correction methods, though, the Brokaw cell (where n =1 in the classic implementation), provides outstanding performance, because the curvature inherent in bipolars is simply not all that bad, and the Brokaw cell contributes little error of its own.

To illustrate this point, let's compute the actual error one could expect over a temperature range of –55 to +150°C, if T_R is chosen as +50°C, and if the quantity $(r - n)$ ranges from 1 to 5.

TABLE 1. Ideal output voltage as function of T and $(r - n)$

$r - n$	V_{OUT} @ T = –55°C	V_{OUT} @ T = 50°C	V_{OUT} @ T = 150°C	Max. Error
1	1.226	1.228	1.227	2mV
2	1.252	1.256	1.253	4mV
3	1.279	1.284	1.280	5mV
4	1.305	1.312	1.307	7mV
5	1.331	1.339	1.333	8mV

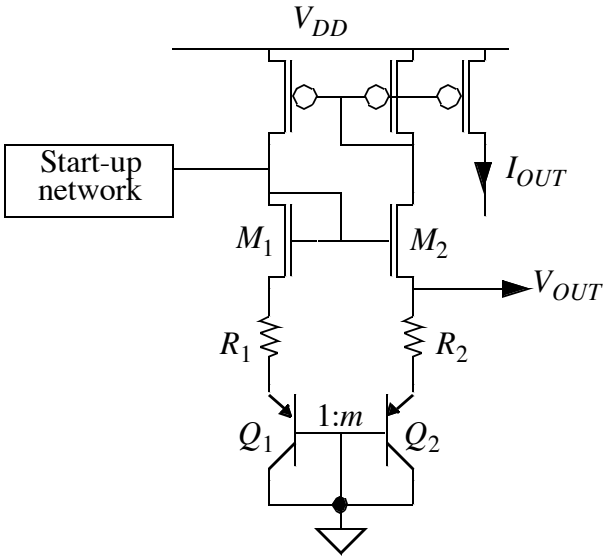
As is evident, the total change in output voltage is ideally less than a percent over the entire temperature range, even with relatively large values of $(r - n)$. Furthermore, the output is a maximum at the reference temperature, and drops off above and below this temperature in a quasi-parabolic manner. As a consequence, setting T_R equal to the center of the desired operating temperature range nearly minimizes the maximum deviation from the value at T_R.

As a final note, the levels of performance in Table1 assume an ideal scenario in which second-order errors due to device mismatch, nonzero contact and interconnect resistance, nonzero resistor TC, β drift, etc., are ignored. Actual performance will be worse in practice owing to the combined effect of these sources. Careful layout of all devices is mandatory to minimize errors, but even so, there can be a considerable spread in output voltages (e.g., 50-100mV) for CMOS bandgap implementations.

5.2 Bandgap References in CMOS Technology

The classic Brokaw cell uses bipolar transistors in which all device terminals float, so it cannot be implemented directly in this form in CMOS technology. Re-arranging the circuit to accommodate the restrictions placed on the parasitic substrate pnp yields the following:

FIGURE 9. CMOS bandgap reference (simplified)



Transistor Q_2 is designed to have m times the emitter area of Q_1. The quad of CMOS transistors enforces equal emitter currents, so that the *collector* current density ratio is only approximately m. Implicit in the last statement is that this circuit has a greater sensitivity to β than the original Brokaw cell. This unfortunate consequence of being forced to use the substrate pnp's leads to larger errors than the classic bandgap cell, particularly because β is rarely large enough to be ignored (values of 5-10 are typical, and values of unity are not unheard of). Nevertheless, even a poorly performing bandgap reference is considerably superior to anything that can be built out of pure CMOS components.

Choosing component values for this circuit proceeds in a manner quite similar to that for the classic cell. Begin by specifying a reference temperature T_R at which the TC is to be zero. For illustrative purposes, assume that this temperature is to be 350 kelvins.

The next step is to calculate the target output voltage at this reference temperature. As mentioned previously, the shallow, heavily-doped p+ diffusions used to make the emitters lead to relatively large curvature coefficients, with r typically 4 or 5. If no device data or models are available, a reasonable starting point is to assume a value of 3 for the quantity $(r - n)$. Hence, the target output voltage should be:

$$V_{OUT} = V_{G0} + (r-n)V_T \approx 1.3V \tag{16}$$

Now assume that we have selected 100μA for the individual emitter currents, and that the larger transistor, Q_2, has a V_{BE} of 0.65V at this current at T_R. Then $R2$ is simply:

$$R2 = \frac{V_{OUT} - V_{BE2}}{I_E} = 6.5k\Omega \tag{17}$$

Assuming an m equal to 8, then V_{BE1} is about 63mV larger than V_{BE2} at the reference temperature. Hence,

$$R1 = \frac{V_{OUT} - V_{BE1}}{I_E} = 5.87k\Omega \tag{18}$$

thus completing the design.

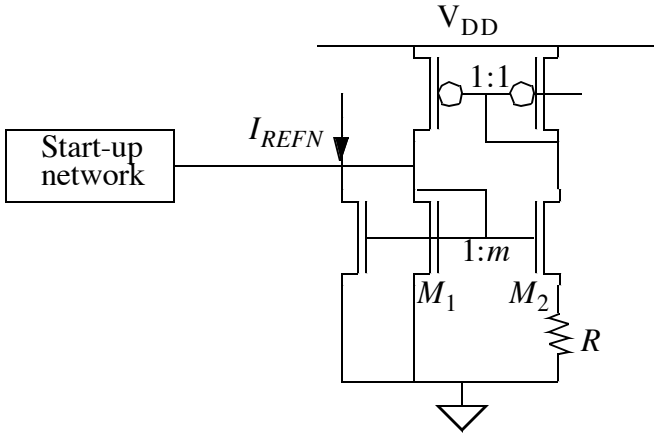
As a final comment on this circuit, one usually finds that the bias current is relatively constant with temperature because resistors typically have a positive TC which offsets the PTAT tendency of the core design. Thus, currents from a mirror slaved to the PMOS mirror may be roughly constant. The precise TC obtained may be adjusted through a suitable choice of resistor type and values if the ultimate goal is to generate a bias *current* rather than a reference voltage.

6.0 Constant-g_m Bias

While a constant current or constant voltage is often desirable, there are important examples in which it is the *transconductance* that must be held constant. In those cases, the bias current must be allowed to vary with temperature (and process) in a way that enforces that constancy.

A circuit whose bias current corresponds to a g_m that is inversely proportional to a reference *resistance* is a modification of the self-biased CMOS quad of transistors we've already seen (again, a crude PMOS mirror is shown for simplicity; better mirrors would generally be used in practice):

FIGURE 10. Basic constant g_m reference



Here transistor M_2 is a factor m times wider than M_1, so its V_{GS} is the smaller of the two. Because the voltage across R equals the difference in gate-source voltages, we may write:

$$I_2 = \frac{\Delta V_{GS}}{R} = \frac{\Delta V_{OD}}{R} = I_1 = I, \tag{19}$$

where we have neglected body effect. Thus, the two threshold voltages are equal, allowing us to say that the difference in gate-source voltages equals the difference in overdrive voltages.

Now recall that the transconductance of a long-channel MOSFET may be expressed as

$$g_m = \frac{2I}{V_{OD}}. \tag{20}$$

The transconductance of M_1 is therefore

$$g_{m1} = \frac{2I}{V_{OD1}} = \frac{2\Delta V_{OD}}{RV_{OD1}} = \frac{2}{R}\left(1 - \frac{V_{OD2}}{V_{OD1}}\right). \tag{21}$$

The ratio of overdrive voltages of two long-channel devices operated at equal currents, but differing widths is just:

$$\frac{V_{OD2}}{V_{OD1}} = \sqrt{\frac{W_1}{W_2}} = \frac{1}{\sqrt{m}}. \tag{22}$$

Therefore,

$$g_{m1} = \frac{2}{R}\left(1 - \frac{1}{\sqrt{m}}\right). \tag{23}$$

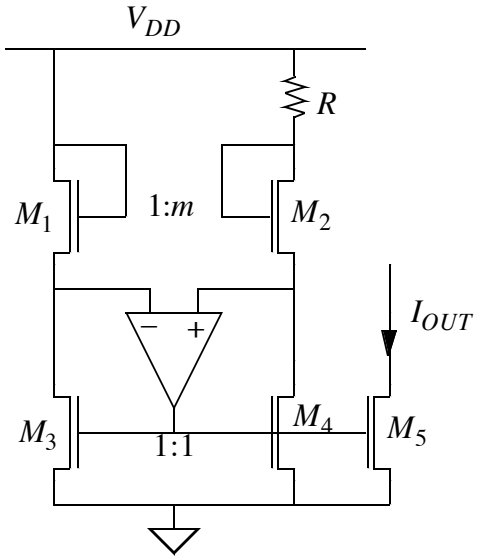
Note that, miraculously, the transconductance of M_1 depends only on a resistance and a width ratio; all process parameters have magically disappeared. As long as the resistor's parameters are more stable than those of the transistors, this circuit provides a net advantage over other methods of setting transconductance.[10]

For the special case of $m = 4$, the transconductance of M_1 becomes precisely equal to $1/R$. For this reason, this particular width ratio is frequently used.

A potentially significant source of error in implementations of this circuit is the body effect, since the two transistors are not operated at equal source-bulk potentials. The resulting difference in threshold voltages introduces a device-dependent term into the expression for transconductance. In *n*-well technologies, this error term can be eliminated for PMOS transistors by connecting the well of each transistor to its source. To take care of this problem for the NMOS transistors, one may employ the following modification:

10. If on-chip resistor options are unsatisfactory, one may always employ an external resistor with superior characteristics.

FIGURE 11. Modification of constant g_m reference to eliminate error due to body effect



Here, as before, M_1 and M_2 operate at equal drain currents. And, as before, the difference in their gate-source voltages appears across a resistor R, because the op-amp forces equal source voltages of M_1 and M_2. Because the same KVL equation applies to this M_1-M_2-R loop as to that of the original circuit, all of the equations for the preceding case apply to this one. What's different is that M_1 and M_2 now operate at equal source-bulk voltages, preventing body effect from causing an error. Finally, equal-sized M_1 and M_3 operate at the same gate *overdrive* because they operate at the same current. They therefore possess the same transconductance. Mirroring via M_5 thus enables delivery of the magic current to other NMOS devices to set their transconductances.

7.0 Summary

We've seen that the self-biased cell is quite versatile, permitting the generation of currents proportional to the ratio of a voltage in one branch to the resistance in the other. The voltage may be provided by a variety of elements, such as a forward-biased junction. While a V_{BE} by itself has limited utility as a voltage reference because of its negative TC, its CTAT behavior is valuable in compensating the PTAT ΔV_{BE} in a bandgap reference circuit to yield an output roughly equal to V_{G0} with extremely small temperature variation. Even when parasitic bipolars are used in an otherwise CMOS circuit, the bandgap principle allows the synthesis of more accurate and stable voltages or currents than possible with ordinary CMOS circuits.

Finally, constant-g_m bias circuits were presented, allowing the stable biasing of transconductance-sensitive circuits, such as some types of active filters and amplifiers.

