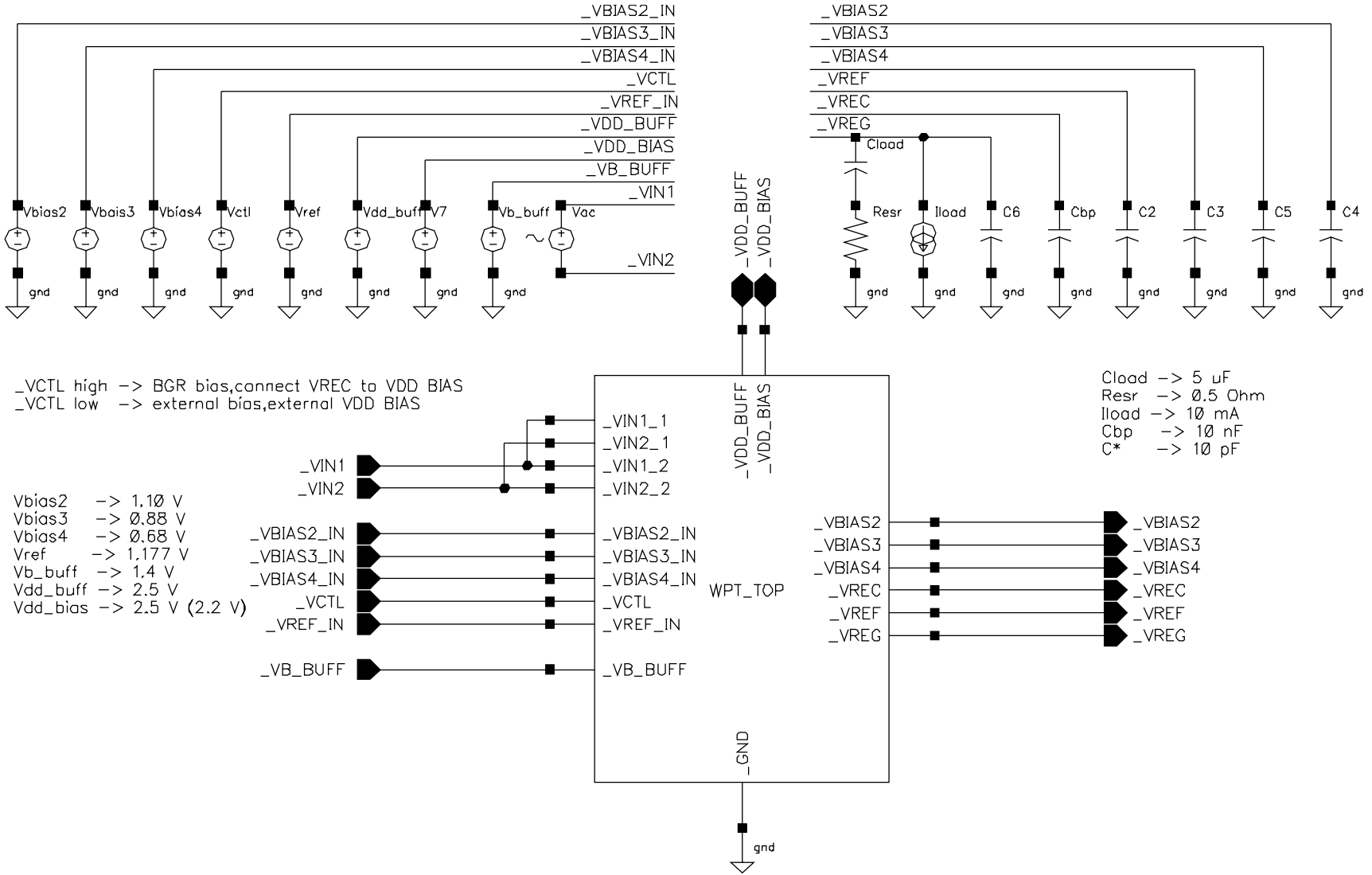
_VBIAS2_IN
_VBIAS3_IN
_VBIAS4_IN
_VCTL
_VREF_IN
_VDD_BUFF
_VDD_BIAS
_VB_BUFF
_VIN1
_VIN2
Vbias2
Vbais3
Vbias4
Vctl
Vref
Vdd_buff
V7
Vb_buff
Vac
gnd
_VBIAS2
_VBIAS3
_VBIAS4
_VREF
_VREC
_VREG
Cload
Resr
Iload
C6
Cbp
C2
C3
C5
C4
_VCTL high -> BGR bias,connect VREC to VDD BIAS
_VCTL low -> external bias,external VDD BIAS
Vbias2 -> 1.1Ø V
Vbias3 -> Ø.88 V
Vbias4 -> Ø.68 V
Vref -> 1.177 V
Vb_buff -> 1.4 V
Vdd_buff -> 2.5 V
Vdd_bias -> 2.5 V (2.2 V)
Cload -> 5 uF
Resr -> Ø.5 Ohm
Iload -> 1Ø mA
Cbp -> 1Ø nF
C* -> 1Ø pF
_VIN1_1
_VIN2_1
_VIN1_2
_VIN2_2
WPT_TOP
_GND