

A REVIEW PAPER ON DESIGN AND SYNTHESIS OF TWO-STAGE CMOS OP-AMP

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ABSTRACT

This paper presents a well defined method for the design of a two-stage CMOS operational amplifier. The OPAMP which has been designed is two stage CMOS OPAMP followed by an output buffer. The op-amp which has been designed, exhibits a unity gain frequency of 14MHz and a gain of 77.25dB with 85.85° phase margin. A new technique which takes into account the effect of transfer function zeros, which are traditionally neglected, has been proposed. The simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage. The compensation method results in higher unity gain bandwidth under the same load condition. Both the theoretical calculations and computer aided simulation analysis have been given in detail. Design has been carried out in Mentor graphics tool. Simulation results have been verified using Model Sim Eldo and Design Architect IC. The simulation results in a tsmc 0.35um CMOS process from a 5V voltage supply demonstrate the designed has a gain 77.25dB.

KEYWORDS: Analog Circuit, 2 stage CMOS Operational amplifier, Stability, GBW, Frequency Compensation.

I. INTRODUCTION

Over the last few years, the electronics industry has exploded. Operational amplifiers are key elements in analog processing systems. Operational amplifiers are an integral part of many analog and mixed-signal systems. As the demand for mixed mode integrated circuits increases, the design of analog circuits such as operational amplifiers (op-amps) in CMOS technology becomes more critical [1]. Operational amplifiers (op-amps) with moderate DC gains, high output swings and reasonable open loop gain band width product (GBW) are usually implemented with two-stage structures [2]. The aim of the design methodology in this paper is to propose straightforward yet accurate equations for the design of high-gain 2 staged CMOS op-amp. To do this, a simple open-loop analysis with some meaningful parameters (phase margin, gain-bandwidth, *etc.*) is performed. The method handles a very wide variety of specifications and constraints. In this paper, we formulate the CMOS op-amp design problem as a very special type of optimization problem called a compensation method. The most important feature of compensation is that they can increase phase margin [3]. So frequency compensation technique is used. Without frequency compensation, this op-amp is not stable in closed-loop applications. A number of frequency compensation techniques are proposed to stabilize a closed-loop two-stage amplifier [4-5]. The realization of a CMOS Op-amp that combines a considerable dc gain with high unity gain frequency has been a difficult problem [6].

CMOS Op-amp can be used efficiently for practical consequences for example designing of a switched capacitor filter, analog to digital converter etc. In this case the designs of the individual op-amp are combined with feedback and by various parameters that affect the amplifier such as input capacitance, output resistance, etc [7]. The method we present can be applied to a wide variety of amplifier architectures, but in this paper we apply the method to a specific two stage CMOS op-amp. The simulation results have been obtained by tsmc 0.35 micron CMOS technology. Design has been carried out in Mentor Graphics tool. Simulation results are verified using Model Sim Eldo and Design Architect IC.

Outline of paper

This paper is organized as follows. Section II presents the 2 stage amplifier. Section III reviews the 2 stage CMOS Op-amp schematic design with compensation capacitor. Its specifications are briefly clarified, also gives the formula or calculation for designing of 2 stage CMOS Op-amp. Section IV presents the simulation results of the proposed op-amp and finally in Section V give my concluding remarks.

II. THE TWO-STAGE AMPLIFIER

MOS Op-Amps are ubiquitous integral parts in various analog and mixed- signal circuits and systems. Operational Amplifiers are the amplifiers that have sufficiently high forward gain so that when negative feed back is applied, the closed loop transfer function is practically independent of the gain of the op-amp [8-9]. This principle has been exploited to develop many useful analog circuits and systems. The primary requirement of an op-amp is to have an open loop gain that is sufficiently large to implement the negative feedback concept [10].

The specific two-stage CMOS op-amp we consider is shown in Figure 1. The circuit consists of an input differential trans-conductance stage forms the input of the op-amp followed by common-source second stage. The common source second stage increases the DC gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. This is important in reducing the power consumption [11-12]. If the Op-Amp must drive a low resistance load the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing [13-14]. Bias circuit is provided to establish the operating point for each transistor in its quiescent stage. Compensation is required to achieve stable closed loop performance [15-16]. However, due to an unintentional feed forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. Such a zero, however, can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor [17].

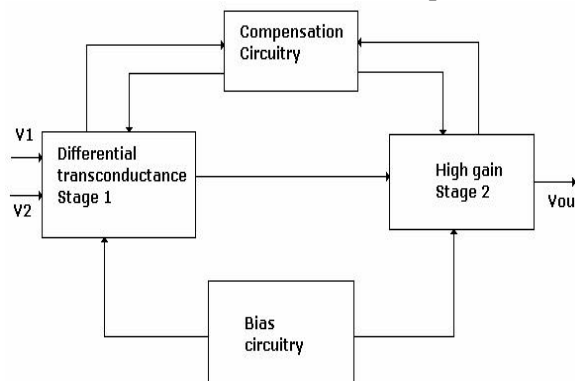


Figure 1: A general two stage CMOS Op-amp

In designing an op-amp, numerous electrical characteristics, e.g., gain-band width, slew rate, common-mode range, output swing, offset, all have to be taken into consideration [18]. Furthermore, since op-amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. The simplest frequency compensation technique employs the Miller effect by connecting a compensation capacitor across the high-gain stage [19].

This op-amp architecture has many advantages: high open-loop voltage gain, rail-to-rail output swing, large common-mode input range, only one frequency compensation capacitor, and a small number of transistors. This op-amp is a widely used general purpose op-amp; it finds applications for example in switched capacitor filters, analog to digital converters, and sensing circuits [20].

Table 1: Comparison of Performance of Various Op-amp Topologies

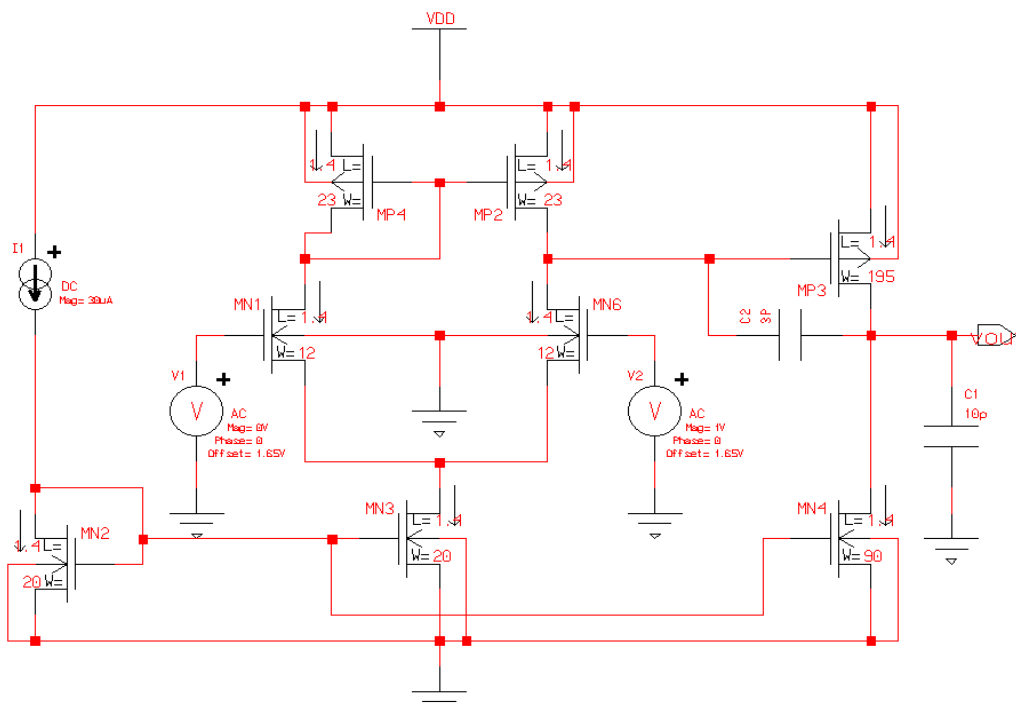
	Gain	Speed	Output Swing	Noise	Power Consumption
Telescopic					
Folded-Cascode					
Multi-Stage					
Gain-Boosted					
	LOWEST	LOW	MEDIUM	HIGH	HIGHEST

As seen from Table I, the telescopic and multi-stage topologies seem to be more suitable for the design. If pure telescopic, it will suffer from low output swing and medium gain despite meeting the custom design specifications yet [21]. While as for the multi-stage topology, especially more than two stages, the stability problem will become severe for us. In order to obtain a high enough gain, two fully differential auxiliary operational amplifiers act like a booster [22]. Hence, we'll depict the two-stage topology method for the amplifier design in this paper.

It consists of a cascade of $V \rightarrow I$ and $I \rightarrow V$ stages and the first stage consists of differential amplifier converting the differential input voltage to differential currents. These differential currents applied to a current-mirror load recovering the differential voltage. The second stage consists of a common source MOSFET converting the second stage input voltage to current. This transistor is loaded by a current sink load, which converts the current to voltage at the output. The second stage is also nothing more than the current sink inverter. This two stage Op Amp is widely used that we will call it the classical two stage Op-amp [23-24].

III. TWO STAGE CMOS OP-AMP SCHEMATIC DESIGN

The Op-Amp DC gain must be greater than 60 dB; settle to 0.1% accuracy is less Figure 2. Schematic of an unbuffered, two-stage CMOS op amp with an n-channel input pair

**Figure 2:** Topology chosen for this Op-Amp.

Fundamental Implications

Table 2: Custom Design Specifications of the amplifier

Specification Names	Values
Supply VDD	VDD=5V
Gain	>= 70dB
Gain Bandwidth	10MHz
Settling Time	1μs
Slew Rate	10V/ μs
Input common Mode Range	1.5 – 2.8V
Common mode rejection ratio	>=60dB
Output Swing	1 – 2.8V
Offset	<=10m

3.1 Design Methodology of Op-amp

3.1.1 Determine the necessary open-loop gain (Ao)

$$g_{m1} = g_{m2} = g_{mI}, g_{m6} = g_{mII}, g_{ds2} + g_{ds4} = G_I, \text{ and } g_{ds6} + g_{ds7} = G_{II}$$

$$Id = \frac{\mu_{n,p} Cox \left(\frac{W}{L}\right) V_{eff2}}{2} \quad (1)$$

$$g_m = \sqrt{2\mu_{n,p} Cox \frac{W}{L} Id} \quad (2)$$

$$g_m = 2 \frac{Id}{V_{eff}} \quad (3)$$

$$\text{Slew rate } SR = \frac{I_5}{C_C} \quad (4)$$

$$\text{First stage gain } A_{v1} = \frac{-g_{m1}}{g_{ds2} + g_{ds4}} = \frac{-2g_{m1}}{I_5 (\lambda_2 + \lambda_4)} \quad (5)$$

$$\text{Second stage gain } A_{v2} = \frac{-g_{m6}}{g_{ds6} + g_{ds7}} = \frac{-g_{m6}}{I_6 (\lambda_6 + \lambda_7)} \quad (6)$$

$$\text{Gain Bandwidth } GB = \frac{g_{m1}}{C_C} \quad (7)$$

$$\text{Output pole } p_2 = \frac{-g_{m6}}{C_L} \quad (8)$$

$$\text{RHP zero } Z_1 = \frac{g_{m6}}{C_C} \quad (9)$$

$$\text{Positive CMR } V_{in}(\max) = V_{DD} - \sqrt{\frac{I_5}{\beta_3}} - |V_{TO3}|(\max) + V_{T1}(\min) \quad (10)$$

$$\text{Negative CMR } V_{in}(\min) = V_{SS} + \sqrt{\frac{I_5}{\beta_1}} + V_{T1}(\max) + V_{DS5}(\text{sat}) \quad (11)$$

$$\text{Saturation voltage } V_{DS}(\text{sat}) = \sqrt{\frac{2I_{DS}}{\beta}} \quad (12)$$

It is assumed that all transistors are in saturation for the above relationships.

3.2 Design Parameters

Model N NMOS Level = 53 +Version = 3.1 $T_{NOM} = 27$

$T_{OX} = 7.8E-9$ $N_{CH} = 2.2E17$ $V_{OFF} = -0.0888645$ $V_{SAT} = 1.583891E5$

$V_{THO} = 0.5490813$

Model P NMOS Level = 53 +Version = 3.1 $T_{NOM} = 27$

$T_{OX} = 7.8E-9$ $N_{CH} = 8.6E16$ $V_{OFF} = -0.1265542$ $V_{SAT} = 1.789066E5$

IV. SIMULATION RESULTS

4.1 AC Analysis

In AC- Analysis we determine Phase margin, Gain and GB of the OP-Amp. Both Gain and Phase margin are calculated using DC operating point and AC analysis. The values given to implement AC-Analysis are

- Start frequency = 1Hz
- Stop frequency = 10 MHz

Output:

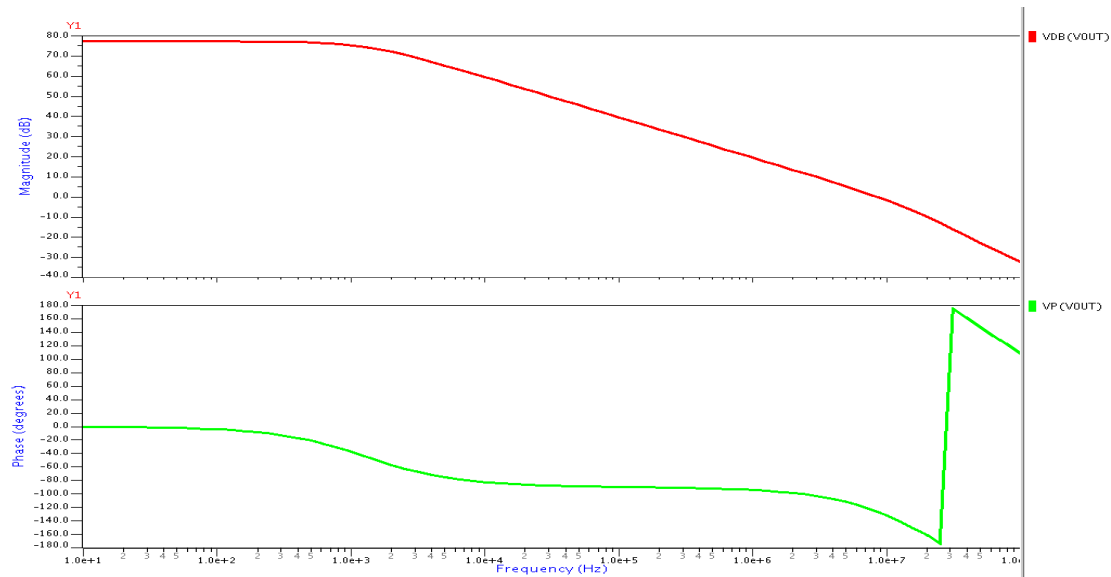


Figure 3: Output of AC Analysis

The output results of AC Analysis is as follows

Gain = 77.24 dB

$\omega_{-3db} = 1.3 \text{ KHz}$

$\omega_{UGB} = 8.6 \text{ MHz}$

Phase margin = 53.46° .

CMRR= 80.985 dB

4.2 To Improve Phase Margin:

To Improve phase margin we use Nulling Resistor. The Setup for improved phase margin is

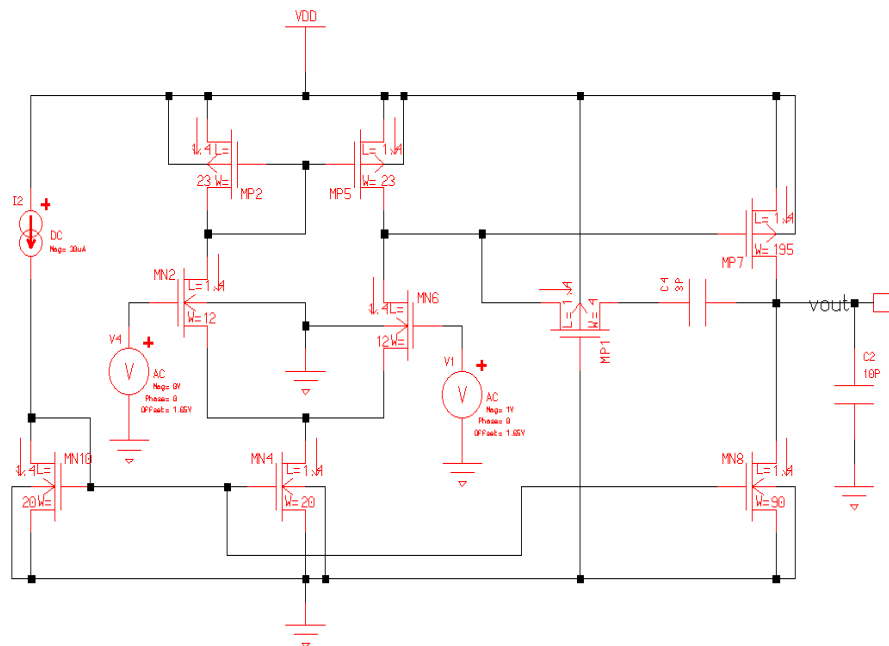


Figure 4: Setup for improved phase margin

Output:

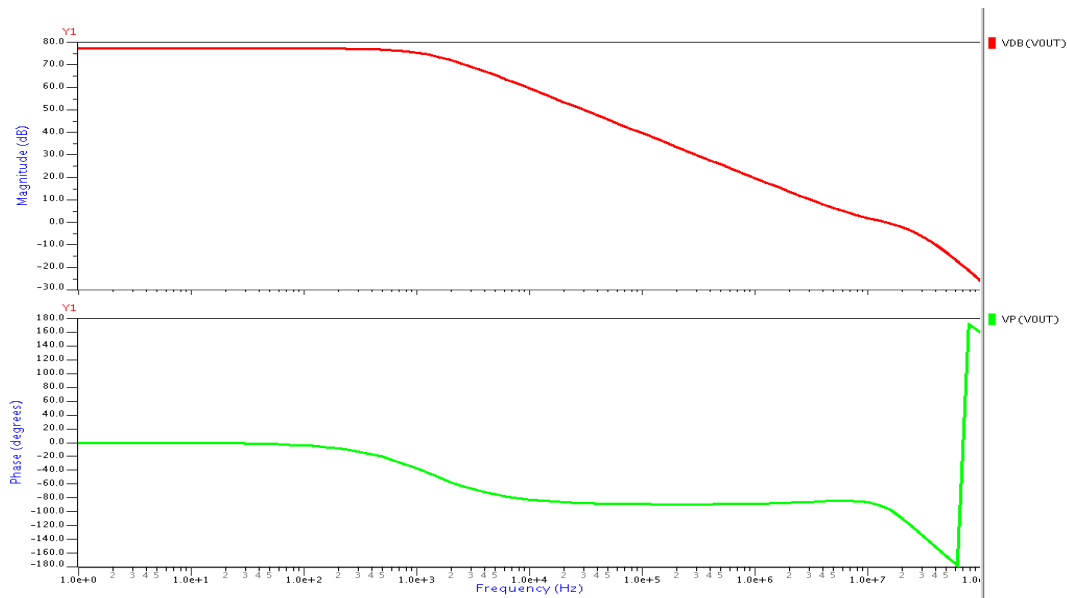


Figure 5: Result of AC Analysis

The output results of AC Analysis is as follows

Gain = 77.249 dB

$\omega_{-3dB} = 1.3 \text{ KHz}$

Phase margin = 85.85°

$\omega_{UGB} = 14.1 \text{ MHz}$

CMRR:

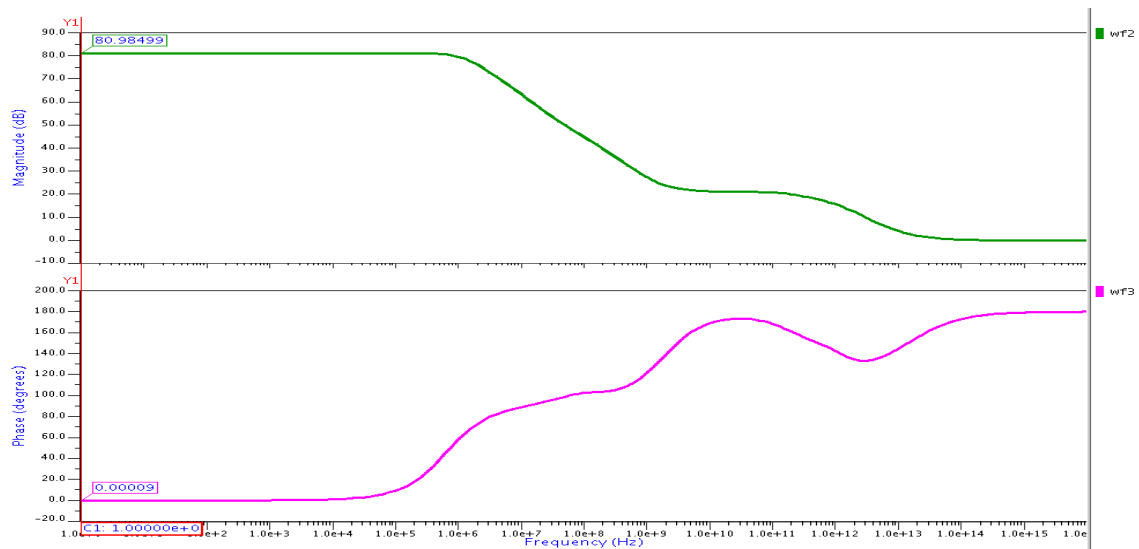


Figure 6: Result of CMRR

CMRR = 80.985 dB

4.3 Transient Analysis

The non inverting terminal is connected to a pulse with a rise and fall time equal to 1n sec (0.1us) and a pulse width of 384.61us. The value of pulse period is 769.23us. This analysis helps to determine the slew rate of the op-amp.

Slew rate is calculated using the transient analysis. Slew rate is the change of output voltage with respect to time. Typically slew rate is expressed in V/ μ s. Ideal value of Slew rate is infinite. The slew rate achieved in this design is 10.32V/ μ s.

Slew Rate:

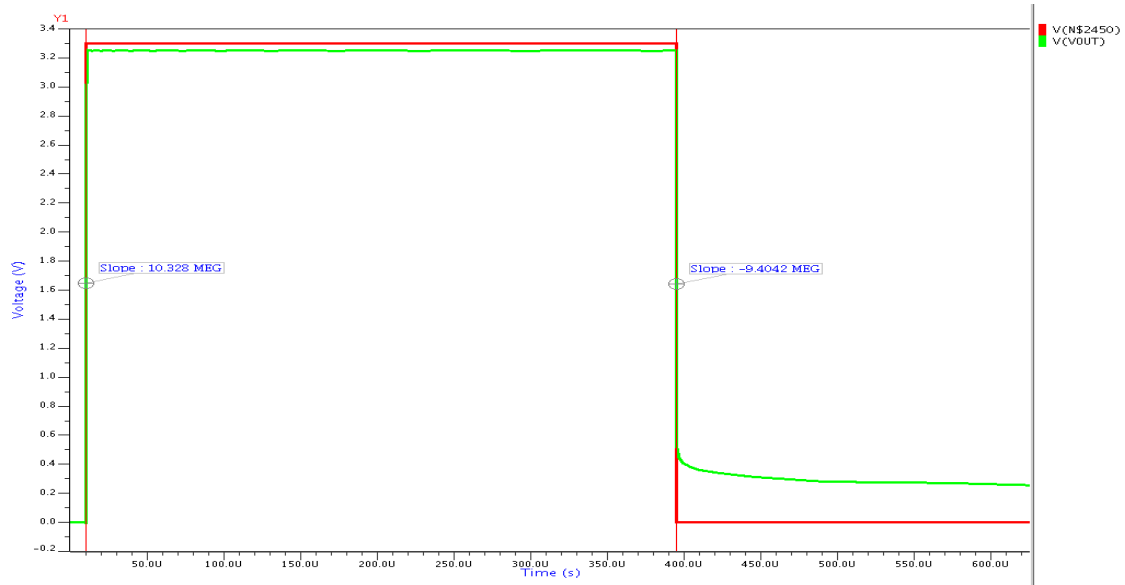


Figure 7: Output of Transient Analysis

The slew-rate of an op-amp is defined as the maximum rate of change of the output Voltage for all possible input signals [25].

$$SR = \frac{\max(|dV_{out}(t)|)}{dt}$$

Here $dV_{out}(t)$ is the output produced by the amplifier as a function of time t . Slew rate is typically expressed in units of V/ μ s.

Typically for high-bandwidth op-amps, the slew rate scales with the band width. Therefore, the fraction of the settling time spent in the slew limited regime is small [26]. Because this is a two-stage amplifier, there are two different slew rates. The lesser of the two will limit the overall rate of voltage of change at the output. C_{out} is the total parasitic and external capacitance at the output. The source of M_2 , however, will only remain a virtual ground if M_1 can supply sufficient charge to C_c to support the voltage change across C_c during a change in voltage at the output. Otherwise, this node will move and potentially cause M_4 to leave saturation or M_2 to cutoff. Therefore,

$$SR = \frac{I_5}{C_c}$$

ICMR:

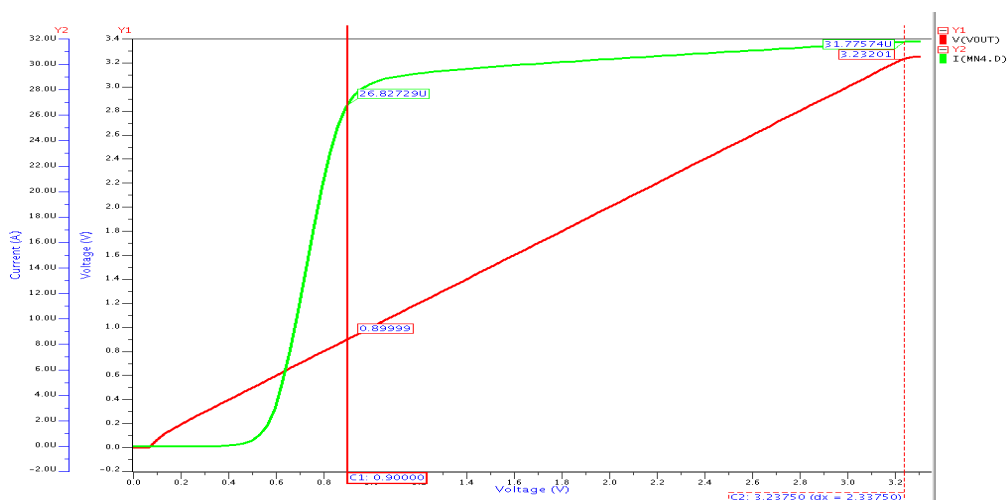


Figure 8: Result of ICMR

This is simply the range of voltage that you can send to the input terminals while ensuring that the op amp behaves as you expect it to. If we exceed the input voltage range, the amplifier could do some unexpected things [27].

This is the voltage range that we can use at input terminal without producing a significant degradation in op-amp performance. Since the typical input stage of an op-amp is a differential pair, the voltage required for the proper operation of the current source and the input transistors limit the input swing. A large input common mode range is important when the op-amp is used in the unity gain configuration. In this case the input must follow the output [28].

Output Swing:

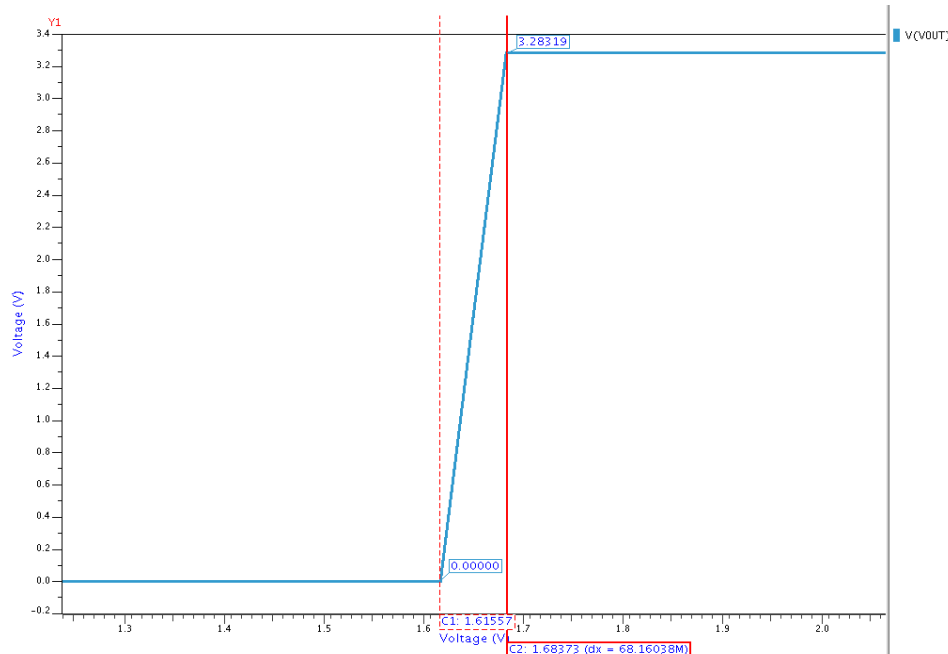


Figure 9: Output Swing

This is the maximum swing of the output node without producing a significant degradation of op-amp performance [29]. Since we have to leave some room for the operation of the devices connected between the output node and the supply nodes, the output swing is only a fraction of (VDD-VSS). Typically it ranges between 60% and 80% of (VDD-VSS). Within the output swing range the response of the op-amp should conform to given specifications and in particular the harmonic distortion should remain below the required level [30].

Positive Slew Rate = 10.328V /us

Settling Time = 0.4 us

Negative Slew Rate = 9.40V/us

ICMR = 0.9 – 3.237 V

Output Swing = 0.0 - 3.28V

V. RELATED WORK

Comparison for CMRR: Figure 10 shows the designing of Op-amp using 4 topologies. The Op-amp has been implemented in a standard 0.8 μm CMOS process. It consumes a total power of 4.8 mW at a 3.3V supply [31]. Out of which CMRR of the 2 stage CMOS op-amp is best. This designing was on 0.8 μm technology. In this paper technology has been reduced and a 2 stage CMOS Op-amp with tsmc 0.35 μm has been designed by which the Gain and CMRR have been increased.

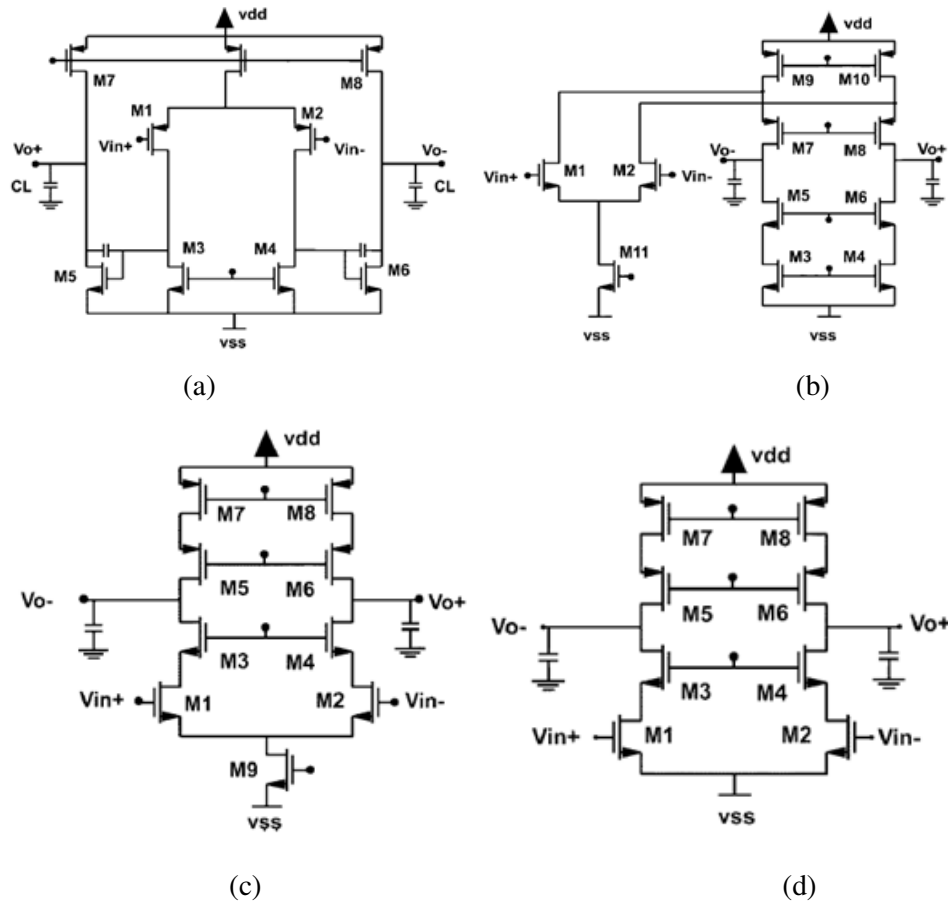


Figure: 10 (a) Two Stage Amplifier, (b) Folded Cascode Amplifier, (c) Telescopic Amplifier, (d) No Tail Telescopic Amplifier

Result of CMRR:

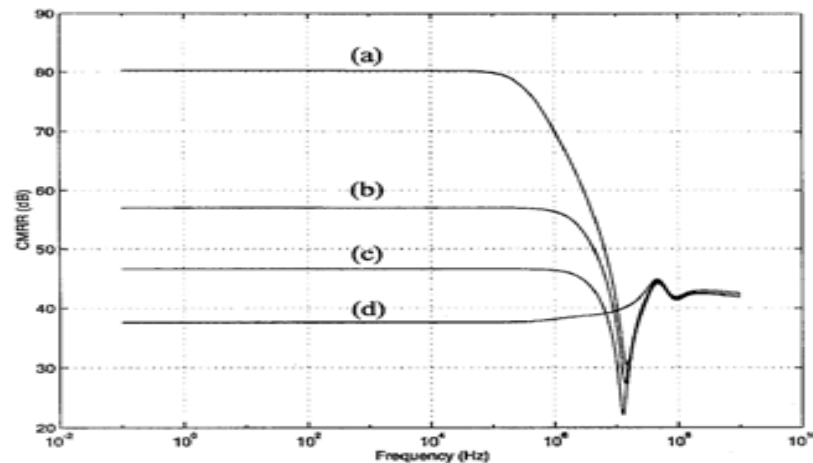


Figure 11: Result of CMRR for Various types of Op-amp

Comparison for Gain: Earlier, a Telescopic OTA Architecture was used, in which a differential pair is used to sense the input voltage difference. If the pair is operating in saturation, when one transistor is turned on, the other will turn off. The current through one leg will be sourced to the output while the other leg will sink current from the load [32].

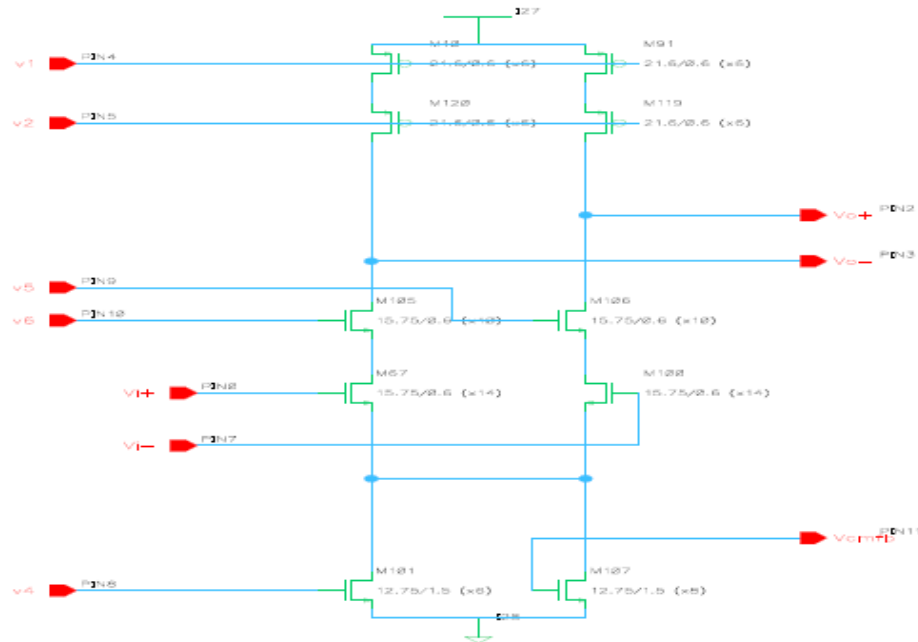


Figure 12: Schematic Design for telescopic OTA Architecture

The AC analysis shows the Gain of this Op-amp which is 67 db, but in this paper a 2 stage CMOS Op-amp has been designed by which the Gain is increased to 77.249 dB.

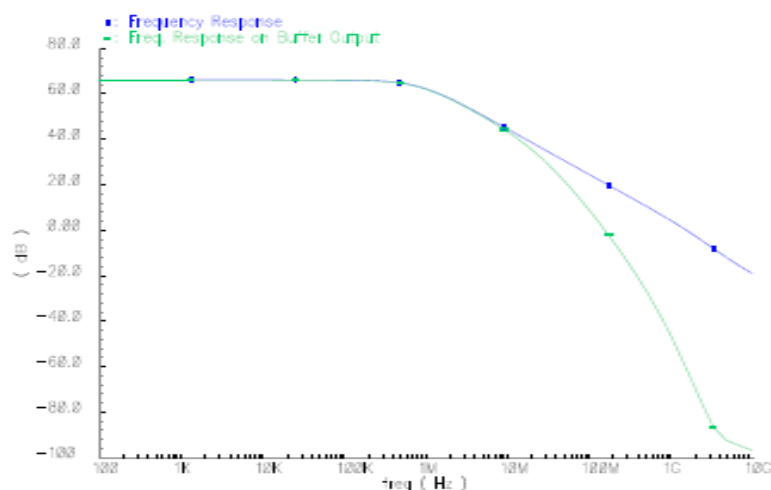


Figure 13: Result of ac analysis for telescopic OTA Architecture

VI. CONCLUSION

We have proposed a 2 stage CMOS op-amp and analyzed its behavior. Simulation results confirm that the proposed design procedure can be utilized to design op-amps that meet all the required specifications. Design techniques for this op-amp were also given. The proposed methodology is relatively accurate because compensation technique to take into account the effect of right half plane zero which is traditionally neglected is employed. Simulations confirm that the settling time can be further improved by increasing the value of GBW , the settling time is achieved 0.4us, gain is 77.25dB and a value of phase margin is 85.85° .

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