

UiO : Department of Physics
University of Oslo

Wireless Power Receiving Unit

*Analysis, design and implementation of inductive power receiving
unit for wireless circuits*

**Master Thesis Presentation
Electronics and Computer Technology
(Microelectronics)**

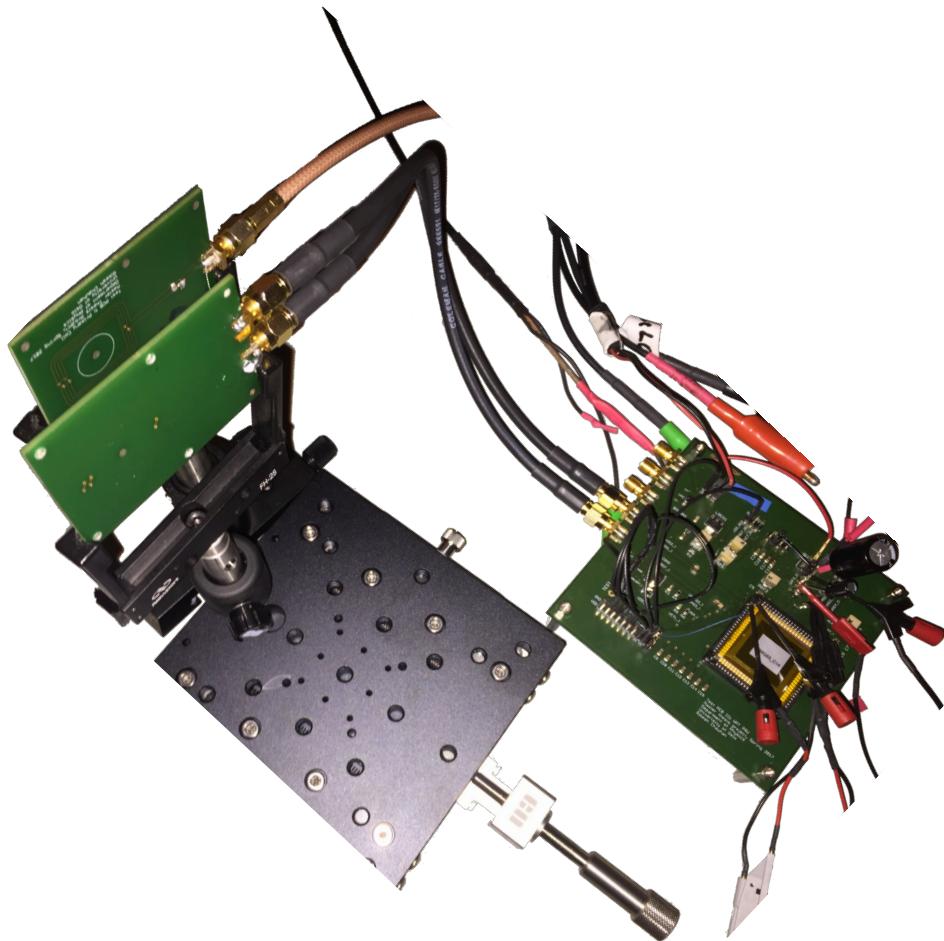
2. Nov. 2017

Rikesh Chauhan



Outline

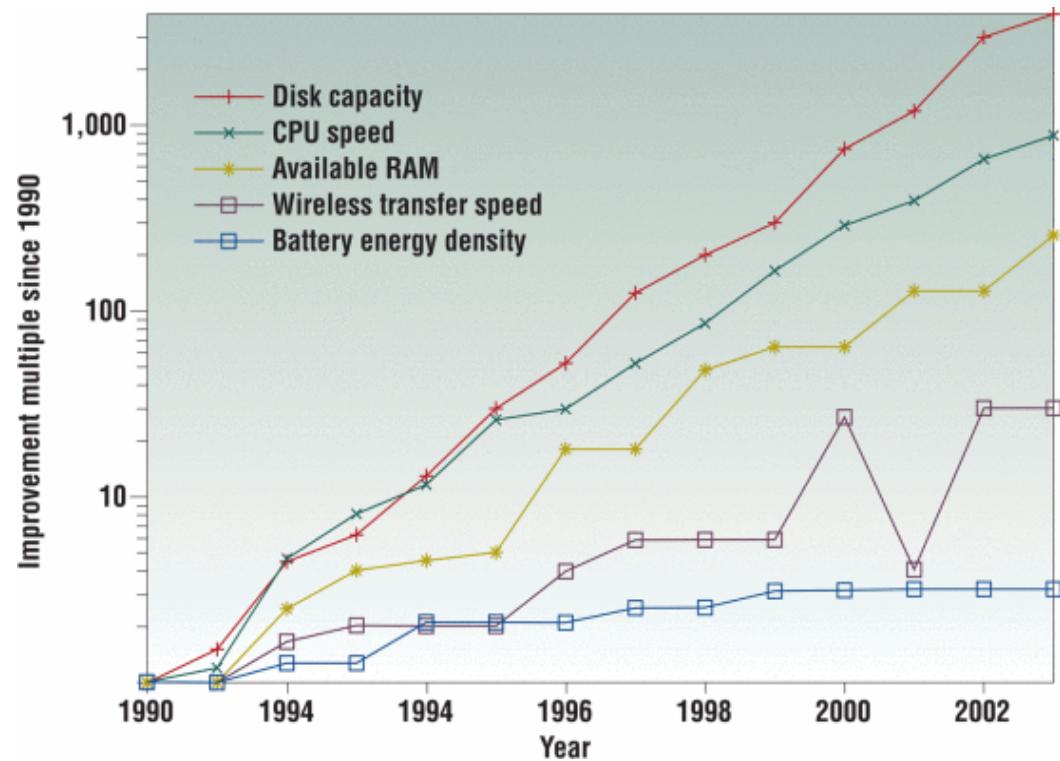
- Motivation
- Background
- Component Design
- PMS Chip
- WPT System
- Measurement and Verification
- Conclusion



Motivation

Technology Trend:

- Size and weight
 - Transistor, IC
- Operation
 - Multifunction, high speed
 - Multi-core, SoC, IoT
- Power consumption
 - Low power
 - Shrinking size, low Vdd
 - Dynamic voltage scaling
 - Operation modes: sleep, nap, doze, active
- Power supply (?)
 - Major constraint
 - Significant proportion of size and weight
 - Regular recharge, replacement

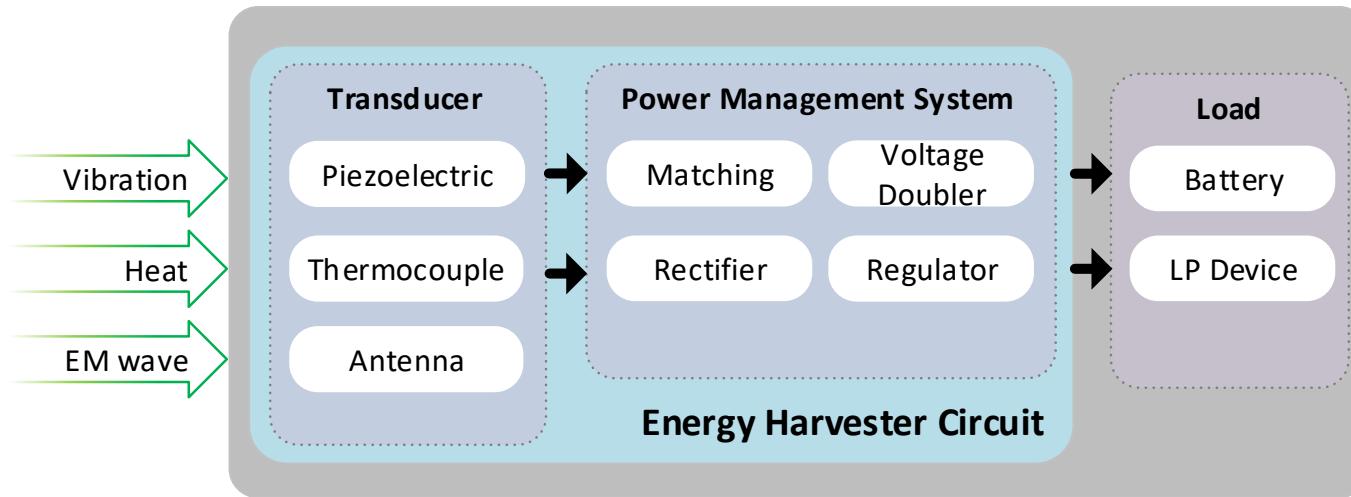


Motivation

- Power supply/Battery
 - Volumetric energy density
 - Gravimetric energy density
 - Reduced self discharge
 - Increased charge cycle
- Lithium-ion battery mostly used
- Research (MORE ON IT)
- Energy Harvesting
 - Ambient energy source
- Wireless Power Transfer
 - Available reliable source

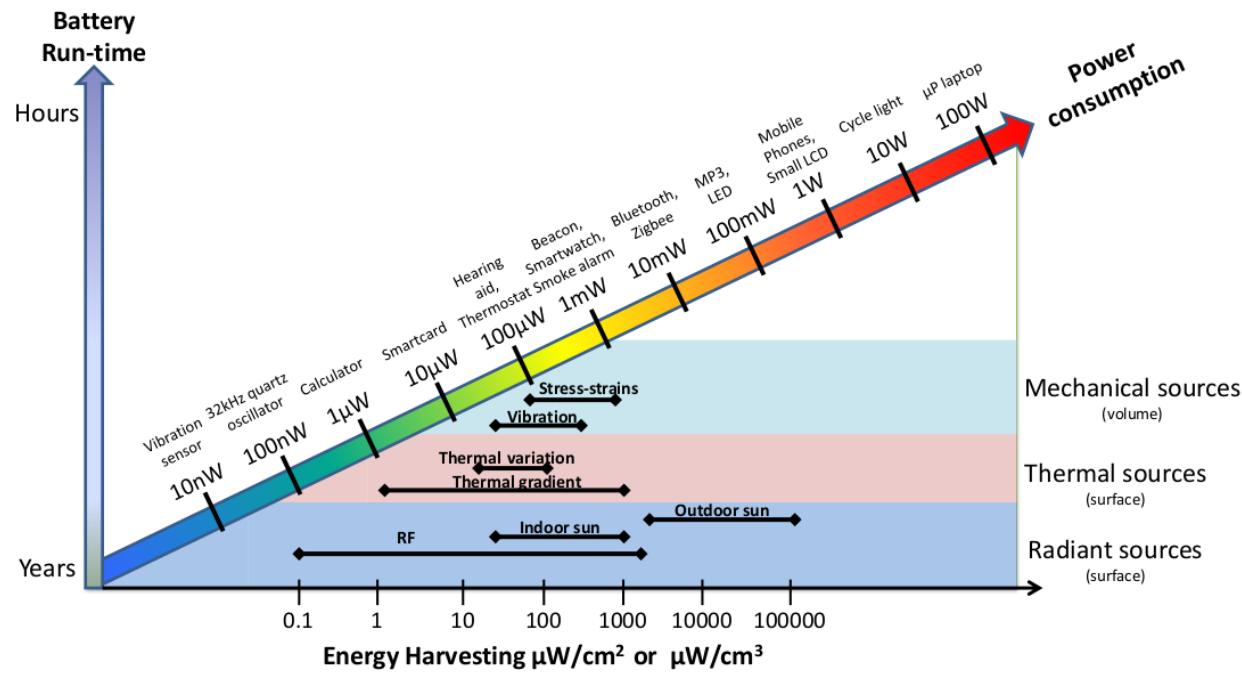


Background: Energy Harvesting



- Perpetual energy source
- Harvesting: Energy source => Transducer => Power Management
- Mostly used 3 types depending on energy source:
 - Kinetic: Mechanical deformation, Piezoelectricity
 - Thermal: Thermocouple, Seebek effect
 - EM: Solar cell, Photoelectric effect

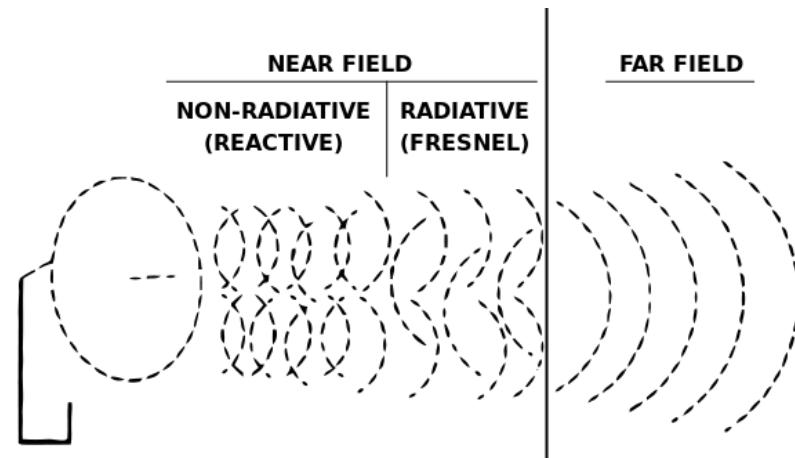
Background: Energy Harvesting



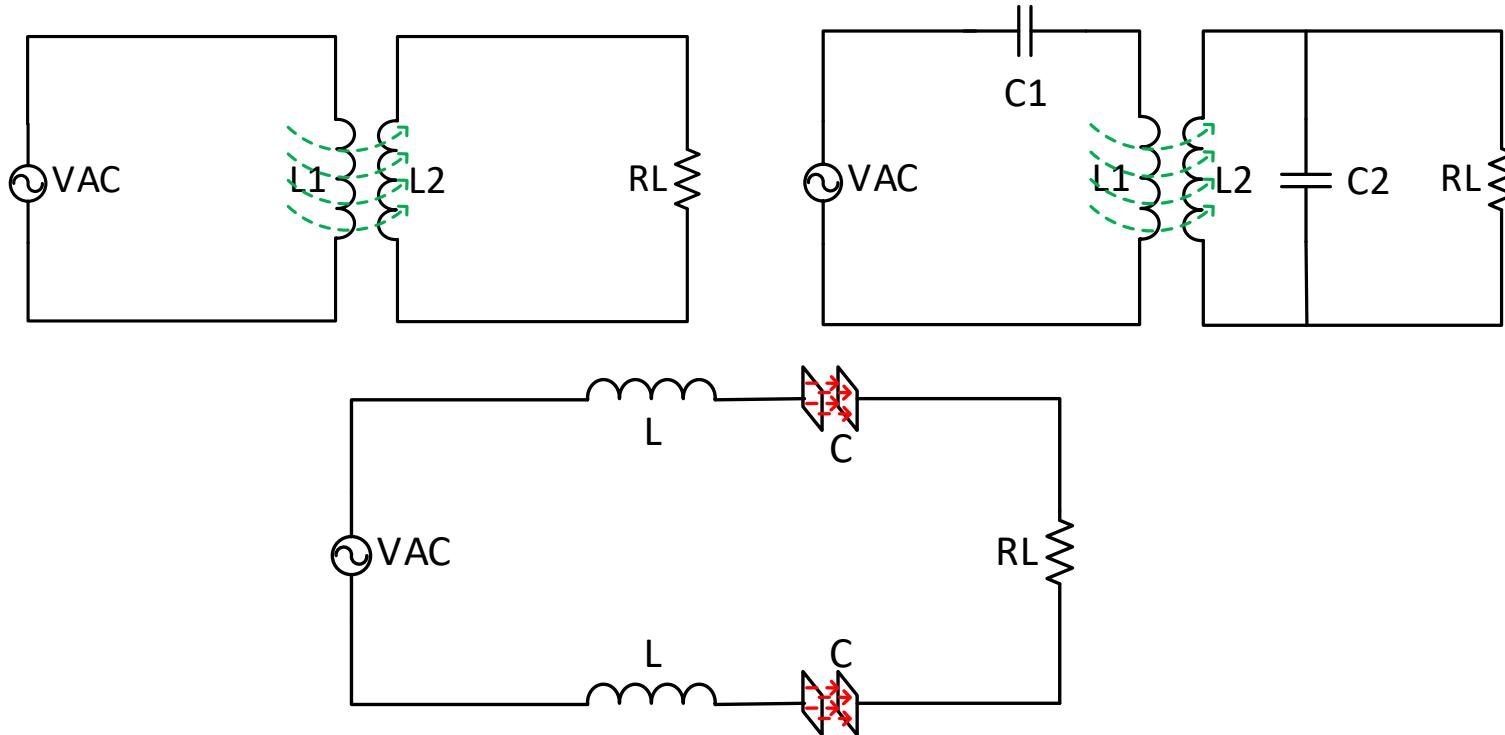
- Low power, low power density
- Applicable to LP sensors
- Not feasible for devices with power $> 1 \text{ mW}$
- If so how about convenient use of already available power ?

Background: WPT

- Cut the cord
 - Minimize most of the constraints
 - Reduced size and weight
 - Water proof, dust proof
 - Reduced accidents
- Transfer distance boundary $\lambda/2\pi$
- Two types depending on transfer distance:
 - Near-field, $< \lambda/2\pi$
 - Non-radiative
 - Magnetic field
 - No RF exposure
 - Far-field, $> \lambda/2\pi$
 - Radiative
 - Electric field
 - RF exposure

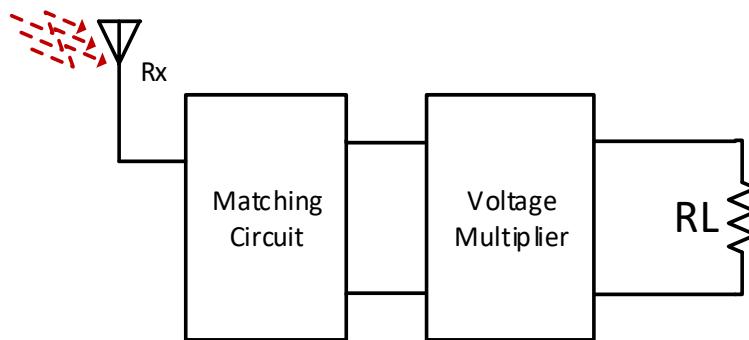


Background: WPT, Near-field



- Inductive power transfer
 - Weakly coupled, mm in range
- Magnetic resonance inductive power transfer
 - Improved coupling, cm in range
 - Simultaneous multiple receiver
- Capacitive power transfer
 - Limited due to large plates, close coupling requirement

Background: WPT, Far-field



- Non-directive
 - Use of isotropic EM wave
 - Non-directive antenna
- Directive
 - Use of beam forming
 - Dedicated directive Rx and Tx
- Health concern, exposure to high power RF wave
- New possibilities:
 - Can transmit both data and energy simultaneously
 - Solar Power Satellite, Stationary High Altitude Relay Platform

Background: WPT, Applications and Standards



(a) Qualcomm EV charger



(b) Qualcomm mobile phone charger with foreign object detection feature

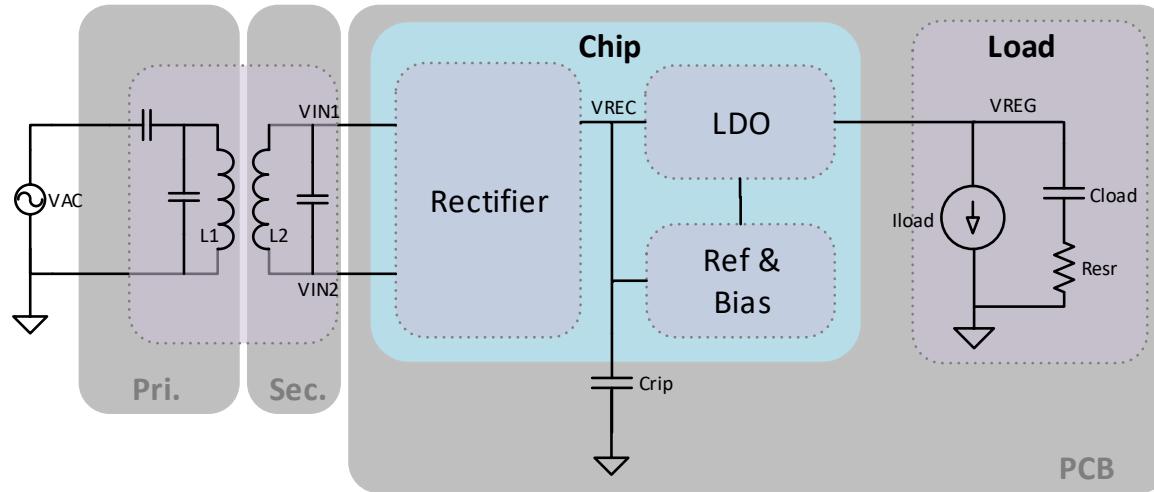


(c) IDT concept of wireless charging of bionic devices

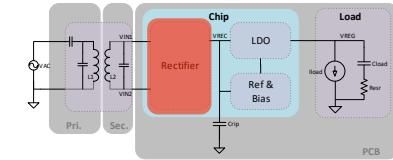
- IPT/MR-IPT application
 - Industrial automation
 - Automotive
 - Consumer electronics
 - Medical implants
- Qi 
 - IPT and MR-IPT
 - Communication and transfer: 80-300 KHz
- A4WP
 - MR-IPT
 - Communication: 2.4 GHz,
Transfer: 6.78 MHz
- AirFuel 
 - A4WP + PMA

Background: This Project

- Pilot project for Nordic Semiconductor
- Resonance inductive coupling
 - Most efficient method so far
- 90 nm CMOS process, 2.5 V devices
 - Design challenge, in literature mostly in higher technology nodes
- 13.56 MHz operating frequency
- Load: 10 mA @1.8V



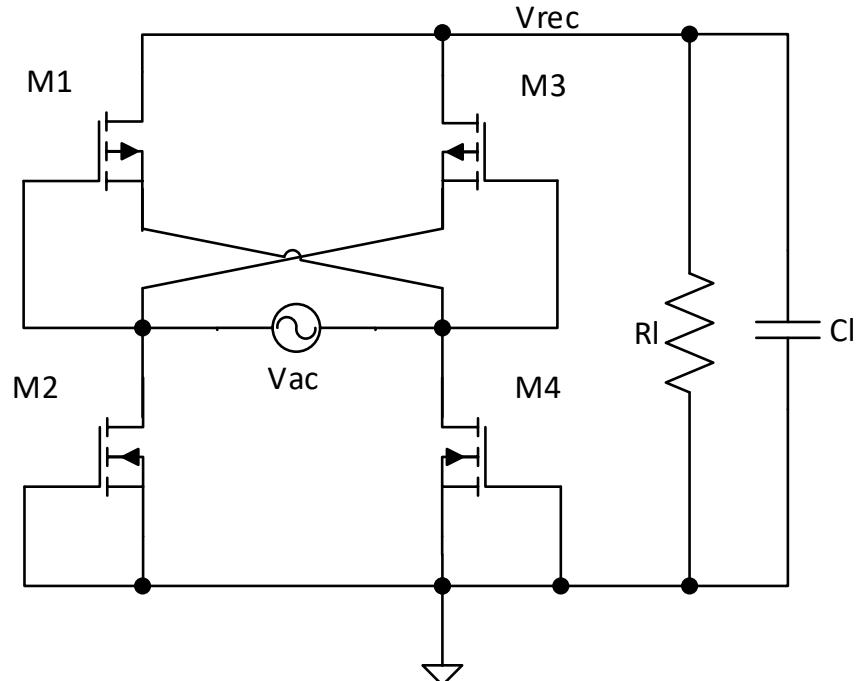
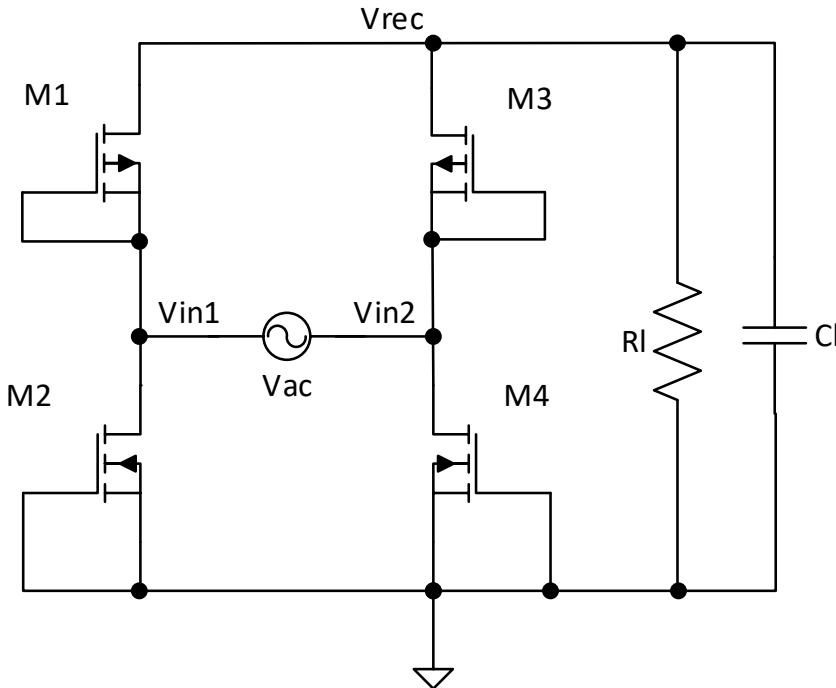
Component Design: Rectifier



Literature:

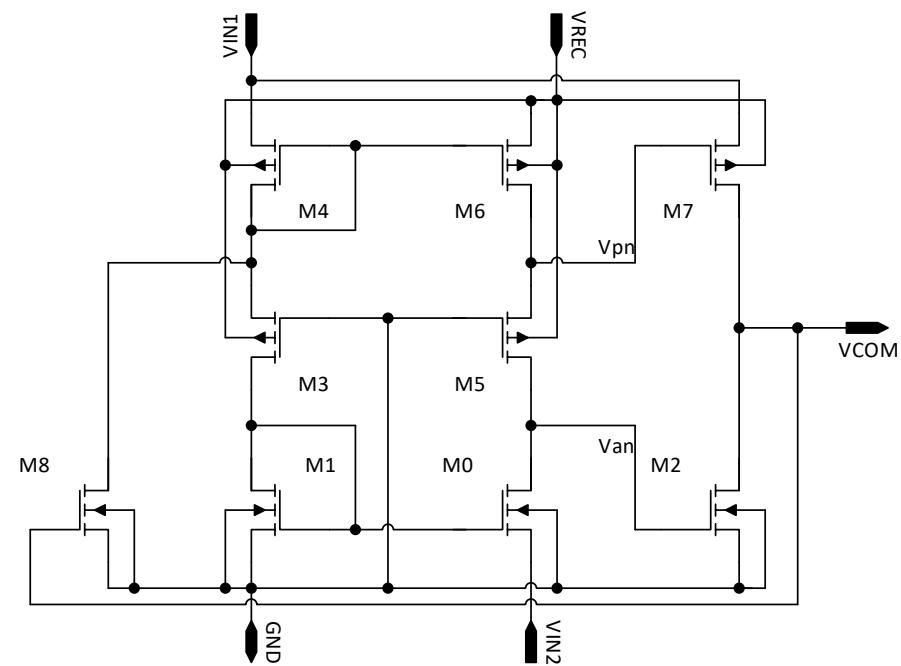
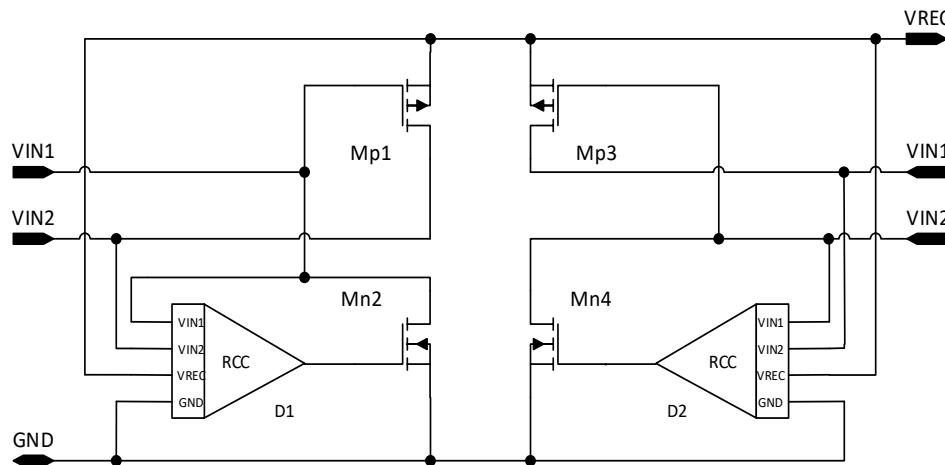
- Full wave bridge rectifier
- Diode connected MOSes
- Voltage drop $2V_{th}$ + conduction drop

- Gate cross coupled full wave bridge
- Diode connected nMOS and gate cross coupled pMOS
- Voltage drop V_{th} + conduction

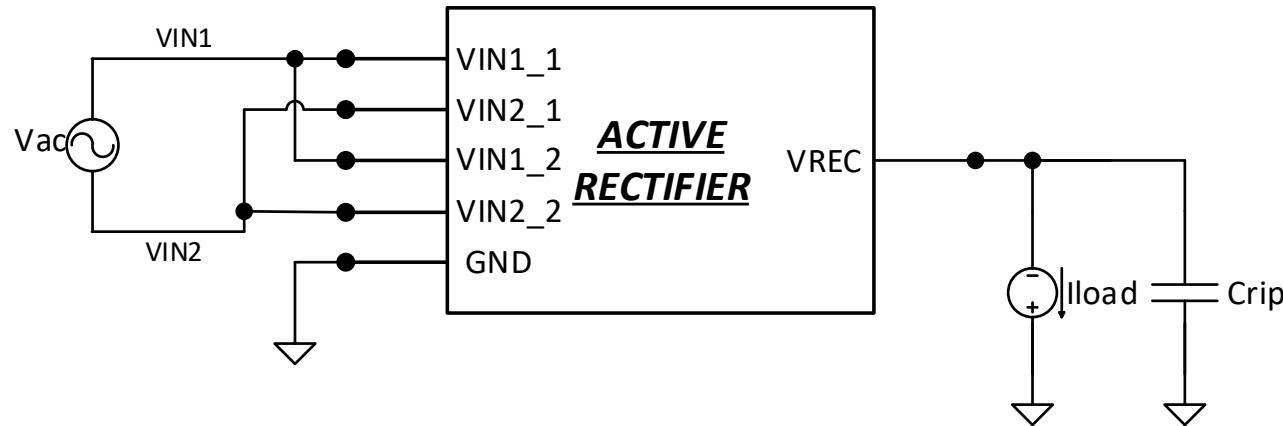


Rectifier: Gate cross coupled with RCC

- Gate cross coupled full wave active rectifier
- Comparator with reverse leakage control (RCC)
- Voltage drop conduction only
- Less conduction drop => increase VCE
- RCC => increase PCE
- Self power start-up
- V_{COM} high when $V_{in1} - V_{in2} > V_{rec}$
- M8 for RCC

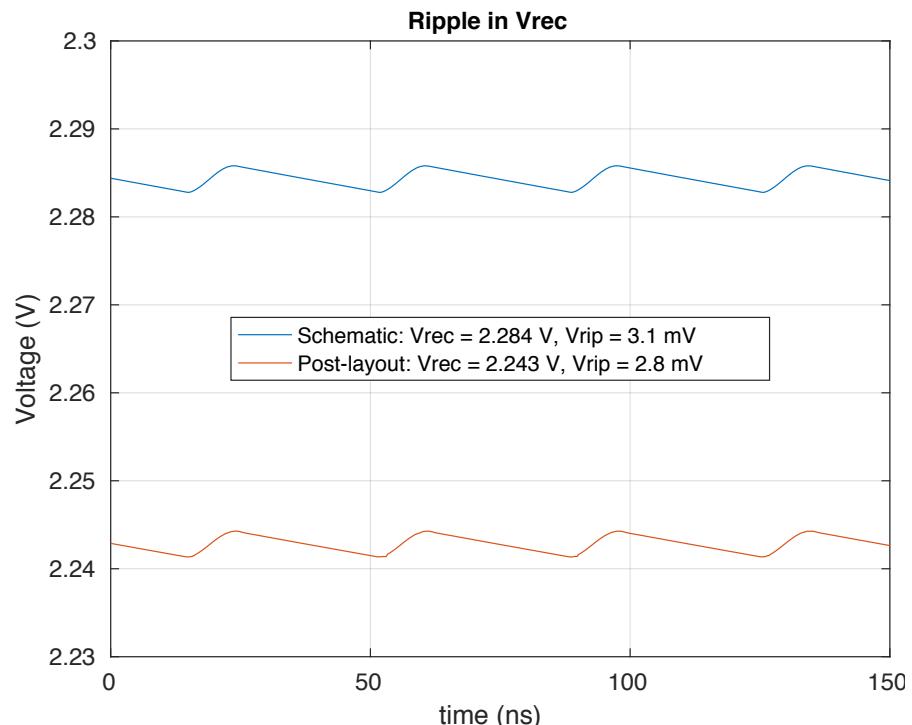
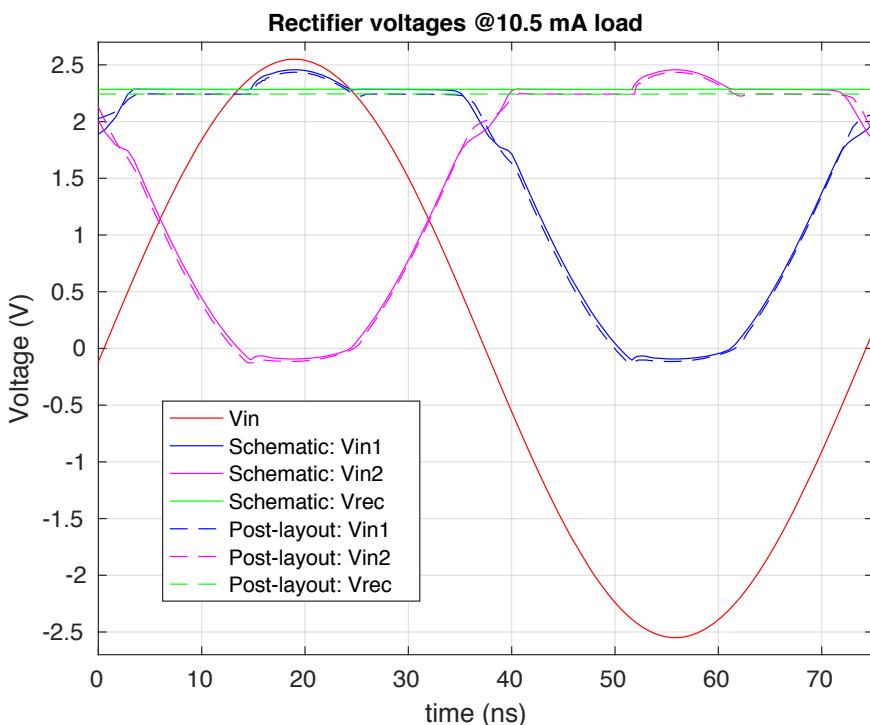


Rectifier: Test bench



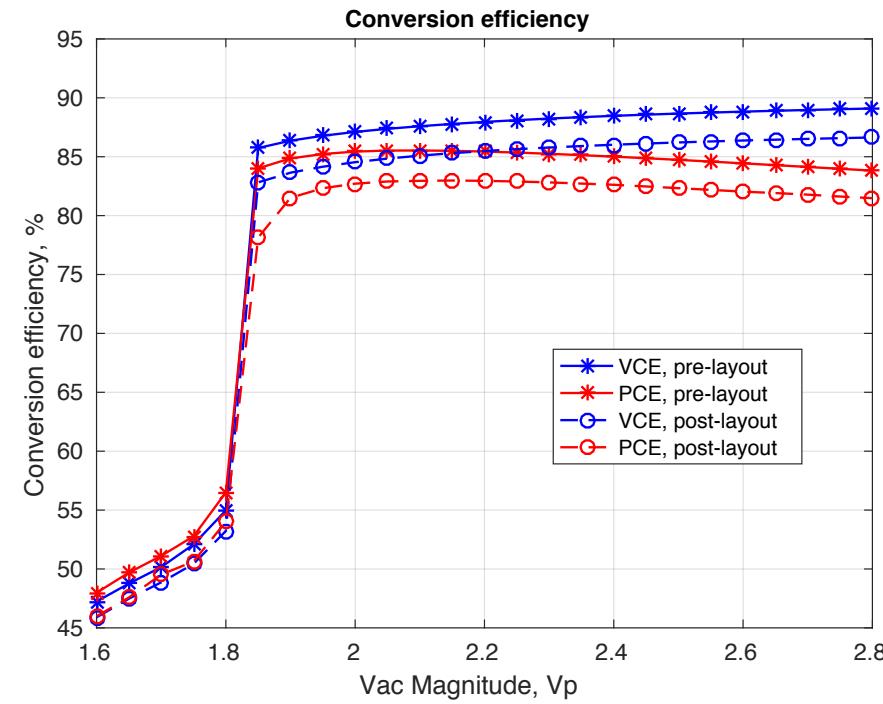
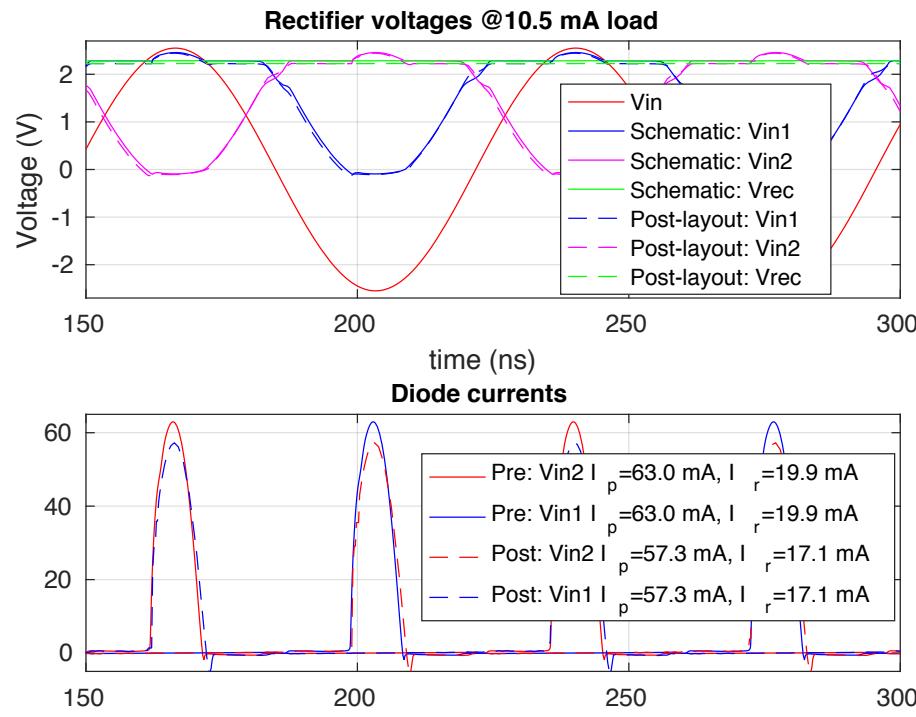
- V_{in1} and V_{in2} differential inputs, 2.5 V
- $I_{load} = 10.5 \text{ mA}$
- $C_{rip} > 100 \text{ nF}$ for $V_{rip} < 3 \text{ mVpp}$

Rectifier: Transient Simulation



- +ve cycle: $V_{in1} > V_{in2}$, $V_{in} = V_{in1} - V_{in2}$
- When $V_{in} < V_{tp}$, M_{p3} and M_{n4} OFF
- When $V_{in} \geq V_{tp}$, M_{p3} ON, V_{in1} shorted to V_{rec}
- When $V_{in} \geq V_{rec}$, M_{n4} ON, Crip charged
- When $V_{in} < V_{rec}$, M_{n4} OFF
- When $V_{in} < V_{tp}$, M_{p3} OFF

Rectifier: Current, PCE and VCE



- Reduced peak diode current
 - Additional R_{on} + resistive conduction path
- More reverse leakage
 - Wide conductive path over D/S, larger parasitic, more comparator delay

Rectifier: Performance

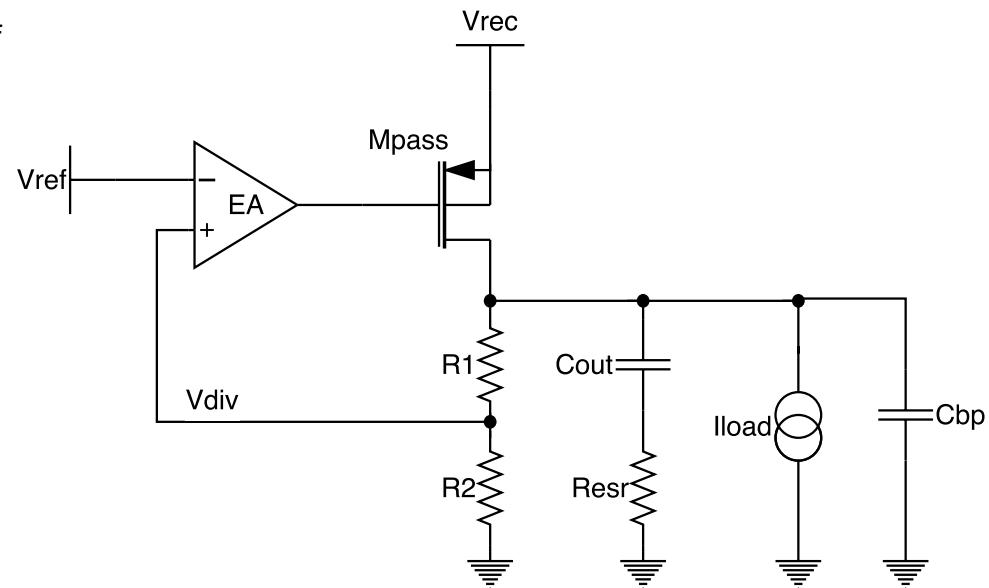
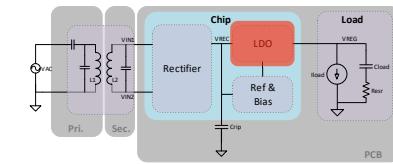
Table 3.2: Rectifier performance summary

| | Schematic | Post-layout |
|--------------------|-----------|-------------|
| Rectified DC | 2.28 V | 2.14 V |
| Ripple Vpp | 3.1 mV | 2.8 mV |
| Peak diode current | 63 mA | 57.3 mA |
| PCE | 84.5 % | 82.9 % |
| VCE | 88.6 % | 86.2 % |

- V_{rec} , diode current, PCE and VCE less in post layout simulation
- Resistive conductive path in layout
- Reverse leakage observed in post layout result
- Wide conductive paths over G, D and S increasing parasitic capacitance

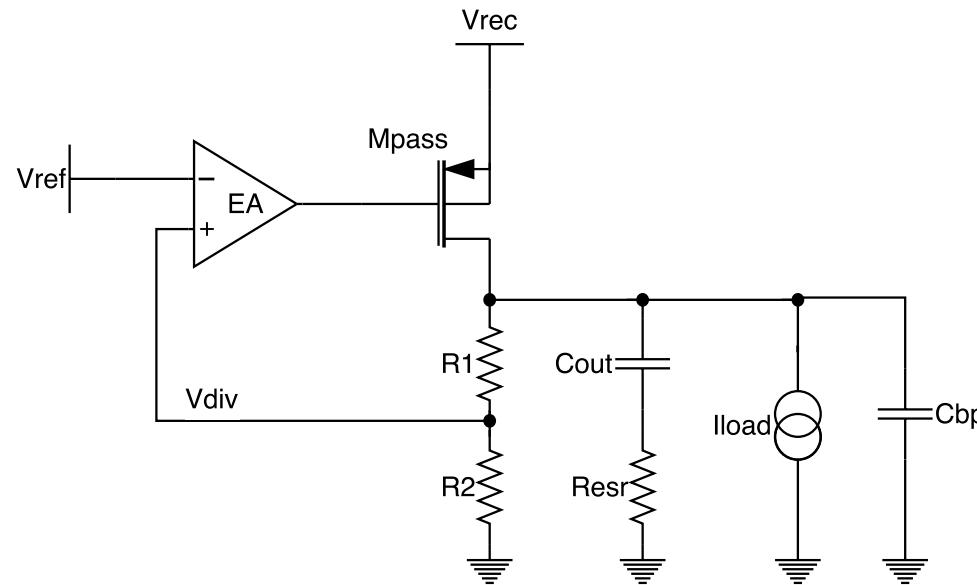
Component Design: LDO

- Conventional LDO meets the requirements
 - $V_{rec} > V_{reg}$
 - Less noise, faster settling
- pMOS as pass device
 - Less dropout, less quiescent current, -ve signal driven
- Folded cascode as error amplifier (EA)
 - High gain, less error, higher V_{reg} accuracy
 - Stability convenience, one high impedance node
- $V_{reg} = (1 + R_2/R_1)V_{ref}$



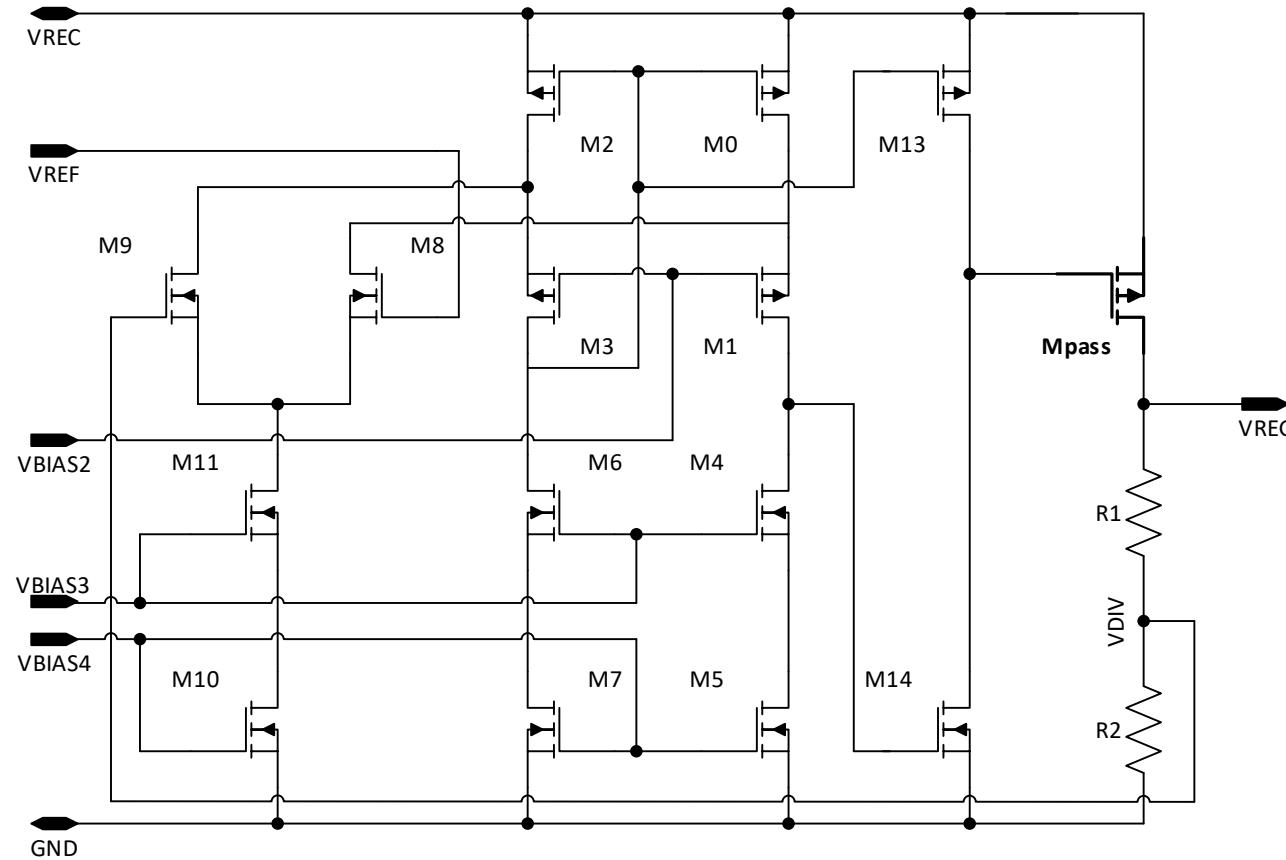
LDO: Stability

- $p_1(r_{o_pass}, C_{out})$, $p_2(R_{sr}, C_{bp})$, $p_3(R_{o_ea}, C_{gs_pass})$
- $z_1(R_{sr}, C_{out})$
- p_1 dominant, p_2 beyond UGF, p_3 below UGF \Rightarrow unstable
- Suitable R_{sr} and large C_{out} to cancel p_3 with z_1 , left half plane zero

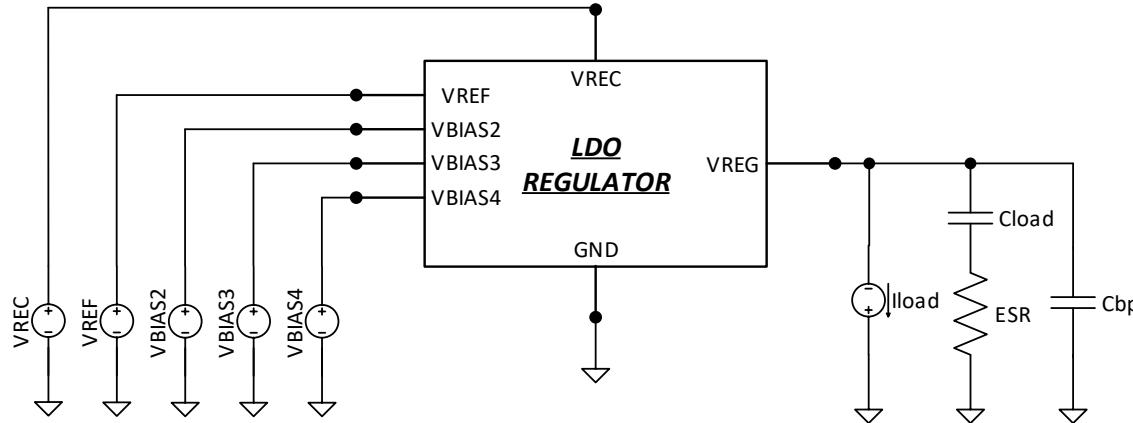


LDO: Design

- EA, Buffer, Pass device, resistive network
- Buffer to drive large pass element, M_{pass}



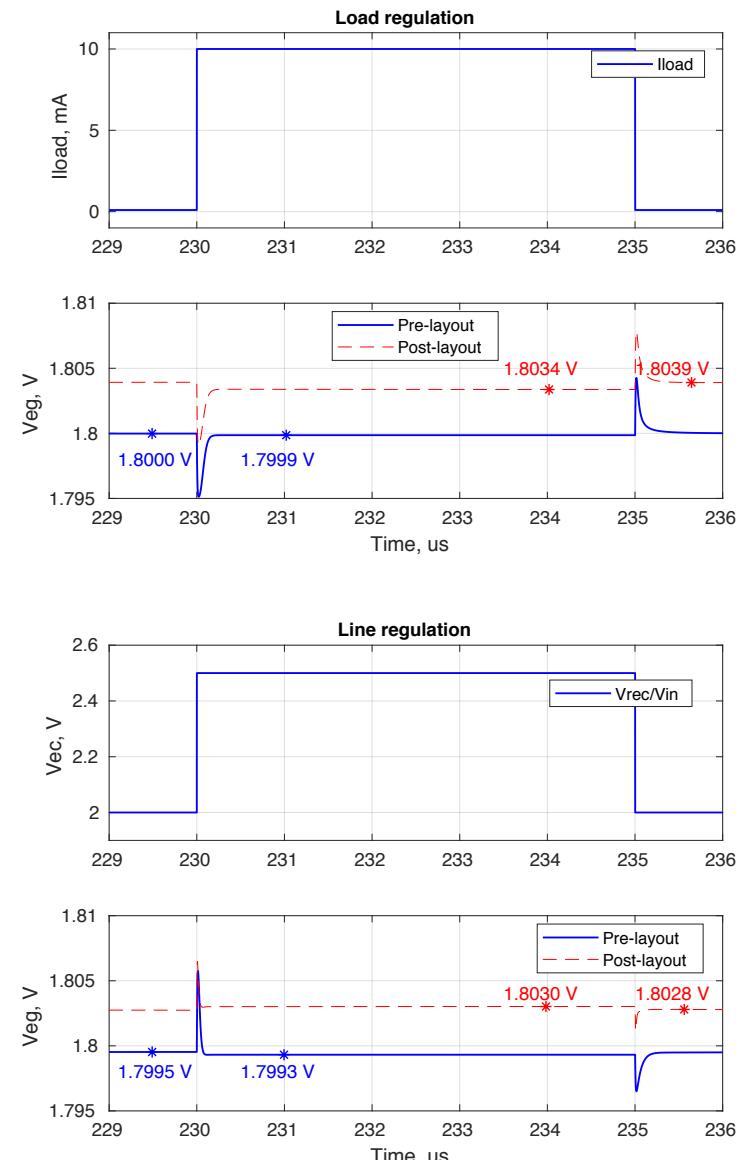
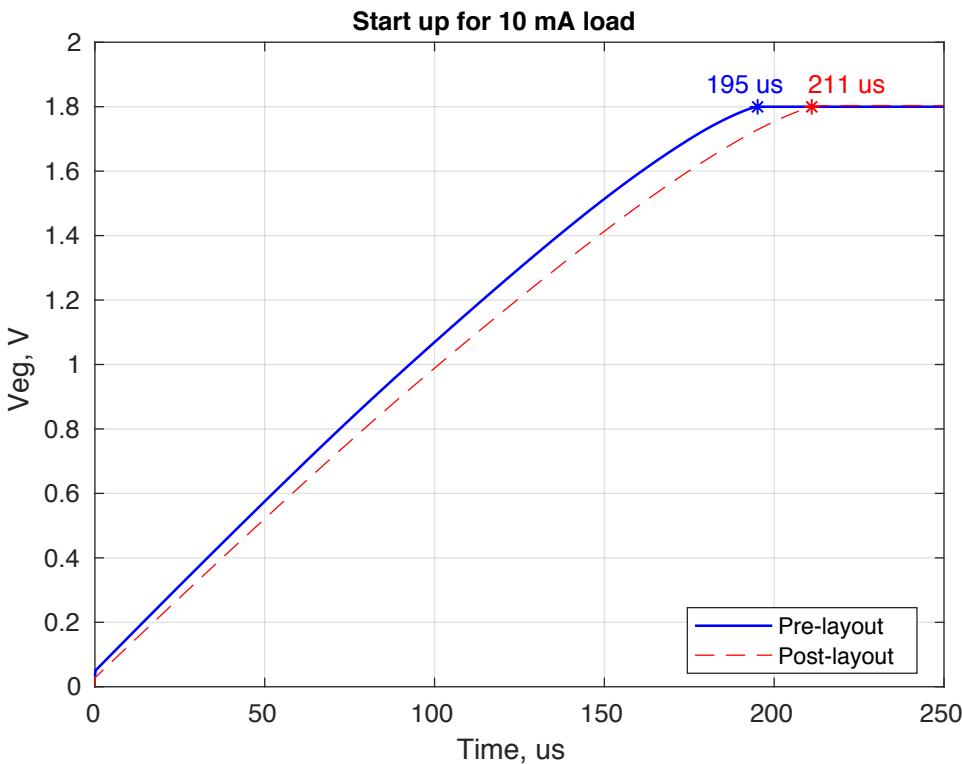
LDO: Test bench



- $V_{rec} = V_{in} > 2.15 \text{ V}$
- V_{ref} , bandgap of Si = 1.177 V
- $V_{bias2}, V_{bias3}, V_{bias4} = 1.1 \text{ V}, 0.88 \text{ V}, 0.68 \text{ V}$ respectively
- $C_{load} > 2.5 \mu\text{F}$ and $R_{load} > 0.5 \Omega$
- $C_{bp} = 10 \text{ nF}$
- $I_{load} = 10 \text{ mA}$

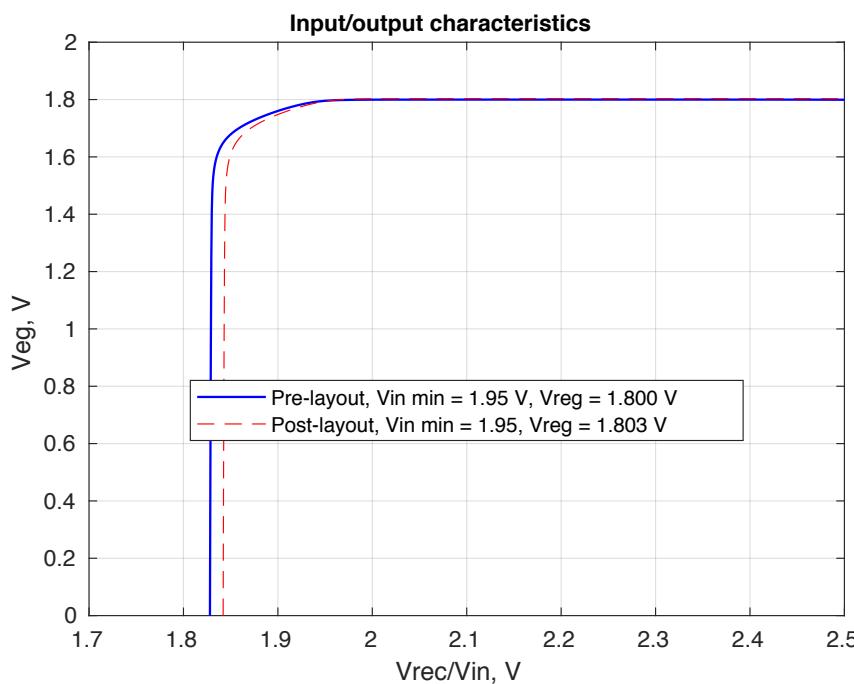
LDO: Transient Simulation

- Line Reg. = $\Delta V_{\text{reg}}/\Delta V_{\text{in}}$
- Load Reg. = $\Delta V_{\text{reg}}/\Delta I_{\text{load}}$
- Startup dependent on C_{load}

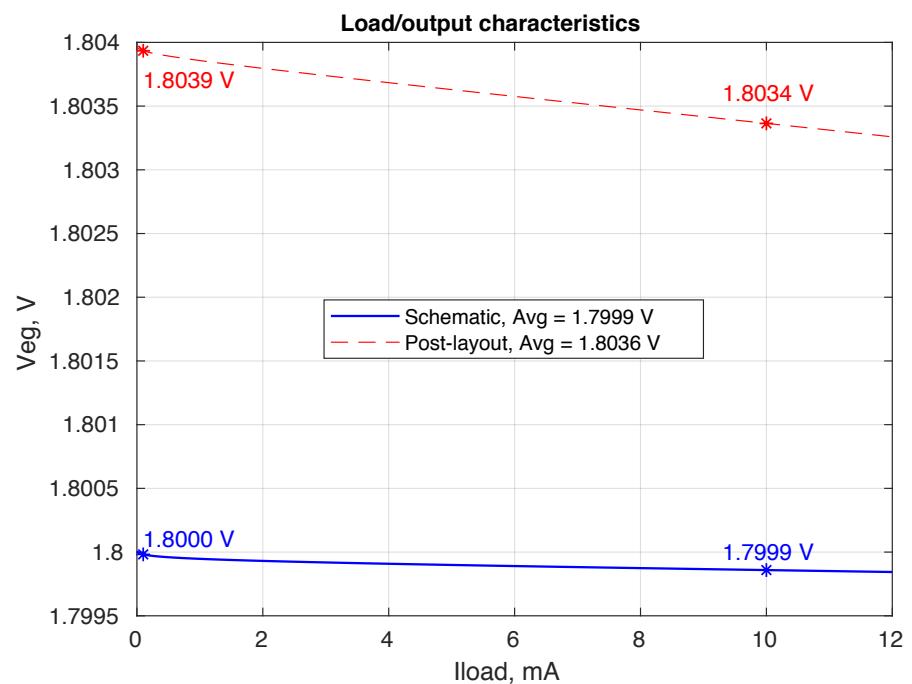


LDO: DC Simulation

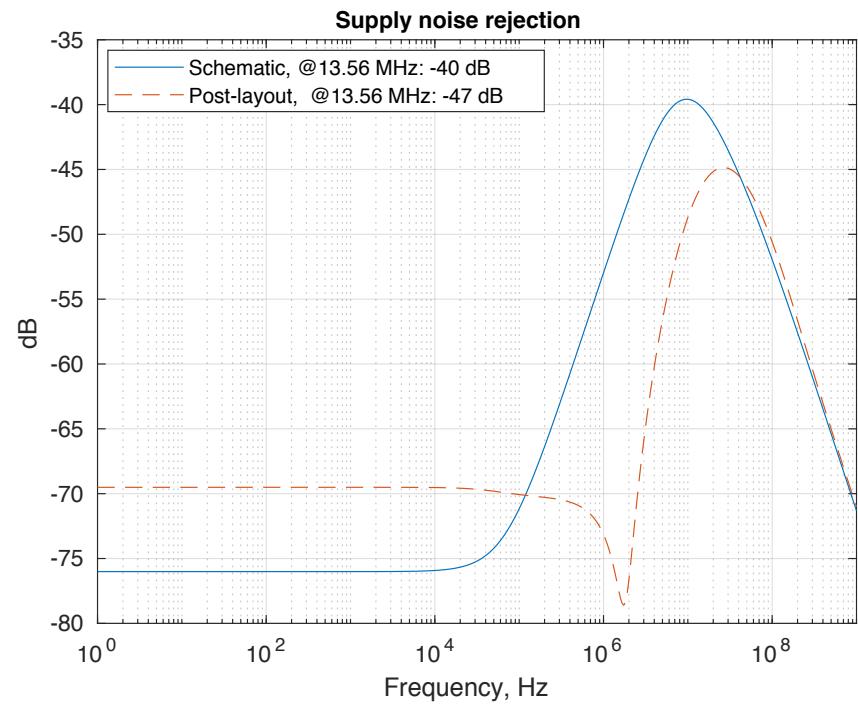
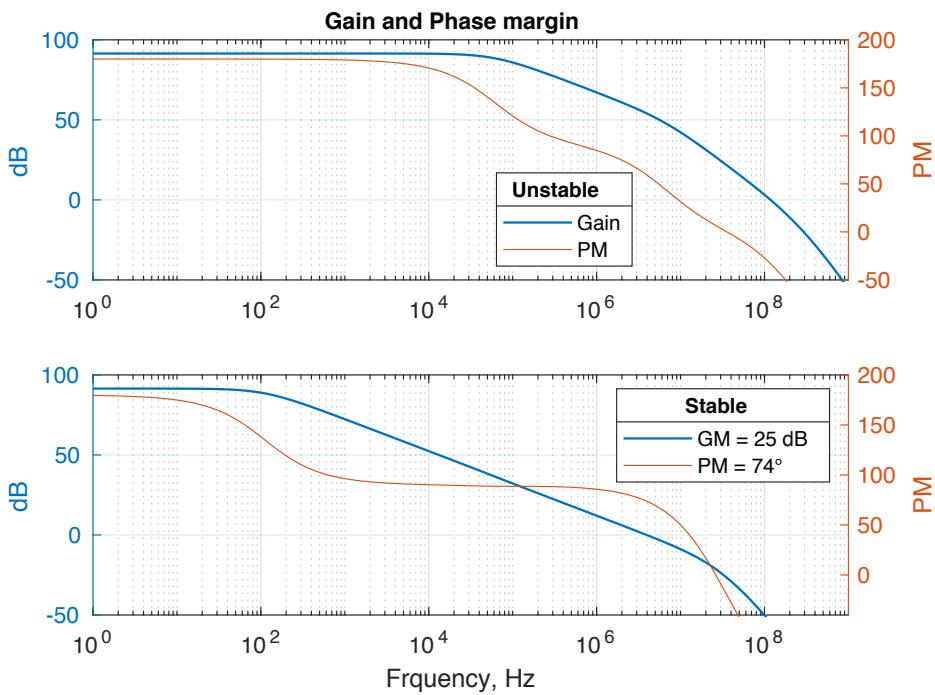
V_{in} Sweep @10mA I_{load}



I_{load} sweep @2.2 V V_{in}



LDO: Stability and PSSR



- 3 poles: 2 below UGF, 1 above
- Zero to cancel non dominant pole
- PSSR:
 - Good at LF with high open loop gain
 - Low at HF, reduced UGF after stability

LDO: Performance

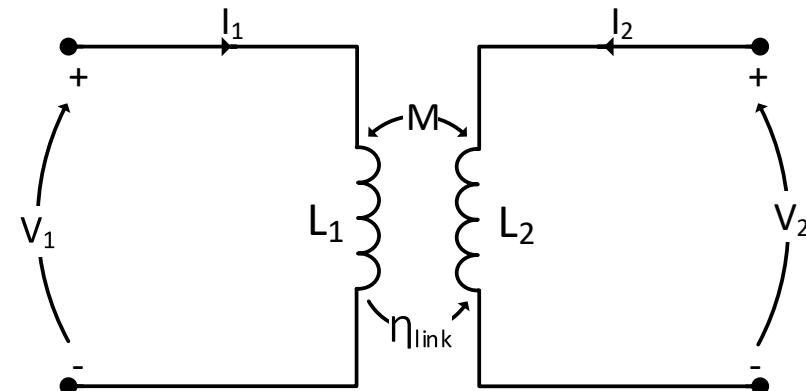
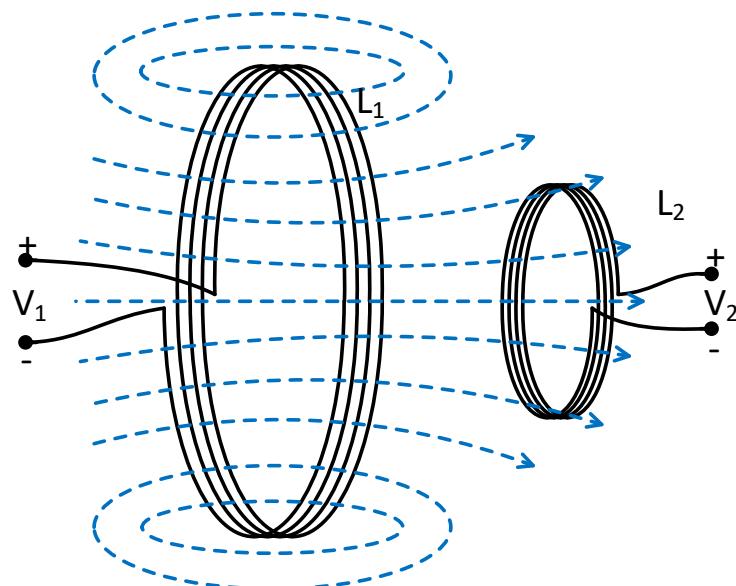
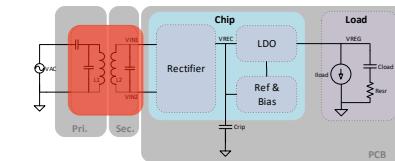
Table 4.2: LDO performance summary

| | Schematic | Post-layout |
|-------------------|--------------------|-------------------|
| PSSR | -36 dB @ 13.56 MHz | -59 dB @ 13.56 MH |
| Phase margin | 75° | |
| Gain margin | 30 dB | |
| Power efficiency | 80.9 % | 81 % |
| Quiescent current | 105 uA | 114 uA |
| Load regulation | 17 uV/mA | 53 uV/mA |
| Line regulation | 435 uV/V | -1.162 mV/V |

- V_{reg} increased by 3mV in post layout
- Load and line regulation has increased too
- Quiescent current increased but efficiency almost the same, interesting(but how?)

Component Design: Antenna

- Faraday's law of EM induction
- $V_2 = M \frac{dI_1}{dt}$
- $M = k \sqrt{L_1 \cdot L_2}$
- $\eta_{\text{link}} = k^2 Q_{L1} \cdot Q_L / [(1 + k^2 Q_{L1} \cdot Q_L)(Q_{L2} + Q_L)]$



Antenna: Modeling

- Nordicsemi antenna
- HFSS model
 - Coil and dielectric properties
 - $R_p = 0.66 \Omega$
 - $C_p = 3.2 \text{ pF}$
 - $L_1 = 509 \text{ nF}$

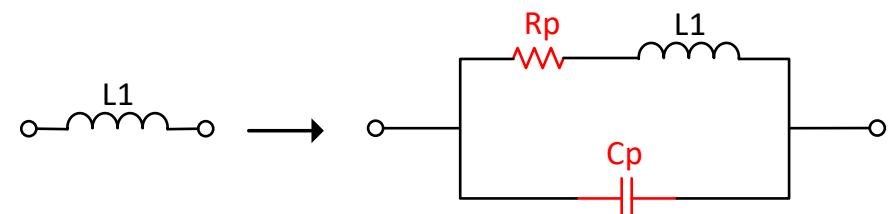
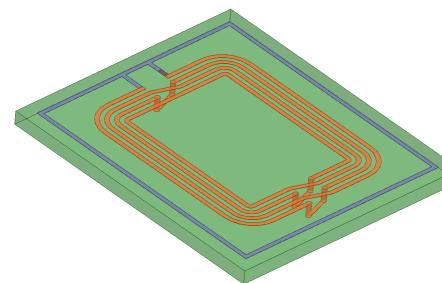
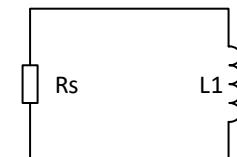


Figure 5.2: Real antenna model

- Modified Wheeler
 - Spiral rectangular, pointed edge
 - $L_1 = 644 \text{ nH}$



(a) HFSS antenna model

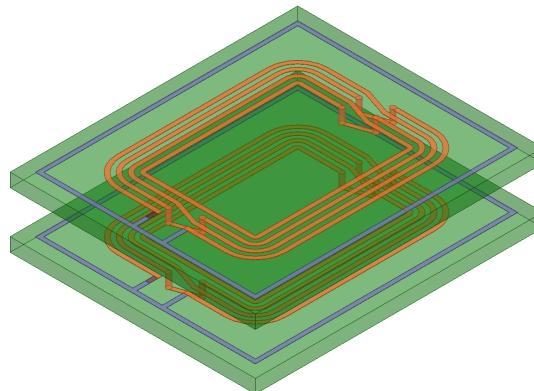


(b) Equivalent schematic

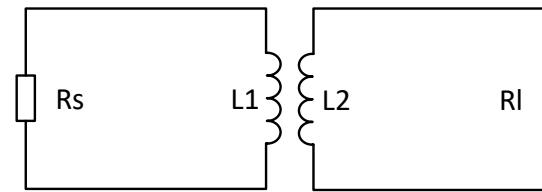
- $Q = \omega L_1 / R_p$
- $SRF = 1/(2\pi\sqrt{L_1 \cdot C_p})$

Figure 5.3: Antenna model

Antenna: Coupling Modeling



(a) HFSS coupling model



(b) Equivalent schematic

Figure 5.4: Antenna coupling model

Table 5.2: Coupling parameters for varying coils distance

| | Sepr: 2 mm | Sepr: 5 mm | Sepr: 10 mm | Unit |
|-----------|------------|------------|-------------|------|
| L_1^* | 357 | 481 | 501 | nH |
| L_2^* | 353 | 476 | 496 | nH |
| M | 254 | 122 | 50 | nH |
| k | 0.52 | 0.25 | 0.10 | - |
| Q_{L_1} | 39-60 | 57-63 | 62 | - |
| Q_{L_2} | 40-64 | 61-67 | 67 | - |

- $L^* = L(1-k^2)$

Antenna: Magnetic Resonance

- HFSS Model to ADS in s2p
- Model RI to as DC load(rectifier + LDO + Iload) $\approx 115 \Omega$
- Cs1: parallel resonance in secondary
 - $X_{L2} < R_L$
- Cp1 and Cp2: series-parallel resonance at primary
 - Matched: canceled both real and imaginary impedance
- Resonance at fixed operating frequency, 13.56 MHz

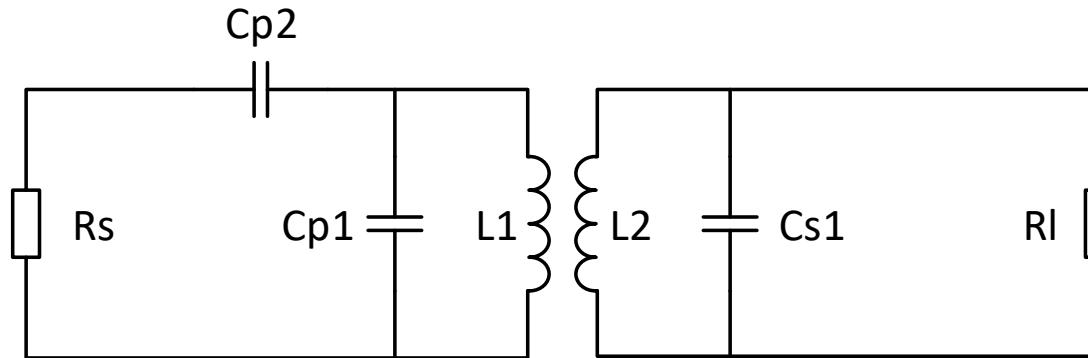
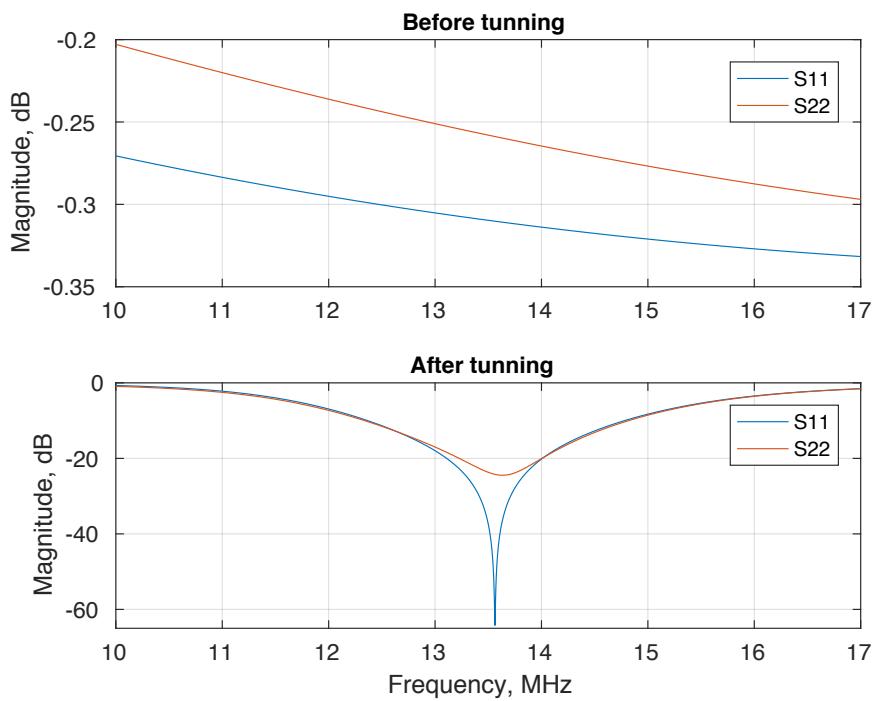


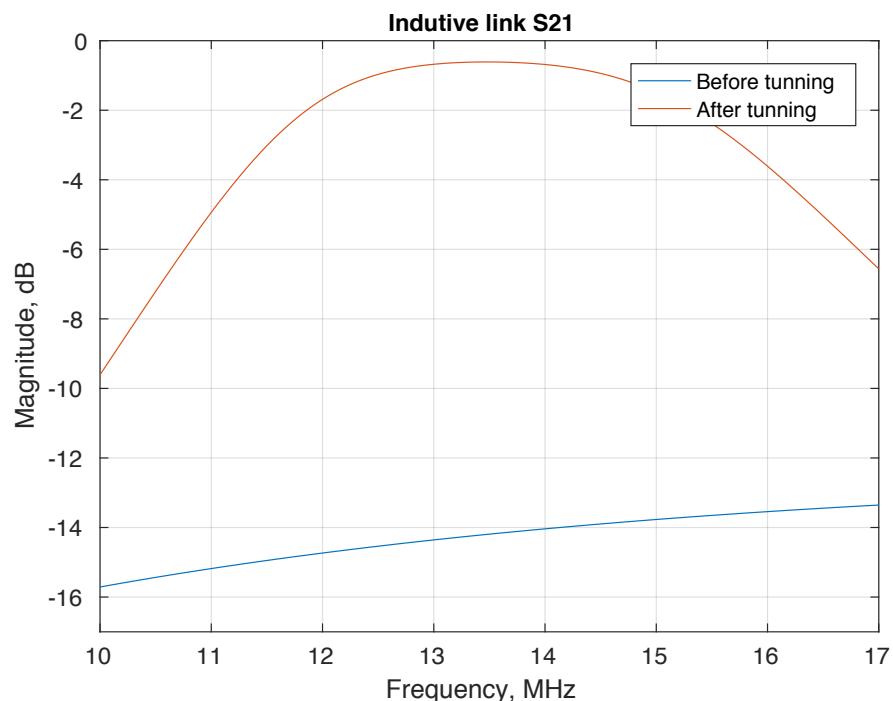
Figure 5.5: Resonant coupled inductive link

Antenna: 5mm Magnetic Resonance

Reflection losses



Power transfer



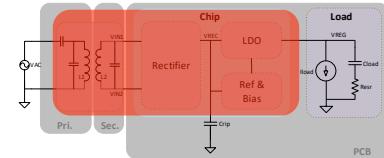
Antenna: Performance

Table 5.3: Performance of resonant inductive link

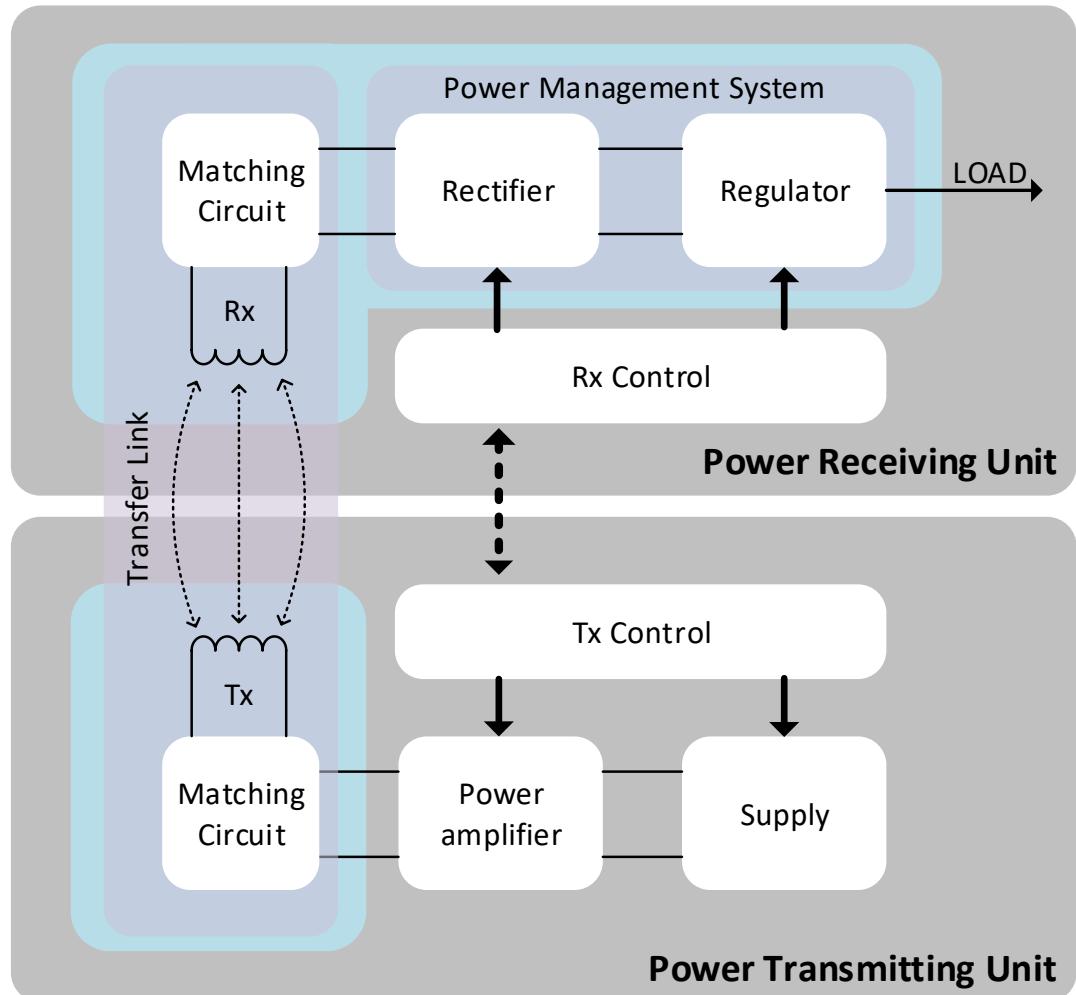
| | Sepr: 1.5 mm | Sepr: 5 mm | Sepr: 10 mm | Unit |
|---------------|---------------------|-------------------|--------------------|-------------|
| C_{P1} , | 660 | 126 | 51 | pF |
| C_{P2} | 80 | 190 | 227 | pF |
| C_{S1} | 288 | 288 | 288 | pF |
| <i>Freq.</i> | 13.56 | 13.56 | 13.56 | MHz |
| S_{11} | -55 | -61 | -29 | dB |
| S_{22} | -30 | -24 | -9 | dB |
| S_{21} | -0.28 (0.97) | -0.61 (0.93) | -2.50 (0.75) | dB (mag.) |
| η_{link} | 94 | 86 | 56 | % |

- Resonance canceled leakage inductance
- Decreased S_{11} and S_{22} , increased S_{21}
- η_{link} for perfectly matched R_L , remember rectifier is non-linear load

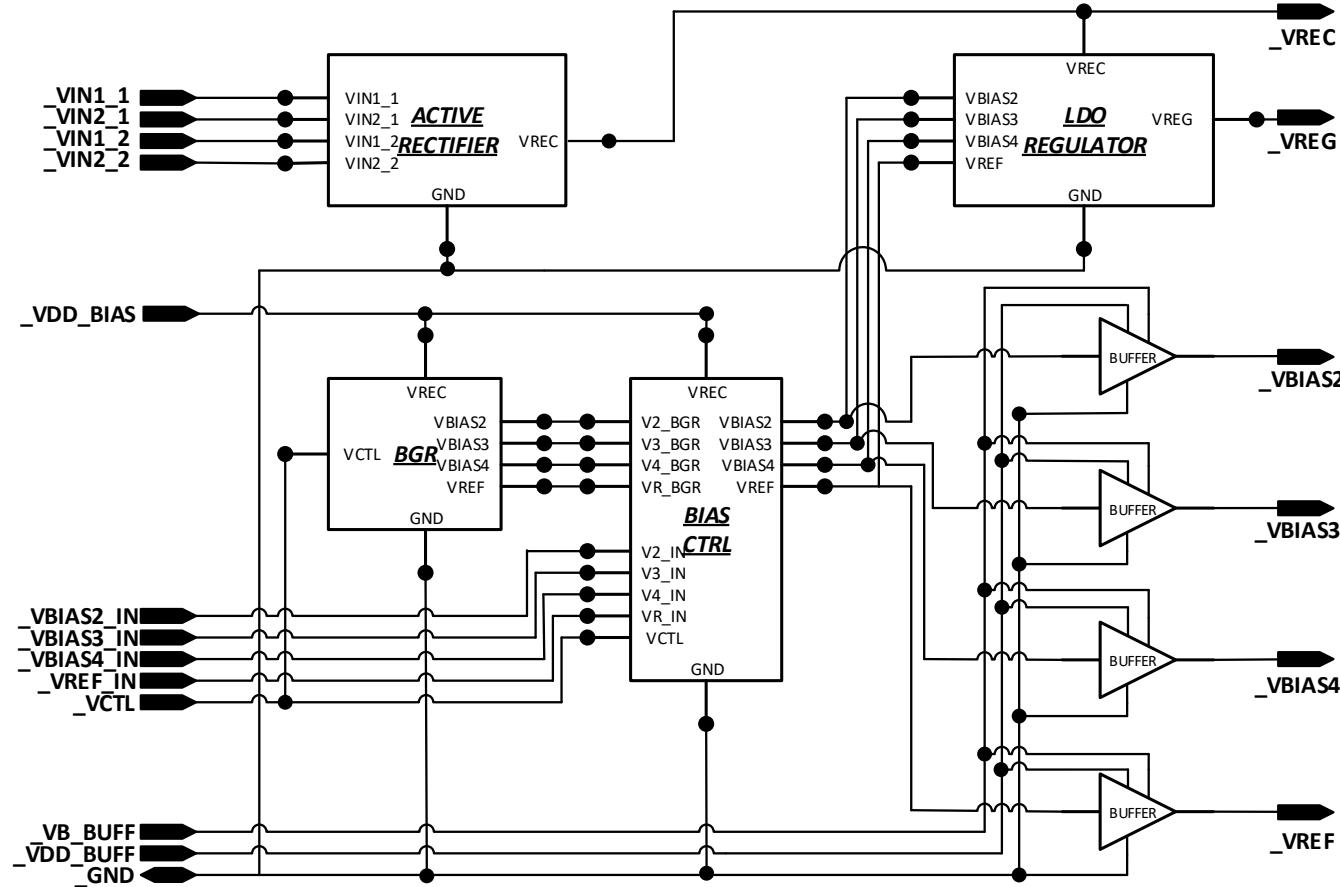
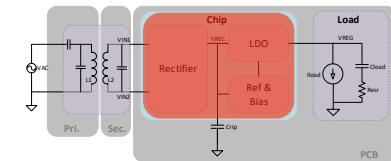
WPT System



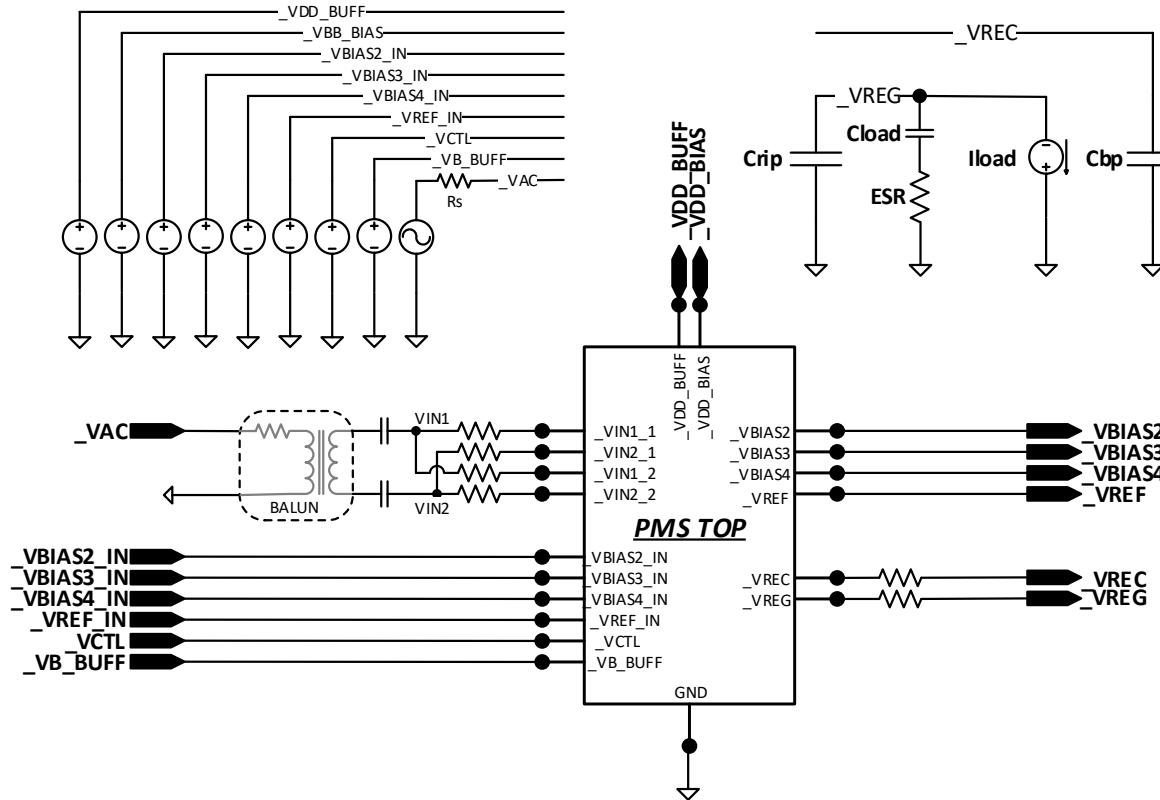
- PTU + PRU
- PTU
 - PA, Tx, Control
- PRU
 - PMS, Rx, Control
- PMS + Transfer Link
- PMS
 - Rectifier
 - LDO
- Transfer Link
 - Rx, Tx
 - Tuning



PMS: Rectifier + LDO

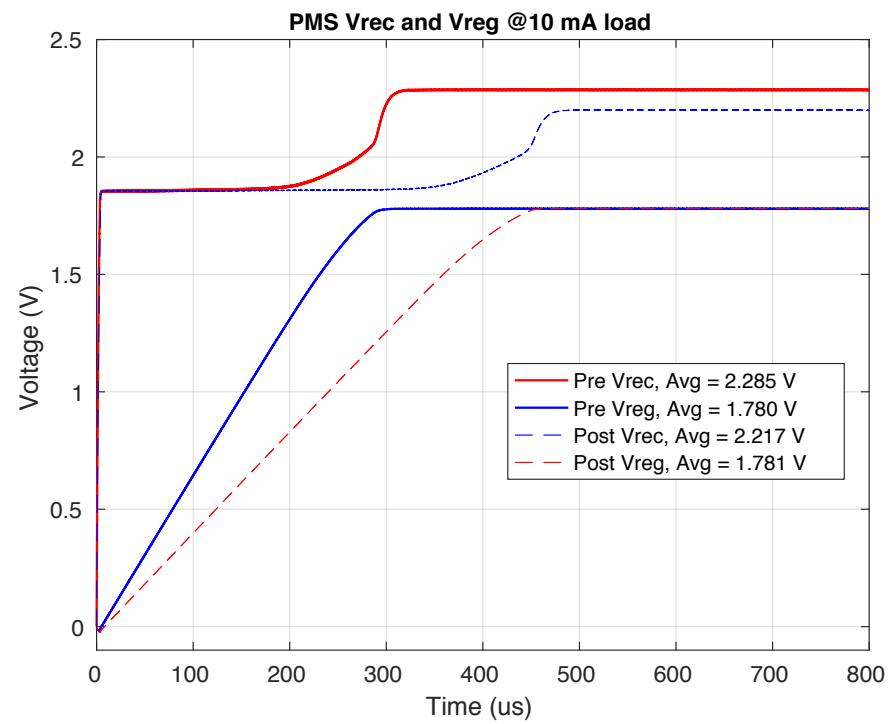
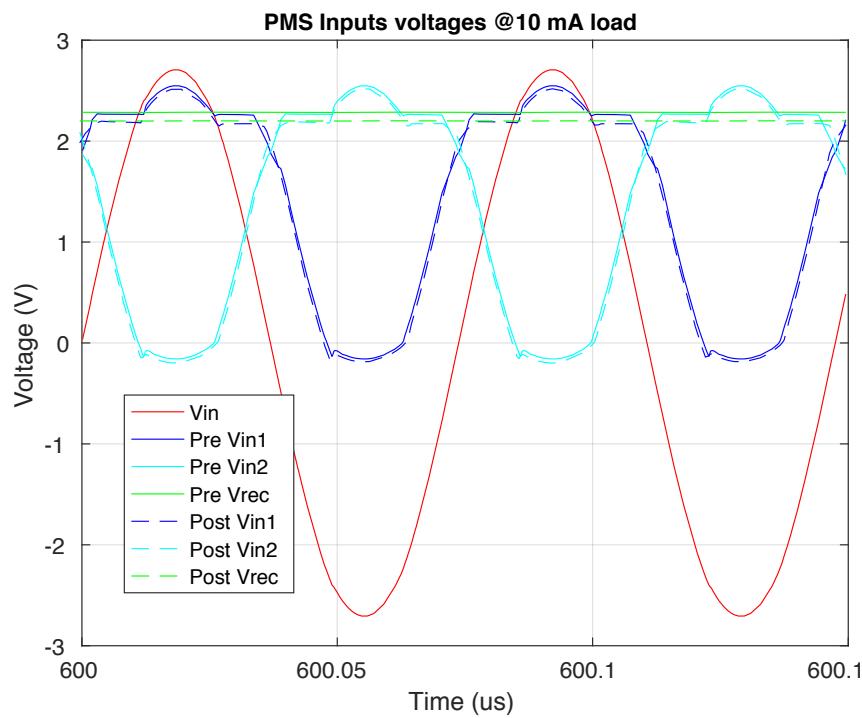


PMS: Test bench

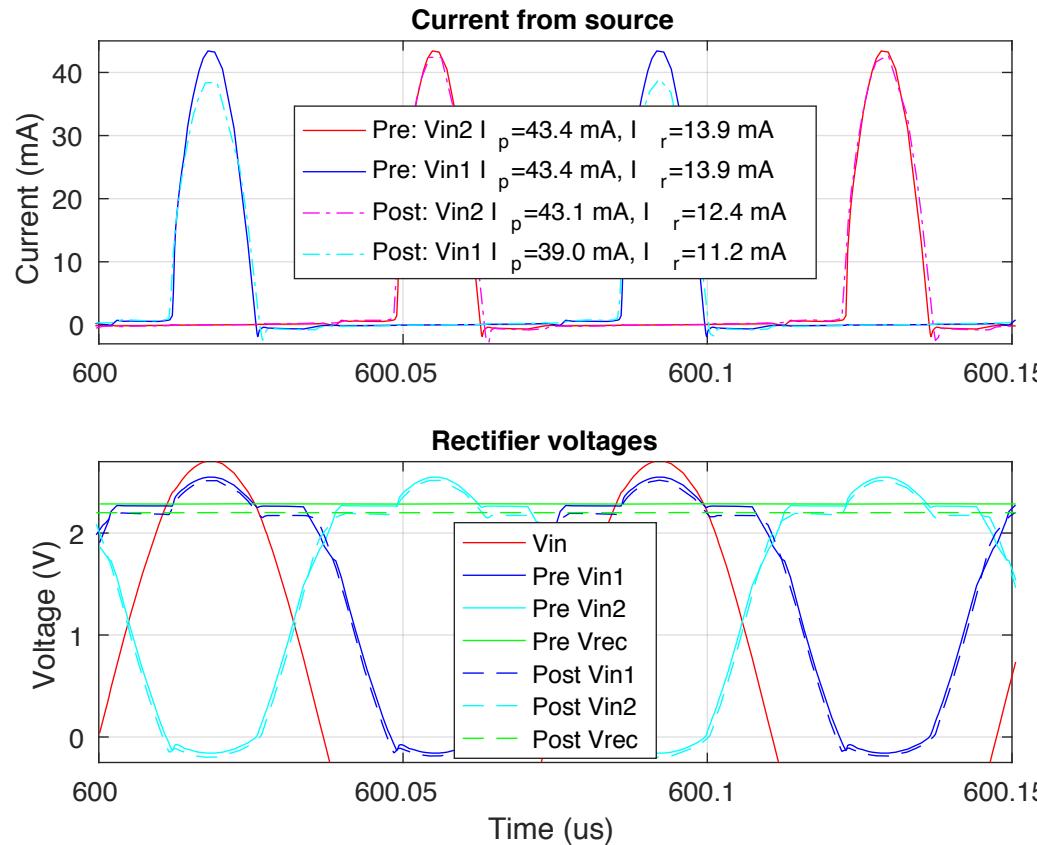


- Inclusion of pad resistance 2Ω , $V_{AC} = 2.6 \text{ V}$
- Balun to create differential V_{IN1} and V_{IN2}
- Rest biases and component values as earlier

PMS: Input, Output Voltages



PMS: Diode currents



- Peak diode current asymmetrical, $I_{\text{vin}2} > I_{\text{vin}1}$
- Uneven resistive path from pad to rectifier inputs
- As in rectifier slight reverse current

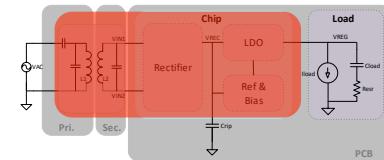
PMS: Performance

Table 6.2: PMS performance summary

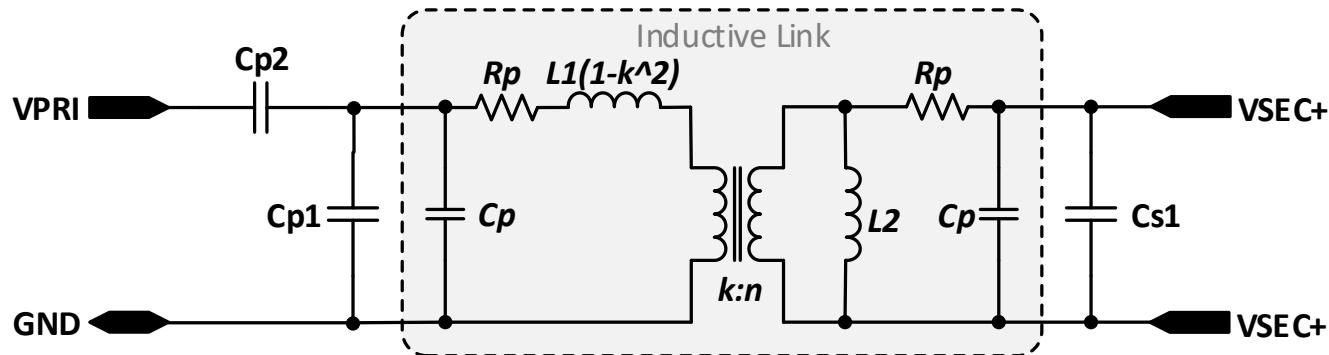
| | Schematic | Post-layout |
|------------------|----------------------|----------------------|
| V_{rec} | 2.285 V | 2.217 V |
| ΔV_{rec} | 2.4 mV _{pp} | 3.6 mV _{pp} |
| V_{reg} | 1.780 V | 1.781 V |
| ΔV_{reg} | 0.1 mV _{pp} | 0.5 mV _{pp} |
| η_{pms} | 58.9 % | 62.7 % |

- 20 mV decrease in V_{reg}, pad resistance*I_{load}
- Increased η_{pms} in post layout
- Reduced I_{rms} and V_{rec}

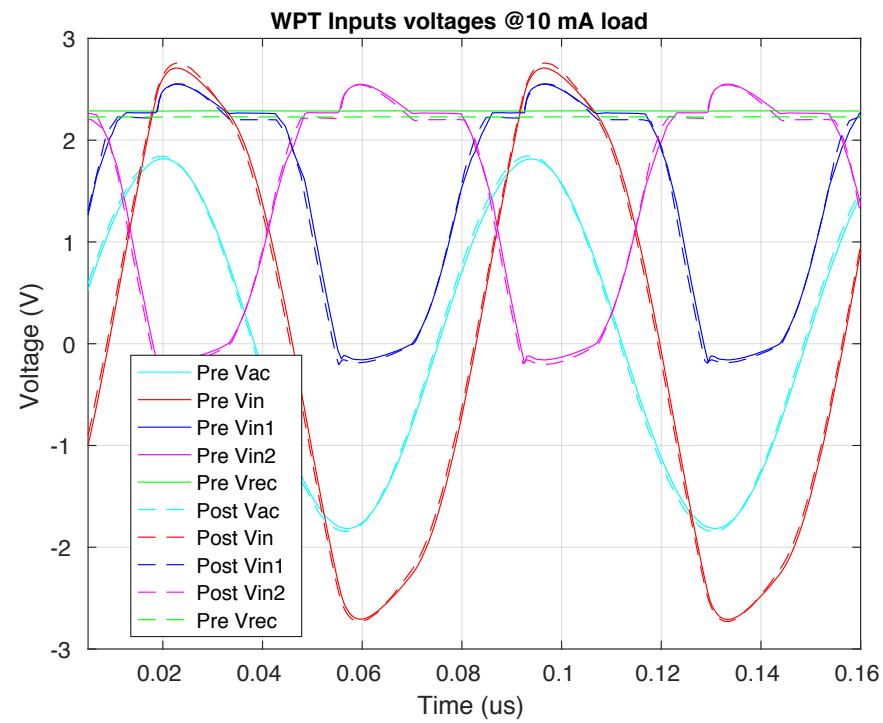
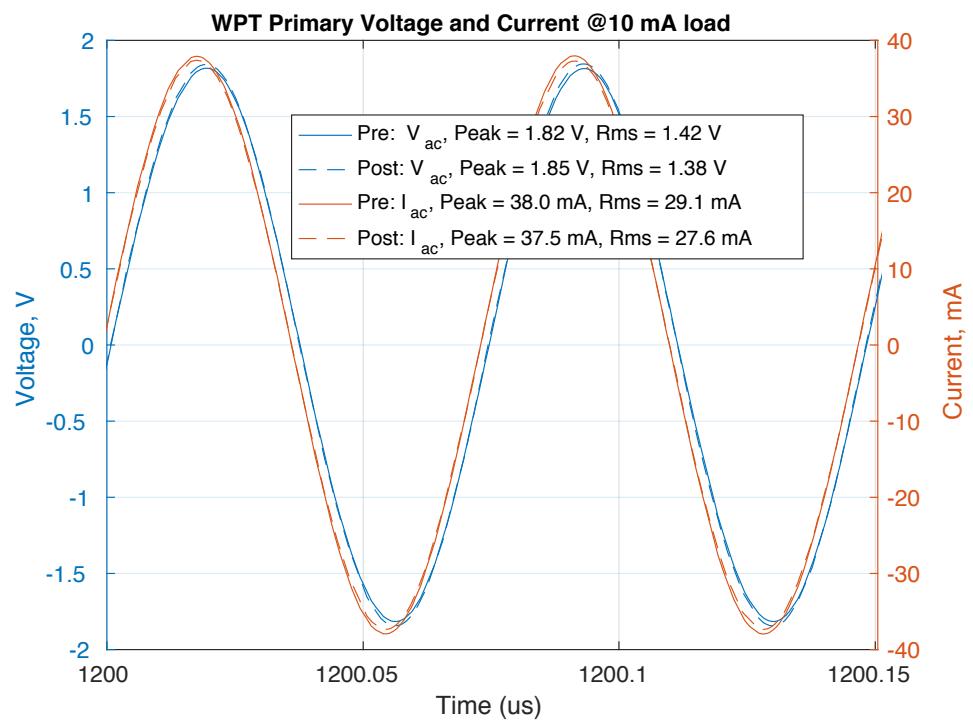
WPT System: Test bench



- PMS + Transfer Link
- Replace balun in PMS test bench with *resonance inductive link* model below
- L1, L2 and k from HFSS model
- Cp1, Cp2 and Cs1 from ADS tuning
- Gradually increased Vac till Vin1/Vin2 are 2.6 V



WPT System: Transfer Link



WPT System: Performance

Table 6.3: WPT performance summary for 5 mm coupling

| | Schematic | Post-layout |
|------------------|----------------------|----------------------|
| V_{ac} | 3.7 V | 3.7 V |
| V_{rec} | 2.287 V | 2.229 V |
| ΔV_{rec} | 3 mV _{pp} | 2.8 mV _{pp} |
| V_{reg} | 1.780 V | 1.781 V |
| ΔV_{reg} | 0.1 mV _{pp} | 0.5 mV _{pp} |
| η_{wpt} | 48 % | 50.6 % |

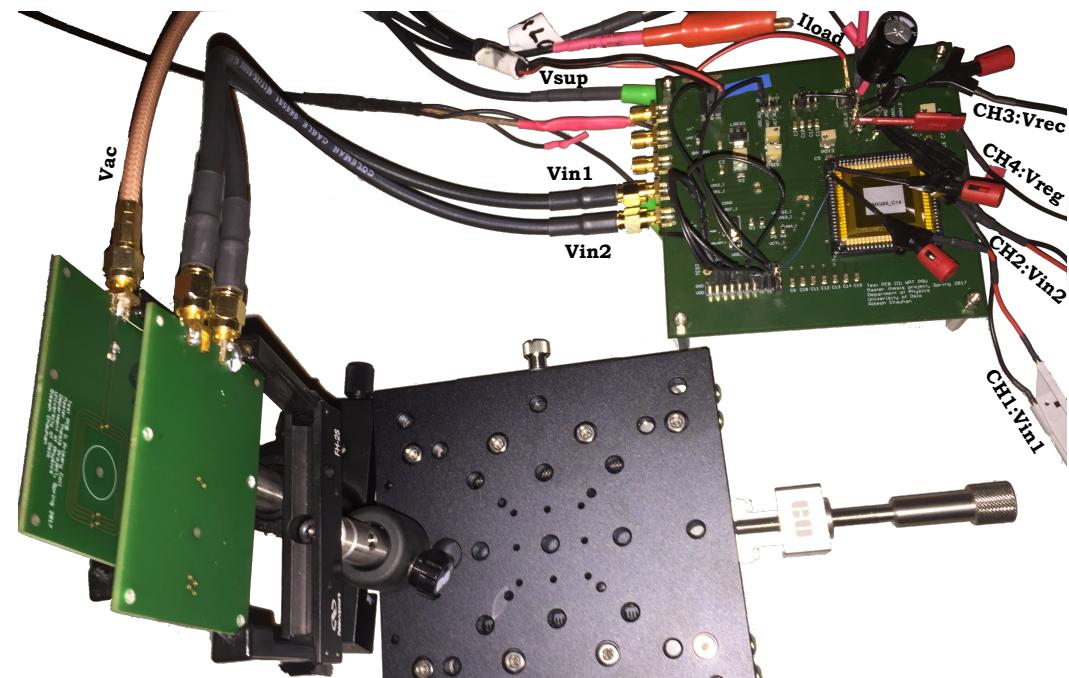
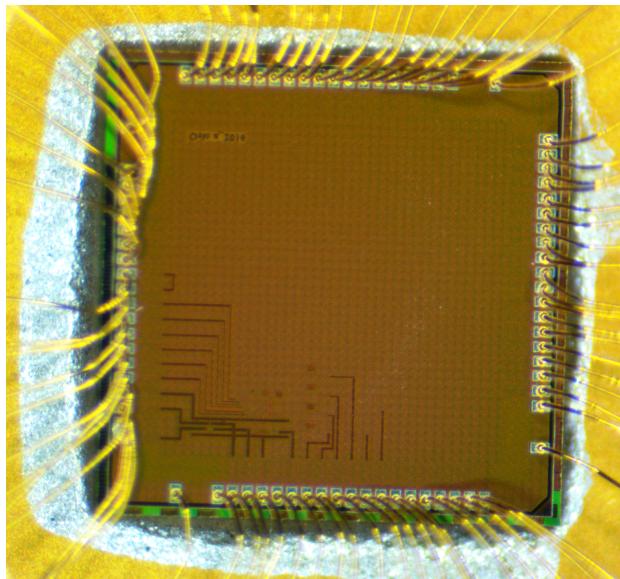
Table 6.4: WPT performance summary for all inductive link

| | Sepr: 1.5 mm | Sepr: 5 mm | Sepr:10 mm |
|--------------|---------------------|-------------------|-------------------|
| k | 0.52 | 0.25 | 0.1 |
| V_{ac} | 3.6 V | 3.7 V | 4.7 V |
| I_{peak} | 41.2 mA | 37.5 mA | 39.2 mA |
| P_{in} | 32.8 mW | 35.2 mW | 51 mW |
| η_{wpt} | 54.3 % | 50.6 % | 34.9 % |

- PMS in WPT same as in PMS only
- $\eta_{wpt} = \eta_{link} * \eta_{rect} * \eta_{ldo}$ is slightly greater (57.8 % for 5mm)
- Increasing separation, decreasing k , decreasing η_{wpt}

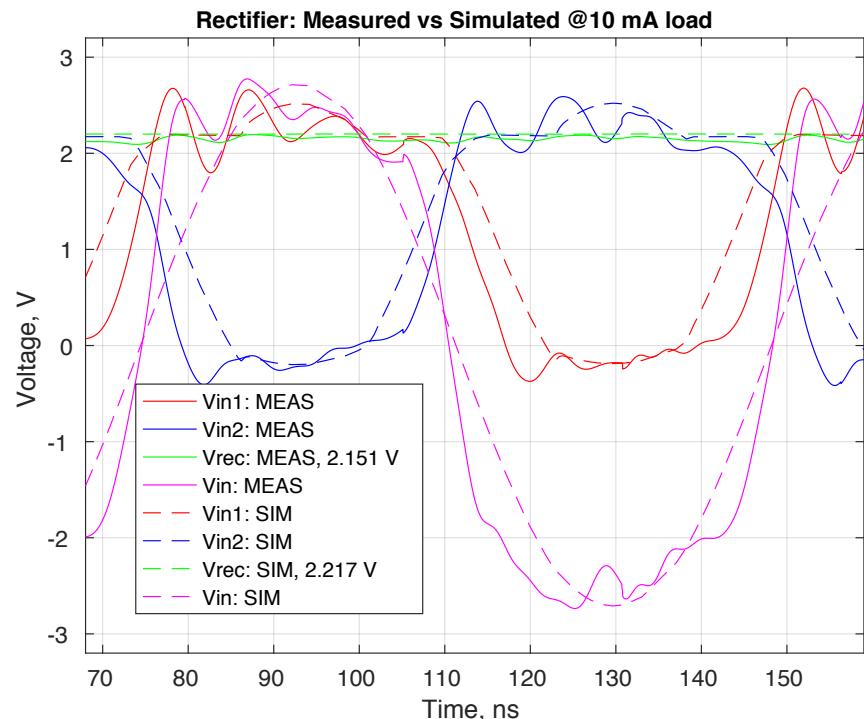
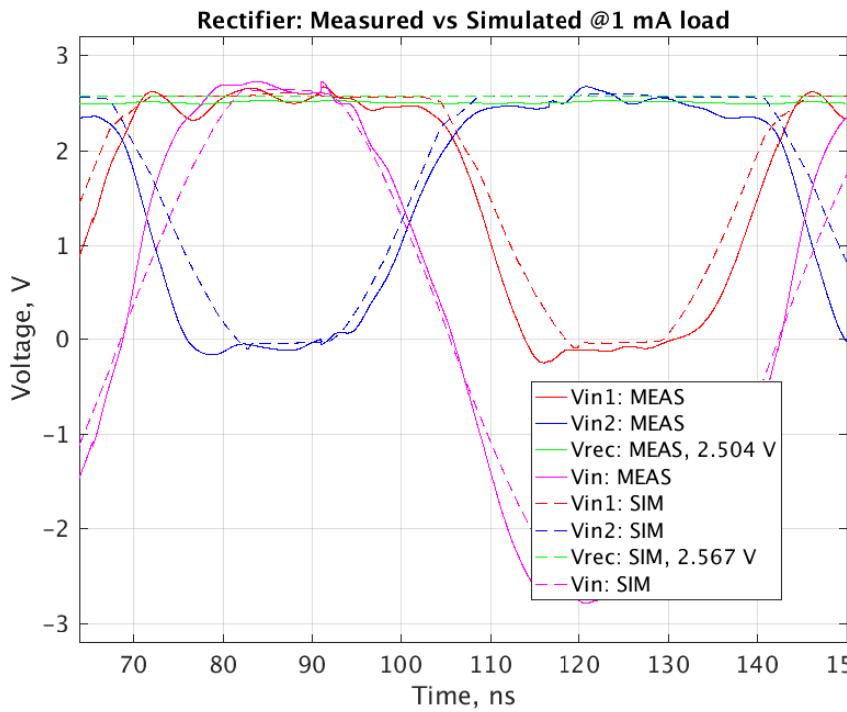
Measurements: Lab Setup

- PMS Chip: CMOS 90nm 1P-9M
- PCBs: Test board, Primary and Secondary
- TGA 1244, Agilent 54624A, Agilent E3648A, Keithley 6514
- Matlab: control and process data



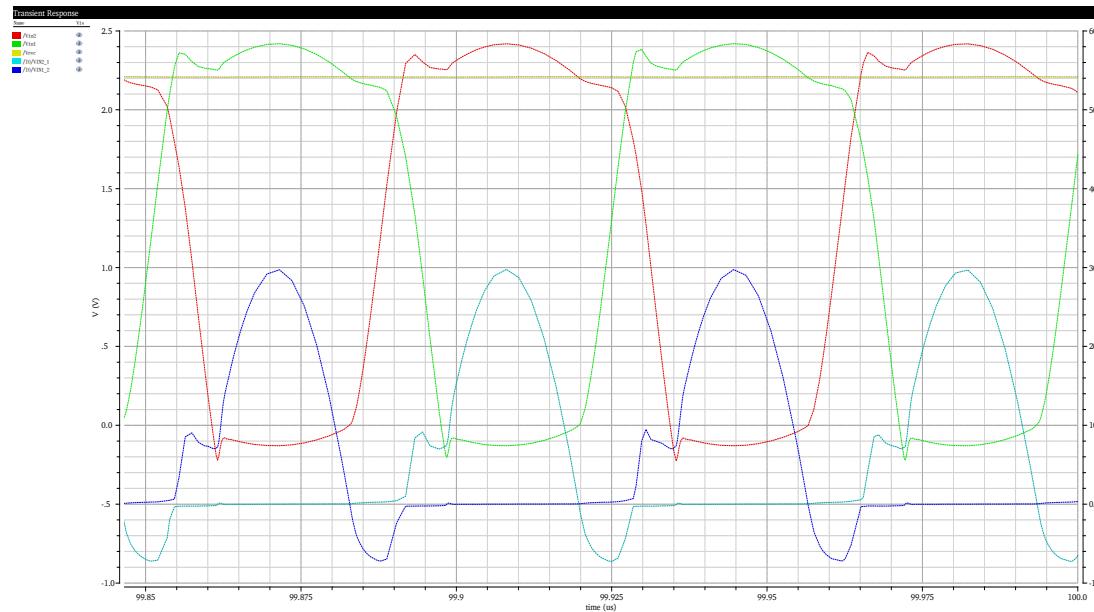
Measurements: Rectifier

- On-board balun for Vin1 and Vin2
- Potentiometer as load at Vrec
- Disable LDO(!)
- Drop in Vrec: bonding wire + PCB trace (+LDO conduction)
- Vin1 and Vin2 distorted



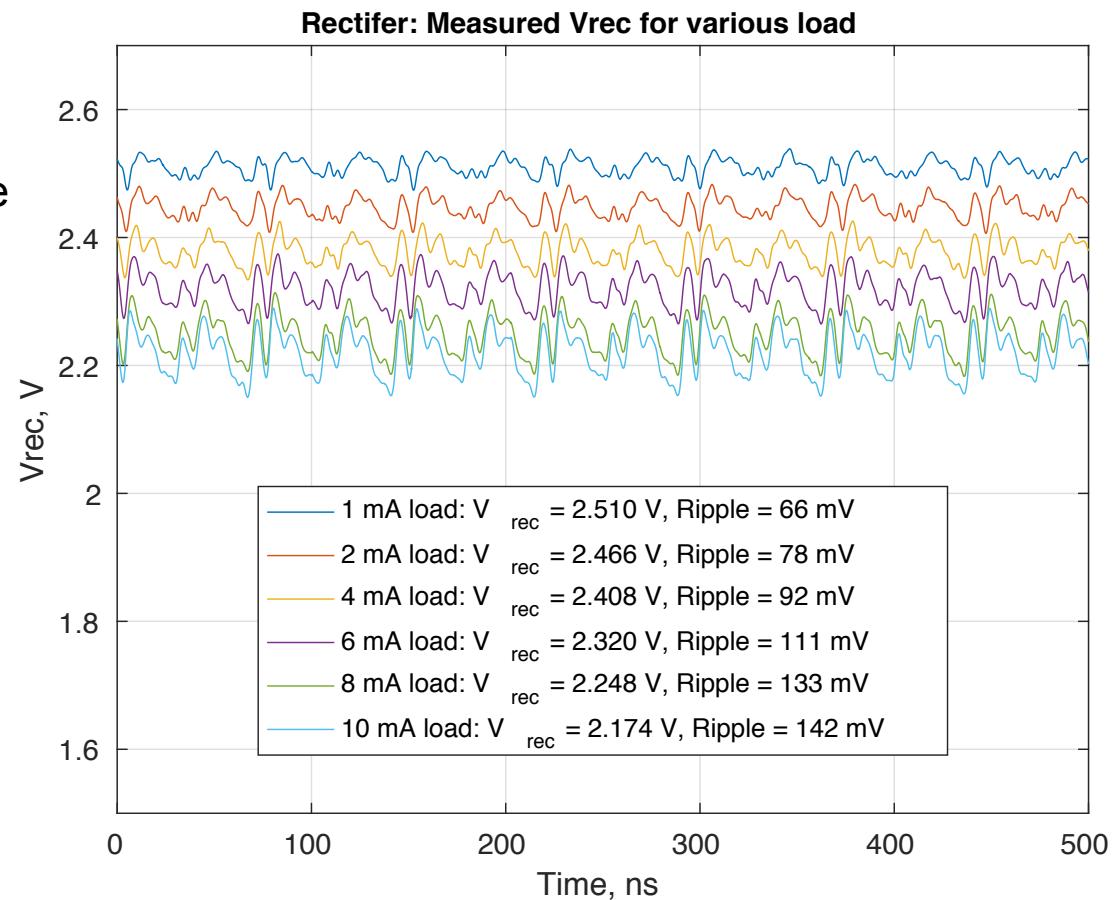
Measurements: Vin1 Vin2 distortion, why?

- Vin1 and Vin2 have peak and valley when diode is turning on and off
- How: parasitic inductance and capacitance @ HF
- Where:
 - Inductance : bonding wire + pcb trace
 - Capacitance: probe + pad
- Effect: Multiple conduction + large reverse leakage



Measurements: Rectifier with various load

- Large ripples, increasing with heavier load
- Ripple frequency ≈ 35 MHz, more than twice input
- Parasitic effect
 - Multiple conduction
 - Large reverse leakage
- Substrate contacts
- Capacitive coupling
 - V_{rec} over V_{in1} and V_{in2} in layout



Measurements: Rectifier performance

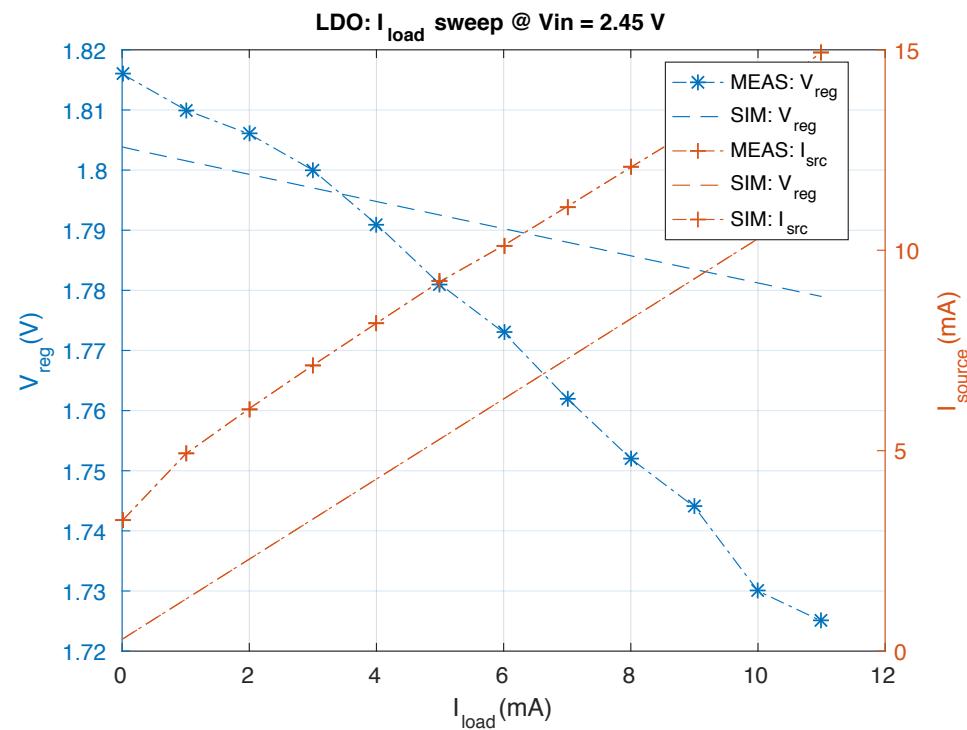
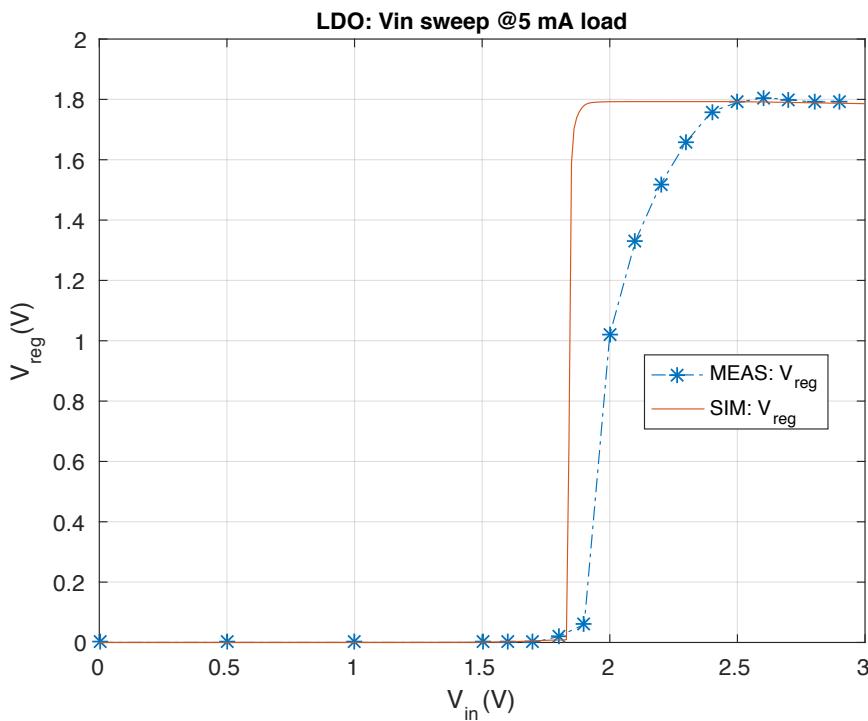
Table 7.1: Rectifier measured performance

| | Measured | Post-layout |
|-----------------|-----------------|--------------------|
| Input magnitude | 2.6 V | 2.65 V |
| Rectified DC | 2.17 V | 2.285 V |
| Ripple Vpp | 142 mV | 4 mV |
| PCE | 64.4 % | 80.5 % |
| VCE | 80.4 % | 87.8 % |

- VCE good, PCE reduced
- Input current, use of series current sense resistor
- Pin: time integral of product of instantaneous input voltage and current average over that time

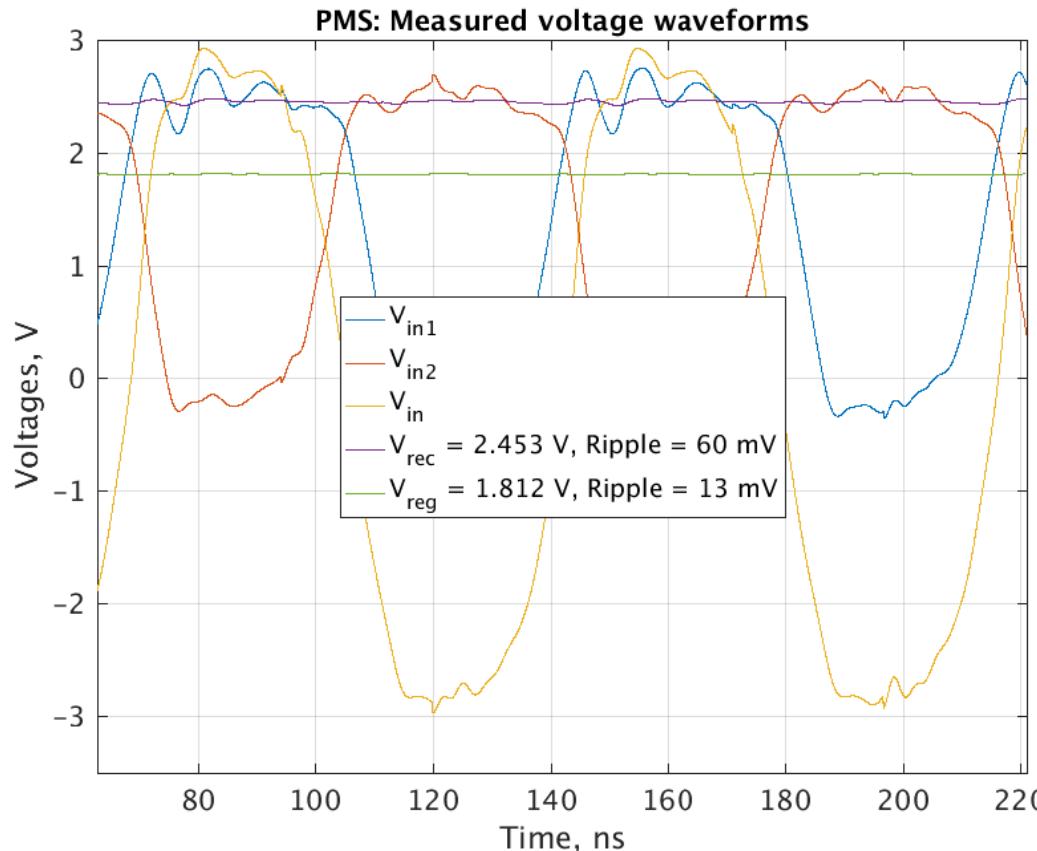
Measurements: LDO

- On-board Vref and biases
- Potentiometer as load at Vreg
- Disable rectifier(!)
- Minimum Vin ≈ 2.45 V
- Current offset 4 mA, are diodes really off?



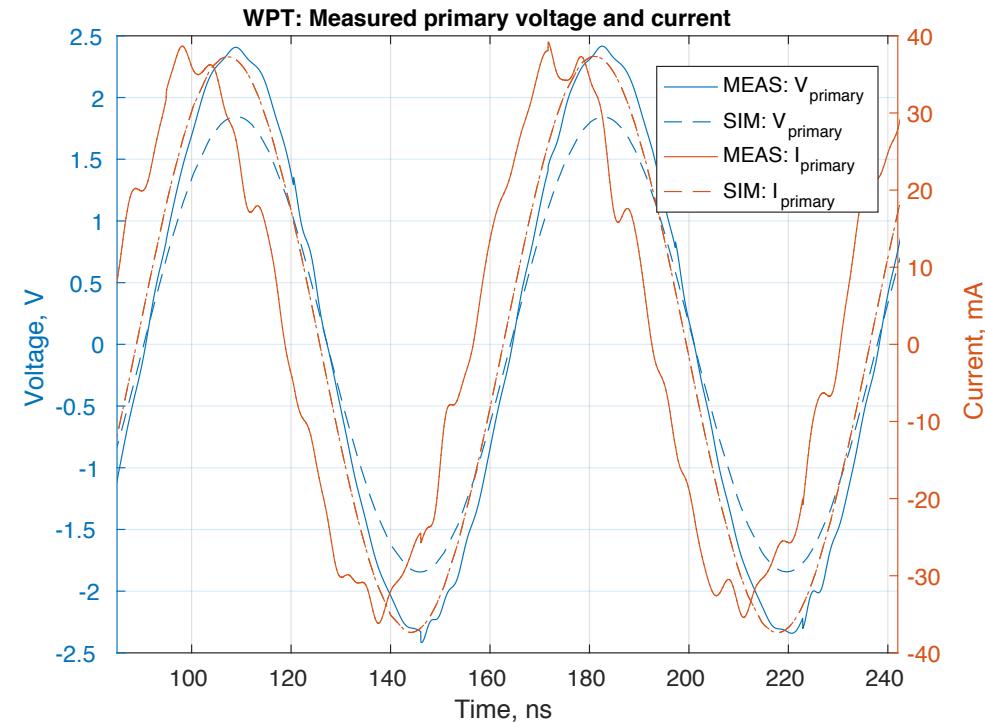
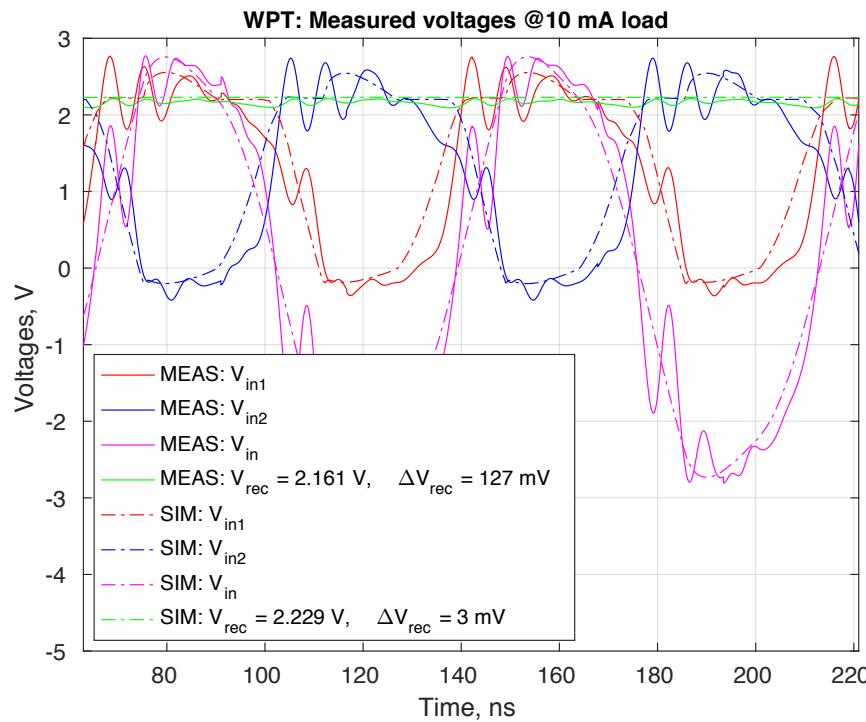
Measurements: PMS

- Minimum $V_{in} \approx 2.45$ V i.e. for 2 mA load
- But for 10 mA load, $V_{rec} = 2.17$ V
- PMS with LDO sanity check only, rectifier only as PMS ahead



Measurements: WPT 5mm coupling

- Resonant primary aligned over resonant secondary at 5 mm
- Potentiometer as load at Vrec
- Primary current lags more in phase with voltage



Measurements: WPT 5mm coupling performance

Table 7.2: WPT measured performance for 5 mm coupling

| | Measured | Post-layout |
|------------------|----------------------|----------------------|
| V_{ac} | 3.8 V | 3.6 V |
| V_{rec} | 2.1 V | 2.23 V |
| ΔV_{rec} | 113 mV _{pp} | 2.8 mV _{pp} |
| η_{wpt} | 46.1 % | 63.4 % |

- Decreased measured η_{wpt}
 - Parasitic affect in rectifier inputs
 - Non-optimal resonance
 - Load variation, rectifier non-linear load
 - Separation distance inaccuracy
 - Misalignment

Measurements: WPT all coupling performance

- Increase coupling distance, less loading to primary, less current, higher input voltage
- 10 mm distance almost open load, very weak coupling
- Weak coupling: link optimization should be done together with rectifier and LDO(!), new technique

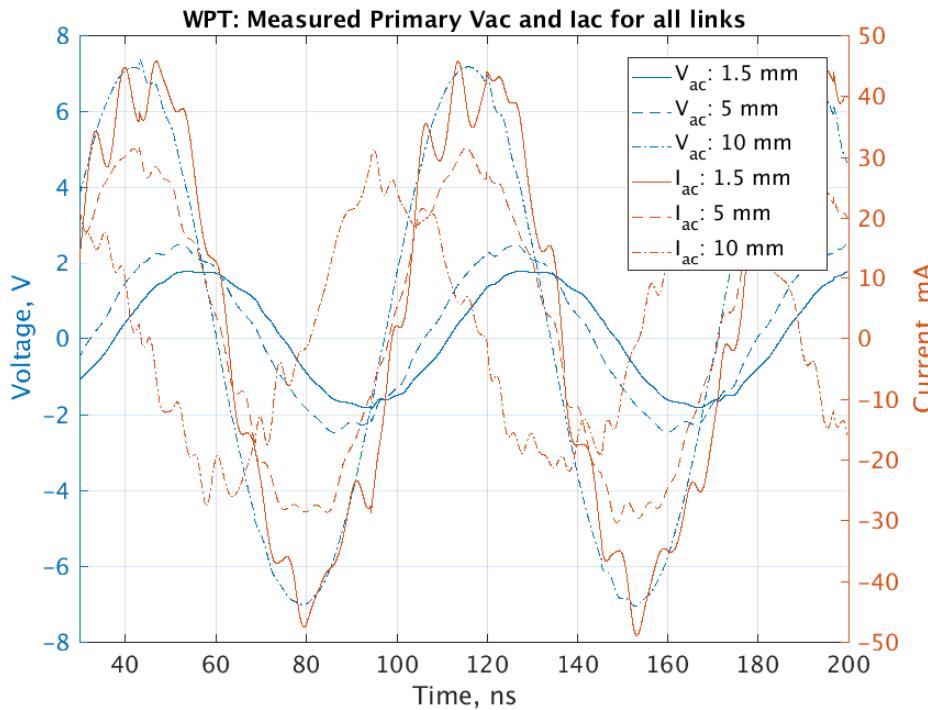


Table 7.3: WPT measured performance for all inductive links

| | Sepr: 1.5 mm | Sepr: 5 mm | Sepr: 10 mm |
|--------------|--------------|------------|-------------|
| V_{ac} | 3.75 V | 3.8 V | 7.8 V |
| I_{peak} | 45.3 mA | 39.2 mA | 28 mA |
| P_{in} | 39.7 mW | 45.6 mW | 99.7 mW |
| η_{wpt} | 52.9% | 46.1 % | 21 % |

Conclusion:

- WPT implementable in 90nm
- Simulation result backed by measurement
- Component architecture and design choices meet the requirements
- Issues mostly on layout
- What can be improved:
 - Device size: chip area, PVT variation
 - Layout: wider guard ring, many substrate contacts, separate grounds, even resistive paths, capacitive coupling, large pass device
 - Inductive Link: resonance shift, non-optimal resonance
 - PCB: proper coupling caps, symmetrical traces, test friendly
 - Test bench: inclusion of all parasitic, power down switches
 - Time management: more on layout

Future Works:

- Application specific design:
 - Address the issues first
 - Integrate OVP and BGR
- Independent WPT system
 - PTU
 - Communication and transfer protocol



LDO: Stability

- $p_1(r_{o_pass}, C_{out})$, $p_2(R_{sr}, C_{bp})$, $p_3(R_{o_ea}, C_{gs_pass})$
- $z_1(R_{sr}, C_{out})$
- p_1 dominant, p_2 beyond UGF, p_3 below UGF \Rightarrow unstable
- Suitable R_{sr} and large C_{out} to cancel p_3 with z_1 , left half plane zero

