Fully Integrated Wideband High-Current Rectifiers for Inductively Powered Devices

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***Abstract*—This paper describes the design and implementation of fully integrated rectifiers in BiCMOS and standard CMOS technologies for rectifying an externally generated RF carrier signal in inductively powered wireless devices, such as biomedical implants, radio-frequency identification (RFID) tags, and smart-cards to generate an on-chip dc supply. Various full-wave rectifier topologies and low-power circuit design techniques are employed to decrease substrate leakage current and parasitic components, reduce the possibility of latch-up, and improve power transmission efficiency and high-frequency performance of the rectifier block. These circuits are used in wireless neural stimulating microsystems, fabricated in two processes: the University of Michigan's 3-μm 1M/2P N-epi BiCMOS, and the AMI 1.5-μm 2M/2P N-well standard CMOS. The rectifier areas are 0.12–0.48 mm^2 in the above processes and they are capable of delivering $>$ 25 mW from a receiver coil to the implant circuitry. The performance of these integrated rectifiers has been tested and compared, using carrier signals in 0.1–10-MHz range.**

***Index Terms*—BiCMOS, biomedical implants, CMOS, full-wave, inductive coupling, latch-up, power supply, rectifier, RFID, substrate leakage, telemetry, wireless.**

I. Introduction

FULLY integrated microsystems and systems-on-a-chip (SoCs) are currently hot topics in many branches of microelectronics and MEMS to miniaturize these devices progressively. Biomedical devices are among those applications that receive the most benefits from progress in this area especially when they are intended to be implantable. Some of these wireless implants, which have relaxed size constraints or low-power requirements, like pacemakers, include a dc power source in the form of rechargeable or long-lifetime disposable batteries. Other implants with high power demands such as auditory and visual prostheses need to be powered by magnetic inductive coupling between an extracorporeal transmitter coil and an internal receiver coil, embedded in the implantable device [1]. Transcutaneous electromagnetic power, which is delivered by an externally generated RF magnetic field in the megahertz range, induces a sinusoidal voltage in the receiver inductive-capacitive (*LC*) tank circuit [1]–[3]. The next block should be a wideband rectifier to convert the ac signal to an unregulated dc supply voltage. In many recent biomedical implant designs, the rectifier block is either a hybrid diode bridge [4], [5], which increases the size of the implant, or an inefficient half-wave rectifier using the substrate or an off-chip diode [6]–[10]. The most important reason behind this fact is the lack of an efficient high-current integrated full-wave rectifier with the following capabilities: to be fast enough to work in the megahertz range, does not dissipate too much power through substrate leakage current and rectifier dropout voltage, and does not increase the risk of latch-up.

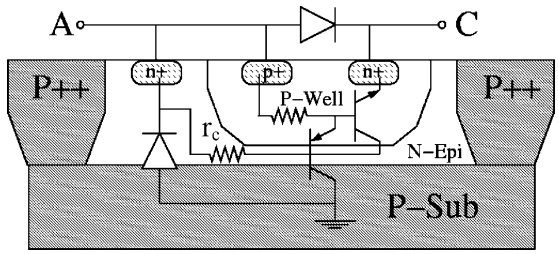

Fig. 1. Cross section of a diode-connected NPN transistor with its parasitics [17].

Low-current integrated full-wave rectifiers are used in wireless sensing and RFID applications [11], [12]. However, they are not studied in detail or employed in high-current applications such as implantable microstimulators with large numbers of stimulating sites [13]–[16]. Designs of several high-current wideband integrated rectifiers are addressed in this paper using CMOS and BiCMOS processes for wireless neural stimulating microsystems [17]. In Section II, diode-connected BJT transistors are characterized in terms of leakage current, and they are used in conventional bridge rectifiers with various topologies in a BiCMOS process. Section III introduces the integrated full-wave bridge rectifiers in a standard CMOS process as well as a new topology for this kind of rectifier in a BiCMOS process with very low risk of latch-up and leakage current. Section IV shows the experimental measurement results as well as a comparison between various rectifiers' performance in an inductive power transmission setup, followed by concluding remarks in Section V.

II. Diode-Connected BJT Transistors

In standard N-epi BiCMOS processes, there is an N^+ buried layer between the N-epi and P-substrate, which reduces the collector parasitic resistance (r_c) in vertical NPN transistors [18], [19]. The effect of r_c can still be significant if a large current passes through the device. There are also BiCMOS processes, such as the MEMS-oriented University of Michigan (UM) BiCMOS process, described in [20], which lack the N^+ buried layer and thereby face some deterioration in the

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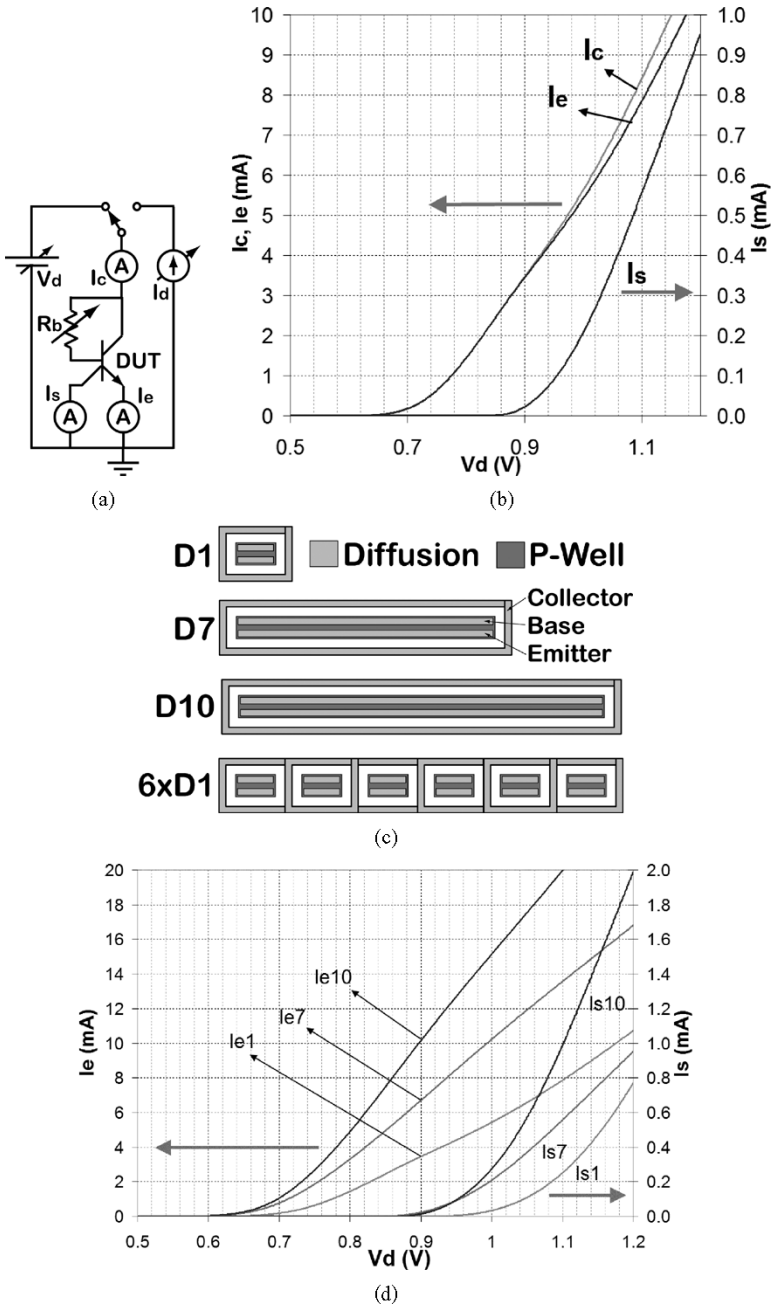


Fig. 2. (a) Substrate leakage current test circuit. (b) Substrate leakage current (I_s) compared to emitter current (I_e) when diode forward bias is increased (c) Diode-connected NPN transistor layouts with different emitter size D1: 7 × 37, D7: 7 × 259, D10: 7 × 370 (μm) (d) The effect of emitter size on substrate leakage current.

performance of the vertical NPN devices. The purpose of this section is to show how to minimize the effects of r_c in diode-connected NPN transistors that are usually used in rectifier bridges [13], [14]. Fig. 1 shows the cross section of a diode-connected NPN transistor in the UM BiCMOS process with its associated parasitic components. The N-epi and P-well are shorted to prevent the parasitic vertical PNP transistor from turning on. However, when the diode is forward biased, base current passes through P-well and turns the original NPN on. This in turn passes some of the diode forward current through the N-epi collector layer, which has a high resistivity under the P-well region (r_c) because of the lack of N^+ buried layer in this process. If the voltage drop across r_c exceeds $|V_{BE}(\text{on})|$, the parasitic vertical PNP transistor turns on, resulting in current leakage from P-well to the grounded P-substrate. The following two methods are proposed to decrease the substrate leakage current without changing the process.

1) Increase the diode-connected NPN geometry: This method puts several of the N-epi distributed resistors in parallel, thus reducing their lumped value (r_c). To show the effect of device geometry, a prototype chip with different emitter size NPN transistors was fabricated. The diode connected minimum-size transistor, called D1, with emitter size of 7 μm× 37 μm, was forward biased as shown in Fig. 2(a). The diode voltage, V_d, was changed from 0.5 to 1.2 V, while measuring I_c, I_e, and substrate leakage current, I_s, using an HP-4155 semiconductor parameter

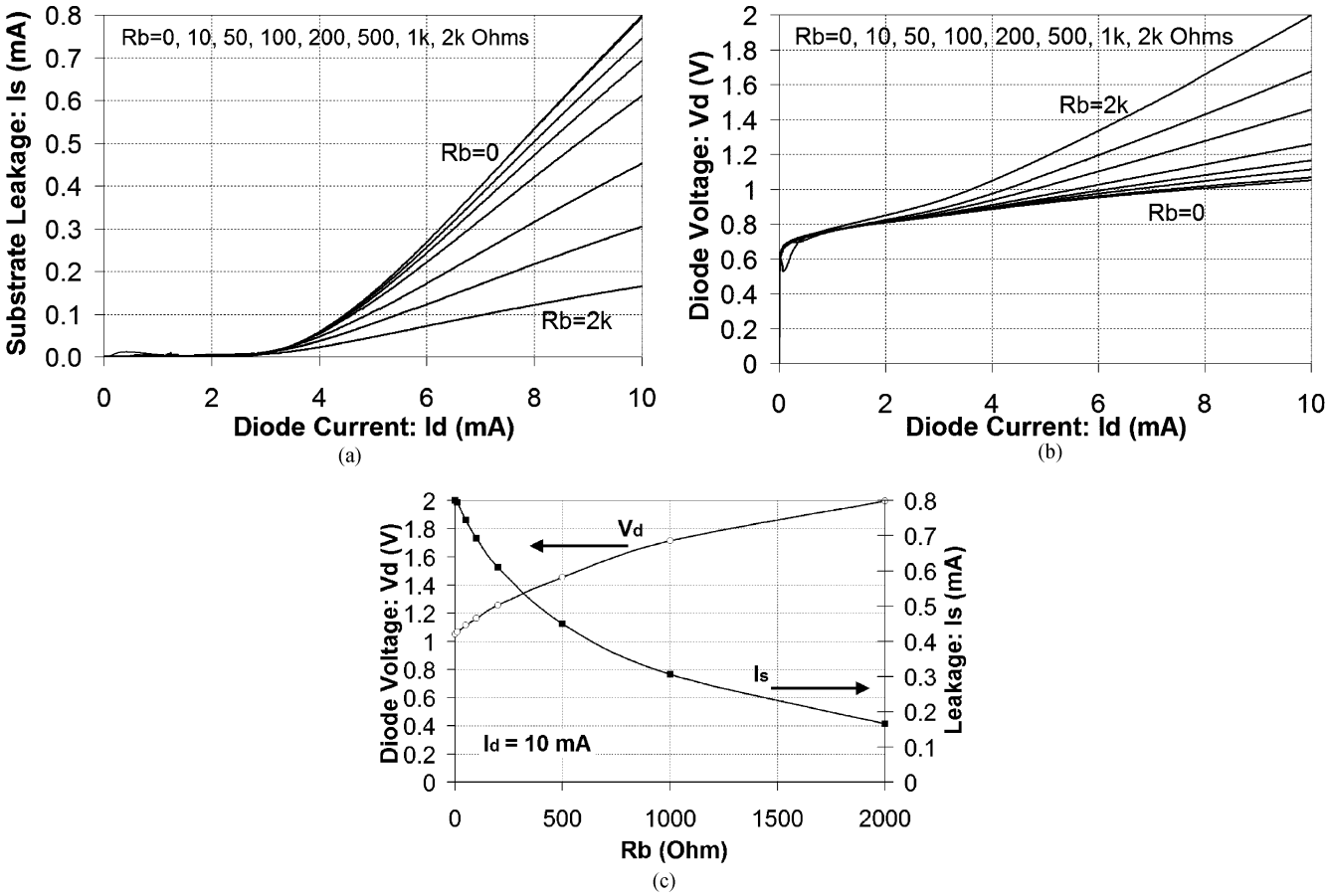


Fig. 3. Effect of base resistance (R_b) on diode-connected NPN when it is changed from 0 to 2 kΩ. (a) Substrate leakage current. (b) Voltage drop across the diode (c) Comparison between the desirable substrate leakage current reduction and undesirable increase in diode voltage drop by increasing R_b when diode current is fixed at 10 mA.

analyzer. The resulting curves in Fig. 2(b) show that I_s becomes significant when $I_d > 3$ mA. However, this current level is not enough for many applications including our wireless neural stimulators [13], [14]. Two other diode-connected NPN transistors, D7 and D10, with emitter areas 7 and 10 times larger than D1, as shown in Fig. 2(c), were tested and compared in a similar fashion. The resulting curves in Fig. 2(d) show that I_{e7} and I_{e10} are only 2–3 times larger than I_{e1} before a significant rise in the substrate leakage. This shows a complex, nonlinear relationship between the diode currents and the emitter area, which is highly dependent on both shape and geometry of the diode-connected NPN [18], [21]. Even though not tested here, it is expected that a layout consisting of six individual D1s [see Fig. 2(c)], which occupies almost the same area as D10, would pass twice as much current without significant substrate leakage.

2) Adding a base resistor: Fig. 1 shows that the base node of the vertical NPN is the emitter node for the parasitic vertical PNP, which is responsible for the substrate leakage. Therefore, one may suggest that adding more base resistance in the leakage current path, while keeping r_c constant in the main current path, can reduce substrate leakage [22]. This hypothesis was tested on D1 by switching to a current source and changing R_b in Fig. 2(a) from 0 to 2 kΩ. Fig. 3(a) shows that the leakage current is decreased significantly especially at higher currents. For example, at $I_d = 10$ mA, I_s is reduced to less than 20% of its initial value, from 0.8 to 0.16 mA as shown in Fig. 3(c). However, the disadvantage of this method is the increase in the diode forward dropout voltage, which is shown in Fig. 3(b). Fig. 3(c) shows that the diode voltage drop increases from 1.05 to 2.0 V when R_b changes from 0 to 2 kΩ at $I_d = 10$ mA. Therefore, even though adding a base resistor saves power in reducing the substrate leakage current, it dissipates more power in the rectifier diodes, and increases the minimum operational coil voltage of the inductively powered device.

A variety of on-chip conventional BJT bridge rectifiers with different topologies, sizes, voltages, and current handling capabilities were fabricated on a rectifier test chip, shown in Fig. 4. In terms of maximum input voltage, designs A, B, and C, which have a single diode in each branch, cannot handle more than 22-V peak input voltage because of the NPN-diode reverse breakdown. Designs D and E have two series diodes in each branch and their reverse breakdown goes beyond 40 V. The disadvantage of the 8-diode full-wave rectifier bridge in design E is its large area consumption. However, in design D the required area is reduced by 50% by using the parasitic N-epi P-substrate diodes (enclosed in dashed boxes) for the returning current path. Even though increasing the emitter area of the diode-connected NPN transistors is the favorable method in decreasing the diode parasitic resistors and leakage current, it increases the parasitic capacitors as well, which degrades

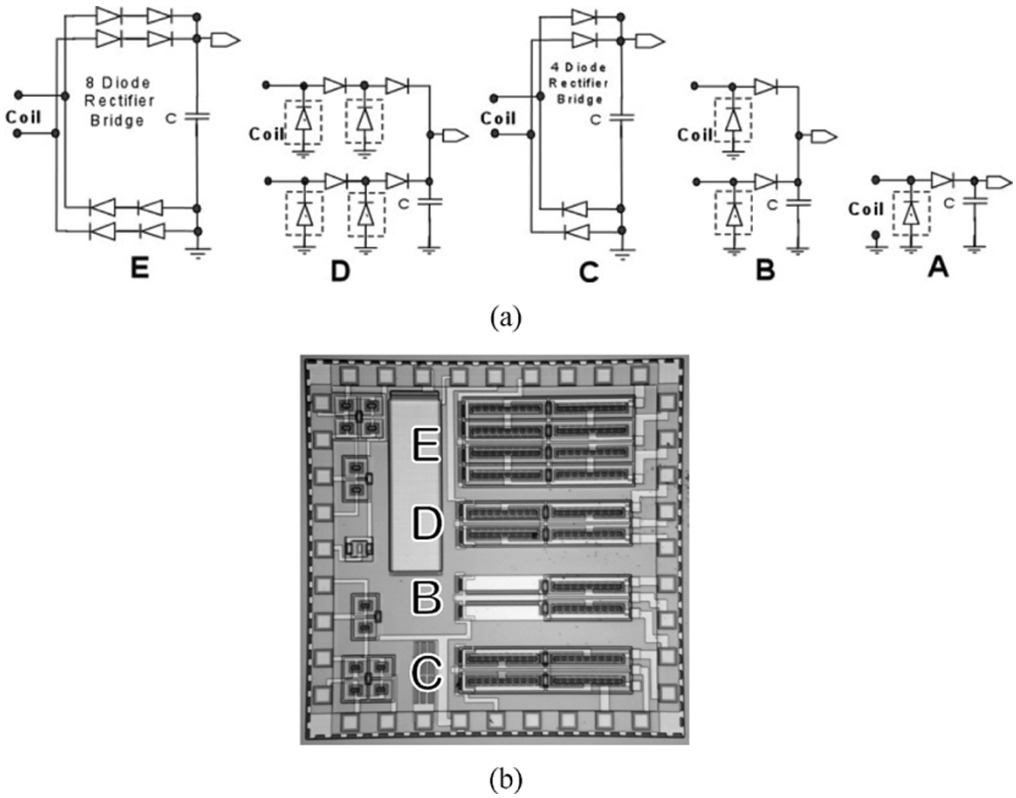


Fig. 4. Conventional BJT bridge rectifiers with different topologies, sizes, voltages, and current handling capabilities on a rectifier test chip (die size 2×2 mm^2).

the high-frequency performance of the rectifier. Therefore, the optimum rectifier topology, size, and layout in each BiCMOS process should be defined based on the rectifier operating frequency and its peak current by compromising between the resistive and capacitive parasitic components.

III. CMOS Bridge Rectifiers

To eliminate substrate leakage current associated with the BJT diodes, described in Section II, diode-connected MOS transistors can be used to form a CMOS full-wave bridge rectifier as shown in Fig. 5(a). Perhaps a greater advantage of these rectifiers is their compatibility with standard CMOS process, which is more popular and cost effective than BiCMOS. $\mathrm{M_{P1}}$ and $\mathrm{M_{P2}}$ conduct in the forward direction when the coil voltages (V_{Coil1} and V_{Coil2}) are higher than $V_{\mathrm{out}} + V_{GS}$, while delivering current (I_D) from the coil to the load. I_D passes through the load to the grounded P-substrate and returns back to the coil via $\mathrm{M_{N1}}$, $\mathrm{M_{N2}}$, $\mathrm{Q_1}$, and $\mathrm{Q_2}$.

Reducing the rectifier dropout voltage decreases power dissipation in the rectifier block and increases the average rectified dc voltage (V_{out}) available at the regulator input. This lowers the minimum operational receiver coil voltage, which in turn saves the required transmitted power significantly or increases the maximum permissible coupling distance between the transmitter and receiver coils. The instantaneous voltage drop on a diode-connected MOS transistor with drain current I_D can be found from

$$|V_{GS}| = |V_{DS}| = |V_{TH}| + \sqrt{\frac{2I_D}{\mu C_{ox}\,(W/L)}} \qquad (1)$$

where V_{TH} is the MOS threshold voltage, μC_{ox} is the intrinsic transconductance, and W and L are the transistor width and length, respectively. In the above equation, V_{TH} is a process-dependent parameter, which can be minimized in the circuit design by eliminating the body effect. To minimize the second term in (1), the W/L ratio should be increased as much as the rectifier area consumption and its parasitic capacitance will permit.

Since the source nodes of the rectifying pMOS transistors in Fig. 5(a) are connected to the coil terminals, which have large voltage variations at high frequency, protecting this circuit against latch-up and substrate leakage is crucial. The separated N-wells are the nodes that increase the risk of substrate leakage current by turning on the parasitic vertical PNP transistors unless their potentials are properly controlled. To dynamically control each separated N-well voltage, two auxiliary pMOS transistors are added to each rectifying pMOS to connect the N-well to V_{out} or the coil terminal whichever is at a higher potential. The resulting rectifier circuit schematic is shown in Fig. 5(a) along with half of its symmetrical cross section in Fig. 5(b), which demonstrates the diode-connected pMOS complex, the nMOS switch, and parasitic PNP transistors and diodes. The source-side auxiliary pMOS ($\mathrm{M_{P3}}$) shares its source and gate terminals with the diode-connected $\mathrm{M_{P1}}$ and turns on whenever $\mathrm{M_{P1}}$ is on, while connecting the separated N-well to V_{Coil1}, which is higher than $V_{\mathrm{out}} + V_{GS1}$ at this time. The drain-side auxiliary pMOS ($\mathrm{M_{P4}}$) shares its drain terminal with $\mathrm{M_{P1}}$ and turns on whenever V_{Coil1} is less than V_{out} by at least $|V_{THp}|$, while connecting the separated N-well to V_{out}. Since no current passes through auxiliary MOSFETs when they turn on, their drain-source voltage is close to zero. Therefore, they prevent the parasitic vertical PNP transistors

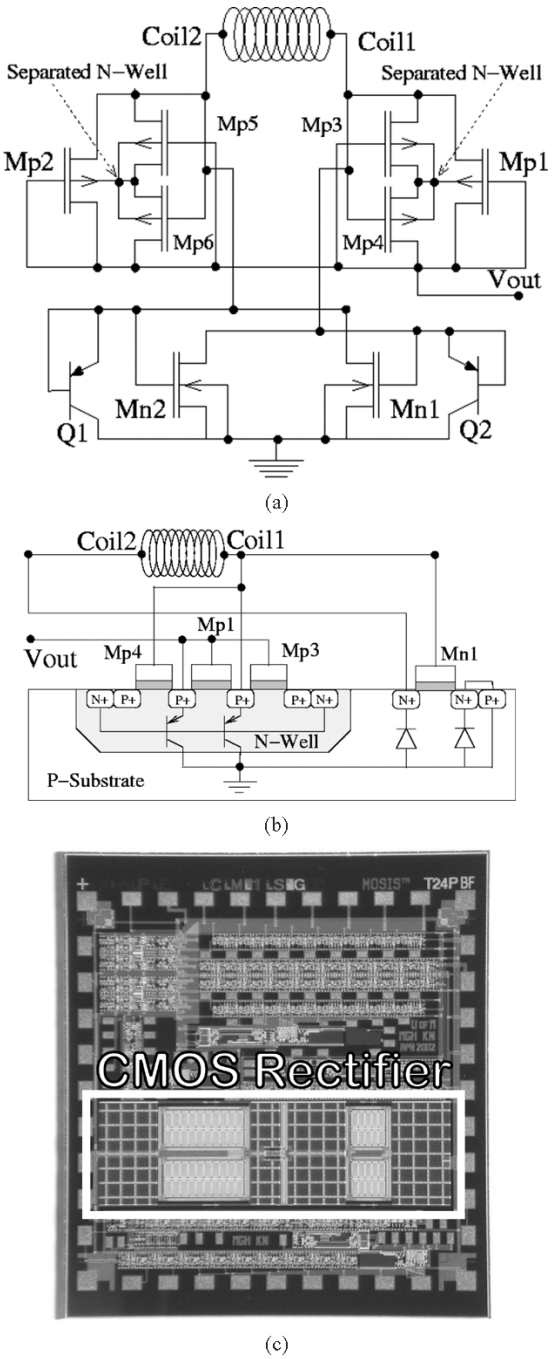


Fig. 5. (a) Schematic diagram of the standard CMOS full-wave rectifier. (b) Cross section of half of the CMOS rectifier showing the diode-connected pMOS complex and parasitic transistors and diodes. (c) Photomicrograph of the prototype CMOS rectifier implemented in 1.5-μm N-well standard CMOS process (die size: 2.2 × 2.2 mm^2, rectifier + capacitor size: 2 × 0.58 mm^2).

from turning on and leave little chance for latch-up or any leakage to the substrate. Even if $|V_{THp}| > |V_{BE}(\text{on})|$ and $V_{\text{out}}+|V_{THp}| > V_{\text{Coil1}} > V_{\text{out}}+|V_{BE}(\text{on})|$, which happens in a small fraction of a cycle, since M_{P3} and M_{P4} start conducting in the subthreshold region, they rapidly adjust the floating N-well potential and do not allow the parasitic PNP transistors to turn on. Another advantage of this configuration, which is also used in charge pumps [23], is eliminating the body effect on the rectifying pMOS transistors, thus reducing the rectifier dropout voltage and power dissipation according to (1).

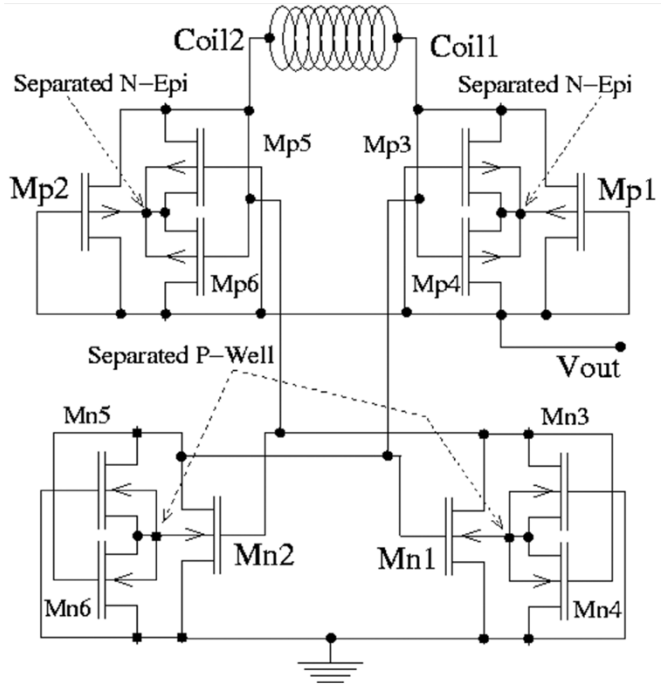
On the nMOS transistor side of Fig. 5(b), when $V_{\text{Coil2}} < -V_{THn}$, the P-substrate to drain N^+ diffusion parasitic diode starts conducting shortly before or after M_{N1}, depending on V_{THn}, and desirably helps M_{N1} to return current (I_D) from the P-substrate to the coil. To facilitate this effect, the M_{N1} drain area can be extended. Another option is adding individual diodes in parallel to M_{N1} and M_{N2}. Many standard CMOS processes have models for common-collector vertical PNP transistors in their libraries, because these devices are used in prevalent circuits such as bandgap references. Therefore, to facilitate simulations, vertical PNP transistors were used in parallel to M_{N1} and M_{N2}, as shown in Fig. 5(a), even though their P^+ emitters are not involved. Fig. 5(c) shows a photomicrograph of the CMOS rectifier that is implemented in the AMI 1.5-μm standard CMOS process, and includes a 250-pF ripple rejection low-pass capacitive filter as well. To decrease the risk of latch-up even further, the pMOS complexes and the nMOS pair are widely separated in the layout and protected by N^+ and P^+ guard rings, respectively [19].

Implementation of the CMOS rectifier in the UM BiCMOS process is slightly different because the N-epi layer on top of the P-substrate generates more parasitic components. Therefore, both nMOS and pMOS transistor pairs have to be separated from the rest of the circuits, and equipped with auxiliary MOSFETs to prevent leakage current and latch-up. Fig. 6 shows the new CMOS rectifier schematic, a cross section of half of its symmetrical structure, demonstrating the nMOS and diode-connected pMOS complexes, and a fabricated prototype. Even though no bipolar transistors are used in this circuit, hereafter we call this rectifier BiCMOS to differentiate it from the standard CMOS version that was described earlier. The role of M_{P3} and M_{P4} in Fig. 6(b) is similar to Fig. 5(b), which is connecting the separated N-epi to the higher of either V_{out} or coil voltages. M_{N3} and M_{N4} dynamically control the separated P-well potential and connect it to the lower of either ground or coil voltages. This is shown in the simulated waveforms of Fig. 7(a). The uppermost trace is V_{Coil1}, and the lowermost trace is the rectifier output (V_{out}). The other two traces show how separated N-epi and separated P-well potentials follow $\max(V_{\text{out}}, V_{\text{Coil1}})$ and $\min(GND, V_{\text{Coil2}})$, respectively. Fig. 7(b) shows measured V_{Coil1}, separated N-epi potential, and V_{out} waveforms on the prototype BiCMOS rectifier of Fig. 6(c), when it is connected to a 1-kΩ load. Fig. 7(c) shows the same waveforms superimposed to demonstrate their relative amplitudes.

At high frequencies, parasitic capacitors should be considered as a limiting factor to the size of the rectifier MOSFETs. However, in an inductively powered device, such as the one shown in Fig. 8(a), most of these capacitors are lumped as C_{in} and C_{out} in parallel with the receiver L_rC_r-tank circuit, and the rectifier capacitive ripple rejection filter (C_{LP}), which is connected between the rectifier output and ground terminals, respectively. Therefore, the most significant effect of these parasitic capacitors is adding to C_r and C_{LP}, which can be accounted for in the design phase or adjusted for after fabrication by trimming provisions.

IV. Experimental Results

Fig. 8(a) shows the experimental inductive power transmission setup that was used to evaluate and compare the performance of four full-wave rectifier bridges: a discrete rectifier



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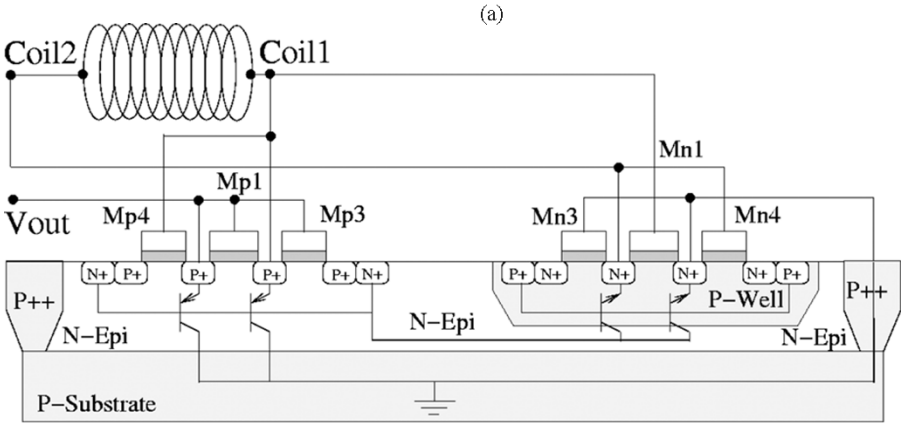

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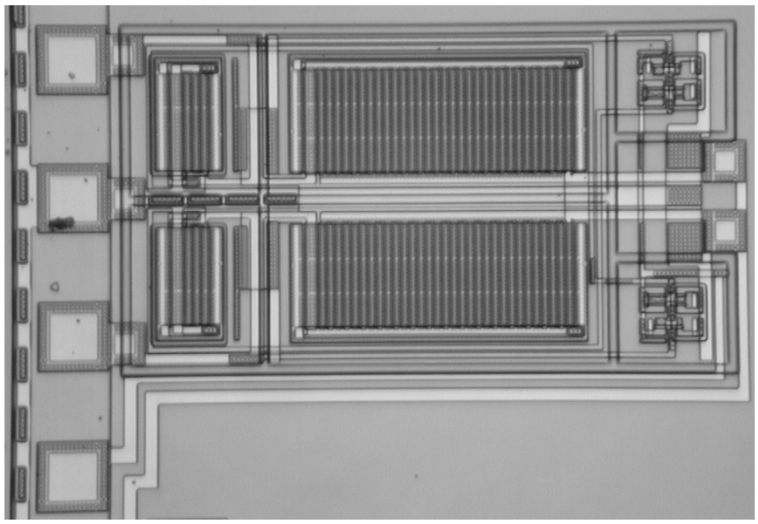
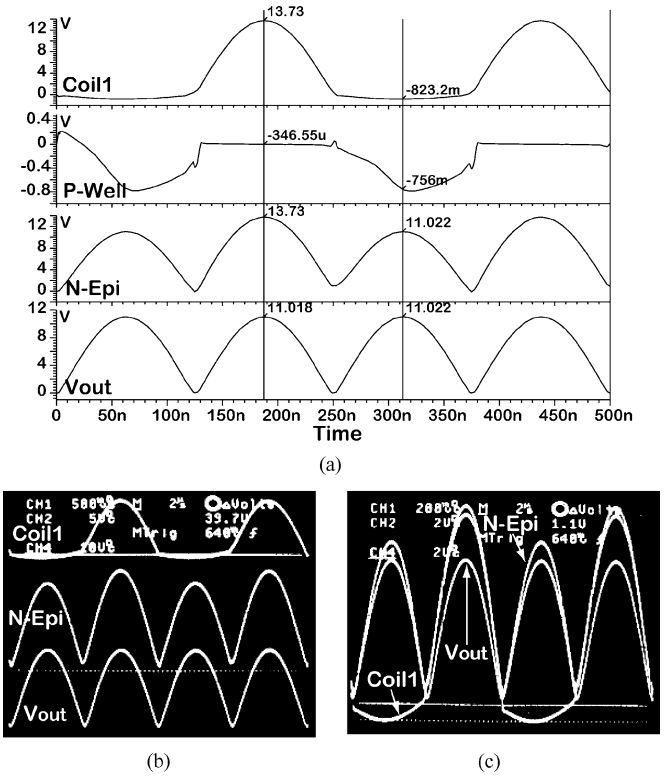


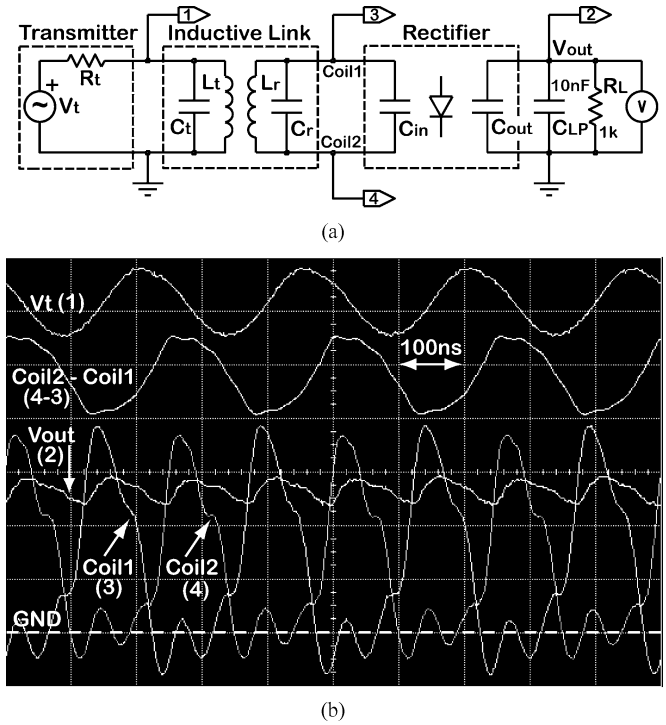
(c)

Fig. 6. (a) Schematic diagram of the BiCMOS full-wave rectifier implemented in the 3-μm N-epi P-well UM BiCMOS process. (b) Cross section of half of the symmetrical structure showing the nMOS and pMOS complexes and parasitic BJTs. (c) A prototype BiCMOS rectifier (size: 0.5×0.73 mm^2) [17].



(a) (b) (c)

Fig. 7. Simulation and measured waveforms when the BiCMOS rectifier is loaded with a 1-kΩ resistor. (a) Simulation waveforms from top: one of the coil input voltages, separated P-well voltage, separated N-epi voltage, and rectified output voltage. (b) Measured waveforms from top: Coil input, separated N-epi, and output voltage. (c) Similar measured waveforms superimposed to show their relative amplitudes [2 μs/div].



(a) (b)

Fig. 8. (a) Rectifier test setup. (b) Sample measured waveform at probing points using the standard CMOS rectifier at 4 MHz: (1) transformer primary voltage; (2) rectified dc output; (3, 4) transformer secondary nodes voltage versus ground (4–3) transformer secondary differential voltage.

made of 1N4148 diodes as a reference [24], standard CMOS (Fig. 5), UM BiCMOS (Fig. 6), and diode-connected UM BJT [Fig. 4(c)]. In these experiments, the wireless link is not tuned to any particular frequency, and all the capacitors except C_{LP} are parasitic. This is to see the effect of rectifiers' parasitic capacitors, such as $C_{\rm in}$ and $C_{\rm out}$, on the overall frequency response. A sample measured waveform using the standard CMOS rectifier at 4 MHz is shown in Fig. 8(b), which also indicates the probing points. The upper trace is the 4-MHz sinusoidal carrier at the transmitter output. The second trace is the differentially measured waveform across the rectifier inputs ($V_{\rm Coil2} - V_{\rm Coil1}$), which single-ended waveforms ($V_{\rm Coil1}$ and $V_{\rm Coil2}$) are also shown on the lower traces, superimposed on $V_{\rm out}$ to demonstrate their relative magnitudes. It should be noted that the external C_{LP} (10 nF) was not included in this measurement to observe the ripple rejection capability of the on-chip 250-pF capacitive filter [Fig. 5(c)].

In the first experiment, a wideband isolation transformer (0016PA – North Hills signal processing with 20-Hz–20-MHz bandwidth) was used as the inductive link to eliminate the effect of the link frequency response on the rectifier characteristics by providing a flat passband. Fig. 9(a) shows the average dc voltage measured across $R_L = 1$ kΩ, while keeping the peak to peak voltage across the rectifier inputs ($V_{\rm Coil2} - V_{\rm Coil1}$) constant at 15 V. Despite using a flat-band transformer, the rectifier frequency responses show several peaks and valleys, which are because of the unavoidable parasitic capacitors. In the second experiment, a custom-made air-core transformer, which specifications are provided in Table I, was used as the inductive link and the overall frequency response of the inductive link and rectifier was measured together. Fig. 9(b) shows the average dc voltage measured across R_L, while keeping the transmitter (Agilent 33250A function generator) peak-to-peak voltage (V_t) constant at 18 V. Since the sole purpose of these experiments is to compare the performance of the above four rectifiers regardless of their applications, they were not tuned, and everything out of the rectifier dashed box in Fig. 8(a) was kept the same. Therefore, variations in the frequency responses are only due to the rectifiers dropout voltages and their parasitic capacitors. In a real application, usually both transmitter and receiver tank circuits are tuned at the carrier frequency by adding external capacitors, which will dominate the parasitic ones. Examples of tuned inductive links can be found in [1], [3], and [25].

TABLE I
AIR-CORE TRANSFORMER SPECIFICATIONS

Parameter	Value (primary / secondary)
Wire size including plastic coating	∅ 1.5 mm (24-AWG)
Number of turns	50 / 50
Solenoid diameter (cm)	2.3 / 2.6
Solenoid length (cm)	7.5 / 7.5
Open circuit parallel RLC equivalent	
R (kΩ)	17.9 / 20.5
L (μH)	16.7 / 19.7
C (pF)	49 / 42

Table II summarizes some of the integrated rectifier specifications. From the measured results, it can be concluded that all

TABLE II
RECTIFIERS SPECIFICATIONS

Type	Area (mm^2)	Breakdown Voltage (V)	Transistor Size W/L (μm)	Average DC output (V) from 1 to 10MHz
1N4148SW	12	75	2300×1200*	7.18
Standard CMOS	0.48	15	4800 / 1.6	6.54
UM-BiCMOS	0.24	22	4659 / 3	5.23
UM-BJT**	0.37	22	7×370***	4.80

* Size of the ultra-small surface-mount package [24].
** Fig. 4(c) with D10 diodes.
*** Size of the emitter.

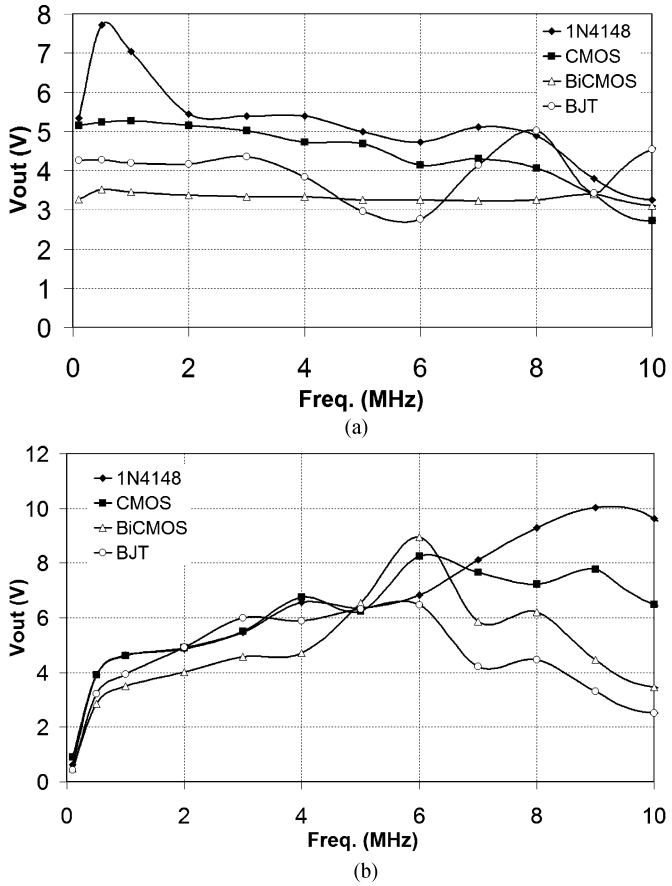


Fig. 9. (a) Rectifiers frequency response with a flat-band inductive link and 15-V constant peak-to-peak input voltage. (b) Rectifiers and inductive link overall frequency response with 18-V constant transmitter peak-to-peak voltage.

of the IC rectifiers that are discussed in this paper can provide high enough dc voltage for an on-chip 5-V regulated supply in a certain frequency range, while delivering 25 mW to the rest of the microsystem. The standard CMOS rectifier has the best performance, close to a discrete full-wave rectifier bridge, even though it occupies only 4% of the discrete rectifier real estate. The high performance of the CMOS rectifier is due to insignificant leakage current and lower dropout voltage compared to the other versions. We believe that the poor performance of the BiCMOS rectifier compared to the standard CMOS is due to the lower transconductance and higher threshold voltage of the MOSETs in our in-house UM BiCMOS process. In addition, the lower W/L ratio compared to the CMOS version (1553 versus 3000), adds to the rectifier dropout voltage at the same current.

V. CONCLUSION

Several fully integrated rectifiers in BiCMOS and standard CMOS technologies are implemented for rectifying externally generated RF carrier signals in inductively powered wireless devices to generate an on-chip unregulated dc supply. New rectifier topologies and low power circuit design techniques are employed to decrease substrate leakage current and parasitic components, reduce the possibility of latch-up, and improve power transmission efficiency. Increasing the size or adding a base resistor can reduce the diode-connected BJT leakage at high currents, however, a compromise should be made between the parasitic resistor and capacitor values based on the current and frequency ranges in which the rectifier is being used. The body voltage of the diode-connected MOSFETs in the CMOS and BiCMOS rectifiers are dynamically controlled using two auxiliary MOSFETs to eliminate the substrate leakage and body effect. These IC rectifiers, occupying areas in the range of 0.12 to 0.48 mm^2, are fabricated in 3-μm UM BiCMOS and 1.5-μm AMI standard CMOS processes to be used in inductively powered biomedical implants [13]–[17].

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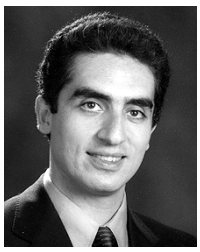

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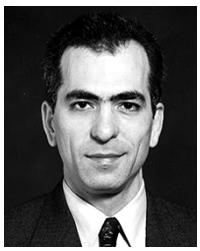

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