A Design of a Wireless Power Receiving Unit With a High-Efficiency 6.78-MHz Active Rectifier Using Shared DLLs for Magnetic-Resonant A4 WP Applications

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***Abstract*— This paper presents a full-CMOS wireless power receiving unit (WPRU) with a high-efficiency 6.78-MHz active rectifier and a dc–dc converter for magnetic-resonant alliance for wireless power (A4WP) applications. The proposed high-efficiency active rectifier with delay-locked loop (DLL) is a highly efficient receiver circuit intended for use in resonant wireless charging applications with a resonant frequency of 6.78 MHz. Each MOSFET of the proposed rectifier is turned on and off based on the ac input voltage. The delay between the ac input current and the ac input voltage due to the delays of internal blocks such as voltage limiter, level shifter, gate driver, and comparator will cause the reverse leakage current, degrading the power efficiency. Thus, the proposed active rectifier adopts the DLL to compensate for the delay caused by internal blocks, which leads to the removal of reverse leakage current and the power efficiency maximization. Moreover, to maximize power efficiency, negative impedance circuit (NIC) is also adopted to minimize switching loss. In the case of dc–dc converter, phase-locked loop is adopted for the constant switching frequency in process, voltage, and temperature (PVT) variation to solve the efficiency reduction problem, especially by heat. This chip is implemented using 0.18 μm BCD technology with an active area of 3.5 mm $\times$ 3.5 mm. When the magnitude of the ac input voltage is 8.95 V, the maximum efficiencies of the proposed active rectifier and dc–dc converter are 91.5% and 92.7%, respectively. The range of ac input voltage is 3–20 V, and the efficiency of the WPRU is about 80.86%.**

***Index Terms*—6.78 MHz, A4 WP, active rectifier, delay-locked loop (DLL), high efficiency, magnetic resonant, wireless power receiving unit (WPRU).**

Manuscript received February 6, 2015; revised May 29, 2015; accepted August 10, 2015. Date of publication August 13, 2015; date of current version January 7, 2016. This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korean government (MSIP) under Grant 2014R1A5A1011478. Recommended for publication by Associate Editor R. Zane.

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Digital Object Identifier 10.1109/TPEL.2015.2468596

I. Introduction

In recent years, research for the wireless charging system is under way actively with the rapid development of smartphones and wearable devices. For the magnetic resonance method compared to the inductive coupling method, it is a powerful wireless charging system since it maintains high efficiency even the distance between transmitter and receiver is far more than several meters. However, since the frequency of A4 WP, one of the standards in magnetic resonance method, is 6.78 MHz, it is a very challenging task to enhance the efficiency of the rectifier, which accounts for the largest portion of the total efficiency of receiver [1], [2].

Especially, high-voltage MOFSET should be used to allow wide input range according to the distance, and it is necessary to solve the side effects occurring due to the MOSFET. Since the parasitic capacitance is much larger than that of general MOSFET, switching loss becomes the critical issue in high-speed applications such as A4 WP.

Another problem is the reduction in efficiency due to heat. In A4 WP systems, since the input power at the normal operation is above 5 W, the heat caused by receiver inefficiency reduces the efficiency of the receiver, which is a vicious circle. Especially, efficiency of the dc–dc converter is drastically decreased when the switching frequency is varied because of the temperature [3].

In this paper, by adopting delay-locked loop (DLL) in active rectifier, the reverse leakage current can be removed, and by adopting negative impedance circuit (NIC), the switching loss of gate driver can be minimized. Moreover, for the low-side MOSFETs, the DLL is shared with the high-side MOSFETs to minimize the size and power consumption.

By adopting phase-locked loop (PLL), the proposed dc–dc converter can maintain constant switching frequency in spite of process, voltage, and temperature (PVT) variation. Moreover, by means of the pulsewidth-modulated (PWM)/pulse frequency modulation (PFM) switching method, the power efficiency can be retained from light load to heavy load.

The remainder of this paper is organized as follows. In Section II, the receiver architecture of the wireless power transfer system is described. Section III provides a description of building blocks, including active rectifier, dc–dc converter, and low-dropout regulator (LDO) regulator. Section IV shows the

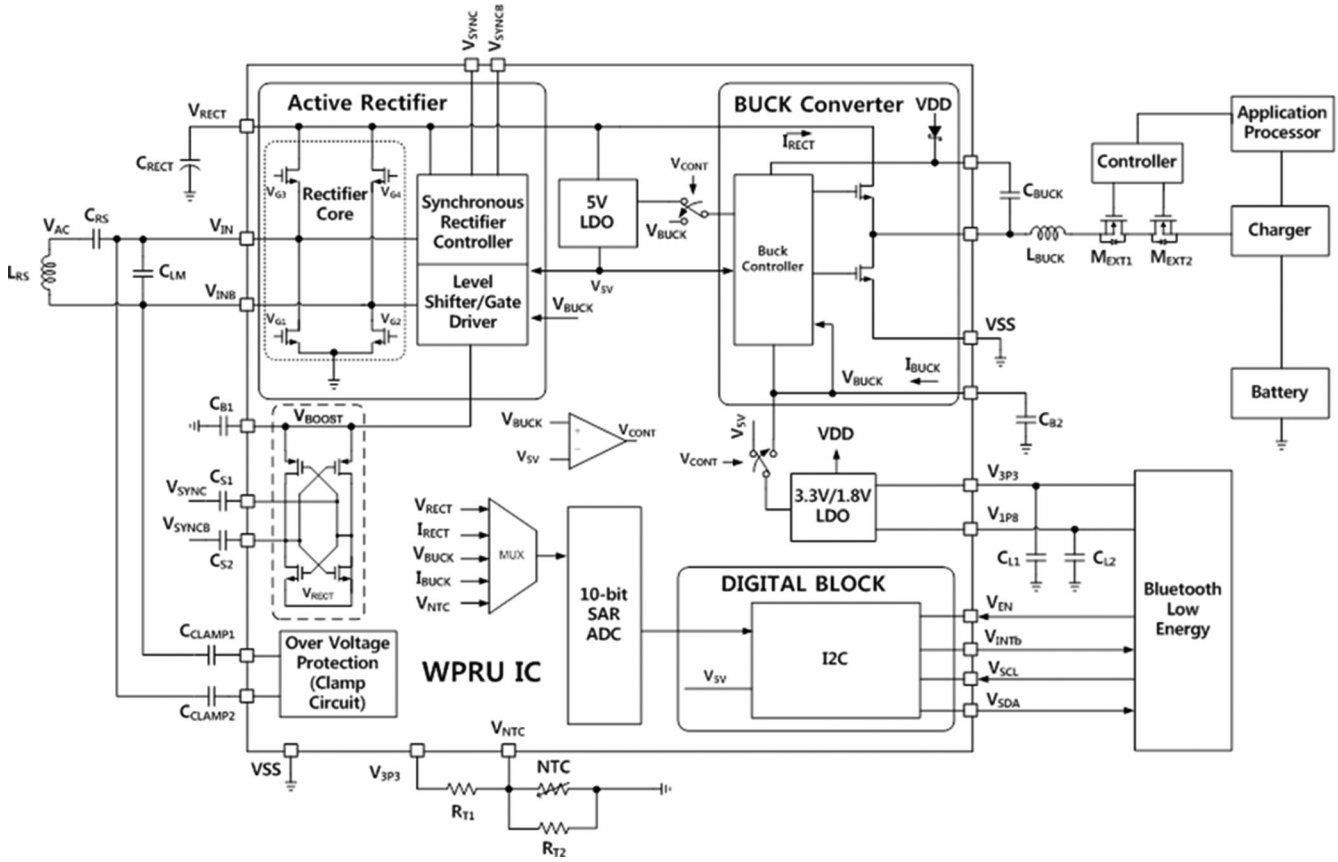


Fig. 1. Block diagram of the proposed WPRU.

experimental results from implementation of a 0.18 μm CMOS, and Section V concludes the paper.

II. Architecture of a Wireless Power Receiving Unit

Fig. 1 shows a block diagram of the proposed wireless power receiving unit (WPRU). Generally, the rectifier dominates the overall efficiency of the wireless power receiver. Power is transferred from the transmitter to the receiver through the coil and matching networks. The ac voltage at the receiver input is converted into dc voltage by the rectifier. The power efficiency of the rectifier is critical, as it provides the dc power supply for all of the following stages. The input voltage from the coil is applied to the rectifier, and the output of the rectifier is converted into the desired dc voltage level through the dc–dc converter. The LDO regulator generates the clean dc voltage required for the battery.

The dc output of the rectifier V_{RECT} is converted into digital code, by the 10-bit successive approximation analog to digital converter (SAR ADC). The output of the ADC is then transferred to the transmitter through the I2 C in the receiver and Bluetooth low energy.

The timing diagram of the proposed WPRU is shown in Fig. 2. The power transfer unit (PTU) generates a short beacon after the initial power on and then detects the load variation to figure out whether or not the WPRU is located nearby.

When a nearby WPRU is detected, the PTU generates a long beacon to transfer a certain amount of power. From the transferred power, the WPRU generates the power needed for the initial operation through the rectification. When LDO for the Bluetooth low energy is turned on, the PRU asks for the power needed.

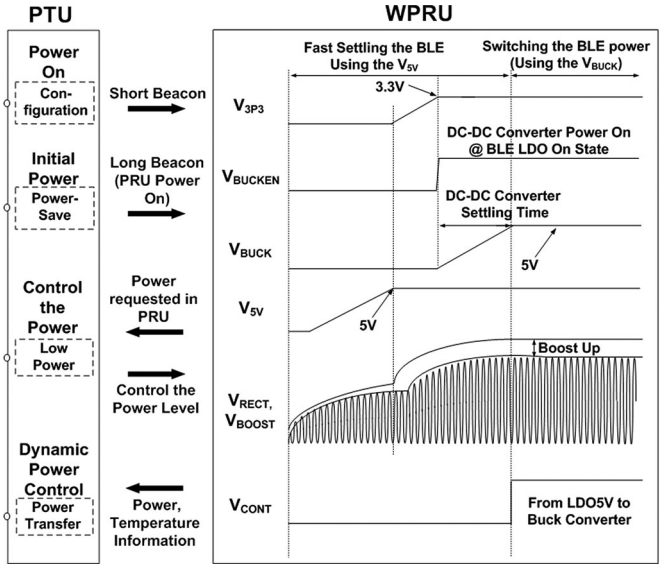


Fig. 2. Timing diagram of the proposed WPRU.

Through the communication, the PTU recognizes and transmits the power demanded from the WPRU. The WPRU detects

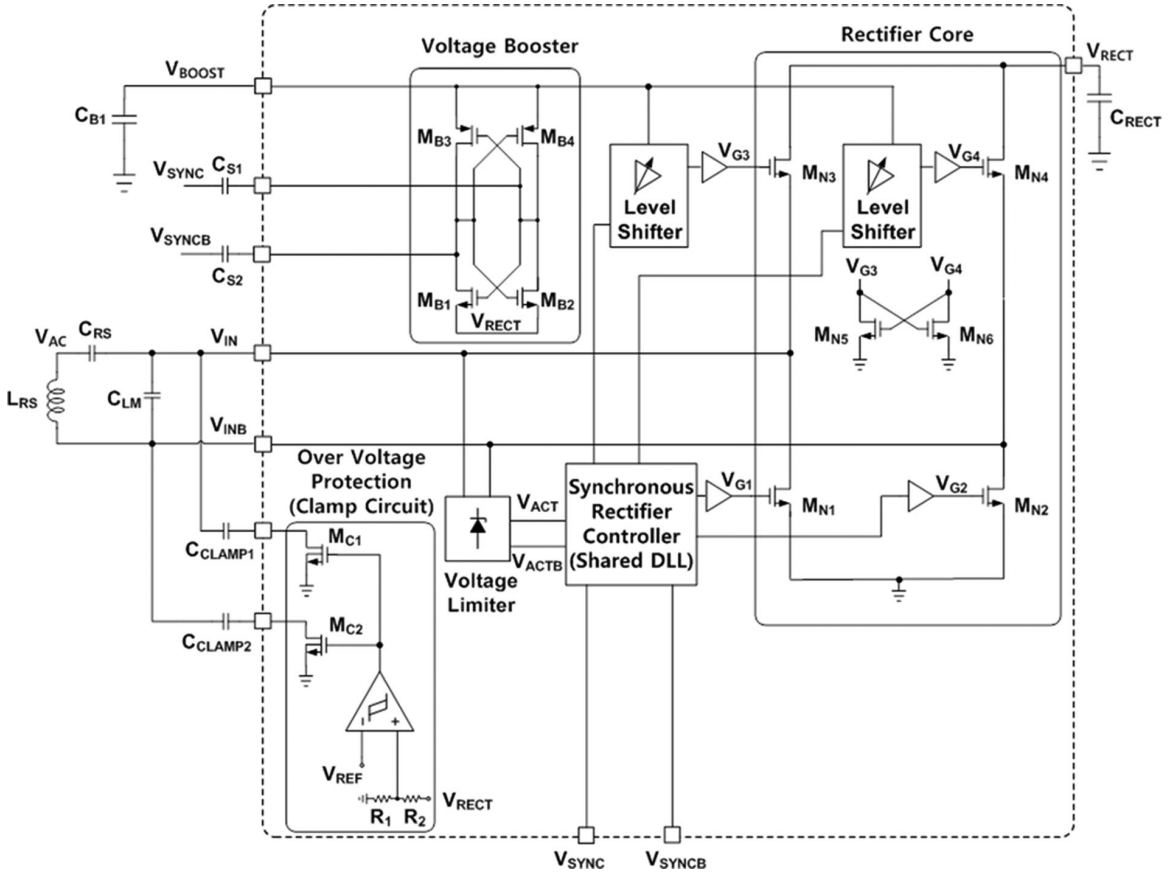


Fig. 3. Block diagram of the proposed active rectifier.

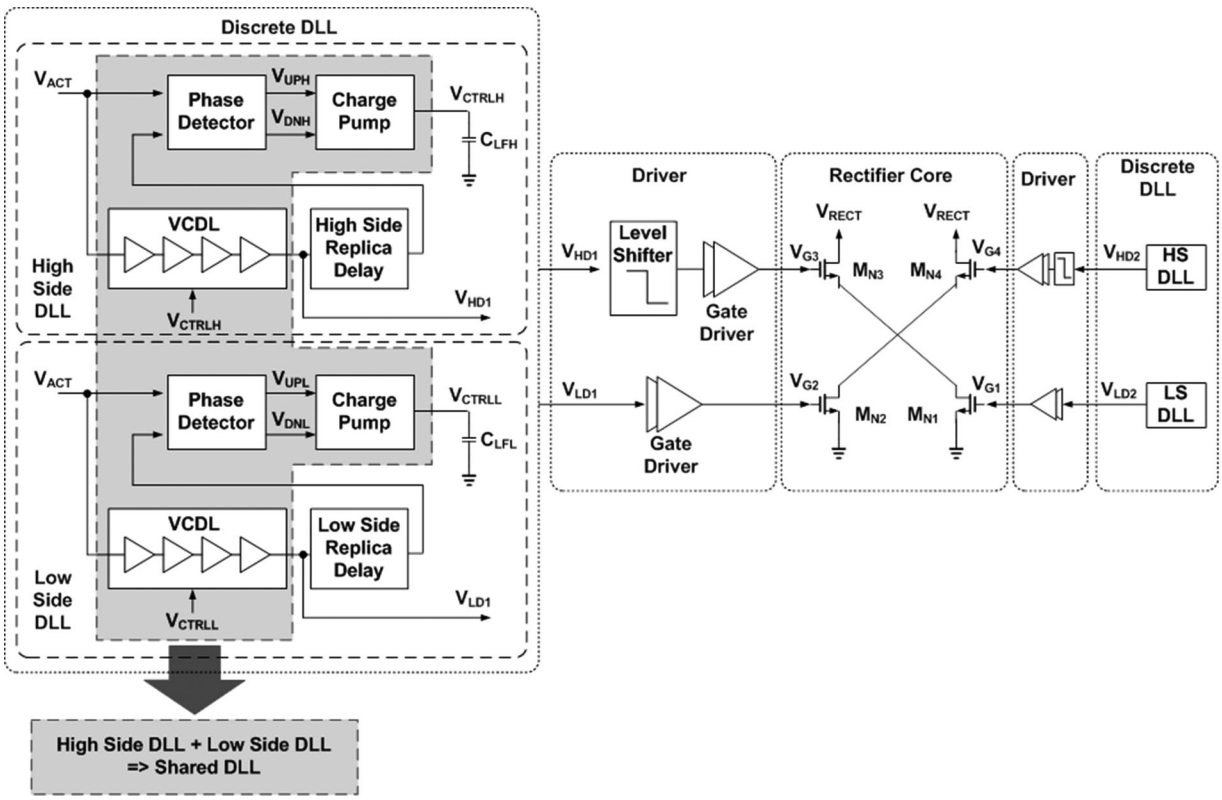


Fig. 4. Concept of the shared DLL architecture.

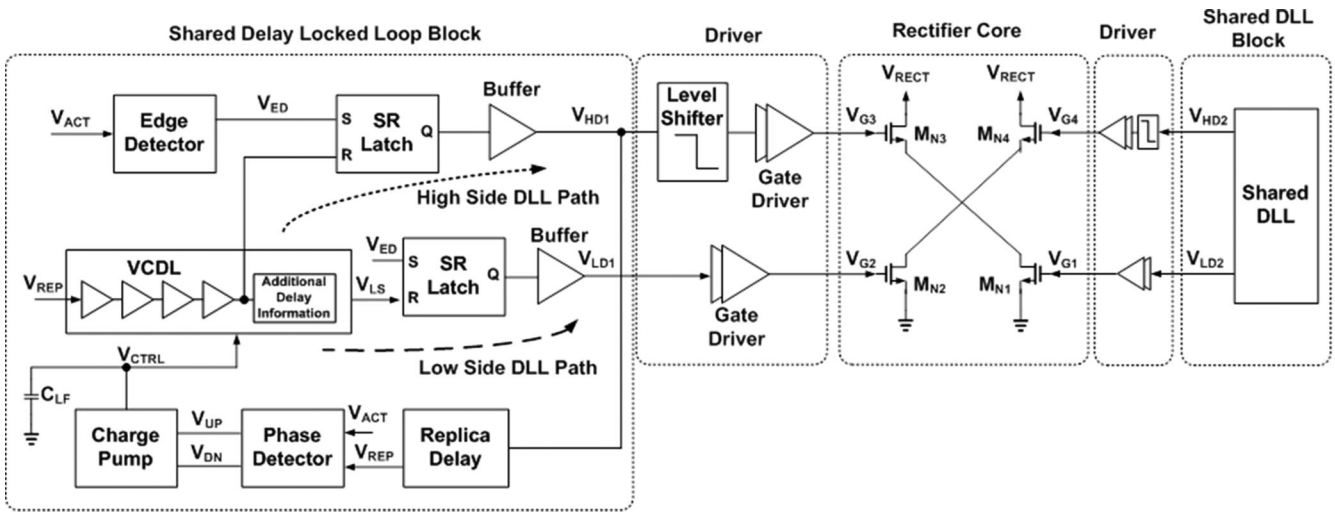


Fig. 5. Shared DLL architecture.

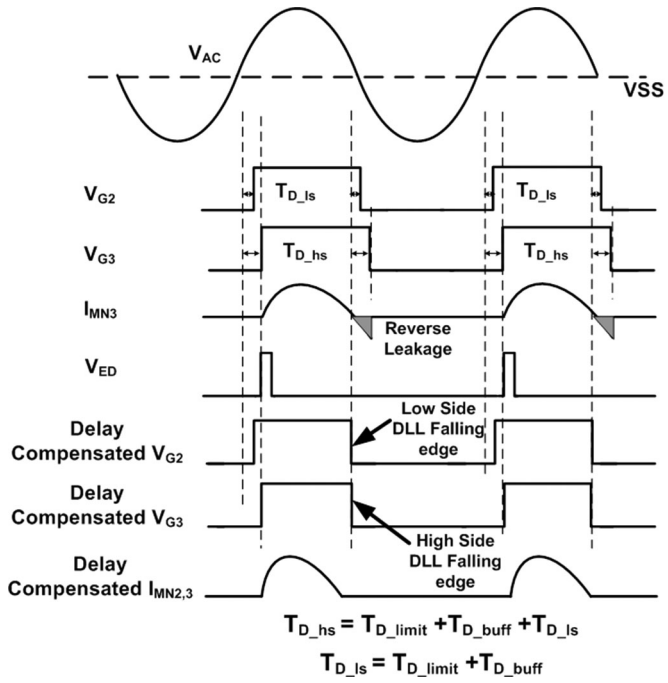


Fig. 6. Timing diagram of the active rectifier with DLL.

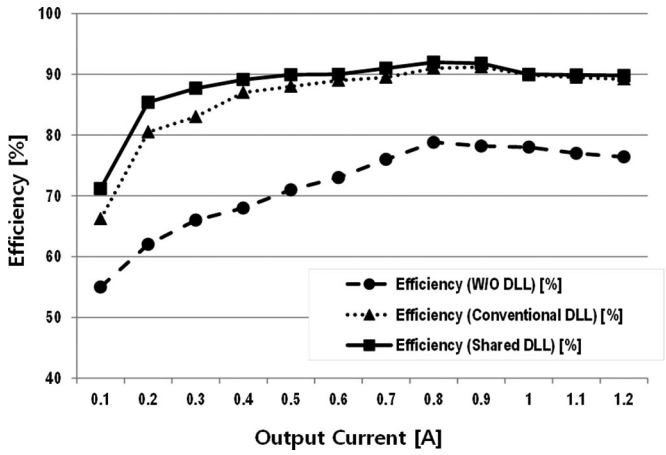


Fig. 7. Efficiency simulation results of three types of active rectifier.

TABLE I
COMPARISON OF THE SIMULATION RESULT ACCORDING TO THE ACTIVE RECTIFIER STRUCTURE

Structure	W/O DLL	Discrete DLL-Type (Using Four DLLs)	Shared (Using Two DLLs)
Current consumption (mA)	15.7	26.8	20.2
Estimated area (mm^2)	2.2	5	3.45
Simulated efficiency (%) @ 0.1 A load current	55	66.2	71.2
Simulated efficiency (%) @ 0.8 A load current	78.8	91.1	92

the voltage, current, and temperature variation through the ADC and transmits the information to the PTU by BLE. As a result, the communication between the PTU and PRU makes it possible to control the dynamic power.

III. BUILDING BLOCKS

A. High-Efficiency Active Rectifier

A block diagram of the proposed active rectifier is illustrated in Fig. 3. Because of the high power level and resonant frequency, it is not easy to get high power conversion efficiency for the rectification of the received ac power input. If a rectifier were implemented with passive diodes, the efficiency would be limited by the forward voltage drop of the passive diodes [4], [5].

In this paper, the active rectifier shown in Fig. 3 is designed where the MOS transistors were actively turned on and off depending on the polarity of the received ac input voltage. The

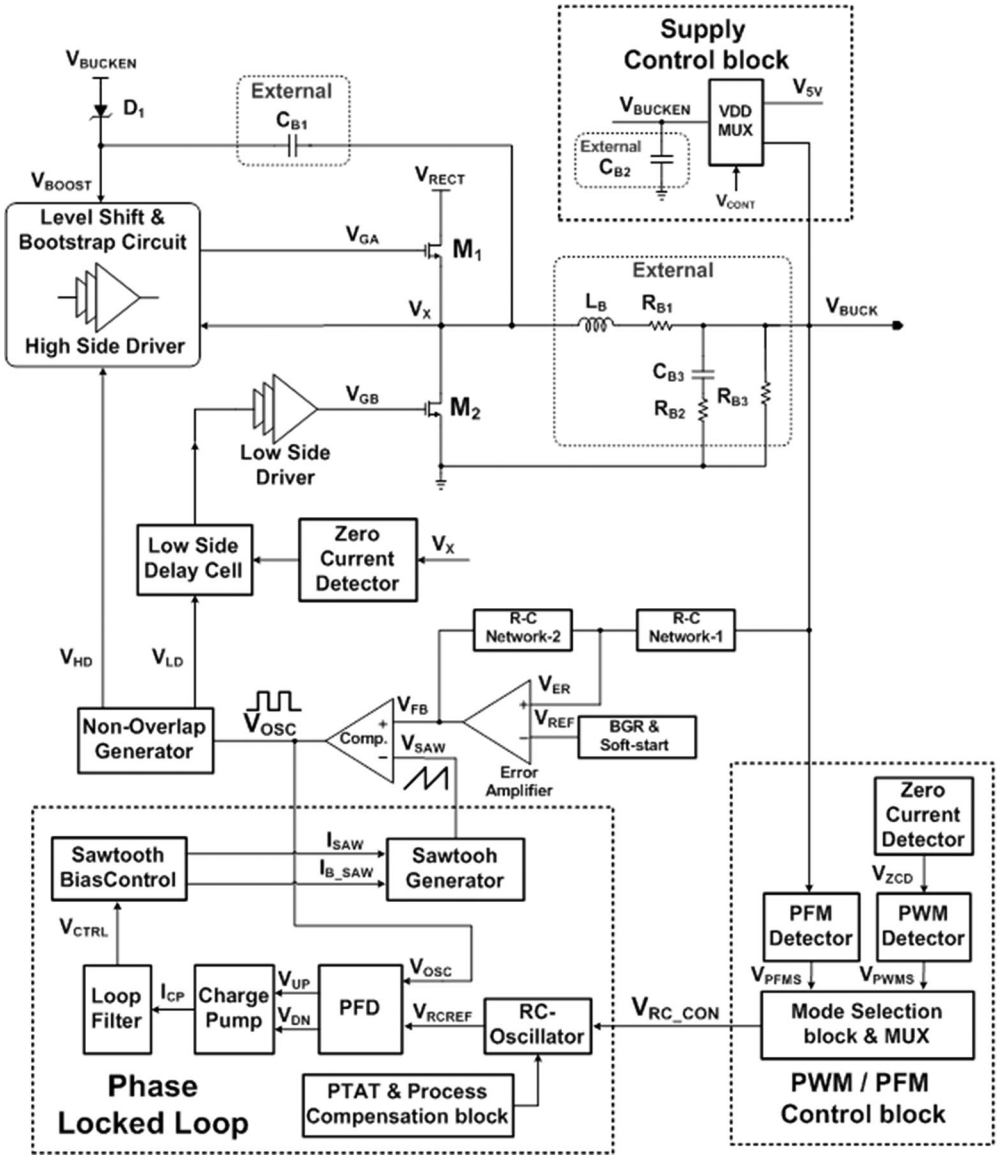


Fig. 8. Block diagram of the dc–dc converter.

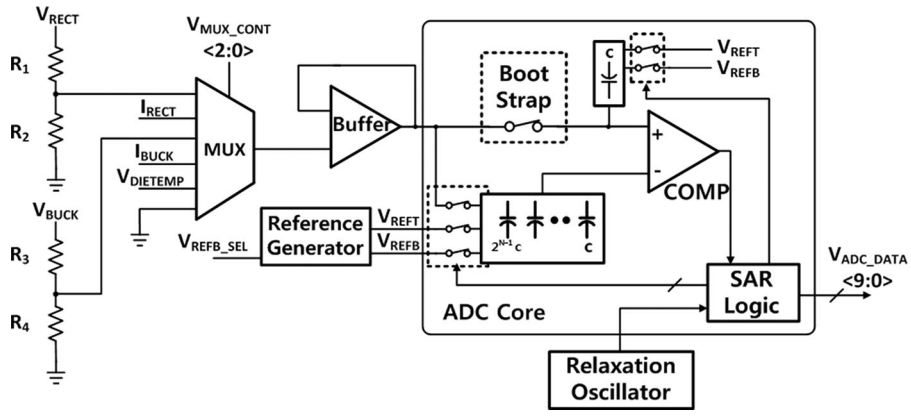


Fig. 9. Block diagram of the SAR ADC.

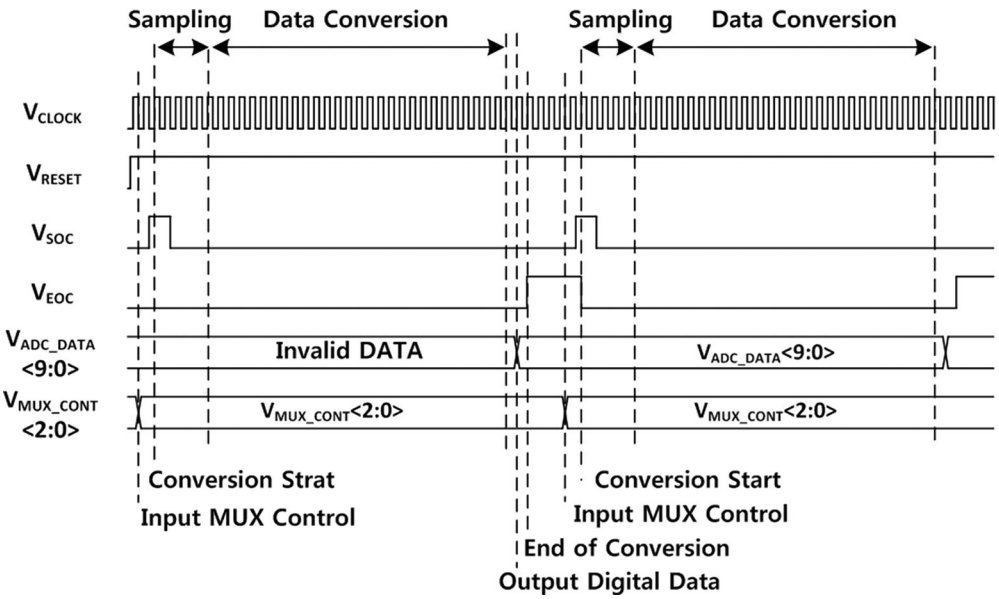


Fig. 10. Timing diagram of the SAR ADC.

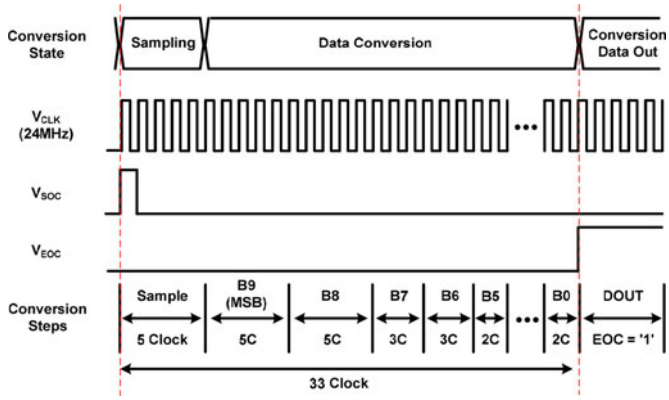


Fig. 11. Detailed timing diagram of the SAR ADC.

voltage drop across the MOS transistors can be made to be much smaller than that of a diode-based passive rectifier, therefore achieving higher power conversion efficiency. Unlike passive diodes, however, the current flow through the MOS transistors is bidirectional, which means that the current may flow from the dc output to the ac input. This reverse leakage current severely degrades the power conversion efficiency [6]–[8].

DLL was adopted for the proposed Rectifier to compensate for the delay caused by limiter, buffer, and level shifter. By compensating for the delay, the reverse leakage current could be removed while maximizing efficiency.

In case of wireless charging standards using hundreds of kHz frequencies such as WPC or PMA, conduction loss is the most significant factor determining the total efficiency [9]. However, in the A4 WP standard where the operating frequency is 6.78 MHz, the switching loss due to the high-voltage MOSFETs drastically increases. In order to reduce the conduction loss, MOSFET sizes should be designed as large as possible to minimize the on resistance. The large MOSFET sizes result in the large parasitic capacitance C_{GS}, C_{DS} and increase the current consumption of the gate driver operating at the frequency of 6.78 MHz.

To compensate for the switching loss explained earlier, an NIC with the cross-coupled structure using M_{N5} and M_{N6} was implemented, as shown in Fig. 3. NIC enables fast discharging, without any additional current consumption at the falling edge. As a result, the current consumption of the gate driver was optimized and the switching loss could be reduced.

Fig. 4 shows the concept of the shared DLL architecture. Since the high-side MOSFET needs level shifter for the proper operation, the delay caused by gates of the both, high-side and low-side MOSFETs cannot be compensated simultaneously. As can be seen from the figure, to compensate for the delay, each side of MOSFETs should have their own DLL structure. In results, four DLLs should be adopted for the active rectifier. To decrease the area and improve the efficiency, it is necessary to share the DLL between high-side and low-side MOSFETs.

Fig. 5 shows the proposed shared DLL architecture between the high-side power MOSFETs and low-side power MOSFETs. It is composed of an edge detector (ED), a phase detector (PD), a charge pump (CP), a voltage-controlled delay line (VCDL), and replica delay. Unlike low-side power MOSFETs, the high-side power MOSFETs need the boosted gate voltage for driving, which leads to a bit larger inevitable delay. This comes with the issue of consuming too much current as well as having too large size to use DLL for compensation of all the delays of the gate control voltage of power MOSFETs.

A4 WP standard mentions the resonant frequency accuracy as 6.78 MHz $\pm$ 15 kHz, so the frequency variation is not an issue to be considered. For the PVT variation, however, CP and replica delay are controllable to guarantee proper operation of DLL.

The timing diagram of the active rectifier with the DLL is illustrated in Fig. 6. In this paper, to overcome the inevitable delay of high-side power MOSFETs and the issues explained earlier,

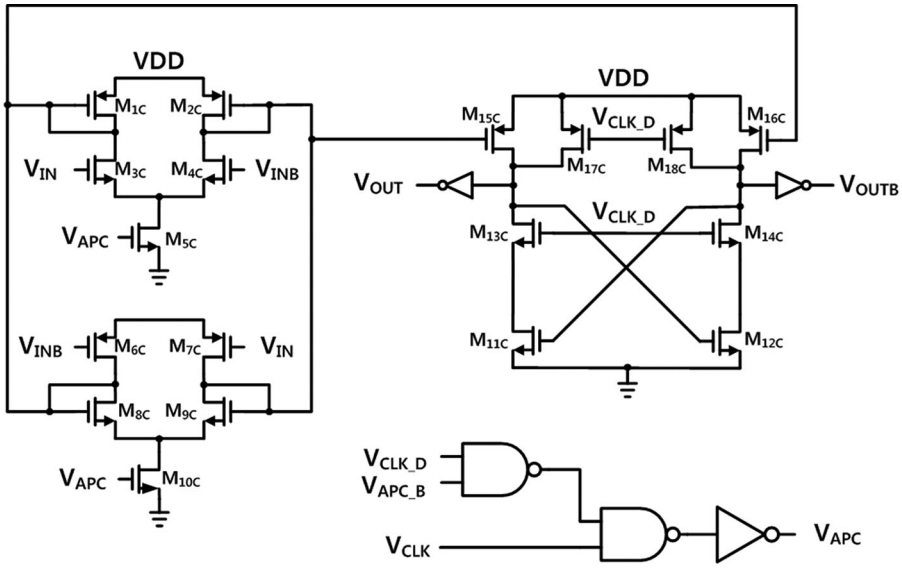


Fig. 12. Schematic of the comparator with APC.

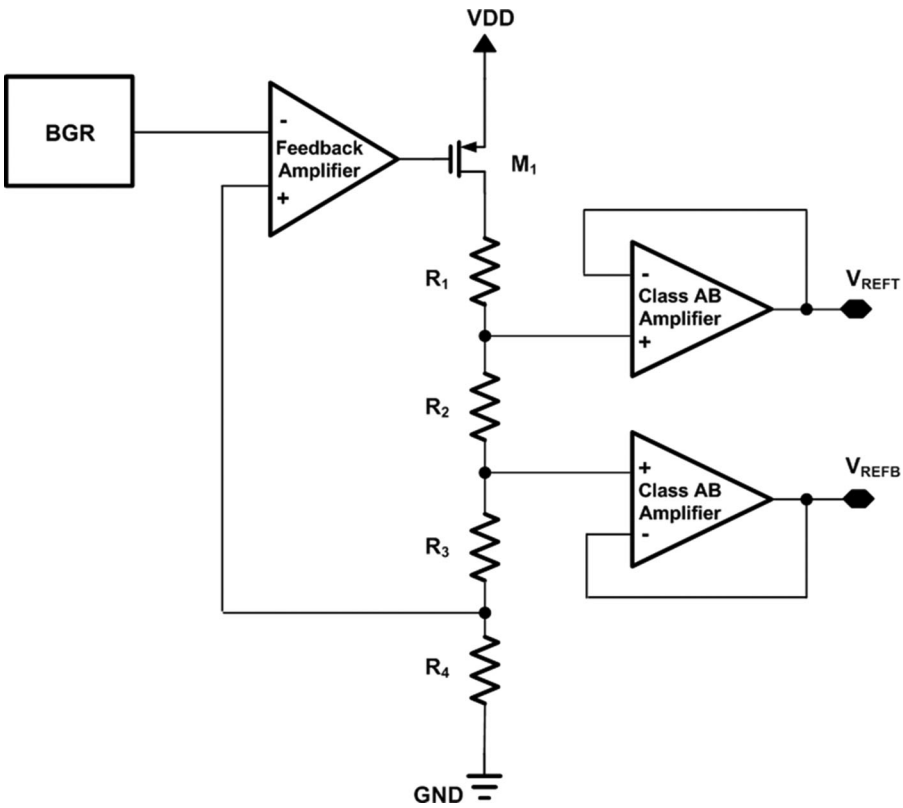


Fig. 13. Schematic of the reference voltage generator.

the shared DLL is proposed to compensate for the difference between the delay of the low side and the delay information from the high-side DLL. By utilizing the control voltage (V_{LS}) from the high-side DLL at the low-side DLL, the power efficiency can be increased because of the current consumption reduction, and the die size also can be reduced.

As can be seen in Fig. 6, the reverse leakage current is mainly due to the finite delay of the limiter, buffer, and level shifter driving the power MOSFETs $M_{N1} - M_{N4}$, which are large enough to minimize the voltage drop across them. The delayed turn-on of the power MOSFETs $M_{N1} - M_{N4}$ are not problematic because it does not cause any reverse leakage current. The delayed turn-off, however, results in reverse current flow, which degrades the power conversion efficiency.

The turn-on and turn-off instants of the high-side MOSFET M_{N3} and M_{N4} were delayed by T_{D_hs} from the zero-crossing

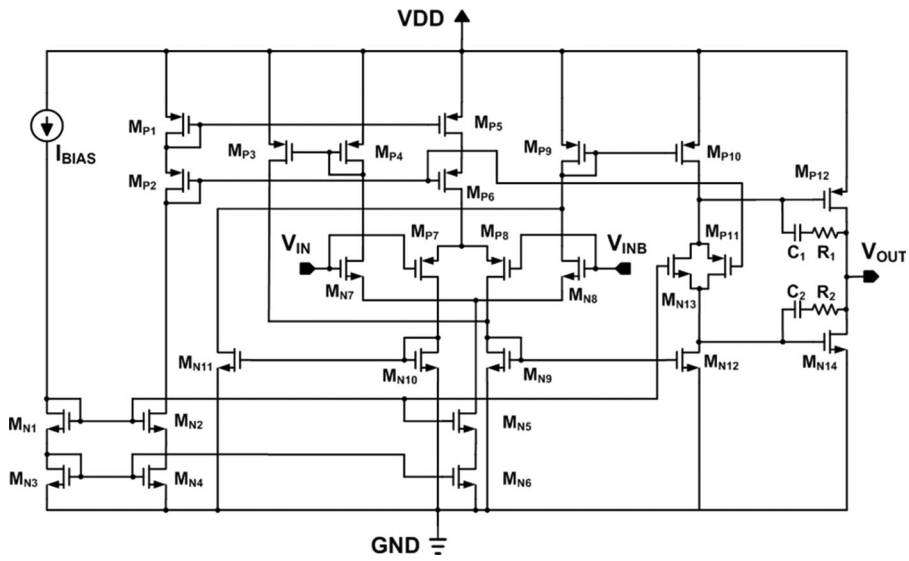


Fig. 14. Class-AB-type buffer used in reference voltage generator.

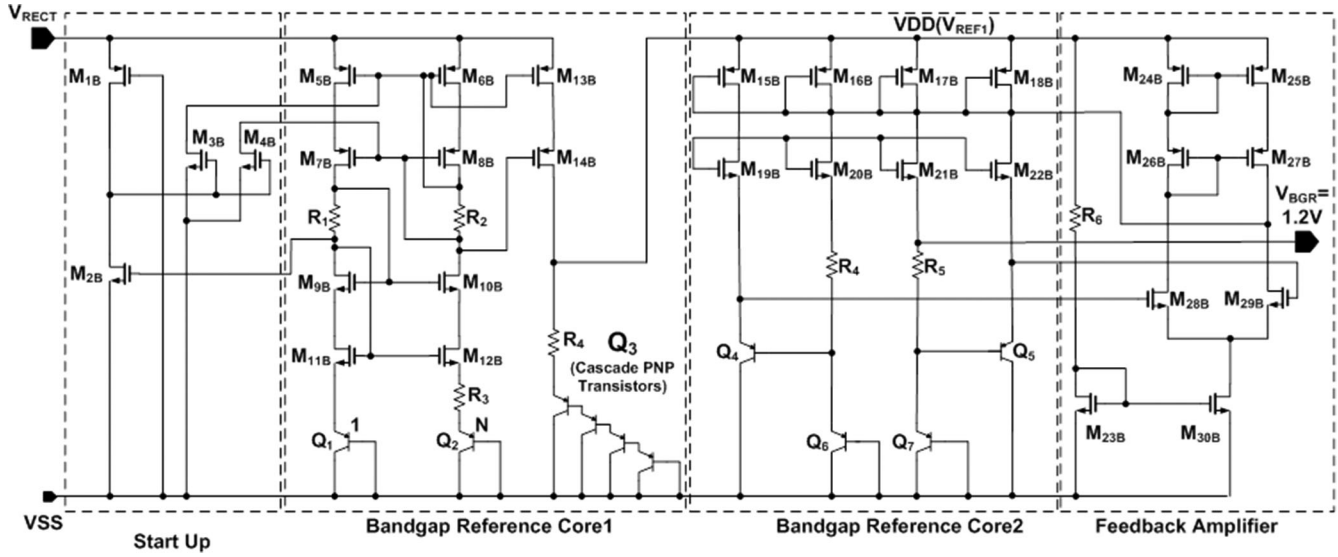


Fig. 15. High-voltage wide input bandgap reference.

instants of the ac input voltage where $T_{D\_\mathrm{limit}}, T_{D\_\mathrm{buff}}$, and T_{D_ls} are the delays of the limiter, buffer, and level shifter, respectively. Since level shifter does not needed for the low-side MOSFET T_{D_ls}, where the gate delay of M_{N1} and M_{N2} only becomes the delay of limiter and buffer.

In this paper, the turn-off delay of the limiter, buffer, and level shifter was compensated by the DLL with the timing shown in Fig. 6. By controlling the delay of the voltage-controlled delay line (VCDL), the DLL aligned the edge of the signal V_{REP} with that of the limiter and buffer output V_{ACT}. In the case of replica delay, the delay exists from the dummy cell of the level shifter. Through this delay, the gate voltage of the power MOSFET V_{G3} is aligned to the instant the ac input voltage V_{IN}, crosses zero, because the delays from V_{IN} to V_{G3} and from V_{ACT} to V_{REP} are all equal to the delay of the limiter, buffer, and level shifter T_{D_hs}.

In case of V_{LS}, shared DLL could be implemented to have the additional delay information of T_{D_ls}, which is the delay caused by level shifter. By shared DLL, with only two DLL structures, falling edge of high-side and low-side MOSFETs can be generated concurrently, while the active rectifier with discrete DLL needs four DLL structures to achieve same efficiency.

Fig. 7 shows the efficiency simulation results according to the structure of active rectifier from same system. As can be seen from the figure, the power efficiency of the active rectifier structure without DLL is degraded due to the reverse leakage current. In case of the discrete DLL type, the power efficiency is drastically decreased at the light-load condition because of the current consumption of four DLLs. At the light-load condition, power efficiency is degraded by maximum 5% compared to the proposed shared DLL.

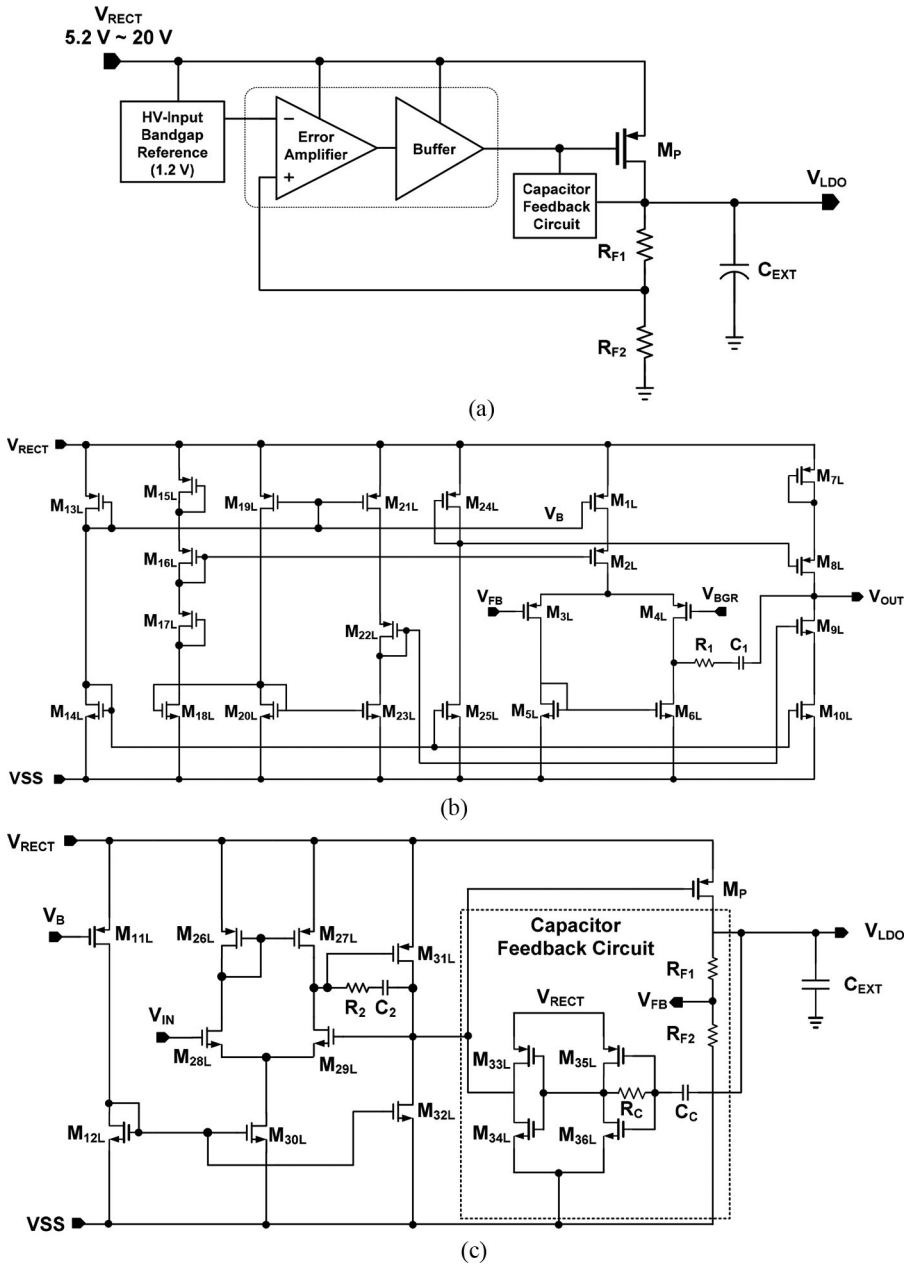


Fig. 16. Block diagram of the LDO regulator. (a) Top block diagram, (b) error amplifier, and (c) buffer and capacitor feedback circuit.

Table I is the comparison of simulation results according to the active rectifier structure. The proposed active rectifier with the shared DLL shows the highest efficiency with small estimated area.

B. DC–DC Converter

Fig. 8 shows a block diagram of the dc–dc converter. The proposed dc–dc buck converter, which employed PLL was composed of BGR, which generates the internal reference voltage; an error amplifier, which amplifies the voltage difference between output the voltage and reference voltage; a PLL, which generates constant frequency in spite of PVT variation and external circumstances; a PWM/PFM control block, which automatically decides the PWM/PFM mode according to the load; a high- or low-side driver for the power MOSFET driving; and a supply control block, which enables generation of the internal supply voltage of the dc–dc buck converter.

The proposed dc–dc buck converter was implemented to sense the high or low load current in the PWM/PFM control block and automatically switches between the PWM or PFM mode [10]–[13]. It operates as PWM mode at load currents of 300 mA–1.2 A, and as PFM mode, at currents below 300 mA. In high load current situations, the output voltage becomes the input to the error amplifier V_{ER} and is compared to V_{REF} generated from band-gap reference (BGR), and the voltage difference between V_{ER} and V_{REF} is amplified by the error amplifier. The output of the error amplifier becomes V_{FB} voltage.

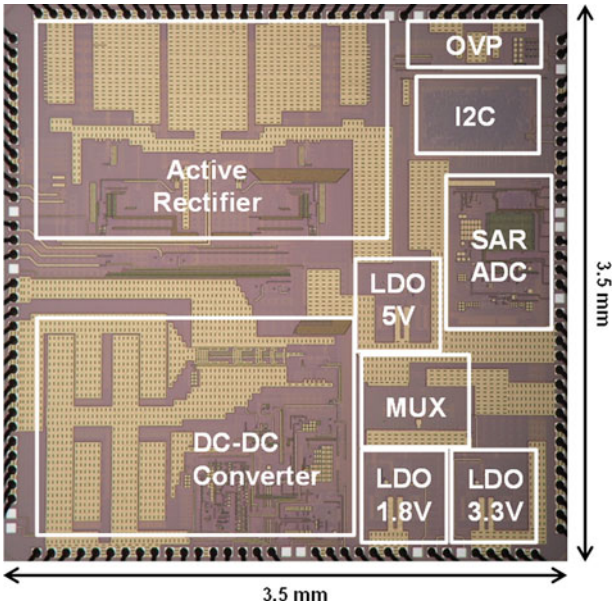


Fig. 17. Chip microphotograph of the WPRU

V_{FB} is compared with the Sawtooth wave from the PLL where the frequency is 2 MHz. A pulse wave $V_{\rm OSC}$ is generated through the comparator, while the duty is decided by the voltage level V_{FB}. The pulse wave $V_{\rm OSC}$ becomes the input for the nonoverlap generator block, which generates two nonoverlapped pulse waves V_{HD} and V_{LD}. The pulse waves V_{HD} and V_{LD} become the inputs of the high-side and low-side drivers, respectively. In case of high-side driver, gate of the power MOSFET M_1 should be switched. Since voltage $V_{\rm RECT}$ can be varied from 10 to 20 V, V_{GS} of power MOSFET M_1 should be guaranteed to make M_1 turn on/off sufficiently. Moreover, V_{GS} cannot exceed 5 V because of the regulation of the process. By implementing a level shifter and bootstrap circuit, which uses V_X node voltage and $V_{\rm BOOST}$ voltage from the diode as inputs, V_{GS} of M_1 can be guaranteed to make M_1 turn on/off, and V_{GS} voltage can always be lower than 5 V. When negative current tries to flow through the zero-current detector, the low-side driver makes the on/off operation of the switch by sensing V_X node to prevent the negative current from flowing. Moreover, the low-side driver helps power MOSFET M_2 to have sufficient driving operation by making the gate switching operation of the power MOSFET M_2.

C. SAR ADC

A block diagram of the SAR ADC is presented in Fig. 9. It consists of a simple analog block, including a DAC, comparator, reference voltage generator and SAR. The reference voltage generator should drive the large binary-weighted capacitor array in the DAC.

SAR ADC operates in processing the voltage and current of the rectifier and dc–dc converter, and the information of the temperature sensing block through MUX. Processed digital information, from which the received power or temperature information can be identified, is transferred to BLE through I2 C. Transmission power can be controlled from the received information.

Fig. 10 shows the timing diagram of the SAR ADC. When the start-of-conversion (SOC) signal is applied, sampling and data conversion begin. Conversely, when finished, the end-of-conversion (EOC) signal is generated while outputting digital data. In the case of MUX, the selection signal $V_{\rm MUX\_CONT}\langle 2:0\rangle$ was composed to save the data and processing during three cycles right after the EOC signal and then controlled by I2 C. In addition, it was set up to process voltage and current information automatically.

A detailed timing diagram of the SAR ADC is shown in Fig. 11. In the sample stage, analog input voltage was sampled during five clock cycles. In the hold stage, the conversion was completed after sixteen steps. The redundancy SAR algorithm was adopted to correct the error occurring during each conversion step.

As can be seen in Fig. 11, the duration of each conversion step was designed to vary considering the settling time of the reference voltage due to the capacitance in the DAC. In Step 1, the MSB was determined and the reference voltage generator drives the largest capacitance in the DAC. Thus, five cycles are required for the reference voltage to settle down in Steps 1 and 2. In Steps 3 and 4, three cycles were assigned for each conversion step. Two cycles are required for Step 5 $\sim$ 10.

Fig. 12 shows the schematic of the comparator. A two-stage latched-type comparator with adaptive power control (APC) was used to minimize the current consumption. APC operation generates short pulse by gating the ADC clock and delayed clock. Since the comparison is finished only if the APC signal is high, it operates so as to minimize the dynamic current.

The schematic of the reference voltage generator is illustrated in Fig. 13. Two buffers were used to generate the reference voltages $V_{\rm REFT}$ and $V_{\rm REFB}$ and drive the large capacitance in the DAC.

Fig. 14 shows the Class-AB-type buffer. In order to meet the settling time and conversion speed, the output current of the buffer should be large enough. Thus, the Class-AB-type buffer was designed to simultaneously meet the requirements for low power consumption and fast settling time.

D. LDO Regulator

The high-voltage wide input bandgap reference (BGR) is presented in Fig. 15. The input range was from 3.5 to 20 V, which covers nearly the whole range of the rectifier output [14].

The output voltage of the first stage cannot be too low (3.0 V) because it needs to drive the second-stage circuit. The traditional BGR circuit output voltage is generally less than 1.5 V because of V_{BE} of the bipolar transistor. At room temperature, V_{BE} of bipolar transistors in different processes are between 0.6 and 0.8 V. In order to increase the output voltage, a stack of V_{BE3} was employed. Although such a practice will affect the temperature coefficient of the circuit, this can be fixed in the second-stage circuit. The *W/L* of M_{13B} is *N* times that of other MOSFET, so $I_{M_{13}} = M \times I_{M_6}$.

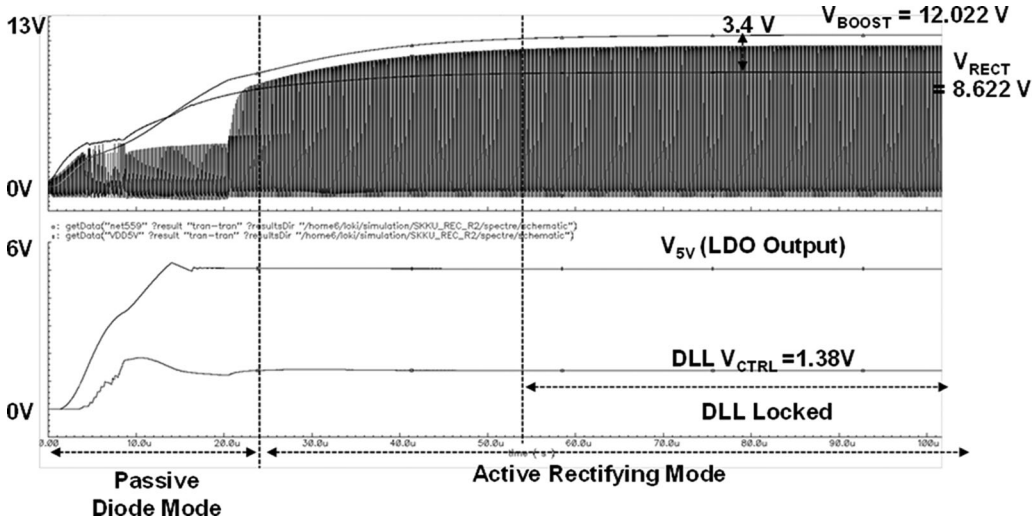


Fig. 18. Simulation results of the active rectifier.

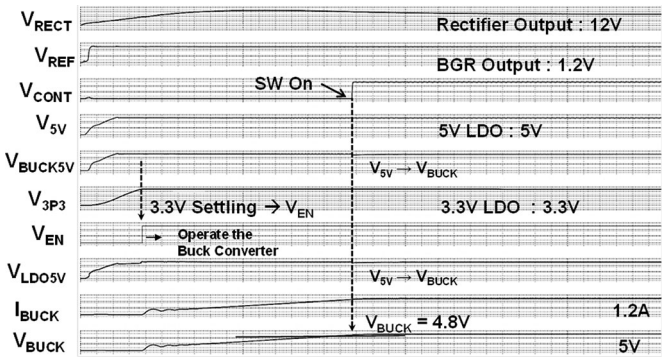


Fig. 19. Simulation results of the WPRU.

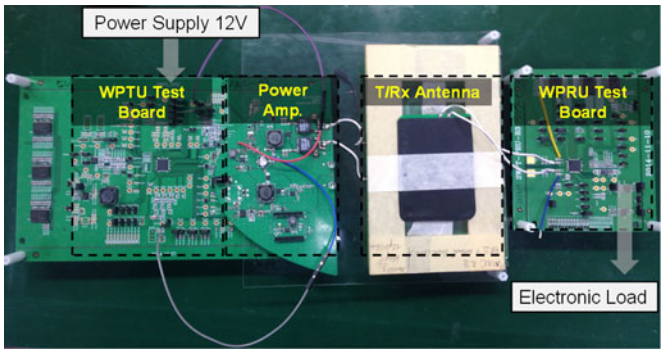


Fig. 20. Measurement environments of the WPRU.

The voltage of the first-stage output is as follows:

$$V_{\mathrm{REF1}} = V_{\mathrm{BE3}} + NI_{M_6} = V_{\mathrm{BE3}} + M\frac{R_4}{R_3} \times V_T \ln N \quad (1)$$

where V_T is the thermal voltage, which is equal to kT/q, where k is Boltzmann's constant and T is the absolute temperature.

Fig. 15 shows that a multiple V_{BE3} can be obtained by replacing Q_3 by four cascade PNP transistors. Through the rational design of M, N, R_1, and R_2, the value of V_{REF1} can meet the objective of 3 V. Because the TC of V_{BE3} is not linear for the stacked structure, the output voltage with zero TC cannot be obtained. The voltage will be refined by the second stage.

The LDO regulator operates to reject ripple and to generate constant output voltage. Fig. 16(a) shows a block diagram of the LDO regulator. The output voltage drop due to rapid and large load variation could be minimized with a fast regulation loop. Application of this fast transient LDO is useful for low noise at wide input ranges to transient response (high voltage at rectifier input). In addition, the proposed LDO was based on a capacitor feedback circuit to compensate for the network and fast settling capability with high PSRR.

The settling time of the LDO can be improved by providing a low-impedance node at the pass transistor input. The proposed LDO is shown in Fig. 16. To avoid nonlinearity of the LDO, M_P was connected with a buffer. The output node of the error amplifier was lower than the gate of M_P making M_P seem to have a large gate-source voltage. A large current was provided to pull down the gate of M_{P} when output of the buffer, the drain of M_{8L}, was higher than the gate of M_P. This boosting of the current technique allows the circuit to settles quickly.

In addition, the push–pull structure of the capacitor feedback circuit can provide a fast path to discharge and charge the gate of the pass transistor, which can react to the transient with buffer stage.

IV. Experimental Results

The chip was fabricated using the 0.18 μm CMOS process with, a single poly layer, four layers of metal, MIM capacitors, and high sheet resistance poly resistors. The chip microphotograph of the WPRU is shown in Fig. 17. The die area of the WPRU is 3.5 mm × 3.5 mm.

Fig. 18 shows the simulation results for the proposed active rectifier. Since the voltage for operation of the active rectifier is not generated at initial operation, the rectifier operates with the passive diode seen from the high-voltage MOSFET. When the output of the rectifier increased above 5.2 V, which indicates that operation of the 5 V LDO used for internal circuit operation starts, the active rectifier also begins to operate without any help

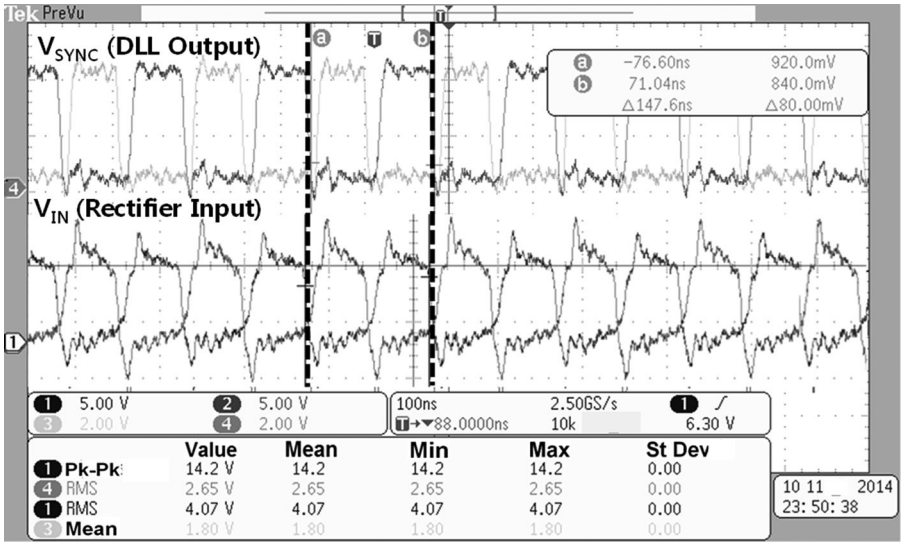


Fig. 21. Measurement results of DLL in the active rectifier.

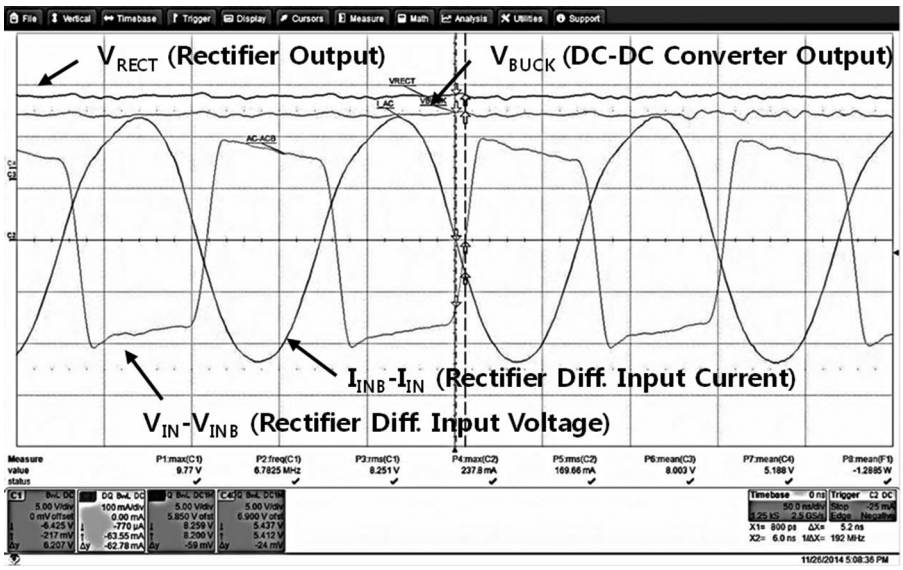


Fig. 22. Measurement results of the WPRU.

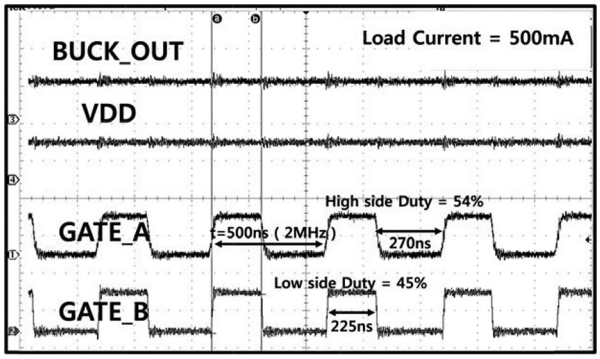
from the passive diode. As can be seen from the simulation results, in the circumstances of 7.5 W input and 10.77 Ω output load, the maximum power of 6.9 W and the efficiency of 92% were achieved at the maximum efficiency condition when DLL was locked.

The top simulation results of the proposed WPRU are presented in Fig. 19. When the rectifier voltage increased above a certain level, the conditions for the 5 V LDO operation can be met and the internal dc–dc converter and ADC can operate. In the case of the dc–dc converter, by using 5 V LDO voltage, the output voltage was generated, and when the output voltage of dc–dc converter increased above 4.8 V, the internal circuits could be operated from the output voltage feedback. As can be seen from the simulation results, the final output of the dc–dc converter was 6 W when the input of 7.4 W was used, which means the system had 81% efficiency.

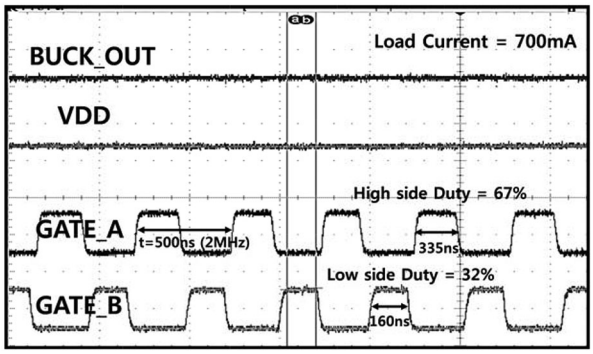
The measurement environments of the WPRU are illustrated in Fig. 20. The Tx Coil and Rx Coil were located at the bottom and top sides, respectively. The power was transferred from the WPTU board to the WPRU board through the Tx Antenna and Rx Antenna.

Fig. 21 shows the measurement results of the DLL in the active rectifier when the output power was 3 W. The phase between the input of the rectifier and the output of the DLL was synchronized by the DLL after the initial start-up operation. It also demonstrated that the gate control signals of the differential inputs of the active rectifier did not overlap with each other.

The measurement results of the WPRU for the output power of 6 W are shown in Fig. 22. The measured output of the rectifier was 8.6 V with the input matching and the output of the dc–dc converter was 5 V. Considering the phase difference between the input voltage and the current of the rectifier at the resonance



(a)



(b)

Fig. 23. Proposed dc–dc converter using PLL measurement for load current: (a) load current = 500 mA and (b) load current = 700 mA.

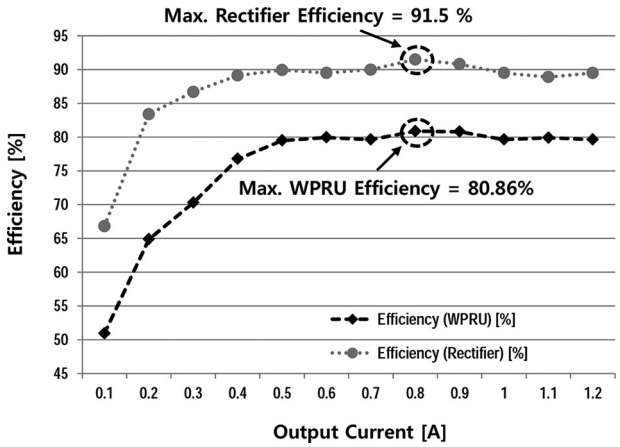


Fig. 24. Measured power efficiency of the WPRU with respect to the output current.

of Tx Coil and Rx Coil, the power efficiency of the WPRU can be calculated using (4)

$$P_{\mathrm{IN}} = \frac{V_{\mathrm{IN\_PEAK}} \times I_{\mathrm{IN\_PEAK}}}{2} \times \cos(\theta_V - \theta_I) \quad (2)$$

$$P_{\mathrm{OUT}} = V_{\mathrm{BUCK}} \times I_{\mathrm{LOAD}} \quad (3)$$

$$\eta = \frac{P_{\mathrm{OUT}}}{P_{\mathrm{IN}}} \times 100. \quad (4)$$

In (4), $V_{\mathrm{IN\_PEAK}}$, $I_{\mathrm{IN\_PEAK}}$, θ_V, θ_I, V_{BUCK}, and I_{LOAD} are the input peak voltage, the input peak current, the phase of input voltage, the phase of input current, the output voltage of buck dc–dc converter, and the load current, respectively.

TABLE II
PERFORMANCE SUMMARY OF THE WIRELESS POWER RECEIVER UNIT

Reference	[1]	[6]	[15]	[16]	**This Work**
Technology	0.35 μm BCD	0.35 μm BCD	0.5 μm CMOS	0.18 μm CMOS	**0.18 μm BCD**
Overall efficiency (%)	86 (Off-chip rectifier)	75 / 68	77 (Rectifier only)	50	**80.86**
Resonant frequency (MHz)	6.78	3.23 / 6.78	13.56	6.78	**6.78**
Input voltage range (V)	20	4∼8	2.15–3.7	20	**7∼20**
Maximum output power (W)	6	3	0.037	1	**6**
Output voltage (V)	5	5	3.1	3.1	**5**
Regulation (%)	-	-	33	-	**2.5**
Die area (mm^2)	5.52 (w/o rectifier)	18.3	0.585	6.25	**12.25**

Fig. 23 shows the duty variation of proposed dc–dc converter. As can be seen from the results, duty is varied by load current. When the load current is 500 mA, V_{BUCK} is regulated to 5 V and the duty ratios of GATE_A (V_{GA}) and GATE_B (V_{GB}) are 270 ns (54%) and 225 ns (45%), respectively, and having about 1% nonoverlap period. Also having about 1% nonoverlap period, when load current is 700 mA, the duty ratios of GATE_A and GATE_B are 335 ns (67%) and 160 ns (32%), respectively.

Fig. 24 shows the measured power efficiency of the WPRU and active rectifier when the output current was swept from 0.1 to 1.2 A. The peak power efficiencies of the WPRU and active rectifier are 80.86% and 91.5%, respectively, when the output current is 0.8 A.

The comparison between reported related WPRUs and this paper is summarized in Table II [1], [6], [15], [16]. The proposed WPRU showed the highest overall efficiency with wide input voltage range.

V. CONCLUSION

This paper presented a full-CMOS receiver for A4 WP applications. The proposed high-efficiency active rectifier with DLL is a highly efficient receiver circuit intended for use in resonant wireless charging application with a 6.78 MHz resonant frequency. Each MOSFET of the proposed rectifier uses ac input voltage for the on/off operation. At that time, DLL can be used to compensate for the delay caused by the voltage limiter, level shifter, and gate driver, which leads to the removal of reverse leakage current and maximization of power efficiency. Moreover, for maximization of the power efficiency, NIC was also adopted to minimize switching loss. In the case of dc–dc converter, PLL was adopted for the constant switching frequency in PVT variation to solve the efficiency reduction problem, especially due to heat. This chip was implemented using 0.18 μm BCD technology with an active area of around 3.5 mm × 3.5 mm. When the magnitude of the ac input voltage was 8.95 V, the maximum efficiency of the proposed rectifier and dc–dc converter were 91.5% and 92.7%, respectively. The

range of the ac input voltage was 3–20 V, and the receiver demonstrated about 80.86% efficiency.

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