Improved Efficiency in the CMOS Cross-Connected Bridge Rectifier for RFID Applications

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***Abstract*—A bridge rectifier based on the cross-connected NMOS-PMOS bridge that avoids the inherent degradation of power conversion efficiency for increasing input levels is presented. Instead of PMOS switches, the proposed rectifier uses diode-connected MOS transistors with static threshold cancellation and minimised diode reverse leakage. With a simple and power efficient circuit solution the new rectifier allows for low-power, passive tag implementation in standard CMOS for both LF and HF RFID applications. Simulation results of the proposed rectifier in a 0.35 μm CMOS process show a power conversion efficiency over 60% for all input levels above 0.75 V with a 100 kΩ load and an input signal frequency of 13.56 MHz. The simulated DC output voltage at the same conditions is approximately $V_{in}-0.3$ V. A model for the PCE of the new rectifier that includes the impact of the V_{th}-generator is developed and compared with simulated results.**

***Index Terms*—RFID, rectifier, power conversion efficiency, reverse leakage, active diode, threshold elimination, CMOS, low power, low voltage, analog integrated circuits.**

I. Introduction

In passive RFID, the ability of the DC-generating block to efficiently convert a weak incoming RF-signal to a stable power supply with enough current to support a complex chip is one of the keys in meeting future demands on RFID technology. These demands include lower cost, higher security and commutation at higher rates and longer reading ranges as well as on chip integration of sensors for environmental monitoring [1]. There are many factors that limit the rectifier performance and power extraction for wireless powered devices. For efficient use of available RF input power, the rectifier is required to have a low turn-on voltage to minimise the dead zone where all input power is wasted. The turn-on voltage directly depends on the threshold of the active devices used, such as MOS diodes, Schottky diodes, low-V_{th} and floating gate transistors [2][3]. A second important limitation is the reverse leakage of these devices that reduces power conversion efficiency after the rectifier is activated.

In this work, a bridge rectifier based on the NMOS-PMOS cross-connected bridge rectifier (cc-bridge) is presented in which the degradation due to reverse leakage is effectively minimised. The PMOS pair of the cc-bridge is exchanged for MOS diodes to avoid the inherent charge leakage. Two active inverters and a V_{th}-generator are added to improve the function of the MOS diodes.

The function of the cc-bridge is described in section II-A. In section II-B, the problem with charge leakage is described and related work is presented. The circuit design, presented in section III, starts with a brief on the V_{th}-cancellation technique in MOS diodes and continues with the design of the proposed rectifier. Simulation results are presented and discussed in section IV, followed by conclusions in section V.

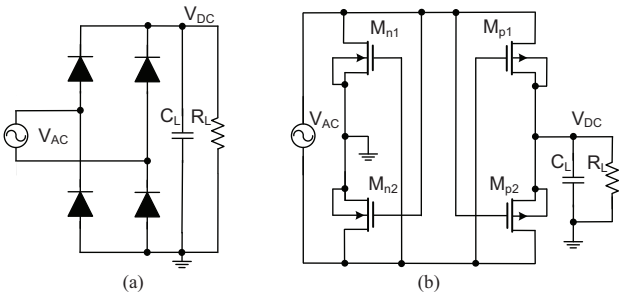

Fig. 1. The conventional full wave diode bridge (a) and the NMOS-PMOS gate cross-connected bridge (b).

II. The Cross-Connected Bridge

A. Principle

As a background to the proposed rectifier the principle of the cc-bridge is presented. The cc-bridge in Fig. 1 is developed from the conventional full wave diode bridge where the diodes have been replaced with switches. During the rectifying operation, the switches conduct in pairs, $M_{p2} \rightarrow M_{n1}$ and $M_{p1} \rightarrow M_{n2}$; thus, the current to the load will have the same direction during both the positive and negative phases of the input signal (see also Fig. 3). Because each switch is driven by the full input swing, the rectifier minimum turn-on voltage becomes V_{th}, and the developed DC voltage across the load capacitor ideally becomes V_{AC} - $2V_{DS}$, where V_{AC} is the peak value of the input signal and $2V_{DS}$ is the drain-source voltage drop on the conducting pair connecting the voltage source and the load. The advantages of using a switched structure compared to a bridge with conventional diodes are reduced minimum turn-on voltage and higher output voltage for the same input swing [4]. The cc-bridge achieves high power conversion efficiency (PCE) at low input signal levels, which has made this structure relevant for low-power and long reading range RFID applications. However, the switched structure suffers from a known problem with reverse charge leakage that severely reduces its PCE for input voltages above a certain level as simulated in Fig. 2. This leakage occurs during the on-off transition when a switching pair conducts

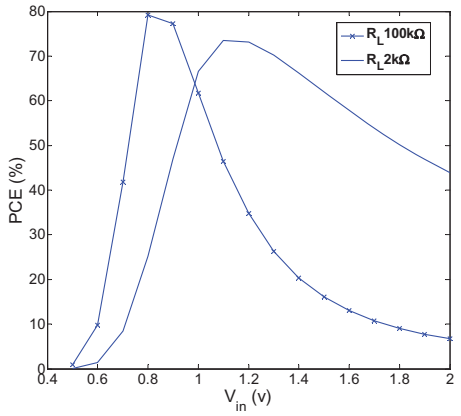

Fig. 2. PCE of the cc-bridge at two different loads simulated at an input signal frequency of 13.56 MHz. Less degradation of PCE can be seen with a heavier load because the loss due to leakage becomes smaller compared with the output power.

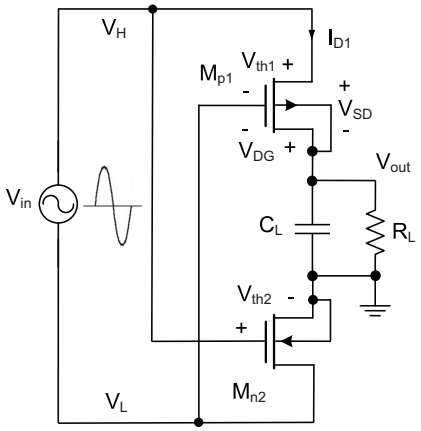

Fig. 3. The simplified schematic of the cc-bridge during the positive phase of the input signal when M_{p2} and M_{n1} are off.

in reverse for a short period of time, as described in more detail in section II-B. As indicated in Fig. 2, the problem with reverse charge leakage is more pronounced for a light load and thus for RFID chips with low power consumption.

B. Reverse charge leakage

As seen in Fig. 2 the cc-bridge reaches a peak in efficiency at relatively low input levels. This has been explained as a result of reverse charge leakage from the output capacitor when the input swings below the DC output level. During this time interval, when one of the output transistors should be completely turned off, its drain and source will interchange and current will flow toward the input, creating additional power loss in the NMOS and PMOS transistors. To investigate this phenomenon in more detail, we consider the cc-bridge during half a period of the input signal when M_{p1} and M_{n2} are on and M_{p2} and M_{n1} are off. The resulting structure is shown in Fig. 3. From the simplified cc-bridge we have the conditions for leakage expressed as

$$V_{th2} < V_H < V_{out} \tag{1}$$

and

$$V_{out} - V_L > V_{th1}. \tag{2}$$

When these conditions are fulfilled, both M_{p1} and M_{n2} are biased in reverse, which results in leakage, as shown in the simulation in Fig. 4. As a result, the maximum output voltage possible without leakage in the cc-bridge, is for $V_{DG} = V_{th1}$ which is typically 0.7 V in 0.35μm CMOS.

An alternative structure replacing only one pair of diodes with MOS switches avoids this problem because the remaining diode pair does not conduct in reverse (except the small leakage current) as the switches do here. However, this structure will suffer from the higher voltage drop of the remaining diodes.

Several works address the problem of reverse charge leakage in the cc-bridge for RFID applications. In [5], a detailed analysis shows the PCE and its peak characteristics for the cc-bridge mathematically. A new bootstrapping technique is used in [6] to eliminate the threshold voltage of diode-connected MOS transistors that are then introduced in simulations instead of the output PMOS pair. Recently, in [7], comparators are used in the cc-bridge to control the reverse leakage in the output PMOS pair resulting in improved voltage conversion efficiency, while PCE is not reported. In [8], the NMOS pair in the cc-bridge is replaced with active diodes. These diodes are realised with NMOS switches driven by high-speed comparators with extremely fast switching, which eliminates reverse leakage and achieves a power conversion efficiency greater that 80% for higher input levels. One of the remaining problems in [8], indicated by the presented results, is that the PCE is low for input signals up to 1.5 V. This problem has been addressed in a recent work [9] where a comparator-driven, low voltage switch is placed between the load and the output of

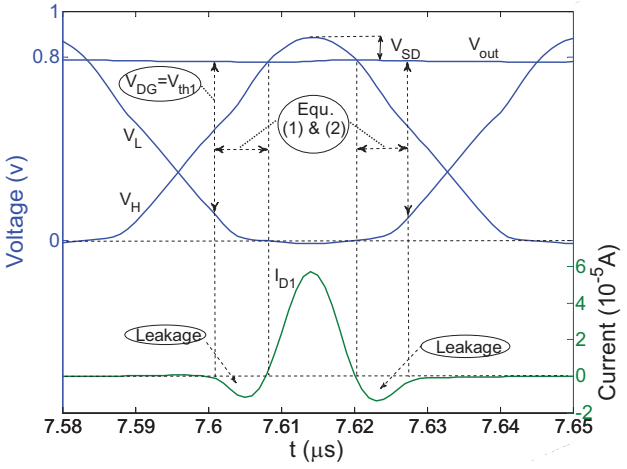

Fig. 4. Transient analysis showing the reverse charge leakage in switch M_{p1} during one period of the input signal with an amplitude of 0.9 V. Two negative current pulses occur for I_{D1} each time the switch turns on, the first starting when the difference between V_{out} and V_L equals V_{th1} and continues until V_H equals V_{out}.

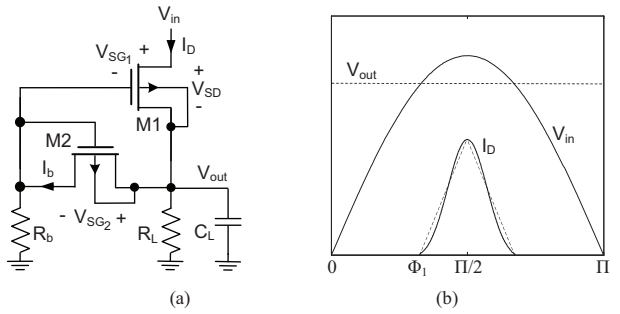

Fig. 5. a) Diode-connected PMOS transistors with static threshold cancellation. b) Triangular approximation of drain current pulse.

the cc-bridge to eliminate the reverse leakage. This result in a PCE greater than 80% for input voltages from 0.7 V to 1.8 V at a frequency of 1.5 MHz and a load of 500 Ω. However, both of the works in [8] and [9] are limited to applications with chip power consumption in the mW range because of the use of relatively power hungry comparator-driven switches to control the reverse leakage.

In the current work, a less power-hungry rectifier architecture, using active diodes to control the reverse leakage, resulted in comparable power conversion efficiency, both in the mW and μW range, as well as for LF and HF RFID applications.

III. Circuit Design

In the proposed rectifier, the leaking PMOS switches in the cc-bridge are replaced with diode-connected PMOS transistors with static threshold cancellation. This section starts with a short description of static V_{th}-cancellation before introducing this technique in the design of the proposed rectifier. The impact of the V_{th}-generator on efficiency is analysed and included in a model for the PCE of the rectifier.

A. Static Threshold Cancellation

Using diode-connected MOS transistors in rectifiers has the disadvantage of low power conversion efficiency and higher turn-on voltage due to the voltage drop of $\approx V_{th}$ from source to drain. For low voltage applications, such as RFID rectifiers, Schottky diodes or low voltage-drop transistors can be used in advanced CMOS processes at an additional cost. In standard CMOS, a static threshold cancellation technique has been used for diode-connected MOS transistors to improve the PCE for RFID rectifiers [10][11]. A simple illustration of this technique is shown in Fig. 5 (a) for a PMOS transistor. In contrast to a diode-connected MOS transistor where $V_{SD} = V_{th} + V_o$, the threshold drop from source to drain is cancelled with an additional diode-connected transistor that is forward biased from drain to gate of M1, so that V_{SD} becomes

$$V_{SD} = V_{in} - V_{out} = V_{in} - (V_{in} - V_{SG_1} + V_{SG_2}) = V_{o_1} - V_{o_2} \quad (3)$$

where V_{o_1} and V_{o_2} are the overdrive voltage of transistor M1 and M2 respectively.

The concept with static threshold cancellation can be adapted easily in the cc-bridge by replacing M_{p1} and M_{p2} with

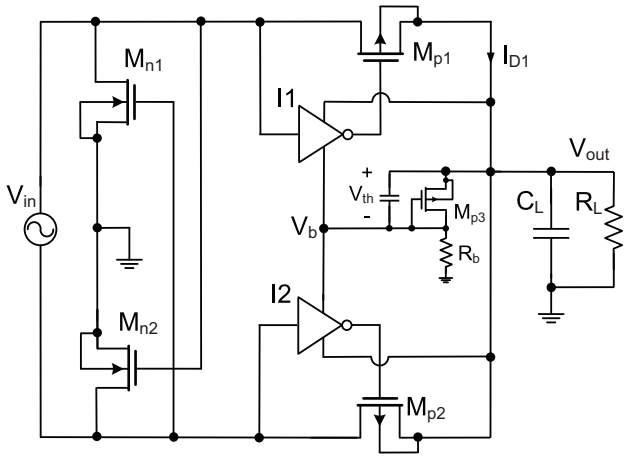

Fig. 6. Proposed rectifier. The leaking PMOS switches of the cc-bridge are replaced by diode-connected PMOS transistors with V_{th} cancellation in combination with inverters for minimized diode reverse leakage, to achieve both low turn on voltage and improved efficiency.

PMOS diodes because the drain of PMOS will be connected to the output voltage so that the V_{th}-generating diode will be forward biased. One problem with using static threshold cancellation MOS diodes comes from reverse leakage current that reduces the efficiency of the rectifier [8]. With the drain-gate fixed to V_{th}, the output transistor M1 will be biased in reverse when $V_{in} < V_{out}$, resulting in leakage in the off-state. In next section a simple technique that use inverters [12] to minimises this leakage is presented.

B. The proposed rectifier

The proposed modification of the cc-bridge is shown in Fig. 6. Here, the cross-connected PMOS switches are replaced by PMOS diodes with V_{th}-cancellation in combination with two standard PMOS-NMOS inverters, I1 and I2.

The purpose of the inverters is to turn the diodes off completely during half of a cycle to minimise diode reverse leakage, as illustrated in Fig. 7. Each inverter has its negative supply connected to the V_{th}-generating diode M_{p3} and its positive supply connected to the output so that the gates of M_{p1} and M_{p2} are connected to either V_b or V_{out}. During the positive phase of the input signal, the negative supply of I1 connects to the gate of M_{p1} so that its drain-gate voltage equals V_{th} and the static threshold cancellation is activated. Similarly, during the negative phase of the input signal, the positive supply connects to the gate so that the drain-gate voltage is zero and the reverse leakage is minimised.

In the design of the rectifier, the widths of M_{n1}, M_{n2}, M_{p1} and M_{p2} were optimised for both loads (35μm and 200μm for 100 kΩ and 2 kΩ, respectively) to achieve maximum power and voltage conversion efficiency. The inverters were optimised for maximum speed by minimizing channel widths of the NMOS-PMOS pair. Bias current in the V_{th}-generator was minimised by the proper choice of R_b as to limit power loss when the output voltage increases. In the critical case with low output power (100 kΩ load), when the loss in R_b becomes

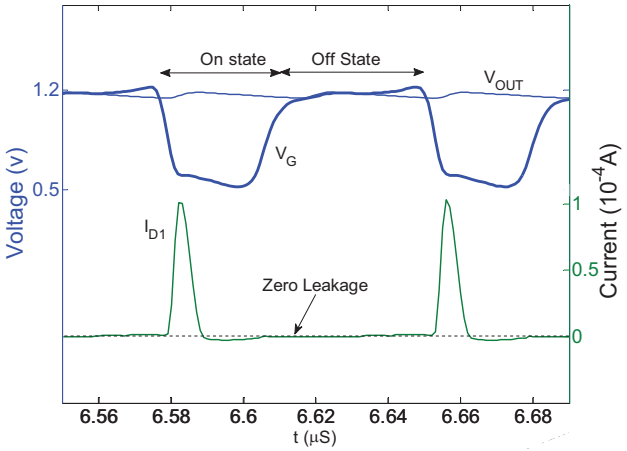

Fig. 7. Drain current I_{D1} and the gate voltage V_G of M_{p1} in the proposed rectifier simulated with the input peak voltage of 1.5 V at 13.56 MHz.

a larger fraction of output power, calculations show that the degradation of PCE due to the V_{th}-generator is below 7% for input voltages up to 2 V.

C. Power conversion efficiency

The efficiency of the cc-bridge have been analysed in [5] where loss in the NMOS and PMOS switches together with the impact of the reverse charge leakage as well as substrate loss is included. For the proposed rectifier, where the PMOS switches are replaced with diodes to avoid reverse charge leakage, the analysis below include loss in the PMOS diodes together with the loss due to the the V_{th}-generator, which are the main contributors to the loss, while loss in the NMOS switches as well as substrate loss can be neglected. Since the PMOS diode reverse leakage is minimised in proposed rectifier it is also neglected while the loss in the two inverters are neglected to simplify the analysis.

The efficiency of the cc-bridge with static threshold cancellation can be written as

$$PCE = \frac{P_{out}}{P_{out} + P_{loss}} \approx \frac{P_{out}}{P_{out} + P_{V_t} + P_{M1}} \tag{4}$$

where P_{out}=V_{out}^2/R_L. In order to achieve a useful expression of PCE, the output voltage is here approximated as $V_{out} = \hat{v}_{in} - \hat{v}_{SD} \approx \hat{v}_{in} - 0.3$ V. The loss due to the V_{th}-generator is given by

$$P_{Vt} = P_{M2} + P_{R_b} \approx I_b V_{th} + \frac{(V_{out} - V_{th})^2}{R_b} = \frac{V_{out}(V_{out} - V_{th})}{R_b} \tag{5}$$

From Fig. 5 (b) the loss due to the current pulse in M1 can be derived as below[13]:

$$P_{M1} \approx \frac{2}{\pi} \int_{\phi_1}^{\pi/2} (\hat{v}_{in} sin(\phi) - V_{out}) \hat{i}_D \frac{\phi - \phi_1}{\frac{\pi}{2} - \phi_1} \, \mathrm{d}\phi \tag{6}$$

where $\phi_1 = sin^{-1}(\frac{V_{out}}{\hat{v}_{in}})$. To find the peak current the input and output charge is written as

$$Q_{in} \approx \frac{1}{2}\hat{i}_D T_1 = \frac{1}{2}\hat{i}_D(\frac{\pi}{2} - \phi_1) \tag{7}$$

$$\text{and} \quad Q_{out} = I_{out} T_2 = \frac{V_{out}}{R_L}\frac{\pi}{2} \tag{8}$$

$$Q_{in} = Q_{out} \rightarrow \hat{i}_D = \frac{V_{out}}{R_L}\frac{\pi}{\frac{\pi}{2} - \phi_1} \tag{9}$$

The resulting PCE is plotted in Fig.8 for $R_L = 100k\Omega$ and $R_b = 300k\Omega$. Simulations showed that the discrepancy between the modelled and simulated efficiency is mainly due to the loss in the two inverters which were neglected in the model.

IV. Simulation Result

The proposed rectifier was designed and simulated in a 0.35 μm CMOS process. In order to verify performance in both the μW and mW range of chip power consumption, the rectifier was designed in two different versions. The power conversion efficiency was simulated based on the following equations:

$$PCE = \frac{P_{out_{DC}}}{P_{in_{RF}}} = \frac{V_{out}^2}{R_L * P_{in_{RF}}} = \frac{V_{out}^2}{R_L * P_{in_{RF}}} \tag{10}$$

$$\text{where } P_{in_{RF}} = \frac{1}{T}\int_0^T V_{in}(t) * I_{in}(t) \, \mathrm{d}t \tag{11}$$

The PCE of the proposed rectifier shown in Fig. 8 clearly reveals the improvement after eliminating the charge leakage in the cc-bridge. Instead of fast degradation with increasing input levels, the efficiency is almost constant at the maximum efficiency. Comparing Fig. 2 and Fig. 8, the cc-bridge shows about 10% higher peak efficiency around V_{in}=0.8 V with a load of 100 kΩ. This result can be explained as incomplete V_{th}-cancellation at low output voltages for the proposed rectifier while the cc-bridge has zero reverse charge leakage. Simulations with V_{in} from 2 V up to the oxide break down voltage 3.6 V showed a maximum power conversion efficiency of 70% for R_L=2 kΩ, and remained almost unchanged for R_L=100 kΩ. The output voltage characteristics in Fig. 9 and Fig. 10 show that the proposed circuit and the cc-bridge has comparable voltage conversion efficiency for both loads.

A simulation of the power dissipation in the rectifier was performed with a load of 100 kΩ and V_{in} 1.5 v. At an input power of 19.8 μW the power developed in the load was 13.1 μW. The loss in the PMOS pair, the two inverters and R_b was 4.5 μW, 1.2 μW and 1.0 μW respectively. The loss in the NMOS pair and the loss due to body leakage was negligible.

The two different versions of the proposed rectifier was also optimized and simulated at 125 kHz to evaluate performance for LF applications. As expected both rectifiers showed slightly improved performance where the proposed rectifier has an average efficiency around 75% up to V_{in} 2 V for both loads. Simulations with V_{in} from 2 V up to 3.6 V showed a power conversion efficiency reaching a maximum above 80% for R_L 2 kΩ, and remained almost unchanged for R_L 100 kΩ. The output voltage for the proposed circuit, compared

to the operation at 13.56 MHz, showed an improved linear characteristic instead of the weak dip around 1.3 V shown in Fig. 10. This improvement is a result of better inverter performance at lower frequencies.

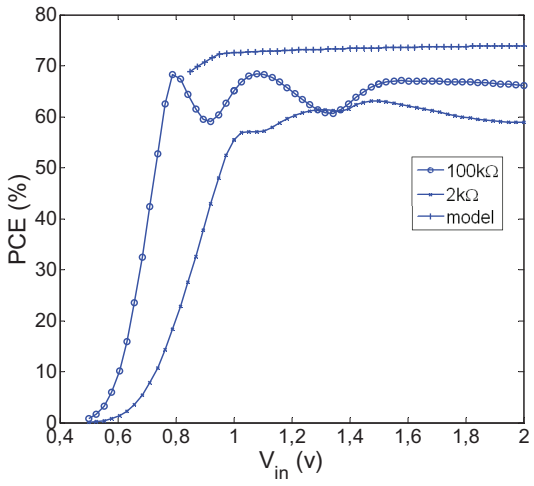

Fig. 8. PCE of proposed rectifier simulated with two different loads at 13.56 MHz.

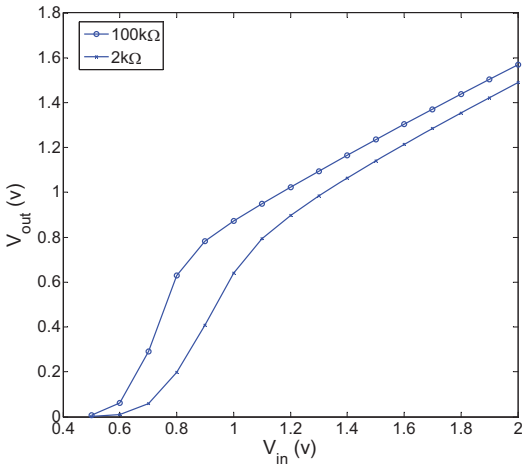

Fig. 9. Simulated output voltage of the cc-bridge at 13.56 MHz.

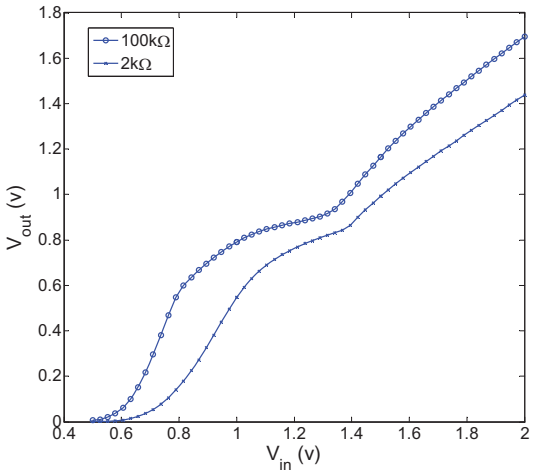

Fig. 10. The simulated output voltage of the proposed rectifier at 13.56 MHz.

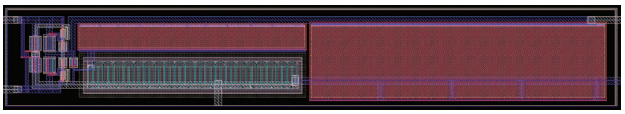

Fig. 11. Layout of the proposed rectifier.

V. Conclusion

In this work, a rectifier circuit based on the cc-bridge is presented that avoids reverse charge leakage and the resulting degradation of PCE with increasing input levels. The output PMOS pair in the cc-bridge is replaced with MOS diodes that employ static threshold cancellation in combination with minimised diode reverse leakage. A model for the power conversion efficiency of the proposed rectifier is developed and compared with simulations. The main advantage of this rectifier compared with earlier works is a simpler structure and high PCE from low to high input levels and without degrading rectifier sensitivity. A one-stage rectifier with a load of 100 kΩ generates a DC voltage in the range of 0.5 to 3.3 V at an efficiency above 60%. Instead of cascading bridges at their peak efficiency when generating the desired supply voltage, the proposed rectifier may be used to achieve a more robust overall DC voltage regulation system.

Acknowledgement

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