A High-Efficiency Low-Voltage CMOS Rectifier for Harvesting Energy in Implantable Devices

S. Saeid Hashemi, Mohamad Sawan, *Fellow, IEEE*, and Yvon Savaria, *Fellow, IEEE*

***Abstract*—We present, in this paper, a new full-wave CMOS rectifier dedicated for wirelessly-powered low-voltage biomedical implants. It uses bootstrapped capacitors to reduce the effective threshold voltage of selected MOS switches. It achieves a significant increase in its overall power efficiency and low voltage-drop. Therefore, the rectifier is good for applications with low-voltage power supplies and large load current. The rectifier topology does not require complex circuit design. The highest voltages available in the circuit are used to drive the gates of selected transistors in order to reduce leakage current and to lower their channel on-resistance, while having high transconductance. The proposed rectifier was fabricated using the standard TSMC 0.18μm CMOS process. When connected to a sinusoidal source of 3.3 V peak amplitude, it allows improving the overall power efficiency by 11% compared to the best recently published results given by a gate cross-coupled-based structure.**

***Index Terms*—Bioelectronics, bootstrapping technique, implantable devices, low-voltage devices, power efficiency, rectifiers.**

I. Introduction

PROGRESSES in microelectronics have resulted in miniaturized smart medical devices [1], [2], advances of radio frequency identification (RFID) tags [3], [4], as well as several types of sensors and body sensor networks [5]–[7]. These devices require energy sources for carrying out their intended functions.

Medical implantable devices dedicated to either sensing and treatment purposes are widely used to monitor and record targeted biological activities [1], [2], [8]–[12], and/or stimulate certain sites of neural or muscle tissues [13], [14]. In order to improve the efficiency of sensing and treatment by electrical stimulation, various forms of implantable devices are employed. These devices often use multi-channel sensing and stimulation through electrode arrays [13]. To support their operation, sufficient energy must be provided. As energy or power available to implanted devices is generally limited, efficient power conversion chains capable of handling sufficient power are strongly required.

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The authors are with the Electrical Engineering Department, Polystim Neurotechnologies Laboratory, Ecole Polytechnique de Montreal, Montreal, QC H3C 3A7, Canada (e-mail: saeid.hashemi@polymtl.ca).

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Classical powering techniques, including embedded batteries [15] and transcutaneous power harvesting methods [1] are relatively constrained in terms of energy density, device lifetime, potential hazards to human safety, integration, and physical size. Moreover, despite remarkable efforts dedicated to developing power harvesting techniques to scavenge power either from the environment or from the human body, these techniques are not yet considered reliable and feasible, but research is steadily progressing [16], [17]. Thus, procuring adequate energy to power electronic implants remains challenging.

Recently reported experimental systems commonly use inductively coupled links to wirelessly deliver needed energy over short distances. This technique suffers from extremely low power transfer efficiency due to poor electromagnetic coupling, skin absorption, and narrow band-pass. It is important to mention that a more efficient rectifier can deliver a given amount of power for a lesser voltage induced across the secondary coil of the link. Thus, for a certain PCC, it requires a smaller coupling coefficient and allows for a greater relative distance between the coils.

Gate cross-coupled rectifiers have been proposed by [18]. In this topology, two diodes of the classical diode rectifier are replaced by two cross-coupled MOS transistors. They introduce a full-wave rectifier constrained with a single threshold voltage (V_{Th}) instead of two, which is the case for conventional bridge full-wave rectifiers.

Another rectifier topology proposed by [19] is the use of the bootstrapped capacitor technique that allowed reducing the effective threshold voltage of a diode-connected transistor to the difference between two threshold voltages. In this paper, we propose a new rectifier configuration for medical implantable devices. It combines the gate cross-coupled configuration with the bootstrapped technique to build a new rectifier architecture that has a voltage drop smaller than the other configurations and that is capable of handling large load currents.

The remainder of this paper includes, in Section II, the architecture and characteristics of passive- and active-rectifier topologies. Section III introduces a short review on different threshold cancellation techniques. Section IV presents a new topology for a full-wave rectifier along with its circuit description. Section V presents simulation and measurement results of the proposed device, as well as a comparison between different topologies followed by concluding remarks in Section VI.

II. Rectifier Topologies and Threshold Cancellation Techniques

Wideband power rectifiers are commonly used within the power conversion chains to convert an input AC signal to an unregulated DC supply using diodes.

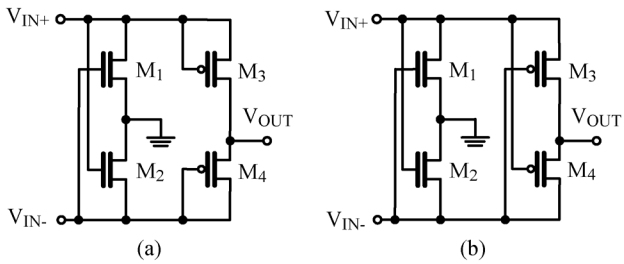

Fig. 1. Schematics of full-wave rectifiers. (a) Gate cross-coupled. (b) Fully cross-coupled.

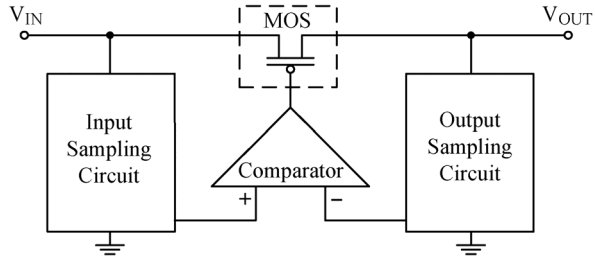

Fig. 2. Block diagram of active rectifier typical configuration.

A. CMOS Rectifier Implementation

In standard CMOS processes, the diodes are commonly replaced with diode-tied MOS transistors that are easier to implement. Here, the structure is still affected by the threshold voltage (V_{Th}) and instantaneous voltage drop across the transistor-based switches due to their channel resistances results in degrading the overall power efficiency and reducing the output voltage. On the other hand, Schottky diodes with a low forward drop are possible, but their implementation is expensive, due to the extra fabrication steps that they imply as they are not available in standard CMOS processes [20]. It is worthy to note that with technology evolution, the required power to operate multi-function devices tends to grow with the application needs and sophistication of their modes of operation. This makes the structure increasingly inefficient in advanced low-voltage sub-micron processes, where the ratio of the normal supply voltage to the threshold voltage of MOS transistors decreases. Bridge full-wave rectifiers (FWBR) are popular version of full-wave rectifiers. They offer higher power efficiencies, smaller output ripples and greater reverse breakdown voltages compared with their counterpart, the half-wave rectifiers [18].

The full-wave gate cross-coupled rectifier (FWGR) shown in Fig. 1(a) was introduced in [18]. The rectifier works such that, in each signal cycle of the circuit, the threshold voltage of one diode-connected MOS transistor is replaced with the effective voltage drop across a MOS switch. The other advantage of such rectifier is to drive the gate of the said MOS transistor with a voltage swing higher than those commonly used with diode-connected structures, which reduces the switches' leakage and improves their conductivity. The resulting rectifier produces higher power efficiency than conventional FWBR structures; however, in each source cycle, it uses a single diode-connected MOS transistor for load connections and thus suffers from the associated (threshold) voltage drop.

Full-wave fully gate cross-coupled rectifiers (FWFR) are also introduced, where the transistors in the two main branches are cross-coupled [21]. Here, unlike the previous rectifier, all the main pass MOS transistors are cross-coupled as illustrated in Fig. 1(b). This circuit solves the problem of threshold voltage drop by diode-tied MOS transistors. However, it was shown that such a structure does not present good power efficiency due to flow-back current from the storage capacitor to the antenna, and other parasitics [22].

Another approach for improving power efficiency of rectifiers relies on active circuit to control pass transistors in place of diodes or diode-connected transistors. Fig. 2 depicts the typical conceptual structure of so-called active rectifiers. As the source is nominally a sine wave, one circuit of this kind is often needed for each phase (positive and negative).

At each source cycle, a comparator regulates the conduction angle of the relevant pass device based on simultaneous comparison between the information obtained from input and output. In this way, the conduction angles of the MOS switches with respect to the sinusoidal source are managed based on the source characteristics and load requirements. These designs are reported to have higher power efficiencies compared to passive topologies [23]–[27] and to generate less heat [28]. There are new active designs where a combination of the classical approach (as above) and the gate cross-coupled structure is employed [29]. Recently, a new version of this class of rectifier was introduced, which is using the inherent characteristics of selected MOS transistors as comparators working in the triode region, where they present very low voltage drops [30].

In spite of the advantages that the active configuration brings, the internal structure of those circuits consumes some additional static power to operate. This can be very challenging as there is no regulated power available at the starting point of the rectifier. This often outweighs expected benefits of active rectifiers when compared to the passive structures, and it limits their application mostly to the circuits leveraging some alternate solution such as: an auxiliary power source, a large capacitor to power up active devices and peripherals [29] or a second parallel lower efficiency rectifier for bootstrap [31]. Another major drawback of many active rectifiers occurs at higher frequencies. The pass transistors are usually very large in order to reduce the voltage drop and handle enough load current, and thus have significant parasitics which must be driven by the active circuitry. This requires more current at higher frequencies and reduces the power efficiency accordingly.

B. Threshold Cancellation Techniques

Threshold voltage is a process-dependent parameter which depends on the choice of oxide and on oxide thickness. Some standard CMOS processes offer low- and medium-threshold devices which could be employed to realize low-threshold designs. However, their availability is not generalized yet, and the implemented devices are subject to significant leakage due to higher channel doping leading to excessive power consumption and reliability problems. Thus, low-threshold devices are generally not good candidates to put in the main flow of current towards the load.

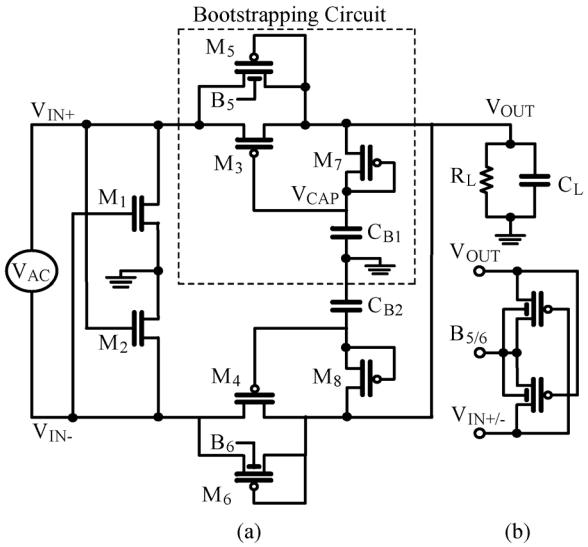

Fig. 3. (a) Schematic of the proposed full-wave rectifier. (b) Schematic of its dynamic bulk biasing circuit for diode-tied transistors of M_{5-6}.

Various circuit techniques are available to alleviate the impact of V_{Th} when turning-on transistors using additional biasing circuitries in a standard CMOS process. They often benefit from using additional biasing circuitry in a standard CMOS process in the form of either a bootstrap capacitor [19] or some dynamic techniques for gate-drain [32] or bulk-source (body-effect) biasing [33]. With these techniques, a DC voltage is generated in an idle phase to eliminate or reduce the effect of V_{Th} in the working phase.

Another approach involves using a floating gate technique to regulate the threshold voltage of given MOS transistors [34]. This technique requires high voltage to program the threshold voltage during set up and erase phases which implies new implementation constraints. They are also restricted to low operating frequencies.

Among the above cited techniques, the bootstrapping approach is the most adapted with standard CMOS integrated circuit design. This method is outlined in the upper part of Fig. 3(a). Here, the diode-connected transistor (DCT), M_5, forms an auxiliary path which provides the required current to charge up the bootstrapping capacitor at start up via another DCT (M_7). The charges stored on C_{B1} are then simultaneously applied to the gate of M_3, the main pass pMOS transistor.

When the input voltage (V_{IN}) is higher than the output voltage (V_{OUT}) by at least the diode forward-bias voltage drop (V_{Th5}), current flows through the diode-tied transistor M_5 and charges the output capacitor. As the output node is being charged, the voltage across the capacitor, V_{CAP}, is also charged through M_7. Recall that, for a given process, ignoring body-effect due to different bulk biasing and process variations, the threshold voltage of the same type transistors are nominally the same, that is, $V_{Th5} = V_{Th7}$. Therefore, the voltage held on the capacitor is twice as high as the pMOS threshold voltage below the input voltage. Considering these facts, it can be shown [19] that the output voltage reaches

$$V_{OUT} = V_{IN} - (|V_{Th3}| - |V_{Th7}|) \quad (1)$$

where V_{Th3} and V_{Th7} are the threshold voltages of the main pass pMOS switch and M_7, respectively.

From (1), the effective V_{Th} of the circuit is reduced compared to that of the conventional diode-connected pMOS structure. Therefore, with a typical MOS transistor threshold voltage, the use of this technique could result in increasing the output voltage range for a given input source voltage. This becomes increasingly significant with new deep sub-micron technologies where the nominal supply voltage of the integrated circuits is less than 1 V.

This technique was applied to a conventional half-wave rectifier built using a voltage-doubler based structure [19]; however, the structure failed to present improved characteristics as expected. The rectifier required very large holding capacitors to procure miliampere-range current. This is due to its nature, which relies on pumping charges from source towards the load. The structure was also slow compared to other structures, as it needs frequent charging and discharging of the involving capacitors. For rectifier using very large capacitors, even with large switches, it results in relatively long settling times. Moreover, the need for remarkably large charge holding capacitors, in the micro-Farad range, is against the objective of implementing the rectifier using standard integrated circuits. The design was also reported as being subject to significant leakage through bulk of transistors, which deteriorate the power efficiency.

III. The Proposed Rectifier

In order to improve the power conversion efficiency (PCE) and increase the output voltage for a given input source amplitude, we propose a new full-wave rectifier (FWNR). It employs a pair of pMOS switches with very low effective threshold voltage to replace the diodes or diode-connected pMOS transistors found in previously reported structures.

The design also benefits from the advantages of gate cross-coupled structures applied on selected MOS transistors. This allows driving the gates of the nMOS transistors with a voltage swing larger than what would be found in conventional structures exploiting diode-connected nMOS transistors. Hence, a higher ON/OFF current ratio can be achieved. Fig. 3(a) provides the schematics of the proposed full-wave rectifier.

The design uses the Dynamic Bulk Switching (DBS) technique to bias the bulk of selected transistors, in order to reduce the leakage current through bulk. Small bootstrapping capacitors were used to reduce the effective threshold voltage of the main pass transistors and to ensure the rectifier holds its functionality along with significant power and voltage efficiencies over a wide range of source voltages. C_{B1-2} can be built using a standard CMOS process.

The modified rectifier operates very much like the gate cross-coupled rectifier [18]. In the input positive cycle, M_3 provides the main conduction path from the source to the load and charges the output reservoir, C_{B1}. The gate cross-coupled nMOS transistor (M_2) provides a low impedance return path for the current charging C_L.

Although the circuit branch (auxiliary path) that includes the diode-connected M_5 is mainly inserted to provide a path between the input and the output nodes to charge the holding ca-

pacitor (C_{B1}), simultaneous conduction of M_3 and M_5 contributes to the output current. Such diode-connected MOS transistor (M_5) does not significantly compromise the overall power efficiency, due to its remarkably small size (large channel resistance) compared to the main path transistor (M_3), which has a much larger size (to produce the desired small channel resistance).

Thus, the bulk of the load current flows through M_3, the transistor for which the effective threshold voltage is significantly reduced by the bootstrapping capacitor connected to its gate. In fact, as only a small part of the load current passes through M_5 in steady state regime, its contribution to power losses of the rectifier remains small. The combination of M_5, M_7, and C_{B1} provides the biasing that reduces the effective threshold voltage of M_3. In negative cycles, the dual circuit (consisting of M_2, M_4, M_6, M_8, and C_{B2}) will rectify the input voltage in the same manner.

The design should be optimized by adjusting the sizes of the transistors to operate at different source frequencies. This is necessary to attain adequate time constants for the charging paths of the bootstrapping capacitors. Various simulations demonstrate that the new rectifier topology can operate over a wide range of operating frequencies up to 60 MHz provided adequate optimizations are performed.

The new design is simple and does not require complex circuit design techniques. Another advantage of the new design is its compatibility with standard CMOS processes, which allows implementing sufficiently large embedded capacitors. Obviously, a rectifier designed with a fixed size constraint must trade off the size of the main switch and the area dedicated to the bootstrapping capacitors.

The source of the pMOS transistors that are connected to the floating signal source terminals (M_{5-6}) see their voltage vary greatly over time. They go above V_{OUT} and below the ground voltage and, therefore, the exposed transistors could inject (leakage) currents in the substrate and induce latch-up. Therefore, DBS, as illustrated in Fig. 3(b), is essential [35]. Using this technique, the bulk of the auxiliary path transistors, M_{5-6}, are selectively connected to the highest available voltage (either V_{OUT} or input source). Note that implementing such bulk biasing requires locally isolated wells or substrate. In the proposed configuration, this is realized by using separate n-well for the pMOS devices used for biasing.

Another advantage of this DBS configuration is eliminating the body effect on the rectifying pMOS transistors, where this technique is applied, thus reducing the rectifier dropout voltage and power dissipation at start up. Since no sustained current passes through DBS transistors when they turn on, their drain-source voltage is close to zero [36]. The dynamic bulk biasing circuits are not shown in the schematics of Fig. 3(a) for simplicity. It was observed that dynamic biasing of the bulk terminals of the main pass transistors (M_{3-4}) may significantly reduce the overall power efficiency. Indeed, they remained off when the voltage difference between their source and gate was too low to allow conduction. Therefore, the bulk of the main pass transistors (M_{3-4}) was connected to V_{OUT} as it is the highest voltage available during the majority of the rectifier operating time due to the presence of an output charge reservoir.

The size of the main pass transistors (M_{1-4}) was optimized with respect to the associated parasitic in order to handle specified load currents with a sufficiently small channel resistance. Considering the time constant associated with the charging path of the bootstrapping capacitor and in order to get the best performance, it is necessary to inject enough charges into the bootstrapping capacitor (C_{B1} or C_{B2}). Thus, the sizes of transistors M_{5-8} should be selected carefully. Similarly, transistors M_{7-8} need to be sufficiently large.

It is of interest that some gate oxides and junctions may be subject to instantaneous voltage stress. Significant design efforts were invested to limit the current passing through the junctions and to ensure that all transistors remain in safe operating regions. A detailed study of possible instantaneous voltage stress was left for future research.

IV. Simulation and Measurement Results

Power Conversion Efficiency (PCE), output average voltage, and Voltage Conversion Ratio (VCR) are the performance metrics commonly used to compare different rectifier structures [30].

The proposed rectifier was implemented at the circuit level using the standard TSMC 0.18 μm CMOS process with 3.3 V nominal supply voltage, and then characterized with the SpectreS simulator in the Cadence environment. A shunt load of $C_L = 200$ pF and $R_L = 2$ kΩ is considered. This load condition, when combined with applying a sinusoidal voltage source peak amplitude of 5 V and frequency of 10 MHz, leads to a load current up to 2.3 mA. This load condition fits the requirements of an intracortical stimulator implant application developed in our laboratory.

The main paths transistors (M_{1-4}) sizes are 20/0.35 μm with multiply factor of 50. Diode-tied transistors of M_5/M_6, which form the auxiliary paths are 1/0.35 μm, while the diode-connected transistors M_7/M_8 are implemented using 6/0.35 μm size transistors with multiply factor of 50. Small size pMOS transistors (0.50/0.35 μm) are employed to form DBS structures for dynamic bulk biasing of auxiliary path transistors. The size of bootstrapping capacitors (C_{B1-2}) is selected as 50 pF.

Power efficiency of a rectifier for a given operating current is a function of its maximum rating and how its key components were sized to support that rating. For instance, larger W/L may lead to higher peak current ratings, but may degrade efficiency due to increased leakage current and CV^2 losses. Similarly larger holding capacitor may be needed for higher current rating, but they can limit response time and increase substrate losses. There is no simple relationship that allows finding the best component sizing for a giving set of target specifications. Sizes leading to the reported performances were obtained by a manual optimization process.

A. Simulation Results

In this section, we compare the simulation results of the FWBR and the FWGR [18] structures discussed earlier with our new proposed FWNR. Fig. 4 shows the simulation results characterizing the PCE variation versus the peak input amplitude for these different structures using the same sizes for the main pass transistors (M_{1-4}) and load as already stated.

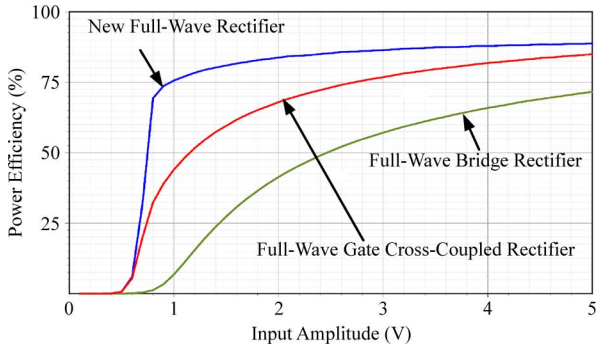

Fig. 4. Simulated power conversion efficiency versus input peak amplitude.

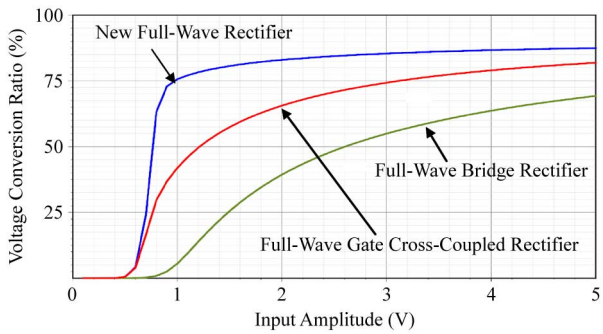

Fig. 5. Simulated voltage conversion ratio versus input peak amplitude.

The FWNR presents significantly higher power conversion efficiency over a wide range of input peak amplitude greater than 0.8 V. Its power efficiency is remarkably higher than that of the other structures. With a 3.3 V AC source peak amplitude, the new rectifier offers a power efficiency up to 87%, which corresponds to an improvement by up to 11% and 47% compared to the FWGR and FWBR topologies, respectively. These improvements result from the reduced effective threshold voltage, which leads to lower voltage drop across drain-source terminals of the pMOS main switches (M_{3-4}) and, from the large V_{GS} in cross-coupled nMOS transistors, M_{1-2}, which results in higher gm and lower channel on-resistance.

Simulated VCRs for different topologies are also illustrated in Fig. 5. The results confirm that the circuit maintains its functionality as a rectifier even for a very low source voltage. It presents voltage conversion ratio larger than 70% for an AC input source with 0.8 V peak amplitude. This is significantly higher compared to other topologies.

Fig. 5 also reveals that for the FWNR structure, the voltage conversion ratio rapidly reaches high values at low input source voltages, and remains the best for larger input voltages.

The significance of the new design with respect to VCR could be better visualized from a graph, in which the ratio of average output voltages for the FWNR and the FWGR structures is plotted. It was shown in [37] that the average output voltage for the FWNR is significantly higher than that of the FWGR, particularly for peak input voltages between 0.6 V to 2.2 V. For example, at 0.8 V input amplitude, the proposed FWNR produces an output voltage almost 2.1 times larger than the FWGR. Therefore, one may expect that the new

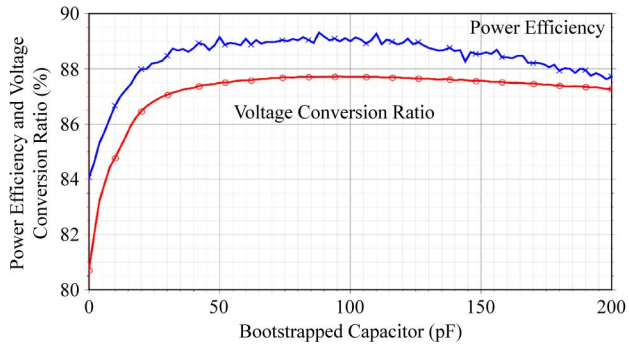

Fig. 6. Simulated power efficiency and voltage conversion ratio versus bootstrapped capacitor size.

design could be applicable to implement integrated rectifiers using new advanced sub-micron CMOS technologies where the nominal supply voltage is below 1 V. Based on separate simulation results, at 0.8 V input amplitude, the VCR is much larger when comparing FWNR and FWBR structures.

An important design concern could be the size of bootstrapping capacitor. Integrated capacitors consume considerable area on the die when implemented using standard CMOS processes. Fig. 6 shows how the PCE and VCR vary with the bootstrapping capacitor size. It shows that over a wide range of capacitance, the design performance in terms of PCE and VCR is not very dependent on the size of the embedded capacitors. The decrease in the PCE and VCR for bootstrapping capacitors larger than 100 pF could be explained by the impact of significant changes in the time constants of charging paths of the said capacitors as already addressed in Section III.

Considering the same input source amplitude, the rectifier with larger bootstrapping capacitors requires longer time to attain the adequate voltage. Therefore, for a given time frame, depending on the period of the input source, the gate-to-source voltage of the main pass transistors will be reduced, which causes them to represent smaller conductance. The results confirm that the new rectifier works very well with 50 pF capacitors which are feasible with standard CMOS processes.

B. Measurement Results

The proposed full-wave rectifier was fabricated using a 0.18 μm 6-Metal/2-Poly TSMC 3.3 V standard CMOS process. The die photomicrograph is provided in Fig. 7. This chip measures 780 μm $\times$ 780 μm and it is mounted in 40 pin dual-in-line package. Local substrates, needed for applying the DBS technique, were implemented using the deep n-well layer. All the main switches are surrounded by guard rings to isolate them from adjacent cells. In agreement with 3.3 V design rules, all transistors have channel lengths of 0.35 μm to maximize the speed of operation. The chip was carefully laid out to have a symmetrical structure minimizing potential imbalance in parasitic capacitances between the source rails ($\mathrm{V}_{\mathrm{IN}+}$ and $\mathrm{V}_{\mathrm{IN}-}$). Pads with electro-static discharge (ESD) protection are used to feed the input source signal into the chip. The ESD supply voltages ($\mathrm{V}_{\mathrm{DD-ESD}}$ and $\mathrm{V}_{\mathrm{SS-ESD}}$) are directly accessible.

1) Measurement Setup and Test Protocol: To measure the performance of the fabricated rectifier, the measurement setup

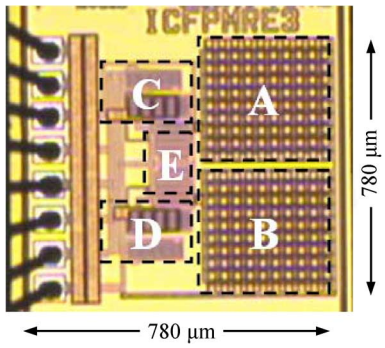

Fig. 7. Photomicrograph of the prototype chip; A and B highlight bootstrapped capacitors (C_{B1-2}), C and D address main pass transistors (M_{1-4}), and E marks the bootstrapping (M_{5-8}) and dynamic bulk biasing circuitry.

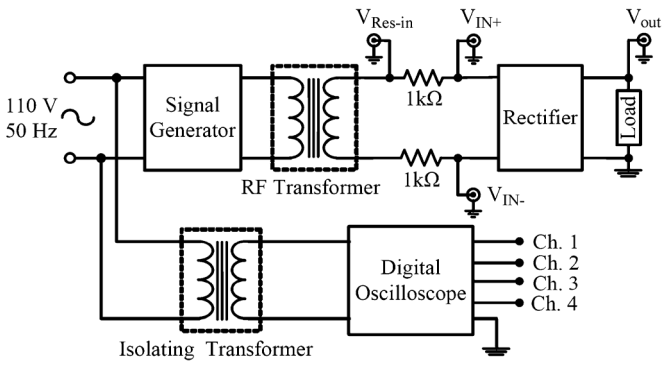

Fig. 8. Voltage and power measurement setup.

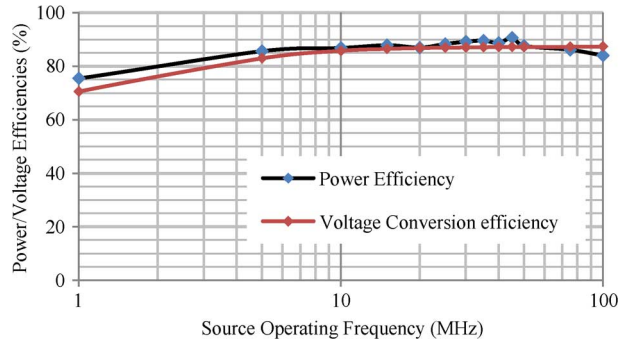

Fig. 9. Simulated frequency response of the proposed rectifier.

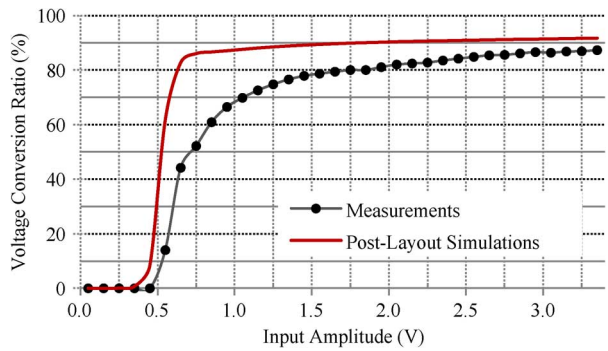

Fig. 10. Measured voltage conversion ratio of the proposed full-wave rectifier versus input amplitude operating at $f = 10$ MHz.

shown in Fig. 8 was used. The rectifier implemented in this design requires a truly floating input signal to act as a full-wave rectifier. A wideband RF transformer with small insertion and return losses was used as an interface between the signal generator and the rectifier. Note that no terminal of the RF transformer secondary is at ground potential. This transformer is responsible to transfer energy to the rectifier inputs.

The input voltage to the rectifier is not referenced to ground. Therefore, the oscilloscope cannot be used to view both the input and the load voltages of the rectifier at the same time. On the other hand, simultaneous measurements are required to increase reading accuracy. A solution to this problem is to use an isolating transformer (1:1) to decouple the oscilloscope from the common ground. This isolation helps avoiding ground loops (especially at operating frequencies in the mega hertz range) in the setup; it also allows referencing the output signal to voltages other than ground. Experiments confirmed that the use of these transformers is a necessity for proper operation.

The input power to the rectifier was measured as the integral of the instantaneous product of the input voltage by the input current over one period of the source. The output power was calculated as the integral of the squared measured output voltage divided by the load resistance over a period. The VCR was calculated as the ratio of the average output voltage to the input peak amplitude.

The input current was calculated using the measured drop voltage across a resistor in series with the RF transformer. The charge holding elements present at the output comprise a 200 pF explicit capacitor in addition to the capacitance of the output pad, of the package parasitics and of the probe of the test equipment. With an input sine wave peak voltage of 3.3 V operating at 10 MHz, the average output voltage was measured to be 2.89 V. This measured voltage represents a VCR of 87% at the given frequency.

A number of different source frequencies were applied to the laid-out rectifier that its results are shown in Fig. 9. Here, the same rectifier which its elements were optimized such that the rectifier presents the maximum power at 10 MHz operating frequency, was used. It is of interest that the parameters producing maximum power efficiency may not be the same as those that produce maximum voltage efficiency. It was noted that, as expected, higher source frequencies produce larger power efficiency and average output voltages, which the later results in larger VCRs. Fig. 10 illustrates the measured and the post-layout simulated VCRs for the same no-load condition (except parasitics associated with probe and pads) at 10 MHz source frequency. At 1.0 V, 1.8 V, and 3.3 V AC peak input amplitudes, voltage conversion ratios of 70%, 80%, and 87% are obtained.

The deviation of the measured results compared to post-layout simulations can be explained by the impacts of two phenomena; 1) the charge sharing between the bootstrapping capacitors and the parasitic capacitances, and 2) the leakage to the bulk of the main pass transistors. For applications with high operating frequency, as encountered in biomedical implants, parasitic capacitors associated with MOS terminals and interconnections should be considered. Many parasitics in the proposed circuit cannot be modeled as capacitors in parallel with the bootstrapping capacitors. Depending on their representations, they might contribute in further charge accumulation

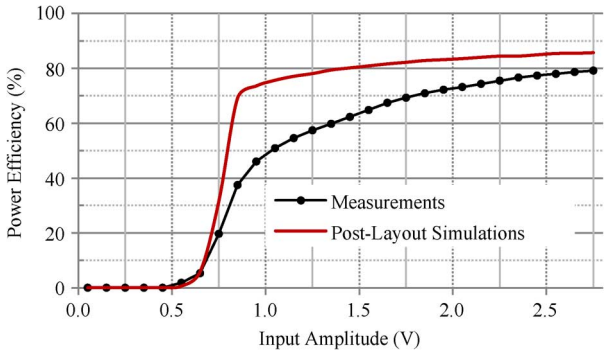

Fig. 11. Measured power conversion efficiency of the proposed full-wave rectifier operating at $f = 10$ MHz.

producing more efficient bootstrapping or in charge sharing degrading the efficiency of the said technique.

Nevertheless, from the observation of the results presented in Fig. 6, one may consider the charge sharing effect to be less affecting the VCR of the circuit than the leakages current, and hence ignore it. This is not particularly true due to lack of accurate simulation models to emulate the representation of the parasitics and to predict their impact on the performance of the rectifier. It is of interest that leakage through bulk to the rectifier output contributes in load current. Depending on the portion of the load current passing through the source-to-n well junction, which is connected to output node, the rectifier efficiency varies.

In the measurements, parasitic capacitances consist of the parasitics associated with the gate of the extremely large main pass pMOS transistors (M_{1-4}), the large interconnection metal strips, and the significant parasitics capacitances associated with the output pads and oscilloscope probe. In fact, the occurred charge sharing may result in wasted charges, which reduces the output voltage. The results are more affected at low voltages, where the threshold reduction technique is less effective due to slow switching. However, the measured results are significantly better than that of the other topologies.

Fig. 11 depicts the measured power efficiency versus input amplitude for the rectifier with a 2 $k\Omega$ load resistance shunting a 200 pF capacitance, at source frequency of 10 MHz. The overall power efficiency is measured to be 37%, 71%, and 80% at 0.8 V, 1.8 V, and 2.7 V peak input source amplitudes.

Here, the difference between the results obtained from simulations and measurements could be explained by the fact that significant leakage currents flow through the bulk of the main pass pMOS transistors (M_{1-4}) considering the fixed biasing of the bulk when the source is floating. In the proposed rectifier, the bulk of M_{1-2} is connected to the ground while the bulk of M_{3-4} is connected to V_{Out}. Therefore, depending on the load and floating source conditions, there will be time intervals when the parasitic vertical diodes, formed between n-well and substrate of the said pMOS transistors, become forward biased, which leads to significant leakage current to their substrate. Thus, protecting the main pMOS transistors against the bulk-to-substrate leakage is crucial. This could be done using the DBS technique as explained for auxiliary paths transistors, M_{6-7}. However, it was found that applying the said technique does not improve the efficiencies due to very short time intervals when the gate-to-source voltage of DBS transistors is not sufficient to form their channels, a necessary condition for the main pass transistors to operate.

TABLE I
POST-LAYOUT AND MEASUREMENT RESULTS

Metrics	Post-Layout Simulations			Measurements		
Source peak Amplitude (V)	0.8	1.8	2.7	0.8	1.8	2.7
Power Efficiency (%)	69	83	86	37	71	80
Average Output Voltage (V)	0.5	1.5	2.3	0.3	1.2	2.0

Moreover, the circuit employs pads with ESD protection implemented using the vertical parasitic diodes formed between diffusion, n-well and substrate. Here, p-diodes are used for directing the input spikes towards the V_{DD-ESD} ring and n-diodes are used for suppressing them using the V_{SS-ESD} ring. In our implementation, there are two parallel p-diodes and two parallel n-diodes used for such protection. The p-diode, n-diode, and n-well diode are respectively subject to a 200 nA, 400 nA, and 650 nA reverse bias current.

Considering the fact that there are 6 pads used for accessing the rectifier, the leakage current through these diodes can be calculated to be 2.4 μA, 4.8 μA and 7.8 μA, respectively. Assuming that normal operation of the rectifier involves all those parasitic diodes to be reversely biased, there are cases where all this leakage occurs simultaneously, leading to a leakage of 15 μA. At a low input voltage, and considering the charge sharing phenomenon as explained in the analysis of the results in Fig. 10, this leakage may constitute more than 10% of the total power consumption of the rectifier. Thus, using proper biasing for the bulk of the main pMOS transistors and using probe connections on die instead of pads, may make measurements and post-layout simulation results more consistent.

Based on a separate observation, measurements confirm that the power efficiency decreases with the load current. This may be due to an increase of the power consumption within the channel of the main pass and auxiliary paths transistors, as well as the leakage current from the source to the bulk of the main pass transistors. Recall that these leakages contribute to the load current when V_{IN} is higher than V_{OUT}. Table I summarizes the results obtained from the post-layout simulation and the measurements for a load of 2 $k\Omega$ in shunt with a 200 pF capacitance.

Unfortunately, the existing differences in terms of process and feature sizes, prevents us to be able to compare all reported characteristics of the state-of-the-art rectifiers. However, among the designs using standard CMOS processes with given feature size, for the same source amplitudes as reported in Table I, the result of the comparison, as stated in Table II, confirms that, the proposed rectifier topology generates the best output voltage and power efficiency compared to other reported results particularly when operating from low source voltages.

The advanced rectifiers rarely provide large load currents, which is the case for most biomedical implantable devices. The

TABLE II
COMPARISON WITH MOST ADVANCED RECTIFIER CHARACTERISTICS

Rectifier Topology	Process	Source Amplitude (V)	Output Voltage (V)	Power Efficiency (%)	Load (kΩ)
Gate Cross-Coupled [18]	BiCMOS 1.50 μm	9.0	6.54	-	1
V_{TH} Reduction [19]	CMOS 0.25 μm	2.5	0.9	55	20
Self V_{TH} Cancelation [38]	CMOS 0.18 μm	1.8	-	32	10
This Work	CMOS 0.18 μm	0.8	0.3	37	2
		1.8	1.2	71	
		2.7	2.0	80	

proposed rectifier and the gate cross-coupled rectifier, even with elements implemented using sub-micron CMOS integrated circuits, are capable of handling significant load currents, as large as a few mA. However, the gate cross-coupled topology uses a BiCMOS process, with significantly longer feature size compared to the standard deep sub-micron CMOS process used in fabricating the proposed rectifier.

Remember that charge-pump-based (voltage doubler) rectifiers realized using small charge reservoirs do not maintain large charges and, therefore, fail to provide significant current. Simulation-based results of implementing the gate cross-coupled structure in deep sub-micron technologies confirm that the resulting rectifier is not power and voltage efficient at low source voltages. Other advanced rectifiers implemented in smaller feature sizes (except the rectifier in [38]) provide neither large load currents, nor present high power efficiencies. Some of them [19] require large off-chip capacitors in the micro-Farad range which makes their implementation unfeasible in advanced integrated circuit processes. Measurements reported in [38] also confirm that the said rectifier is not a good candidate for implementing rectifiers with high voltage and power efficiencies when using low source voltages.

The stated results for voltage conversion ratios could be explained as the result of leakage through bulk terminals of the main pass transistors and of the flow-back current from output node toward the source when the output voltage is larger than the inputs. Charge sharing between the bootstrapping capacitor and the parasitic capacitances associated with the gate of the main pMOS pass devices may caused result derivation. The leakage currents due to use of large ESD protection diodes and the parasitics associated with the interconnections could also be considered as other potential reasons for the drift in simulation and measurements.

As a general design practice, the reported implementation uses ESD (electrostatic discharge) protected pads. The full impact of this design choice was fully appreciated when the prototype circuit was experimentally tested. Even though dedicated V_{SS} and V_{DD} pads that can be tied to suitable voltage allow mitigating this effect in our prototype, we noticed that leakage paths to the substrate can be activated. ESD protection with this class of circuit can become a challenging issue that was left for future research.

From power efficiency standpoint, the measured results are in agreement with simulations if the proper bulk biasing technique is employed to bias the bulk of the pMOS main transistors and the leakage through large ESD protection diodes is mitigated.

It was also noted that for peak voltages higher than 1.8 V, the power efficiency is significantly reduced. It is conjectured that the main pass transistors have significant leakage currents resulting from voltage stress. Table II presents the comparison between the measured characteristics obtained from the proposed rectifier and the most advanced full-wave rectifiers described in the literature. Note that the performance of respective circuits is quoted for different load conditions and processes.

V. CONCLUSIONS

A full-wave integrated rectifier was presented. It is suitable for many applications including smart biomedical implants and RFID tags. The structure does not require complex circuit design. The new design employs MOS-based gate cross-coupled nMOS switches along with pMOS switches equipped with reduced effective threshold voltage technique to achieve AC to DC conversion. The simultaneous application of a cross-coupled structure and threshold reduction techniques can result in very low voltage drop across the MOS switches. The rectifier also uses dynamic body biasing in auxiliary paths. This design has been fabricated using the standard 0.18 μm 3.3 V TSMC CMOS process. The schematic and post-layout simulations confirm significantly higher power and voltage efficiencies of the proposed rectifier compared to other advanced rectifier structures. The measurements also confirm that the proposed rectifier provides a higher voltage conversion ratio than previously reported designs. It also confirms that the use of the proposed rectifier is advantageous, particularly when the power supply source voltage is low.

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S. Saeid Hashemi received the B.Sc. degree in electrical engineering from Iran University of Science and Technology, Tehran, Iran, in 1987, and the M.Sc. degreee in electrical engineering from Ecole Polytechnique de Montreal, Montreal, QC, Canada, in 2004.

Currently, he is working toward the Ph.D. degree at Ecole Polytechnique de Montreal. His thesis topic involves the design and implementation of low-voltage high-efficiency integrated rectifiers. He is interested in analog and mixed-signal IC design for low-power and low-voltage applications.

Mohamad Sawan (S'88–M'89–SM'96–F'04) received the Ph.D. degree in electrical engineering from Université de Sherbrooke, Sherbrooke, QC, Canada, in 1990.

He joined Ecole Polytechnique, Montréal, QC. Canada, in 1991, where he is currently a Professor of microelectronics and biomedical engineering. His scientific interests are the design and test of analog and mixed-signal circuits and systems, signal processing, modeling, integration, and assembly. He holds the Canada Research Chair in Smart Medical Devices, and he is leading the Microsystems Strategic Alliance of Quebec (ReSMiQ). He is Deputy Editor-in Chief of the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS III, Associate Editor of the IEEE TRANSACTIONS ON BIOMEDICAL CIRCUITS AND SYSTEMS, and Editor of the Springer *Mixed-Signal Letters*.

Dr. Sawan is Founder of the International IEEE-NEWCAS Conference and of the Polystim Neurotechnologies Laboratory, and Co-Founder of the International IEEE-BioCAS Conference, and the International IEEE-ICECS. He received the Barbara Turnbull 2003 Award for spinal cord research, the Medal of Merit from the President of Lebanon, the Bombardier Medal of Merit, and the American University of Science and Technology Medal of Merit. He is Fellow of the Canadian Academy of Engineering, and Fellow of the Engineering Institutes of Canada. He is also Officer of the National Order of Quebec.

Yvon Savaria (S'77–M'86–SM'97–F'08) received the B.Ing. and M.Sc.A. degrees in electrical engineering from École Polytechnique de Montréal, Montréal, QC, Canada, in 1980 and 1982, respectively, and the Ph.D. degree in electrical engineering from McGill University, Montréal, QC, Canada, in 1985.

Since 1985, he has been with École Polytechnique de Montréal, where he is currently Professor and Chairman of the Department of Electrical Engineering. He has carried work in several areas in microelectronic circuits and microsystems, such as testing, verification, clocking methods, defect and fault tolerance, high-speed interconnects and circuit design techniques, computer-aided-design methods, reconfigurable computing and applications of microelectronics to telecommunications, aerospace, image and video processing, radar signal processing, and digital signal processing acceleration. He is currently involved in several projects that relate to green IT, such as wireless sensor networks, virtual networks, computational efficiency, and application-specific architecture design. He holds 15 patents, has published many journal and conference papers, and was the thesis advisor of 134 graduate students who completed their studies.

Dr. Savaria was the Program Co-Chairman of the 1992 edition and the Chairman of the 1993 edition of the IEEE Workshop on Defect and Fault Tolerance in VLSI systems. He was Program Co-Chairman of ASAP2006 and the

General Co-Chair of ASAP2007. He has been a Consultant or was sponsored for carrying research by Bombardier, CNRC, Design Workshop, Dolphin, DREO, Genesis, Gennum, Hyperchip, LTRIM, Miranda, MiroTech, Nortel, Octasic, PMC-Sierra, Technocap, Thales, Tundra, and VXP. He is a member of the Regroupement Stratégique en Microélectronique du Québec, of the Ordre des Ingénieurs du Québec, and is the Chairman of the board of CMC Microsystems. In 2001, he was awarded a Canada Research Chair (www.chairs.gc.ca) for the design and architectures of advanced microelectronic systems. In 2006, he received a Synergy Award from the Natural Sciences and Engineering Research Council of Canada.