0.35µm CMOS C35 Matching Parameters

Document Number: ENG - 228

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Company Confidential

Table of Contents

1 Introduction

1.1 Revision

Change Status of Pages (including short description of change)

Rev. 1.0	Affected pages:	1 to 32	(February 2003)
Subject of change: first version of mismatch parameter specification			
Rev. 2.0	Affected pages:	1 to 30	(April 2006)
Changed: Related Documents: update Update of all matching parameters Added: Process Family: new processes LVT-MOS transistors Chapter: Drain Current Mismatch Monitoring Pelgrom plots for VTH, KP, ID Chapter: Bipolar Transistor Matching Parameters VERT10 matching parameters CMIM matching parameter			
Rev. 3.0	Affected pages:	3,4,8,9,27,29	(May 2008)
Changed: Process Family: refer to PPD Changed: Related Documents: update Changed: VERT10 matching parameters Added: RPOLYZ resistor matching parameter			

1.2 Process Family

See document 0.35 µm C35 CMOS Process Parameters ENG – 182.

1.3 Related Documents

Description	Document Number
0.35µm CMOS C35 Process Parameters	ENG – 182
0.35µm CMOS C35 Design Rules	ENG – 183
0.35µm CMOS C35 Noise Parameters	ENG – 189
0.35µm CMOS C35 RF SPICE Models	ENG – 188
C35 ESD Design Rules	ENG – 236
Standard Family Cells	ENG – 42
Assembly Related Design Rules	ASSY – 15

1.4 Process parameter description

PASS/FAIL PARAMETERS and INFORMATION PARAMETERS are monitored and statistically controlled for each wafer. The wafer must meet the specification of the PASS/FAIL parameters, whereas INFORMATION parameters are intended to get additional information about the process.

CHARACTERISATION PARAMETERS are provided to increase the knowledge about the process behaviour. They are not under 100% statistical control because they require extra large test structures (e.g. parasitic capacitors) or time consuming measurement procedures (e.g. temperature coefficients). These data are extracted from special process control monitor (PCM) test structures and do not lead to wafer reject in case of failure.

Note: Characterisation parameters are extracted from typical wafers only, therefore no corner models are available. It is strongly recommended that a design shall rely only on pass/fail parameters.

2 Matching Parameters

2.1 Introduction

This document presents fundamental parameters describing the matching behaviour of MOS transistors, resistors and capacitors. All matching parameters are characterisation parameters and represent typical values only.

The matching parameters describe the short distance matching - the matching of two identically designed elements located close to each other.
The stochastic mismatch between two parameters P1 and P2 measured at two identically designed elements is defined as the standard deviation of the normal distribution for

1. absolute differences $\Delta P = (P1 - P2)$ [mV]
(for threshold voltages)

or

2. relative differences $\frac{\Delta P}{P} = \frac{200 \cdot (P1 - P2)}{(P1 + P2)}$ [%]
(for transistor currents, resistors, capacities).

We assume that all ΔPi values are normally distributed with a variance σ^2 (squared standard deviation). The estimator μ of the distribution mean is close to zero – indicating a low fraction of systematic mismatch - except in the case of strong process parameter gradients or layout related asymmetries.

2.1.1 Model used for evaluation of measured data

Matching measurements are performed for MOS transistors, resistors and capacitors. The following Pelgrom model describes the dependency of parameter matching on two identically designed devices on their area (W·L):

$$\sigma(P1 - P2) = \frac{A\_P}{\sqrt{W \cdot L}}$$

where A_P is the process-dependent matching parameter describing the area dependence.

2.1.2 Model used for matching simulation

Additionally, final matching parameters are extracted for MOS transistors. These parameters are used for simulator model implementation and Monte Carlo simulation.

2.2 MOS Transistor Matching Parameters

2.2.1 Matching Parameter Extraction / Simulator Implementation

Matching parameters are determined by fitting a suitable mismatch model to the measured data σ(ΔID/ID) of each device size. The variances of the relative matching deviations are fitted by a non-linear optimisation procedure. The resulting parameters give an optimal fitting result for the whole measured biasing region (see section Characteristic Curves).
A linear regression is applied to the fitting parameters to calculate the area dependence A_P of the matching parameters.

$$\sigma(\Delta P) = \frac{A\_P}{\sqrt{W \cdot L}}$$

The simulator model implementation for the Monte Carlo simulation includes the parameter A_P_{sim}. The implementation is done by using extended sub-circuit device models. Since the simulation model describes the variation of a single device parameter, the value $A\_P_{sim} = A\_P/\sqrt{2}$ is used assuming statistically independent parameters.

Final matching parameters are extracted for

VT	threshold voltage
K	current gain factor

CHARACTERISATION PARAMETERS		
Parameter	A_VT	A_K
Unit	mV µm	% µm
NMOS	9.5	0.7
PMOS	14.5	1.0
NMOSM	14.5	0.5
PMOSM	21.0	1.0
NMOSL	9.5	0.7
PMOSL	17.5	0.8
NMOSML	13.5	0.5
PMOSML	25.0	0.9
Note	1	1

2.2.2 Drain Current Mismatch Monitoring

Structures for monitoring the drain current mismatch of NMOS and PMOS devices are implemented on each wafer. Two matched pairs including transistors of size W/L=10/0.35 and W/L=0.4/0.35 are measured in saturation and the relative differences of the drain currents are determined, which are the basis for statistical analysis.

Statistical results of the drain current mismatch monitoring:

$\sigma(\Delta ID/ID)$ variance of relative drain current mismatch
$4\sigma(\Delta ID/ID)$ 4 σ limits of the relative drain current mismatch for CPK=1.33.

INFORMATION PARAMETERS		
Parameter	$\sigma(\Delta ID/ID)$	$4\sigma(\Delta ID/ID)$
Unit	%	%
NMOS, W/L = 10/0.35	0.54	2.16
PMOS, W/L = 10/0.35	0.92	2.88
NMOS, W/L = 2.5/0.35	0.94	2.96
PMOS, W/L = 2.5/0.35	1.62	6.48
Note	2	2

2.3 Bipolar Transistor Matching Parameters

2.3.1 Matching Parameter Extraction / Simulator Implementation

Matching parameters are determined by fitting a suitable mismatch model to the measured relative base current mismatch $\sigma(\Delta IB/IB)$ and relative collector current mismatch $\sigma(\Delta IC/IC)$. An appropriate variance model is fitted to extract the bipolar parameter variances for BF (forward current gain) and IS (saturation current) from the measured data. The extraction procedure of the relative matching deviations uses non-linear optimisation. The resulting parameters give an optimum fitting result over the whole biasing region.

The simulator model implementation for the Monte Carlo simulation includes the parameter A_P_{sim}. The implementation is done by using extended sub-circuit device models. Since the simulation model describes the variation of a single device parameter, the value $A\_P_{sim} = A\_P/\sqrt{2}$ is used assuming statistically independent SPICE parameters.

Final matching coefficients are extracted for the following bipolar parameters:

BF	forward current gain
IS	saturation current
ISE	nonlinear saturation current

CHARACTERISATION PARAMETERS			
Parameter	A_BF	A_IS	A_ISE
Unit	%	%	%
VERT10	0.42	0.14	13.4
Note	3	3	

Note: The VERT10 has a fixed size.

2.4 Resistor Matching Parameters

The resistor matching is described by

$$\sigma\left(\frac{\Delta R}{R}\right) = \frac{A\_R}{\sqrt{W \cdot L}}$$

CHARACTERISATION PARAMETERS	
Parameter	A_R
Unit	% µm
RPOLY2	9.5
RPOLYH	6.5
RPOLYZ	5.8
Note	4

2.5 Capacitor Matching Parameters

The capacitor matching is described by

$$\sigma\left(\frac{\Delta C}{C}\right) = \frac{A\_C}{\sqrt{W \cdot L}}$$

CHARACTERISATION PARAMETERS	
Parameter	A_C
Unit	% µm
CPOLY	0.45
CMIM	1.0
Note	5

3 Notes / Measurement Conditions

Note 1 Drain-current matching

The measurements of ID are performed at
VDS=3V and VGS=0.5 - 3.5V for N/PMOS(L)
VDS=5V and VGS=0.5 - 5.5V for N/PMOSM(L)

Note 2 Process monitoring of drain-current matching

The measurements of ID are performed at
VDS=3V and VGS=2.2V for N/PMOS

Note 3 Collector-, base-current matching

VERT10: IE and IB are measured at VBC= 0 and VBE= -0.4 to –0.9V

Note 4 Resistor matching

The resistance measurements are performed at constant power (1mW) for different resistor dimensions (W, L).

Note 5 Capacitor matching

Due to the very low capacitances a direct measurement and calculation of mismatch parameters are not possible. Therefore a floating gate measurement technique with a source follower on the (floating) middle node of a capacitive voltage divider is used. By applying different input voltages (0.5V to 4.5V) and measuring the corresponding output voltages at the source of the p-channel transistor a slope S_1 is determined. After exchanging the nodes of the voltage divider a second slope S_2 is measured. The resulting capacitor mismatch is defined by

$$\frac{\Delta C}{C} = 2 \cdot \frac{S1 - S2}{S1 + S2} = 2 \cdot \frac{C1 - C2}{C1 + C2}$$

4 Characteristic Curves

The plotted mismatch model corresponds to the individual extracted parameters $\sigma(\Delta VTH)$ and $\sigma(\Delta KP / KP)$ for each device size. These parameters are used in the plots showing mismatch vs. device area (Pelgrom's relation).

4.1 NMOS Characteristic Matching Curves

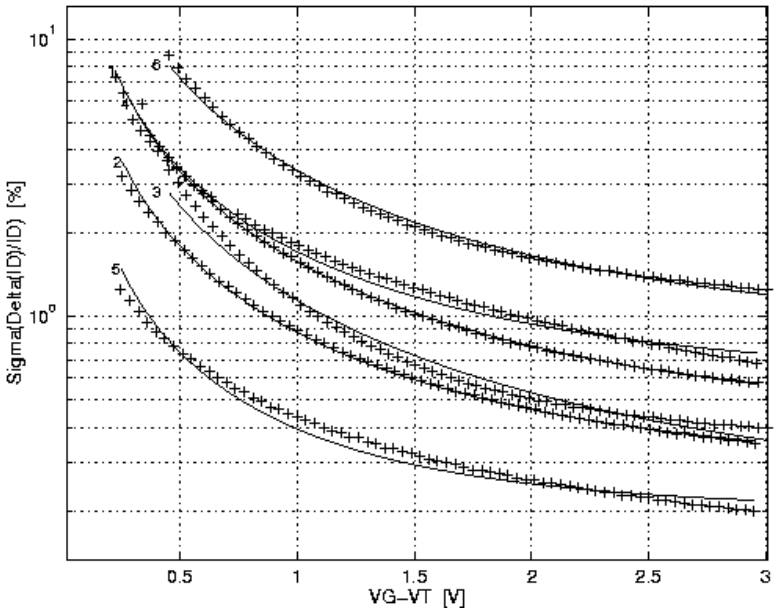

Fig. 4.1 NMOS relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

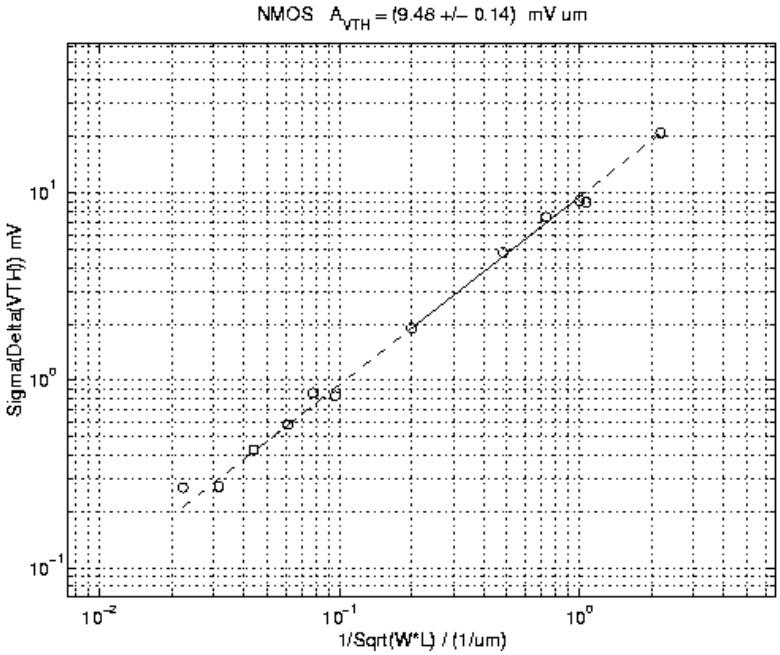

Fig. 4.2 NMOS threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

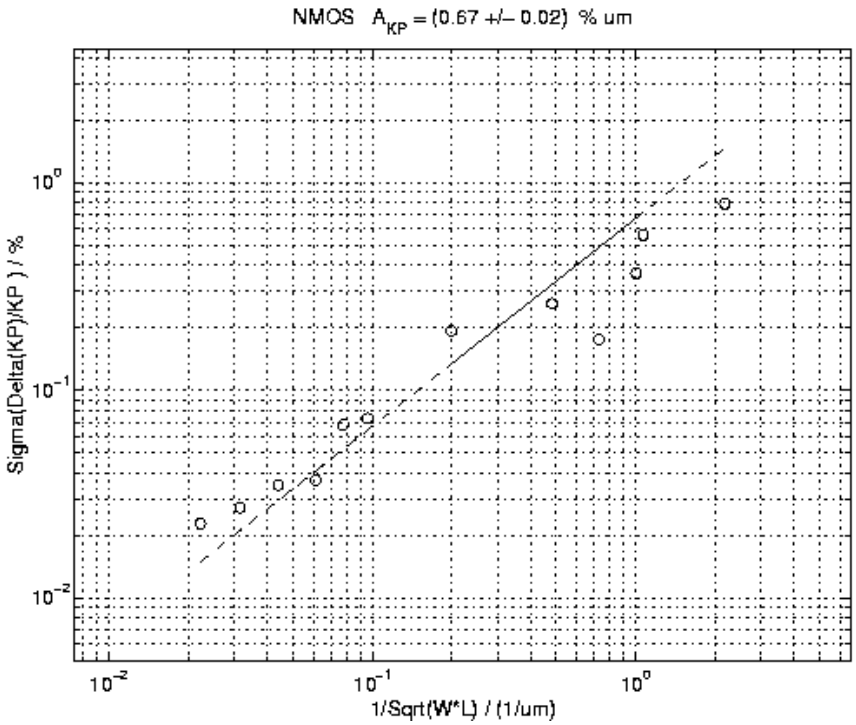

Fig. 4.3 NMOS current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

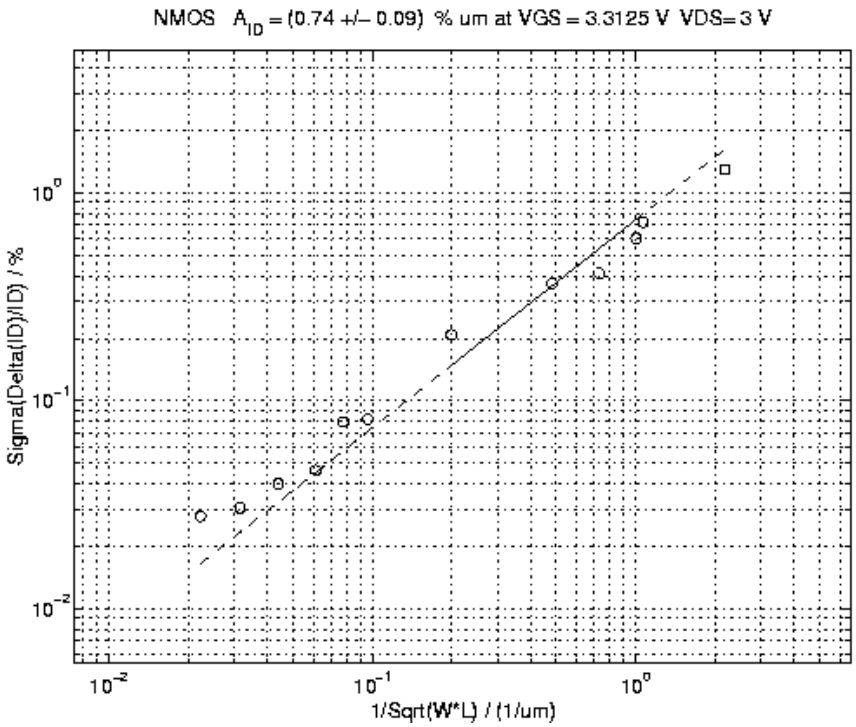

Fig. 4.4 NMOS drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.2 PMOS Characteristic Matching Curves

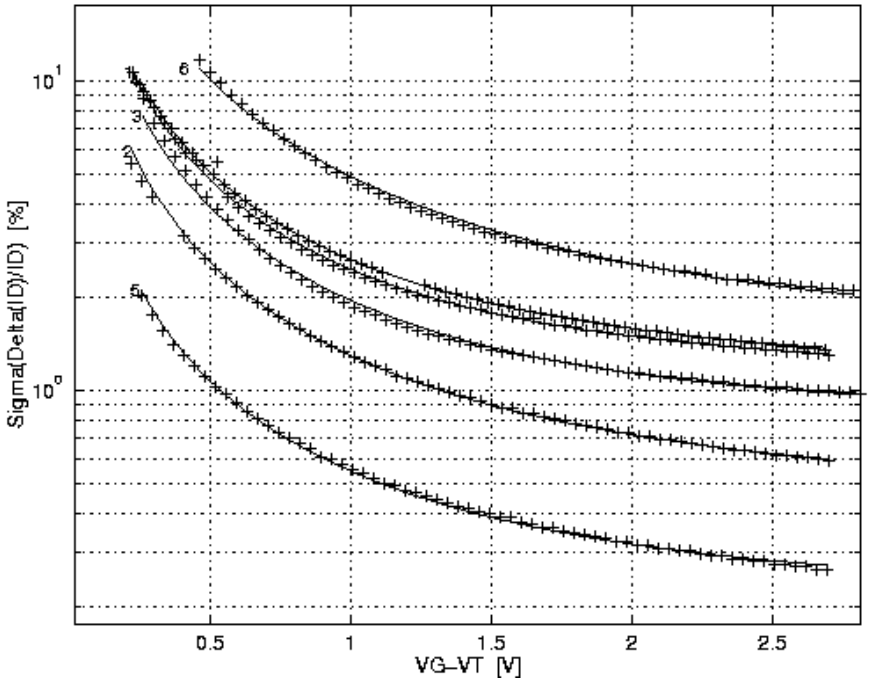

Fig. 4.5 PMOS relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

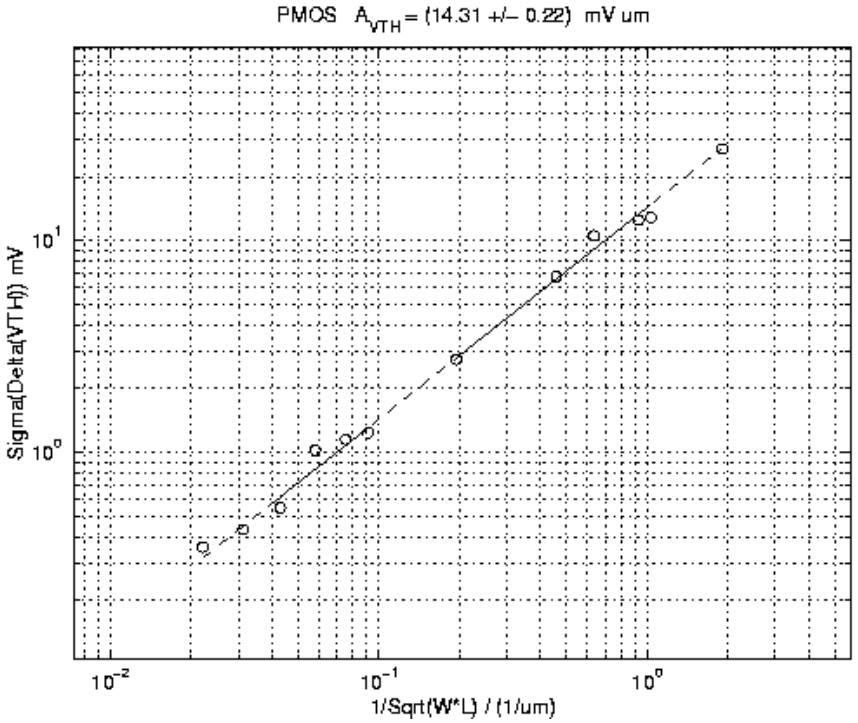

Fig. 4.6 PMOS threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

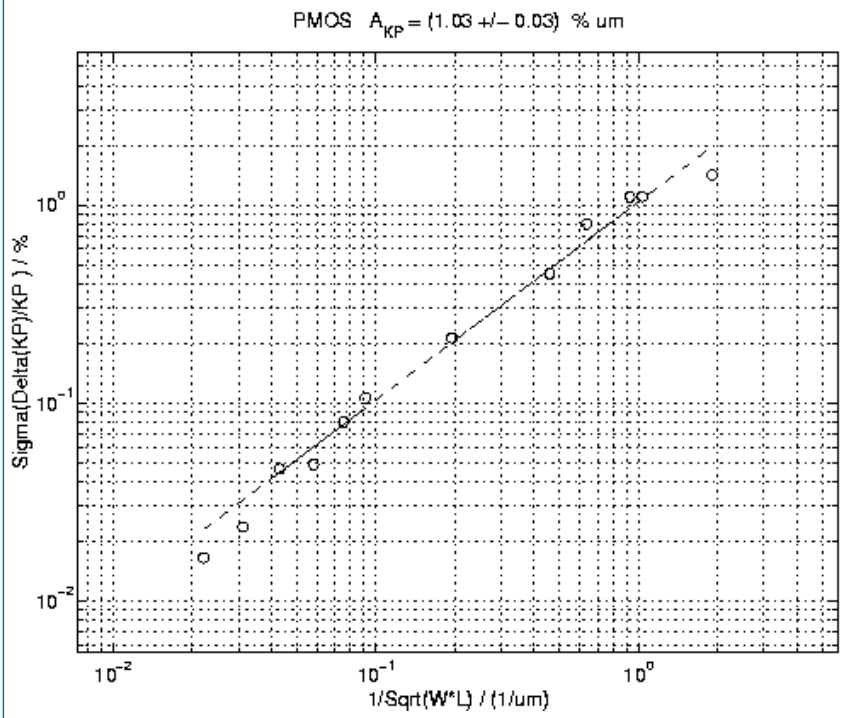

Fig. 4.7 PMOS current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

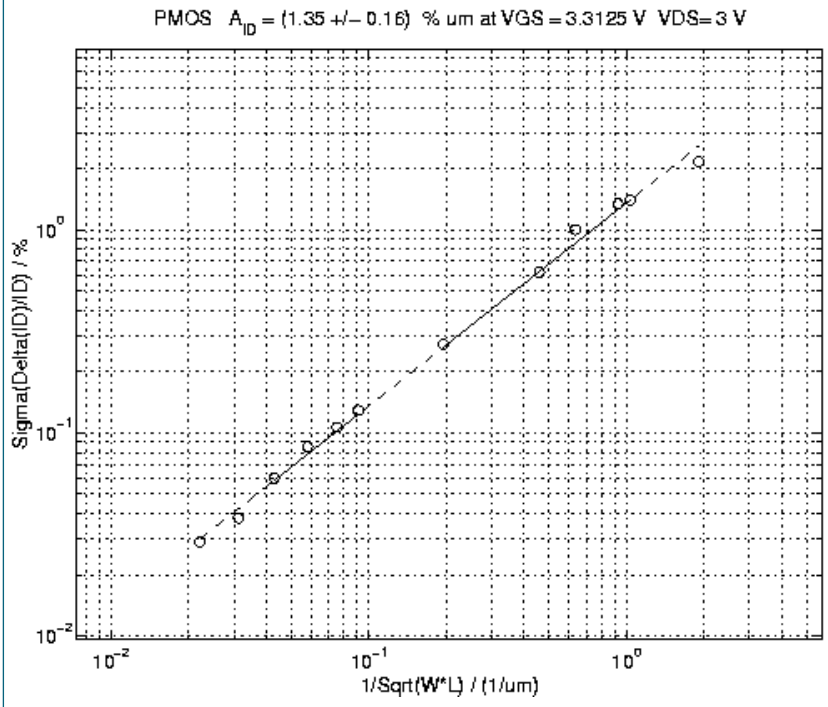

Fig. 4.8 PMOS drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.3 NMOSM Characteristic Matching Curves

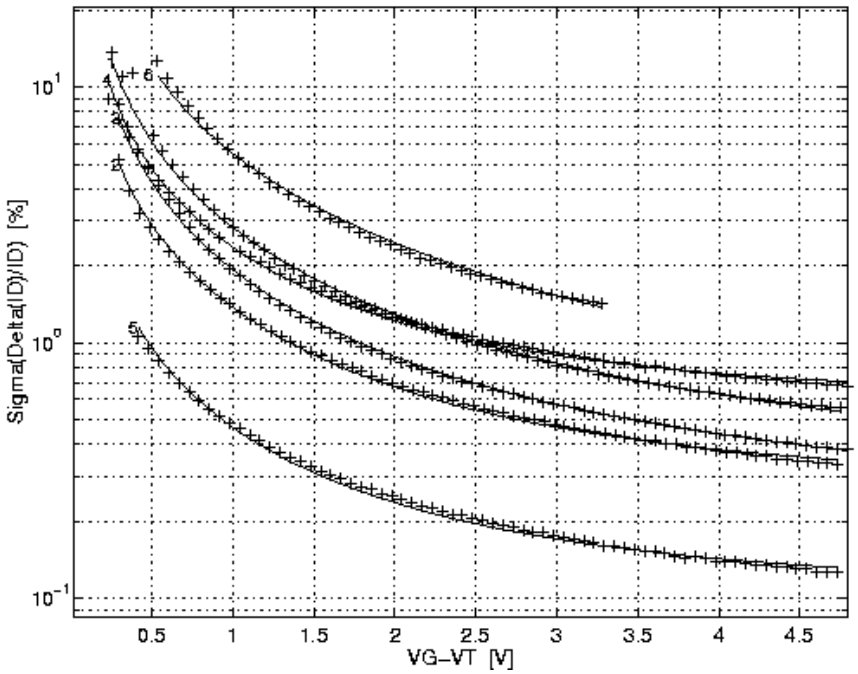

Fig. 4.9 NMOSM relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

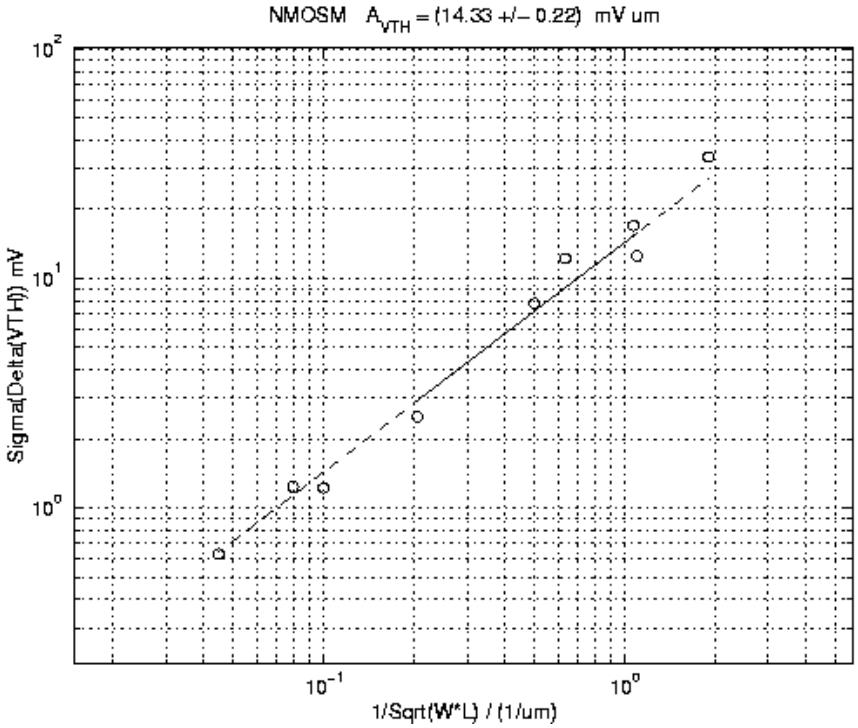

Fig. 4.10 NMOSM threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

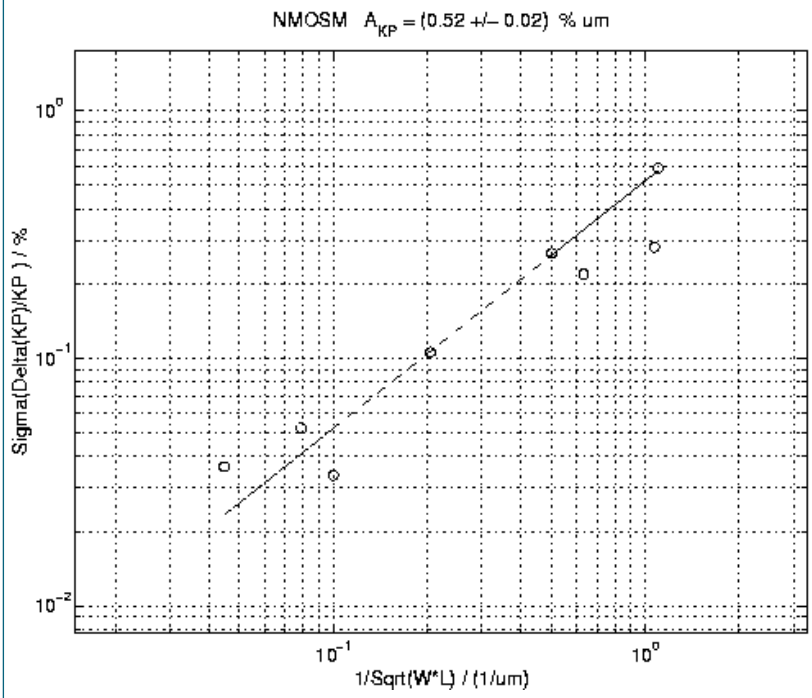

Fig. 4.11 NMOSM current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

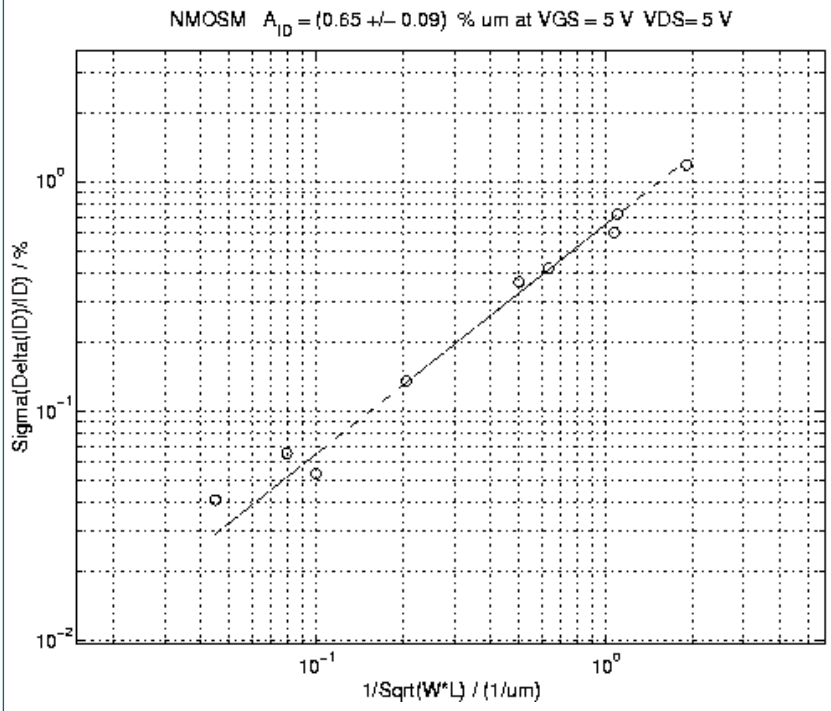

Fig. 4.12 NMOSM drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.4 PMOSM Characteristic Matching Curves

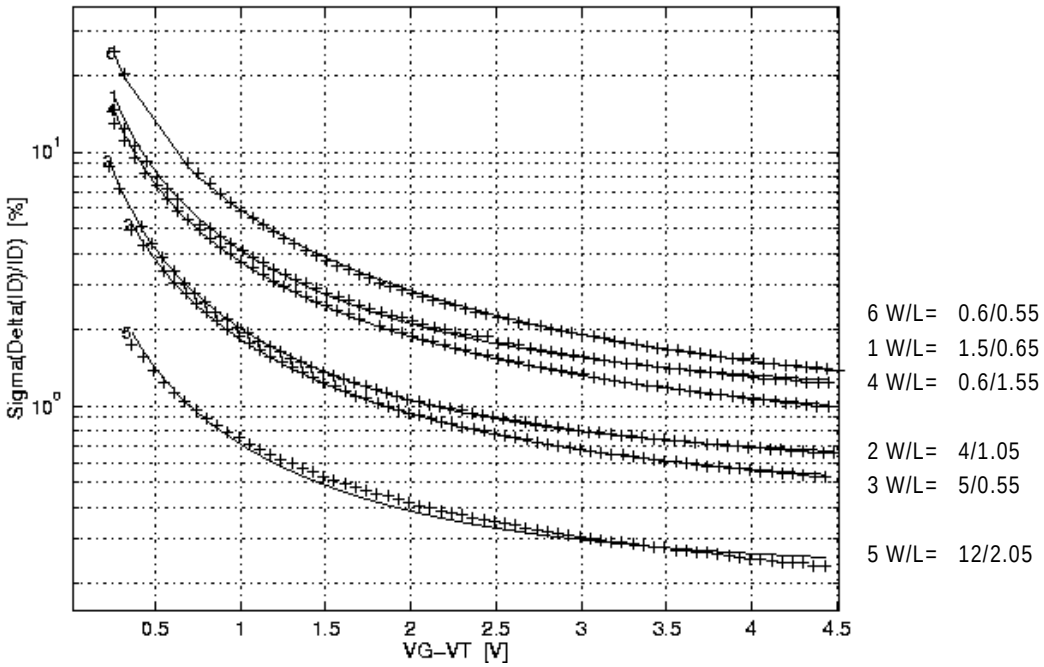

Fig. 4.13 PMOSM relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

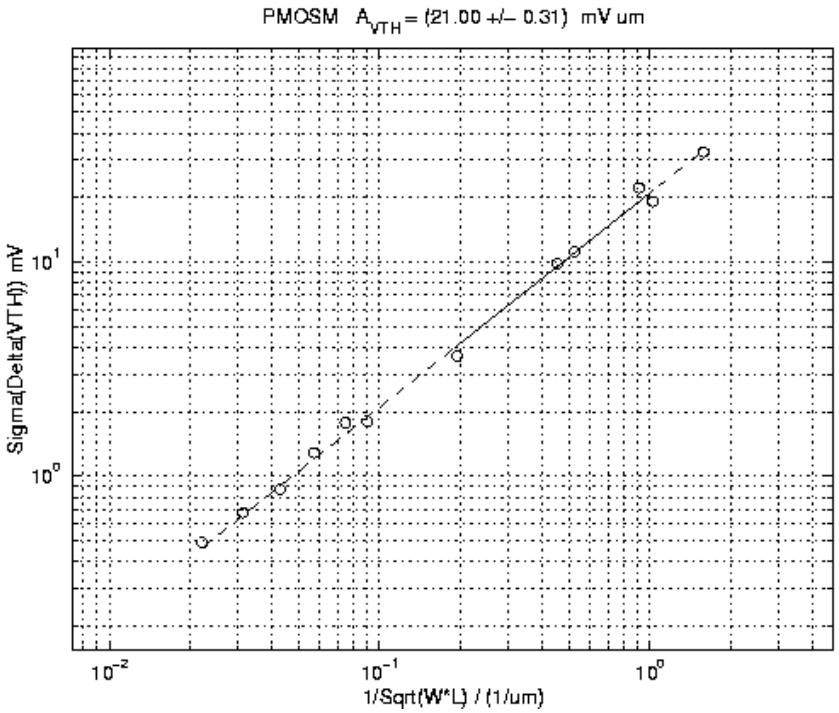

Fig. 4.14 PMOSM threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

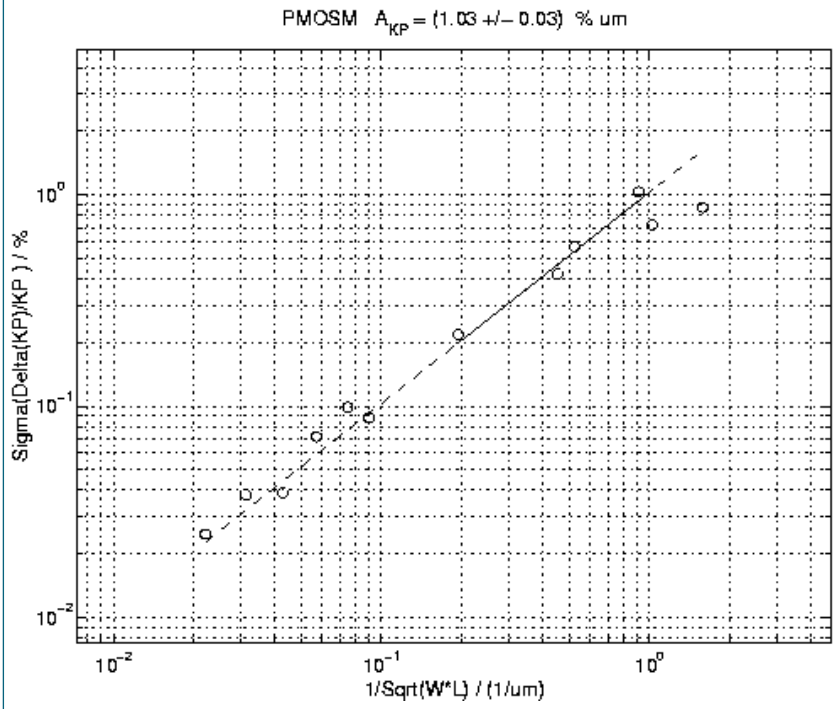

Fig. 4.15 PMOSM current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

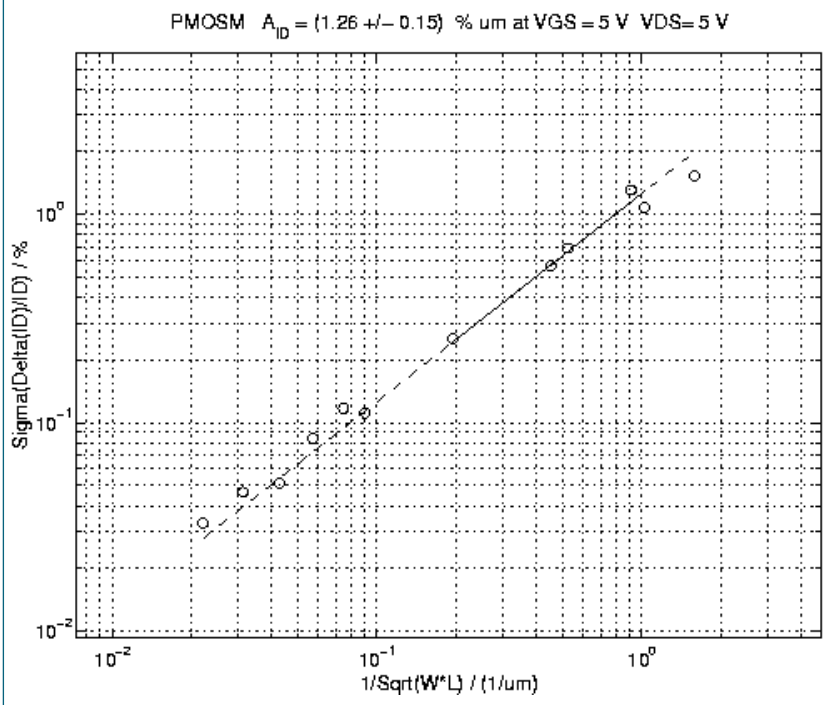

Fig. 4.16 PMOSM drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.5 NMOSL Characteristic Matching Curves

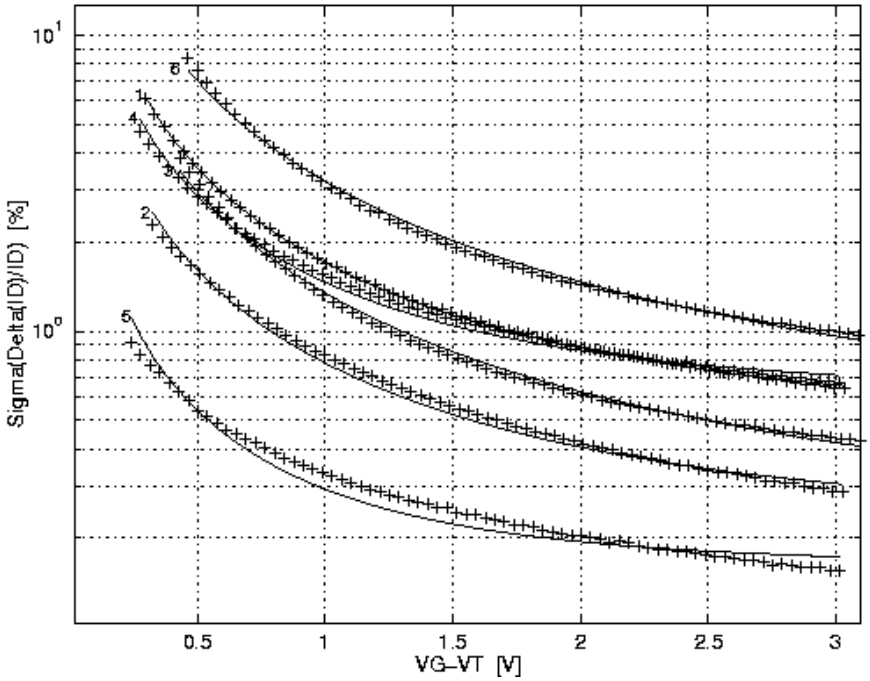

Fig. 4.17 NMOSL relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

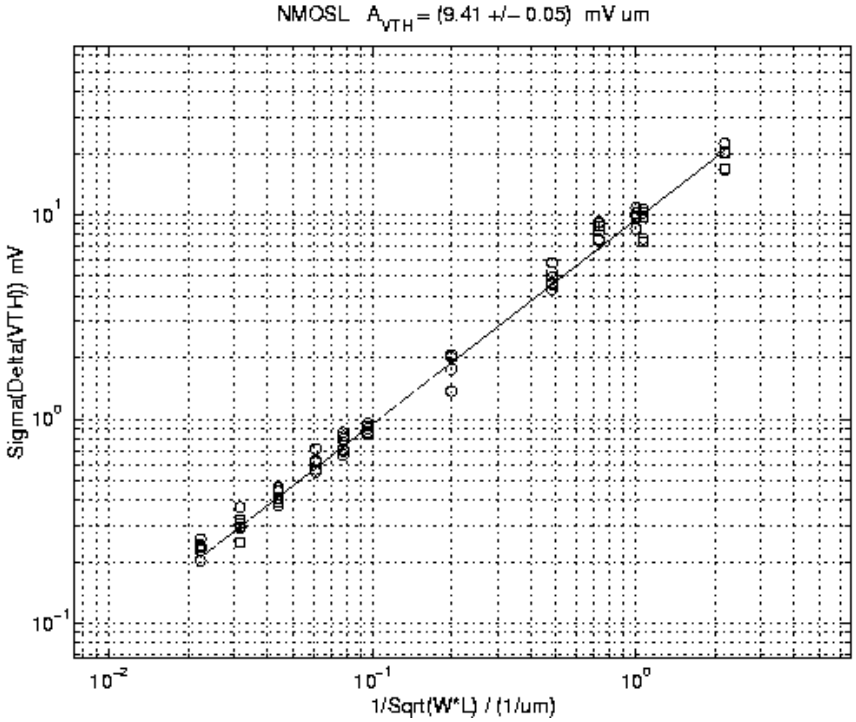

Fig. 4.18 NMOSL threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

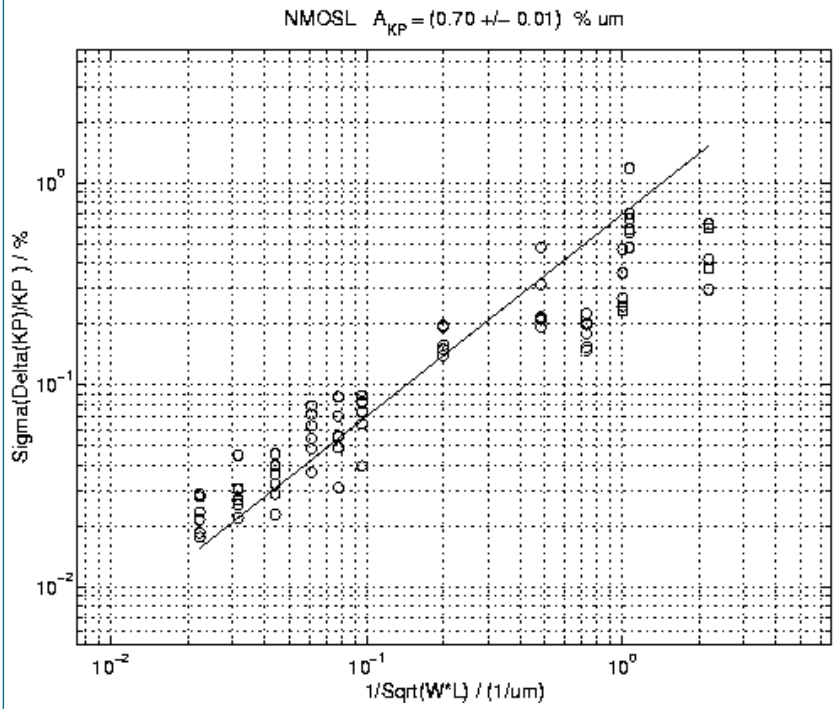

Fig. 4.19 NMOSL current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

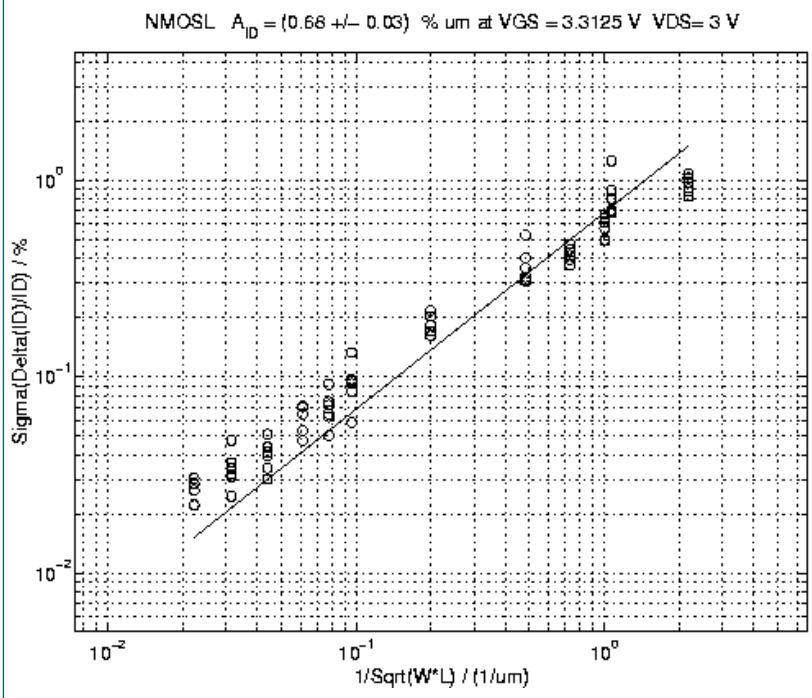

Fig. 4.20 NMOSL drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.6 PMOSL Characteristic Matching Curves

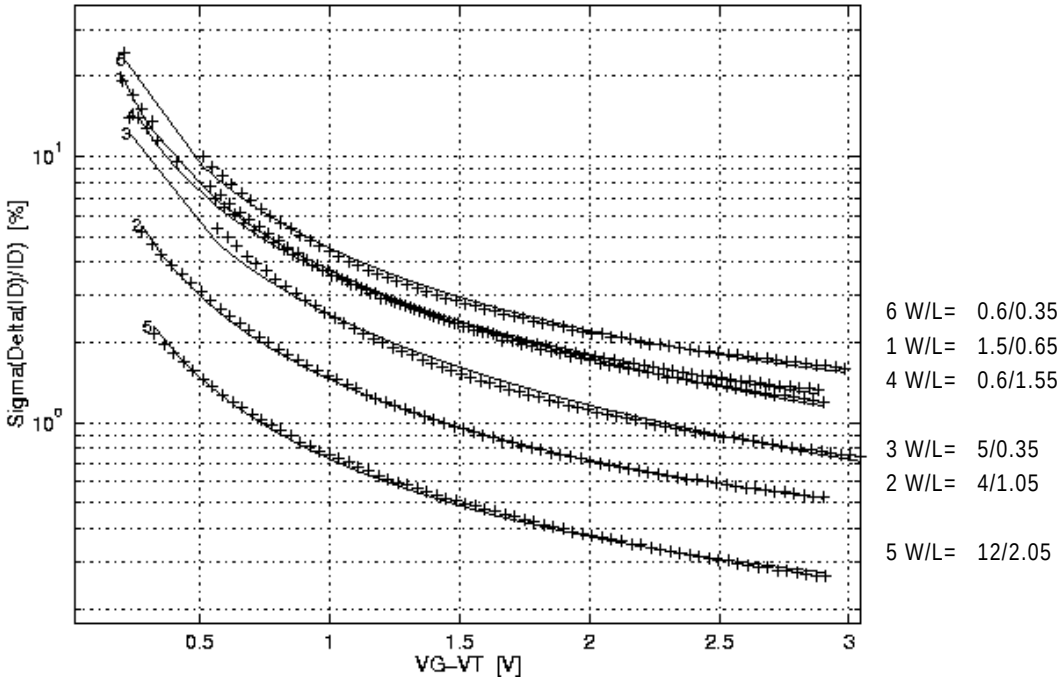

Fig. 4.21 PMOSL relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

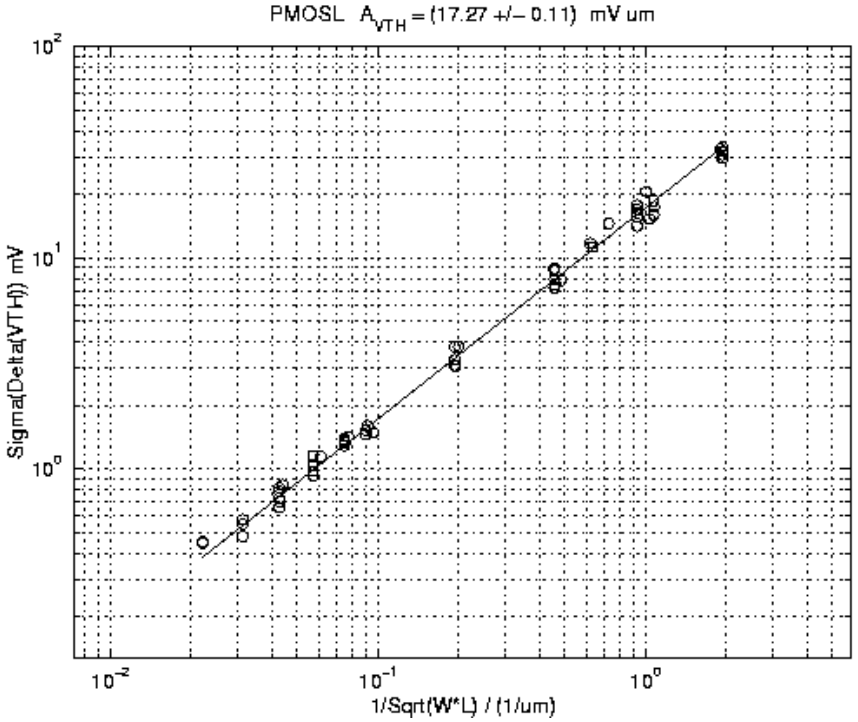

Fig. 4.22 PMOSL threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

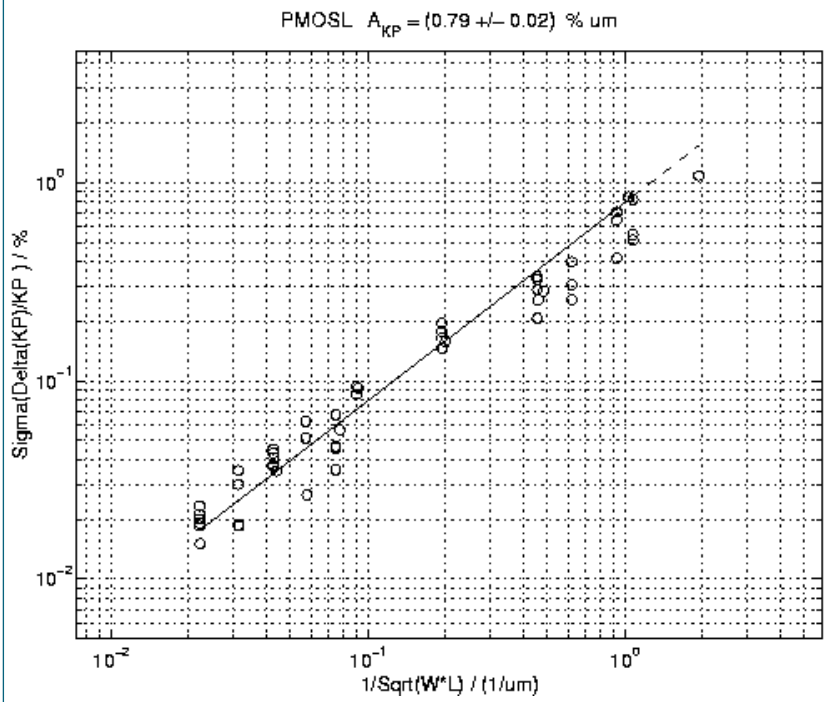

Fig. 4.23 PMOSL current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

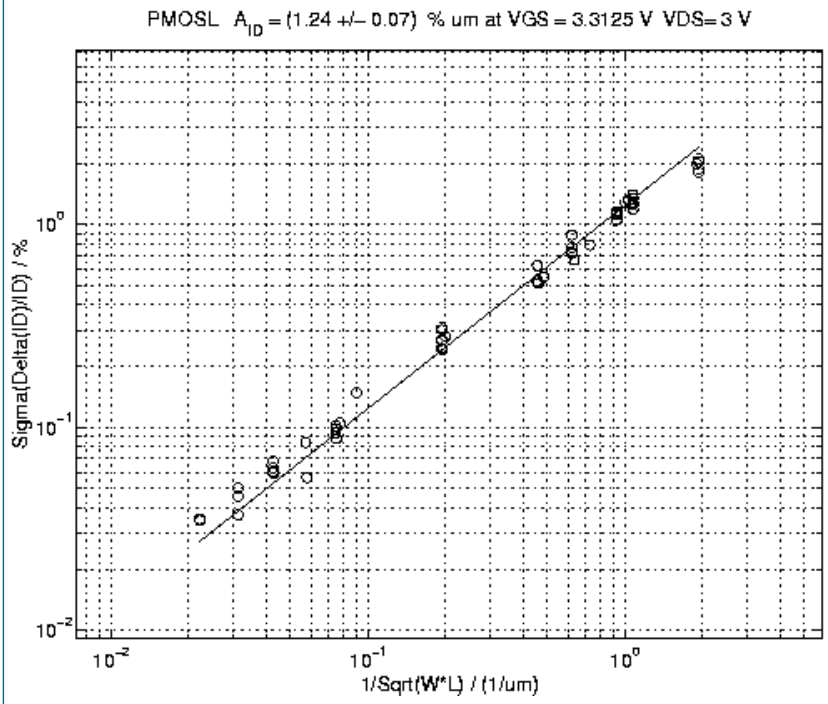

Fig. 4.24 PMOSL drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.7 NMOSML Characteristic Matching Curves

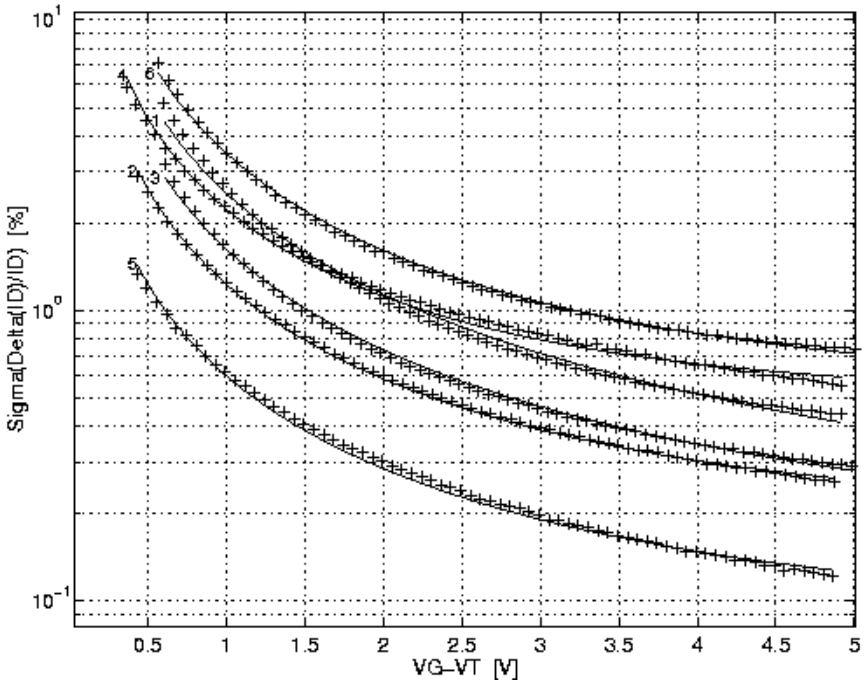

Fig. 4.25 NMOSML relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

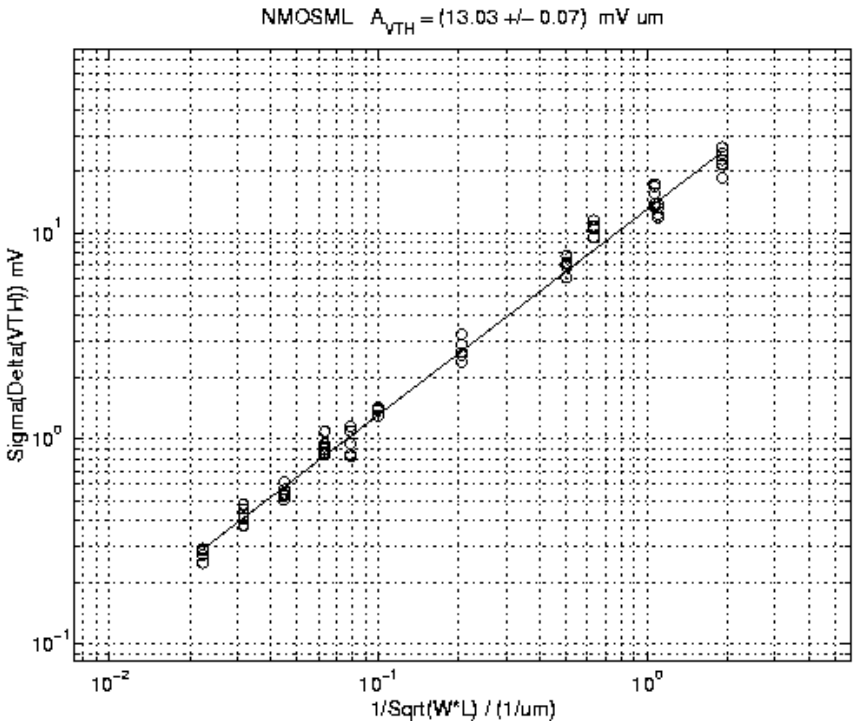

Fig. 4.26 NMOSML threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

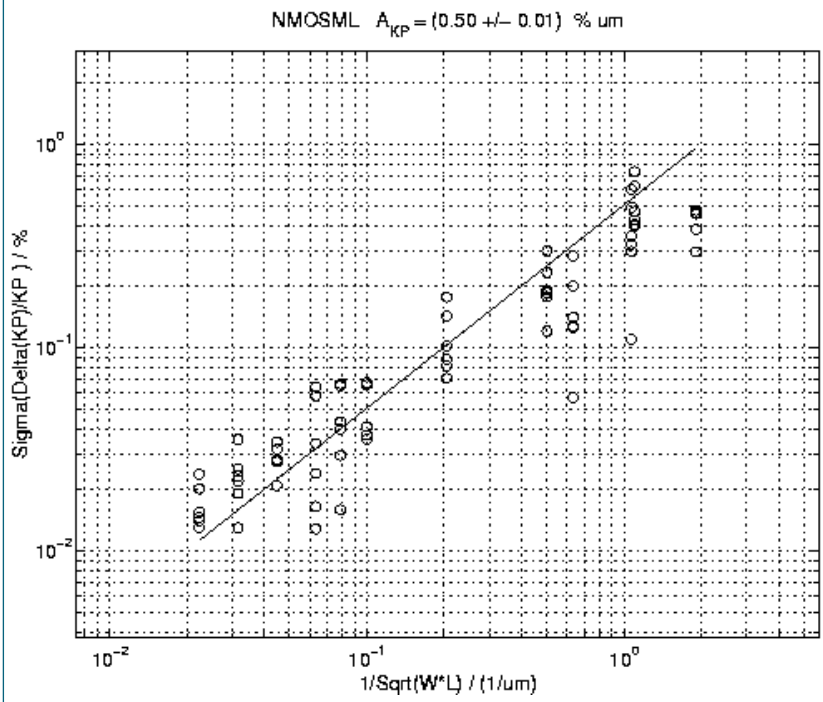

Fig. 4.27 NMOSML current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

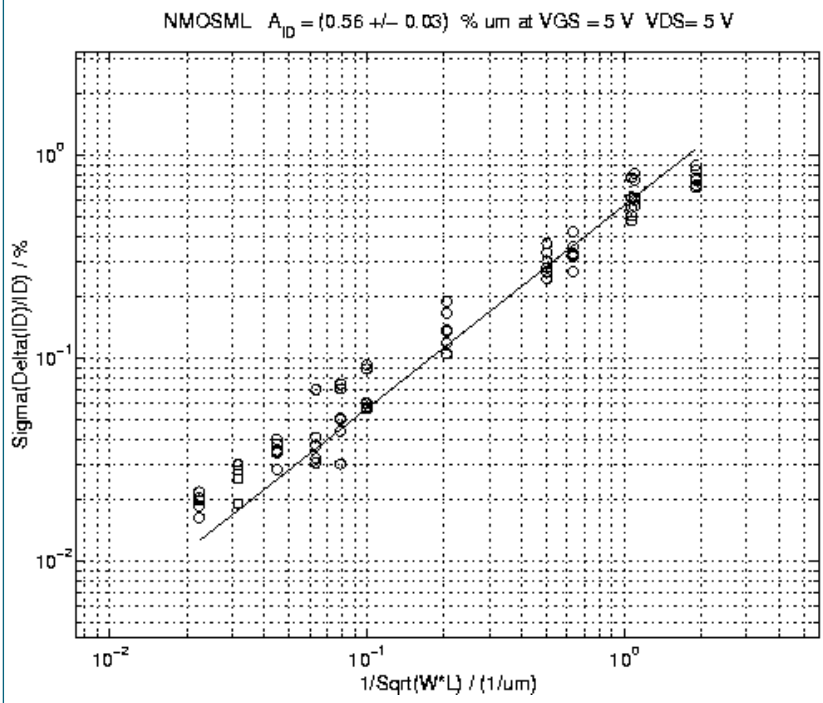

Fig. 4.28 NMOSML drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.8 PMOSML Characteristic Matching Curves

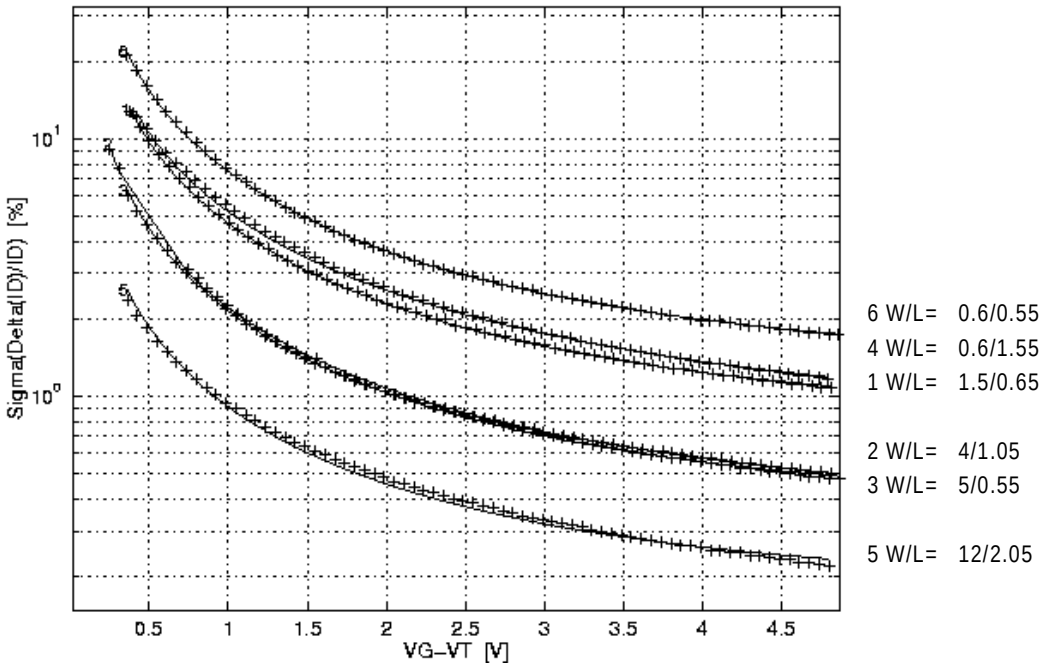

Fig. 4.29 PMOSML relative drain current mismatch vs. VG-VT, +...measurement, —...mismatch model

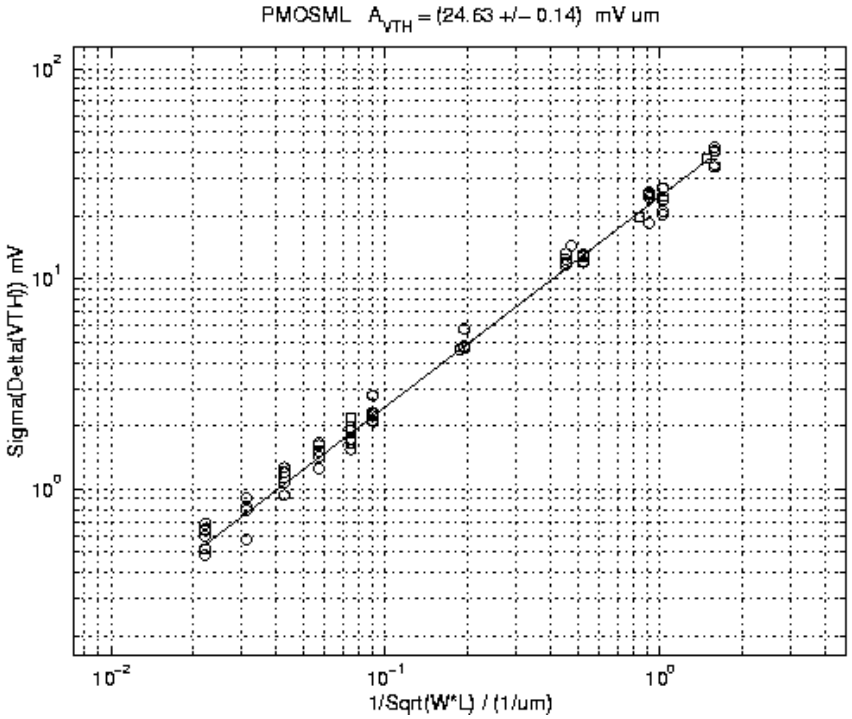

Fig. 4.30 PMOSML threshold voltage mismatch vs. device size $W.L$: $\sigma(\Delta VTH)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

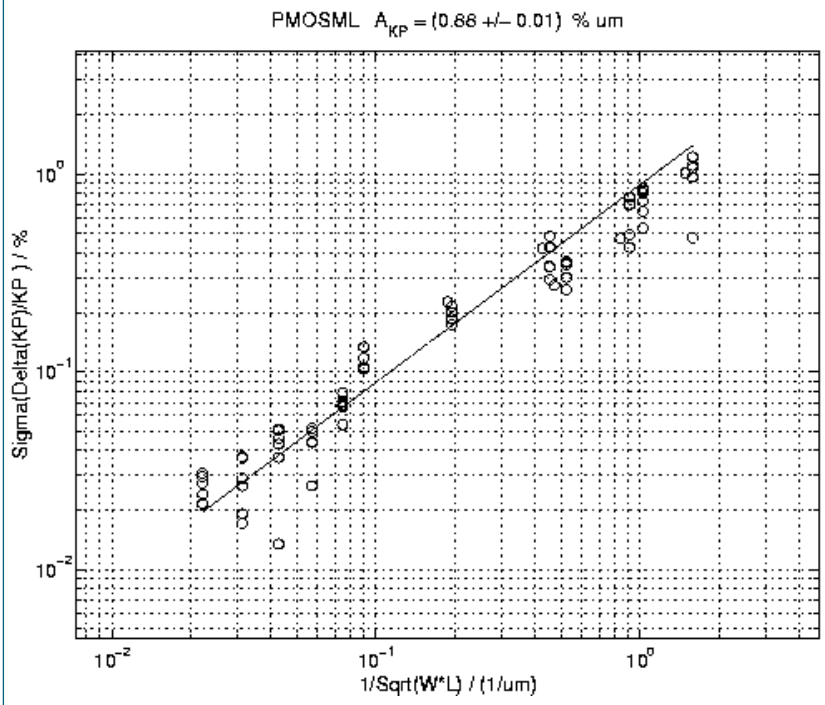

Fig. 4.31 PMOSML current gain factor mismatch vs. device size $W.L$: $\sigma(\Delta KP / KP)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

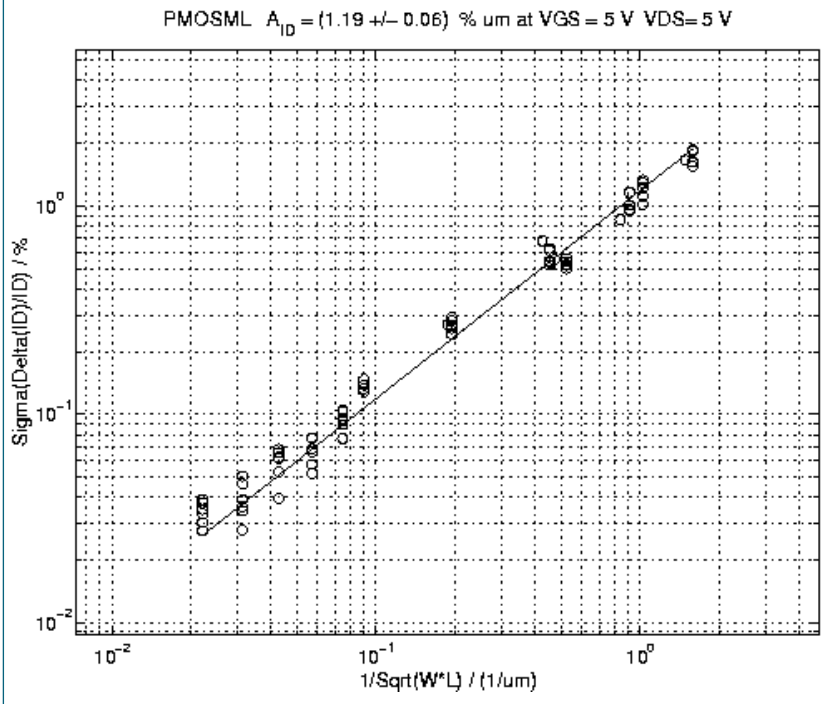

Fig. 4.32 PMOSML drain current mismatch vs. device size $W.L$: $\sigma(\Delta ID / ID)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

4.9 Bipolar Transistor Characteristic Matching Curves

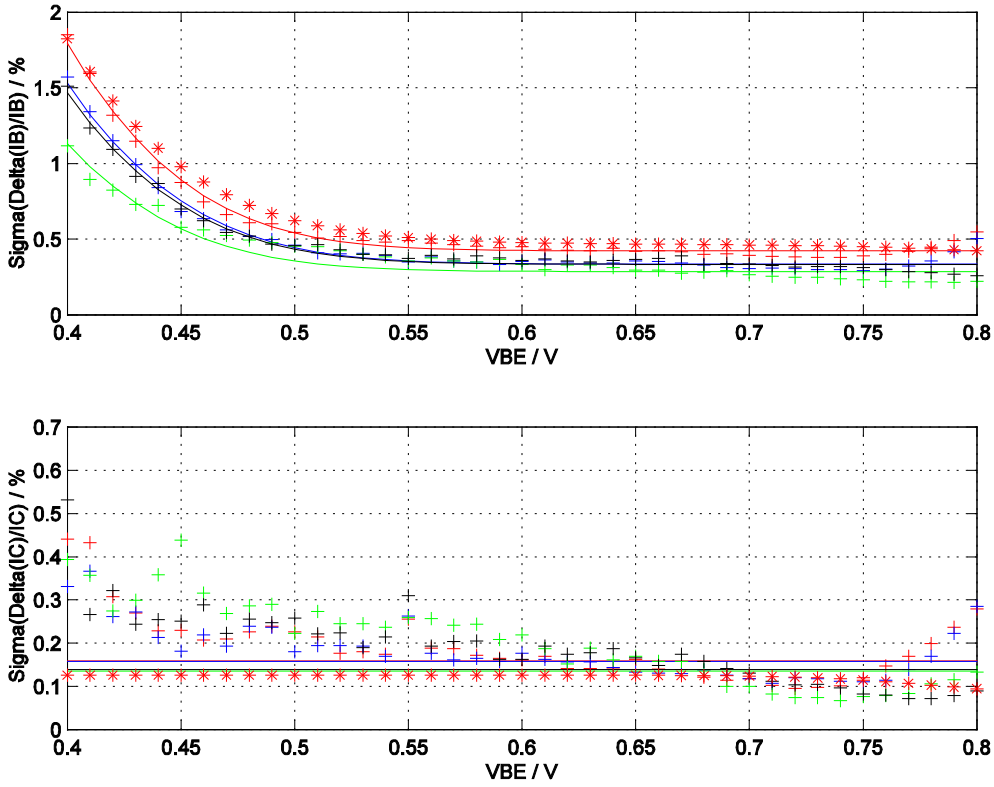

Fig. 4.33 Bipolar transistor VERT10, base current mismatch vs. base-emitter voltage VBE: $\sigma(\Delta IB / IB)$ vs. VBE (top) and collector current mismatch vs. base-emitter voltage VBE: $\sigma(\Delta IC / IC)$ vs. VBE (bottom)
+...measurement, -... extracted model, *... final implemented mismatch model

4.10 Resistor Characteristic Matching Curves

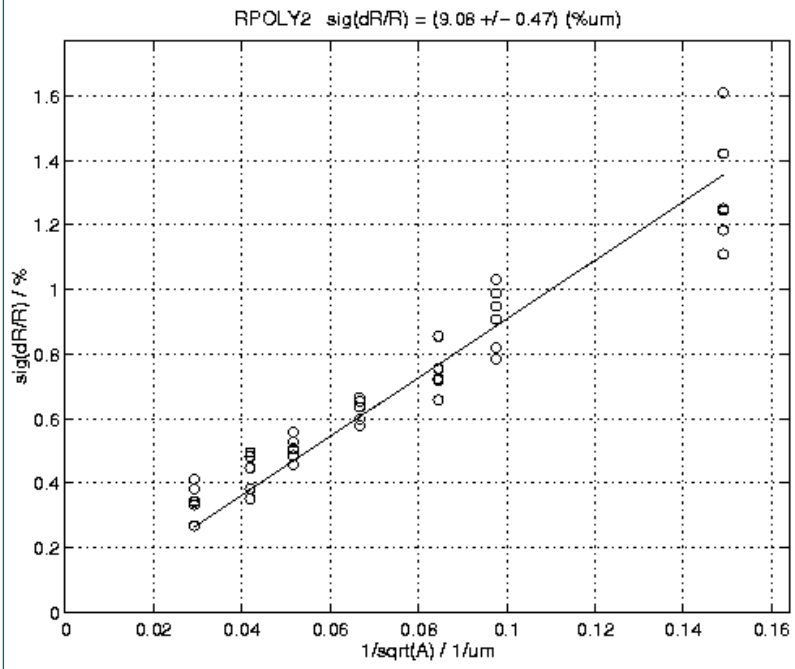

Fig. 4.34 Resistor RPOLY2, mismatch vs. resistor size $W.L$: $\sigma(\Delta R/R)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

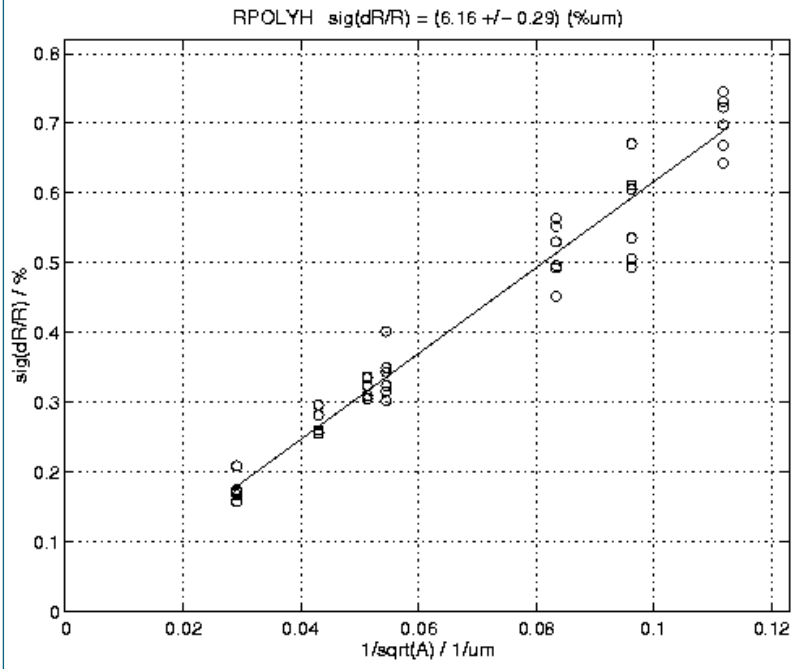

Fig. 4.35 Resistor RPOLYH, mismatch vs. resistor size $W.L$: $\sigma(\Delta R/R)$ vs. $1/\sqrt{W \cdot L}$:
o...measurement, ----...mismatch model

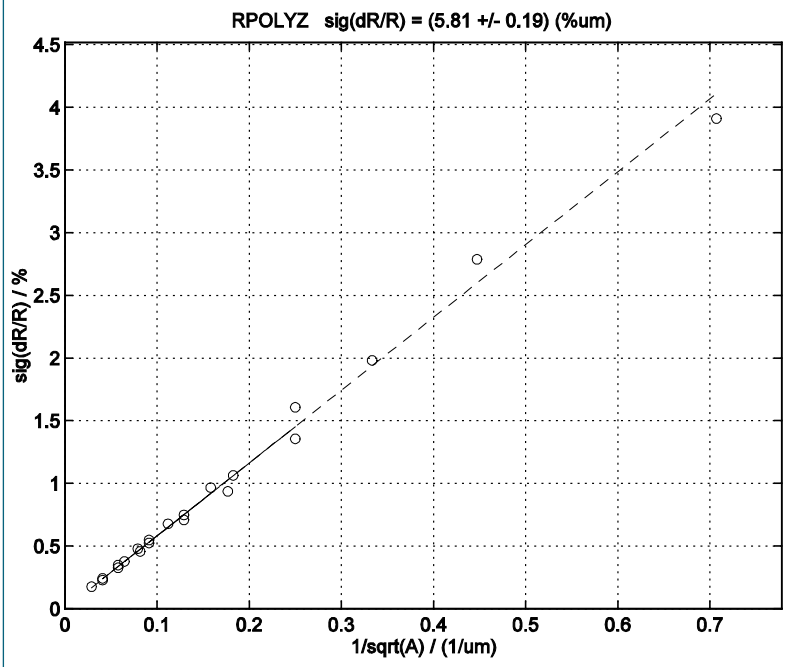

Fig. 4.36 Resistor RPOLYZ, mismatch vs. resistor size $W.L$: $\sigma(\Delta R / R)$ vs. $1/\sqrt{W \cdot L}$: o...measurement, ----...mismatch model

4.11 Capacitor Characteristic Matching Curves

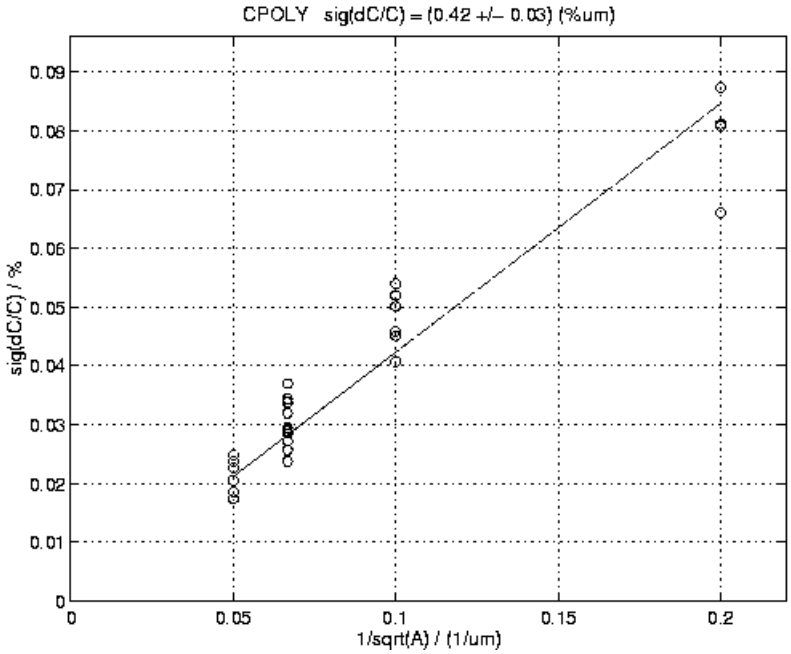

Fig. 4.37 Capacitor CPOLY, mismatch vs. capacitor area A: $\sigma(\Delta C / C)$ vs. $1/\sqrt{A}$: o...measurement, – ...mismatch model

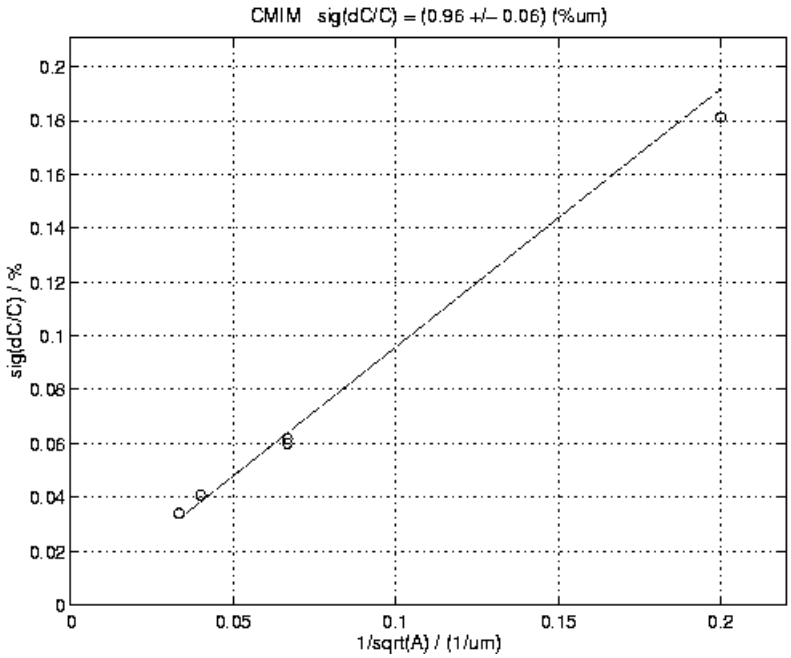

Fig. 4.38 Capacitor CMIM, mismatch vs. capacitor area A: $\sigma(\Delta C / C)$ vs. $1/\sqrt{A}$: o...measurement, – ...mismatch model

5 Circuit Simulators and Models

The models are supported and qualified for the specified simulator revision.

Simulator	MOS Model	Bipolar Model
	BSIM3v3	GUMMEL-POON
Spectre	5.1.41	5.1.41
Eldo	6.5.2	6.5.2

The following models are supported for mismatch simulation:

MOS transistor:	BSIM3v3
Bipolar transistor:	Gummel-Poon
Resistors:	R / JFET level 1
capacitors:	C / SUBCKT

Our technical web server http://asic.austriamicrosystems.com provides:

- Updates of model revisions (section “Simulation Parameters”)
- Updates of netlist formats (section “Netlist Formats”)
- Updates of simulation parameters (section “Download Area”)
- Mismatch models for Monte Carlo simulation as a part of the Cadence HIT-Kit. A tutorial on Monte Carlo simulation using Spectre/Cadence is provided in the “Statistical Circuit Simulation” section of the HIT-Kit link.

6 Support

For questions on process parameters please refer to:

austriamicrosystems AG

A 8141 Schloss Premstätten, Austria
T. +43 (0) 3136 500 0
F. +43 (0) 3136 525 01

E-mail: tips@austriamicrosystems.com
Technical Webserver: http://asic.austriamicrosystems.com
Homepage: http://www.austriamicrosystems.com

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