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Analysis, design, and implementation of a high-efficiency full-wave rectifier in standard CMOS technology

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Abstract In this paper we present analysis, design, and implementation of a high-efficiency active full-wave rectifier in standard CMOS technology. The rectifier takes advantage of the dynamic voltage control of its separated n-well regions, where the main rectifying PMOS elements have been implemented in order to eliminate latch-up and body effect. To minimize rectifier dropout and improve AC–DC power conversion efficiency (PCE), all the MOSFET switching elements have been pushed into deep triode region to minimize their resistance along the main current path during conduction. A prototype rectifier was implemented in the AMI 0.5-μm 3M/2P n-well CMOS process. An input sinusoid of 5 V peak at 0.5 MHz produced 4.36 V DC output across a 1 kΩ||1 μF load, resulting in a measured PCE of 84.8%.

Keywords CMOS · Inductive power transmission · Power conversion efficiency · Rectifier · Telemetry · Implantable devices · Wireless sensors · System-on-a-chip

1 Introduction

Wireless transmission of power in applications where batteries cannot be used due to size, lifetime, or cost constraints usually takes place by inducing an AC power carrier signal through a pair of tuned inductively-coupled coils that constitute a transformer. A rectifier follows the receiver LC-tank circuit to convert the AC carrier signal to a DC voltage, which supplies the rest of the system after being regulated. The small coupling coefficient between the two coils, particularly when they are misaligned, is the bottleneck in inductive power transmission. Hence, the received power is considered precious and should be preserved in the AC–DC conversion process. Radio frequency identification (RFID), implantable microelectronic devices, and wireless sensors are some of the size-constrained applications in which an integrated rectifier plays a significant role [1–4]. Taking the cost into consideration, leads application specific integrated circuit (ASIC) designers of such systems towards implementing the entire system, including the rectifier, on a single chip (SoC) in standard CMOS technology.

However, up until recently CMOS rectifiers have generally suffered from low power conversion efficiency (PCE) mainly due to the large dropout voltage across the diode-connected MOSFETs that were biased in the saturation region [5]. Other factors that can potentially degrade the PCE include reverse current from the load back to the receiver LC-tank circuit and the leakage current into the substrate. A few research groups have proposed different methods to address these issues in their IC-rectifier designs [6–10]. However there is still a lack of detailed analysis and deep understanding about how these IC-rectifiers work and what parameters affect their performance the most. This knowledge is necessary in design and development of new SoC ASICs for the aforementioned applications.

In this paper we explain the analysis, design, and implementation of a new synchronous full-wave CMOS rectifier with minimized dropout voltage through active biasing of the main conducting MOSFETs in the deep triode region, eliminating the body effect, and decreasing

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the reverse and substrate leakage currents. We also ensure the rectifier safe startup by employing a supporting parallel path. Simulation and measurement results on a prototype rectifier have been described followed by a detailed discussion of how to model and optimize various rectifier design parameters.

2 Circuit description

A generic inductive link for power transmission through L_1 and L_2 plus a simplified schematic of the proposed rectifier are shown in Fig. 1. Instead of diode-connecting the main rectifying PMOS transistors (P_1, P_2) as in our prior work [5], a pair of comparators is used here to sense the difference between the input coil voltages (V_{C1}, V_{C2}) and the rectified output voltage (V_{OUT}) across each rectifying PMOS. The comparator outputs switch $P_{1,2}$ on or off depending on whether $V_{C1,2}$ are greater or lesser than V_{OUT}, respectively. When the comparator outputs are low, $V_{SG1,2} \approx V_{C1,2} > (V_{SD1,2} + |V_{TP}|)$, where V_{TP} is the PMOS threshold voltage and $V_{SD1,2} = V_{C1,2} - V_{OUT}$. Hence, as long as $V_{OUT} > |V_{TP}|$, which is usually the case during rectifier normal operation, $P_{1,2}$ are pushed into deep triode region. Therefore, they produce a much smaller dropout, $V_{SD1,2}$, along the forward current path from the L_2C_P tank to the R_LC_L load compared to when they are in saturation.

Similarly, N_1 and N_2 experience a large $V_{GS1,2} = V_{C1,2} > V_{TN}$ when they are on and, therefore, show a small dropout in the return current path from load back to the L_2C_P tank. Further, $P_{1\sim5}$ have been implemented in separate n-well regions and their bulk voltages are dynamically controlled using a pair of auxiliary PMOS devices (P_{1A}, P_{1B}) to eliminate the body-effect and substrate leakage. This would also reduce the risk of latch-up by keeping parasitic BJT transistors off [5]. All of these provisions help improving the rectifier PCE.

One of the challenges in this design was to provide a stable operating voltage for the comparators during rectifier startup when V_{OUT} has not yet been stabilized. This could potentially be fatal for the rectifier operation since it can result in the rectifier not to wakeup as a result of $P_{1,2}$ staying off due to lack of proper gate drive. Our solution was utilizing a diode-connected startup rectifier, $P_{3,4}$, in parallel with the main rectifier to quickly charge a relatively small capacitor, C_{SUP} = 1 nF, and provide an early operating supply, V_{SUP}, just for the comparators in Fig. 1. It should be noted that $N_{1,2}$ can provide the return current path for both the startup and main rectifiers. Once V_{OUT} raises above V_{SUP}, due to smaller dropout, transistor P_5, which is controlled by a threshold voltage monitoring circuit, connects V_{OUT} to V_{SUP} and automatically turns the startup rectifier off.

In the rest of this section we describe the details of the rectifier operation, some of the design issues, and post-layout simulation waveforms.

2.1 Comparators

The key components in this IC-rectifier topology, which determine its performance, are the two comparators, $A_{1,2}$, in Fig. 1. Our simulations show that the faster these comparators operate would be the better for the PCE, as long as their power consumption is negligible w.r.t. the rectifier output power (see Sect. 4). We used two-stage hysteresis

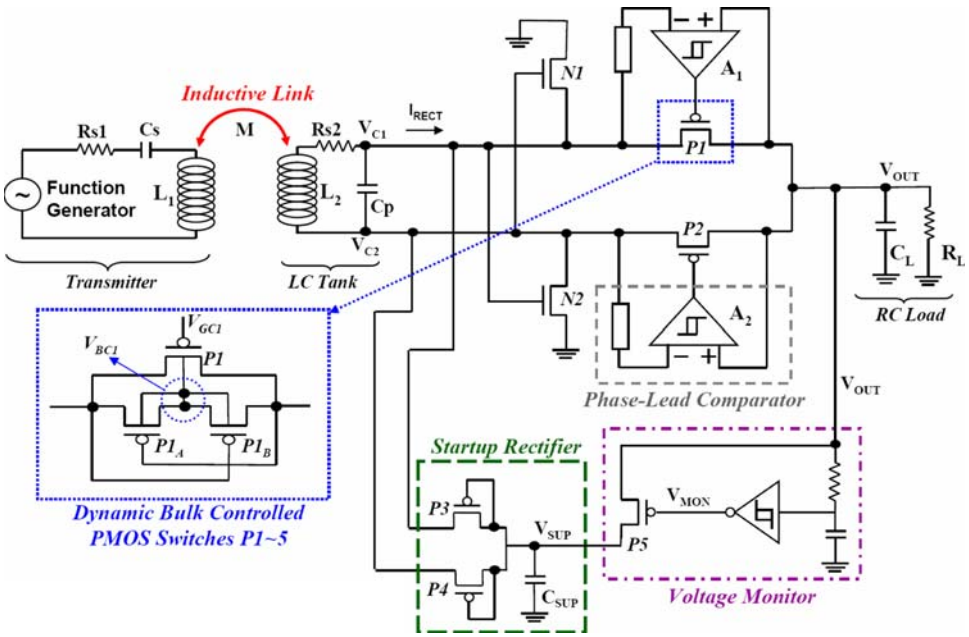

Fig. 1 Complete rectifier schematic including the inductive-link used for telemetry power transmission

comparators, shown in Fig. 2, and accelerated them with positive feedback [11]. Input common-mode range of the comparators have been extended beyond the supply level by utilizing an NMOS folded cascode differential pair. An output stage is also added to provide rail-to-rail output swing as well as high-speed driving capability of the large $P_{1,2}$ capacitive gate terminals ($W/L = 2500/0.6$). Hysteresis is important for this application to eliminate spurious output due to noise and interference at the input of the comparators, and to reject the dip in $V_{C1,2}$ when $P_{1,2}$ are turned on. This dip, shown in Fig. 3 simulation waveforms, is due to the fact that when current passes through P_1 and returns through N_2, the dropout across N_2 causes V_{C2} to become slightly negative and consequently decrease V_{C1}.

A supply-independent bias for the comparator is provided by a beta multiplier, which is designed to provide a 2 μA reference current [12]. Both the bias generator and comparator are connected to V_{SUP} to quickly start up and initiate the main rectification process. There exists a possibility of back current propagation from the ripple-rejection capacitor, C_L, back to the coil when $V_{C1,2} < V_{OUT}$

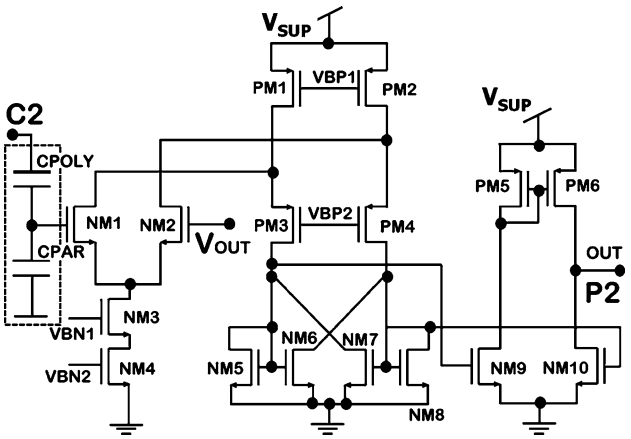

Fig. 2 Comparator schematic representing the gray dashed box in Fig. 1

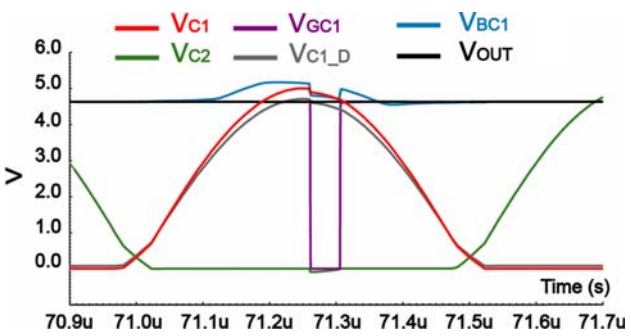

Fig. 3 Simulation results showing the input coil voltages ($V_{C1,2}$), capacitively divided V_{C1} voltage (V_{C1_D}), voltage at gate and bulk terminals for P_1 (V_{GC1} and V_{BC1}), and the rectifier output DC voltage (V_{OUT})

and the comparator tends to switch $P_{1,2}$ off. This current, which can reduce the rectifier PCE by stealing the stored charge from C_L, is mainly resulted from the comparators' delay. Increasing the comparators switching speed would be helpful only up to a certain extent because it often costs more power consumption, which also degrades the PCE. Our remedy was to create a phase-lead and initiate an early comparison by utilizing lossless capacitive voltage dividers at the negative input terminal of each comparator, as shown in Figs. 1 and 2. The small phase-lead will compensate for the comparator delay at the onset of $P_{1,2}$ turning on and off. The effect of the capacitive divider on the L_2C_P resonance frequency can be accounted for by adjusting the value of C_P.

The capacitive division is achieved by using a poly-poly capacitor, C_{POLY}, and the input parasitic gate capacitance of the comparator folded cascode NMOS, C_{PAR}, as shown in Fig. 2. Even though C_{PAR} is highly nonlinear, since $P_{1,2}$ switching mainly takes place when the coil voltages are high, we can expect C_{PAR} to show a constant capacitance in the strong inversion region. Care must be taken in layout by connecting the bottom plate of C_{POLY} to the input coil nodes and not to the floating input node of the comparator.

In this design, the comparator delay, hysteresis, and capacitive divider work synergistically to prevent reverse currents (see Sect. 4.5). Disruptions in their balance can lead to PCE degradation. For example, an increased comparator hysteresis delays $P_{1,2}$ firing and lowers the PCE. The effect of capacitive voltage divider is more complicated. An increased ratio would mean that $P_{1,2}$ turn on early and turn off late. This would result in reverse currents before and after $V_{C1,2}$ peaks and lowers the PCE. Therefore, an adjustment mechanism for one or more of these parameters would be desirable. Simulation waveforms in Fig. 3 show comparator A_1 operation with V_{OUT} and V_{C1D} being its inputs and V_{GC1} as its output.

2.2 Output voltage monitor

Comparators $A_{1,2}$ are initially powered by the startup rectifier ($P_{3,4}$) to quickly become functional and kick off the main rectifier. However, once the main rectifier started, V_{OUT} easily surpasses V_{SUP} due to its smaller dropout voltage. Thus, it would be necessary to supply the comparators from V_{OUT} to extend their input dynamic range. A simple circuit, shown in Fig. 4(a), which has no static power consumption, monitors V_{OUT} and as it surpasses a certain threshold ($2|V_{TP}|$), activates a one-shot circuit to turn P_5 on after a short delay (R_MC_M) [13]. Note that the last inverter in the chain must be supplied by V_{SUP} since during the time when V_{OUT} is not yet stable, P_5 should be kept off by the only stable voltage present on chip, which is V_{SUP}. It can be seen in the rectifier startup simulation in

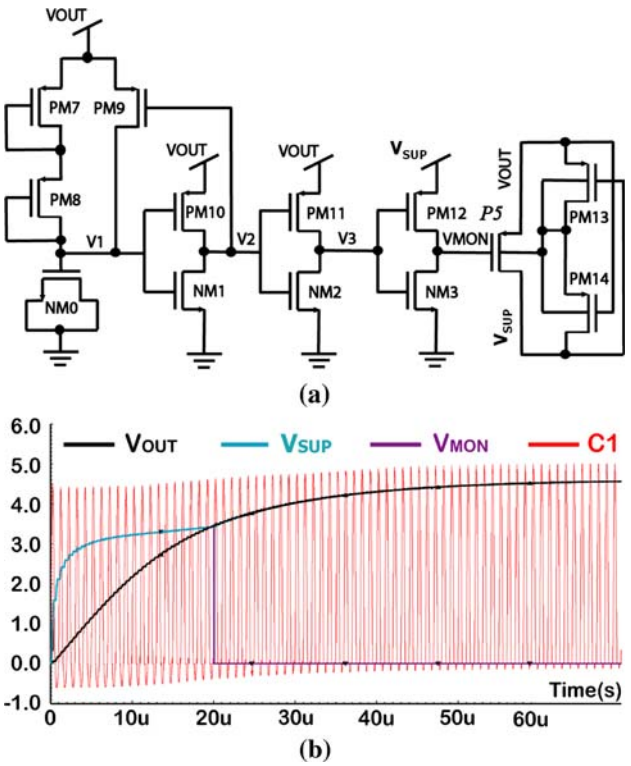

Fig. 4 (**a**) Schematic diagram of the output voltage monitor. (**b**) Post-layout transient simulation of the rectifier waveforms at startup

Fig. 4(b) that V_{SUP} raises rapidly up to about 3.5 V in ~4 µs. However, it takes V_{OUT} about 20 µs to catch up. Then the output monitor turns P_5 on, shorting V_{SUP} to V_{OUT}. This automatically turns the less efficient startup rectifier off.

3 Measurement results

A prototype IC-rectifier was designed and fabricated in the AMI 0.5-µm n-well 5 V standard CMOS process through MOSIS for a nominal loading of R_L = 1 kΩ. Figure 5 shows the rectifier die microphotograph in which we have maximized the separation between highly dynamic $P_{1,2}$ and $N_{1,2}$ transistors, and equipped them with guard-rings to further reduce the risk of latch-up and substrate leakage. The IC-rectifier occupies ~0.4 mm^2 of silicon area in this process.

To test the rectifier, we setup an inductive wireless link similar to Fig. 1 using a pair of planar spiral coils with primary and secondary inductances of L_1 = 24.3 and L_2 = 14.8 µH, respectively. The relative distance between the coils was 10 mm, about the average thickness of the human skin, and their geometries were optimized for operation at 1 MHz as described in [14]. The coupling coefficient between the coils when they were aligned was measured $k \approx 0.25$ using a network analyzer (Agilent E5071B). L_1 was driven by an HP 8111A function generator, and measurements on L_2 were done using a multichannel digital oscilloscope (Tektronix DPO-4034). Figure 6 shows the measured rectifier waveforms when $V_{C1,2}(peak) = 5$ V, $f = 0.5$ MHz, and the rectifier is loaded with $R_L \| C_L = 1\,\text{k}\Omega \| 1\,\mu\text{F}$.

The measured rectifier performance is shown in Fig. 7 in terms of PCE and V_{OUT} vs. f and R_L when $V_{C1,2}(peak) = 5$ V. In the present prototype, which was not optimized, we could achieve a maximum PCE = 84.8% and V_{OUT} = 4.36 V around $f = 0.5$ MHz, while PCE was above 80% in the frequency range of 0.125–1 MHz. Figure 7(b) illustrates the effects of R_L variations on the IC-rectifier dropout voltage that affects PCE and V_{OUT}. It should be noted that dropout voltage also depend on the sizes of the rectifying elements ($P_{1,2}$ and $N_{1,2}$) as discussed in Sect. 4.4. For heavy loads, $R_L < 1$ kΩ, PCE decreases due to the increased dropout across $P_{1,2}$ and $N_{1,2}$, while D increases. For light loads, $R_L > 1$ kΩ, the output power

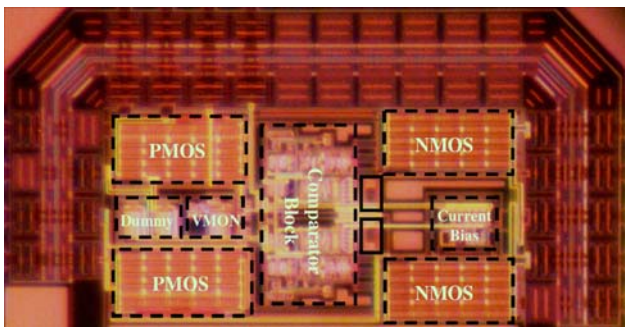

Fig. 5 Die photo of the IC-rectifier in the AMI-0.5 µm CMOS process

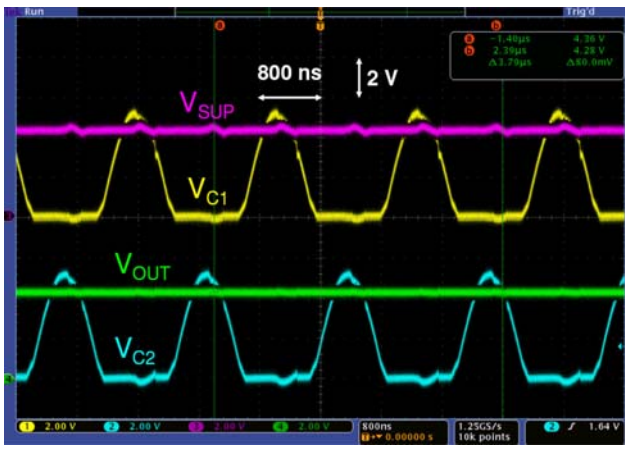

Fig. 6 Measured IC-rectifier input and output waveforms when $V_{C1,2}(peak) = 5$ V, $R_L = 1$ kΩ and $C_L = 1$ µF (see Fig. 1 schematic)

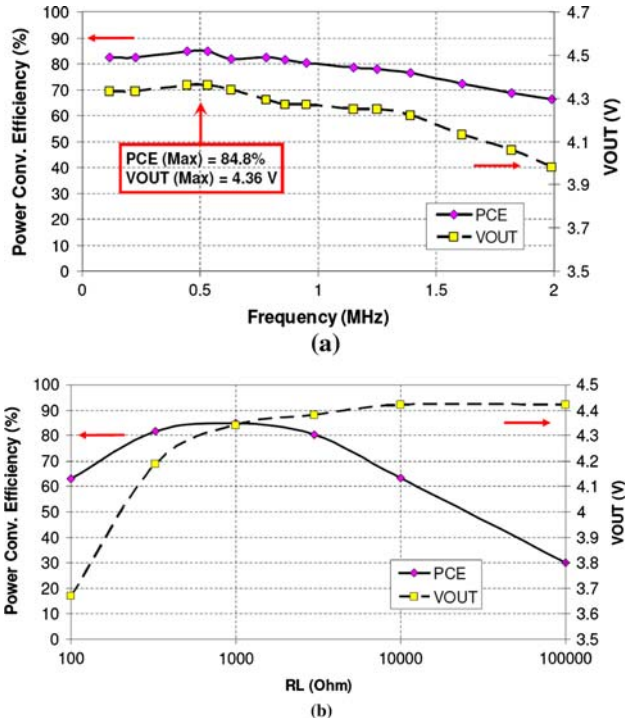

Fig. 7 Measured rectifier PCE and V_{OUT} when $V_{C1,2}(peak) = 5$ V and $C_L = 1$ μF. (**a**) As a function of input carrier frequency (f) with $R_L = 1$ kΩ. (**b**) As a function of R_L at $f = 0.5$ MHz

becomes comparable to the rectifier's internal losses, hence decreasing the PCE.

4 Discussion

In this section, we model and analyze the operation of the active rectifier to gain greater quantitative insight into various parameters that affect the RC-loaded IC-rectifier PCE. In the following subsections, we use a simplified rectifier model to derive a closed-form approximation for the PCE and verify our model through numerous simulations. We find a closed-form expression for an optimal MOSFET switch-size for the rectifying elements, and finally demonstrate the effects of using the capacitive phase-lead divider on the PCE.

4.1 Triangular waveform approximation

A simplified equivalent circuit of a rectifier can be represented by a switch connecting a sinusoidal voltage source to an RC load whenever $V_{IN} > V_{OUT}$ as shown in Fig. 8(a). A series resistor, R_s, represents the switch parasitic resistance during conduction. The switch off resistance is considered infinite in this simple model. If we ignore the

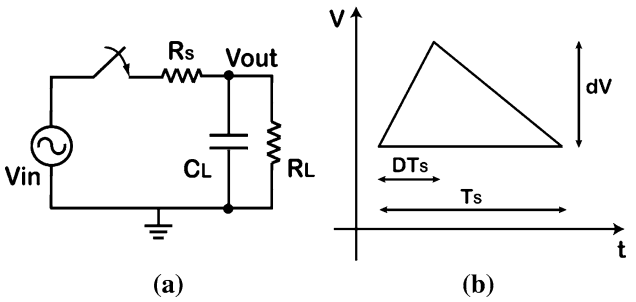

Fig. 8 (**a**) Equivalent circuit model of a half-wave rectifier. (**b**) Triangular approximation of the V_{OUT} steady state ripple waveform during charging and discharging phases of C_L when the rectifier switch closes and opens with duty cycle, D, in every carrier cycle, $T_S = 1/f$. The same model applies to full-wave rectifiers if V_{IN} is commutated and $T_S = 1/2f$

switching delay and assume that the output peak-to-peak ripple, ΔV, is small compared to V_{OUT}, the charging and discharging of C_L, which are sine and exponential functions, respectively, can be approximated with linear functions and represented by the triangular waveform shown in Fig. 8(b). The charge acquired by C_L when the switch is closed is given by

$$Q_{CH} = C_L \cdot \Delta V = (I_{RS} - I_{RL}) \cdot D \cdot T_S, \tag{4.1.1}$$

where I_{RS} is the average current flowing through the switch, $I_{RL} = V_{OUT}/R_L$ is the average current flowing through R_L, D is the rectifier switching duty cycle, and T_S is 100% or 50% of the period of the input sinusoid ($1/f$) in half- or full-wave rectifiers, respectively. Similarly, the charge lost by C_L when the switch is open is given by

$$Q_{DISCH} = C_L \cdot \Delta V = I_{RL} \cdot (1 - D) \cdot T_S. \tag{4.1.2}$$

At steady state, the amount of charge gained and lost by C_L are equal, and by equating (4.1.1) and (4.1.2),

$$I_{RS} = \frac{V_{OUT}}{D \cdot R_L}. \tag{4.1.3}$$

Using this simple model, we can approximate the average output power and the power dissipated in R_S,

$$P_{OUT} = {I_{RL}}^2 \cdot R_L, \tag{4.1.4}$$

$$P_{DISS} = {I_{RS}}^2 \cdot R_S \cdot D. \tag{4.1.5}$$

Hence, the rectifier PCE is given by

$$\eta = \frac{P_{OUT}}{P_{DISS} + P_{OUT}} = \frac{{I_{RL}}^2 \cdot R_L}{{I_{RS}}^2 \cdot R_S \cdot D + {I_{RL}}^2 \cdot R_L}. \tag{4.1.6}$$

Substituting I_{RL} and I_{RS} in (4.1.6),

$$\eta = \frac{1}{1 + \frac{R_S}{D \cdot R_L}}. \tag{4.1.7}$$

An obvious conclusion from (4.1.7) is that the PCE increases by reducing the switch parasitic resistance, R_S. In our

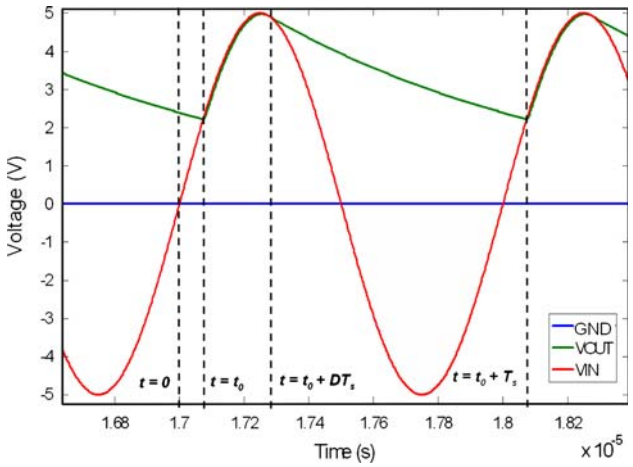

Fig. 9 Half-wave rectifier waveforms generated in MATLAB based on more realistic differential equations setup in Sect. 4.2 to find the relationship between switching duty cycle, D, and other circuit parameters in Fig. 8(a). $V_{IN} = 5$ V, $f = 1$ MHz, $R_S = 5\ \Omega$, $R_L = 1$ kΩ, and $C_L = 1$ nF

prototype implementation, we have tried to achieve this by biasing the switching MOSFETs in deep triode region, where they show the lowest resistance. A less intuitive insight from this simple model is that the PCE is also a function of R_L and the rectifier duty cycle, D, which in turn depends on the ripple rejection filter, C_L, and other circuit parameters. An increase in D tends to increase the PCE, which explains why a full-wave rectifier is preferred over a half-wave one. In the next section, we find the relationship between the rectifier duty cycle, D, and other rectifier circuit parameters.

4.2 Rectifier differential equations

The IC-rectifier PCE can be modeled using the 1st order differential equations that describe the simple equivalent circuit in Fig. 8(a) when the switch is open or closed. In Fig. 9, a more realistic charging and discharging sequence for C_L has been depicted with the time reference, $t = 0$, set at a zero-crossing of the input sine wave. At $t = t_0$, the switch closes and C_L charges till $t = t_0 + DT_S$. From this time onward, the switch opens and C_L exponentially discharges till $t = t_0 + T_S$. At steady state, $V_{OUT}(t_0) = V_{OUT}(t_0 + T_S)$ and

$$V_{OUT}(t_0 + T_S) = V_{OUT}(t_0 + DT_S) \cdot \exp\left(\frac{-(1-D)T_S}{R_L C_L}\right). \tag{4.2.1}$$

Therefore,

$$V_{OUT}(t_0 + DT_S) = V_{OUT}(t_0) \cdot \exp\left(\frac{(1-D)T_S}{R_L C_L}\right). \tag{4.2.2}$$

This is a relation between the initial and final V_{OUT} during C_L charging phase. For this phase, we can write the following differential equation using KCL at the output node,

$$\frac{V_{IN}(t) - V_{OUT}(t)}{R_S} = \frac{V_{OUT}(t)}{R_L} + C_L \frac{dV_{OUT}(t)}{dt}, \tag{4.2.3}$$

where V_{IN} is the AC input sine wave given by,

$$V_{IN}(t) = V_{C1}(t) - V_{C2}(t) = V_i \sin(\omega_0 t). \tag{4.2.4}$$

Solving this equation for V_{OUT} gives,

$$V_{OUT}(t) = A_i \sin(\omega_0 t - \theta) + K \times e^{\xi(t-t_0)} \tag{4.2.5}$$

$$\omega_0 = \frac{2\pi}{T_S}, \quad \theta = \tan^{-1}\left(\frac{\omega_0 R_{SW} C_L}{1 + (R_{SW}/R_L)}\right),$$

$$\xi = \frac{-1}{C_L \times (R_{SW} \| R_L)},$$

$$A_i = \frac{V_i}{\sqrt{(1 + (R_{SW}/R_L))^2 + (\omega_0 R_{SW} C_L)^2}},$$

$$K = V_{OUT}(t_0) - A_i \sin(\omega_0 t_0 - \theta).$$

The comparator firing angle, t_0, is another dependent parameter, which can be found with the assumptions that the comparator has negligible delay, offset, and hysteresis. Thus, as soon as V_{IN} crosses V_{OUT}, the switch changes its position,

$$V_{OUT}(t_0) = V_i \sin(\omega_0 t_0) \tag{4.2.6}$$

$$V_{OUT}(t_0 + DT_S) = V_i \sin(\omega_0 (t_0 + DT_S)) \tag{4.2.7}$$

Making use of (4.2.2)–(4.2.7), we can arrive at two equations that relate t_0 and D, to other circuit parameter,

$$\cot(\omega_0 t_0) = \frac{e^{\frac{(1-D)T_S}{R_L C_L}} - \cos(\omega_0 D T_S)}{\sin(\omega_0 D T_S)} \tag{4.2.8}$$

$$\cot(\omega_0 t_0) = \frac{\frac{V_i}{A_i}\left(e^{\frac{(1-D)T_S}{R_L C_L}} - e^{\xi_n D T_S}\right) - e^{\xi_n D T_S}\cos(\theta) - \cos(\omega_0 D T_S - \theta)}{\sin(\omega_0 D T_S - \theta) - \sin(-\theta) e^{\xi_n D T_S}} \tag{4.2.9}$$

It is also possible to eliminate t_0 from the above equations by simply subtracting them to find D,

$$f(D) = 0. \tag{4.2.10}$$

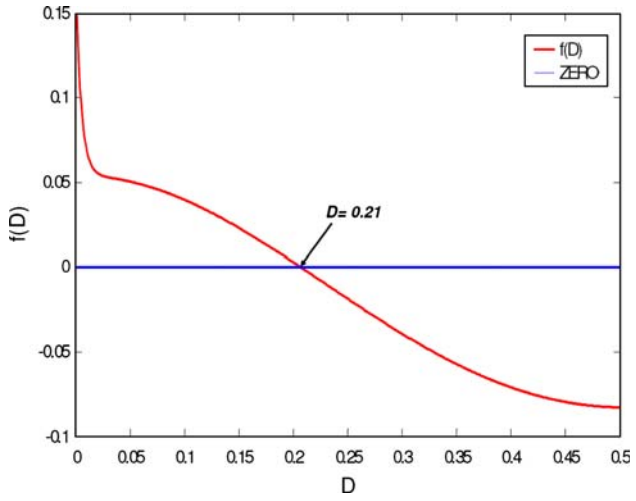

Fig. 10 Plot of $f(D)$, defined in Sect. 4.2, with zero crossing at $D = 0.21$ for $V_{IN} = 5$ V, $f = 1$ MHz, $R_S = 5\ \Omega$, $R_L = 1$ kΩ, and $C_L = 1$ nF in Fig. 8(a)

$f(D)$ is a nonlinear function and difficult to solve in a closed form. However, it can be solved numerically as shown in Fig. 10 where $f(D)$ is evaluated in the range, $0 < D < 0.5$, for a half-wave rectifier with $R_L = 1$ kΩ, $R_S = 5\Omega$, and $C_L = 1$ nF. Figure 10 shows that the solution to (4.2.10) in this condition is $D = 0.21$, which is also verified in SPICE simulations. Once having D and t_0, finding PCE would be straight forward.

4.3 A comparison between methods

We described an approximate closed-form expression for PCE in Sect. 4.1 and a numerical platform for the rectifier waveforms based on differential equations in Sect. 4.2. Here we call the PCE resulted from these methods *PCE-Aprx* and *PCE-Num*, respectively, and compare them with the PCE resulted from circuit simulation in SPICE, *PCE-Sim*. Our purpose is to validate and compare the accuracy of our PCE calculation models using the simulator as the gold standard.

We simulated the half-wave rectifier of Fig. 8(a) with $V_i = 5$ V at 1 MHz and an ideal comparator of negligible delay (<1 ns) controlling the switch that has $R_S = 5\Omega$. For *PCE-Aprx*, D is obtained from SPICE simulations first, and then fed into (4.1.7). Figure 11(a) shows PCE and D when $C_L = 1$ μF and R_L is swept from 10 Ω to 100 kΩ; Fig. 11(b) shows the same when $R_L = 1$ kΩ and C_L is swept from 100 pF to 100 μF, and in Fig. 11(c), $R_L = 1$ kΩ, $C_L = 1$ μF, and R_S is swept from 1 to 100 Ω. It can be seen that despite some minor differences, both approximation and numerical methods give accurate results in the practical range of interest. It can also be observed that *PCE-Aprx* often gives an optimistic estimate of the PCE.

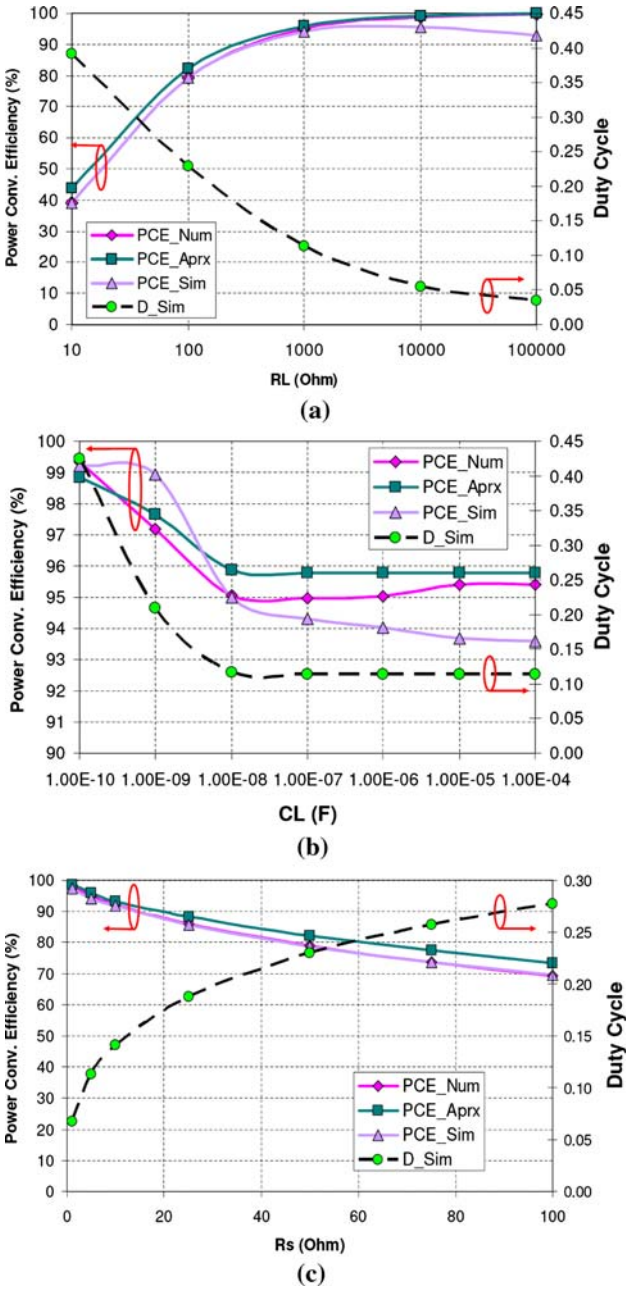

Fig. 11 Comparing closed form approximation, numerical differential equations, and SPICE simulation methods for evaluating the rectifier PCE vs. (**a**) R_L, (**b**) C_L and (**c**) R_S, chosen as variables. Nominal values are $C_L = 1$ μF, $R_L = 1$ kΩ, and $R_S = 5\ \Omega$

4.4 NMOS and PMOS switch-size optimization

Once given the nominal RC load and V_{IN}, one can design an IC-rectifier based on two different scenarios. First, an IC-rectifier with minimum possible silicon area that can provide a desired PCE. Second, an IC-rectifier with optimized switch-sizes for a given area on silicon that achieves the highest possible PCE. Considering 4.1.7 and Fig. 11(c), it is obvious that R_S needs to be minimized in both cases. In

the full-wave IC-rectifier of Fig. 1, the PMOS and the NMOS transistors P_1–N_2 and P_2–N_1 connect in series in the main current path during each half-wave conduction. Thus R_S would be the sum of their resistances while they operate in the triode region.

Two constraints for area and switch resistance can be given by the following equations [15]:

$$A = L \cdot (W_P + W_N), \tag{4.4.1}$$

$$R_S = L \cdot \left[\frac{1}{K_P \cdot W_P \cdot (V_{OUT} - |V_{THP}|)} + \frac{1}{K_N \cdot W_N \cdot (V_{OUT} - V_{THN})}\right] \tag{4.4.2}$$

where A, Area of the half-wave structure (mm^2); $K_P = \mu_P C_{ox}$, $K_N = \mu_N C_{ox}$ (A/V^2); W_P,W_N = Width of the PMOS and NMOS switches (mm); L = Length of the MOSFET switches (mm); and V_{THP}, V_{THN} = Threshold voltages of PMOS and NMOS (V).

Our assumptions are: the NMOS and PMOS gate drives are close to $V_{OUT} > |V_{THP}|$ and V_{THN} during conduction such that they are biased in deep triode region, and all MOSFET switches have the same length (L), which can be the minimum length allowed by the fabrication technology as long as their breakdown voltage is not a concern.

4.4.1 Minimizing area for a given switch resistance

In this case, we attempt to minimize (4.4.1) with W_P and W_N as variables keeping other parameters constant. W_N can be evaluated from (4.4.2) and substituted in (4.4.1),

$$A = L \cdot W_P + \frac{L^2}{K_N \cdot (V_{OUT} - V_{THN}) \cdot \left[R_S - \frac{L}{K_P \cdot W_P \cdot (V_{OUT} - |V_{THP}|)}\right]}. \tag{4.4.3}$$

This expression can be written in a simpler form,

$$A = L \cdot \left(W_P + 1 \Big/ \left[K_1 - \frac{K_2}{W_P}\right]\right), \tag{4.4.4}$$

by defining

$$K_1 = \frac{R_S \cdot K_N \cdot (V_{OUT} - V_{THN})}{L}, \tag{4.4.5}$$

$$K_2 = \frac{K_N \cdot (V_{OUT} - V_{THN})}{K_P \cdot (V_{OUT} - |V_{THP}|)}. \tag{4.4.6}$$

We can differentiate (4.4.4) w.r.t. W_P to find the roots that minimize A. The result after a few steps would be,

$$W_P = \left(\frac{K_2 + \sqrt{K_2}}{K_1}\right). \tag{4.4.7}$$

Substituting (4.4.5) and (4.4.6) in (4.4.7) we get,

$$W_P = \frac{L}{K_P \cdot R_S \cdot (V_{OUT} - |V_{THP}|)} + \frac{L}{R_S \sqrt{(K_N \cdot (V_{OUT} - V_{THN}))(K_P \cdot (V_{OUT} - |V_{THP}|))}} \tag{4.4.8}$$

Rearranging (4.4.8) and substituting (4.4.6), we get,

$$R_S = \frac{L}{K_P \cdot W_P \cdot (V_{OUT} - |V_{THP}|)} + \frac{L}{W_N \cdot K_N \cdot (V_{OUT} - V_{THN}) \cdot \left(\frac{W_P}{W_N}\right) \cdot \frac{1}{\sqrt{K_2}}} \tag{4.4.9}$$

Comparing (4.4.9) with (4.4.2) readily gives,

$$\left(\frac{W_P}{W_N}\right)_{opt} = \sqrt{K_2} = \sqrt{\frac{K_N \cdot (V_{OUT} - V_{THN})}{K_P \cdot (V_{OUT} - |V_{THP}|)}} \tag{4.4.10}$$

Equations 4.4.8–4.4.10 provide a useful guideline on how to choose the size of the PMOS and NMOS switches in an IC-rectifier to achieve the minimum area for a given R_S.

4.4.2 Minimizing switch resistance for a given area

In this case, we used (4.4.1) to eliminate W_N in (4.4.2),

$$W_N = \left(\frac{A}{L} - W_P\right) \tag{4.4.11}$$

$$R_S = \frac{L}{K_P \cdot W_P \cdot (V_{OUT} - |V_{THP}|)} + \frac{L}{K_N \cdot (V_{OUT} - V_{THN}) \cdot \left(\frac{A}{L} - W_P\right)}, \tag{4.4.12}$$

and minimized R_S by differentiating (4.4.12) w.r.t W_P and finding its roots.

Interestingly, the resulting optimal W_P for minimizing R_S when the area is given results in the same $(W_P/W_N)_{opt}$ ratio as in (4.4.10), confirming that in fact the same conditions apply to both aforementioned design scenarios. Hence, we can conclude that choosing $(W_P/W_N)_{opt}$ based on (4.4.10) results in minimum rectifier area and switch resistance.

As an example, we designed a rectifier based on the specifications listed in Table 1 from the AMI-0.5 μm standard CMOS process. The optimal ratio, $(W_P/W_N)_{opt}$ from (4.4.10) with $A = 2500$ μm^2 for the half-wave structure came out to be 1.78. Figure 12 shows R_S plotted using (4.4.12) for W_P in 0.5–4 mm range. It can be seen that $R_{S,min} = 2.33\ \Omega$ occurs at $W_P \approx 2700$ μm and $W_N \approx 1500$ μm. It is also observed that for 1.6 mm $< W_P <$ 3.5 mm, $R_S < 3\ \Omega$ and outside this range it increases rapidly.

In order to find the best possible PCE when only the losses in the rectifier switches are considered, we set up a

Table 1 Typical model parameters for AMI-0.5 μm process at room temperature

Process parameter	Symbol	Value
Minimum feature length	$L_{P,N}$	0.6 μm
PMOS transconductance parameter	$K_P = \mu_P C_{ox}$	36.8 μA/V^2
NMOS transconductance parameter	$K_N = \mu_N C_{ox}$	109.6 μA/V^2
NMOS threshold voltage	V_{THN}	0.67 V
PMOS threshold voltage	$\|V_{THP}\|$	0.90 V

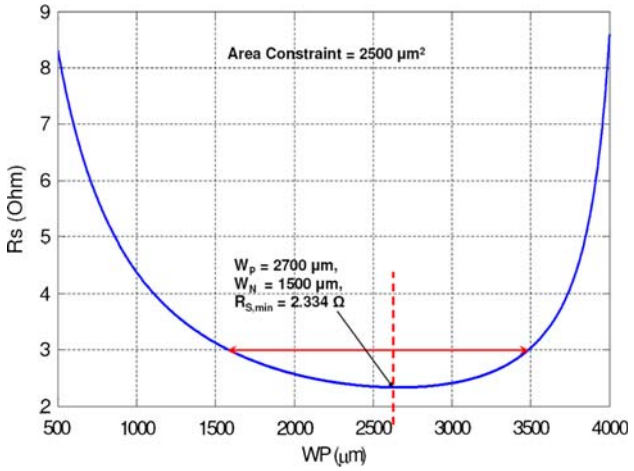

Fig. 12 Plot showing the variation of the total switch resistance, R_S, with the choice of the width of the PMOS transistor, for a given area constraint of $A = 2500$ μm^2 in AMI-0.5 μm standard CMOS technology (Table 1)

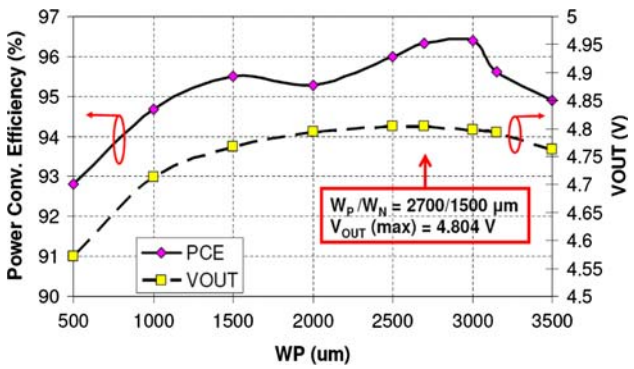

Fig. 13 SPICE simulation results showing the variation of PCE and V_{OUT} vs. the PMOS switch size (W_P) for a given silicon area, $A = 5000$ μm^2, in a full-wave IC-rectifier with ideal comparators in 0.5-μm CMOS technology

SPICE model for the full-wave rectifier in Fig. 1 using ideal comparators ($A_{1,2}$) to drive the gates of $P_{1,2}$ with no delay (<1 ns), hysteresis, offset, or power dissipation. It can be seen in Fig. 13, where W_P is swept from 0.5 to 3.5 mm and W_N is obtained from the area constraint (4.4.11), that V_{OUT} is indeed peaking at $W_P \approx 2700$ μm, which agrees with the results shown in Fig. 12. The PCE, however, peaks slightly higher at $W_P \approx 3000$ μm. We can attribute this change to the effect of a slightly higher switching duty cycle with higher W_P, which can improve the rectifier PCE according to (4.1.7).

Another observation that is important in design and optimization of IC-rectifiers is that R_S is a function of V_{OUT}, which is not known a priori. Therefore, assuming that the switching transistors' gate-drive is equal to $V_{C1,2}(peak)$ results in an optimistic estimate for R_S, V_{OUT}, and PCE. However, since the dropout voltage is small compared to V_{OUT} in this architecture, $V_{OUT} = V_{C1,2}(peak) = V_i$ would be an acceptable estimate in the first design step. Once V_{OUT} is found in simulations, as in Fig. 13, it can be used in successive iterations to obtain better $(W_P/W_N)_{opt}$, R_S, and PCE estimates.

4.5 Effect of phase-lead control

In this section, we take a closer look at the effects of the phase-lead capacitive divider in the control of back currents from C_L to the L_2C_P tank. For this purpose, we built a rectifier model in SPICE using an ideal comparator with adjustable delay, T_d, for both rising and falling edges. The sizes of the rectifying elements in this case were the same as the prototype implementation specified in Table 2. Figure 14 compares the PCE for compensated and uncompensated rectifiers vs. T_d. It can be seen that the capacitive phase-lead, described in Sect. 2.1, is quite effective in maintaining a high PCE especially for slower comparators or when the carrier frequency is high and T_d is comparable to T_S. Figure 14 also shows the required ratio, $\sigma = C_{POLY}/(C_{PAR} + C_{POLY})$, that would maximize the PCE for each delay. It should also be noted that increased T_d results in a slight degradation in the

Table 2 Full-wave IC-rectifier specifications

Parameter	Value (Simulation)
Fabrication process	AMI 0.5-μm, 3M/2P, n-well
Die size (including 2 rectifiers)	1.5 × 1.5 mm^2
Active silicon area	0.4 mm^2
$(W/L)_{P_1,P_2,N_1,N_2}$	2.5 mm/0.6 μm
Carrier frequency range (f)	0.1–2 MHz
Maximum input voltage	5 V
V_{OUT} @ 0.5 MHz	4.36 V (4.6 V)
PCE @ 0.5 MHz	84.8% (90.4%)
Static current consumption	60 μA (58 μA)
Nominal loading (R_L)	1 kΩ
Filter capacitors (C_L & C_{SUP})	1 μF & 1 nF

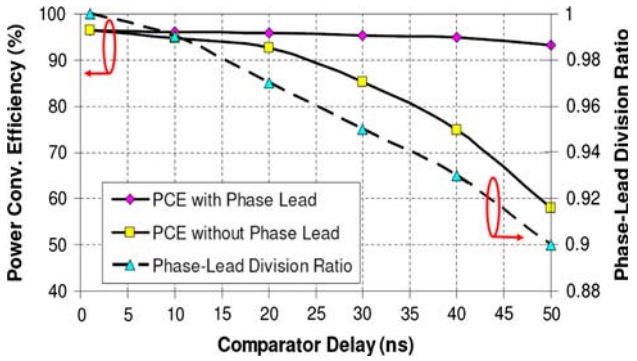

Fig. 14 PCE variation vs. comparator delay, T_d, at 1 MHz with and without phase-lead compensation using a capacitive divider with the voltage division ratio shown on the left vertical axis. The capacitive divider is added to the input of the comparator to control the reverse current

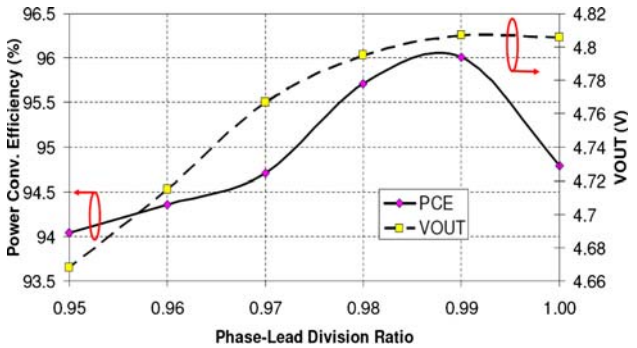

Fig. 15 PCE variations vs. phase-lead division ratio, $\sigma = C_{POLY}/(C_{PAR} + C_{POLY})$, for a fixed comparator delay of $T_d = 10$ ns when $V_{IN} = 5$ V at 1 MHz

PCE despite phase-lead compensation because of the steady reduction in the switching duty cycle, D.

As mentioned earlier, the rectifier PCE is quite sensitive to the phase-lead capacitive divider ratio. Figure 15 shows how PCE changes vs. σ for a constant delay of $T_d = 10$ ns, and peaks at $\sigma \approx 0.99$. In practice, process variations and various mismatches can affect σ. In addition, the comparator rising and falling delays are not necessarily equal. For the latter case, σ should be indicated based on the comparator delay at the time of the switch being opened. Further, the comparator being a voltage/current sense-and-amplification device, its delay would always be a function of the input voltage amplitude and frequency, as well as the corresponding output voltage level [16]. These effects along with the comparator offset, hysteresis, and dynamic non-idealities can complicate evaluation of the right value for σ. Therefore, σ may need to be empirically adjusted for the chosen comparator topology, and a certain degree of programmability or control via a closed-loop feedback would be desirable.

5 Conclusions

We have presented an integrated active full-wave CMOS rectifier that can achieve low dropout voltage and high power conversion efficiency. This is accomplished by employing a pair of fast comparators to monitor the difference between the input and output voltages, and keep the rectifying PMOS and NMOS switches in the deep triode region when the input voltage is higher than the output voltage. This would result in a small dropout across the switches and improves the PCE.

Mathematical analysis and modeling as well as circuit simulations are performed to understand the factors influencing the IC-rectifier characteristics, particularly its PCE, which provides ASIC designers with the necessary understanding about the relationships between the IC-rectifier PCE, switching duty cycle, and other circuit- and process-dependent parameters. In addition, size optimization of the PMOS and NMOS switching elements, operating in deep triode region, was performed for PCE- and silicon area-centered design criteria.

A prototype rectifier was designed and fabricated in the AMI-0.5 μm standard CMOS process occupying an active area of ~ 0.4 mm^2. An output voltage of 4.36 V was reached at 0.5 MHz with an input voltage of 5 V_{Peak} and loading of 1 kΩ in parallel with 1 μF for ripple rejection. The measured efficiency of the prototype rectifier was 84.8%. A summary of the prototype rectifier specifications is given in Table 2. From the discussions in Sect. 4, it can be deduced that this IC-rectifier can be further optimized in terms of chip area, capacitive phase-lead, dropout voltage, and PCE.

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