Preliminary report on master project

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1 Introduction

This report is a brief overview of my master project on wireless power transfer through inductive coupling. It is the documentation of the schematic of complete design of the power receiving unit. It includes brief explanation about choices of design topologies and techniques. Figure 1 is the block diagram of the complete design including the test PCB and the test chip on it.

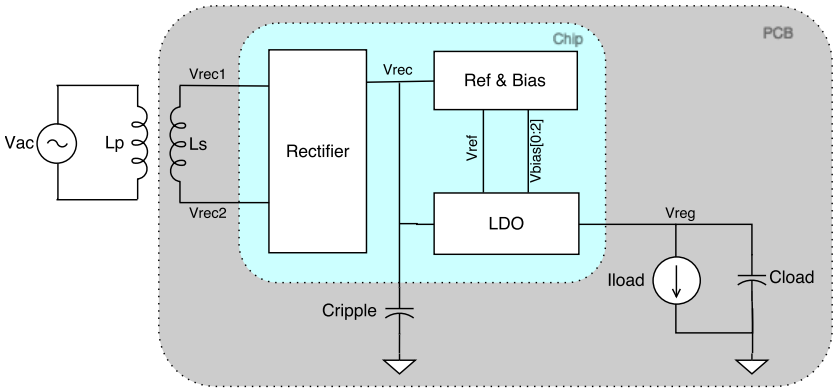


Figure 1: Block diagram of complete design

As shown in the block diagram above, the design includes antennas rectifier, LDO regulator and reference and biasing circuits. This report mainly discusses about the various design aspect of rectifier and LDO. The inductor is designed with the specifications provided by NORDIC. The biasing and reference circuit is designed solely for learning the design technique without much effort on the accuracy of the generated biases and references. So externally supplied bias and reference will be the secondary option. The project is designed in tsmc90nm process. Table 1 lists the main specifications of this project.

Table 1: Project specifications

Technology	TSMC 90nm CMOS
Chip area	TBA mm^2
Vpp for chip	2.5 V
Max. load	10 mA
Output dc voltage	1.8 V

A brief discussion of rectifier design is followed next.

2 Rectifier

The most basic rectifier is conventional full wave bridge structure where the diodes are replaced by the diode connected MOS. devices in CMOS. technology. This topology though being simple to implement, has a major drawback. It requires at least twice the Vtn of a MOS device as there are two diode connected MOSes in the conduction path for each cycle of the input signal.

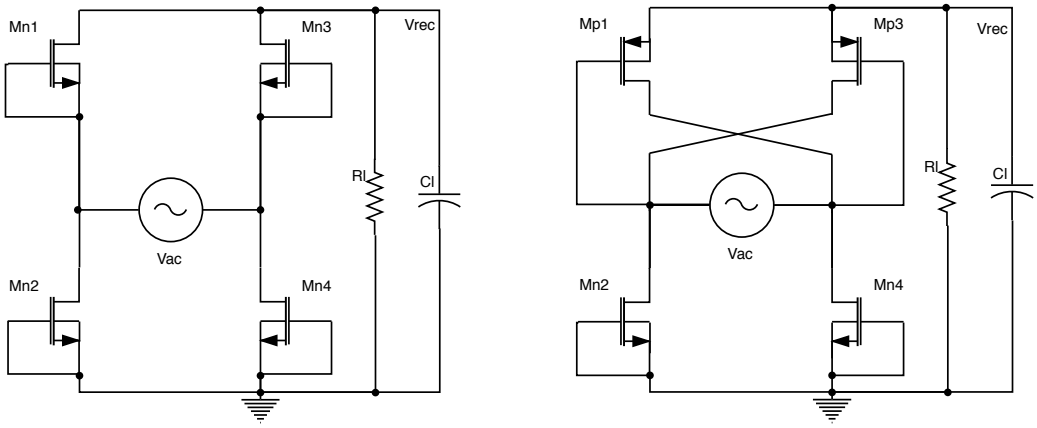
Gate cross coupled and fully gate cross coupled topologies are improvements over conventional full wave rectifier. In gate cross coupled rectifier, two diodes of conventional rectifier is replaced by two gate cross coupled MOSes working as switches where the voltage drop for every cycle is reduced to one threshold voltage. Similarly, in the fully gate cross coupled rectifier, all diodes are replaced by switches and hence the voltage drop is further reduced to twice the conduction drop only for every cycle. Even though this topology has least voltage drop, it suffers from the problem of reverse charge leakage because when the input ac amplitude is less than the output rectified voltage and the conducting pass devices are on simultaneously, current flows backward from output to input.

All the above discussed topology suffer from either large voltage drop or large power loss because of which their use are limited in low power and low voltage devices. The popular techniques for higher efficiency are using gate cross coupled rectifier along with passive or active circuitry for controlling other two pass devices. In passive rectifier, additional circuitry including bootstrap capacitor are used to reduce or eliminate threshold voltage one of which is discussed in this paper [**rectboot**]. However, use of on-chip bootstrap capacitors limits it use where chip area and speed is of importance. On the other hand, in active rectifier, active circuitry is used control pass devices. The use of active circuitry increase both voltage conversion efficiency (VCE) and power conversion efficiency (PCE) because the pass devices are made to conduct in linear region and hence less conduction drop, and reverse current flow can be completely eliminated and hence less power loss. However active rectifier is not problem free either. The major issue is starting of the active circuit as there is no regulated supply at the start up.

In this project, active rectifier is chosen, primarily for better VCE

and PCE and secondarily to avoid the use large on chip capacitors. [**rectrcc**] and [**rectcomp**] have discussed same active rectifier topology with a slight difference in active circuitry. [**rectrcc**] has implemented comparator with compensating the delay of comparator's output falling whereas [**rectcomp**] has implemented comparator with compensating both the falling and the rising delay of comparator's output in expense of added circuit complexity and power consumption. [**rectrcc**] has been used here for its simple design.

Figure 2a, 2b and 3a is the CMOS implementation of conventional full wave bridge rectifier, gate cross coupled rectifier and proposed active rectifier in [**rectrcc**]. The problem with 2a and 2b has already been briefly mentioned above. Though 2b is significantly improvement over 2a , it is still not a favourable topology with respect to the design technology chosen. In the gate cross couple rectifier of 2b, the cross coupled pMOSes act as switches, so the only voltage drop across them is conduction drop due to channel resistance. However the other two nMOSes are diode connected, so they have at least Vtn drop across them which means $Vac \geq Vdc + Vtn$ for conduction.



(a) Conventional full wave bridge rectifier

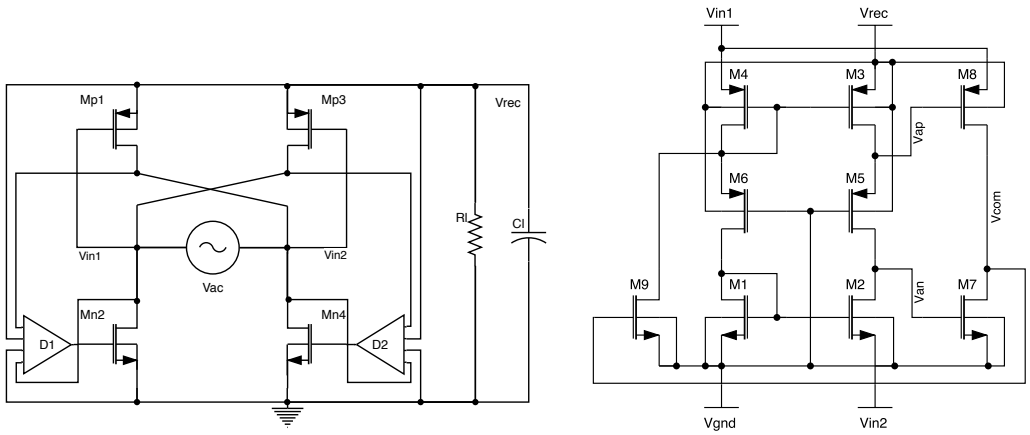
(b) Gate cross coupled full wave rectifier

Figure 2: Rectifier topologies: conventional and gate cross coupled

The proposed active circuit in 3a is improvement over 2b which eliminates Vtn drop required for conduction by replacing diode connected nMOS with devices controlled by active circuit as shown in figure 3b. The active circuit is a four input comparator that turns on nMOSes

fast when Vac > Vdc and turns off fast to avoid flow of current.

For the illustration of operation of comparator, consider the case when $Vin1 > Vin2$ i.e. $Vin1 > 0$ and $Vin2 < 0$. During this half cycle, comparator $D1$ output is low and turns off $Mn2$ and also, $Mp1$ is reversed biased and hence there is no path to flow current along $Mn2$ and $Mp1$. For simplicity, assume $Vac = Vin1 - Vin2$. When Vac reaches Vtp, $Mp3$ turns on which shorts $Vin1$ to $Vrec$. When $Vac > Vrec$, $D2$ output goes high, which turns on $Mn4$ and starts the conduction path for the first half cycle and starts charging Cl. When Vac reaches maximum, it starts to decrease and at $Vac < Vrec$, conduction stops as output of $D2$ is low and $Mn4$ is off. As Vac further decreases to below Vtp, $Mp3$ if off too. This way rectifier in 3a conducts during positive half cycle eliminating the Vtn drop seen in 2b. Now the only drop is the conduction drop due to channel resistance of two pass devices along the conduction path. This drop is much less because during conduction both the device are operating in the linear region with small resistance. The operation is similar for $Vin2 > Vin1$ where $Mn4$ and $Mp3$ are off and $Mn2$ and $Mp1$ conduct to charge Cl.



(a) Gate cross coupled full wave active rectifer (b) Active circuit $D2$

Figure 3: Active rectifier and active circuitry (comparator)

Figure 3b is the implementation of four input comparator $D2$ used in 3a as proposed in [**rectrcc**]. It is designed to self power and bias because no steady state supply is available at start up. $M1$, $M2$ and $M7$ monitors voltage across $Mn4$ i.e $Vin2 - Vgnd$ and $M3$, $M4$ and $M8$ monitors voltage across $Mp3$ ie $Vin1 - Vrec$. So when $Vin1 - Vrec >$

$Vin2 - Vgnd$ which means $Vac > Vrec$, output of $D2$ is high and turns on $Mn4$ instantly. But when $Vac < Vrec$, the output of comparator is delayed to fall which causes $Mn4$ to conduct in reverse direction leading to significant reduction in power delivered to load. $M9$ is introduced in order to overcome this problem which adds offset currents to increase Van and Vpn faster, causing the output to decrease faster and turns off $Mn4$ before $Vac < Vrec$. This reverse current control technique compensates the comparator delay and increases the power efficiency of the rectifier.

The dimensions of the pass devices are first hand calculated by using square law current equation and devices parameters values given in the technology documents, and later optimised with simulation tool in order to make the rectifier to deliver the required current. Since nMOS does not have to have same device size as pMOS to deliver same current, optimal size ratio equation from [**rectsize**] is used to find nMOS pass devices sizes. Similarly, the value of ripple rejection capacitor is chosen 100nF for better ripple rejection at the expense of some additional settling time.

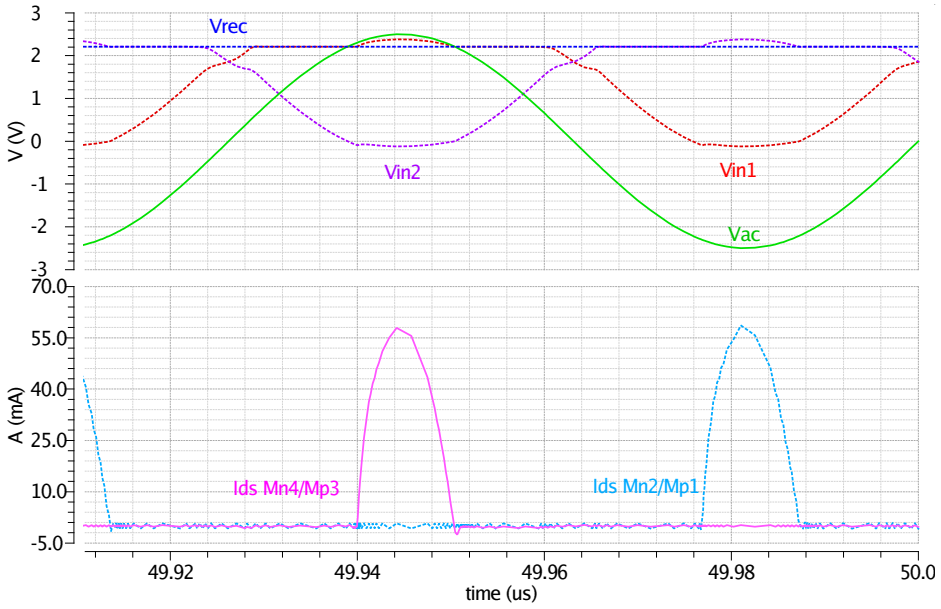


Figure 4: Voltage and current waveforms of the rectifier

Figure 4 show the simulation results showing voltages and current waveform of this designed rectifier. The generated waveforms clearly follows the working principle discussed above. Two important observa-

tions can be made from plots. First, the rectified output $Vrec$ is 2.2 V for Vpp ac input of 2.5 V which means the voltage loss has been significantly reduced and the loss of around 300 mV yields to the conduction loss due the the channel resistance. Secondly, the reverse current from output to input has been effectively eliminated as there is only positive current flowing to the load when all conducting devices are on. Similarly, figure 5 shows PCE and VCE with respect to magnitude peak ac input signal. Both PCE and VCE are very less for input ac amplitude less then 1.8 V. It can be explained by the fact that required bias current and gate drive voltage are not achieved for smaller input. Finally, table 2 summarises the rectifier design parameters and its performance.

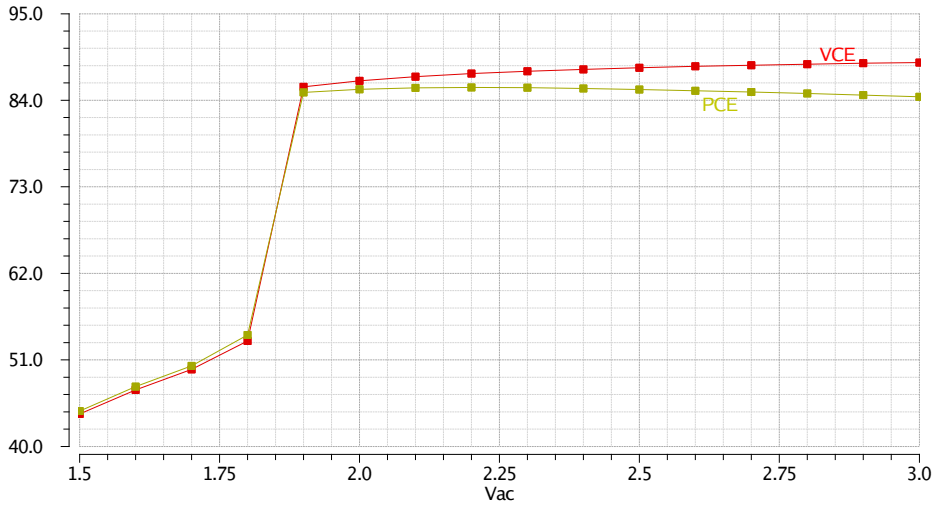


Figure 5: Voltage and power conversion efficiency

Table 2: Rectifier parameter and performance

Wn/Ln, Wp/Lp	550um/270nm, 900um/270nm
Rectifier area	TBA mm^2
Input ac frequency	13.56 MHz
Input ac Vp	2.5 V
Load current	11 mA
Ripple rejection cap	100nF
Output dc voltage	2.2 V
Ripple Vpp	3 mV
PCE	>85%
VCE	>88%

3 LDO

Voltage regulator follows the rectifier designed above in order to regulated the rectified voltage to 1.8 V and deliver maximum current of 10 mA. Since the output from the active rectifier is 2.2 V and the required regulated voltage is 1.8 V, charge pump or SMPS of boost type is irrelevant here. Buck SMPS could be an option for voltage regulation but LDO is preferred for it better performance in terms of noise and faster settling of regulated voltage. [**ldo_psu**].

Figure 6 shows a circuit of typical pMOS LDO. As shown in the figure, the components includes an error amplifier (EA), a pass device (Mpass), a feedback circuit (R1 and R2) and load (C_{out} and I_{load}). A more general and complete LDO circuit also includes the circuitry for generation of reference voltages and bias current/voltages. However, in this project it will be discussed separately for now. In short the working principle of LDO is that the error amplifier compares the scaled down regulated voltage, Vdiv with Vref and regulates the internal resistance of the pass transistor such that the error, V_{ref} - V_{div} is least or zero ideally.

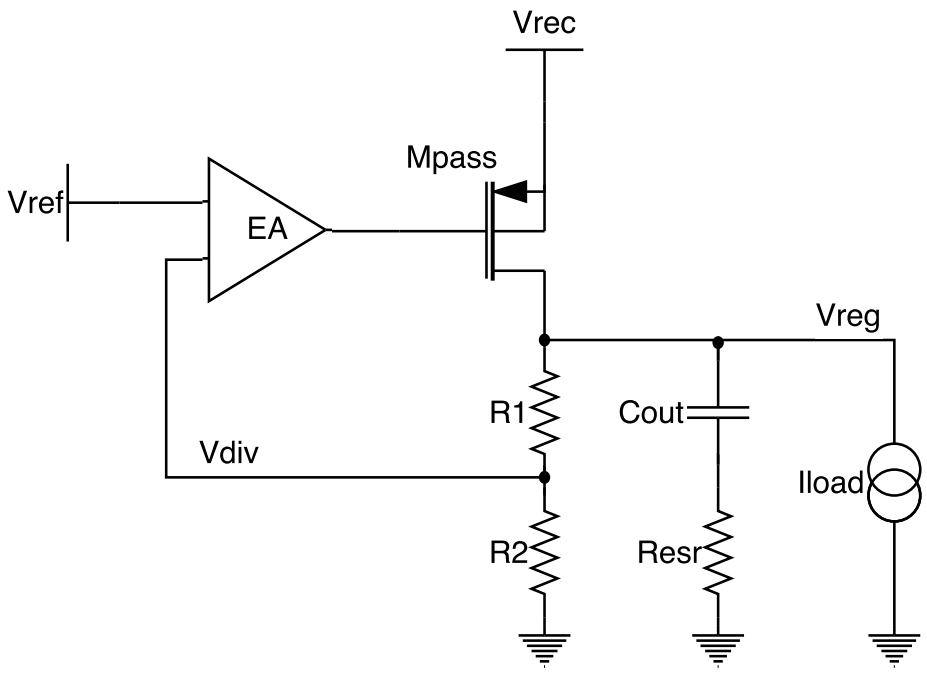


Figure 6: Generic LDO with pMOS pass device

[**ldo_bulkmod**] and [**ldo_quiescent**] are two examples of CMOS implementation of LDO. [**ldo_bulkmod**] has proposed bulk modulation technique for improving load regulation and stability of capacitorless LDO. Similarly [**ldo_quiescent**] has proposed techniques for increasing current efficiency of LDO especially at no or low load condition. Though the techniques discussed in these designs have not been used, they have given good insight into different design parameters of LDO.

Figure 7 shows the CMOS implementation of LDO in this project. The components in this design include a folded cascode differential amplifier as error amplifier, pMOS buffer, pMOS pass device and feedback network of resistors.

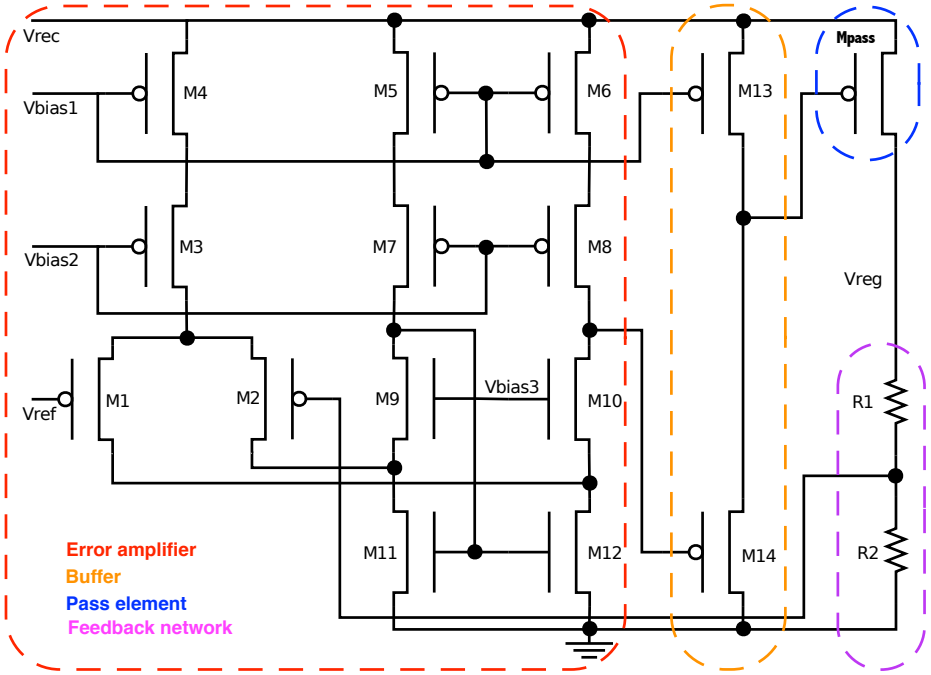


Figure 7: CMOS implemenation of LDO

As briefly mentioned above, the error amplifier amplifies scaled regulated voltage, V_{div} and reference voltage, V_{ref}. It is known that an amplifier with higher open loop DC gain reduced the closed loop gain error and hence amplifier with higher gain is desired here which is turn increase the accuracy of regulated voltage, Vreg [**ldo_bulkmod**]. Typically error amplifier has gain $> 40dB$ which is not achieved with the single stage amplifier with this technology. Higher gain could have

been achieved with multiple single stage but with increased difficulty in making the amplifier stable. So for achieving higher DC gain and at the same time for stability convenience, folded cascode amplifier [**razavi_2001**] is chosen.

The amplifier has a pMOS differential input stage in order to obtain lower ICMR of the amplifier closer to gnd because so is V_{ref}. In addition, this helps in pushing the poles at the folding point farther, easing the stability of the amplifier[**razavi_2001**]. Similarly, a pMOS buffer is used to supply sufficient current to drive the large pass transistor. Moreover, pMOS as buffer passes 1 better which means it can turn off the pass device completely and hence LDO regulates better at low load or no load condition. However at heavy load/large load current, the pMOS buffer is not able to pull down the gate of pass device as low as possible. This is overcome by making the pass device large enough to feed the required load current.

The pass device is a pMOS transistor in this design. It is chosen because it has several advantages over it's counterparts like nMOS and BJT devices in terms of dropout voltage, quiescent current, input voltage, thermal response and noise[**ldo_ti_pmos**]. Prominently, there are two factors that give pMOS edge over other devices; dropout voltage and quiescent current, when it comes to application in low power and low voltage devices. nMOS as a pass device requires a positive drive voltage with respect to output to operate. On the other hand, pMOS is driven by a negative signal with respect to input which means pMOS is preferable for a low input LDO. Similarly compared to BJTs, pMOS requires less headroom and less quiescent current to be driven[**ldo_ti_pmos**], [**ldo_ti_stability**], which means low dropout and low power operation, typical requirement of today's micro devices' power supply.

However, pMOS as a pass device in LDO causes challenges in stability. As mentioned above, LDO utilises a high gain feedback loop in order to provide a regulated output voltages independent of load current and in any system with feedback loop, the locations of poles and zeros determine stability of the system. In case of the pMOS LDO, the pass device is configured in a common source configuration. LDO with big output cap has a dominant pole pole at the output, which is a low frequency pole. The second pole is located at the gate of pass device because as mentioned earlier pMOS pass device is large and

has a big parasitic capacitance. This second pole may be located closer to the dominant pole, resulting in significant reduction in phase margin (PM). Consequently, this may lead to instability of the LDO with pMOS pass device. Various methods have been implemented for ensuring the stability of the pMOS LDO. In this project, a large external capacitor, C_{load} in figure 6, is used for stabilising the system at the cost of additional settling time. When an external capacitor is used for designing a stable LDO, the minimum value of capacitance, C_{load} and minumum value of its equivalent series resistance (ESR), R_{esr} should be specified[**ldo_ti_stability**]. C_{load} determines the dominant pole of the LDO and R_{esr} in series with C_{load} introduces a left half plane zero below unity gain frequency(UGF) of LDO in order to cancel out the non-dominant pole below UGF, producing a stable LDO system.

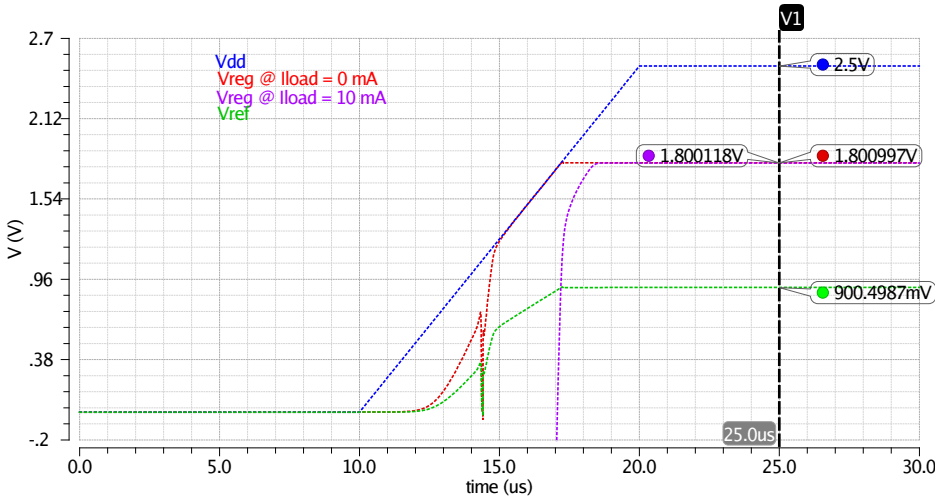


Figure 8: LDO transient simulation

Figure 8 is the transient simulations of the LDO which illustrates the generation of $Vreg$ for both high load and no load condition. This waveforms show that once the Vdd reaches high enough to create proper biasing, the regulated voltage of 1.8 V is produced and remains constant henceforth.

Figure 9 the gain open loop gain and phase margin of LDO without (upper plot) and with (lower plot) compensation. Though the stability analysis plots shown above is for typical corner of the devices, the values of R_{esr} and C_{load} are chosen for PM of at least 45°for the worst case i.e. slow corner and maximum load condition.

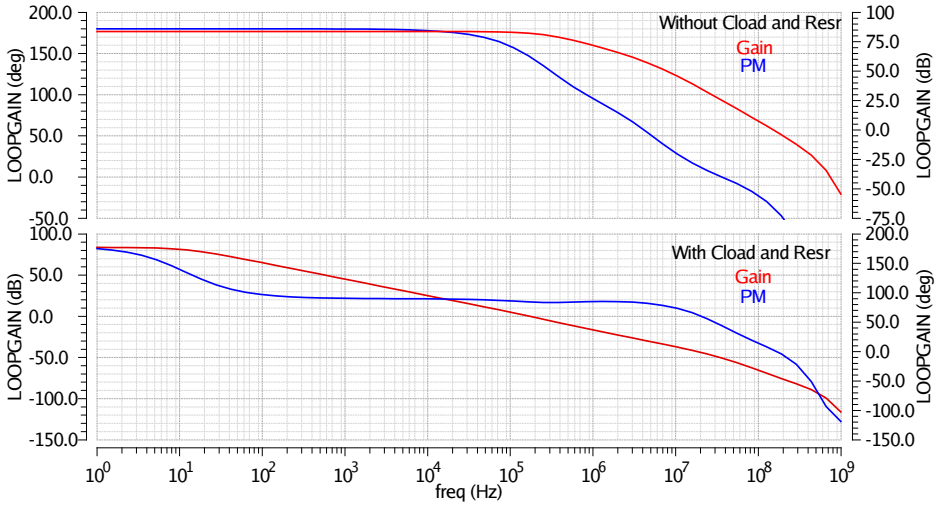


Figure 9: LDO stability before and after compensation

Table 3: LDO parameter and performance

$(Wp/Lp)_{pass}$	240um/280nm
Input supply voltage	2.2 V
Regulated output voltage	1.8 V
I_{load} max.	10 mA
C_{load} min.	> 0.6 µF
R_{esr} min.	> 0.8 Ω
PM	84°(typical)

Reference and biasing circuit design follows next.

4 Reference and biasing

Reference and biasing circuit is important part of any analog circuit. It is required to bias the designed circuitry with proper voltages and currents for operating all the devices in the intended region. For reliable and consistent performance of the system, the references and biases should be independent of supply voltage and temperature variations. Moreover with the trend of shrinking device sizes, mismatch and process parameters variations have been so pronounced that these factors affect the operation of the devices. So for the todays' devices, it is necessary to design reference and biasing independent of PVT variations.

There are different methods of generating reference voltages and bias currents discussed in literatures. Basically, supply independent current source is generated first and then this current is passed through a resistor to get a reference voltages. Some ways of creating supply insensitive current sources are threshold voltage referenced, diode (V_{BE} in BJT) referenced thermal voltage referenced current sources [**gray_2009**]. However, these current sources are not temperature independent. Threshold voltage of MOS and forward voltage of diode or V_{BE} have a negative temperature coefficient TC and hence they produce a CTAT (complementary to absolute temperature) current. On the other hand, the thermal voltage(V_T) has positive TC and hence it produce a PTAT (proportional to absolute temperature) current. So these techniques, though being insensitive to supply variations, still cannot be used for accurate reference voltage generation because of temperature dependence. So bandgap reference (BGR) design is used to generate the required reference voltage for the LDO in this design which has significantly less PVT variations than the last three methods.

BGR design involves summing up two voltages of which one is PTAT and the other is CTAT, both having equal and opposite TCs. The equal and opposite TCs cancels out leaving the resultant voltage with a zero TC. Figure 10 is the CMOS implementation of reference and biasing circuit for this project which includes startup circuit, BGR circuit and biasing circuit.

PTAT current is first generated using thermal voltage referenced current source using PNP transistor as diodes, resistor and a op-amp controlled current mirror [**razavi_2001**]. The current is $I = V_T ln(n)/R_1$,

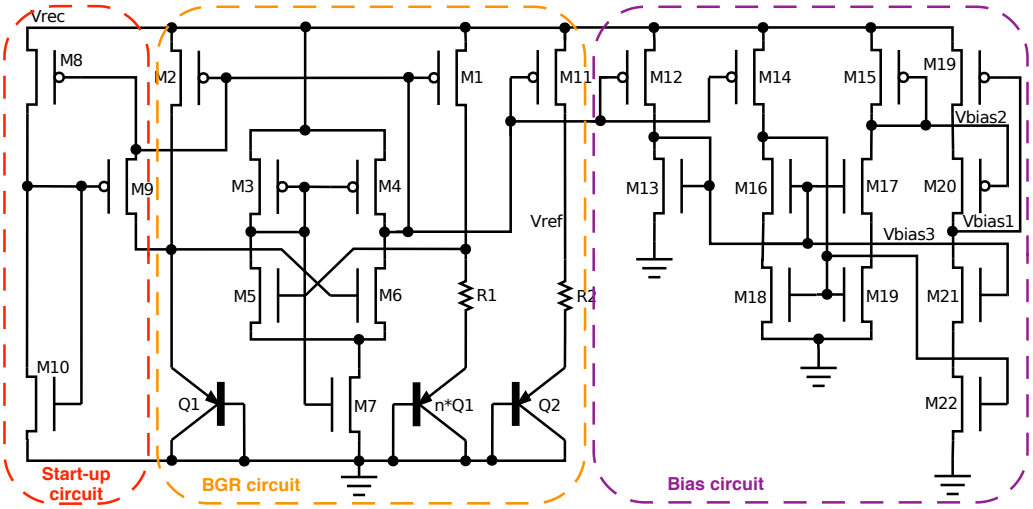


Figure 10: BGR and bias generation circuit

where $V_T = kT/q$ is thermal voltage with positive TC and n is number of parallel PNP transistors. This current is passed through a resistor, R_2 to create a PTAT voltage which is in series with a diode realised with a parasitic PNP transistor. The value of R_2 is so chosen such that the positive TC of PTAT voltage across it is equal to negative TC of V_{BE}. The temperature independent reference voltage is then given as $V_{ref} = V_{BE} + \alpha V_T ln(n)$, where $\alpha = R_2/R_1$ is equal to $\Delta V_{BE}/\Delta T$. Similarly the folded cascode operational transconductance amplifier (OTA) working as an error amplifier in LDO requires additional bias voltages which are produced as shown. Wide swing current mirror topology is used here for bias voltage generation.

In case of the supply independent and self biased circuit, there may be start-up issue. If all the transistors carry zero current, they may indefinitely remain off even when the supply is turned on. Therefore start-up circuit is added in order to ensure that the devices are turn on as supply voltage is provided. Once the circuit is fully operational, the start-up circuit is off and does not effect the normal operation of BGR circuit.

Figure 11, 12 and 13 illustrates temperature, DC and transient simulation of the BGR circuit respectively for slow(ss), fast(ff) and typical(tt) corners. The plots shows that V_{ref} is fairly independent with PVT variations. Similarly, I_{bias} varaitons used for generating the bias

voltages remains within condiderable range. Table 4 summarizes the performances of the BGR design.

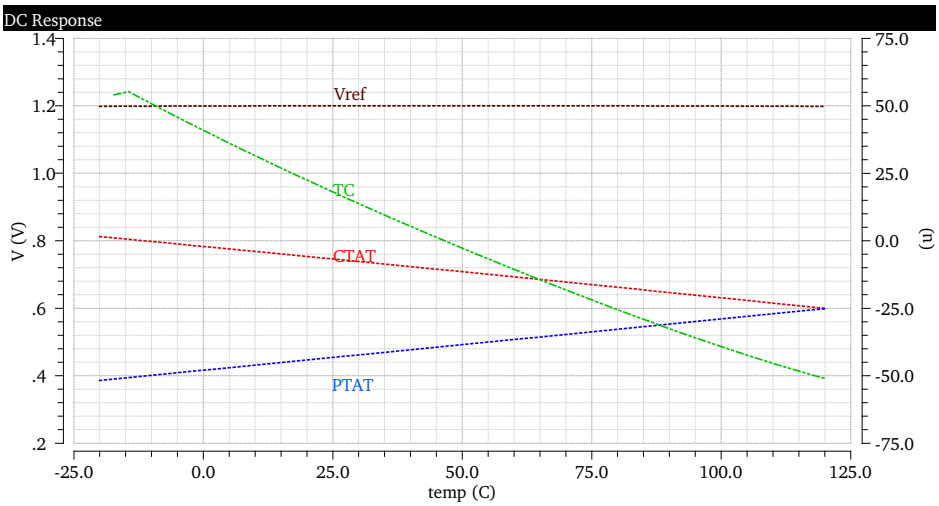


Figure 11: BGR over temperature varitaion

Table 4: BGR parameter and performance

V_{ref}	1.201.1 V @slow corner
	1.201.4 V @fast corner
	1.200.1 V @typical corner
TC @27°C	16.4 µV/°C
I_{bias}	8.95 µA @slow corner
	11.37 µA @fast corner
	10.04 µA @typical corner

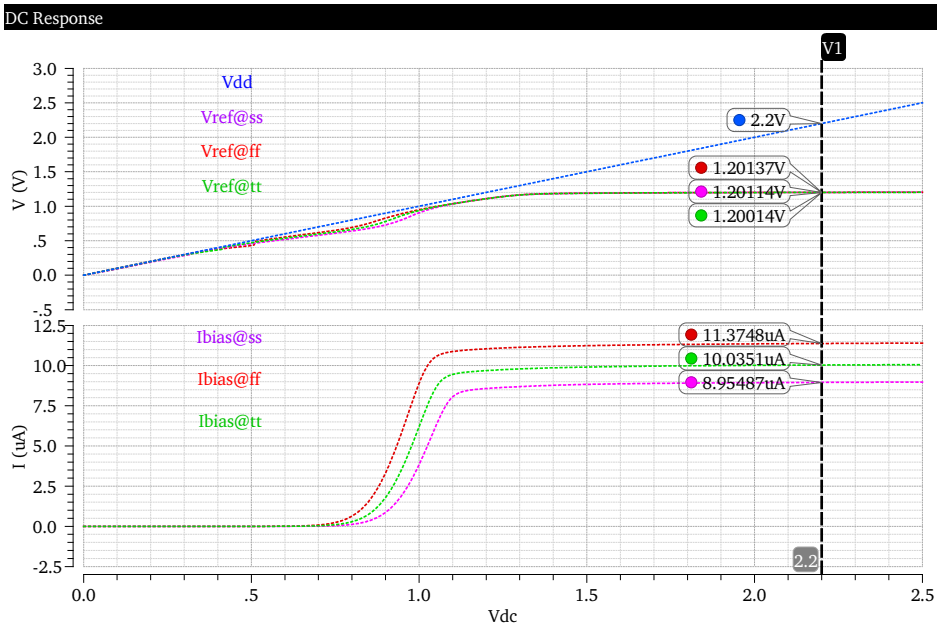


Figure 12: BGR DC performance

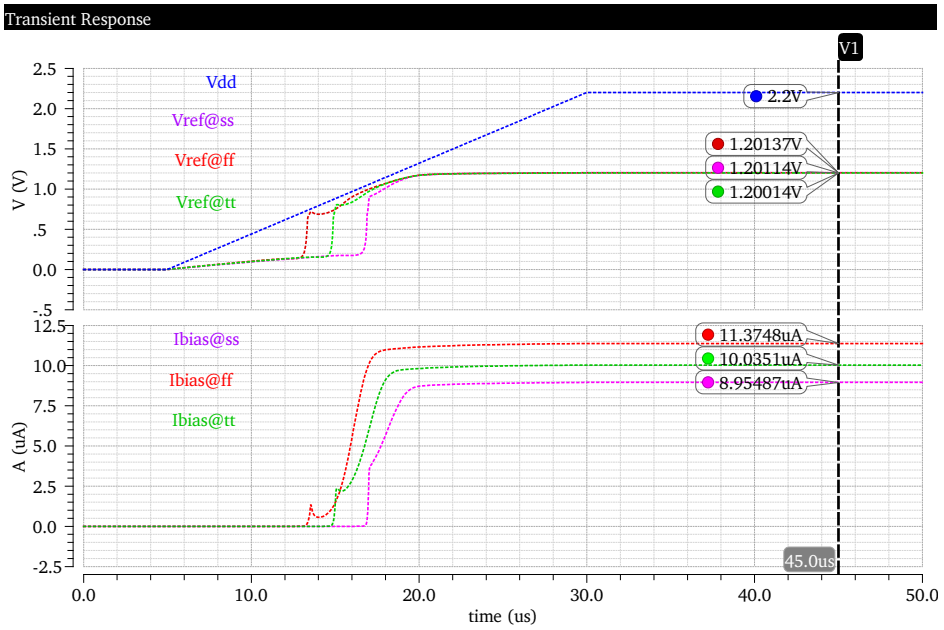


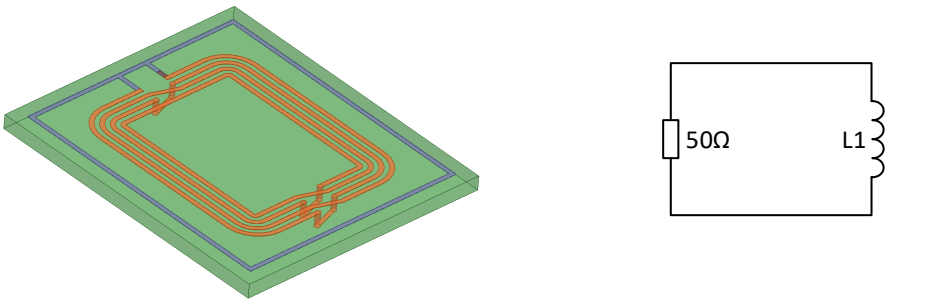
Figure 13: BGR transient performance

5 Antenna Design

All the components discussed above are part of any power management system. However, it is a pair of antennas which created inductive links for transferring power wirelessly and hence it is the actual physical component which makes wireless power transfer possible.

As already stated inductive coupling means coupling one coil with other, through magnetic field created in the first coil which induces the voltage in the second one. This is exactly the phenomenon for creating wireless power transfer link. In this project, the antenna dimensions are provided by Nordic Semiconductor which is one of their design already used in some application. Since having similar shape and size of antennas is important in gaining more transfer efficiency, the same antenna type is used as both primary and secondary coils.

For purpose of this work, with provided dimensions of the antenna, it is first modelled in HFSS as shown in figure 14a. More accurately, a planar antenna on a PCB can be modelled as in figure 15 which includes parasitic: Rp, series Dc resistance of wire and Cp, inter-winding self capacitance. These parasitic values minimise quality factor and self resonance frequency of the antenna. In the discussion ahead, these will not be explicitly mentioned because the parameter extraction will include these factors too. To realise a real antenna, physical parameters of materials used for making printed antenna on a PCB are also given for the model. After completing model, frequency sweep is done for extracting S parameter of the antenna which was eventually used to estimate self inductance of the modelled coil. The performance estimation of single antenna here and couple system later is based on formulas in [**ant_SZ_formula**]. In order to check and compare the estimated inductance value from the model, two different mathematical approximation methods described in [**ant_inductance_calculation**] were used. All the values of inductance of the antenna estimated from different method is listed in table 5. The table shows that the modelled value is less than mathematically approximated values. This difference can be explained with two things. Firstly, mathematical calculation assumed that the antenna is spiral and rectangular with sharp edge but the model has rounded edge. Secondly, during modelling besides dimensions of the coils, physical parameters of coil materials are also used but these are not considered for mathematical calculation.



(a) HFSS antenna model (b) Equivalent schematic

Figure 14: Antenna model

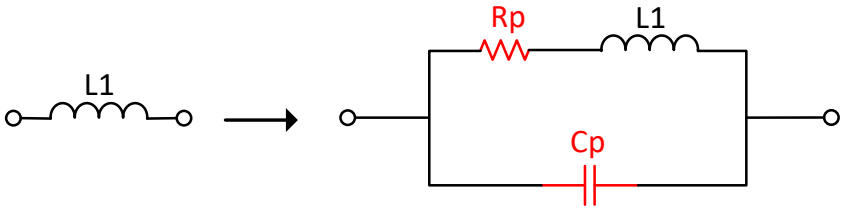
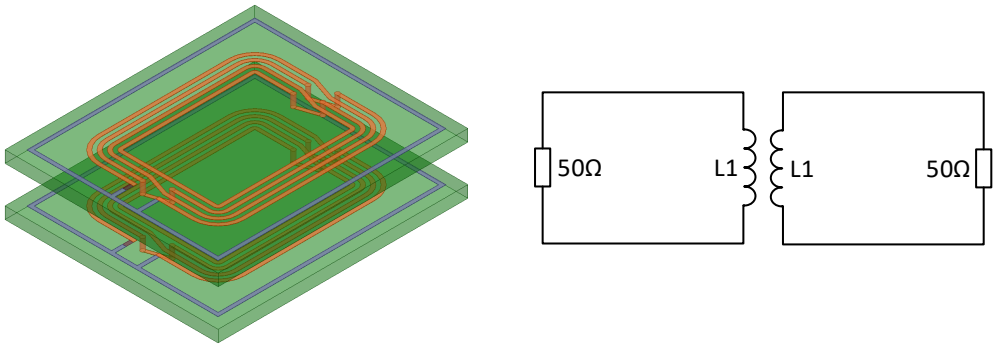


Figure 15: Real antenna model schematic

Table 5: Self inductance estimates comparision

HFSS model extraction	448 nH
Modified Wheeler Formula [**ant_inductance_calculation**]	644 nH

The next step is to observe coupling of two antenna for varying distance of field interaction. Two coils, primary and secondary are aligned together separated by some distance as shown in 16. The same procedure as used for single coil above, is used to extract self inductance of each coil, $L1$ and $L2$, mutual inductance of two coils, $L12$, coupling coefficient between the coils, k and quality factor, Q. The extracted values for coil separation of 1mm, 5mm and 10mm are listed in table 6. $L1$ and $L2$ are same as in table 5 as it is the same coil used as primary and secondary. Similarly $L12$ and k are both decreasing with distance as expected.



(a) HFSS coupling model (b) Equivalent schematic

Figure 16: Antenna coupling model

Table 6: Coupling parameters for varying coils distance

Parameter	1 mm	5 mm	10 mm	mm
L1	-	-	-	nH
L2	-	-	-	nH
L12	-	-	-	nH
k	-	-	-	-
Q	-	-	-	-

The power transfer efficiency of the physical link created by coupled coils is very important. [CITE] states that efficiency depends k of coupling system and Q of coil and hence high k and high Q is always desirable and obviously coil optimisation is the most important part of coupling system design. [**ant_optimal_resonance**] and [**ant_PSC_geometry**]

discusses some techniques to optimise transfer efficiency of inductive link: [**ant_optimal_resonance**] about matching the load for better resonance whereas [**ant_PSC_geometry**] about designing optimal coil geometry for higher Q. The former one compares the efficiency of general inductive coupling and conventional resonant coupling and their limitation in achieving higher efficiency. This eventually proposes optimal resonant load transformation which has better immunity to poor coupling and load variation. Likewise, the later one describes step by step iterative process of designing an antenna with optimal geometry for the given design constraints.

In this project, conventional resonance coupling as in [CITE] is implemented to tune both primary and secondary to the power career frequency. This method makes the bandwidth narrower but increase Q at operating frequcncy, making gain maximum at this desired frequency.

For the purpose of making a resonant inductive link, the S parameter of coupled antenna system in HFSS is exported to ADS in order to design matching networks using capacitors only. Impedance of primary antenna is matched to 50 Ω source resistance and impedance of secondary is matched to load impedance (50 Ω load or input impedance chip(?)) as shown in 17. $Cp1$ and $Cp2$ together with $L1$ created parallel resonant circuit on the primary side and $Cs1$ together with $L2$ creates the secondary resonant circuit at 13.56 MHz, a pair of Lc tanke circuit si thus made tuned at same frequency. Resonant coupling system with 5 mm separation is taken as a typical example. The losses at both the terminals for this case just around our operating frequency are as shown in figure 18. These plots show that power losses at both the ports have been reduced by at least an order of magnitude.

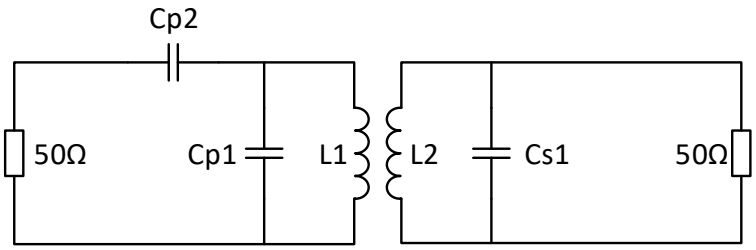


Figure 17: Resonant coupled inductive link

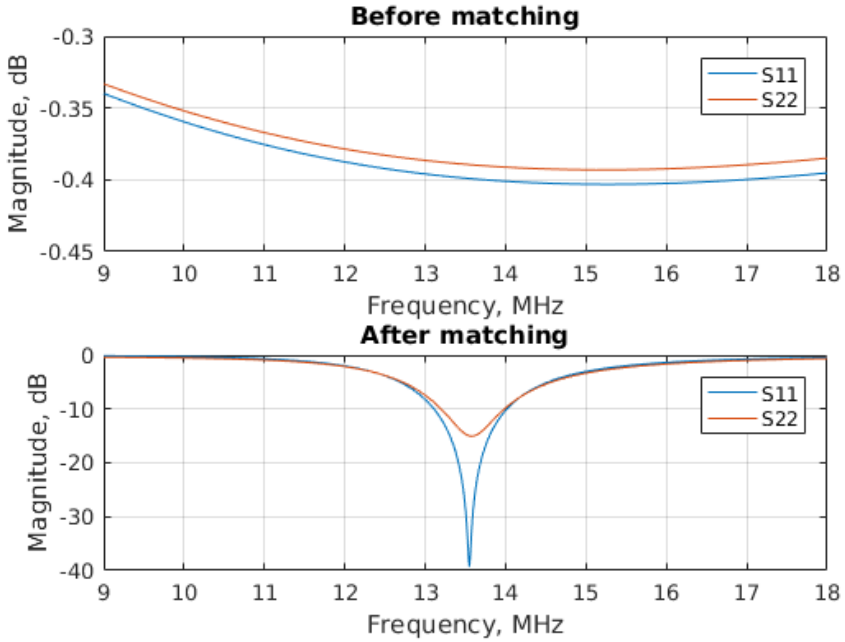


Figure 18: Power loss before and after matching

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Acronyms

BGR bandgap reference

CMOS complementary metal-oxide-semiconductor

CTAT complementary to absolute temperature

DC direct current

ESR equivalent series resistance

ICMR input common mode range

LDO linear dropout

MOS metal-oxide-semiconductor

nMOS n-channel MOS

OTA operational transconductance amplifier

PCB printed circuit board

PCE power conversion efficiency

PM phase margin

pMOS p-channel MOS

PTAT proportional to absolute temperature

PVT process voltage temperature

SMPS switch mode power supply

TC temperature coefficient

UGF unity gain frequency

VCE voltage conversion efficiency

Vp peak voltage

Vpp peak to peak voltage

Vtn thresold voltage of n-channel MOS

Vtp thresold voltage of p-channel MOS