Integrated electronic system for implantable sensory NFC tag

Ali Zaher, Joar Saersten, Thanh Trung Nguyen and Philipp Häfliger
Department of Informatics, Oslo University
P.o.Box 1080, Blindern NO-0316 Oslo, Norway
Email: alizah@ifi.uio.no

***Abstract*—We have designed the complete electronic system for an implanted sensory NFC-A tag (type 1) that monitors a physiological parameter, e.g. blood glucose, dehydration, bladder pressure, to name some of the target applications that we pursue. The tag is meant to be implanted under the skin and is powered by an NFC reader held close to it, such as a smart phone or a smart watch. The electronic system consists of a sensor front-end, ADC, NFC-A transceiver and NFC power harvester. In its present status, the physical layer of the communication and the power harvester have been implemented on one ASIC, and the sensor front-end and ADC on another, while the digital circuits realizing the higher level NFC protocol have been implemented on an FPGA. Simulations and a few preliminary test results are presented in this paper. The ultimate goal after thorough testing of this first prototype is to integrate all of these modules on a single ASIC.**

***Index Terms*—NFC, sensor, implant, tag, mixed-signal, smart phone, smart watch, invasive,**

I. INTRODUCTION

In recent years, smart phones are becoming more and more abundant and available for cheaper prices in a wider segment of the global population. These phones are coming equipped with different communication facilities like 3G, Wifi, bluetooth, IR and more lately Near Field Communication (NFC). At the same time, there is a global widespread of different diseases, diabetes among them as made clear by [1], that requires more attention from the health-care authorities. This includes monitoring, follow up and guidance that is given to each and every patient. Due to the huge cost attached to this from one side, and to the lack of flexibility from another side, many governments are looking into exploiting more the new technologies to introduce what is referred to as e-health [2]. Monitoring, if automated, is one of the major operations that can be done on the patient side, with the flexibility that suits the patient, and the results can be forwarded to the health station using internet connections available in any smart phone. More specifically, having an implant that monitors different physiological parameters and communicates the results with a nearby smart phone will offer great convenience and flexibility to many patients while trying at the same time not to threaten their integrity at any level.

While medical implants have been on the stage for quite some time, e.g. pacemaker, sensing implants are making a big advancement in the last decade. [3] classifies different implanted sensors and goes over the state of the art sensors published (blood pressure, oxygen saturation, heart beat, glucose, temp, ...). Different sensors are using different methods to communicate the sensed data at different frequencies, like 2.4GHz, 433MHz, 304MHz, 200MHz, and 13.56MHz. All of the mentioned sensors are battery-less and they are remotely powered by the reader which is of course designed along side with the sensors. [4] uses Infrared to transmit power and data to an implant that senses the temperature of the patient.

NFC has been used to run sensors in different scenarios and mostly for out-viva applications [5]. In this case, the system is built from discrete components bought from different manufacturers. [6] is one of the few which builds a complete system using NFC to run an implantable continuous glucose monitoring system. In addition to the implant itself, they design also the reader which is an extra device the patients needs to carry all the time. Our approach on the contrary is based on the idea that the patient should not carry extra devices only used for the sensor. Instead, the patient should be able to use a smart phone, or a smart watch as a reader.

In this paper, we are presenting the NFC communication and control system as well as the control for the attached sensor. Section II gives a short introduction to NFC. Section III goes over the electronic design in details. Section IV describes how the design has been implemented before section V presents the simulation results. We conclude finally in section VI.

II. NFC BACKGROUND

NFC technology is partly based on ISO/IEC 14443 standard for proximity cards. As the name suggests, it is known to be a touch technology since it works with inductive coupling at 13.56MHz, and as a consequence the range is limited to few centimeters. NFC technology is an umbrella for many different standards and protocols which vary based on complexity, security and data throughput. Tags, which are the tockens the readers read, also come in different flavours and capabilities to match different NFC protocols. Table I classifies different tags and protocols used in NFC.

A typical design of a tag contains a power unit to power up the electronics from the magnetic field, digital and analog blocks that together secure a successful communication between the tag and the reader, and finally a non volatile memory, byte addressed, that holds a unique ID and the data whenever the tag is not powered up. Data is exchanged

Tag	Standard	Android Protocol	Memory	Bit rate
Type 1	ISO 14443A	NFC-A	96B-2KB	106Kb/s
Type 2	ISO 14443A	NFC-A	48B-2KB	106Kb/s
Type 3	JIS 6319-4	NFC-F	2KB-1MB	212Kb/s
Type 4	ISO 14443A-B	NFC-A,B	32KB	106Kb/s-424Kb/s
Mifare	ISO 14443A-B	NFC-A,B	1KB-8KB	106Kb/s-424Kb/s
LR family	ISO 15693	NFC-V	8KB	26Kb/s-53Kb/s

TABLE I
DIFFERENT TAG TYPES MAPPED TO THEIR CHARACTERISTICS

between the reader and the tag in well defined packets and in a synchronized manner [7]. These packets usually start with a command with the type of action the tag should do, then an address and data in case of READ or WRITE commands, the tag ID comes next and finally a 2 bytes CRC. Table II shows a summary of the commands used by tag type 1. Though the protocol reserves 7 bits for defining a command, only few commands are implemented in the tag specifications [8]. This opens the door for implementing custom made commands needed for the monitoring process.

Command	Hex	Comments
REQA	26_h	Request command, type A
WUPA	52_h	Wake-up, type A
RID	78_h	Read ID of the tag
RALL	00_h	Read all the bytes
READ	01_h	Read a single byte
WRITE-E	53_h	Write with erase a single byte
WRITE-NE	$1A_h$	Write without erase a single byte

TABLE II
COMMANDS USED BY TAG TYPE 1 IN CASE OF STATIC MEMORY MODEL.

III. Circuit Design

We started from tag type 1 design as defined in [8]. The choice has been based on the complexity of the tag and the requirements we have from the sensor design. The tag design, as shown in fig 1 can be divided into the analog part and the digital part. In addition to that we have the RF front end which includes the antenna and the tuning capacitor, power supply unit and the sensor(s) interface. Notice the lack of a non-volatile memory that is usually present in any tag design. This is due to the fact that, at the current stage of the design, the sensor will run only in the presence of the reader which delivers the power needed. In what follows, we are going to present the different sub-blocks.

A. Power supply unit

It is made of the rectifier, fig 2(a), that generates a rectified output (VREC) from the signal captured across the antenna. VREC is then forwarded to the 3 different regulators to generate 3 adjustable isolated power levels; VDD for the analog parts (VDD-A), for the digital parts (VDD-D), and for the sensor(s) (VDD-S).

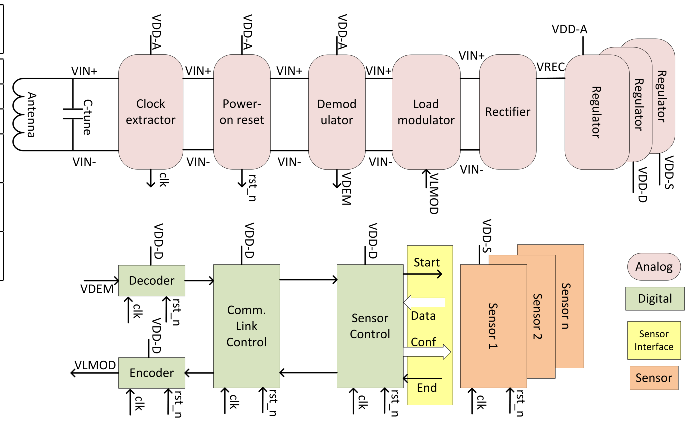
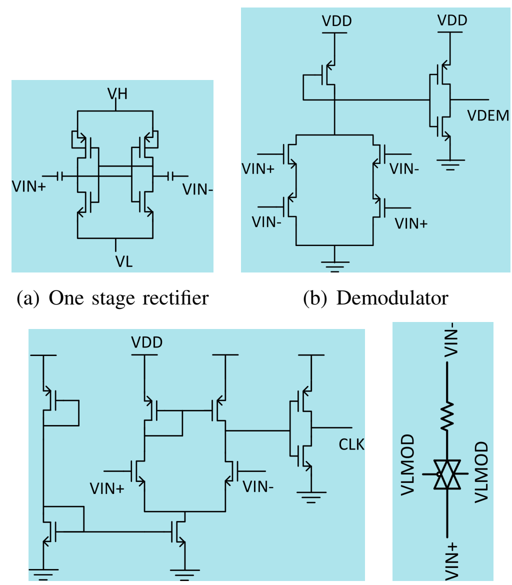


Fig. 1. The system from the antenna terminals to the sensor interface



(a) One stage rectifier (b) Demodulator

(c) clock extractor (d) Load Modulator

Fig. 2. Power supply and analog parts. The demodulator for ASK works with above 30% modulation index, while the clock extractor generates the clock as long as the magnetic filed is present. The rectifier is made of 3 cascaded stages.

B. Analog parts

Here we can find the 4 basic elements in the communication link; the demodulator, the load-modulator, power-on reset, and the clock extractor.

1) The demodulator: it translates the signal that appears across the antenna into 0s and 1s by interpreting the absence of modulation as a 1, and the presence of the modulation as a 0. The output, VDEM as it appears in fig 2(b), represents the sequence of the patterns X, Y and Z as defined in [7]. It is forwarded afterwards to the decoder in the digital part to decode the commands and data sent from the reader to the sensor.

2) The load modulator: It changes the load across the antenna to generate the 10% modulation of the reflected signal from the tag to the reader. This is done as shown

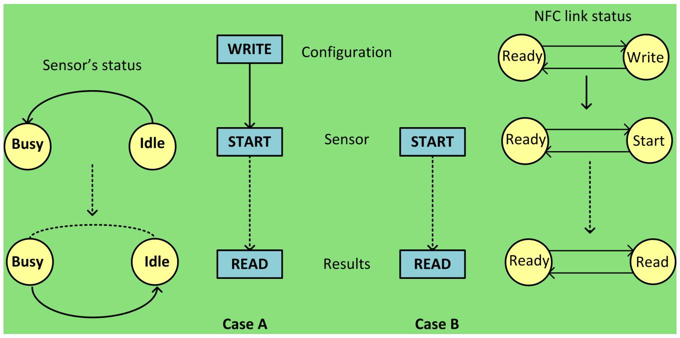


Fig. 3. The sensor and NFC link's status during a typical sequence of operation

in fig 2(d) to generate the patterns D, E and F as defined in [7]. The signal VLMOD controlling the transmission gate is generated by the encoder in the digital part based on the data sent from the sensor to the reader.

3) Power-on reset: this is a sub-block that is used to generate the reset signal needed by the digital part and the sensors. It generates a reset pulse that lasts for 2us directly after the regulator output stabilizes.

4) The clock extractor: fig 2(c) shows a simple 13.56 MHz clock extractor that is needed to run the digital part and the sensor. The clock is available only during the period where the modulation is below 30%, so this creates a challenge for the digital part to decode correctly the transmitted signal from the reader without the need of an extra oscillator on chip. When there is no modulation from the reader to the sensor, the clock is available for the sensor to run as required.

C. Digital parts

This is where we find the decoder, encoder, the control of the communication link between the sensor and the reader and the control of the sensor.

1) The decoder: it receives VDEM signal from the demodulator and then translates it into the bits that constitute the down-link frame sent.

2) The encoder: it receives the bits already packed in the up-link frame ready to be sent. It uses Manchester coding as defined in [7] to generate signal VLMOD controlling the load modulator.

3) Communication link control: the link between the reader and the sensor is dead when there is no magnetic field. Once the magnetic field is high enough to turn on the electronics, the link goes directly into the idle state, and waits for the REQA command. Once this command is received it goes into the ready state, where it can exchange data between the reader and the sensor. For every command that is received after, the link executes the command, and then goes back to the ready state.

4) Sensor control: The sensor goes into idle state waiting for the start command (custom made) to start sensing. Once finished, it tells the communication link control that the sensing result is ready to be read. It goes back to the idle state. Each sensor is memory mapped into 3 different addresses: 15 bits to hold the output of the sensor, 1 bit to hold the status of the sensor; busy or idle, and finally up to 8 bits to hold the configuration for the sensor. There can be two scenarios for running the sensor as it appears in fig 3. Case A shows when the reader configures the sensor first before starting it. It will later retrieve the result by a read command. In case B, the reader will run the sensor with the previous configuration, it can start the sensor directly without configuring it first.

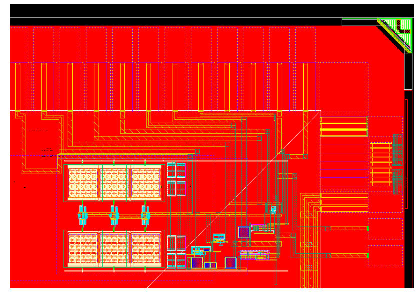


Fig. 4. Layout for the analog parts in CMOS 90nm

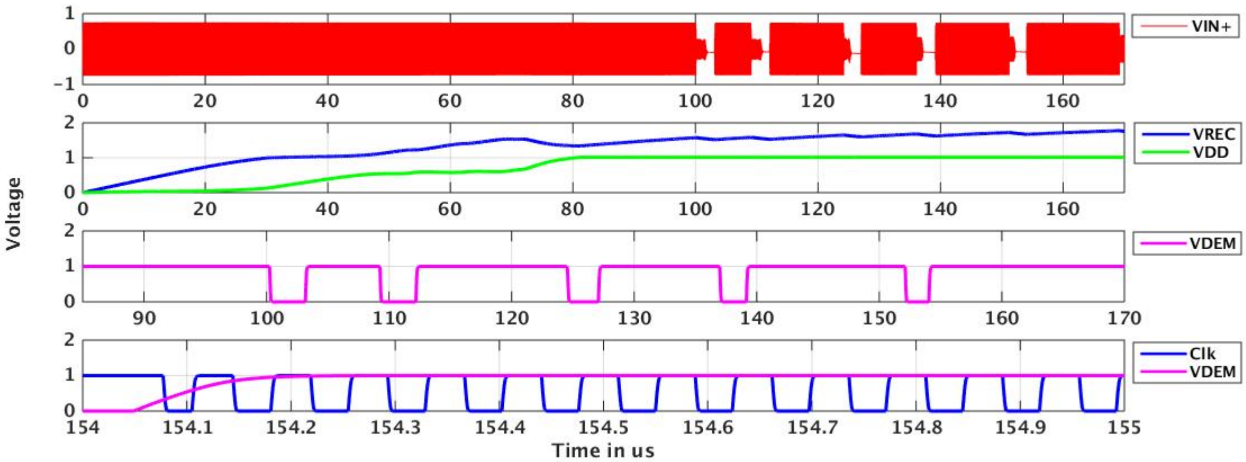
IV. Implementation

The Analog parts are design in TSMC CMOS 90nm process. The digital parts are designed using VHDL and synthesized on a Xilinx Spartan6 FPGA. Fig 4 shows the layout where it is clear that the rectifier on the left is the part that occupies most space. The estimated size of the tag is $0.115mm^2$ on a die of size $3.31mm^2$. The sensor frontend [9] has been fabricated on a different ASIC previously and will be attached to the FPGA during testing.

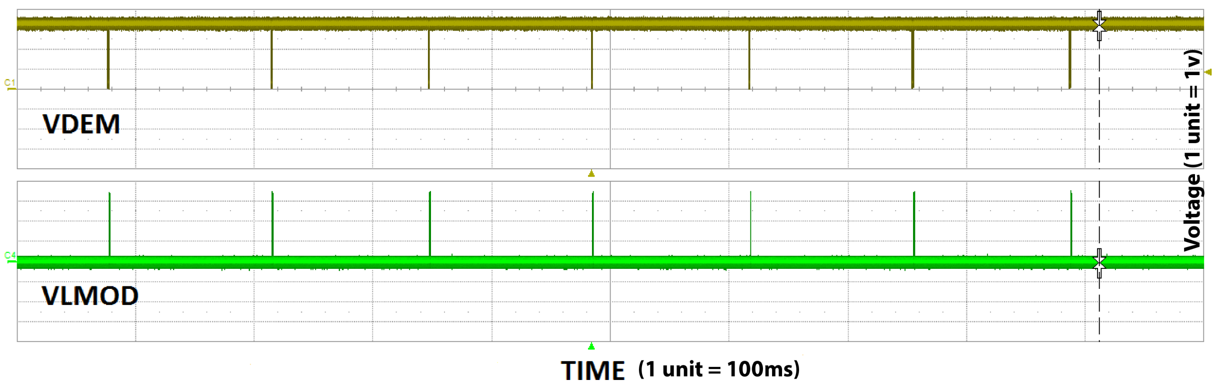
V. Simulations and Results

We have simulated the analog parts in Cadence tools. The antenna has been replaced with a 6.56μH inductor, and a 12pF capacitor connected across the terminals representing C-tune. The 3 stages rectifier generates enough current to drive the regulator output at 1V while clamping the voltage across the antenna at $\pm$800mv to protect against higher voltages as shown in fig 5(a). Both VREC and VDD are connected to 8.2nF capacitors, and VDD is connected to an extra load consuming 100μA. VREC goes towards 2v while VDD reaches 1v and stays stable there after 80us from the start of oscillations at the antenna. Data transmission starts after 100us, where VDEM changes between 0v and 1v. Finally we show CLK and VDEM towards the last demodulation at 154us. The extracted clock has a frequency of 13.56MHz when stable with an error of 59ppm which satisfies the timing requirements for synchronized transmission defined in [7] as $\pm$6 clock cycles in 70996 clock cycles period. The clock disappears when the signal is modulated from the reader, and comes back within 1000ppm in 166ns (less than 3 clock cycles) after the modulation is finished. The current consumption of all the analog parts has an rms value of 4.4μA.

We have newly received back the ASIC, and using an LG-800 smart phone, we are able to do an ASIC alive test, as



(a) Simulation



(b) Measurement

Fig. 5. a) Simulation of the analog parts under 170us. b) One of the early measurements showing uplink and donwlink.

shown in fig 5(b). VDEM and VLMOD are shown while interfacing to the FPGA that is running at 3.3v. The graph shows 1 second of the communication where the phone sends a RID command every 156ms, asking if the tag is still attached. The tag answers by sending its ID. Between these commands, the smart phone keeps powering up the tag and the sensor.

VI. Conclusion and Future work

We have presented the complete electronic system for an implanted sensory NFC-A tag (type 1). We demonstrated the way the system should work with a smart phone or watch. Simulations for the physical link has been presented as well as one of the early lab measurements on the real ASIC showing that the physical link is up and running. More work is waiting ahead. Measurements on the ASIC will be carried on to characterize the analog parts. The digital parts implemented on the FPGA will be tested against the NFC-A tag type 1 protocols. Specifically, custom made commands should be checked and analyzed. To manage to do that, an NFC app needs to be designed that can communicate with the tag and send these special commands. To close the loop, the sensor frontend in [9] will be connected to the FPGA so the app on the smart phone can access it via the tag. Once the system is stable, an ASIC containing all the modules will be implemented and tested.

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