Preliminary report on master project

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1 Introduction

This report is a brief overview of my master project on wireless power transfer through inductive coupling. It is the documentation of the schematic of complete design of the power receiving unit. It includes brief explanation about choices of design topologies and techniques. Figure 1 is the block diagram of the complete design including the test PCB and the test chip on it.

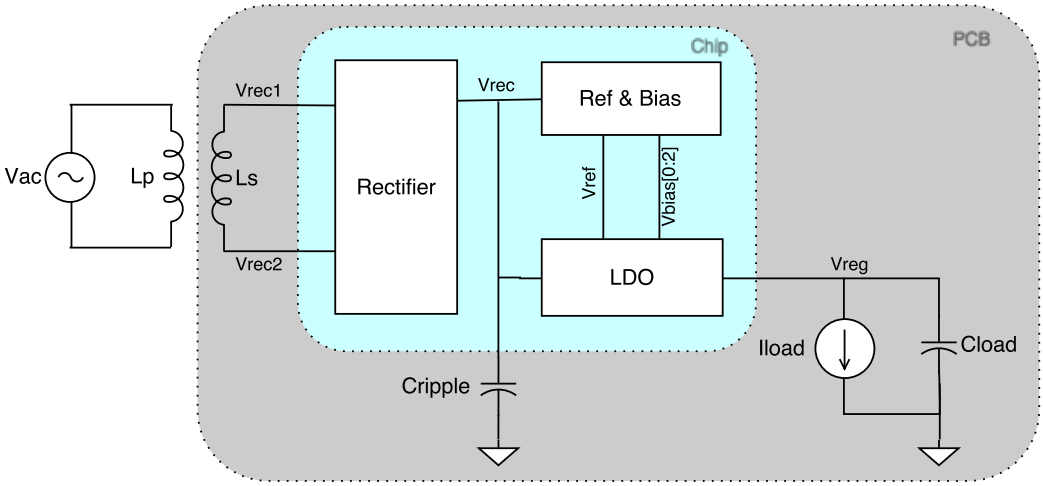


Figure 1: Block diagram of complete design

As shown in the block diagram above, the design includes antennas rectifier, LDO regulator and reference and biasing circuits. This report mainly discusses about the various design aspect of rectifier and LDO. The inductor is designed with the specifications provided by NORDIC. The biasing and reference circuit is designed solely for learning the design technique without much effort on the accuracy of the generated biases and references. So externally supplied bias and reference will

be the secondary option. The project is designed in tsmc90nm process. Table 1 lists the main specifications of this project.

Table 1: Project specifications

Technology	TSMC 90nm 9M-1P
Chip area	TBA mm^2
Input AC voltage	2.5 Vp
Operating frequency	13.56 MHz
Maximum load	10 mA
Output DC voltage	1.8 V

A brief discussion of rectifier design is followed next.

2 Rectifier

The most basic rectifier is conventional full wave bridge structure where the diodes are replaced by the diode connected MOS. devices in CMOS. technology. This topology though being simple to implement, has a major drawback. It requires at least twice the Vtn of a MOS device as there are two diode connected MOSes in the conduction path for each cycle of the input signal.

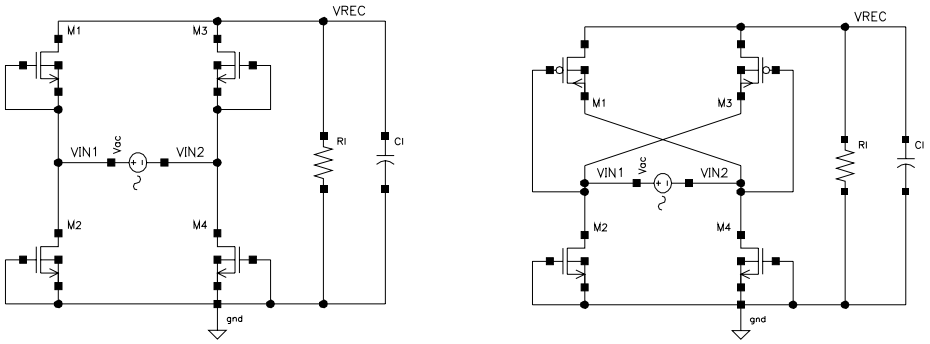
Gate cross coupled and fully gate cross coupled topologies are improvements over conventional full wave rectifier. In gate cross coupled rectifier, two diodes of conventional rectifier is replaced by two gate cross coupled MOSes working as switches where the voltage drop for every cycle is reduced to one threshold voltage. Similarly, in the fully gate cross coupled rectifier, all diodes are replaced by switches and hence the voltage drop is further reduced to twice the conduction drop only for every cycle. Even though this topology has least voltage drop, it suffers from the problem of reverse charge leakage because when the input ac amplitude is less than the output rectified voltage and the conducting pass devices are on simultaneously, current flows backward from output to input.

All the above discussed topology suffer from either large voltage drop or large power loss because of which their use are limited in low power and low voltage devices. The popular techniques for higher efficiency are using gate cross coupled rectifier along with passive or active circuitry for controlling other two pass devices. In passive rectifier, additional circuitry including bootstrap capacitor are used to reduce or eliminate threshold voltage one of which is discussed in this paper [1]. However, use of on-chip bootstrap capacitors limits it use where chip area and speed is of importance. On the other hand, in active rectifier, active circuitry is used control pass devices. The use of active circuitry increase both voltage conversion efficiency (VCE) and power conversion efficiency (PCE) because the pass devices are made to conduct in linear region and hence less conduction drop, and reverse current flow can be completely eliminated and hence less power loss. However active rectifier is not problem free either. The major issue is starting of the active circuit as there is no regulated supply at the start up.

2.1 Design

In this project, active rectifier is chosen, primarily for better VCE and PCE and secondarily to avoid the use large on chip capacitors. [2] and [3] have discussed same active rectifier topology with a slight difference in active circuitry. [2] has implemented comparator with compensating the delay of comparator's output falling whereas [3] has implemented comparator with compensating both the falling and the rising delay of comparator's output in expense of added circuit complexity and power consumption. [2] has been used here for its simple design.

Figure 2a, 2b and 3 is the CMOS implementation of conventional full wave bridge rectifier, gate cross coupled rectifier and proposed active rectifier in [2]. The problem with 2a and 2b has already been briefly mentioned above. Though 2b is significantly improvement over 2a , it is still not a favourable topology with respect to the design technology chosen. In the gate cross couple rectifier of 2b, the cross coupled pMOSes act as switches, so the only voltage drop across them is conduction drop due to channel resistance. However the other two nMOSes are diode connected, so they have at least Vtn drop across them which means $Vac \geq Vdc + Vtn$ for conduction.



(a) Conventional full wave bridge rectifier (b) Gate cross coupled full wave rectifier

Figure 2: Rectifier topologies: conventional and gate cross coupled

The proposed active circuit in 3 is improvement over 2b which eliminates Vtn drop required for conduction by replacing diode connected nMOS with devices controlled by active circuit as shown in figure 4. The active circuit is a four input comparator that turns on nMOSes fast when Vac > Vdc and turns off fast to avoid flow of current.

For the illustration of operation of comparator, consider the case when $Vin1 > Vin2$ i.e. $Vin1 > 0$ and $Vin2 < 0$. During this half cycle, comparator $D1$ output is low and turns off $Mn2$ and also, $Mp1$ is reversed biased and hence there is no path to flow current along $Mn2$ and $Mp1$. For simplicity, assume $Vac = Vin1 - Vin2$. When Vac reaches Vtp, $Mp3$ turns on which shorts $Vin1$ to $Vrec$. When $Vac > Vrec$, $D2$ output goes high, which turns on $Mn4$ and starts the conduction path for the first half cycle and starts charging Cl. When Vac reaches maximum, it starts to decrease and at $Vac < Vrec$, conduction stops as output of $D2$ is low and $Mn4$ is off. As Vac further decreases to below Vtp, $Mp3$ if off too. This way rectifier in 3 conducts during positive half cycle eliminating the Vtn drop seen in 2b. Now the only drop is the conduction drop due to channel resistance of two pass devices along the conduction path. This drop is much less because during conduction both the device are operating in the linear region with small resistance. The operation is similar for $Vin2 > Vin1$ where $Mn4$ and $Mp3$ are off and $Mn2$ and $Mp1$ conduct to charge Cl.

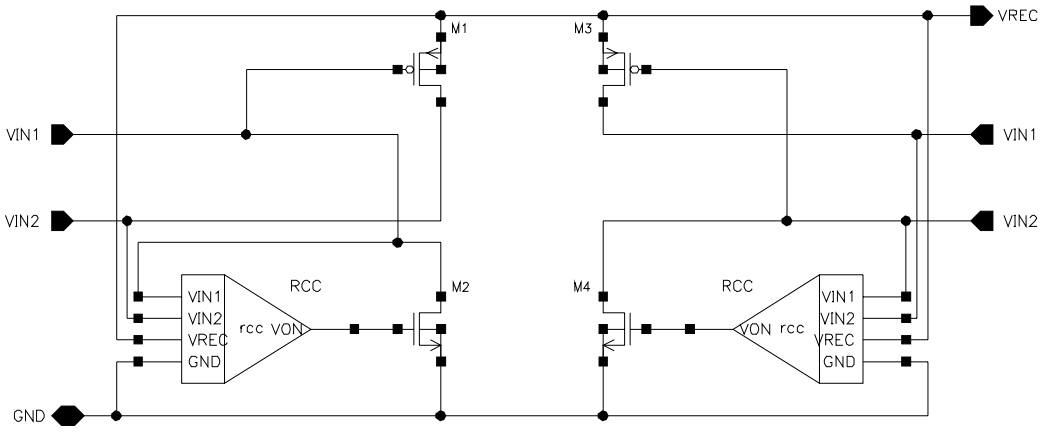


Figure 3: Gate cross coupled full wave active rectifer]

Figure 4 is the implementation of four input comparator $D2$ used in 3 as proposed in [2]. It is designed to self power and bias because no steady state supply is available at start up. $M1$, $M2$ and $M7$ monitors voltage across $Mn4$ i.e $Vin2 - Vgnd$ and $M3$, $M4$ and $M8$ monitors voltage across $Mp3$ ie $Vin1 - Vrec$. So when $Vin1 - Vrec > Vin2 - Vgnd$ which means $Vac > Vrec$, output of $D2$ is high and turns on $Mn4$ instantly. But when $Vac < Vrec$, the output of comparator is delayed to

fall which causes $Mn4$ to conduct in reverse direction leading to significant reduction in power delivered to load. $M9$ is introduced in order to overcome this problem which adds offset currents to increase Van and Vpn faster, causing the output to decrease faster and turns off $Mn4$ before $Vac < Vrec$. This reverse current control technique compensates the comparator delay and increases the power efficiency of the rectifier.

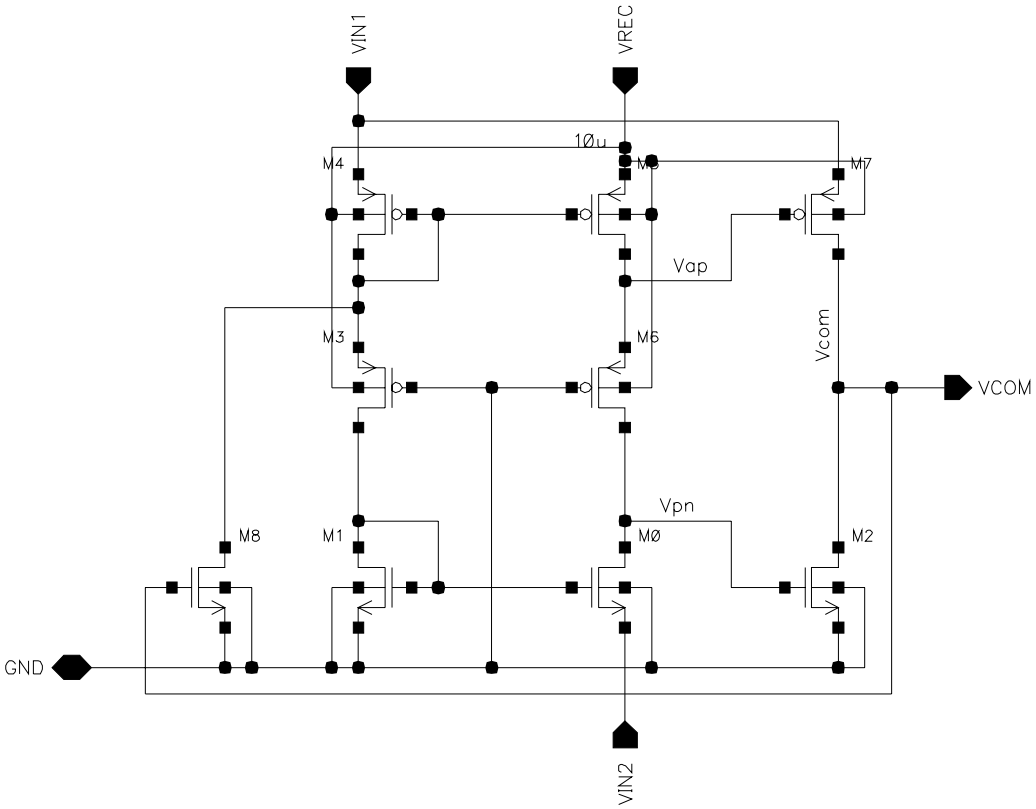


Figure 4: Comparator circuit, RCC

The design parameters for the rectifier is listed in table 2. The dimensions of the pass devices are first hand calculated by using square law current equation and devices parameters values given in the technology documents, and later optimised with simulation tool in order to make the rectifier to deliver the required current. Since nMOS does not have to have same device size as pMOS to deliver same current, optimal size ratio equation from [4] is used to find nMOS pass devices sizes. Thought maximum load for this work is 10 mA, It is always simulated with 1 mA extra load. This extra current is to account for the

fact that RCC is self powered and LDO which will follow this rectifier will be powered by $Vrec$. Similarly, the value of ripple rejection capacitor is chosen 100nF. This size of filter capacitor is calculated from capacitor current-voltage relationship with the assumption of keeping peak to peak ripple voltage below 5 mV to deliver 11 mA current.

Table 2: Rectifier design parameters

Wn/Ln, Wp/Lp	720um/280nm, 1.2mm/280nm
Rectifier area	TBA mm^2
Operating frequency	13.56 MHz
Input ac magnitude	2.5 Vp
Load current	11 mA
Ripple rejection capacitor	100 nF

2.2 Transient performance

Figure 5 is the test bench setup for simulation of the rectifier. Figure 6 show the simulation results showing voltages at the input ac and output rectified DC voltages and current through rectifying MOSes. These waveforms clearly follows the working principle discussed above. Two important observations can be made from plots. First, the rectified output $Vrec$ is 2.2 V for Vpp ac input of 2.5 V for driving which means the voltage loss has been significantly reduced and the loss of around 300 mV yields to the conduction loss due the channel resistance. Secondly, the reverse current from output to input has been effectively eliminated as there is only positive current flowing to the load when all conducting devices are on.

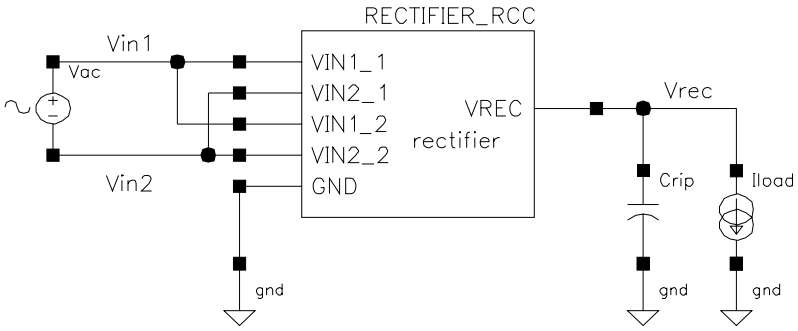


Figure 5: Testbench for rectifier

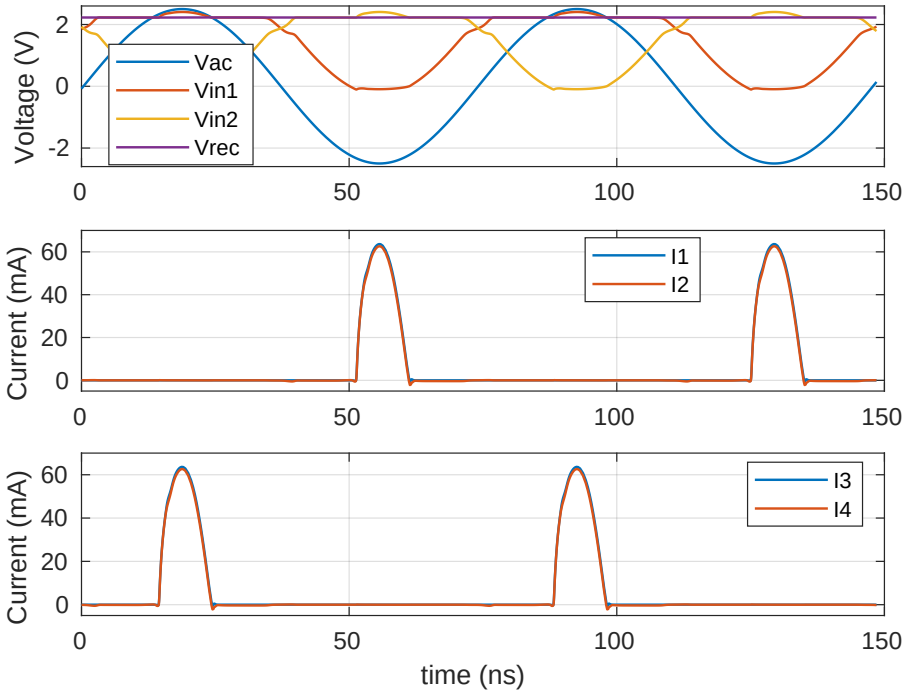


Figure 6: Voltage and current waveforms of the rectifier

Figure 7 presents both pre and post layout results of input voltages, $Vin1$ and $Vin2$ and output voltage, $Vrec$, for one cycle of ac input. The closer view of rectified output is shown in figure 8. The voltage drop of about 60 mV in layout result is accounted for the voltage drop due to the resistance of high current conduction path.

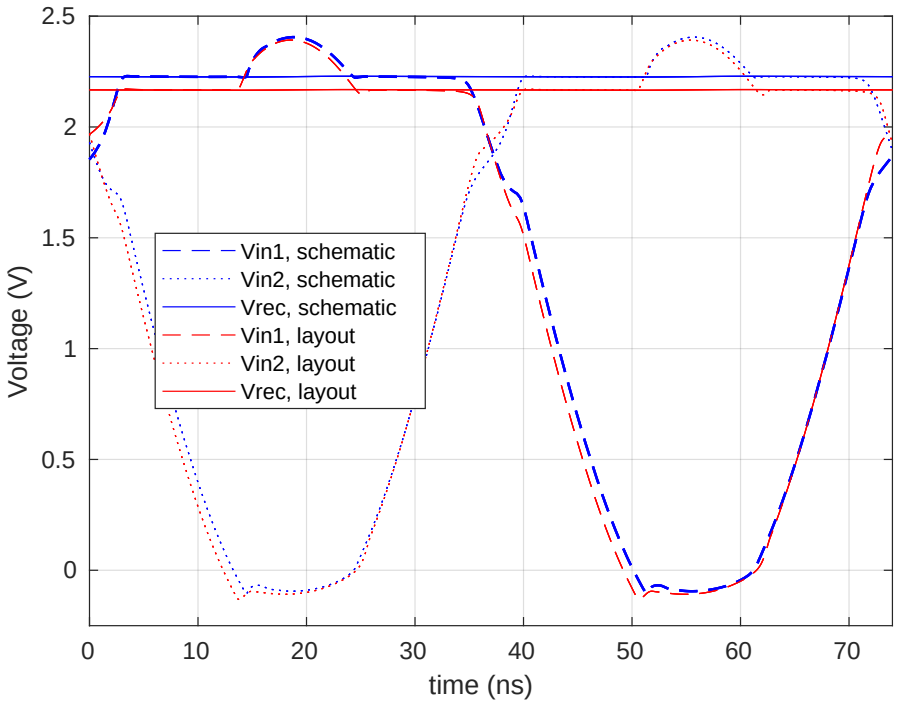


Figure 7: Voltages waveform for pre and post layout

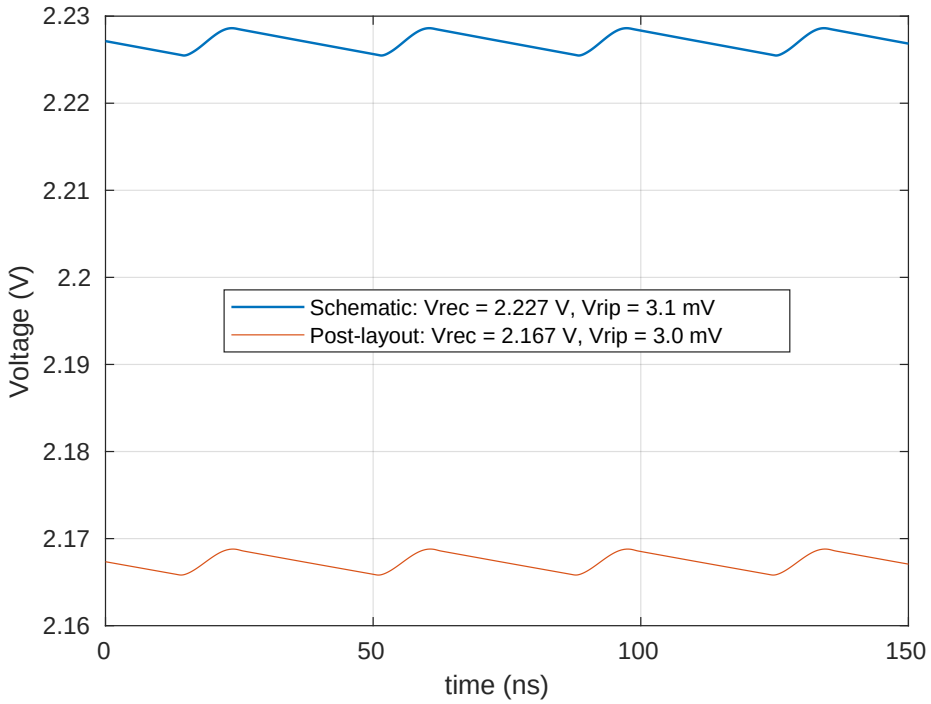


Figure 8: Rectified DC output for pre and post layout

2.3 DC performance

Similarly, figure 9 shows PCE, ratio of powered delivered to load to average power from the source and VCE, ratio of rectified DC, $Vrec$ to peak ac input, $|Vac|$ with respect to magnitude peak ac input signal. $|Vac|$ is gradually increased in peak magnitude in step of 50 mV and VCE and PCE is calculated for every step. The plot shows both PCE and VCE are very less for input ac amplitude less then 1.8 V. It can be explained by the fact that required bias current and gate drive voltage for RCC circuit are not achieved for smaller input. [INCLUDE POST LAYOUT RESULT TOO]

Table 3 comparatively summarises performance for pre and post layout result of the design. The layout design is attached in appendix. The layout is made symmetrical with four inputs, as seen in test bench figure 5, instead of two. This is done to make the current conducting path equal which result in equal drop in voltage when it reaches the rectifying MOSes. Simialarly the paths from the pad to the recitifier

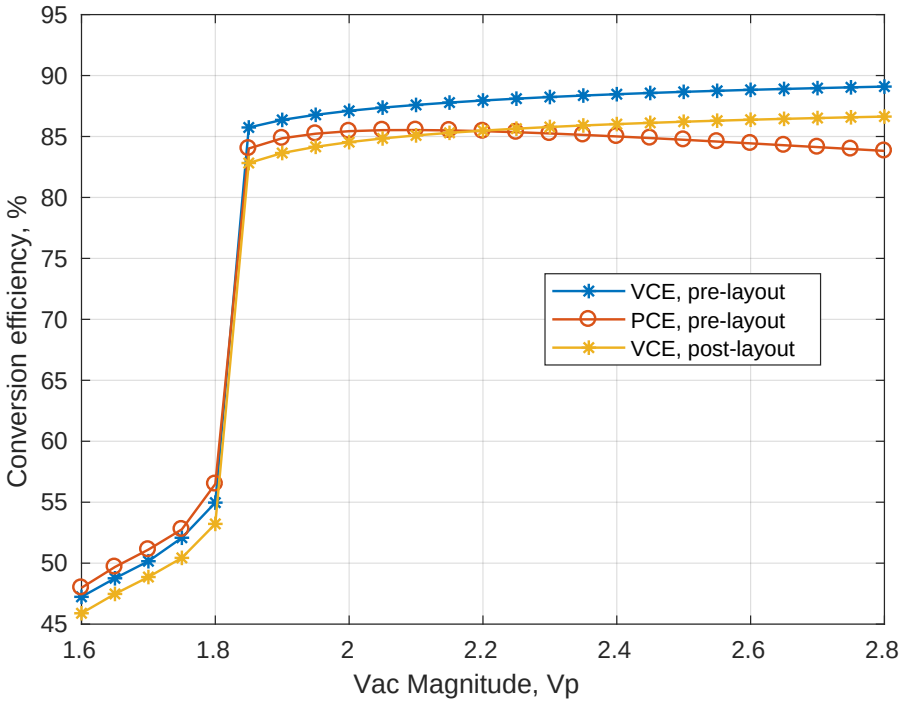


Figure 9: Voltage and power conversion efficiency

inputs are mask blocked for random metal fill to avoid inter layer coupling [WHY???]. The high current conduction routes are designed with wide parallel path of many higher level metal layers for reducing resistance in conduction path.

Table 3: Rectifier performance summary

	Schematic	**Post-layout**
Rectified DC	2.23 V	2.17 V
Ripple Vpp	3.1 mV	3 mV
Peak diode current	63.7 mA	-
PCE	84.5 %	-
VCE	88.6 %	86.2 %

3 LDO

Voltage regulator follows the rectifier designed above in order to regulated the rectified voltage to 1.8 V and deliver maximum load current of 10 mA. Since the output from the active rectifier is 2.2 V and the required regulated voltage is 1.8 V, charge pump or SMPS of boost type is irrelevant here. Buck SMPS could be an option for voltage regulation but LDO is preferred for it better performance in terms of noise and faster settling of regulated voltage. [5].

Figure 10 shows a circuit of typical LDO with pMOS as pass element. As shown in the figure, the components includes an error amplifier (EA), a pass device (Mpass), a feedback circuit (R1 and R2) and load (C_{out} and I_{load}). A more general and complete LDO circuit also includes circuitry for generation of reference voltage and bias current/voltage. In this project it will be discussed separately later. The working principle of LDO is that the error amplifier compares the scaled down regulated voltage, Vdiv with Vref and regulates the internal resistance of the pass transistor such that the error, V_{ref} - V_{div} is least or zero ideally.

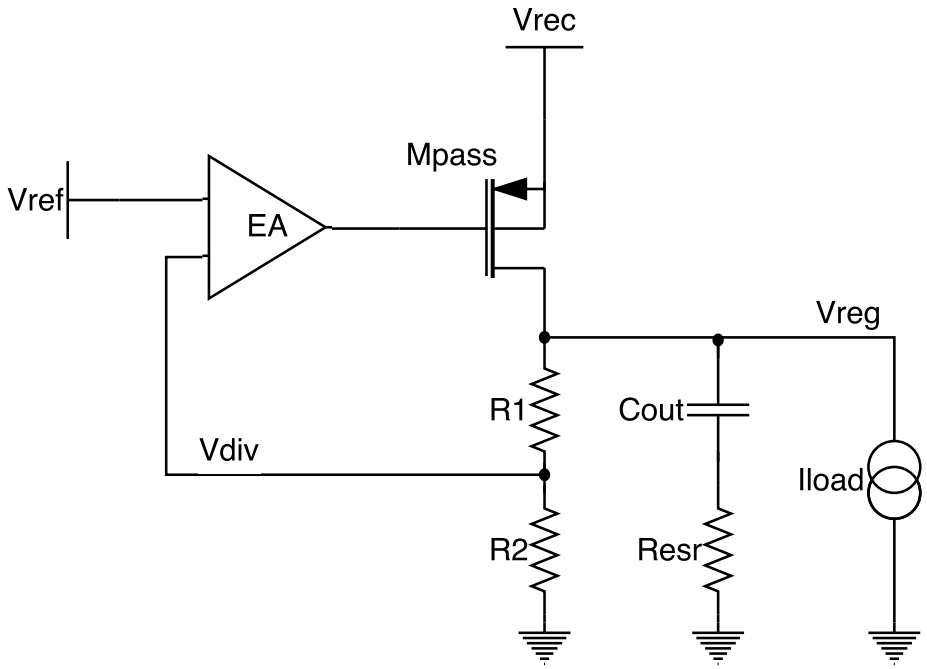


Figure 10: Generic LDO with pMOS pass device

[6] and [7] are two examples of CMOS implementation of LDO. [6] has proposed bulk modulation technique for improving load regulation and stability of capacitor-less LDO. Similarly [7] has proposed techniques for increasing current efficiency of LDO especially at no or low load condition. Though the techniques discussed in these designs have not been used, they have given good insight into different design parameters of LDO.

3.1 Design

Figure 11 shows the CMOS implementation of LDO in this project. The components in this design include a folded cascode differential amplifier as error amplifier, pMOS buffer, pMOS pass device and feedback network of resistors.

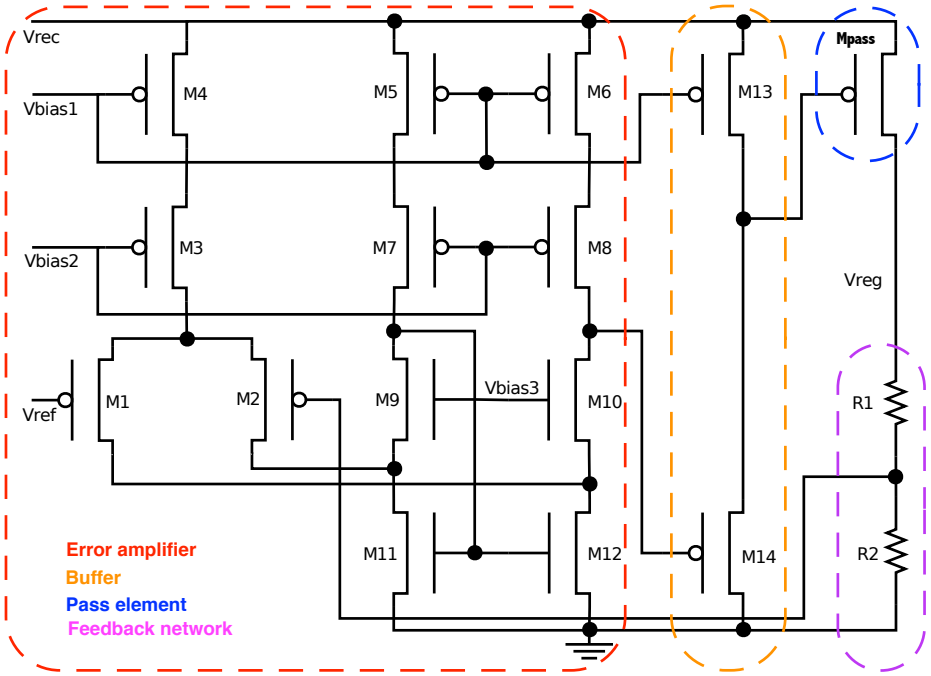


Figure 11: CMOS implemenation of LDO

As briefly mentioned above, the error amplifier amplifies the error i.e. difference in scaled regulated voltage, V_{div} and reference voltage, V_{ref}. It is known that an amplifier with higher open loop DC gain reduces the closed loop gain error and hence amplifier with higher

gain is desired here which is turn increase the accuracy of regulated voltage, Vreg [6]. Typically error amplifier has gain $> 40dB$ which is not achieved with a single stage amplifier with this technology. Higher gain can be achieved by cascading multiple single stage but with increased difficulty in making the multistage amplifier stable. So for achieving higher DC gain and at the same time for stability convenience, folded cascode amplifier [8, pp. xx] is chosen.

Table 4: LDO design parameters

Pass device	pMOS
$(Wp/Lp)_{pass}$	540um/280nm
Input supply	>2.2 V
Error amplifier	folded cascode
Vbias2	1.1 V
Vbias3	0.88 V
Vbias4	0.68 V
Vref	1.17 V
C_{load}	> 2.5 µF
R_{esr}	> 0.8 Ω
Regulated output voltage	1.8 V
I_{load} max.	10 mA

The amplifier has a nMOS differential input stage, perferably for its higher mobility for achieving more gain. Reference voltage, V_{ref} will be bandgap voltage, 1.17 V, of silicon and thus ICMR for EA lies almost at half the supply voltage. This amplifier drives a pMOS buffer which is used to supply sufficient current to drive the large pass transistor. Moreover, pMOS as a buffer passes 1 better which means it can turn off the pass device completely and hence LDO regulates better at low load or no load condition. However for heavier load/larger load current, this pMOS buffer is not able to pull down the gate of pass device suffuiciently lower. This is overcome by making the pass device large enough to feed the required maximum load current.

The pass device is a pMOS transistor in this design. It is chosen because it has several advantages over it's counterparts like nMOS and BJT devices in terms of dropout voltage, quiescent current, in-

put voltage, thermal response and noise[9]. Prominently, there are two factors that give pMOS edge over other devices; dropout voltage and quiescent current, when it comes to application in low power and low voltage devices. nMOS as a pass device requires a positive drive voltage with respect to output to operate. On the other hand, pMOS is driven by a negative signal with respect to input which means pMOS is preferable for a low input LDO. Similarly compared to BJTs, pMOS requires less headroom and less quiescent current to be driven[9], [10], which means low dropout and low power operation, typical requirement of today's micro devices' power supply.

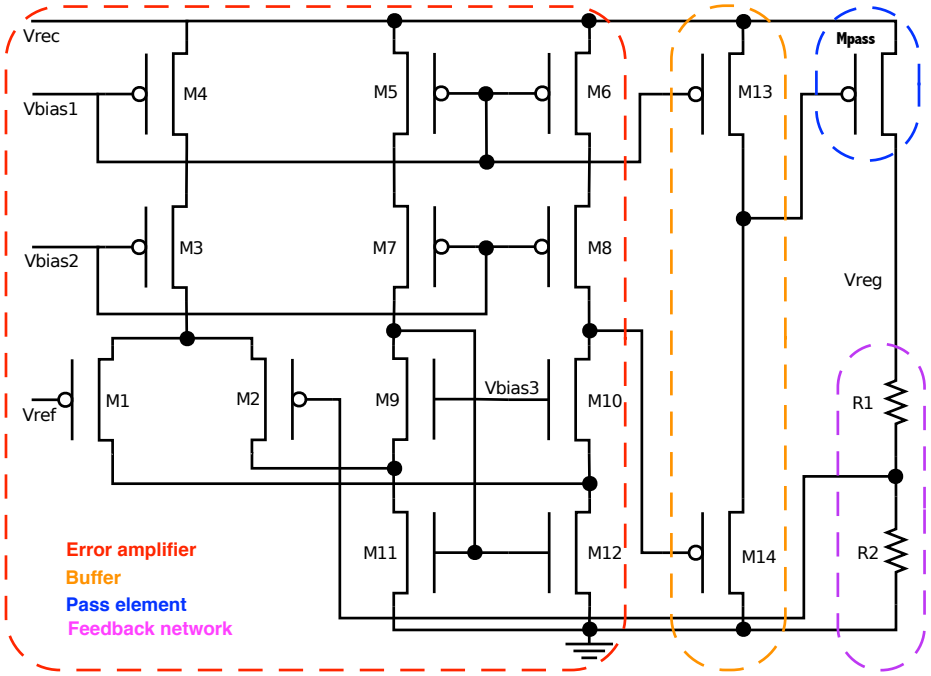


Figure 12: LDO testbench setup

However, pMOS as a pass device in LDO causes challenges in stability. As mentioned above, LDO utilises a high gain feedback loop in order to provide a regulated output voltages independent of load current and in any system with feedback loop, the locations of poles and zeros determine stability of the system. In case of the pMOS LDO, the pass device is configured in a common source configuration. LDO with big output cap has a dominant pole pole at the output, which is a low frequency pole. The second pole is located at the gate of pass device because as mentioned earlier pMOS pass device is large and

has a big parasitic capacitance. This second pole may be located closer to the dominant pole, resulting in significant reduction in phase margin (PM). Consequently, this may lead to instability of the LDO with pMOS pass device. Various methods have been implemented for ensuring the stability of the pMOS LDO. In this project, a large external capacitor, C_{load} in figure 10, is used for stabilising the system at the cost of additional settling time. When an external capacitor is used for designing a stable LDO, the minimum value of capacitance, C_{load} and minumum value of its equivalent series resistance (ESR), R_{esr} should be specified[10]. C_{load} determines the dominant pole of the LDO and R_{esr} in series with C_{load} introduces a left half plane zero below unity gain frequency, UGF of LDO in order to cancel out the non-dominant pole below UGF, producing a stable LDO system.

3.2 Transient response

Figure 13 is the transient simulations of the LDO which illustrates generation of regulated output voltage, $Vreg$ for both maximun load, 10 mA. For maximum load, it takes minimum 107 us to produce stable voltage. Since a large capacitor is used for stabilising LDO, it take longer time. Compared to schematic result, it takes 9 us extra time which can be accounted additional parasitic capacitance of interconnects at the output of LDO.

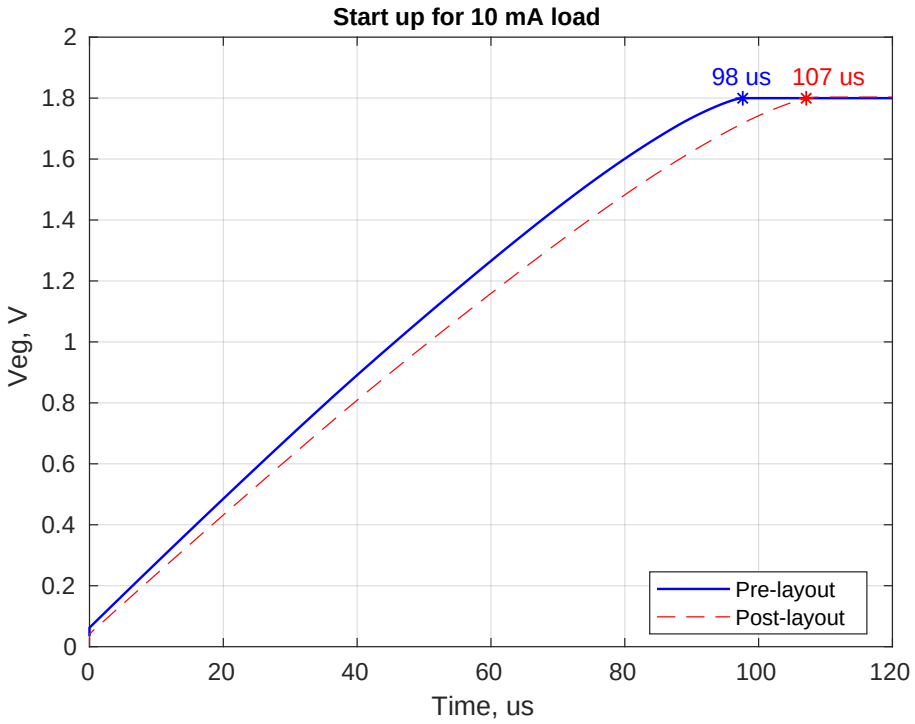


Figure 13: LDO transient simulation

Figure 14 and 15 show the transient response of LDO for line, $Vrec$ and load, $Iload$ variation. It gives information about how well and how fast regulated output settles for line and load variations. In figure 14 load is given as pulse varying from 10 uA to 10 mA with both falling and rising time of 1 ns keeping input supply constant to 2.2 V. Sudden increase in load causes the output voltage to drop. The error amplifier then takes some time adjusts the gate voltage of pass device to low to fully turn on the device. Likewise when the load suddenly drops to minimum, it causes the output voltage to increase. Again error amplifier adjust it back by increasing the gate voltage of pass device to turn it off. Similarly for line variation observation, input, $Vrec$ is pulsed from 2 V to 2.5 V with 1 ns rising and falling time keeping load current constant to 10 mA. Sudden increase in input voltage causes output to increase and vice-versa. As in load variation case, similar recovery pattern is seen. In both case of load and line regulation, the out put voltage is maintained quickly, less than 0.15 us. Both results from schematic and post layout have same transition behaviour except post layout result offset by 3.7 mV as explained in DC response section below.

Line regulation, change in regulated output voltage due to maximum change in input voltage and load regulation, change in output voltage due to maximum change in load current are calculated from values shown in respective plots and are listed in table 5.

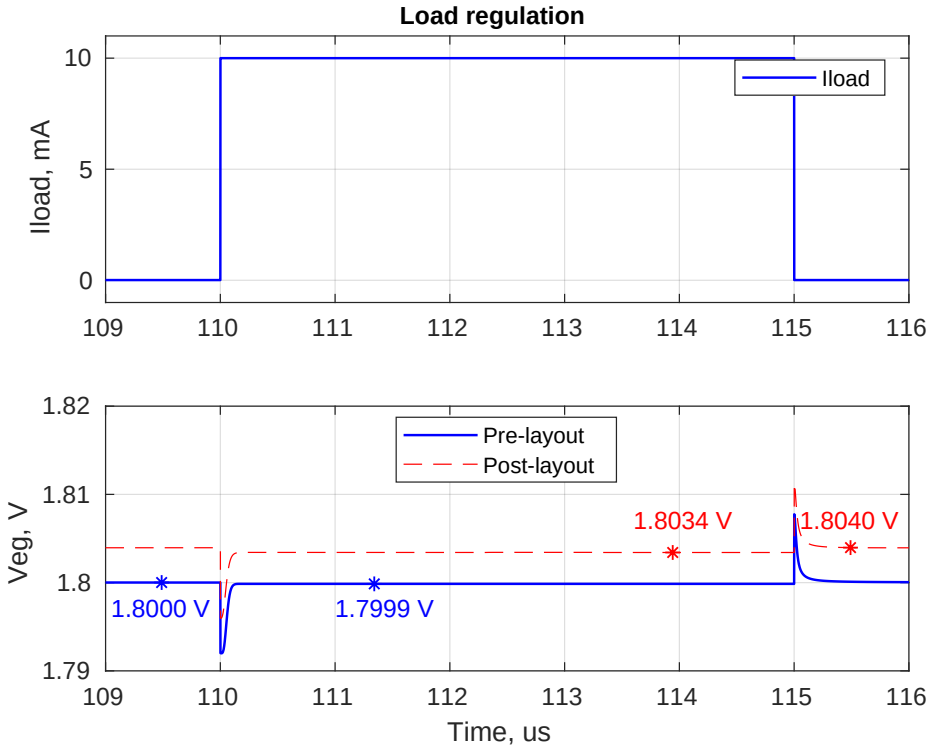


Figure 14: LDO step load regulation

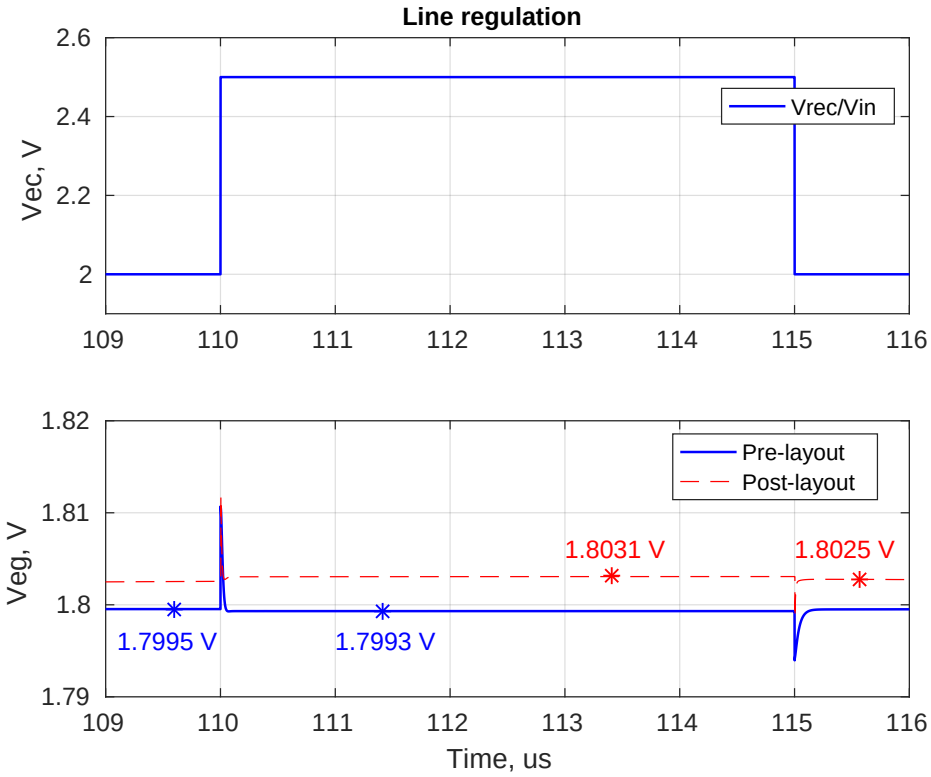


Figure 15: LDO step line regulation

3.3 DC response

Figure 16 and 17 show LDO response to input voltage, $Vrec$ sweep and output load, $Iload$ sweep. As seen in 16, the regulator is turned off for input below 1.85 V. Since the input is also the supply for the entire design, higher voltage is required for creating proper biasing of internal folded cascode error amplifier. However after turning on, it requires only 100 mV drop for proper regulation for maximum load and is even lesser for lighter load. This shows that minimum value of supply required for LDO to function properly is 1.95 V. In 17, it is seen that regulated output voltage for post layout simulation is 3.7 mV higher than for schematic. Since $Vreg = (1 + R1/R2) * Vref$, the mismatch in the resistors has resulted in slightly higher ratio, consequently increasing the close loop gain.

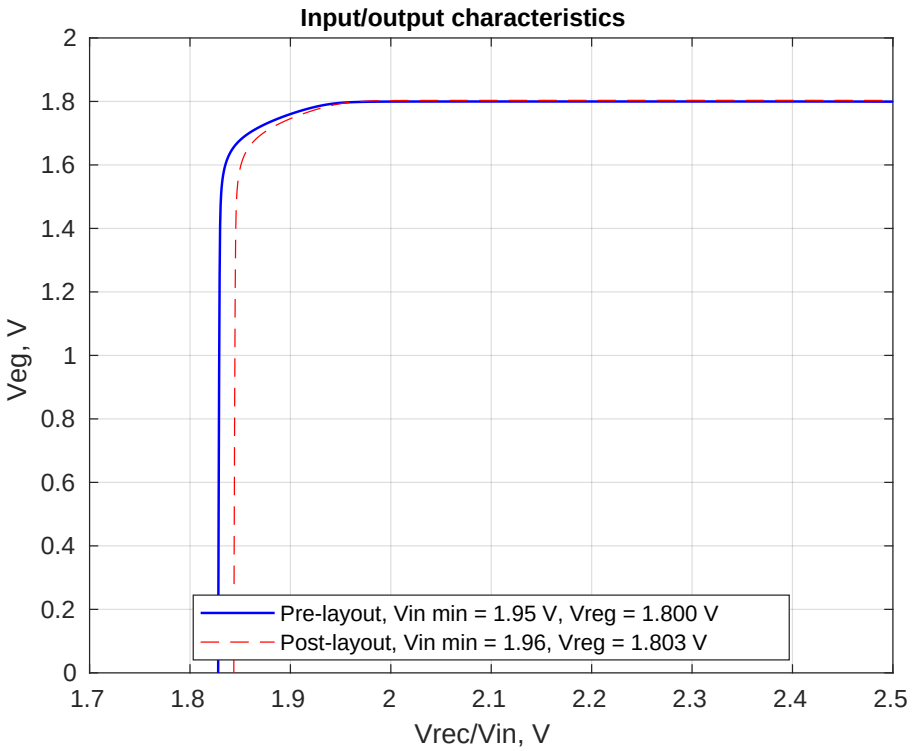


Figure 16: Regulated voltage with supply variation

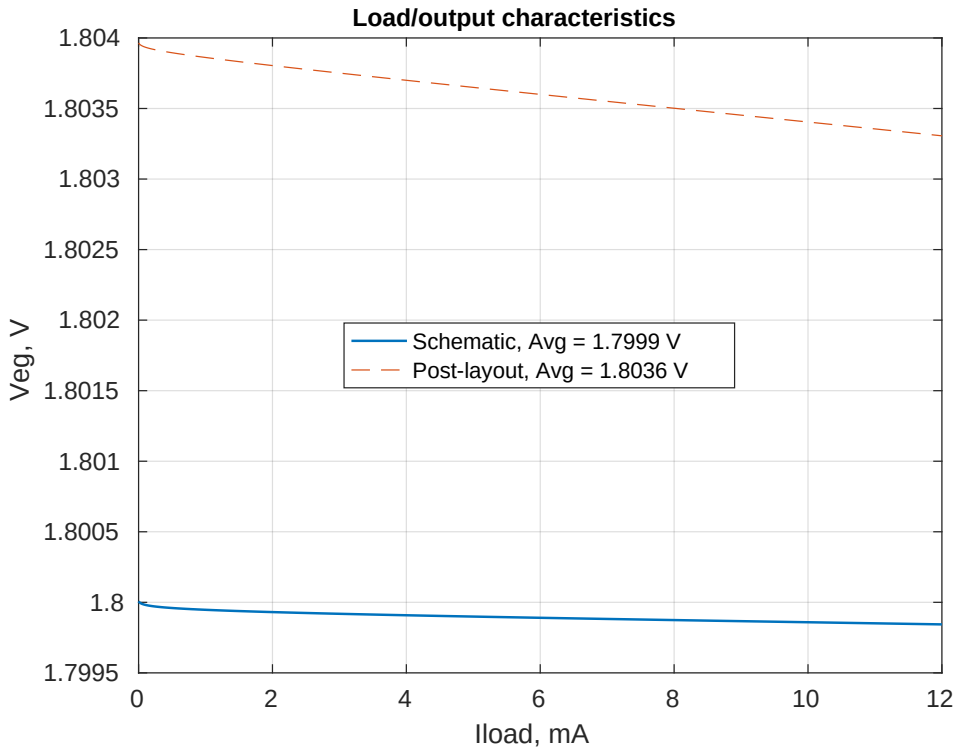


Figure 17: Regulated voltage with load variation

3.4 AC response

Figure 18 is open loop gain and phase margin of LDO without and with compensation. In the upper uncompensated bode plot, two poles below UGF are seen: the first one at 300 KHz due to output resistance of pass device and its parasitic capacitance, and the second one at 60 MHz due to buffer output resistance and gate capacitance of pass device. UGF is at 100 MHz. Due to these two poles both occurring below UGF, the PM fallen to -45°. For making the LDO stable, as discussed in the beginning, a capacitor, C_{load}, 2.5 uF with specific series equivalent resistance, R_{esr}, 0.8 Ω is used at the output. C_{load} and pass device output resistance creates the dominant pole at 1 KHz and R_{esr} and C_{load} creates a left half plane zero below UGF which cancels the non dominant pole. This eventually gives 75°PM and 30 dB GM.

Likewise figure 19 is the plot showing PSSR of this LDO. It can be seen that it has poor PSSR performance for frequency higher than 200

KHz. Low frequency noise like 50Hz supply ripple is effectively rejected. In this design 13.56 MHz ripple and its first harmonics is expected in the input of LDO because rectified output from rectifier operating at 13.56 MHz as input signal is used as supply and/or input for this LDO. Unfortunately, PSSR performance is worst around this frequencies. However the ripple rejection is still -36 dB at 13.56 MHz which is decent. As seen in figure 18, the open loop gain of LDO feedback circuit is 90 dB, which has contributed in achieving decent PSSR even at higher frequency[11]. This paper also discusses that UGF frequency corresponds to the roll off frequency of PSSR, which can also been seen by comparing plots 18 and 19. The stability technique in this design also gives adverse effect on PSSR performance as UGF is significantly lowered by large output capacitor.

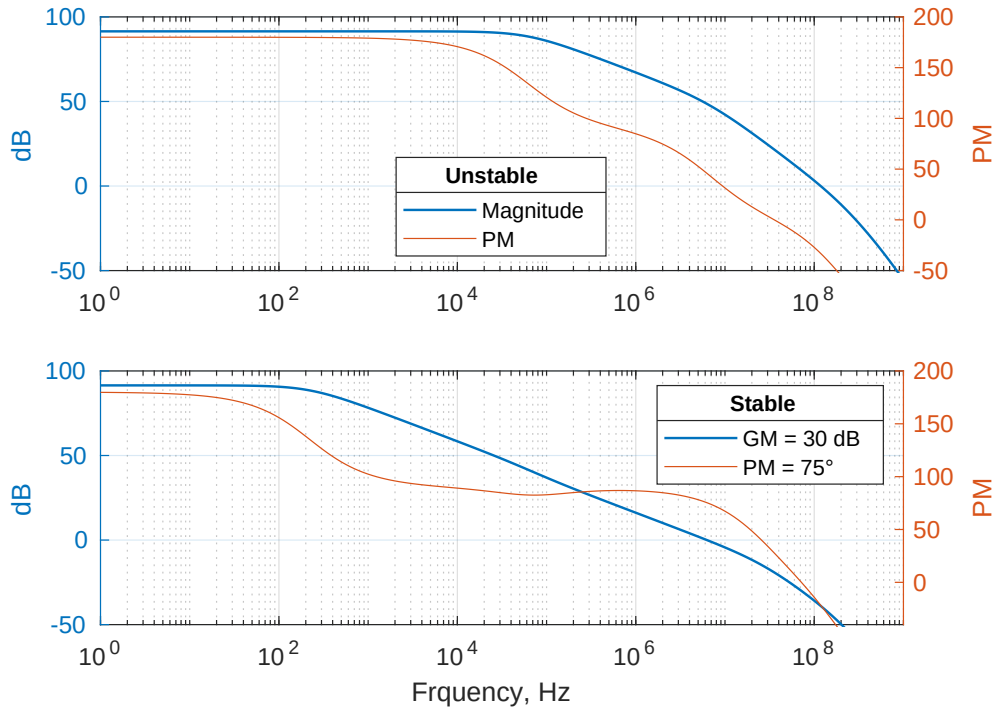


Figure 18: LDO stability before and after compensation

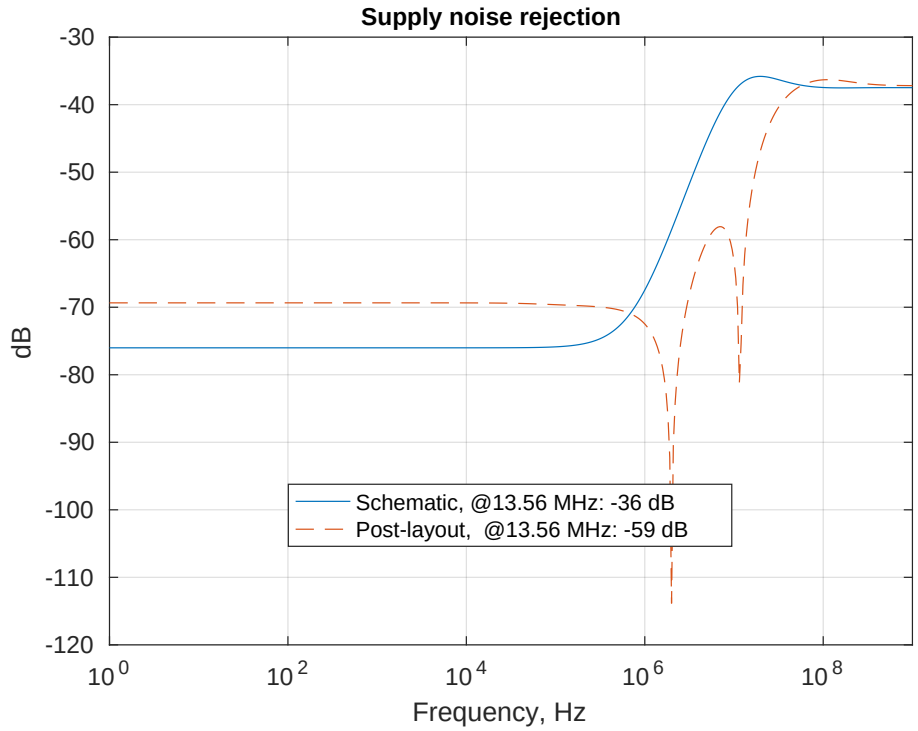


Figure 19: PSSR performance

Table 5 summaries the performance of LDO regulator discussed above. Power efficiency is calculated as power delivered to load to power consumed from the source. Quiescent current includes biasing currents for error amplifier, feedback resistors and buffer which is obtained by taking the difference of current drawn from the source and current delivered to the load. Both power efficiency and quiescent current is calculated for maximum load operation.

Table 5: LDO performance summary

	Schematic	**Post-layout**
PSSR	-36 dB @ 13.56 MHz	-59 dB @ 13.56 MH
Phase margin	75°	
Gain margin	30 dB	
Power efficiency	80.9 %	81 %
Quiescent current	105 uA	114 uA
Load regulation	17 uV/mA	53 uV/mA
Line regulation	435 uV/V	-1.162 mV/V

Reference and biasing circuit design follows next.

4 Reference and biasing

Reference and biasing circuit is important part of any analog circuit. It is required to bias the designed circuitry with proper voltages and currents for operating all the devices in the intended region. For reliable and consistent performance of the system, the references and biases should be independent of supply voltage and temperature variations. Moreover with the trend of shrinking device sizes, mismatch and process parameters variations have been so pronounced that these factors affect the operation of the devices. So for the todays' devices, it is necessary to design reference and biasing independent of PVT variations.

There are different methods of generating reference voltages and bias currents discussed in literatures. Basically, supply independent current source is generated first and then this current is passed through a resistor to get a reference voltages. Some ways of creating supply insensitive current sources are threshold voltage referenced, diode (V_{BE} in BJT) referenced thermal voltage referenced current sources [12, pp. 305-315]. However, these current sources are not temperature independent. Threshold voltage of MOS and forward voltage of diode or V_{BE} have a negative temperature coefficient TC and hence they produce a CTAT (complementary to absolute temperature) current. On the other hand, the thermal voltage(V_T) has positive TC and hence it produce a PTAT (proportional to absolute temperature) current. So these techniques, though being insensitive to supply variations, still cannot be used for accurate reference voltage generation because of temperature dependence. So bandgap reference (BGR) design is used to generate the required reference voltage for the LDO in this design which has significantly less PVT variations than the last three methods.

BGR design involves summing up two voltages of which one is PTAT and the other is CTAT, both having equal and opposite TCs. The equal and opposite TCs cancels out leaving the resultant voltage with a zero TC. Figure 20 is the CMOS implementation of reference and biasing circuit for this project which includes startup circuit, BGR circuit and biasing circuit.

PTAT current is first generated using thermal voltage referenced current source using PNP transistor as diodes, resistor and a op-amp controlled current mirror [8, pp. 391-392]. The current is $I = V_T ln(n)/R_1$, where $V_T = kT/q$ is thermal voltage with positive TC and n is number

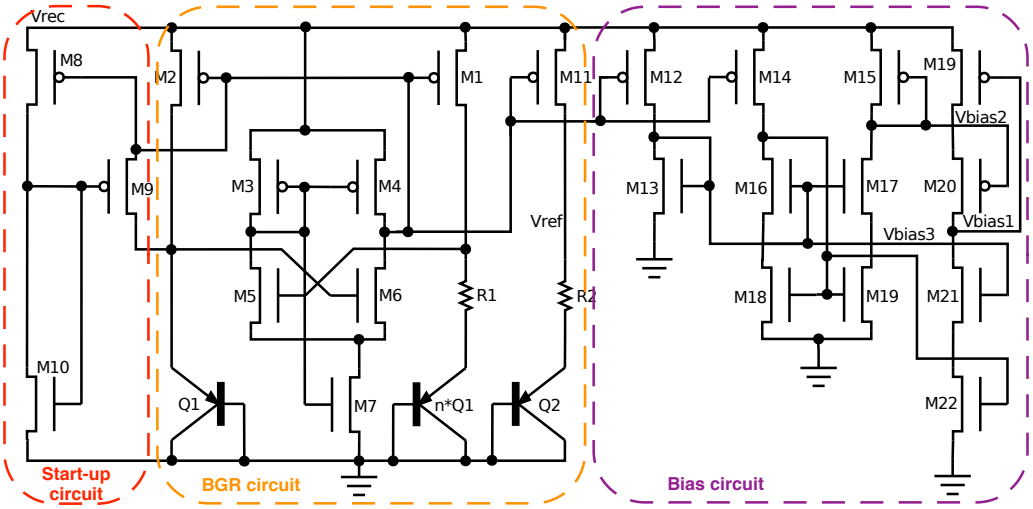


Figure 20: BGR and bias generation circuit

of parallel PNP transistors. This current is passed through a resistor, R_2 to create a PTAT voltage which is in series with a diode realised with a parasitic PNP transistor. The value of R_2 is so chosen such that the positive TC of PTAT voltage across it is equal to negative TC of V_{BE}. The temperature independent reference voltage is then given as $V_{ref} = V_{BE} + \alpha V_T ln(n)$, where $\alpha = R_2/R_1$ is equal to $\Delta V_{BE}/\Delta T$. Similarly the folded cascode operational transconductance amplifier (OTA) working as an error amplifier in LDO requires additional bias voltages which are produced as shown. Wide swing current mirror topology is used here for bias voltage generation.

In case of the supply independent and self biased circuit, there may be start-up issue. If all the transistors carry zero current, they may indefinitely remain off even when the supply is turned on. Therefore start-up circuit is added in order to ensure that the devices are turn on as supply voltage is provided. Once the circuit is fully operational, the start-up circuit is off and does not effect the normal operation of BGR circuit.

Figure 21, 22 and 23 illustrates temperature, DC and transient simulation of the BGR circuit respectively for slow(ss), fast(ff) and typical(tt) corners. The plots shows that V_{ref} is fairly independent with PVT variations. Similarly, I_{bias} varaitons used for generating the bias voltages remains within condiderable range. Table 6 summarizes the

performances of the BGR design.

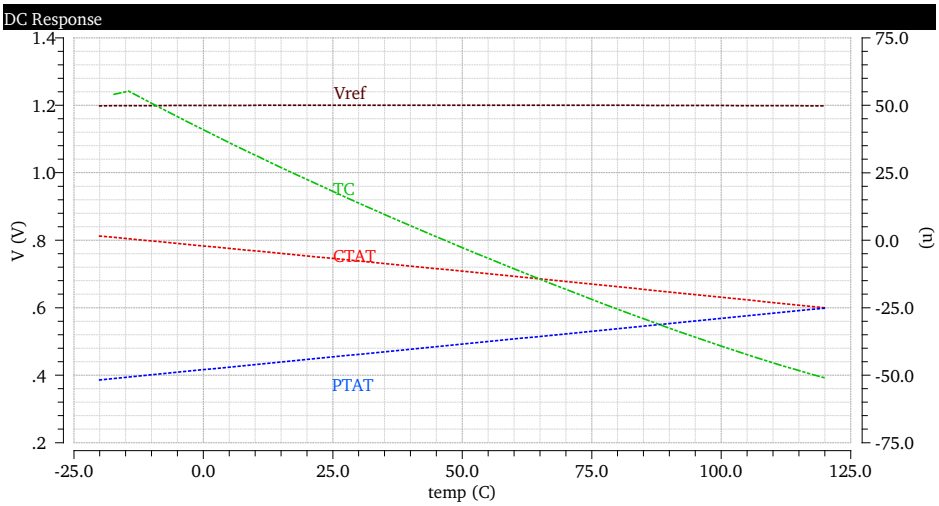


Figure 21: BGR over temperature varitaion

Table 6: BGR parameter and performance

V_{ref}	1.201.1 V @slow corner
	1.201.4 V @fast corner
	1.200.1 V @typical corner
TC @27°C	16.4 µV/°C
I_{bias}	8.95 µA @slow corner
	11.37 µA @fast corner
	10.04 µA @typical corner

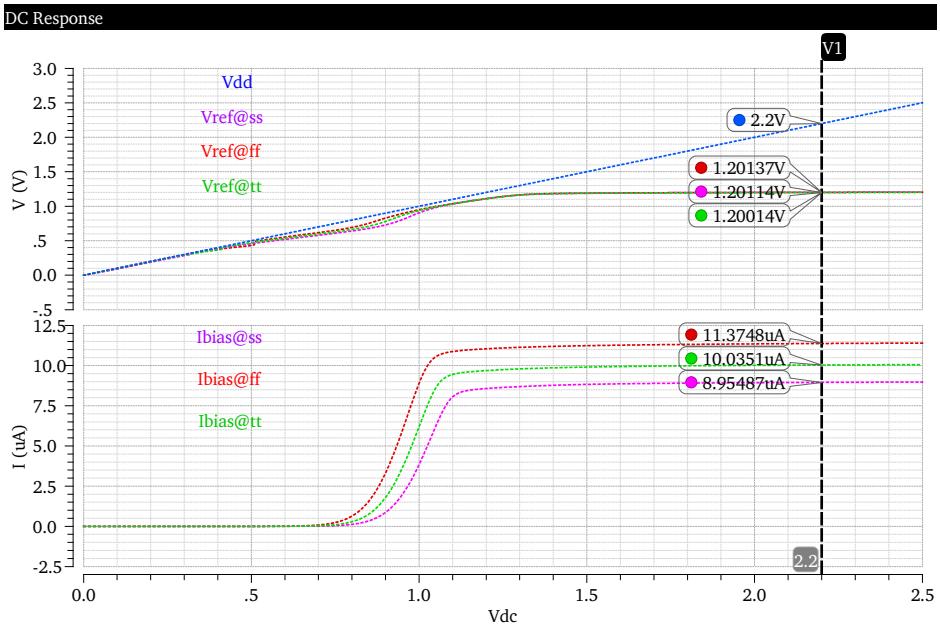


Figure 22: BGR DC performance

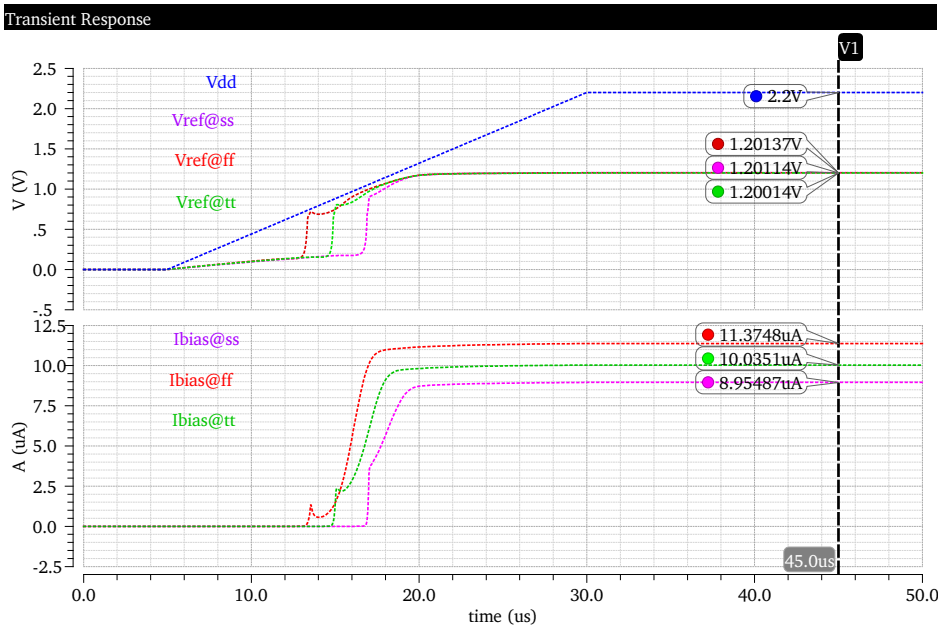


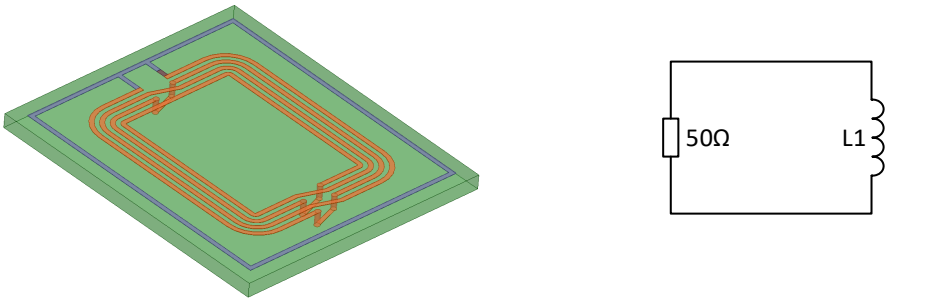
Figure 23: BGR transient performance

5 Antenna Design

All the components discussed above are part of any power management system. However, it is a pair of antennas which created inductive links for transferring power wirelessly and hence it is the actual physical component which makes wireless power transfer possible.

As already stated inductive coupling means coupling one coil with other, through magnetic field created in the first coil which induces the voltage in the second one. This is exactly the phenomenon for creating wireless power transfer link. In this project, the antenna dimensions are provided by Nordic Semiconductor which is one of their design already used in some application. Since having similar shape and size of antennas is important in gaining more transfer efficiency, the same antenna type is used as both primary and secondary coils.

For purpose of this work, with provided dimensions of the antenna, it is first modelled in HFSS as shown in figure 24a. More accurately, a planar antenna on a PCB can be modelled as in figure 25 which includes parasitic: Rp, series Dc resistance of wire and Cp, inter-winding self capacitance. These parasitic values minimise quality factor and self resonance frequency of the antenna. In the discussion ahead, these will not be explicitly mentioned because the parameter extraction will include these factors too. To realise a real antenna, physical parameters of materials used for making printed antenna on a PCB are also given for the model. After completing model, frequency sweep is done for extracting S parameter of the antenna which was eventually used to estimate self inductance of the modelled coil. The performance estimation of single antenna here and couple system later is based on formulas in [13]. In order to check and compare the estimated inductance value from the model, two different mathematical approximation methods described in [14] were used. All the values of inductance of the antenna estimated from different method is listed in table 7. The table shows that the modelled value is less than mathematically approximated values. This difference can be explained with two things. Firstly, mathematical calculation assumed that the antenna is spiral and rectangular with sharp edge but the model has rounded edge. Secondly, during modelling besides dimensions of the coils, physical parameters of coil materials are also used but these are not considered for mathematical calculation.



(a) HFSS antenna model (b) Equivalent schematic

Figure 24: Antenna model

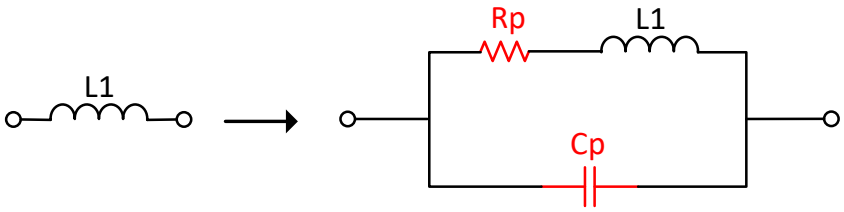
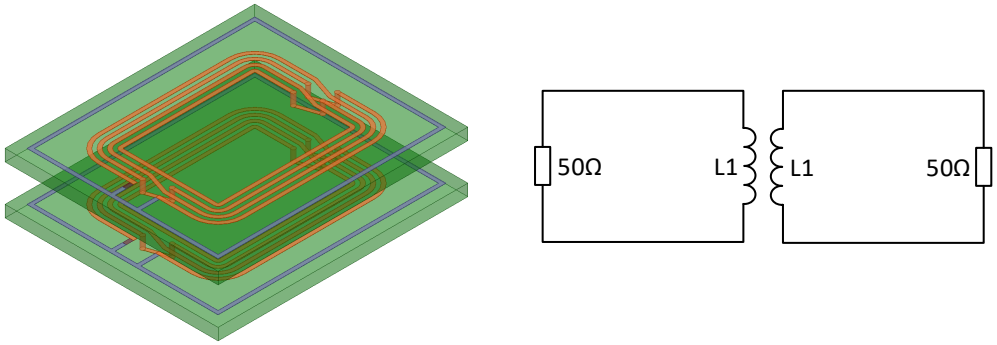


Figure 25: Real antenna model schematic

Table 7: Self inductance estimates comparision

HFSS model extraction	448 nH
Modified Wheeler Formula [14]	644 nH

The next step is to observe coupling of two antenna for varying distance of field interaction. Two coils, primary and secondary are aligned together separated by some distance as shown in 26. The same procedure as used for single coil above, is used to extract self inductance of each coil, $L1$ and $L2$, mutual inductance of two coils, $L12$, coupling coefficient between the coils, k and quality factor, Q. The extracted values for coil separation of 1mm, 5mm and 10mm are listed in table 8. $L1$ and $L2$ are same as in table 7 as it is the same coil used as primary and secondary. Similarly $L12$ and k are both decreasing with distance as expected.



(a) HFSS coupling model (b) Equivalent schematic

Figure 26: Antenna coupling model

Table 8: Coupling parameters for varying coils distance

Parameter	1 mm	5 mm	10 mm	mm
L1	-	-	-	nH
L2	-	-	-	nH
L12	-	-	-	nH
k	-	-	-	-
Q	-	-	-	-

The power transfer efficiency of the physical link created by coupled coils is very important. [CITE] states that efficiency depends k of coupling system and Q of coil and hence high k and high Q is always desirable and obviously coil optimisation is the most important part of

coupling system design. [15] and [16] discusses some techniques to optimise transfer efficiency of inductive link: [15] about matching the load for better resonance whereas [16] about designing optimal coil geometry for higher Q. The former one compares the efficiency of general inductive coupling and conventional resonant coupling and their limitation in achieving higher efficiency. This eventually proposes optimal resonant load transformation which has better immunity to poor coupling and load variation. Likewise, the later one describes step by step iterative process of designing an antenna with optimal geometry for the given design constraints.

In this project, conventional resonance coupling as in [CITE] is implemented to tune both primary and secondary to the power career frequency. This method makes the bandwidth narrower but increase Q at operating frequcncy, making gain maximum at this desired frequency.

For the purpose of making a resonant inductive link, the S parameter of coupled antenna system in HFSS is exported to ADS in order to design matching networks using capacitors only. Impedance of primary antenna is matched to 50 Ω source resistance and impedance of secondary is matched to load impedance (50 Ω load or input impedance chip(?)) as shown in 27. $Cp1$ and $Cp2$ together with $L1$ created parallel resonant circuit on the primary side and $Cs1$ together with $L2$ creates the secondary resonant circuit at 13.56 MHz, a pair of Lc tanke circuit si thus made tuned at same frequency. Resonant coupling system with 5 mm separation is taken as a typical example. The losses at both the terminals for this case just around our operating frequency are as shown in figure 28. These plots show that power losses at both the ports have been reduced by at least an order of magnitude.

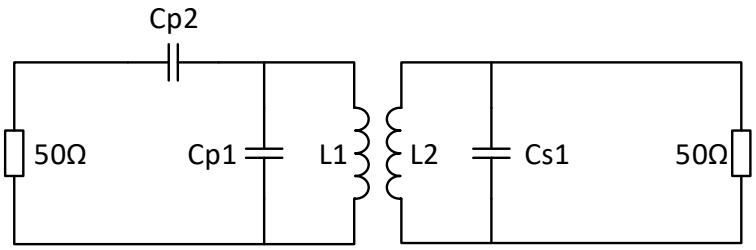


Figure 27: Resonant coupled inductive link

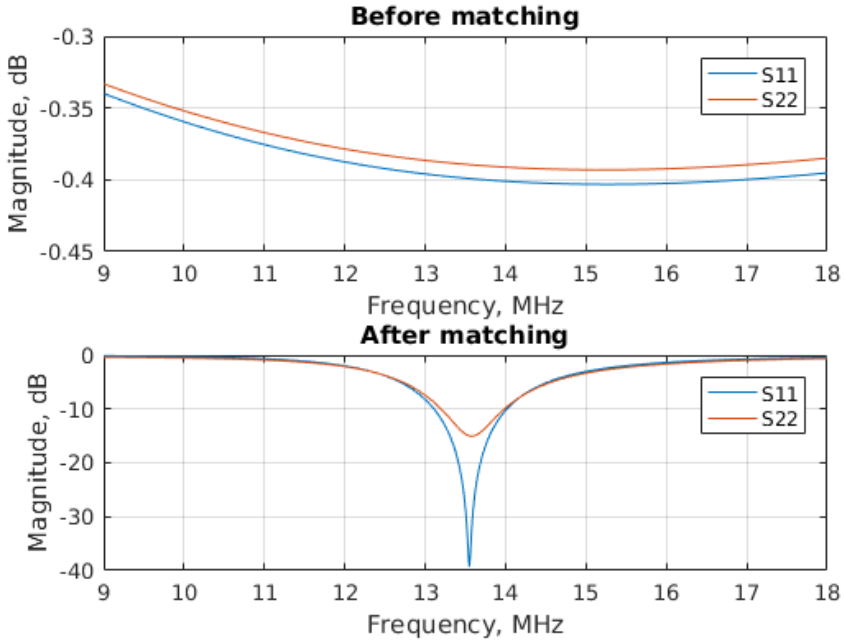


Figure 28: Power loss before and after matching

6 Power Receiving Unit

Power receiving unit is the complete system which includes all the component designed above: coupled antenna, rectifer, LDO and reference and biasing, as shown in figure[FIGURE]. The primary of tunned antenna system is driven by a power source and AC signal is generated at the secondary as discussed earlier in antenna design section. The rectifer then rectifies this AC singnal to DC. The DC output of the rectifer inherently has ripple, so LDO follows this rectifer to produce regulated DC output. The reference and biasing circuit generates required reference and biasing DC voltages for the LDO.

The simulation of the PRU system is done is two steps. As this system can be functionally divided into two sub-system: coupling system and Power Management System (PMS), fisrtly PMS is simulated excluding the coupled antennas to characterise the performace of PMS. Secondly, the whole PRU system: PMS with coupled antenna is simulated to observe the wireless power transfer and then management of this transferred power. Though it has already been told earlier, one important thing must be mentioned here again before going further. Even though reference and biasing circuit has been integrated into the PMS system, it has been designed with an option to override it externally. This externally supplied reference and biasing will be primarily used for the PRU system simulation. The result with on-system baises and reference will be explicitly noted.

Figure [FIGURE] is testbench setup for PMS simualtion. PMS block in the picture includes rectifer, LDO and RB. The values external biases and references and off-chip components are listed in table [TABLE]. The requirement and choice of these components are described in their respecitve design section above.

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Acronyms

BGR bandgap reference

CMOS complementary metal-oxide-semiconductor

CTAT complementary to absolute temperature

DC direct current

ESR equivalent series resistance

GM gain margin

ICMR input common mode range

LDO linear dropout

MOS metal-oxide-semiconductor

nMOS n-channel MOS

OTA operational transconductance amplifier

PCB printed circuit board

PCE power conversion efficiency

PM phase margin

pMOS p-channel MOS

PMS Power Management System

PSSR power supply rejection ratio

PTAT proportional to absolute temperature

PVT process voltage temperature

SMPS switch mode power supply

TC temperature coefficient

UGF unity gain frequency

VCE voltage conversion efficiency

Vp peak voltage

Vpp peak to peak voltage

Vtn thresold voltage of n-channel MOS

Vtp thresold voltage of p-channel MOS