Preliminary report on master project

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1 Introduction

This report is a brief overview of my master project on wireless power transfer through inductive coupling. It is the documentation of the schematic of complete design of the power receiving unit. It includes brief explanation about choices of design topologies and techniques. Figure 1 is the block diagram of the complete design including the test PCB and the test chip on it.

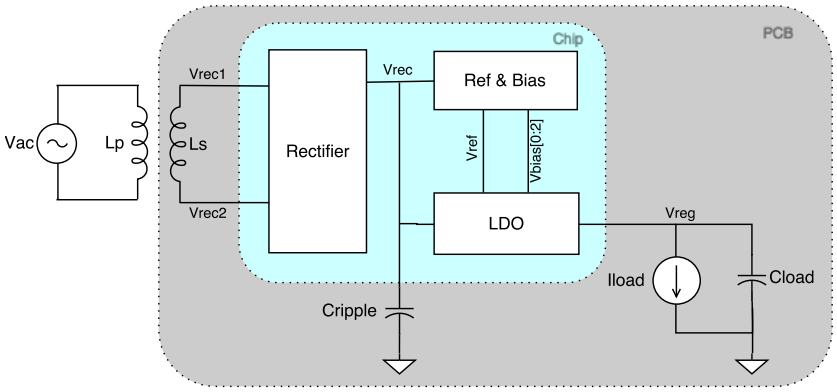


Figure 1: Block diagram of complete design

As shown in the block diagram above, the design includes inductor, rectifier, LDO regulator and reference and biasing circuits. This report mainly discusses about the various design aspect of rectifier and LDO. The inductor is designed with the specifications provided by NORDIC. The biasing and reference circuit is designed solely for learning the design technique without much effort on the accuracy of the generated biases and references. So externally supplied bias and reference will be the secondary option. The project is designed in tsmc90nm process. Table 1 lists the main specifications of this project.

Table 1: Project specifications

Technology	TSMC 90nm CMOS
Chip area	TBA mm^2
Max. load	10 mA
Output dc voltage	1.8 V

A brief discussion of the design is followed next.

2 Rectifier

The most basic rectifier is conventional full wave bridge structure where the diodes are replaced by the diode connected MOS. devices in CMOS. technology. This topology though being simple to implement, has a major drawback. It requires at least twice the Vtn of a MOS device as there are two diode connected MOSes in the conduction path for each cycle of the input signal.

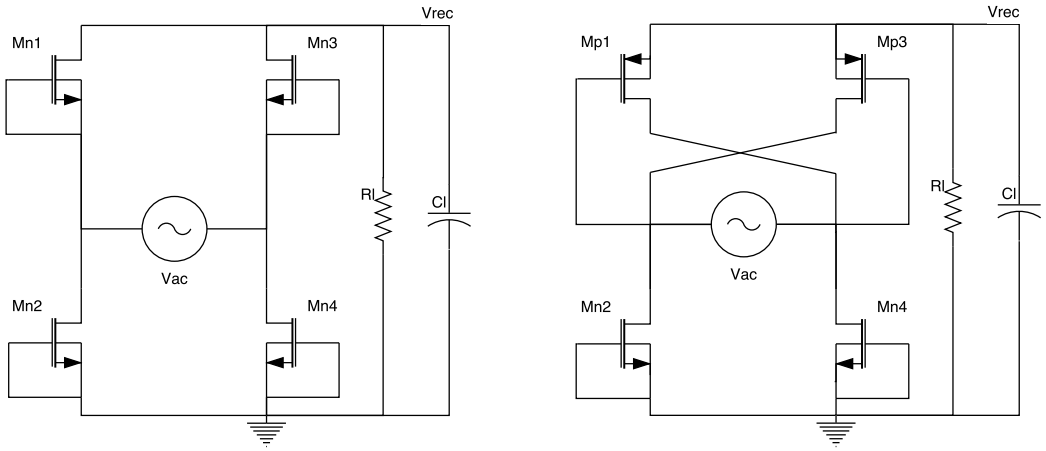
Gate cross coupled and fully gate cross coupled topologies are improvements over conventional full wave rectifier. In gate cross coupled rectifier, two diodes of conventional rectifier is replaced by two gate cross coupled MOSes working as switches where the voltage drop for every cycle is reduced to one threshold voltage. Similarly, in the fully gate cross coupled rectifier, all diodes are replaced by switches and hence the voltage drop is further reduced to twice the conduction drop only for every cycle. Even though this topology has least voltage drop, it suffers from the problem of reverse charge leakage because when the input ac amplitude is less than the output rectified voltage and the conducting pass devices are on simultaneously, current flows backward from output to input.

All the above discussed topology suffer from either large voltage drop or large power loss because of which their use are limited in low power and low voltage devices. The popular techniques for higher efficiency are using gate cross coupled rectifier along with passive or active circuitry for controlling other two pass devices. In passive rectifier, additional circuitry including bootstrap capacitor are used to reduce or eliminate threshold voltage one of which is discussed in this paper [1]. However, use of on-chip bootstrap capacitors limits it use where chip area and speed is of importance. On the other hand, in active rectifier, active circuitry is used control pass devices. The use of active circuitry increase both VCE and PCE because the pass devices are made to conduct in linear region and hence less conduction drop, and reverse current flow can be completely eliminated and hence less power loss. However active rectifier is not problem free either. The major issue is starting of the active circuit as there is no regulated supply at the start up.

In this project, active rectifier is chosen, primarily for better VCE and PCE and secondarily to avoid the use large on chip capacitors.

[2] and [3] have discussed same active rectifier topology with a slight difference in active circuitry. [2] has implemented comparator with compensating the falling output delay whereas [3] has implemented comparator with compensating both the falling and the rising output delay in expense of added circuit complexity and power consumption. [2] has been used here for its simple design.

Figure 2a, 2b and 3a is the CMOS implementation of conventional full wave bridge rectifier, gate cross coupled rectifier and proposed active rectifier in [2]. The problem with 2a and 2b has already been briefly mentioned above. Though 2b is significantly improvement over 2a , it is still not a favourable topology with respect to the design technology chosen. In hte gate cross couple rectifier of 2b, the cross coupled pMOSes act as switches, so the only voltage drop across them is conduction drop due to channel resistance. However the other two nMOSes are diode connected, so they have at least Vtn drop across them which means $Vac \geq Vdc + Vtn$ for conduction.



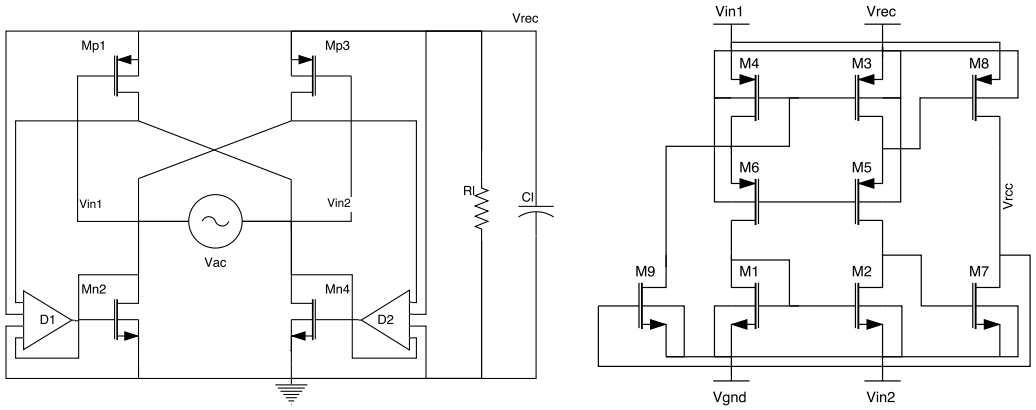
(a) Conventional full wave bridge rectifier

(b) Gate cross coupled full wave rectifier

Figure 2: Rectifier topologies: conventional and gate cross coupled

The proposed active circuit in 3a is improvement over 2b which eliminates Vtn drop required for conduction by replacing diode connected nMOS with devices controlled by active circuit as shown in figure 3b. The active circuit is a four input comparator that turns on nMOSes fast when Vac > Vdc and turns off fast to avoid flow of current.

For the illustration of operation of comparator, consider the case when $Vin1 > Vin2$ i.e. $Vac1 > 0$ and $Vac2 < 0$. During this half cycle, comparator $D1$ and $Mp3$ are reversed biased and hence both are off. For simplicity, assume $Vac = Vin1 - Vin2$. When Vac reaches Vtp, $Mp3$ turns on which shorts $Vin1$ to $Vrec$. When $Vac > Vrec$, $D2$ output goes high, which turns on $Mn4$ and starts the conduction path for the first half cycle and starts charging Cl. When Vac reaches maximum, it starts to decrease and at $Vac < Vrec$, conduction stops as output of $D2$ is low and $Mn4$ is off. As Vac further decreases to below Vtp, $Mp3$ if off too. This way rectifier in 3a conducts during positive half cycle eliminating the Vtn drop seen in 2b. Now the only drop is the conduction drop due to channel resistance of two pass devices along the conduction path. This drop is much less because during conduction both the device are operating in the linear region with small resistance. The operation is similar for $Vin2 > Vin1$ where $Mn4$ and $Mp3$ are off and $Mn2$ and $Mp1$ conduct to charge Cl.



(a) Gate cross coupled full wave active rectifer (b) Active circuit $D2$

Figure 3: Active rectifier and active circuitry (comparator)

Figure 3b is the implementation of four input comparator $D2$ used in 3a as proposed in [2]. It is designed to self power and bias because no steady state supply is available at start up. $M1$, $M2$ and $M7$ monitors voltage across $Mn4$ i.e $Vin2 - Vgnd$ and $M3$, $M4$ and $M8$ monitors voltage across $Mp3$ ie $Vin1 - Vrec$. So when $Vin1 - Vrec > Vin2 - Vgnd$ which means $Vac > Vrec$, output of $D2$ is high and turns on $Mn4$ instantly. But when $Vac < Vrec$, the output of comparator is delayed to fall which causes $Mn4$ to conduct in reverse direction leading to significant reduction in power delivered to load. $M9$ is introduced in order to

overcome this problem which adds offset currents to increase Van and Vpn faster, causing the output to decrease faster and turns off $Mn4$ before $Vac < Vrec$. This reverse current control technique compensates the comparator delay and increases the power efficiency of the rectifier.

The dimensions of the pass devices are first hand calculated by using square law current equation and devices parameters values given in the technology documents, and later optimised with simulation tool in order to make the rectifier to deliver the required current. Since nMOS does not have to have same device size as pMOS to deliver same current, optimal size ratio equation from [4] is used to find nMOS pass devices sizes. Similarly, the value of ripple rejection capacitor is chosen 100nF for better ripple rejection at the expense of some additional settling time.

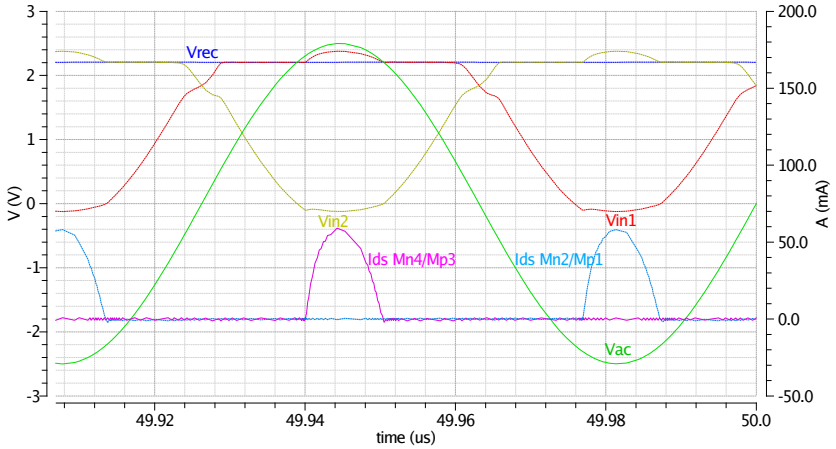


Figure 4: Voltage and current waveforms of the rectifier

Figure 4 show the simulation results showing voltages and current waveform of this designed rectifier. The generated waveforms clearly follows the working principle discussed above. Two important observations can be made from plots. First, the rectified output $Vrec$ is 2.2 V for Vpp ac input of 2.5 V which means the voltage loss has been significantly reduced and the loss of around 300 mV yields to the conduction loss due the the channel resistance. Secondly, the reverse current from output to input has been effectively eliminated as there is only positive current flowing to the load when all conducting devices are on. Similarly, figure 5 shows PCE and VCE with respect to magnitude peak ac input signal. Both PCE and VCE are very less for input ac amplitude less then 1.8 V. It can be explained by the fact that required bias cur-

rent and gate drive voltage are not achieved for smaller input. Finally, table 2 summarises the rectifier design parameters and its performance.

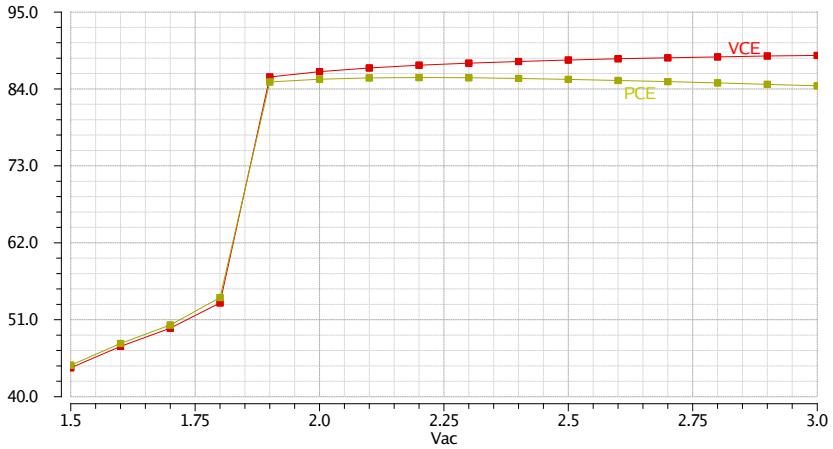


Figure 5: Voltage and power conversion efficiency

Table 2: Rectifier parameter and performance

Wn/Ln, Wp/Lp	550um/270nm, 900um/270nm
Rectifier area	TBA mm^2
Input ac frequency	13.56 MHz
Input ac Vp	2.5 V
Load current	11 mA
Ripple rejection cap	100nF
Output dc voltage	2.2 V
Ripple Vpp	3 mV
PCE	>85%
VCE	>88%

LDO design discussion is followed next.

3 LDO

Voltage regulator follows the rectifier designed above in order to regulated the rectified voltage to 1.8 V and deliver maximum current of 10 mA. Since the output from the active rectifier is 2.2 V and the required regulated voltage is 1.8 V, charge pump or SMPS of boost type is irrelevant here. Buck SMPS could be an option for voltage regulation but LDO is preferred for it better performance in terms of noise [5].

Figure 6 shows a circuit of typical pMOS LDO. As shown in the figure, the components includes an error amplifier (EA), a pass device (Mpass), a feedback circuit (R1 and R2) and load (Cout and Iload). A more general and complete LDO circuit also includes the circuitry for generation of reference voltages and bias current/voltages. However, in this project it will be discussed separately for now. In short the working principle of LDO is that the error amplifier compares the scaled down regulated voltage, Vdiv with Vref and regulates the internal resistance of the pass transistor such that the error, Vref - Vdiv is least or zero ideally.

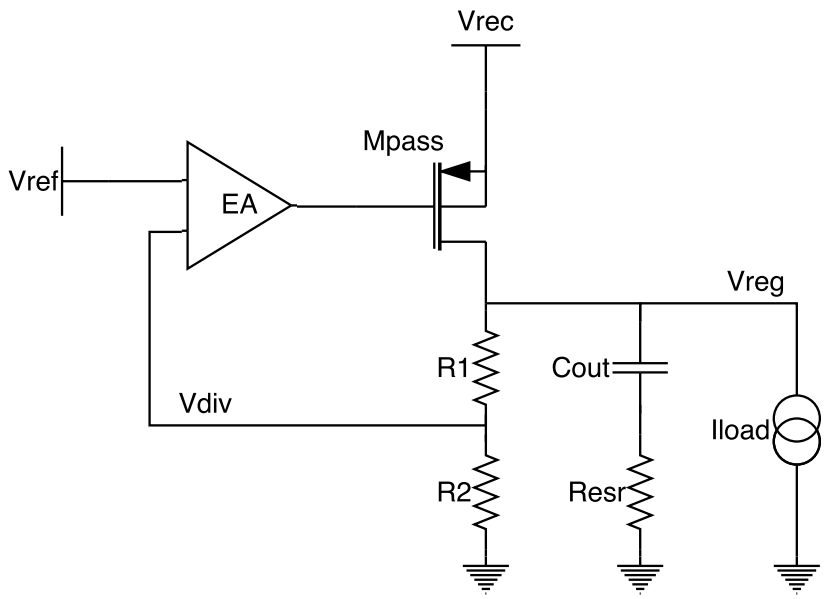


Figure 6: Generic LDO with pMOS pass device

[6] and [7] are two examples of CMOS implementation of LDO. [6] has proposed bulk modulation technique for improving load regulation and stability of capacitor-less LDO. Similarly [7] has proposed tech-

niques for increasing current efficiency of LDO especially at no or low load condition. Though the techniques discussed in these designs have not been used, they have given good insight into different design parameters of LDO.

Figure 7 shows the CMOS implementation of LDO in this project. The components in this design include a folded cascode differential amplifier as error amplifier, pMOS buffer, pMOS pass device and feedback network of resistors.

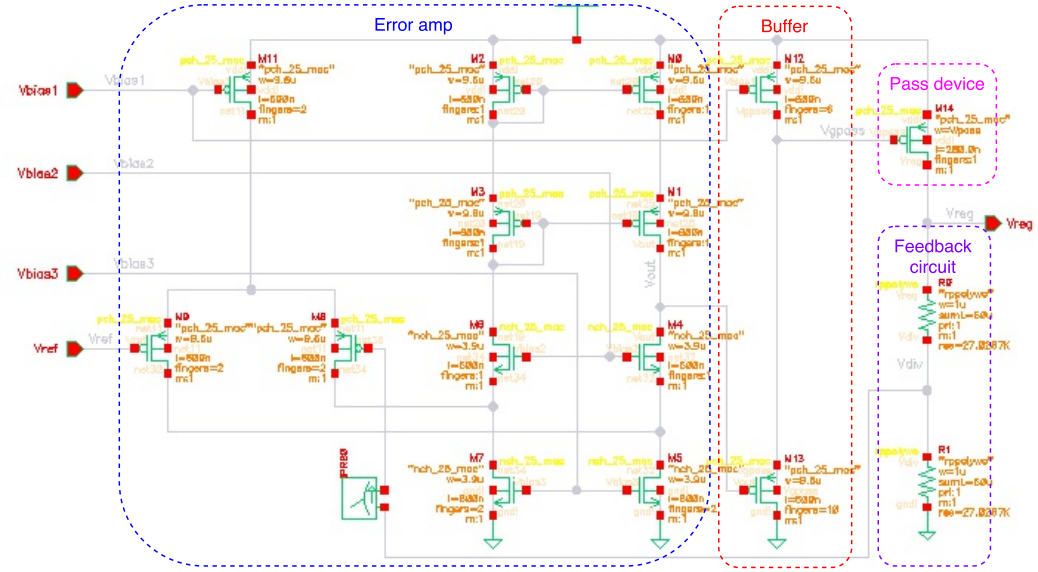


Figure 7: CMOS implemenation of LDO

As briefly mentioned above, the error amplifier amplifies scaled regulated voltage, Vdiv and reference voltage, Vref. It is known that an amplifier with higher open loop DC gain reduced the closed loop gain error and hence amplifier with higher gain is desired here which is turn increase the accuracy of regulated voltage, Vreg [6]. Typically error amplifier has gain $> 40dB$ which is not achieved with the single stage amplifier with this technology. Higher gain could have been achieved with multiple single stage but with increased difficulty making the amplifier stable. So for achieving higher DC gain and at the same time for stability convinence, folded cascode amplifier [8, pp. xx] is choosen.

The amplifier has a pMOS differential input stage in order to obtain lower ICMR of the amplifier closer to gnd because so is Vref.

Table 3: LDO parameter and performance

Regulated output voltage	1.8 V
I_{load} max.	10 mA
C_{load} min.	1.2 uF for PM >60°
Load regulation	TBA
Line regulation	TBA

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List of Figures

List of Tables

Acronyms

CMOS complementary metal-oxide-semiconductor

DC direct current

ICMR input common mode range

LDO linear dropout

MOS metal-oxide-semiconductor

nMOS n-channel MOS

PCB printed circuit board

PCE power conversion efficiency

pMOS p-channel MOS

SMPS switch mode power supply

VCE voltage conversion efficiency

Vp peak voltage

Vpp peak to peak voltage

Vtn thresold voltage of n-channel MOS

Vtp thresold voltage of p-channel MOS