Band-Gap References for near 1-V operation in standard CMOS technology

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Abstract

This paper presents two novel implementations of the current-mode band-gap reference (BGR) which support the very low supply voltages of the near future CMOS technologies, without resorting to special devices. Moreover the problem of the start-up of low-voltage BGRs is discussed and a simple solution which guarantees correct start-up over process, supply voltage and temperature variations is proposed. The band-gap references were implemented in a conventional $0.35\mu m$ CMOS technology and provides an output voltage of about 500 mV.

1 Introduction

Reference voltage generators are widely used in a variety of applications, from analog and mixed-signal circuits to digital circuits such as DRAM and flash memories. These cells are required to provide a stable voltage reference featuring a low sensitivity to temperature and supply voltage. One of the most popular architecture is the bandgap reference (BGR) which was firstly implemented in bipolar technology. In digital CMOS the need for a bipolar device in order to develop the bandgap voltage was fulfilled by adapting the original scheme to the commonly available substrate-vertical pnp BJT. However, the constant trend of microelectronics towards smaller lithographies and the booming market of battery-powered portable systems are forcing a continuous reduction of the supply voltage which is going to reach the value of the silicon band-gap voltage, i.e. 1.25 V. This makes the well established BGR architectures not feasible in the last available technologies (0.18 μm). Recently, a low-voltage BGR based on the current-mode principles and providing an output voltage of about 0.52 V was proposed [1]. The implementation of the basic idea, however, suffers from some, relevant, drawbacks such as the use of non-standard devices, the need for an external start-up signal and a minimum supply voltage of about 2 V. This paper presents two novel implementations of the current-mode BGR, overcoming the above cited limitations: the former (BG1) is designed for very-low voltage operation while in the latter (BG2) a correct start-up is achieved without an external signal. Moreover, both of them are designed for standard CMOS technology, without resorting to special devices. It should be remarked that near 1-V operation was achieved with a conventional 0.35 μm technology, therefore using MOS devices with higher thresholds than in the last, deep sub-micron technologies.

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2 Low-voltage Bandgap reference Circuit

Conventional BGRs in CMOS technology are designed with the commonly available substrate-vertical pnp BJT. In the voltage-mode configuration derived from the bipolar designs, the output voltage (V_{REF}) is obtained as the sum of a PTAT term and a forward diode voltage (V_f). The lowest sensitivity to the temperature is invariably obtained by setting $V_{REF} \approx 1.25\ V$, i.e. the silicon band-gap voltage. For very-low voltage applications, the reduction of the reference voltage without affecting the original temperature dependence is of concern.

One of the few solutions to this problem is the current-mode BGR reported in Fig. 1 [1]. Two currents, proportional respectively to V_f and $V_T = \frac{KT}{q}$ are generated by a single feedback loop. If the same aspect ratio is used for $M1$, $M2$ and $M3$ and $R1 = R2$, currents $I1$, $I2$ and $I3$ have the same value, $I1b = I2b$ and, therefore, $I1a = I2a$, as long as the op. amp. is able to keep its inputs at the same voltage.

The value of $I2b$ is readily obtained from circuit inspection, i.e. $I2b = \frac{V_{f1}}{R2}$, while $I2a$ can be expressed as a function of V_T (PTAT term):

$$I2a = \frac{\Delta V_f}{R3} = \frac{V_T \cdot ln(N)}{R3} \qquad (1)$$

where ΔV_f is the difference between the forward voltage of diodes, i.e. base-to-emitter junctions, $D1$ and $D2$, and N is the area ratio between the two diodes. From the

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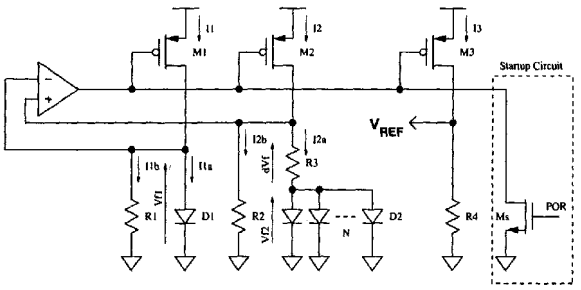

Figure 1: The current-mode Bandgap Reference [1].

above derivations, $I3$ can be expressed as the sum of a term linearly dependent on a diode voltage and a PTAT contribution:

$$V_{REF} = R4 \cdot \left(\frac{V_{f1}}{R2} + \frac{\Delta V_f}{R3} \right) \quad (2)$$

Therefore, by choosing a convenient value for resistor $R4$, a voltage reference with the same properties in terms of temperature sensitivity of the conventional BGR but with an arbitrary low value can be obtained in principle.

Nevertheless, the implementation of this current-mode BGR, highlights some important limits. Indeed, in [1] the input stage of the op. amp. makes use of depletion-mode pMOS transistors, in order to cope with the supply voltage reduction. This solution makes the circuit not useful for standard, low-cost CMOS technologies, where such special devices are rarely available and/or precisely modeled. Moreover, an external start-up signal is necessary, thus raising problems at system level if a Power-on-Reset signal is not available. Finally, the proposed implementation of the current-mode BGR in a 0.4 μm CMOS can tolerate a minimum supply voltage of about 2 V, thus well far from the required 1.2 V of near future technologies [2].

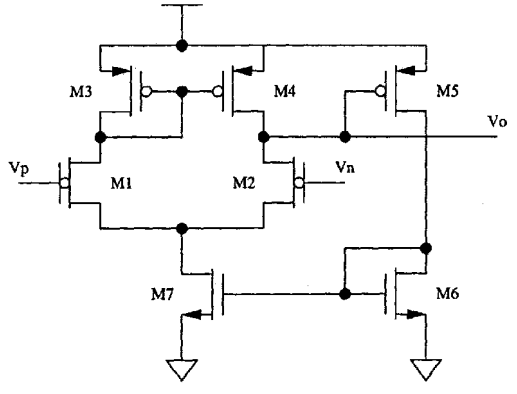

Figure 2: The depletion-mode op. amp. proposed by [1].

3 Low-voltage BGRs for digital CMOS

The circuit in Fig. 1 can operate in principle with a very low supply voltage since we have to accommodate only a forward biased diode and a pMOS transistor in saturation-mode between ground and the supply voltage. However, several problems arise in the implementation of the op. amp. which has to establish the correct bias point. Moreover, if properly designed, the op. amp. could also guarantee a correct start-up at the circuit power-on.

3.1 The op-amp

The differential amplifier used in [1] make use of a MOS depletion differential pair (Fig. 2), in order to accommodate a common-mode voltage as low as V_f. However, use of special devices is not convenient due to the higher costs related to the further process steps and to device characterization and modeling. A general-purpose architecture should make use of devices available in conventional CMOS technologies. To this aim two different implementation of the op. amp. were developed:

- *pMOS* input stage working in weak inversion.
- *nMOS* input stage with level shifter.

The implementation based on a *pMOS* differential pair in weak inversion is shown in Fig. 3. It should be noted that the second gain stage (*M5*, *M6*) is loaded by a diode connected pMOS transistor, *M6*). Therefore the biasing of the op. amp. is derived from the output voltage, *Vo*, leading to a high power supply rejection (PSRR) at the cost of a lower voltage gain. The devices in the input stage, *M1-4*, work in strong inversion when the supply voltage is decreased from the maximum allowed value,

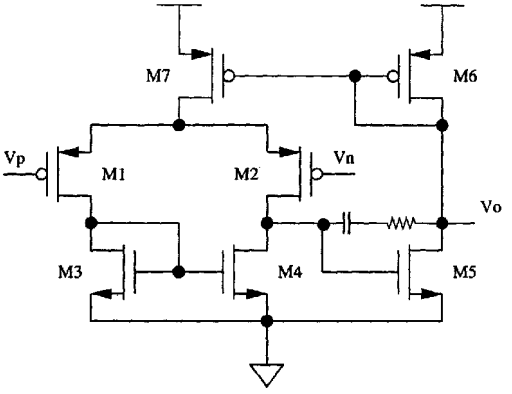

Figure 3: Weak-inversion *pMOS* op-amp for the current-mode BGR (BG1).

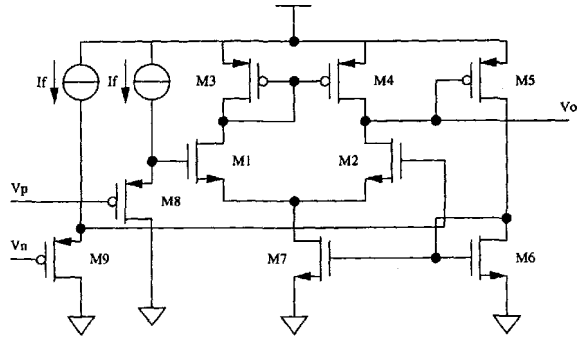

Figure 4: The proposed *nMOS* op-amp for the current-mode BGR (BG2).

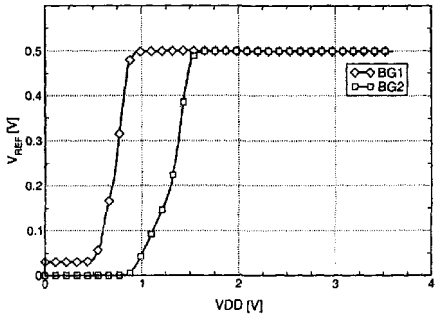

Figure 5: Simulated output voltage at 27 °C and at different supply voltages of the two proposed BGRs, BG1 and BG2, using the op. amp. in Fig.s 3 and 4, respectively.

3.6 V, down to about 1.4 V. Below this value the input devices enter in weak inversion reaching a bias current of few nA at *Vdd*=1 V. Simulation, Fig. 5, reveals that with a supply voltage lower than 0.9 V there is no more enough loop gain to keep the BGR at the correct bias point. A sufficient stability margin is achieved by means of the pole-zero compensation provided by the R-C series. Regarding the behavior of the circuit at the power-on, the op. amp. in Fig. 3 is not able to guarantee a correct start-up. Indeed, with *Vf1*=*Vf2*=0 V, the op. amp. output settles to the supply voltage, thus determining a bias current equal to zero. Therefore, this unwanted bias point for the BGR must be avoided be a proper start-up circuit, as discussed in the next sub-section.

The second proposed op. amp. implementation is based on the use of an input level shifter, made by a couple of pMOS source followers, providing a correct common-mode voltage at the input of the nMOS differential stage, Fig. 4. The further V_{gs} voltage introduced in the signal path limits the minimum supply voltage to about 1.4 V, as confirmed by simulation, Fig. 5. Below this bound the input transistors in the differential pair, i.e. *M1* and *M2*, enter in the triode region, thus causing a significant reduction of the voltage gain. Further disadvantages of this architecture are a higher power consumption and a higher input offset voltage for the op. amp.. This non-ideality of the op. amp. increases the spread of the reference voltage, V_{REF}, around the typical value. On the contrary, a significant advantage of using this second op. amp. is that, in principle, no start-up circuit is necessary to bring the BGR to the correct bias point at the power-on, as discussed in the next sub-section.

3.2 Circuit startup

With the op. amp. in Fig. 1, the BGR may settle at the power-on in an stable bias point where the positive and the negative input of the operational amplifier are at the ground potential, i.e. where the bias current of the BGR is negligible. This unwanted condition must be avoided by the startup circuit. Many startup circuits are reported in literature, using flip flops, comparators or power-on reset (POR) circuits. In the BGR reported in [1], Fig. 1, the gate of *Ms* is brought to the the supply voltage for a relatively short time in order to force some bias current to flow in the BGR core (*R1*, *R3*, *D1*, *D2*). This simple solution can raise problems if a POR signal is not available in the system. Using a diode which connects for a short time the BGR output to a reference potential raises several difficulties in the low-voltage CMOS BGRs due to the low output voltage, well below the typical diode voltage drop, and the low supply. Indeed, because of the lower voltage swing which the nodes of the BGR in Fig. 1 experience then in a typical 1.25 V BGR, that common start-up technique cannot be used. This is due to the fact that or this technique is not able to guarantee a correct start-up over every process, supply voltage and temperature (PVT) condition or the diode is not turned off completely when the proper bias point is established, leading to a non-negligible leakage current affecting the output reference voltage. At the same time, the use of comparators raises several design difficulties due to the low value of V_{REF}. To circumvent these problems, a novel startup circuit was developed, Fig. 6,

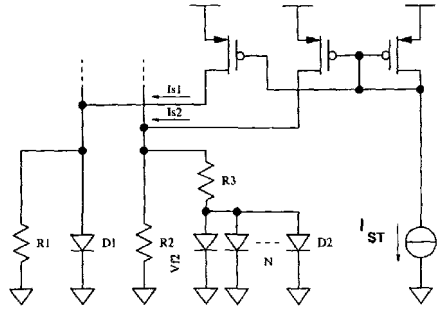

Figure 6: The proposed startup circuit with different injected currents.

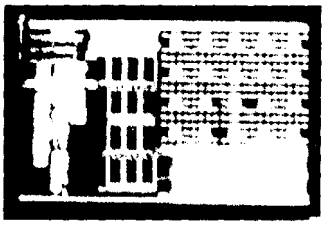

Figure 7: Chip photograph of the BG2 cell.

where two currents, $Is1$ and $Is2$, with **different values** ($Is1 \approx 4 \cdot Is2$) are injected in the BGR core. It should be remarked that unlike in the previously proposed BGR, Fig 1, two different currents are injected at each side of the BGR core, i.e. at the input nodes of the op. amp.. This brings the common mode voltage at the op. amp. input to a sufficiently high level and forces a some differential input voltage at the same time. By properly setting the sign of the differential input voltage of the op. amp. at the start-up, the output of the op. amp. stays low at the power-on, thus ensuring a non-null bias current for the BGR. In order to avoid that $Is1$ and $Is2$ affect the BGR output when the correct bias point is established, the current generator I_{ST} should be designed as a pulse current generator, driven by a POR signal. Unlike the weak-inversion op. amp., the circuit in Fig. 4 could in principle be used without any start-up circuit, since it works properly with an input common-mode voltage equal to the ground potential. However, its input offset voltage might force Vo near to the supply voltage at the start-up, i.e. when both inputs are at zero volt, thus setting the BGR in the wrong bias point. To avoid this possibility and ensuring a correct start-up over PVT corners, the same start-up circuit in Fig. 6 was used also in the second BGR using the nMOS op. amp.. However, since a low current value for I_{ST} is sufficient to this purpose, the second BGR was designed with a fixed start-up current, thus avoiding the need for an external POR signal, at the cost of a little error affecting V_{REF} caused by $Is1$ and $Is2$. However, this error is usually negligible in many applications

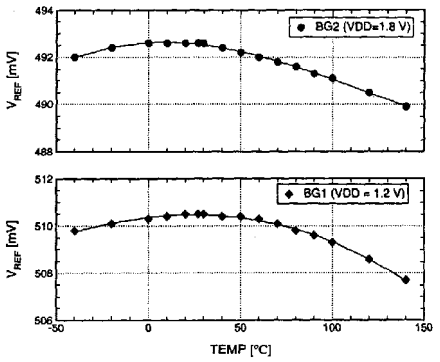

Figure 8: Measured V_{REF} at different temperatures for BG1 at 1.2 V supply (bottom graph) and BG2 at 1.8 V supply (top graph).

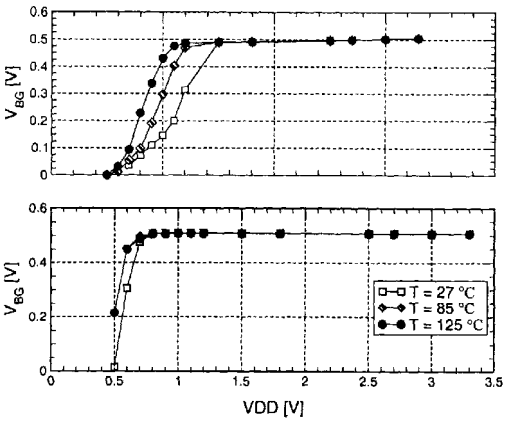

Figure 9: Measured V_{REF} for BG1 (bottom graph) and BG2 (top graph) Vs. supply voltage at different temperatures.

4 Experimental results

Two BGRs using respectively the weak-inversion (BG1) and the nMOS op. amp. (BG2) were implemented in a digital 0.35 μm CMOS technology. A photograph of the BG2 cell is reported in Fig. 7. Fig. 8 shows the measured reference voltage over the extended temperature range at 1.2 V and 1.8 V supply for BG1 and BG2, respectively. Fig. 9 shows the measured dependence of the reference voltage on the supply voltage, at three different temperatures. These measurements highlight a minimum supply voltage of about 0.9 V for the BG1 reference using the weak-inversion op. amp. and 1.4 V for the BG2 reference which does not require an external power-on signal.

Acknowledgments

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References

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