DESIGN OF A 1.5-V HIGH-ORDER CURVATURE-COMPENSATED CMOS BANDGAP REFERENCE

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ABSTRACT

A novel low-voltage low-noise high-order curvature-compensated CMOS bandgap reference is proposed in this paper. Two resistor strings are added to the bandgap circuit to reduce the supply voltage. In addition, a temperature-dependent resistor ratio generated by a high-resistive poly resistor and a diffusion resistor is used to provide the high-order compensation. The proposed bandgap voltage reference can operate down to a 1.5V supply (where V_{th} = 0.9V at 0^{o}C) with a temperature coefficient of less than 15.2ppm/^{o}C and an average line regulation of 5.5mV/V.

1. INTRODUCTION

Voltage reference is an essential component in many electronics device such as power converters, data converters and also RF circuits [1]-[6]. The temperature dependence of the voltage reference undoubtedly affects the performance of these applications. As a result, low-voltage low-power low-temperature-drift voltage references become increasingly important in commercial products. In fact, there are many existing techniques to reduce the temperature coefficient (tempco) of the reference voltage such as quadratic temperature compensation techniques proposed by Song *et al*. [1] and piecewise-linear curvature correction developed by Rincon-Mora *et al*. [2]. A simpler approach for second-order and third-order curvature-compensated bandgap references based on a temperature-dependent resistor ratio has been proposed by Lewis *et al*. [4] and Audy [5], respectively. This idea has been further extended by Leung *et al*. [6] to high-order curvature correction and applied in a CMOS voltage reference design [6].

The curvature-compensated CMOS bandgap voltage reference in [6] utilizes the negative-temperature-coefficient high-resistive poly resistor and the positive-temperature-coefficient diffusion resistor to implement a temperature-dependent resistor ratio which can effectively reduce the temperature drift of the bandgap reference voltage. Both of the resistors can be implemented in CMOS technology [7]. The reported minimum supply voltage is 2V, and is not low enough for future applications [8].

In order to further reduce the required supply voltage for future applications, a low-voltage curvature-compensated bandgap reference based on the idea in [6] is proposed in this paper. It is achieved by using two identical resistor strings to simultaneously provide the curvature-compensation and voltage-level shifting.

In this paper, the proposed low-voltage voltage reference is presented in the Section 2. The important design considerations that will affect the accuracy of the voltage reference such as current-mirror matching, offset voltage of the amplifier and output noise are all included. The experimental results are presented in Section 3 to verify the idea. Finally, a conclusion is given in Section 4.

2. PROPOSED CURVATURE-COMPENSATED BANDGAP REFERENCE

The circuit structure and the complete schematic of the proposed low-voltage high-order curvature compensated bandgap reference are shown in Figs. 1 and 2, respectively.

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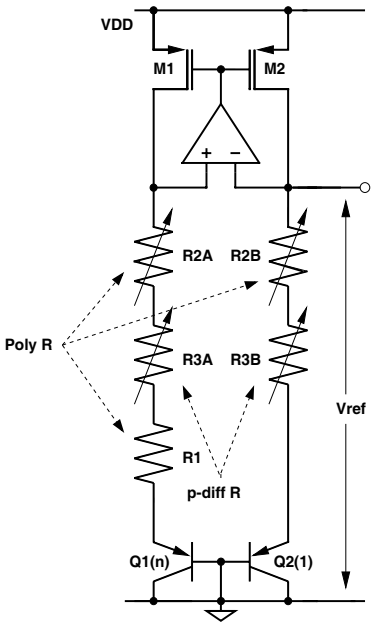

Fig. 1: Circuit structure of the proposed bandgap reference with high-order curvature compensation.

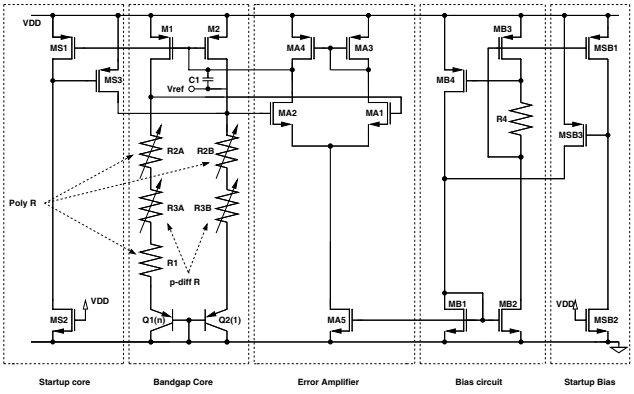

Fig. 2: Complete schematic of the proposed design.

In order to lower the supply voltage, which is limited by the V_{GS} drop of the PMOS input-stage of the error amplifier in conventional designs, a NMOS input-stage amplifier is used. The resistors strings R_{2A}, R_{2B}, R_{3A} and R_{3B} are used to level-shift up the dc voltage at the inputs of the error amplifier such that the error amplifier can operate in a high-gain region. The values of the resistors are set to R_{2A}=R_{2B} and R_{3A} =R_{3B}. The reference voltage is obtained at the negative input but not the positive input of the error amplifier due to stability issue.

In addition, the resistor string can also provide a high-order compensation of the bandgap reference voltage. The principle of operation is similar to the one in [6], R_1, R_{2A} and R_{2B} are high-resistive poly resistors (poly R), while R_{3A} and R_{3B} are p-diffusion resistors (p-diff R). The reference voltage, V_{REF}, is given by

$$V_{REF} = V_{EB2} + \left[\frac{R_{2B}}{R_1}\ln(N)\right]V_T + \left[\frac{R_{3B}}{R_1}\ln(N)\right]V_T \quad (1)$$

The resistor ratio R_{2B}/R_1 is temperature-independent as R_{2B} and R_1 are implemented by the same material, while the ratio of R_{3B}/R_1 is temperature-dependent as two different types of materials are used. The temperature coefficients of resistivities of poly R and p-diff R are $-1.05\text{x}10^{-3}$ and $1.65\text{x}10^{-3}$, respectively, in the technology used [9].

To achieve a high output accuracy that is less sensitive to process variations, the design of the current mirror and amplifier with low offset voltage is very important. Moreover, the stability of the reference circuit is one key point to consider. The design requirements and methods are stated below.

1. *Current-Mirror Matching*

The error-amplifier is used to enforce V_{DS} of M_1 equal to V_{DS} of M_2 in order to maintain the accuracy of the reference voltage. Moreover, M_1 and M_2 are designed with long channel devices to reduce the channel-modulation effect. This will not degrade the performance of the bandgap reference as the speed is not a concern in the bandgap reference design.

2. *Amplifier with Low Offset Voltage*

As the offset voltage of the error amplifier is temperature dependent, it will affect the accuracy of the reference voltage. The temperature-dependent offset voltage is given by [10]

$$V_{OS} = \Delta V_{THN} + \left(\frac{g_{mP}}{g_{mN}}\right)\cdot|\Delta V_{THP}| + \frac{1}{2}\cdot\sqrt{\frac{2I_{DN}}{\mu_N C_{OX}(W/L)_N}}\left[\frac{\Delta(W/L)_P}{(W/L)_P} - \frac{\Delta(W/L)_N}{(W/L)_N}\right] \quad (2)$$

To reduce the offset voltage, the g_m of M_{A3} and M_{A4} (g_{mp}) should be much smaller than that of M_{A1} (g_{mn}). The biasing current I_{DN} from M_{A5} should be small and the sizes $(W/L)_N$ of M_{A1} and M_{A2} should be large.

3. *Output Noise*

Minimization of the noise source from the error amplifier can reduce the noise at the reference output. The output noise of the amplifier is given by [10]

$$v_{oea} = \sqrt{2v_n^{\,2} + 2v_p^{\,2}\left(g_{mp}/g_{mn}\right)^2} \qquad (3)$$

To minimize the output noise, (g_{mp}/g_{mn}) should be small, and it is achieved by the same design approach as the offset-voltage minimization.

4. *Frequency compensation*

As mentioned previously, the reference output is taken from the negative input of the error amplifier due to the two feedback loops (positive feedback formed by error amplifier and M2, while negative feedback formed by error amplifier and M1) in the circuit. The capacitive load at the negative input of the error amplifier reduces the bandwidth of the positive feedback for better stability. Moreover, pole splitting by C_1 is used for stability enhancement. A design guideline is to use a larger C_1 for a larger load capacitance.

3. EXPERIMENTAL RESULTS

The proposed CMOS bandgap reference has been implemented in AMS 0.6-μm CMOS technology. The threshold voltage is about 0.9V at 0°C. The chip micrograph is shown in Fig. 3 and the active chip area is 283μm × 413μm. Fig. 4 shows the measurement result of the reference voltage under different supplies and temperatures. The temperature coefficient of the proposed bandgap reference at supply voltages of 1.5V, 1.6V, 1.7V, 1.8V, 1.9V and 2V are 14.36ppm/°C, 15.16ppm/°C, 15.17ppm/°C, 14.39ppm/°C, 13.59ppm/°C and 13.58ppm/°C, respectively. The measurement results show that the reference provides a low-tempco reference voltage.

The measured power-supply rejection ratio (PSRR) and the output noise spectrum are shown in Fig. 5 and 6, respectively. The measured PSRR of the proposed bandgap reference is -42dB at 10MHz, and the output noise is 0.135μV/sqrt Hz@100Hz. The line regulation is approximately 5.5mV/V at room temperature. The total current consumption is less than 20μA. Table 1 summarizes the performance of the proposed bandgap reference.

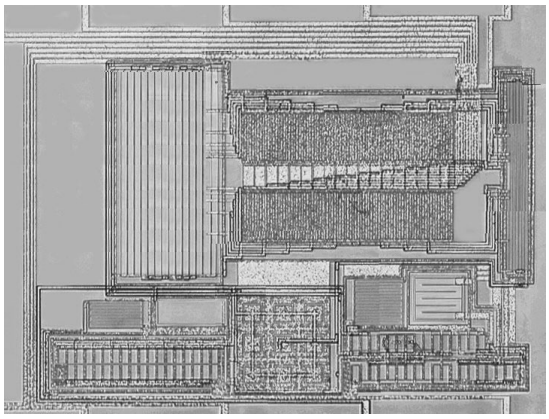

Fig. 3: Micrograph of the proposed CMOS bandgap voltage reference.

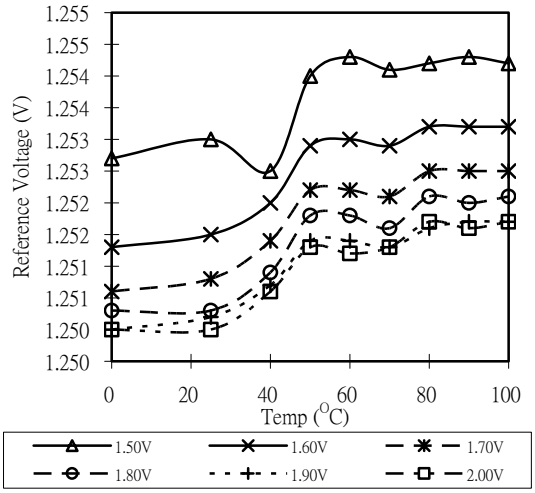

Fig. 4: Measured reference voltage vs. temperature.

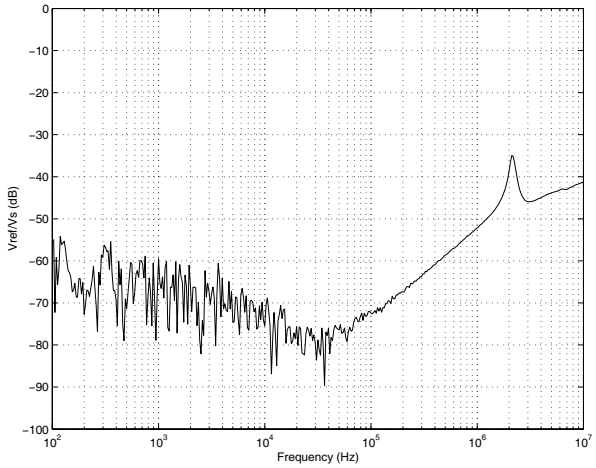

Fig. 5: Measured PSRR.

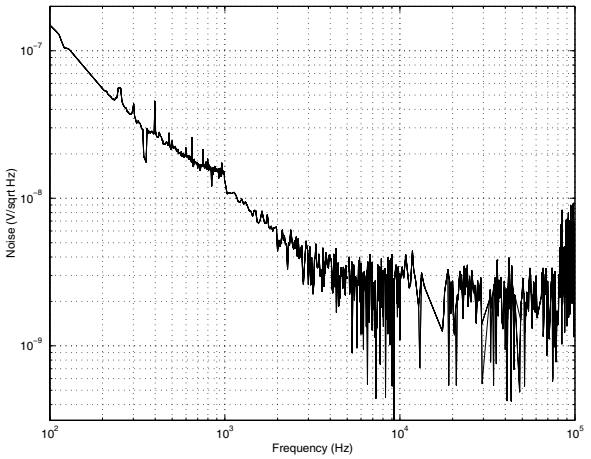

Fig. 6: Measured output noise spectrum.

Table 1: Measured Performance Summary of the Proposed Voltage Reference.

Specification	Measured Result
Supply Voltage	1.5-2V
Current Consumption	<20μA
Nominal Reference Voltage	~1.2525V
Tempco@V_{DD}=1.5V	14.36ppm/°C
Line Regulation@T=27°C	5.5mV/V
Output Noise@100Hz	0.135μV/sqrt Hz
PSRR@10MHz	-42dB
Chip area: 283μm × 413μm in AMS 0.6-μm CMOS N-well technology	

4. CONCLUSION

A 1.5-V CMOS bandgap voltage reference has been presented in this paper. High-order curvature correction based on temperature-dependent resistor ratio is used. With the proposed structural balanced circuitry, the accurate and error-free implementation provides a reference voltage with a low temperature coefficient, high PSRR and low noise.

ACKNOWLEGDEMENT

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