Design and Optimization of Printed Spiral Coils for Efficient Transcutaneous Inductive Power Transmission

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***Abstract*—The next generation of implantable high-power neuroprosthetic devices such as visual prostheses and brain computer interfaces are going to be powered by transcutaneous inductive power links formed between a pair of printed spiral coils (PSC) that are batch-fabricated using micromachining technology. Optimizing the power efficiency of the wireless link is imperative to minimize the size of the external energy source, heating dissipation in the tissue, and interference with other devices. Previous design methodologies for coils made of 1-D filaments are not comprehensive and accurate enough to consider all geometrical aspects of PSCs with planar 3-D conductors as well as design constraints imposed by implantable device application and fabrication technology. We have outlined the theoretical foundation of optimal power transmission efficiency in an inductive link, and combined it with semi-empirical models to predict parasitic components in PSCs. We have used this foundation to devise an iterative PSC design methodology that starts with a set of realistic design constraints and ends with the optimal PSC pair geometries. We have executed this procedure on two design examples at 1 and 5 MHz achieving power transmission efficiencies of 41.2% and 85.8%, respectively, at 10-mm spacing. All results are verified with simulations using a commercial field solver (HFSS) as well as measurements using PSCs fabricated on printed circuit boards.**

***Index Terms*—Coupling coefficient, implantable microelectronic devices, inductive wireless links, neuroprostheses, power transmission efficiency, telemetry.**

I. Introduction

WIRELESS operation of implantable microelectronic devices is necessary for clinical applications in order to reduce the risk of infection and patient discomfort, which can result from transcutaneous wires breaching the skin. A wireless implant is also safer, more robust, and less likely to be damaged as a result of broken interconnects. Another important requirement, which has made implantable devices applicable to the treatment of a growing number of ailments and conditions such as deafness, blindness, and paralysis, is being minimally invasive, which is a direct consequence of small size. Cochlear implants need to be placed inside the $3 \sim 6$ mm thick temporal bone near the ears [1], retinal implants are expected to be placed inside the eyeball through a 5-mm incision [2], and invasive brain–machine interfaces are being developed for the $1 \sim 3$ mm epidural spacing between the outer surface of the brain and the skull [3].

Unlike pacemakers, high power requirements and extreme size constraints in aforementioned applications, which belong to a broader category of implantable devices known as neuroprostheses, have prevented the use of batteries as the primary source of energy within the implanted devices. Instead, the battery is kept out of the patient's body and power is delivered wirelessly across the skin through a pair of inductively coupled coils that constitute a transformer [4]. In the case of deep brain stimulators (DBS), however, the electrodes are kept in place within the neural tissue and the rest of the implant has been displaced to the chest area where there is more space available [5]. Hence, DBS implants can afford to include a primary battery at the cost of a subcutaneous cable running from the chest across the neck to the electrodes on top of the head [6].

Even outside of the body, the battery needs to be small, light weight, and have a long lifetime due to portability, aesthetic, and economic reasons. The external part of the cochlear implants, for example, should fit comfortably behind the user's ears. Therefore, the efficiency of the power transmission from the external battery to the implanted electronic load should be maximized to extend the battery lifetime. Another reason is the limited allowable tissue exposure to the ac magnetic fields, which can result in excessive heat dissipation if violated [7], [8]. Interference between the RF link and other nearby communication devices and appliances is also a concern, which is regulated by the Federal Communications Commission (FCC) [9].

Fig. 1 shows a simplified diagram of the transcutaneous power flow and various losses along the way as well as the inductive link circuit model schematic. L_1 is the primary coil that is attached to the skin from outside of the body and L_2 is the secondary coil that is implanted under the skin flap often with the rest of the implant electronics. In the case of cochlear implants a pair of permanent magnets, one in the center of each coil, aligns and holds them together. Coil windings have distributed parasitic resistance and capacitance associated with them, which are shown as lumped elements, (R_{S1}, R_{S2}) and (C_{P1}, C_{P2}), in Fig. 1(b). Capacitors C_{S1} and C_R are usually added to the circuit to form a pair of resonance LC-tank circuits with L_1 and L_2, respectively.

The largest power loss usually takes place in the primary coil parasitic resistance R_{S1} followed by R_{S2} and the power conditioning blocks within R_L on the implant side. The latter may

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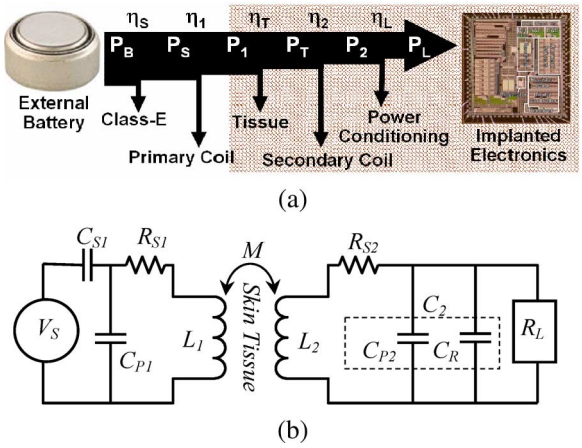


Fig. 1. (a) Power flow diagram in a transcutaneous inductive power transmission link from the external battery to implanted electronics. (b) Simplified schematic diagram of the inductive link with lumped equivalent circuit elements.

however deem to be more important because it is within the tissue [7]. There is also power loss within the external ac source, V_S, which is often an efficient class-E power amplifier [10]. The power loss within the surrounding tissue can be ignored if the operating frequency is chosen below 20 MHz or so $(\eta_T \approx 1)$ [11]. Therefore, it is fair to say that the overall power transmission efficiency, $\eta = \eta_S\eta_1\eta_T\eta_2\eta_L$, is often dominated by $\eta_{12} = \eta_1 \cdot \eta_2$, which we will focus on throughout the rest of this paper. It should also be pointed out that all efficiencies are functions of the inductive link operating frequency, $\omega = 2\pi f$, which is also known as the power carrier [12].

Design and optimization of efficient inductive power transmission links have been well studied over the last few decades [4], [13]–[16]. More recently there have been a number of publications proposing new approaches to the same optimization problems [17]–[21]. A summary of these studies in Section II shows that the coils mutual inductance and quality factor, $Q_1 = \omega L_1/R_{S1}$ and $Q_2 = \omega L_2/R_{S2}$, are the most important parameters affecting η_{12}. It is also well known from electromagnetics that M, L_1, and L_2 are dependant on the coils geometries, which in general terms can also include their relative distance, orientation, and number of turns. Hence, we can conclude that the coils geometries are the most important factors in defining the link power efficiency.

Previous designs have been mostly based on coils made of filament wires in the form of a single or multiple individually insulated strands. The latter type, which is also known as Litz wire, helps in reducing the skin-loss resistive effects especially at higher frequencies by increasing the circumferential area of the wire [22]. Wire-wound coils, however, cannot be batch-fabricated or reduced in size without the use of sophisticated machinery. Therefore, the shape and geometry of the coils used in the next generation of high power implantable devices is more likely to be planar and lithographically defined in one or multiple layers on rigid or flexible substrates similar to printed circuit boards (PCB). Printed spiral coils (PSC) offer more flexibility in optimizing their geometry and aspect ratio, deeming them attractive for implantation under the skin or within the epidural space. They can also conform to the outer body or brain surface curvature if fabricated on thin flexible substrates such as polyimide [23]. Rigid hermetically sealed PSCs can also be fabricated on silicon chips or low temperature co-fired ceramics (LTCC) using micromachining techniques [24], [25].

When dealing with PSCs, the design procedures that are devised for coils made of 1-D filament wires are only good for finding the optimal lumped values for the inductive link circuit models, shown in Fig. 1(b). They are not comprehensive enough to predict the intertwined effects of the distributed inductive, resistive, and capacitive elements on power efficiency when dealing with 3-D PSCs. Further, the previous methods do not take into account many of the design constraints that are dictated by implantable device application or PSC fabrication technology. Therefore, a new design methodology is needed to find all the parameters associated with the geometries of the planar PSCs and maximize η_{12}. Since the closed form equations governing the electromagnetic fields and parasitics of 3-D conductors rapidly become complicated, it becomes necessary to take advantage of the available simulation tools as part of the design methodology and validate the design outcome.

Even though PSCs have been used quite widely in radio frequency identification (RFID) applications, there has been little research on optimizing the geometry of these coils in order to maximize their power transmission efficiency [12], [19]. This is probably because most RFID applications are extremely low power (data storage and retrieval) and less size constrained compared to high power neuroprosthetic applications. Shah *et al.* derived some general guidelines from experimental data [23]. However, they stopped short of a well-defined design methodology supported by theoretical foundation and validated by simulations and experiments.

In this paper, we provide a procedure for designing the geometries of a pair of lithographically defined single layer planer spiral coils that optimizes their mutual inductance and quality factors in a way that η_{12} is maximized. The design procedure also takes into account the major design constraints imposed by regulations, application, and PSC fabrication technology. We limited our design to single layer PSCs even though many fabrication processes allow using multilayer conductors. Because the PSC internal parasitic capacitance of multilayer PSCs is much larger than single layer and it has a significant effect on reducing the self-resonance frequency (SRF) of the PSC, which in turn limits the power carrier frequency, as can be seen in our design examples.

We have used closed-form equations in MATLAB (MathWorks, Natik, MA) in combination with HFSS (Ansoft, Pittsburgh, PA) to find the optimal coil geometries. However, any other field solver can also be used for this purpose [26]. We have also fabricated a number of PSCs, designed through this procedure, on FR4 PCB and characterized them to validate our PSC design technique.

In the next section we have briefly reviewed the theoretical design equations followed by the design procedure and simulation results in Section III. Measurement results are included in Section IV followed by concluding remarks.

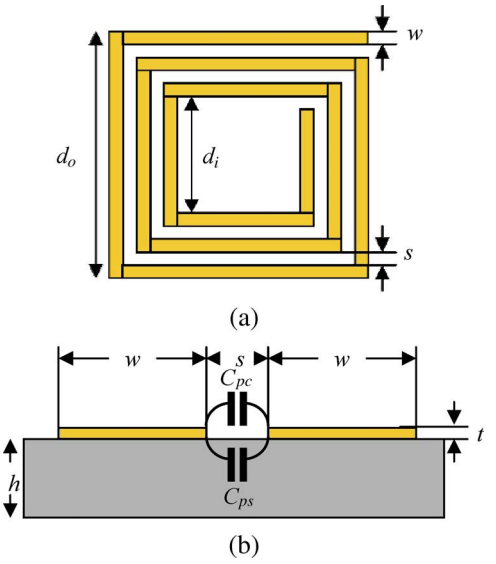


Fig. 2. Geometrical parameters of a square-shaped printed spiral coil. (a) Top view. (b) Cross section of a pair of parallel conductors showing the parasitic capacitor components within the insulator and substrate.

II. Inductive Coupling and Power Efficiency Theory

A. Planar Spiral Coils Quality Factor

The ratio between the magnetic flux generated by a current carrying conductor and the current passing through it indicates its self-inductance. Several closed-form equations have been proposed to approximate L in PSCs [27]–[30]. We adopted (1) from [30] for square coils shown in Fig. 2(a)

$$L = \frac{1.27 \cdot \mu_0 n^2 d_{\text{avg}}}{2}\left[\ln\left(\frac{2.07}{\varphi}\right) + 0.18\varphi + 0.13\varphi^2\right] \quad (1)$$

$$\varphi = \frac{d_o - d_i}{d_o + d_i} \quad (2)$$

where n is the number of turns d_o and d_i are the outer and inner diameters of the coil, respectively, $d_{\text{avg}} = (d_o + d_i)/2$, and φ is a parameter known as fill factor, which changes from 0, when all the turns are concentrated on the perimeter like filament coils, to 1, when the turns spiral all the way to the center of the coil.

To find the total parasitic dc resistance of the PSC, we need to know the length of the conductive trace l_c, resistivity of the conductive material ρ_c, and its thickness t_c

$$l_c = 4 \cdot n \cdot d_o - 4 \cdot n \cdot w - (2n+1)^2(s+w) \quad (3)$$

$$R_{\text{dc}} = \rho_c \frac{l_c}{w \cdot t_c} \quad (4)$$

where w and s are the line width and spacing, respectively.

The skin effect will increase the coil ac resistance at higher frequencies and should be taken into account

$$R_S = R_{\text{dc}} \cdot \frac{t_c}{\delta \cdot (1 - e^{-t_c/\delta})}, \quad \delta = \sqrt{\frac{\rho_c}{\pi \cdot \mu \cdot f}}, \quad \mu = \mu_r \cdot \mu_0 \quad (5)$$

where δ is the skin depth, μ_0 is the permeability of space, and μ_r is the relative permeability of the conductor [31]. Thus, the quality factor of the PSC without its parasitic capacitance can be found by substituting (1)–(5) in $Q = \omega L / R_S$.

We adopted a semi-empirical approach in finding the parasitic capacitance of the PSC using a combination of theoretical, simulation, and measurement results [32]. A parallel plate parasitic capacitor forms between the spiral conductor sidewalls, shown in Fig. 2(b) cross section, along the spiral gap, shown in Fig. 2(a). The length of the gap is slightly shorter than the length of conductor and can be found from

$$l_g = 4(d_o - w \cdot n)(n-1) - 4s \cdot n(n+1). \quad (6)$$

There are two types of insulating materials affecting this capacitance. One is air or the coating insulator that fills the gap between adjacent traces. The other is the PSC substrate, which could be ceramic, polyimide, or FR4. Therefore, we divided C_p into C_{pc} and C_{ps} components

$$C_P = C_{pc} + C_{ps} \approx (\alpha\varepsilon_{rc} + \beta\varepsilon_{rs})\varepsilon_0 \frac{t_c}{s} l_g \quad (7)$$

where ε_{rc} and ε_{rs} are the relative dielectric constants of the coating and substrate materials, respectively. We empirically found that in the case of air and FR4, $(\alpha, \beta) = (0.9, 0.1)$. From insulator characteristic tables, $(\varepsilon_{rc}, \varepsilon_{rs}) = (1, 4.4)$ [33].

Considering that R_S is in series with L and C_P is in parallel with both [see Fig. 1(b)], the overall impedance and quality factor of a PSC can be found from (8) and (9), respectively

$$Z = \frac{R_S + j\omega L}{1 - \omega^2 L C_P + j\omega R_S C_P} \quad (8)$$

$$Q = \frac{\omega L - \omega\left(R_S^2 + \omega^2 L^2\right) C_P}{R_S} \approx \frac{\omega L}{R_S} \text{ for small } C_P \text{ or low } f. \quad (9)$$

B. Coils Mutual Inductance

A PSC can be considered a set of concentric single-turn coils with shrinking diameters, connected in series. Therefore, once we find the mutual inductance between a pair of single-turn coils in parallel planes, the overall M can be found by summing the partial mutual inductance values between every turn on one coil and all the turns on the other coil. Using Maxwell equations, M_{ij} between a pair of parallel circular single-turn coils at radii r_{i} and r_{j} can be found from

$$M_{ij} = \mu\pi\sqrt{r_i \cdot r_j} \int_0^\infty J_1\left(x\sqrt{\frac{r_i}{r_j}}\right) J_1\left(x\sqrt{\frac{r_j}{r_i}}\right) \times J_o\left(x\frac{\gamma}{\sqrt{r_i \cdot r_j}}\right) . \exp\left(-x\frac{D}{\sqrt{r_i \cdot r_j}}\right) dx \quad (10)$$

where D is the relative distance between the two coils, μ is the permeability of the medium, and γ is the lateral misalignment [15], [34]. J_0 and J_1 are the Bessel functions of the zeroth

and first order, respectively. For perfectly aligned coaxial coils, where $\gamma = 0$, (10) can be simplified to

$$M_{ij} = \frac{2\mu}{\alpha}\sqrt{r_i \cdot r_j}\left[\left(1 - \frac{\alpha^2}{2}\right)K(\alpha) - E(\alpha)\right] \quad (11)$$

$$\alpha = 2\sqrt{\frac{r_i \cdot r_j}{(r_i + r_j)^2 + D^2}} \quad (12)$$

where $K(\alpha)$ and $E(\alpha)$ are the complete elliptic integrals of the first and second kind, respectively [35]. By adding the partial mutual inductances between every two turns on a PSC pair

$$M = g\sum_{i=1}^{n_1}\sum_{j=1}^{n_2} M_{ij}(r_i, r_j, D) \quad (13)$$

where g is a factor dependent on the shape of the PSC. Even though the area of a square-shaped coil with a side length of $2r$ is 27% larger than a circular coil with equal diameter, we empirically found that M between a pair of square-shaped PSCs is only 10% higher than a pair of similar circular PSCs. Thus, $g \approx$0.95, 1.0, and 1.1 for a pair of hexagonal, circular, and square-shaped PSCs with equal diameters, respectively.

C. Inductive Link Efficiency

It can be shown mathematically that the highest voltage gain and efficiency across an inductive link can be achieved when both LC-tanks are tuned at the link operating frequency, $\omega = \omega_0 = 1/\sqrt{L_1C_1} = 1/\sqrt{L_2C_2}$. This is the first set of constraints in choosing L and C values in Fig. 1(b). The power delivered to the primary LC-tank, P_S, divides between R_{S1}, which is wasted as heat, and the secondary loading, which is reflected onto the primary through M. To simplify the efficiency equations, M is usually normalized w.r.t. L_1 and L_2 by defining k as the coils coupling coefficient [36]

$$k = M/\sqrt{L_1L_2}. \quad (14)$$

In practice, the secondary coil is always loaded as shown in Fig. 1 by R_L. The loaded secondary quality factor at resonance can be found from [12]

$$Q_L = \frac{1}{\frac{R_{S2}}{\omega L_2} + \frac{\omega L_2}{R_L}} = \frac{1}{R_{S2}\cdot\sqrt{\frac{C_2}{L_2}} + \frac{1}{R_L}\cdot\sqrt{\frac{L_2}{C_2}}} \quad (15)$$

where $Q_L \approx \omega_0 R_L C_2$ if $R_L \gg R_2$. If the nominal R_L is known, it is also possible to find the L_2 value that maximizes Q_L by differentiating (15) w.r.t. L_2

$$L_2 = \frac{\sqrt{R_{S2}R_L}}{\omega} \Rightarrow Q_{L\max} = \frac{1}{2}\sqrt{\frac{R_L}{R_{S2}}}. \quad (16)$$

Considering the above points, Ko *et al.* showed that [4]

$$\eta_1 = \frac{P_1}{P_S} = \frac{k^2Q_1Q_L}{1 + k^2Q_1Q_L}. \quad (17)$$

On the secondary side, there is a power division between R_{S2}, which is wasted as heat, and R_L. To find η_2, R_{S2} can be transformed to its parallel equivalent at resonance [37]

$$R_{PS2} = \frac{(\omega_0 \cdot L_2)^2}{R_{S2}}. \quad (18)$$

Since R_{PS2} and R_L both receive the same voltage across the tank, it is easy to verify that

$$\eta_2 = \frac{P_L}{P_2} = \frac{R_{P2}}{R_{P2} + R_L} = \frac{Q_2}{Q_2 + Q_L}. \quad (19)$$

Therefore, from (17) and (19), we can demonstrate the factors that are most effective in the link power efficiency [21]

$$\eta_{12} = \eta_1 \cdot \eta_2 = \frac{k^2Q_1Q_L}{1 + k^2Q_1Q_L} \cdot \frac{Q_L}{Q_2 + Q_L}. \quad (20)$$

In PSCs, most aforementioned parameters are interrelated. For example, increasing the number of turns for each coil without changing the coil outer diameter can increase L and k. However, it may decrease Q by increasing R_S due to increased l and reduced w. Therefore, there are optimal PSC geometries that would maximize η_{12}. Parameters such as substrate loss and eddy current also play a role, which are not included in detail due to their small effects. Another parameter that has not been included is the V_S output resistance, which is small in class-E amplifiers and should be considered in η_S [10].

III. Design Procedure

An iterative design procedure has been depicted in this section which starts with a set of design constraints and initial values, and ends with the optimal PSC pair geometries. HFSS simulations have been used for fine tuning and verifying the values suggested by theoretical calculations. MATLAB-produced 3-D curves demonstrate the changes in η_{12} when geometrical parameters change in a wide range. By sweeping numerous parameters included in (1)–(20), even those that are not directly utilized in our optimization procedure, such as PSC misalignments in (10), the designer can get a good sense of how to make necessary compromises and changes to achieve a satisfactory performance.

Step 1: Applying Design Constraints: There are a set of parameters affecting the wireless link efficiency which are imposed by other factors related to the implantable device application or fabrication technology. The former usually defines the overall size constraints depending on where the implant will be located inside the body. The latter indicates the minimum size features that result in acceptable yield in manufacturing. Table I summarizes a number of these parameters and their exemplary values in our design for a cortical visual prosthesis [23], [38], [39].

The power carrier frequency f has a significant effect on the efficiency and optimal geometry of the PSCs. In order to demonstrate its effects, in the next few steps we have followed the iterative procedure for two different operating frequencies, 1 and 5 MHz. The difference between the final design outcomes shows the importance of f and the efficacy of the proposed design method.

TABLE I
DESIGN CONSTRAINS IMPOSED BY APPLICATION AND FABRICATION TECHNOLOGY

Parameter	Symbol	Design Value
Implanted coil outer diameter	d_{o2}	20 mm
Minimum coil inner diameter*	d_{imin}	0 or 8 mm
Coils relative distance	D	10 mm
Link operating frequency	f	1 and 5 MHz
Secondary nominal loading	R_L	500 Ω
Minimum conductor width	w_{min}	150 µm
Minimum conductor spacing	s_{min}	150 µm
Conductor thickness	t_c	38 µm**
Conductor material properties	ρ, μ_{rc}	~17 nΩm, ~1**
Substrate thickness	t_s	1.5 mm
Substrate dielectric constant	ε_{rs}	4.4 (FR4)

* Depending on whether a chip or magnet is going to be placed in the center of the PSC or not.
** 1-oz copper on FR4 printed circuit board.

Step 2: Initial Values: A set of initial values need to be selected before starting the iterative optimization process. In our earlier work [40], we found that the optimal fill factor for a pair of identical spiral filament coils is $\varphi = 0.43$. For $d_{o2} = 20$ mm, this leads to $d_{i2} = 8$ mm. The optimal value for d_{o1} depends on the coils relative distance, D, which is usually not fixed and has a certain range. Therefore, depending on the application and design constraints, D can be chosen to be the nominal distance where the coils are for most of the time during normal operation or the maximum distance, which indicates the worst case power transmission.

In a single-turn circular filament coil with radius r, it can be shown that the field strength, H, along the axis at distance x from the coil center can be found from [12]

$$H(x,r) = \frac{I \cdot r^2}{2\sqrt{(r^2+x^2)^3}}. \tag{21}$$

Differentiating (21) w.r.t. r, shows that for $r = x \cdot \sqrt{2}$, H will be maximized. Therefore, a good choice for d_{o1} would be

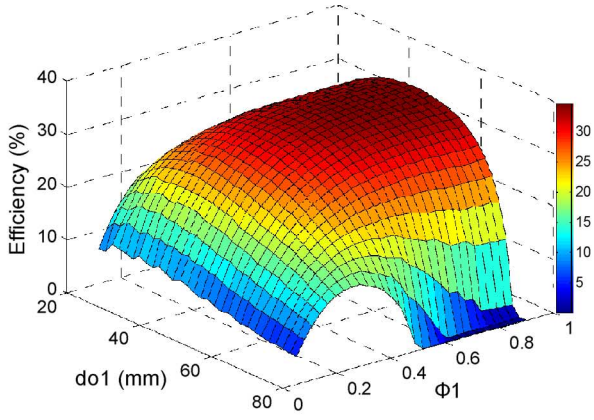
$$d_{o1} = D \cdot 2\sqrt{2}. \tag{22}$$

In our design example, $D = 10$ mm and $d_{o1} = 28$ mm.

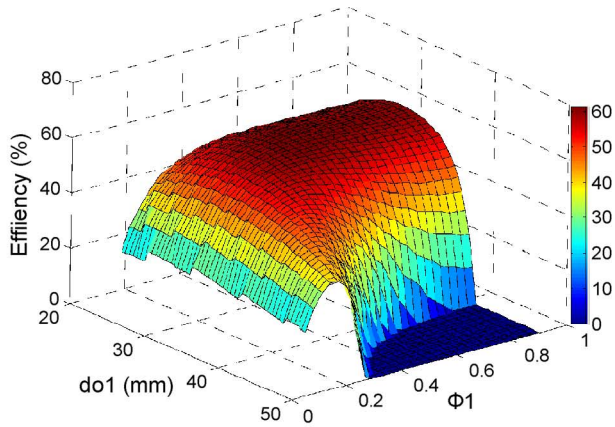
The number of turns in a PSC is defined based on d_o, w, and s, as opposed to 1-D filament coils, which have no limits. A larger number of turns generally results in larger L, Q, M, and R_S. We initiate w and s with the minimum values permitted by the fabrication technology, $(w, s) = (w_{\min}, s_{\min})$, considering the fact that this choice may not be optimal. Increasing w in the subsequent steps is likely to improve η_{12} since it can reduce R_S. However, since increasing s results in decreasing w or n, it should only be considered if the SRF of the PSC, $f_{sr} = 1/2\pi\sqrt{L \cdot C_P}$, approaches f.

Step 3: Size and Fill Factor of Primary PSC: To optimize η_1 component of η_{12} in the primary PSC, k and Q_1 need to be considered together according to (17). Plugging the initial values from Steps 1 and 2 in (1)–(20), we found η_{12} while sweeping d_{o1} and φ_1 in a wide range around their initial values. Since s_1 and w_1 are constants in this step, changing φ_1 directly affects n_1 according to

$$n_1 = \frac{d_{o1}}{(s_1 + w_1)} \cdot \frac{\varphi_1}{(1+\varphi_1)}. \tag{23}$$



(a)



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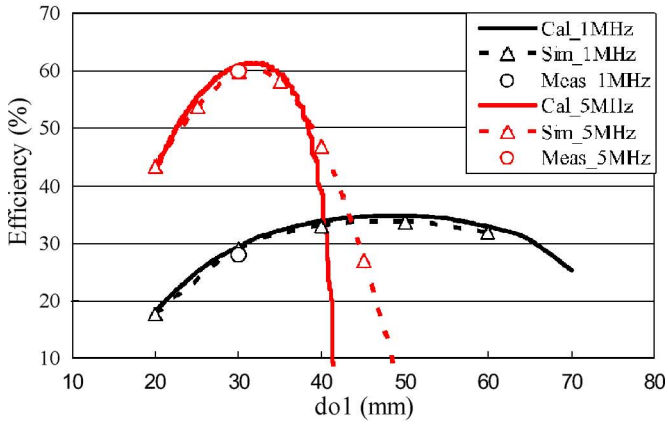

(c)

Fig. 3. Optimizing the size and fill factor of the primary PSC while w and s are at their minimum. (a) η_{12} versus d_{o1} and φ_1 at 1 MHz. (b) η_{12} versus d_{o1} and φ_1 at 5 MHz. (c) Calculated, simulated, and measured efficiency versus d_{o1}.

For $f = 1$ MHz, it can be seen in Fig. 3(a) that the best choice for d_{o1} would be 48 mm and η_{12} almost flattens for $\varphi_1 > 0.8$. This indicates that the turns very close to the center of the PSC do not help with improving the efficiency. If we set $\varphi_1 = 0.8$, then $d_{i1} = 5$ mm and $n_1 = 71$. Assuming $d_{i1} = d_{\text{imin}} = 8$ mm results in $n_1 = 68$ and $\eta_{12} = 34.7\%$, which should improve once w_1 and secondary PSC are optimized. Similarly, when $f = 5$ MHz, the 3-D surface in Fig. 3(b) reaches its maximum at $d_{o1} = 32$ mm and η_{12} flattens for $\varphi_1 > 0.49$. Setting $\varphi_1 = 0.49$ results in $d_{i1} = 11$ mm, $n_1 = 36.5$, and $\eta_{12} = 66.6\%$.

Fig. 3(c) compares the simulated and calculated efficiencies versus d_{o1}. Calculated results at low frequency (1 MHz) are very accurate because conductive traces are narrow (150 μm) and close to filament wires. Narrow traces also reduce the effects of eddy currents. At higher frequencies (5 MHz), the effects of PSC parasitic capacitance become more significant and (5) overestimates C_P for larger diameters. The peak efficiency is significantly higher at 5 MHz due to higher PSC quality factors. However, η_{12} rapidly drops as L_1 approaches its SRF. The hollow circles at $d_{o1} = 30$ mm are the measured efficiency values, using PSC11 and PSC21 in Table III to form a link, which validate calculation and simulation results.

Step 4: Fill Factor and Line Width of Secondary PSC: After temporarily resolving the geometry of the primary PSC in Step 3, we focus on the secondary PSC. Considering that d_{o2} is already specified based on the implant size in Step 1, we sweep φ_2 around its nominal value and increase w_2 from $w_{2\min}$, while calculating η_{12} from (1)–(20). It can be seen from Fig. 4(a) that in our exemplary design at 1 MHz the peak is slightly below $w_{2\min}$. Since the fabrication technology does not allow any thinner conductor, we chose $w_2 = w_{2\min}$ and $\varphi_2 = 0.78$, which corresponds to $n_2 = 31$ turns. This yields $\eta_{12} = 35\%$. Substituting φ_2 in (2) gives $d_{i2} = 2.5$ mm, which is smaller than $d_{i\min}$. If we choose $d_{i2} = 8$ mm to leave room for a chip or magnet in the center of the secondary PSC, φ_2, n_2, and η_{12} reduce to 0.43, 20, and 34.8%, respectively. At 5 MHz, the secondary PSC geometries that result from Step 4 are $d_{i2} = 8$ mm, $w_2 = 450$ μm, $\varphi_2 = 0.43$ mm, and $n_2 = 10$, which yield $\eta_{12} = 75.1\%$, as shown in Fig. 4(b).

Fig. 4(c) compares cross-sections of Fig. 4(a) and (b) curves at $\varphi_2 = 0.43$ with simulated values of η_{12} versus w_2 using HFSS. It can be seen that the theoretical and simulated values are very close with maximum efficiencies of 33.2% and 75.12% at 1 and 5 MHz, respectively.

Step 5: Size and Line Width of Primary Coil: In this step we return back to the primary PSC and increase the conductor width, w_1, towards its optimal value while providing room for this change by increasing d_{o1}. Increasing w_1 is likely to increase η_{12} by reducing R_{S1} and increasing Q_1. However, it also requires larger d_{o1} and may reduce k by deviating from (22) or by reducing n_1. Fig. 5(a) shows how an optimal point with $\eta_{12} = 41.2\%$ is reached at 1 MHz when $w_1 = 2410$ μm and $d_{o1} = 69$ mm. Substituting these values in (23) along with $d_{i1} = 8$ mm from Step 3 gives $\varphi_1 = 0.78$. Following the same steps at 5 MHz results in the 3-D curve shown in Fig. 5(b) with a peak at $w_1 = 2890$ μm and $d_{o1} = 70$ mm, yielding $\varphi_1 = 0.43$ and $\eta_{12} = 82.7\%$.

Fig. 5(c) compares cross-sections of Fig. 5(a) and (b) at $d_{o1} = 70$ mm, with simulated values of η_{12} versus w_1. Once again there is a good agreement between calculated and simulated values especially in the midrange. The difference is higher at the higher end of these curves for wider conductors because the effects of eddy currents become more prominent, particularly at higher frequencies. HFSS considers those effects while our equations in Section II do not. The simulation versus calculation difference also increases at the lower end of these curves for narrower conductors because of the inaccuracies of (7) and the effects of fringe and substrate parasitic capacitors, which are ignored in calculations but not in simulations.

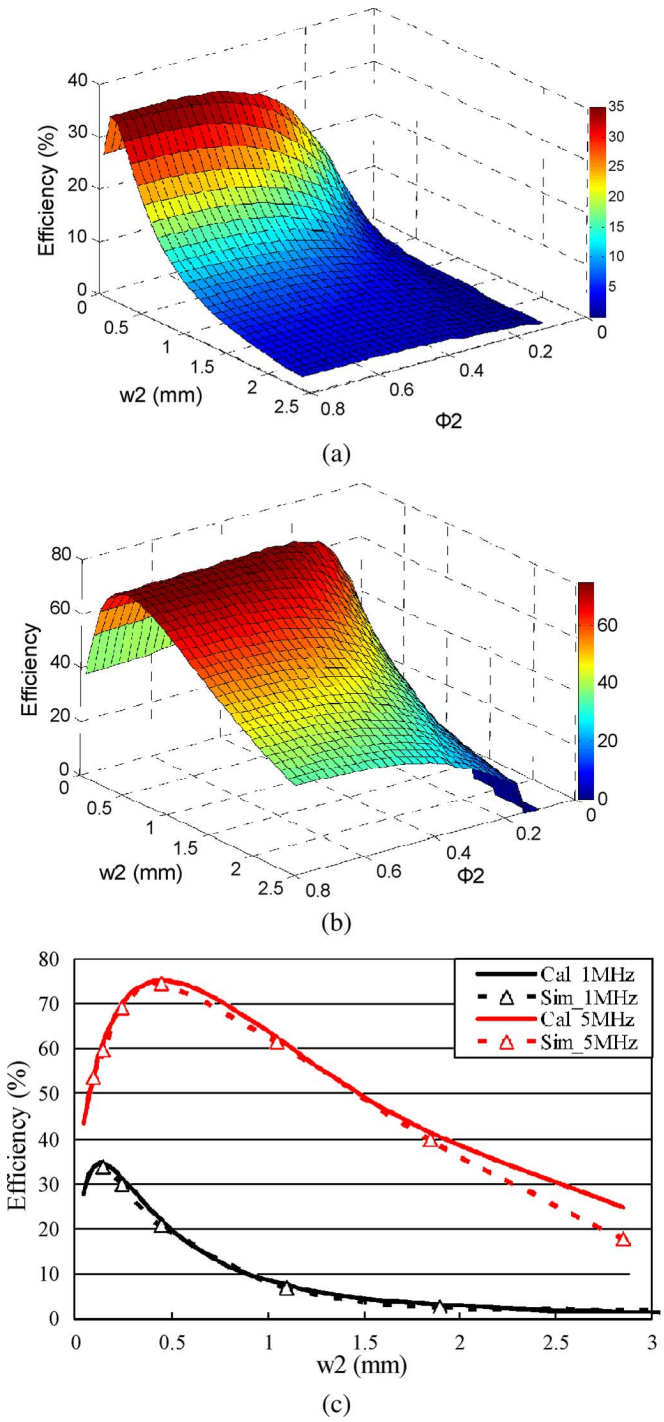

Fig. 4. Optimizing the fill factor and conductor line width of the secondary PSC. (a) η_{12} versus w_2 and φ_2 at 1 MHz. (b) η_{12} versus w_2 and φ_2 at 5 MHz. (c) Comparison between calculated and simulated η_{12} versus w_2 when $\varphi_2 = 0.43$.

Step 6: Iteration by Going to Step 3: The PSC geometries from Step 5 significantly improve η_{12} compared to the initial values. However, further improvement is possible by iterating through Steps 3–5. Iterations can continue until improvement in η_{12} per iteration is less than 0.1%. Table II depicts the final optimized values of the design examples in Table I after several iterations. Fig. 6 summarizes the iterative PSC design procedure in a flowchart.

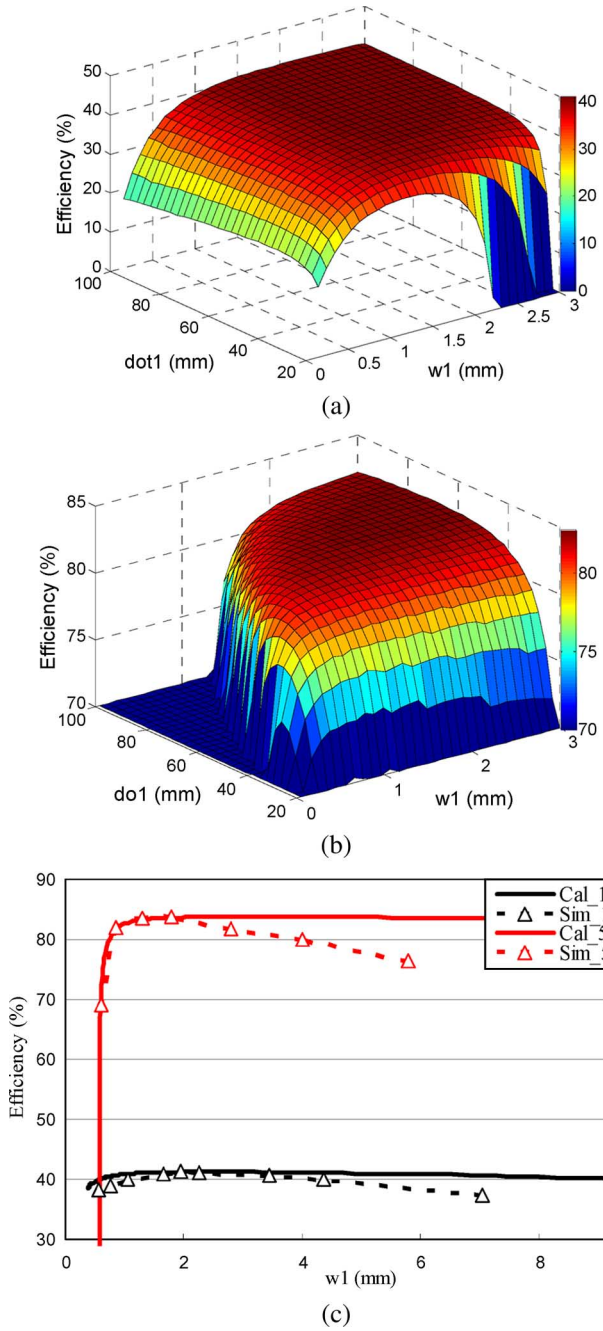

Fig. 5. Optimizing the size and conductor line width of the primary PSC. (a) η_{12} versus d_{o1} and w_1 at 1 MHz. (b) η_{12} versus d_{o1} and w_1 at 5 MHz. (c) Comparison between calculated and simulated η_{12} versus w_1 when $d_{o1} = 70$ mm.

TABLE II
OPTIMIZED GEOMETRIES FOR PSC PAIR DESIGN EXAMPLES

PSC Parameter	f = 1 MHz	f = 5 MHz
d_{o1}	69 mm	70 mm
d_{i1}	8 mm	8 mm
d_{o2}	20 mm	20 mm
d_{i2}	8 mm	8 mm
w_1	2480 µm	3250 µm
w_2	150 µm	250 µm
s	150 µm	150 µm
n_1	12 turns	9 turns
n_2	20 turns	15 turns
φ_1	0.79	0.85
φ_2	0.43	0.43
η_{12} *at D = 10 mm*	41.2%	85.8%

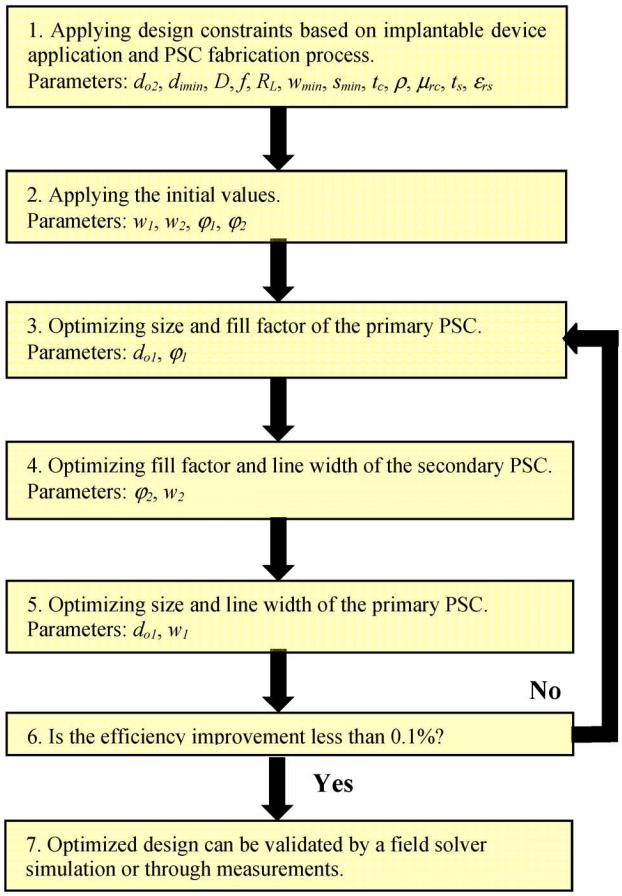

Fig. 6. Iterative PSC design flowchart.

IV. MEASUREMENT RESULTS

Table III shows the geometries and specifications of five square-shaped PSCs that were fabricated using 1-oz copper on FR4 substrates. PSC11 ∼ 14 were used as primaries and formed an inductive link with PSC21 as the secondary. PSC pairs were mounted on Plexiglas sheets using plastic screws, aligned, and held in parallel. Even though these geometries were not exactly the same as the optimal values found in Section III, they could validate the accuracy of our calculations and HFSS simulations, which can be extended to the proposed optimization procedure.

For efficiency measurements we used two setups. First, a network analyzer (Agilent E5071B), shown in Fig. 7(a) connected

TABLE III
SPECIFICATIONS OF THE PSCS USED IN MEASUREMENTS

Parameter	PSC11	PSC12	PSC13	PSC14	PSC21
Shape	square	square	square	square	square
d_o (mm)	30	30	40	40	20
d_i (mm)	8	6.6	8	6	8
φ	0.58	0.58	0.67	0.67	0.43
n (turns)	37	13	32	17	20
w (µm)	150	750	250	750	150
s (µm)	150	150	250	250	150
L (µH)	29.38	3.36	26.56	6.88	7.73
R_S (Ω)	11.95	0.63	6.81	1.36	5.02
SRF (MHz)	11.6	52.7	13.2	28.2	24.5

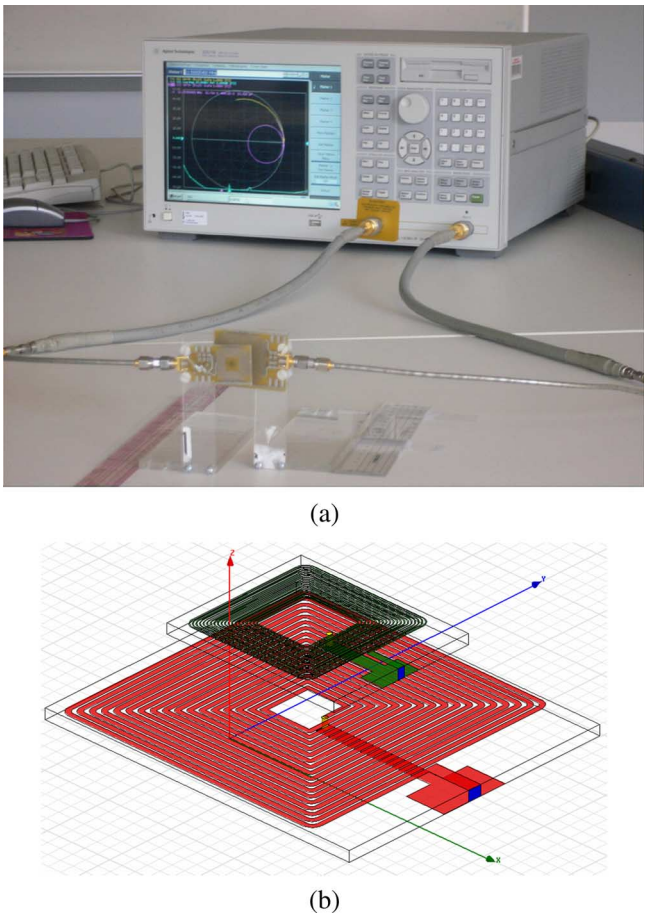

Fig. 7. (a) Experimental setup for measuring the S-parameters between a pair of PSCs using a network analyzer. (b) 3-D PSC models constructed in the HFSS full-wave electromagnetic field simulator.

to PSC1x and PSC21 to measure the S-parameters. The S-parameters are converted to Z-parameters [41], which can then be substituted in (14)–(20) to find η_{12}. Second, a circuit similar to Fig. 1(b) was used with a function generator (HP 8111A) driving PSC1x at resonance frequency, f. An oscilloscope (Tektronix DPO 4034) was also connected to one of the PSCs at a time measuring its current and voltage waveforms without violating the wireless link isolation. The transmitted and received powers can then be easily calculated by multiplying these waveforms.

Fig. 7(b) shows 3-D PSC models constructed with the same dimensions as the fabricated ones in the HFSS full-wave electromagnetic field simulator. Fig. 8 shows Q variations versus frequency for PSC13. This is also a comparison between calculated (Section II), simulated (HFSS), and measured (network analyzer) Q values. It can be seen that the results are close and all suggest that the highest Q can be achieved around 5 MHz. At low frequencies Q increases as $\omega L/R$. At high frequencies, however, the skin and loading effects degrade Q according to (5) and (15), respectively.

Fig. 9(a) and (b) compares η_{12} versus D at 1 and 5 MHz, respectively. It can be seen that calculated, simulated, and measured results are in agreement. PSC12 and PSC14, which w_1 is closer to the optimal value in Table II, provide better efficiencies particularly at the nominal $D = 10$ mm.

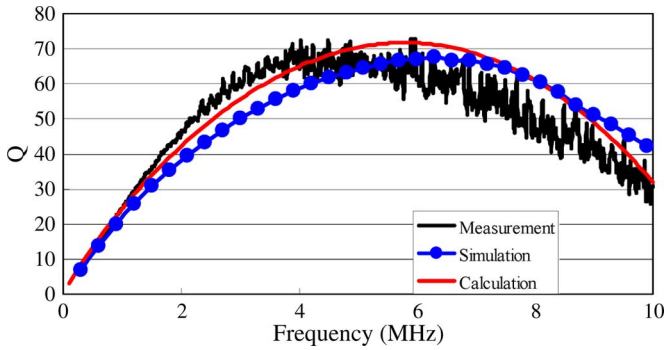

Fig. 8. Comparison between calculated (Section II), simulated (HFSS), and measured (network analyzer) variations of Q versus f for PSC13 in Table III.

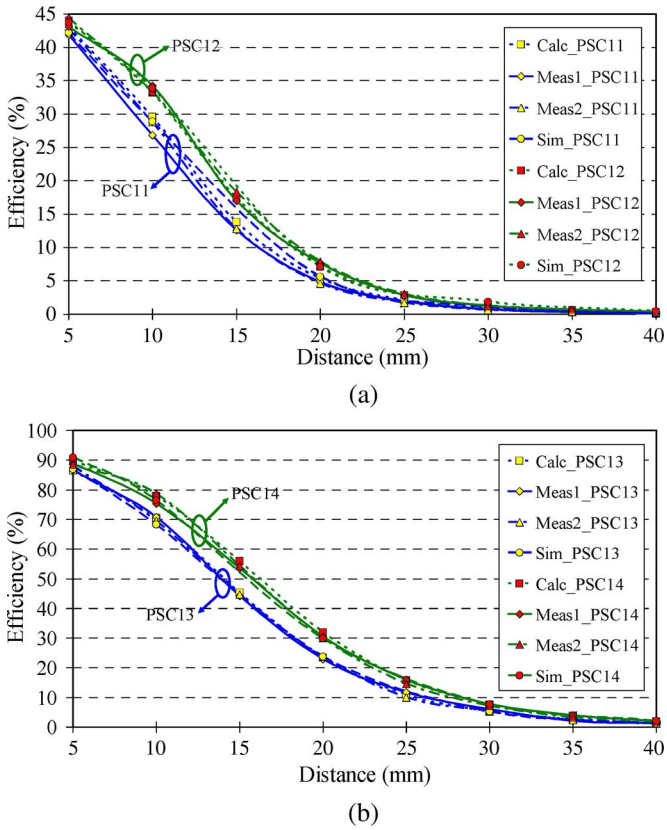

Fig. 9. Efficiency variations with coils relative distance for PSC21 in Table III as secondary and (a) PSC11 and PSC12 as primary at 1 MHz and (b) PSC13 and PSC14 as primary at 5 MHz.

Fig. 10(a) and (b) compares η_{12} versus f for fabricated coils in Table III at $D = 10$ mm. Once again there is a good agreement between calculated, simulated, and measured values particularly at low frequencies. Efficiency is maximized around $4 \sim 5$ MHz mainly because of the high Q of the PSCs at these frequencies, as shown in Fig. 8.

V. Conclusion

We have devised an iterative design procedure to optimize the geometries of a pair of printed spiral coils used in implantable microelectronic devices to maximize the inductive power transmission efficiency between them. Unlike previous design procedures which are mostly based on 1-D filament

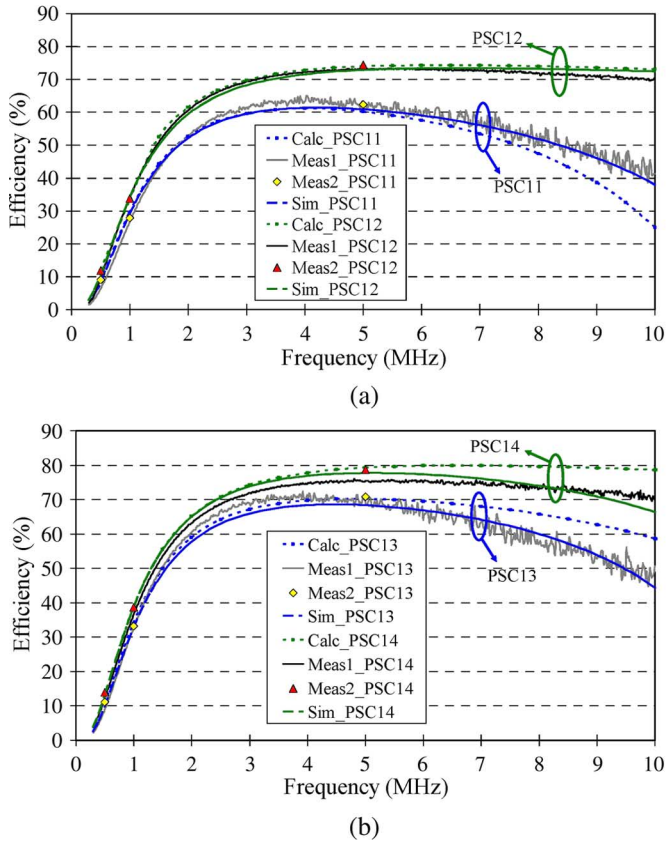

Fig. 10. Efficiency variations with power carrier frequency for PSC21 in Table III as secondary located 10 mm away from (a) PSC11 and PSC12 as primary and (b) PSC13 and PSC14 as primary.

wires, the new method takes into account the effects of the distributed inductive, resistive, and capacitive components simultaneously on the coils quality factors and coupling coefficient and changes the PSC geometries such that the net result would improve the overall power transfer efficiency. Further, since this procedure shows how power efficiency changes when various PSC geometrical parameters vary in a wide range, it allows the designer to make proper compromises to accommodate for other non-geometrical design considerations. The procedure starts with applying the design constraints that are usually imposed by the intended application of the implantable device and PSC fabrication technology. Initial values are also chosen for all PSC geometrical parameters that affect the power efficiency. The next step is optimizing size and fill factor of the primary PSC, followed by fill factor and conductor width in the secondary PSC. Then we return back to the primary side and optimize its size and conductor width. This iteration repeats until the power efficiency reaches its maximum level for the selected operating frequency and the PSCs relative distance.

The PSC design procedure was validated by applying it to design examples for a cortical visual prosthesis at 1 and 5 MHz. We constructed finite element analysis models in HFSS using the optimal geometries and simulated them. We also fabricated several PSC pairs with different geometries on FR4 and measured their coupling coefficient and power efficiency. All calculation, simulation, and measurement results were in close agreement in the desired range of parameters and demonstrated that the proposed iterative PSC design procedure can maximize the power transfer efficiency and provide insight on its changes with PSC geometries. We are now using this PSC design technique in development of a multicarrier inductive wireless link [36], [42].

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