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Design Considerations of Recent Advanced Low-Voltage Low-Temperature-Coefficient CMOS Bandgap Voltage Reference

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Abstract

The design considerations of CMOS bandgap voltage references focusing on low-voltage and low-temperature-coefficient methodologies are discussed in this paper. Some recently reported circuits of bandgap voltage references are included and analyzed. Moreover, a CMOS voltage reference is also addressed.

Introduction

Voltage reference is a pivotal building block in mixed-signal and radio-frequency systems. For example, a generic mixed-signal system, as shown in Fig. 1, has more than one voltage reference due to different voltage reference requirements and also to avoid crosstalk through a single reference circuit. In such a system, a voltage reference is needed for the power-management block, which includes many on-chip DC-DC power converters to provide regulated power. Some other voltage references are utilized in ADCs and DACs, which need high-accuracy reference voltages to provide high-resolution high-speed data conversions even in low supply-voltage conditions.

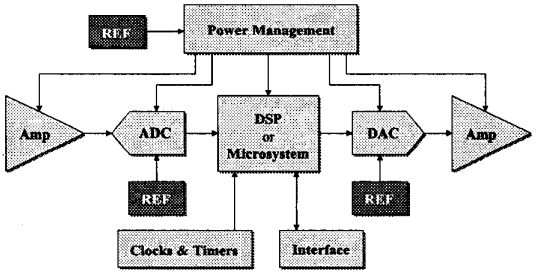

Fig. 1: A generic mixed-signal system.

Undoubtedly, reference-voltage accuracy determines the maximum achievable performance of all IC systems. There are many types state-of-the-art design [1]. Bandgap voltage reference, which was firstly proposed by Widlar [2] and was further developed by Kuijk [3] and Brokaw [4], is the one commonly used in many advanced designs and commercial products since it can provide a predictable reference voltage. Moreover, it is also possible for low voltage and low temperature dependence.

The working principle of a bandgap voltage reference can be illustrated by Fig. 2. Since V_{BE} decreases approximately linear with temperature while V_T increases linearly with temperature, a low-temperature-dependence V_{REF} can be obtained by scaling up V_T and summing it with V_{BE}.

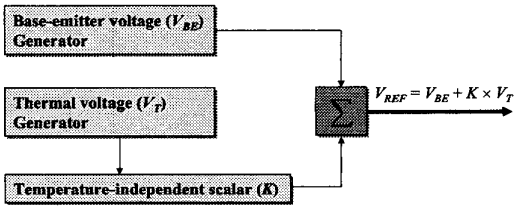

Fig. 2: Concept of bandgap voltage reference.

The above-mentioned concept can be implemented as shown in Fig. 3 [5] by using parasitic vertical BJTs. Current mirrors formed by M1, M2 and M3 enforce branch currents equal to a proportional-to-absolute-temperature (PTAT) I, which is generated by Q1, Q2 and R_1 when $V_A = V_B$ is enforced by a voltage-clamping circuit composed of M4 and M5. Thus, V_{REF} is given by

$$V_{REF} = V_{EB3} + (R_2/R_1)\ln(N)\cdot V_T \qquad (1)$$

The achieved V_{REF} is around 1.205V, which is the value of energy bandgap of silicon. A V_{REF} with low temperature coefficient (tempco) can be easily obtained by optimizing temperature-independent circuit parameters R_2/R_1 and N.

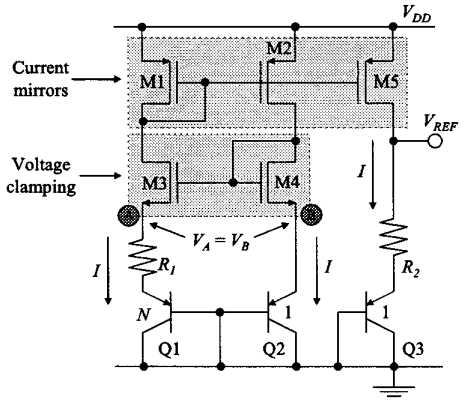

Fig. 3: Simple implementation of bandgap reference.

The previous review reveals the design problems of bandgap voltage reference in a low supply voltage. The intrinsically-defined 1.205-V V_{REF} is one of the limitations. Moreover, a perfect voltage reference should contain no

error. However, there are many sources of error in the voltage reference such as error current from the current mirrors, error voltage from the clamping circuit, as well as device mismatches of Q1-Q2 and R_1-R_2. Undoubtedly, there are many well-developed circuits and layout techniques to minimize the errors. However, low supply voltages limit the available methodologies and cause severe design problems.

Moreover, typical bandgap references have non-zero tempco of typically around 25-50ppm/°C [1]. This is, no doubt, an error of V_{REF}. This error is not significant in the past 5-V and 10-V systems, but is a fatal error in current 1.8-V or even future sub-1-V systems. Solutions have been proposed but are less useful in low-voltage conditions.

In regards to the above-mentioned low-voltage design trends and problems, many novel structures of bandgap reference have been proposed and well-proven by experimental results. Thereby, in this paper, the designs of low-voltage and low-tempco bandgap voltage reference are reviewed and studied. Discussions will not only be on the circuit structures, but some design considerations and design problems due to technology limitations will also be discussed as well. Lastly, a CMOS voltage reference is introduced.

I. Design Challenges and Considerations

The design of voltage reference mainly improves accuracy and rejects errors. Thus, the errors in every part should be minimized by circuit and layout techniques. With reference to Fig. 3, considerations should be focused on BJT-ratio and resistor-ratio matching, current mirror, as well as voltage clamping. These considerations are discussed below.

A. Design Issues on BJT and Resistor

Laser trimming can be used to optimize the performance of bandgap voltage references, but it is a costly procedure. As a result, layouts on both BJTs and resistors should be well planned and designed so that consistent performance can be maintained with minimum need of trimming in mass productions. Better matching can be achieved by a common-centroid layout [6], [7]. In Fig. 4(a), there shows two matched BJTs in a ratio of 1:8 as shown.

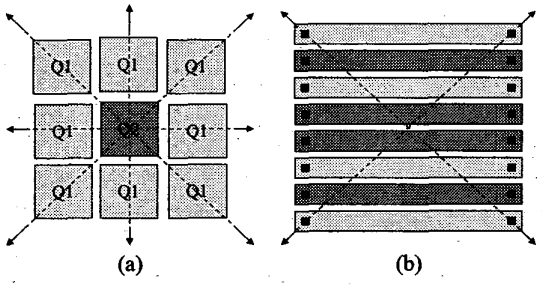

Fig. 4: Layouts of (a) two BJTs (b) two resistors.

In the figure, N = 8 is chosen and all BJTs are placed closely. N, in fact, can be 24, 48 or even 80 as these integers can be used to obtain common-centroid structures. However, a large value of N is not preferred as the separation of devices increases, and this will introduce more errors. Moreover, as shown in (1), there is no significant increase on the ln(N) function when N increases.

For the resistor layout, common-centroid layout should be also used to obtain better matching. Fig. 4(b) shows two resistors with equal values in two layout arrangements. The resistor layout should be arranged in a square-like structure instead of a thin and long structure. Although the structure in Fig. 4(b) provides a very stable resistor ratio including the effect of contact resistances, each resistor must be sufficiently long such that the contact resistances are negligible and cause less influence. Moreover, polysilicon is a better material than diffusion to implement resistors since the minimum separation is shorter and that provides a better matching.

The tempco of V_{REF} is also affected by the materials used to implement the resistors. It is known that the finite tempco of V_{REF} is due to the non-linear behavior of V_{BE} at different temperatures. Tsividis has found that the V_{BE} can be expressed by [8]

$$V_{BE} = V_{GO} + \frac{T}{T_r}\cdot\left[V_{BE}(T_r) - V_G(T_r)\right] + (\eta - \beta)\frac{kT}{q}\ln\left(\frac{T_r}{T}\right) \quad (2)$$

where V_{GO} is the extrapolated bandgap voltage of silicon at 0K, T_r is the reference temperature, η is a constant of less than 4 depending on doping level, and β is the order of temperature dependence of the collector current (i.e. $I_C = I_{CO}T^{\beta}$). The non-linear voltage is due to $T\ln T$ term in (2).

In fact, the current I in Fig. 3 is not a pure PTAT current. When a material with a low tempco is used, (η - β) in (2) becomes smaller and this results in a smaller non-linear voltage. Therefore, polysilicon is a better material than diffusion since its tempco is low [6]. An even better material is high-resistive polysilicon (lightly-doped polysilicon), since it has a negative tempco [6]. Fig. 5 shows different V_{REF}-T plots of different tempcos of resistors. The tradeoff on low-tempco resistors is higher current level at high temperatures, and that implies more power consumption.

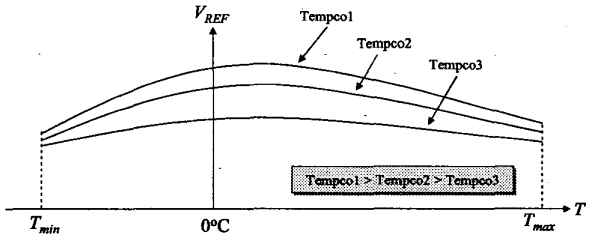

Fig. 5: Reference voltage using different resistor materials.

B. Current Mirror and Voltage Clamping

The current mirror and voltage-clamping circuit formed by M1-M5 in Fig. 3 are not effective at different supply voltages. Although long channel lengths are always used to reduce the channel-modulation effect, there are still problems. When $I_{D1} \neq I_{D2}$ occurs due to $V_{DS1} \neq V_{DS2}$, $V_{GS4} \neq V_{GS5}$ causes an error in the PTAT loop to generate an error-contained V_{REF}. Cascode current mirror is a good choice for reducing error, but a higher supply voltage is needed and therefore it cannot be used in low-voltage design. One solution widely used recently is the error-amplifier-based current mirror. Fig. 6 shows a bandgap circuit using this method.

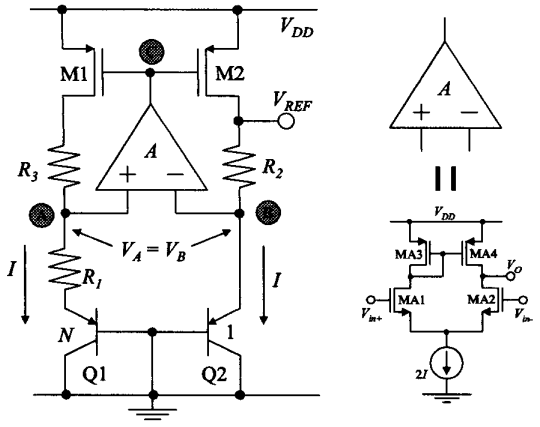

Fig. 6: A CMOS bandgap voltage reference using error-amplifier-based current mirror.

Ideally, the error amplifier has a high voltage gain A, and therefore, $V_A = V_B$ can be achieved. When $R_2 = R_3$, $V_{DS1} = V_{DS2}$ can be easily obtained to provide a very good current matching by M1 and M2. V_{REF} can be generated by this structure without the need of an extra current branch. Both power consumption and errors can be reduced effectively.

In this design, the error amplifier should be simple. The error amplifier shown in Fig. 6 is an excellent choice since there are only two pairs of matched devices to consider on the random offset voltage (V_{OFFR}). In additional to using long-channel-length devices, the bias current used should be the generated PTAT current. MA3 and MA4 should have the same transistor sizes as M1 and M2. By doing so, V_{DS} of both MA3 and MA4 can match very well to reduce the systematic offset voltage (V_{OFFS}) at different temperatures.

Using common sense, a very high-gain error amplifier is preferred. However, it is very difficult to design a simple and high-gain amplifier in a low supply voltage. In fact, the error from error amplifier introduced to bandgap core is due to $V_A \neq V_B$ in practice. This error V_{ERR} is given by

$$V_{ERR} = V_A - V_B = V_{OFFR} + V_{OFFS} + V_{DD}/A \qquad (3)$$

V_{ERR} must be much smaller than $V_{EB2} - V_{EB1} = V_T \ln(N)$. Therefore, a large N is a useful and commonly-used method [7]. The estimation of the required A should be done at the lowest operational temperature such that $V_T \ln(N)$ is the smallest. A correct concept on the design of error amplifier is that A can be low in low-voltage design. When both V_{OFFR} and V_{OFFS} are significant, errors at V_{REF} cannot be reduced by using a high-gain error amplifier. Thus, the main consideration in error-amplifier design is simplicity rather than high voltage gain.

The design of the error-amplifier-based current mirror involves stability issues since there are more than one high impedance nodes at nodes A, B and C in Fig. 6. Stability can be achieved by inserting a compensation capacitor. There are, in fact, three possibilities. One possibility is to add the capacitor between V_{DD} and node C to achieve dominant-pole compensation. The required value is large, and supply noise will couple to the reference circuit easily. Another method is to insert the capacitor between node C and ground. However, this method has a problem on line transient response. The change of V_C cannot respond quickly at rapid changes of V_{DD}. As a result, V_{REF} cannot settle immediately. The best approach is to add the capacitor between nodes A and C to compensate by Miller effect with a small compensation capacitor.

C. Other Considerations on Parasitic Vertical BJTs

C1. Base resistance

The base resistance of parasitic vertical BJT is large [7]. Including its low current gain [7], there will be a large voltage drop (V_B) across the base resistance of the BJT. Therefore, the designed PTAT current cannot be too large. The design guideline is that $V_{EB} >> V_B$, which can be generally achieved by setting $I < 1$mA.

C2. Low current gain

The design equation (1) assumes $I_C \approx I_E$, which is not very valid since the current gain of the parasitic BJT is low (typically lower than 20). A circuit technique can be used to compensate the difference, as shown in Fig. 7.

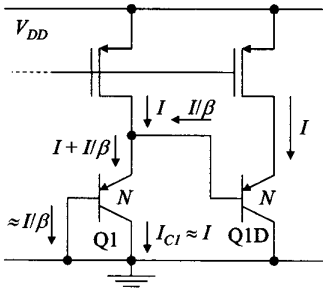

Fig. 7: A circuit for base-current compensation.

An extra transistor Q1D, which has the same emitter area as Q1, is added. According to figure, the extra base current by Q1D is added to form the emitter current of Q1. As a result, $I_{C1} = I$ can be achieved. The drawback is the additional V_{EB} drop which increases the minimum V_{DD}.

Fig. 8 shows an example bandgap voltage reference, which is designed based on some of the previous suggestions.

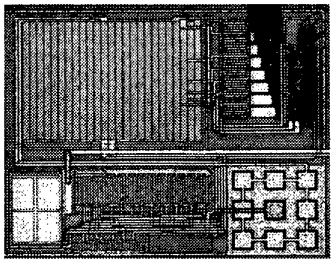

Fig. 8: Micrograph of a bandgap voltage reference.

II. Advanced Bandgap Voltage References with Sub-1-V Supply Operation

The 1.205-V bandgap reference voltage is a hindrance to developing a reference voltage with a sub-1-V supply. Therefore, Banba *et al.* [9] and Leung *et al.* [10] have developed bandgap references with sub-1-V operations. The concept is basically a current-mode method to scale down the bandgap reference voltage by a factor defined by a resistor ratio.

A. *A CMOS Bandgap Reference with Sub-1-V Operation Proposed by Banba et al.* [9]

Fig. 9 shows the circuit proposed by Banba [9]. The reference voltage is formed by two currents I_1 and I_2. For I_1, it is a PTAT current formed by Q1, Q2 and R_1 as given by $I_1 = V_T \ln(N)/R_1$, while I_2 is a current due to V_{EB2} and R_2 as given by $I_2 = V_{EB2}/R_2$. Thus, V_{REF} is given by

$$V_{REF} = (I_1 + I_2)\cdot R_3 = \left(\frac{R_3}{R_2}\right)\cdot\left[V_{EB2} + \left(\frac{R_2}{R_1}\right)\ln(N)\cdot V_T\right] \quad (3)$$

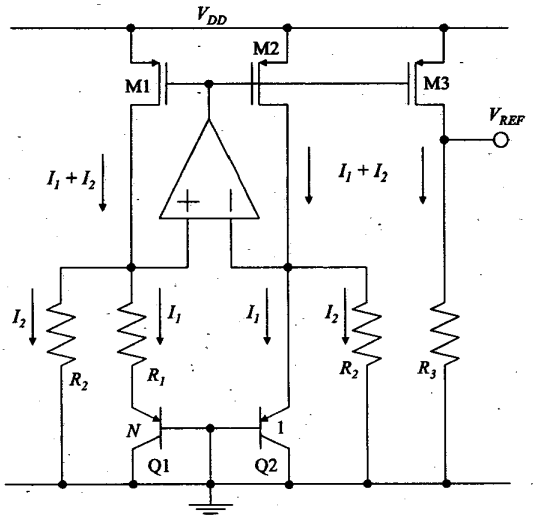

Fig. 9: A CMOS bandgap reference with sub-1-V operation proposed by Banba *et al.* [9].

It is noted that the temperature dependence of the reference voltage can be cancelled by an appropriate R_2/R_1 ratio and N. A resistor ratio of R_3/R_2, which is less than one, is used to scale down the bandgap voltage reference to be less than 1.205V. Therefore, the magnitude of V_{REF} can be adjusted for different applications. In [9], V_{REF} is set to 515mV, which is a good value to achieve $V_{DS1} = V_{DS2} \approx V_{DS3}$ for good current matching at different temperatures. Moreover, the error amplifier shown in Fig. 6 with biasing current from the bandgap core is used to minimize V_{OFFS}. V_{OFFR} can be reduced by a small g_m ratio of MA3 to MA1 and a large transistor size of MA1 and MA2 [5].

B. *A Sub-1-V CMOS Bandgap Voltage Reference without Low Threshold-Voltage Devices by Leung et al.* [10]

The bandgap reference by Banba *et al.* has been implemented in a technology having native NMOSTs (non-standard devices in CMOS technology) to implement an NMOS input stage of the error amplifier. The threshold voltage of NMOSTs should be always much lower than one V_{EB} in the full operational temperature. Thus, one V_{EB}, even at the highest operational temperature (lowest V_{EB}), is therefore sufficiently high to turn on the input stage of the error amplifier for proper operation as shown in Fig. 10(a) (i.e. $V_{EB} > V_{THN} + 2V_{DS(sat)}$). When a PMOS input stage is used, a low supply voltage cannot be achieved easily since the minimum supply voltage, as shown in Fig. 10(b), is given by $V_{DD(min)} = V_{EB} + |V_{THP}| + 2V_{SD(sat)}$. The above implies a low $|V_{THP}|$ is needed.

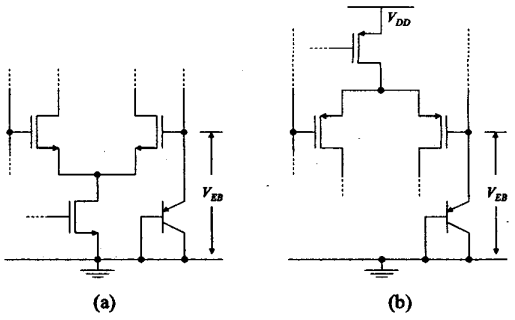

Fig. 10: Bandgap voltage references using (a) an NMOS input stage (b) a PMOS input stage.

Therefore, a circuit technique based on potential divider can be used, as shown in Fig. 11. Instead of enforcing the voltages at E and F directly, the voltages at X and Y are enforced to be equal. As the resistances at the two current branches are set to be equal, the voltages at E and F are equal. It is noted that the voltages at X and Y are given by

$$V_X = V_Y = \left(\frac{R_{2B}}{R_{2A} + R_{2B}}\right)\cdot V_{EB2} \quad (4)$$

An error amplifier with a PMOS input stage can therefore be used. The minimum supply voltage of the bandgap voltage reference is reduced, and V_{REF} of this circuit is

given by

$$V_{REF} = \left(\frac{R_3}{R_2}\right)\cdot\left[V_{EB2} + \left(\frac{R_2}{R_1}\right)\ln(N)\cdot V_T\right] \quad (5)$$

However, the tradeoff of this design is the amplified effect of the offset voltage (V_{OFF}) due to the error amplifier. This relationship can be stated clearly by

$$V_{REF} = \left(\frac{R_3}{R_2}\right)\cdot\left\{V_{EB2} + \left(\frac{R_2}{R_1}\right)\cdot\left[\ln(N)\cdot V_T + V_{ERR1}\right]\right\} \quad (6)$$

where $V_{ERR1} = [(R_{2A} + R_{2B})/R_{2A}]\cdot V_{OFF} > V_{OFF}$ is the increased error voltage due to the offset voltage. This, in practice, can be reduced by using a large value of N in this design. In the design of [10], $N = 64$ is used.

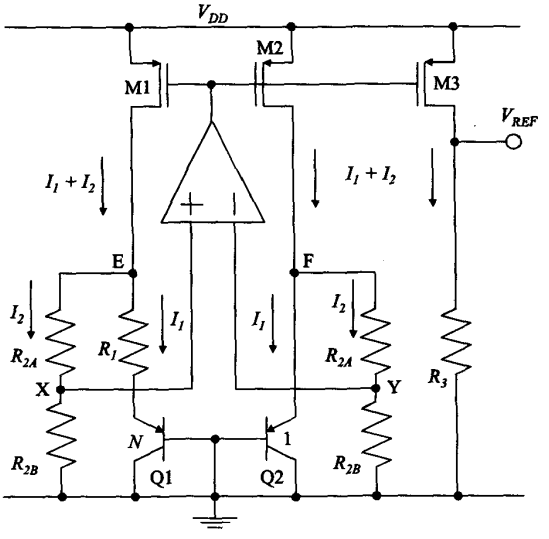

Fig. 11: A sub-1-V CMOS bandgap reference without low threshold-voltage devices proposed by Leung *et al.* [10].

In addition, the bulk-source junctions of M1-M3 are forward-biased such that $|V_{THP}|$ is reduced. The forward bias voltage is set to about 0.3V at the highest operational temperature so that the p-n junction of the p-substrate and N-well will not be turned on. With this scheme, the error amplifier can operate in its high-gain output region to enforce voltages at nodes X and F more closely.

C. *A Bandgap Voltage Reference Using Transimpedance Amplifier Proposed by Jiang et al.* [11]

The minimum supply voltage of the previous bandgap reference structures is limited by the input stage of the voltage-mode error amplifier. A novel structure using transimpedance amplifier in Fig. 12 has been reported [11].

The transimpedance amplifier has a very low input resistance and has a large impedance gain. The internal nodes of the two inputs are set to V_B, which is lower than one V_{EB}.

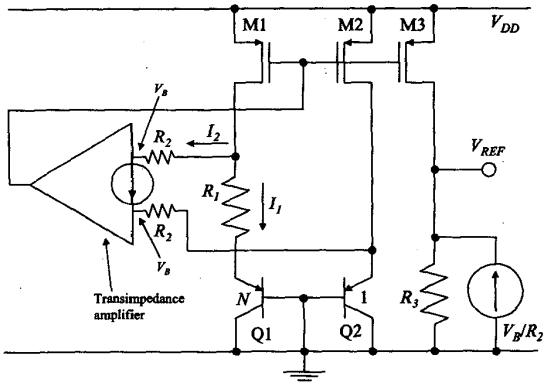

Fig. 12: Bandgap voltage reference using transimpedance amplifier proposed by Jiang *et al.* [11].

As a result, the current I_2 is given by $I_2 = (V_{EB2} - V_B)/R_2$. In addition, the PTAT loop generates a current given by $I_1 = V_T\ln(N)/R_1$. Therefore, the drain currents of M1, M2 and M3 are the sum of I_1 and I_2. With a current source depending on V_B, V_{REF} is given by

$$\begin{aligned} V_{REF} &= (I_1 + I_2 + V_B/R_2)\cdot R_3 \\ &= \left[\frac{V_T\ln(N)}{R_1} + \frac{V_{EB2} - V_B}{R_2} + \frac{V_B}{R_2}\right]\cdot R_3 \\ &= \frac{R_3}{R_2}\cdot\left[V_{EB2} + \left(\frac{R_2}{R_1}\right)\ln(N)\cdot V_T\right] \end{aligned} \quad (7)$$

which is a scalable bandgap reference voltage.

In this design, the matching of devices is very important so that the required node voltages can be set to V_B accurately to reduce the error appearing at V_{REF}. As there is no critical constraint on V_B, it can be any value. Although the reported minimum supply voltage is 1.2V, this approach has a great potential to further reduce the minimum supply voltage.

III. Advanced Structures of Low-Tempco Bandgap Voltage References

In additional to low-voltage bandgap-reference structures, low-tempco structures are also important, especially for high-resolution ADCs and DACs. This is due to the fact that the errors suffering from temperature variations will significantly increase the bit-error rate.

Many novel and creative methods for low-tempco voltage reference have been proposed, including the second-order curvature compensation by Song *et al.* [12] and exponential-curvature compensation by Lee *et al.* [13]. Moreover, low-tempco bandgap reference based on linearized V_{BE} was proposed by Meijer *et al.* [14] and was used by Malcovati *et al.* [15] in their low-voltage BiCMOS bandgap design.

A. A Curvature-Compensated Bandgap Voltage Reference Proposed by Malcovati et al. [15]

The circuit proposed by Malcovati *et al.* is shown in Fig. 12. It can be shown from (2) that different V_{BE} can be obtained by different temperature-dependent collector currents. In this circuit, Q2 is biased by a PTAT current:

$$V_{EB2} = V_G(T_r) + \frac{T}{T_r}\cdot[V_{BE}(T_r) - V_G(T_r)] + (\eta - 1)\frac{kT}{q}\ln\left(\frac{T_r}{T}\right) \quad (8)$$

while Q3 is biased by a temperature-independent current:

$$V_{EB3} = V_G(T_r) + \frac{T}{T_r}\cdot[V_{BE}(T_r) - V_G(T_r)] + \eta\frac{kT}{q}\ln\left(\frac{T_r}{T}\right) \quad (9)$$

A non-linear current I_{NL}, which is the current flowing through R_4 is generated and is given by $I_{NL} = (V_{EB2} - V_{EB3})/R_4 = -V_T\ln(T_r/T)/R_4$.

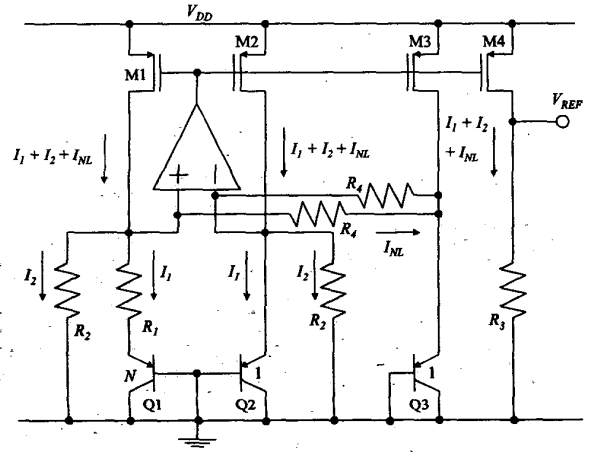

Fig. 12: A curvature-compensated bandgap voltage reference proposed by Malcovati *et al.* [15].

Therefore, V_{REF} is given by

$$V_{REF} = (I_1 + I_2 + I_{NL})\cdot R_3 = \left[\frac{V_T\ln(N)}{R_1} + \frac{V_{EB2}}{R_2} - \frac{V_T\ln\left(\frac{T_r}{T}\right)}{R_4}\right]\cdot R_3 = \left(\frac{R_3}{R_2}\right)\cdot\left[V_{EB2} + \left(\frac{R_2}{R_1}\right)\ln(N)\cdot V_T - \frac{R_2}{R_4}\ln\left(\frac{T_r}{T}\right)\cdot V_T\right] \quad (10)$$

When the easy-control resistor ratio $R_2/R_4 = \eta - 1$, the non-linear voltage in V_{EB2} is cancelled. A theoretical zero-tempo V_{REF} can be obtained. However, it cannot always be achieved due to the non-ideal PTAT and temperature-independent currents from the temperature dependence of resistors. In addition, errors due to mismatch of current mirrors is another problem. However, it is not due to M3 as $V_{DS1} = V_{DS2} = V_{DS3} = V_{DD} - V_{EB}$. Attention should be given, instead, to M4 and V_{REF}. V_{REF} can be set to about one V_{EB} in order to match the V_{DS} of M4 with M1-M3.

B. A Curvature-Corrected Bandgap Reference Based on Temperature-Dependent Resistor Ratio Proposed by Lewis et al. [16], *Audy* [17] *and Leung et al.* [18]

Another method is to implement a bandgap circuit that has a temperature-dependent resistor ratio. This idea can be implemented by the circuit shown in Fig. 13. Both R_1 and R_2 are made of the same material, while R_3 is made of high-resistive polysilicon, which has a negative tempco. Therefore, V_{REF} is given by

$$V_{REF} = V_{EB2} + \left(\frac{R_2}{R1}\right)\ln(N)\cdot V_T + \left(\frac{R_3}{R_1}\right)\ln(N)\cdot V_T \quad (11)$$

T-dependent resistor ratio

Since the non-linear temperature-dependent voltage in V_{EB} ($T\ln T$) can be expressed into a sum of high-order T terms, high-order temperature-dependence cancellation can be achieved depending on the relative temperature-coefficients of R_1 and R_3. In [18], a fourth-order curvature correction has been reported. It is noted here that R_4 is made of the same material of R_1 and R_2, and is set to $R_2 + R_3$ at room temperature to achieve good matching of V_{DS1} and V_{DS2}.

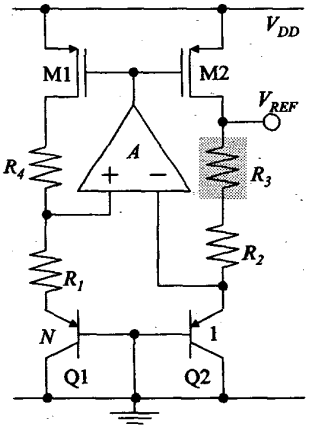

Fig. 13: A curvature-corrected bandgap reference based on T-dependent resistor ratio proposed by Leung *et al.* [18].

Trimming of this circuit can be done by adjusting R_3/R_1 such that the nonlinear error voltage is minimum. Then, the second step involves the minimization of the linear temperature dependence by finding an optimum R_2/R_1. In the trimming procedure, two temperature measurements (minimum and maximum) are sufficient for linear trimming, while four temperature measurements evenly distributed in the considered temperature range are sufficient for nonlinear trimming. In [18], the tempco is proven to be improved by 5 times when comparing the first-order compensated bandgap voltage reference.

IV. A CMOS Bandgap Design without Resistor

In the previous sections, low-voltage and low-tempco methodologies in the state-of-the-art CMOS voltage reference have been reviewed. It is well understood that technology limitations on passive components may occur. Large values of resistors are problematic in IC technologies as the resistors require large chip area that increases production cost. Moreover, coupling noise causes the reference voltage to become noisy, and this affects some noise-sensitive analog circuits. Therefore, a CMOS bandgap voltage reference without the resistor was developed by Buck *et al.* [19] and shown below.

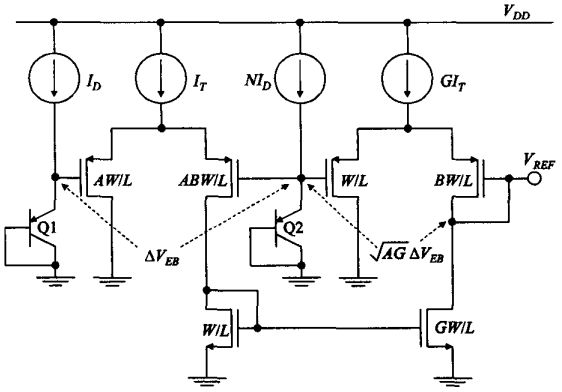

Fig. 14: A CMOS bandgap voltage reference without resistors proposed by Buck *et al.* [19].

The circuit makes use of voltage-to-current transducer to eliminate the need of the resistors. From Fig. 14, when I_D is a PTAT current, there is a ΔV_{EB} formed by the differently biased Q1 and Q2. Therefore,

$$\Delta V_{EB} = \Delta V_{GS} = \sqrt{\frac{2I_1}{\mu_N C_{OX}(AW/L)}} - \sqrt{\frac{2I_2}{\mu_N C_{OX}(ABW/L)}} \quad (12)$$

where $I_T = I_1 + I_2$. It is noted that this ΔV_{EB} is a PTAT voltage. With the use of the voltage-to-current transducer, the re-generated voltage is given by $\sqrt{AG}\Delta V_{BE}$. This can be explained by

$$\sqrt{\frac{2GI_1}{\mu_N C_{OX}(BW/L)}} - \sqrt{\frac{2GI_2}{\mu_N C_{OX}(W/L)}} = \sqrt{AG}\Delta V_{EB} \quad (13)$$

Therefore, V_{REF} is equal to the sum of V_{EB2} and this scaled-up PTAT voltage is given by

$$V_{REF} = V_{EB2} + \sqrt{AG}\Delta V_{EB} \quad (14)$$

By appropriate values of A and G, a bandgap reference voltage can be obtained with no need of a resistor. The zero-tempco performance can be obtained by trimming of transistor arrays.

In this design, the PTAT current to bias Q1 and Q2 is generated from the bandgap core itself. Therefore, a startup circuit is necessary. Moreover, the current and device matching are both critical to achieve a good result. Any variations on the threshold voltage and mobility will lead to additional temperature errors on the reference voltage.

V. Alternative Solution - A CMOS Voltage Reference

Although bandgap voltage reference shows very good performance, it is not the only voltage reference available in CMOS technologies. Thus, a voltage reference based on MOS characteristics is introduced in this section.

A voltage reference can be implemented by using MOS transistors only. This type of voltage reference relies on the temperature dependence of V_{TH}. The threshold voltage is approximated as a linear function of temperature, and the temperature dependences of NMOS and PMOS transistors are different in different technologies, as illustrated in Fig. 16.

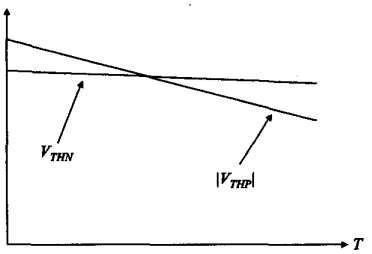

Fig. 16: Temperature dependence of V_{TH} [20]-[22].

It is very difficult to extract V_{TH} by simple circuits. Instead, V_{GS} is used in the design of [21] and [22]. Fig. 17 shows the simple circuit to form a temperature-insensitive V_{REF} based on weighted differences of V_{GS} of an NMOST and a PMOST.

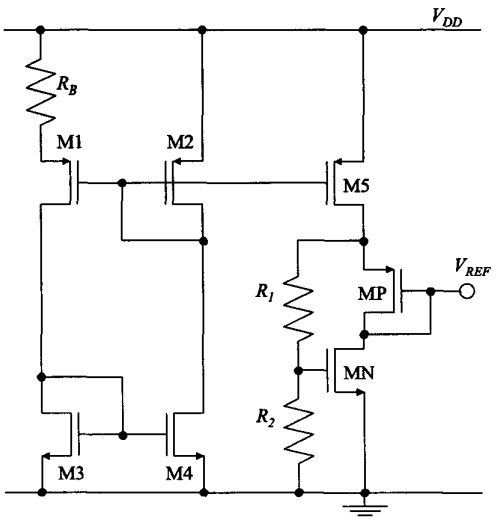

Fig. 15: A voltage reference in standard CMOS technologies proposed by Leung *et al.* [21], [22].

The reference voltage is given by

$$V_{REF} = \left(1 + \frac{R_1}{R_2}\right) \cdot V_{GSN} - |V_{GSP}| \qquad (15)$$

When R_1 and R_2 are large, the current in these two resistors is negligible. The temperature dependence of the reference voltage can be obtained by taking differentiation to the function of V_{REF} with respect to T. It is found that the circuit can be optimized by a resistor ratio of R_1/R_2 and a transistor-size ratio of the NMOST to PMOST. The reported tempco can be as low as 24ppm/°C, which is close to the performance of a bandgap voltage reference.

Moreover, the supply dependence is low. Since, as shown in equation (15), both V_{GSN} and $|V_{GSP}|$ increase/decrease simultaneously when I_B increases/decreases due to the change of the supply voltage, the effect is partially cancelled to achieve supply-less-sensitive performance.

One issue of concern on this design is that V_{REF} depends on process parameters. As a result, the magnitude of V_{REF} may vary. However, it is not a problem in some applications such as power-management ICs since the magnitude trimming can be easily done in the resistive feedback network of the on-chip power converters.

Conclusion

The design trend and current design methodologies of bandgap voltage reference have been discussed. The focus of this paper is mainly on the low-voltage and low-tempco designs, which are the vital requirements of future IC systems. Several reported circuit structures, therefore, have been analyzed. In addition, a design technique of no-resistor feature has also been studied.

Finally, a voltage reference other than bandgap type has been included. The working principle of this voltage reference is based on MOSFET characteristics. It has advantages, especially in its simple circuit implementation. This voltage reference is found to be a good voltage reference particularly for power-management applications.

Acknowledgement

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