

Assessment of parameter extraction methods for integrated inductor design and model validation

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Abstract— This work analyzes different parameter extraction methods for on-chip integrated inductors and assesses and their impact on inductor design. The relationship between extracted single-ended and differential parameters is investigated through the use of theoretical network models that support the calculation equations. Experimental results from a test chip are presented and a lumped model, which adequately simulates the inductor performance with and without ground shield, is validated in comparison to the simple nine-element model..

I. INTRODUCTION

Integrated inductors have been the subject of RF research the past two decades and with the on-growing trend towards high frequency wireless products have rendered themselves a corner stone in today's state of the art analog wireless circuitry. With higher demands for high performance RF circuits in CMOS technologies, it has become absolutely vital for the circuit designers to have accurate and reliable inductor models based on a systematic design method that would lead to robust knowledge of their performance at design time. Inductor designs on silicon, nowadays, employ additional features such as shields [1] in order to have superior RF performance.

The characterization of on-chip inductors is typically performed using two-port scattering parameter measurements. The inductance and quality factor are extracted based on specific equivalent model topologies although a universal definition has not yet been agreed upon for. Recently, inductor designs are also been validated assuming either single-ended or differential excitation depending on their use in a circuit.

This work analyzes two singled-ended and differential extraction methods assuming a simple π -type equivalent model. The relationship between the two methods is investigated and extended for more complicated equivalent model topologies. The clarification of the impact of the utilized model and parameter extraction equations on the calculated performance characteristics is aimed in this paper, together with the validation of two simple lumped models taken from the literature. The effect of a patterned ground shield is presented when both single-ended and differential excitation schemes are assumed.

The theoretical analysis of the models and the extraction methods is presented in the next section. Comparative experimental results between the different models and methods are given in section III, leading to their assessment and validation.

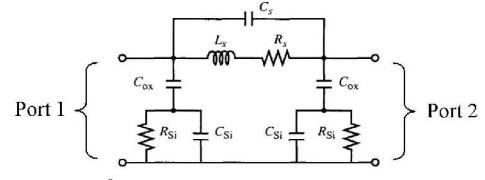


Fig. 1. Conventional π -type nine-element equivalent model of on-chip inductor.

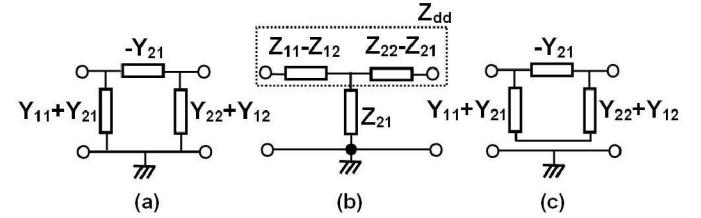


Fig. 2. Grounded π -type (a), T-type (b) and floating π -type (c) block diagram of a two port network.

A discussion and comments for further work are concluding the paper.

II. THEORETICAL MODEL ANALYSIS AND SIMULATIONS

The established conventional nine-element equivalent circuit is shown in Fig. 1 [2],[3]. The series inductance and resistance are represented by L_S and R_S . The capacitance between the two ports C_S is assumed very small and may be omitted. C_{OX} is the capacitance through the dielectric oxide and R_{Si} , C_{Si} account for ohmic and capacitive substrate losses. The three branches of this model are related to two-port admittance parameters as shown in Figure 2a. The series inductance and resistance can be extracted by the following equations (1) and (2), while the quality factor is defined in (3) and (4) depending on which port is used as input port.

$$L_S = \text{Im} \left(\frac{1/Y_{11}}{2\pi f} \right) = L_{SY_{11}} \quad (1)$$

$$R_S = \text{Re} (1/Y_{11}) = R_{SY_{11}} \quad (2)$$

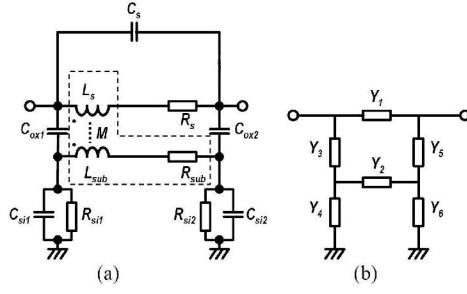


Fig. 3. Improved lumped element model of on-chip inductor that includes the effect of eddy currents in the substrate, based on [4]

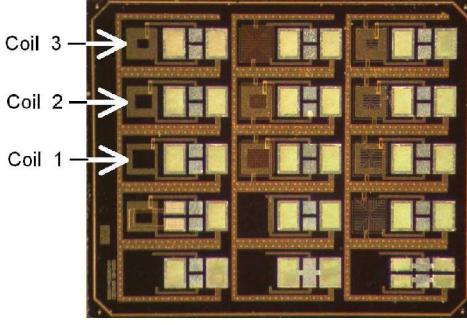


Fig. 4. Photograph of the fabricated test chip.

$$Q_{y11} = Q_{11} = \frac{Im(1/Y_{11})}{Re(1/Y_{11})} \quad (3)$$

$$Q_{y22} = Q_{22} = \frac{Im(1/Y_{22})}{Re(1/Y_{22})} \quad (4)$$

Another approach of extracting L_S , R_S and Q is through the differential input impedance Z_{dd} as defined in [5] and [6]:

$$Z_{dd} = Z_{11} + Z_{22} - Z_{12} - Z_{21} \quad (5)$$

where Z_{11} , Z_{12} , Z_{21} , Z_{22} are the two-port impedance parameters of the inductor. Figure 2b also shows how z-parameters are related to an equivalent T-type model.

Using this approach, R_S , L_S and Q are calculated by:

$$L_S = Im\left(\frac{Z_{dd}}{2\pi f}\right) = L_{Zdd} \quad (6)$$

$$R_S = Re(Z_{dd}) = R_{Zdd} \quad (7)$$

$$Q_{Zdd} = \frac{Im(Z_{dd})}{Re(Z_{dd})} \quad (8)$$

For a purely symmetrical network, $Z_{11}=Z_{22}$ and $Z_{21}=Z_{12}$. Differential excitation of the T-type model would result in a virtual ground at the node where Z_{21} connects to the other two branches of the network. This would result in artificial shorting of Z_{21} , as both its terminals would be at the ground potential either real or virtual. Impedance and admittance parameters are related to each other as shown in:

$$Z_{11} = \frac{Y_{22}}{\Delta_y}, Z_{12} = -\frac{Y_{12}}{\Delta_y}, Z_{21} = -\frac{Y_{21}}{\Delta_y}, Z_{22} = \frac{Y_{11}}{\Delta_y} \quad (9)$$

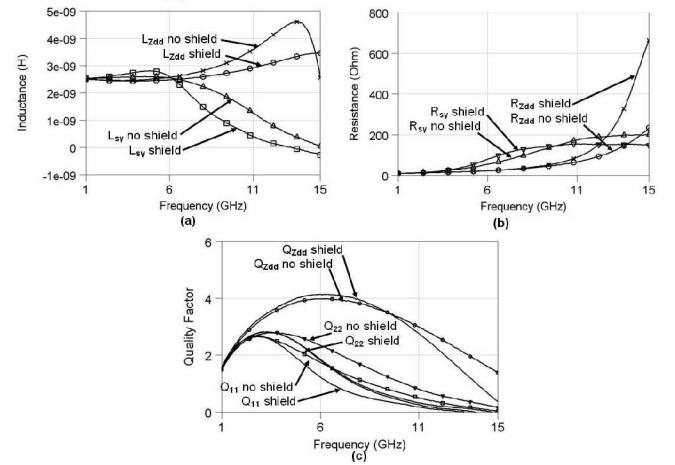


Fig. 5. (a) L, (b) R, and (c) Q of a 3.75-turn inductor with and without n-diffusion shield.

where

$$\Delta_y = Y_{11} \cdot Y_{22} - Y_{21} \cdot Y_{12} \quad (10)$$

Using the previous equation, we can define Z_{dd} in terms of admittance parameters as:

$$Z_{dd} = \frac{Y_{11} + Y_{22} + Y_{21} + Y_{12}}{\Delta_y} \quad (11)$$

If the ground node of the π -model is omitted, the input admittance of the resulting circuit (Fig. 2c) may be calculated as:

$$Y_{in} = Y_{dd} = -Y_{21} + \frac{(Y_{11} + Y_{21}) \cdot (Y_{22} + Y_{12})}{Y_{11} + Y_{22} + Y_{21} + Y_{12}} \quad (12)$$

Circuit symmetry ($Y_{21} = Y_{12}$) simplifies (12) to (13):

$$Y_{in} = Y_{dd} = \frac{\Delta_y}{Y_{11} + Y_{22} + Y_{21} + Y_{12}} = \frac{1}{Z_{dd}} \quad (13)$$

Comparison of (13) and (11) shows that Z_{dd} is essentially the input impedance of the π -type model with the substrate node floating. This equivalence is valid for any two-port model with $Y_{21} = Y_{12}$. In the case where $Y_{21} \neq Y_{12}$, it can be shown, using (11) and (12), that:

$$\frac{1}{Z_{dd}} - Y_{dd} = \frac{(Y_{11} + Y_{21}) \cdot (Y_{21} - Y_{12})}{Y_{11} + Y_{22} + Y_{21} + Y_{12}} \quad (14)$$

From the above equation it is clear that the proximity of the two approaches (single-ended and differential) depends upon the difference between Y_{21} and Y_{12} . If $Y_{21} \approx Y_{12}$, then (13) is approximately still valid. This will be indicated in the following examples.

For the conventional 9-element equivalent model of Fig. 1 it holds that $Y_{21} = Y_{12}$, since there is only one complex passive branch between ports 1 and 2 (Fig. 2a). For the improved model, which has been presented in [4] and is adopted in this work as shown in Fig. 3a, the block diagram is shown in Fig. 3b. A branch containing L_{SUB} and R_{SUB} is included that accounts for the eddy currents in the substrate. This model is applied to show that when the substrate node is

TABLE I

EXTRACTED MODEL PARAMETERS FOR A 3.75 TURN INDUCTOR WITH
AND WITHOUT N-DIFFUSION SHIELD

	No shield	Shield
L_S (nH)	2.46	2.46
R_S (Ω)	9.59	9.59
C_S (fF)	0	0
L_{SUB} (nH)	1.21	0.84
R_{SUB} (Ω)	12	0
K	0.84	0.86
C_{OX1} (fF)	201	246
C_{OX2} (fF)	202	238
R_{Si1} (Ω)	108	83
R_{Si2} (Ω)	174	123
C_{Si1} (fF)	9	0
C_{Si2} (fF)	9	0

floating, then the two methods of extracting L_S , R_S and Q yield the same results, even though $Y_{21} \neq Y_{12}$, while with a grounded substrate node, significant differences are observed. The component values used are given in Table I and they are extracted from the experiment test chip (see section III). From these values and the circuit of Fig. 3b it is obvious that theoretically $Y_{21} \neq Y_{12}$. However, circuit simulation gives almost the same diagram for Y_{12} and Y_{21} over a frequency range of 1 to 15 GHz. The difference for the real as well as the imaginary part is in the order of $10^{-17} \Omega^{-1}$, so they are practically the same.

This analysis reveals potential difficulties in determining the values of fundamental inductor components at frequencies in the GHz range. The two methods of extraction give different results that correspond to different equivalent network topologies.

III. EXPERIMENTAL RESULTS AND ANALYSIS

A test chip consisting of various inductors was designed and fabricated with AMIS 0.7 μm CMOS DM1P n-well technology (Fig. 4). The inductors were designed on the top metal layer (metal2) with a width of 12 μm , spacing of 2 μm and external diameter of 160 μm . The grounded shield was patterned to form perpendicular segments that were grounded without forming a ground loop, which might support eddy currents. Additional dummy structures for de-embedding purposes were included in the chip, such as open and short circuits with and without ground shields.

Scattering parameter measurements were performed using 150 μm pitch, 50 GHz, Picoprobe GSG probes and a HP8510 vector network analyzer in a frequency range of 1 to 15 GHz. The experimental set-up was calibrated with a two-port Line-Reflect-Match (LRM) standard. The metal chuck of the probe station was grounded. The effect of the GSG probing pads and connection tracks was eliminated by applied open-short de-embedding.

De-embedded experimental measurements of the fabricated devices are presented in Fig. 5 for a 3.75-turn inductor. The

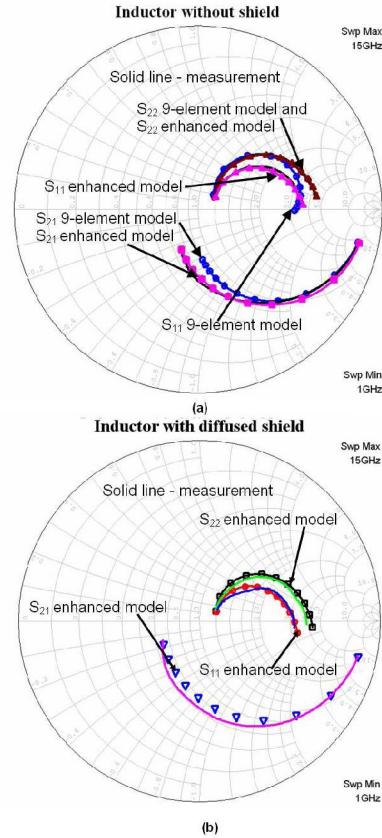


Fig. 6. Comparison of extracted model and measured S-parameters for the 3.75 turn inductor with (b) and without shield (a).

inductance, series resistance and quality factor are extracted from the measurements using equations (1), (2), (3) and (6), (7), (8) respectively. Results include measurements from inductors with diffused shields and with no shields at all.

At low frequencies both equations converge to the same value of L_S and R_S because the capacitive components C_{OX} isolate the R_{Si} , C_{Si} network and substrate node and the entire circuit is equivalent to the lateral L_S , R_S branch. This is clearly observed in all plots where each set of traces start from the same value at 1 GHz. The effect of shields is also shown clearly. The quality factor is slightly improved for both definitions, with Q_{Y11} and Q_{Y22} improvement below the peak value and Q_{Zdd} over the entire frequency range.

Apart from the quality factor it is interesting to observe how single-ended R_{Sy} , L_{Sy} and differential R_{Zdd} , L_{Zdd} are affected by the presence of ground shields. In particular R_{Sy} and L_{Sy} increase when diffused shields are used. The same trend applies for R_{Zdd} and L_{Zdd} as they tend to increase the value of series resistance and inductance when shields are incorporated into the structure. The self-resonance frequency in both cases tends to decrease when shields are present.

Such behaviour is captured by the lumped-element model of Fig. 3. Numerical regression optimization was utilized to determine the values of C_{OX} , L_{SUB} , R_{SUB} , C_{Si} and R_{Si} , while the remaining components were given initial values based

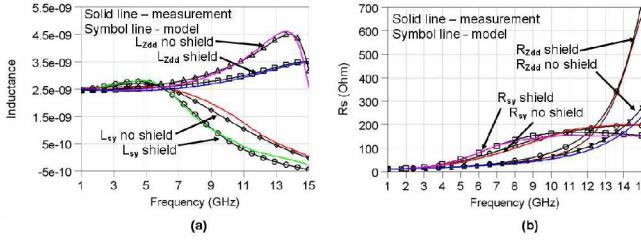


Fig. 7. Series inductance (a) and resistance (b) comparison of model and measurement data of the 3.75 turn inductor with and without a shield.

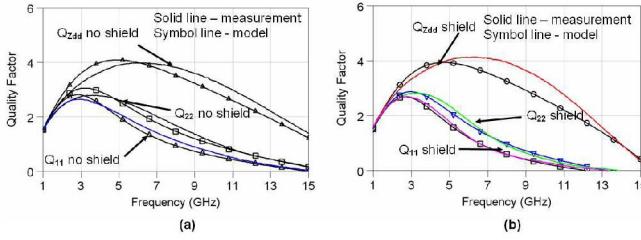


Fig. 8. Comparison of measurement and model quality factors of the 3.75 turn inductor (a) without and (b) with a shield.

on the lowest frequency data. The optimization goal was to match the S-parameters of the model with the measured ones. Table I summarizes the extracted model parameters for a 3.75 turn inductor. Fig. 6 shows that good agreement is observed between the S-parameters of the model and measurements. Fig. 6a also illustrates the inability of the nine element model to capture the dynamic behaviour of the inductor. Comparison of L_{Sy}, R_{Sy} and Q with or without diffused shields is shown in Fig. 7 and 8.

The behavior of the extracted model parameters (Table I) when a shielding scheme is included can be explained when the effect of the shield on the self-resonance frequency of the inductor is taken into account. Shielding schemes were initially investigated by [1]. As it can also be seen in the experimental results in this work, a diffused shield results in higher quality factors at the expense of lower resonance frequencies. The peak Q values are higher but the slope of the quality factor curve is now steeper. Steeper slopes would result in lower self-resonance frequencies. For example, Fig. 5 shows that the self-resonance frequency decreases from 14.8 GHz to 13.3 GHz when the shield is present. This occurs because the R_{Si}, C_{Si} network that represents substrate losses changes when a shield is inserted. The capacitive component C_{Si} disappears because of the lower resistivity of the diffusion shield and at the same time the ohmic component becomes lower. The capacitance through the oxide C_{Ox} is now connected to the ground node through a low resistivity diffusion path. The presence of a "better" ground gives rise to additional fringing components of the oxide capacitance and the effective capacitance to ground is now higher and causes the self-resonance frequency to decrease.

With lower resonance frequency inductance curves would rise with a faster slope before the inductor resonates. The

same applies to the series resistance that would approach its maximum value at the resonance frequency faster. The previous descriptive analysis can be fully correlated to the component values of the equivalent model of Fig. 3 shown in Table I.

IV. CONCLUSION

Two methods of series inductance and resistance extraction and quality factor estimation were analyzed and assessed in this work. Their relation was investigated utilizing the simple two-port single-ended and differential models and it was shown that quality factor estimation based on the differential input impedance assumes that the substrate node of the equivalent circuit is floating. This result is applicable to all 2-port models with more added complexity, such as branches that account for the skin effect or substrate eddy currents, provided that Y₂₁ = Y₁₂ or Y₂₁ ≈ Y₁₂. The quality factor could be overestimated and the series inductance and resistance both exhibit different frequency behavior based on the extraction procedure used, a fact that can be confusing for designers. Hence, caution must be taken when these figures of merit and performances are extracted in practice. A lumped-element model that includes a branch for the eddy current losses is adopted, which captures the measured characteristics even when ground shields are integrated to the structure. The use of shields does not perhaps give always a better solution, since their use also incorporates a loss of inductance value, according to the model, which is the case for grounded models. Thus a compromise must be followed by the designer. An interesting observation is that in all cases Q₁₁ < Q₂₂, which implies that the same inductor gives a better performance when port 1 is grounded, instead of port 2 (port 2 is the one where the underpass of the inductor layout is connected). This aspect is currently under investigation.

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REFERENCES

- [1] C. P. Yue and S. Wong, "On-chip spiral inductors with patterned ground shields for Si-based RF IC's," *IEEE Journal of Solid State Circuits*, vol. 33, no. 5, pp. 743 – 752, May 1998.
- [2] D. Melendy, P. Francis, C. Pichler, K. Hwang, G. Srinivasan, and A. Weisshaar, "A new wide-band compact model for spiral inductors in RFICs," *IEEE Electron Device Letters*, vol. 25, no. 5, pp. 273–275, May 2002.
- [3] Y. Cao, R. A. Groves, X. Huang, N. D. Zamdmer, J.-O. Plouchart, R. A. Wachnik, T.-J. King, and C. Hu, "Frequency-independent equivalent-circuit model for on-chip spiral inductors," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 3, pp. 419–426, March 2003.
- [4] M. Fujishima and J. Kino, "Accurate subcircuit model of an on-chip inductor with a new substrate network," in *Proc. IEEE Symposium on VLSI Circuits*, 2004, pp. 376–379.
- [5] R. Havens, L. Tiemeijer, and L. Gambus, "Impact of probe configuration and calibration techniques on quality factor determination of on-wafer inductors for GHz applications," in *Proc. ICMTS*, 2002, pp. 19–24.
- [6] L. Tiemeijer and R. Havens, "A calibrated lumped-element de-embedding technique for on-wafer RF characterisation of high-quality inductors and high-speed transistors," *IEEE Transactions on Electron Devices*, vol. 50, no. 3, pp. 822–829, March 2003.