

Wireless Power Receiving Unit

Analysis, design and implementation of inductive power receiving unit for wireless circuits

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Part I

Component Design and Analysis

Chapter 1

Rectifier

1.1 Introduction

The most basic rectifier is conventional full wave bridge structure where the diodes are replaced by the diode connected MOS. devices in CMOS. technology. This topology though being simple to implement, has a major drawback. It requires at least twice the V_{tn} of a MOS device as there are two diode connected MOSEs in the conduction path for each cycle of the input signal.

Gate cross coupled and fully gate cross coupled topologies are improvements over conventional full wave rectifier. In gate cross coupled rectifier, two diodes of conventional rectifier is replaced by two gate cross coupled MOSEs working as switches where the voltage drop for every cycle is reduced to one threshold voltage. Similarly, in the fully gate cross coupled rectifier, all diodes are replaced by switches and hence the voltage drop is further reduced to twice the conduction drop only for every cycle. Even though this topology has least voltage drop, it suffers from the problem of reverse charge leakage because when the input ac amplitude is less than the output rectified voltage and the conducting pass devices are on simultaneously, current flows backward from output to input.

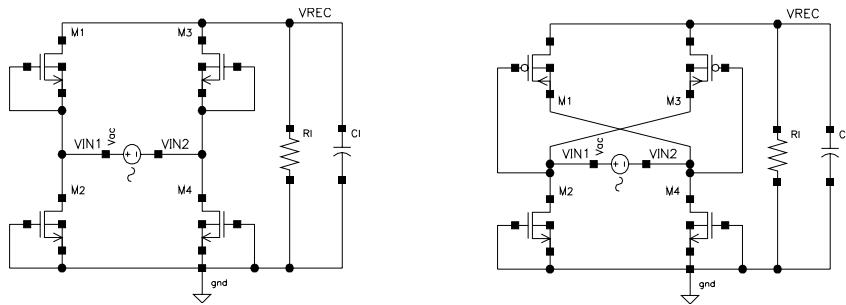
All the above discussed topology suffer from either large voltage drop or large power loss because of which their use are limited in low power and low voltage devices. The popular techniques for higher efficiency are using gate cross coupled rectifier along with passive or active circuitry for controlling other two pass devices. In passive rectifier, additional circuitry including bootstrap capacitor are used to reduce or eliminate threshold voltage one of which is discussed in this paper [1]. However, use of on-chip bootstrap capacitors limits its use where chip area and speed is of importance. On the other hand, in active rectifier, active circuitry is used to control pass devices. The use of active circuitry increase both voltage conversion efficiency (VCE) and power conversion efficiency (PCE) because the pass devices are made to conduct in linear

region and hence less conduction drop, and reverse current flow can be completely eliminated and hence less power loss. However active rectifier is not problem free either. The major issue is starting of the active circuit as there is no regulated supply at the start up.

1.2 Design

In this project, active rectifier is chosen, primarily for better VCE and PCE and secondarily to avoid the use large on chip capacitors. [2] and [3] have discussed same active rectifier topology with a slight difference in active circuitry. [2] has implemented comparator with compensating the delay of comparator's output falling whereas [3] has implemented comparator with compensating both the falling and the rising delay of comparator's output in expense of added circuit complexity and power consumption. [2] has been used here for its simple design.

Figure 1.1a, 1.1b and 1.2 is the CMOS implementation of conventional full wave bridge rectifier, gate cross coupled rectifier and proposed active rectifier in [2]. The problem with 1.1a and 1.1b has already been briefly mentioned above. Though 1.1b is significantly improvement over 1.1a , it is still not a favourable topology with respect to the design technology chosen. In the gate cross couple rectifier of 1.1b, the cross coupled pMOSes act as switches, so the only voltage drop across them is conduction drop due to channel resistance. However the other two nMOSes are diode connected, so they have at least V_{tn} drop across them which means $V_{ac} \geq V_{dc} + V_{tn}$ for conduction.



(a) Conventional full wave bridge rectifier (b) Gate cross coupled full wave rectifier

Figure 1.1: Rectifier topologies: conventional and gate cross coupled

The proposed active circuit in 1.2 is improvement over 1.1b which eliminates V_{tn} drop required for conduction by replacing diode connected nMOS with devices controlled by active circuit as shown in figure 1.3. The active circuit is a four input comparator that turns on nMOSes fast when $V_{ac} > V_{dc}$ and turns off fast to avoid flow of current.

For the illustration of operation of comparator, consider the case when $Vin_1 > Vin_2$ i.e. $Vin_1 > 0$ and $Vin_2 < 0$. During this half cycle, comparator $D1$ output is low and turns off Mn_2 and also, Mp_1 is reversed biased and hence there is no path to flow current along Mn_2 and Mp_1 . For simplicity, assume $Vac = Vin_1 - Vin_2$. When Vac reaches Vtp , Mp_3 turns on which shorts Vin_1 to $Vrec$. When $Vac > Vrec$, $D2$ output goes high, which turns on Mn_4 and starts the conduction path for the first half cycle and starts charging C_1 . When Vac reaches maximum, it starts to decrease and at $Vac < Vrec$, conduction stops as output of $D2$ is low and Mn_4 is off. As Vac further decreases to below Vtp , Mp_3 is off too. This way rectifier in 1.2 conducts during positive half cycle eliminating the Vtn drop seen in 1.1b. Now the only drop is the conduction drop due to channel resistance of two pass devices along the conduction path. This drop is much less because during conduction both the device are operating in the linear region with small resistance. The operation is similar for $Vin_2 > Vin_1$ where Mn_4 and Mp_3 are off and Mn_2 and Mp_1 conduct to charge C_1 .

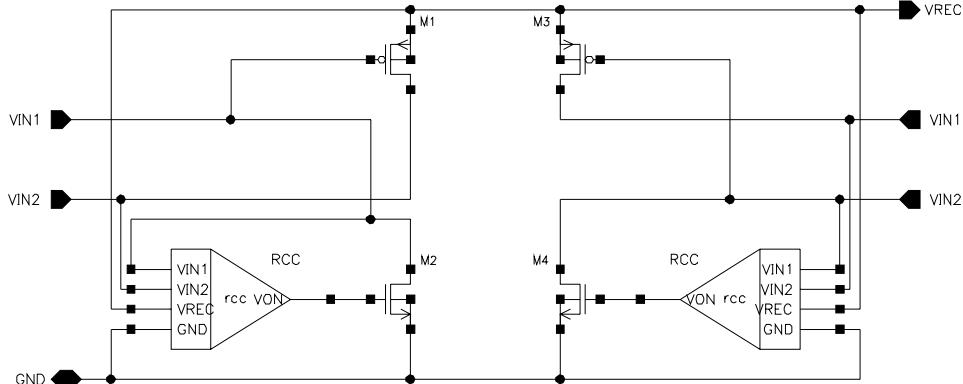


Figure 1.2: Gate cross coupled full wave active rectifier]

Figure 1.3 is the implementation of four input comparator $D2$ used in 1.2 as proposed in [2]. It is designed to self power and bias because no steady state supply is available at start up. $M1$, $M2$ and $M7$ monitors voltage across Mn_4 i.e $Vin_2 - Vgnd$ and $M3$, $M4$ and $M8$ monitors voltage across Mp_3 ie $Vin_1 - Vrec$. So when $Vin_1 - Vrec > Vin_2 - Vgnd$ which means $Vac > Vrec$, output of $D2$ is high and turns on Mn_4 instantly. But when $Vac < Vrec$, the output of comparator is delayed to fall which causes Mn_4 to conduct in reverse direction leading to significant reduction in power delivered to load. $M9$ is introduced in order to overcome this problem which adds offset currents to increase Van and Vpn faster, causing the output to decrease faster and turns off Mn_4 before $Vac < Vrec$. This reverse current control technique compensates the comparator delay and increases the power efficiency of the rectifier.

The design parameters for the rectifier is listed in table 1.1. The di-

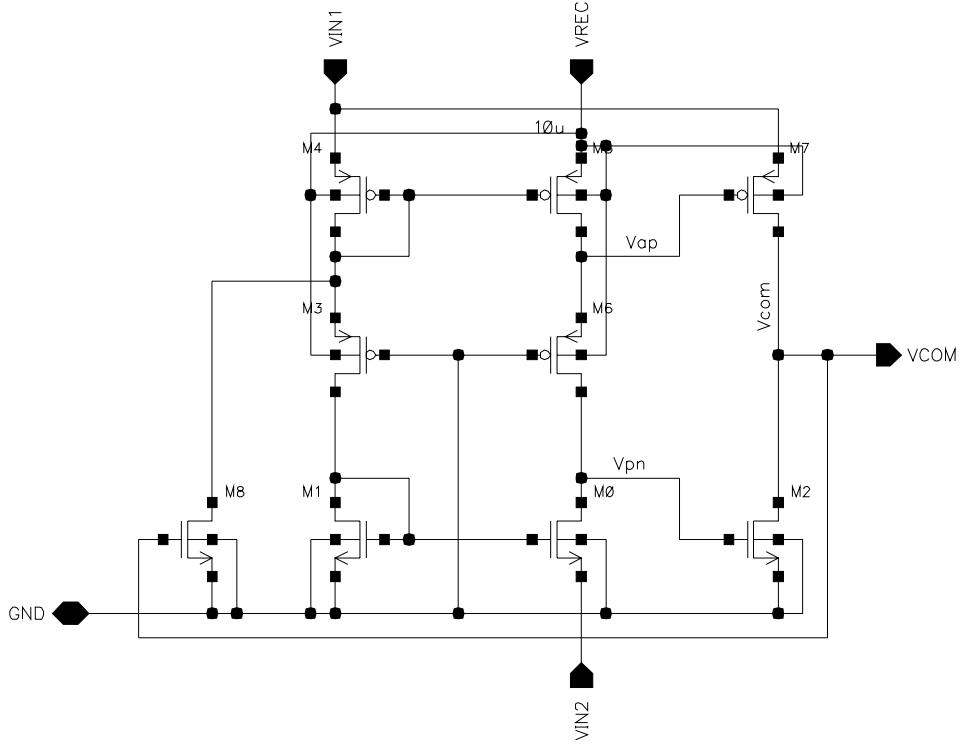


Figure 1.3: Comparator circuit, RCC

mensions of the pass devices are first hand calculated by using square law current equation and devices parameters values given in the technology documents, and later optimised with simulation tool in order to make the rectifier to deliver the required current. Since nMOS does not have to have same device size as pMOS to deliver same current, optimal size ratio equation from [4] is used to find nMOS pass devices sizes. Thought maximum load for this work is 10 mA, It is always simulated with 1 mA extra load. This extra current is to account for the fact that RCC is self powered and LDO which will follow this rectifier will be powered by V_{rec} . Similarly, the value of ripple rejection capacitor is chosen 100nF. This size of filter capacitor is calculated from capacitor current-voltage relationship with the assumption of keeping peak to peak ripple voltage below 5 mV to deliver 11 mA current.

Table 1.1: Rectifier design parameters

Wn/Ln, Wp/Lp	720um/280nm, 1.2mm/280nm
Rectifier area	TBA mm ²
Operating frequency	13.56 MHz
Input ac magnitude	2.5 Vp
Load current	11 mA
Ripple rejection capacitor	100 nF

1.3 Simulation result

1.3.1 Transient performance

Figure 1.4 is the test bench setup for simulation of the rectifier. Figure 1.5 show the simulation results showing voltages at the input ac and output rectified DC voltages and current through rectifying MOSes. These waveforms clearly follows the working principle discussed above. Two important observations can be made from plots. First, the rectified output V_{rec} is 2.2 V for V_{pp} ac input of 2.5 V for driving which means the voltage loss has been significantly reduced and the loss of around 300 mV yields to the conduction loss due the channel resistance. Secondly, the reverse current from output to input has been effectively eliminated as there is only positive current flowing to the load when all conducting devices are on.

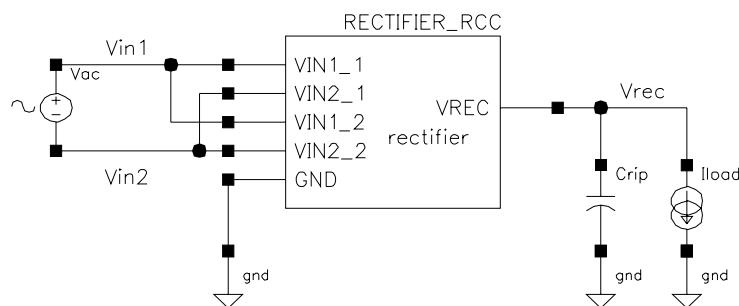


Figure 1.4: Testbench for rectifier

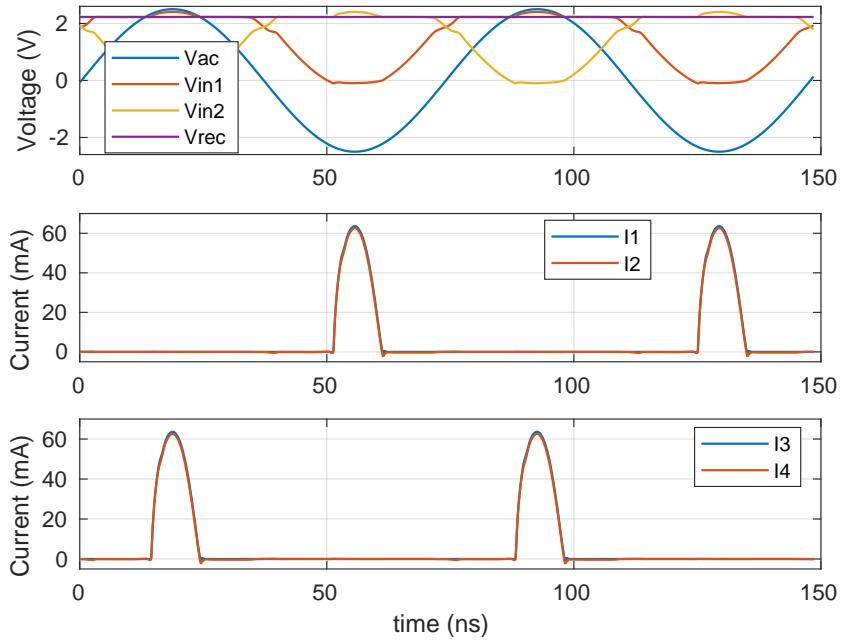
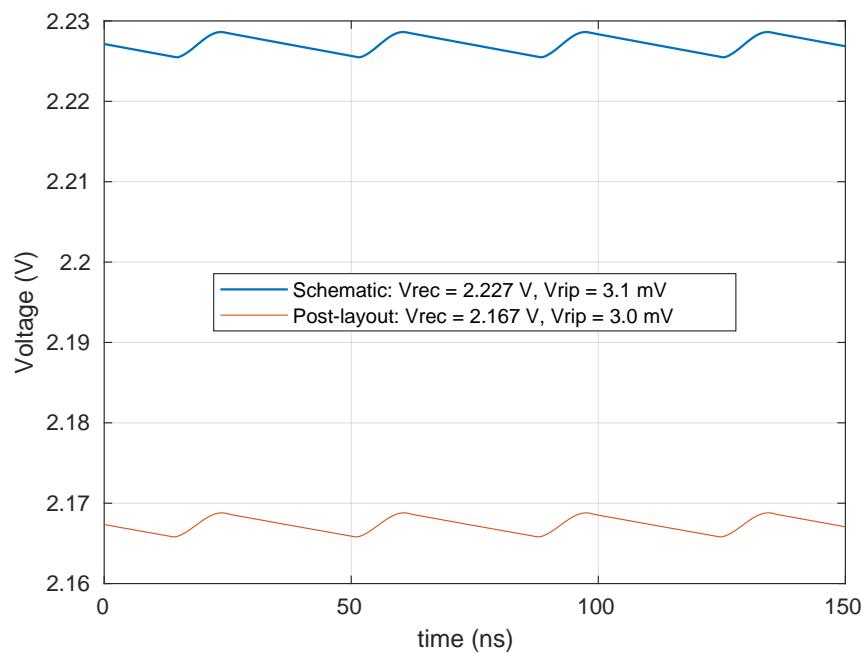
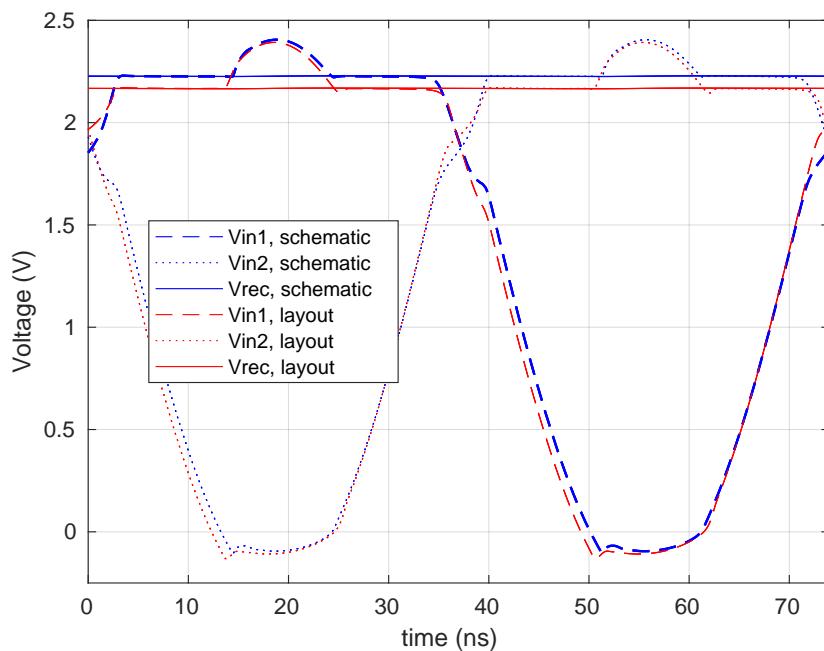


Figure 1.5: Voltage and current waveforms of the rectifier

Figure 1.6 presents both pre and post layout results of input voltages, Vin_1 and Vin_2 and output voltage, V_{rec} , for one cycle of ac input. The closer view of rectified output is shown in figure 1.7. The voltage drop of about 60 mV in layout result is accounted for the voltage drop due to the resistance of high current conduction path.



1.3.2 DC performance

Similarly, figure 1.8 shows PCE, ratio of powered delivered to load to average power from the source and VCE, ratio of rectified DC, V_{rec} to peak ac input, $|V_{ac}|$ with respect to magnitude peak ac input signal. $|V_{ac}|$ is gradually increased in peak magnitude in step of 50 mV and VCE and PCE is calculated for every step. The plot shows both PCE and VCE are very less for input ac amplitude less than 1.8 V. It can be explained by the fact that required bias current and gate drive voltage for RCC circuit are not achieved for smaller input. [INCLUDE POST LAYOUT RESULT TOO]

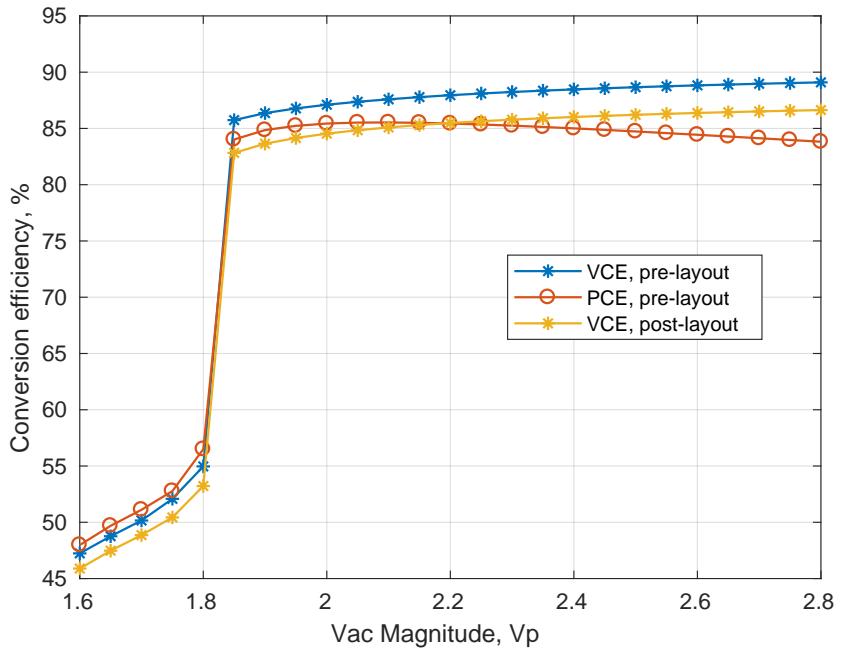


Figure 1.8: Voltage and power conversion efficiency

Table 1.2 comparatively summarises performance for pre and post layout result of the design. The layout design is attached in appendix. The layout is made symmetrical with four inputs, as seen in test bench figure 1.4, instead of two. This is done to make the current conducting path equal which result in equal drop in voltage when it reaches the rectifying MOSes. Simialrly the paths from the pad to the recitifier inputs are mask blocked for random metal fill to avoid inter layer coupling [WHY??]. The high current conduction routes are designed with wide parallel path of many higher level metal layers for reducing resistance in conduction path.

Table 1.2: Rectifier performance summary

	Schematic	Post-layout
Rectified DC	2.23 V	2.17 V
Ripple Vpp	3.1 mV	3 mV
Peak diode current	63.7 mA	-
PCE	84.5 %	-
VCE	88.6 %	86.2 %

Chapter 2

Low Dropout Regulator

2.1 Introduction

Voltage regulator follows the rectifier designed above in order to regulated the rectified voltage to 1.8 V and deliver maximum load current of 10 mA. Since the output from the active rectifier is 2.2 V and the required regulated voltage is 1.8 V, charge pump or SMPS of boost type is irrelevant here. Buck SMPS could be an option for voltage regulation but LDO is preferred for it better performance in terms of noise and faster settling of regulated voltage. [5].

Figure 2.1 shows a circuit of typical LDO with pMOS as pass element. As shown in the figure, the components includes an error amplifier (EA), a pass device (M_{pass}), a feedback circuit (R_1 and R_2) and load (C_{out} and I_{load}). A more general and complete LDO circuit also includes circuitry for generation of reference voltage and bias current/voltage. In this project it will be discussed separately later. The working principle of LDO is that the error amplifier compares the scaled down regulated voltage, V_{div} with V_{ref} and regulates the internal resistance of the pass transistor such that the error, $V_{ref} - V_{div}$ is least or zero ideally.

[6] and [7] are two examples of CMOS implementation of LDO. [6] has proposed bulk modulation technique for improving load regulation and stability of capacitor-less LDO. Similarly [7] has proposed techniques for increasing current efficiency of LDO especially at no or low load condition. Though the techniques discussed in these designs have not been used, they have given good insight into different design parameters of LDO.

2.2 Design

Figure 2.2 shows the CMOS implementation of LDO in this project. The components in this design include a folded cascode differential amplifier as error amplifier, pMOS buffer, pMOS pass device and feedback net-

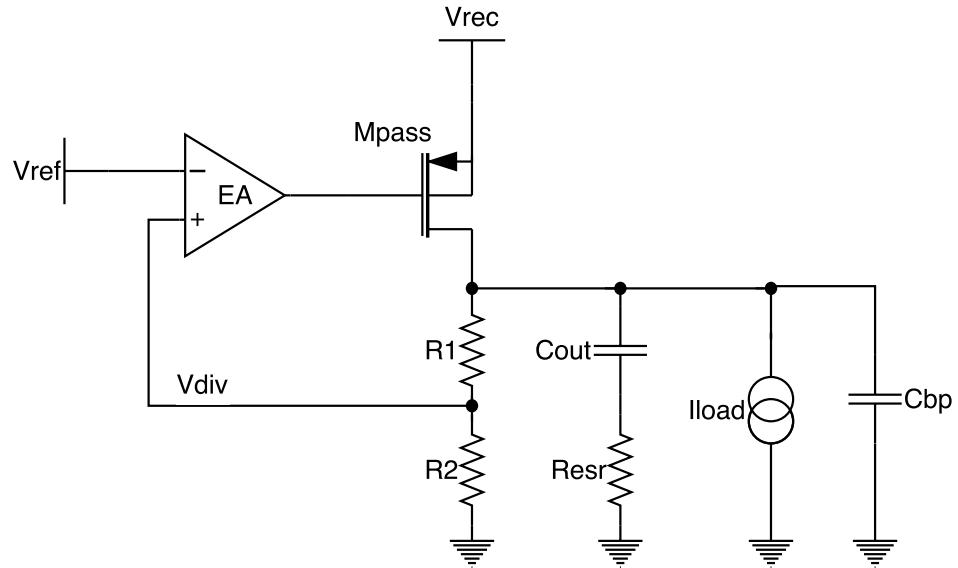


Figure 2.1: Generic LDO with pMOS pass device

work of resistors.

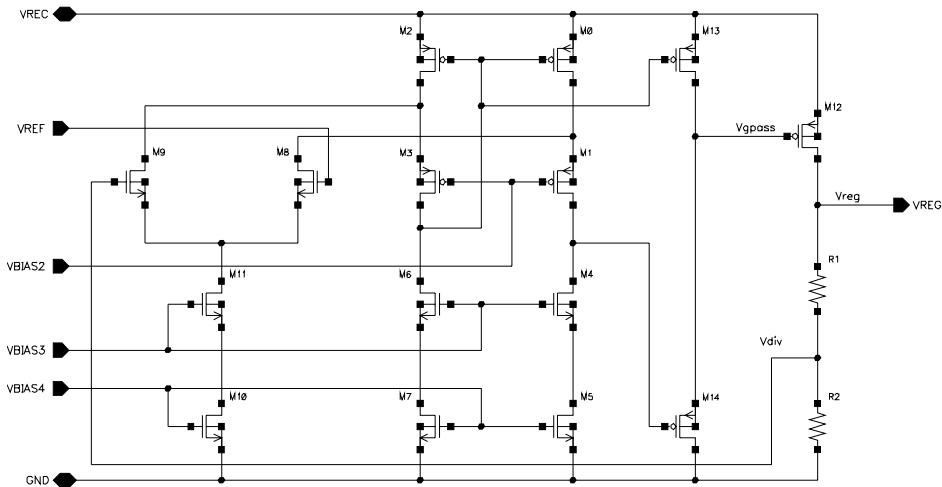


Figure 2.2: CMOS implementation of LDO

As briefly mentioned above, the error amplifier amplifies the error i.e. difference in scaled regulated voltage, V_{div} and reference voltage, V_{ref} . It is known that an amplifier with higher open loop DC gain reduces the closed loop gain error and hence amplifier with higher gain is desired here which in turn increases the accuracy of regulated voltage, V_{reg} [6]. Typically error amplifier has gain $> 40 \text{ dB}$ which is not achieved with a single stage amplifier with this technology. Higher gain can be achieved by cascading multiple single stage but with increased difficulty in making the multistage amplifier stable. So for achieving

higher DC gain and at the same time for stability convenience, folded cascode amplifier [8, pp. xx] is chosen.

Table 2.1: LDO design parameters

Pass device	pMOS
$(W_p/L_p)_{\text{pass}}$	540um/280nm
Input supply	>2.2 V
Error amplifier	folded cascode
Vbias2	1.1 V
Vbias3	0.88 V
Vbias4	0.68 V
Vref	1.17 V
C _{load}	> 5 μF
R _{esr}	> 0.5 Ω
Regulated output voltage	1.8 V
I _{load} max.	10 mA

The amplifier has a nMOS differential input stage, preferably for its higher mobility for achieving more gain. Reference voltage, V_{ref} will be bandgap voltage, 1.17 V, of silicon and thus ICMR for EA lies almost at half the supply voltage. This amplifier drives a pMOS buffer which is used to supply sufficient current to drive the large pass transistor. Moreover, pMOS as a buffer passes 1 better which means it can turn off the pass device completely and hence LDO regulates better at low load or no load condition. However for heavier load/larger load current, this pMOS buffer is not able to pull down the gate of pass device sufficiently lower. This is overcome by making the pass device large enough to feed the required maximum load current.

The pass device is a pMOS transistor in this design. It is chosen because it has several advantages over its counterparts like nMOS and BJT devices in terms of dropout voltage, quiescent current, input voltage, thermal response and noise[9]. Prominently, there are two factors that give pMOS edge over other devices; dropout voltage and quiescent current, when it comes to application in low power and low voltage devices. nMOS as a pass device requires a positive drive voltage with respect to output to operate. On the other hand, pMOS is driven by a negative signal with respect to input which means pMOS is preferable for a low input LDO. Similarly compared to BJTs, pMOS requires less headroom and less quiescent current to be driven[9], [10], which means low dropout and low power operation, typical requirement of today's micro devices' power supply.

However, pMOS as a pass device in LDO causes challenges in sta-

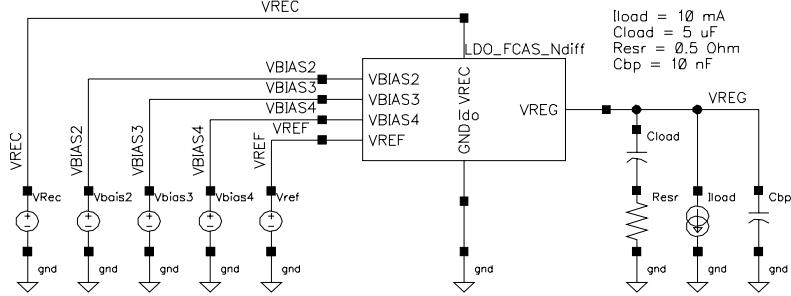


Figure 2.3: LDO testbench setup

bility. As mentioned above, LDO utilises a high gain feedback loop in order to provide a regulated output voltages independent of load current and in any system with feedback loop, the locations of poles and zeros determine stability of the system. In case of the pMOS LDO, the pass device is configured in a common source configuration. LDO with big output cap has a dominant pole at the output, which is a low frequency pole. The second pole is located at the gate of pass device because as mentioned earlier pMOS pass device is large and has a big parasitic capacitance. This second pole may be located closer to the dominant pole, resulting in significant reduction in phase margin (PM). Consequently, this may lead to instability of the LDO with pMOS pass device. Various methods have been implemented for ensuring the stability of the pMOS LDO. In this project, a large external capacitor, C_{load} in figure 2.1, is used for stabilising the system at the cost of additional settling time. When an external capacitor is used for designing a stable LDO, the minimum value of capacitance, C_{load} and minumum value of its equivalent series resistance (ESR), R_{esr} should be specified[10]. C_{load} determines the dominant pole of the LDO and R_{esr} in series with C_{load} introduces a left half plane zero below unity gain frequency, UGF of LDO in order to cancel out the non-dominant pole below UGF, producing a stable LDO system.

2.3 Simulation result

2.3.1 Transient response

Figure 2.4 is the transient simulations of the LDO which illustrates generation of regulated output voltage, V_{reg} for both maximum load, 10 mA. For maximum load, it takes minimum 107 us to produce stable voltage. Since a large capacitor is used for stabilising LDO, it take longer time. Compared to schematic result, it takes 9 us extra time which can be accounted additional parasitic capacitance of interconnects at the output of LDO.

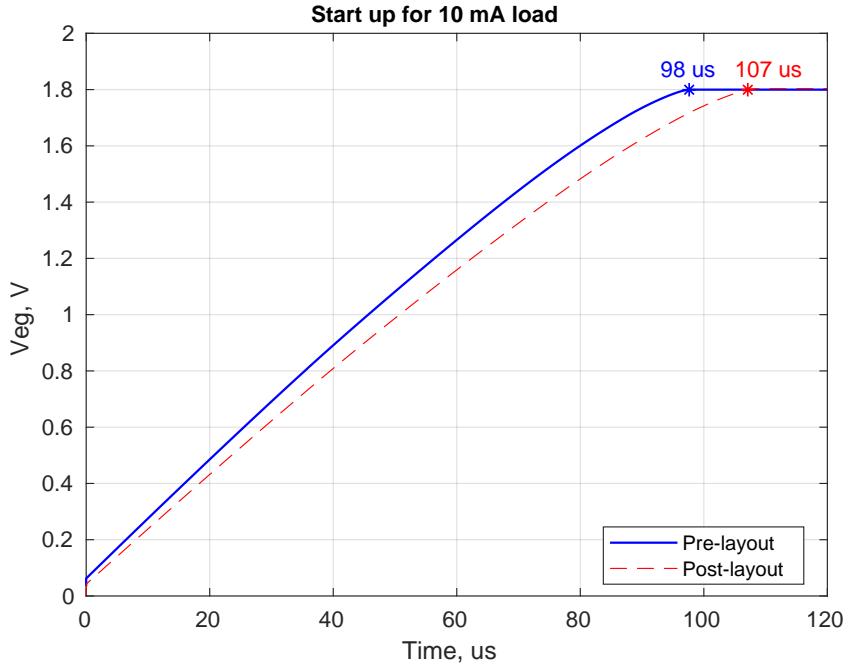


Figure 2.4: LDO transient simulation

Figure 2.5 and 2.6 show the transient response of LDO for line, V_{rec} and load, I_{load} variation. It gives information about how well and how fast regulated output settles for line and load variations. In figure 2.5 load is given as pulse varying from 10 μ A to 10 mA with both falling and rising time of 1 ns keeping input supply constant to 2.2 V. Sudden increase in load causes the output voltage to drop. The error amplifier then takes some time to adjust the gate voltage of pass device to low to fully turn on the device. Likewise when the load suddenly drops to minimum, it causes the output voltage to increase. Again error amplifier adjusts it back by increasing the gate voltage of pass device to turn it off. Similarly for line variation observation, input, V_{rec} is pulsed from 2 V to 2.5 V with 1 ns rising and falling time keeping load current constant to 10 mA. Sudden increase in input voltage causes output to increase and vice-versa. As in load variation case, similar recovery pattern is seen. In both cases of load and line regulation, the output voltage is maintained quickly, less than 0.15 us. Both results from schematic and post layout have same transition behaviour except post layout result offset by 3.7 mV as explained in DC response section below.

Line regulation, change in regulated output voltage due to maximum change in input voltage and load regulation, change in output voltage due to maximum change in load current are calculated from values shown in respective plots and are listed in table 2.2.

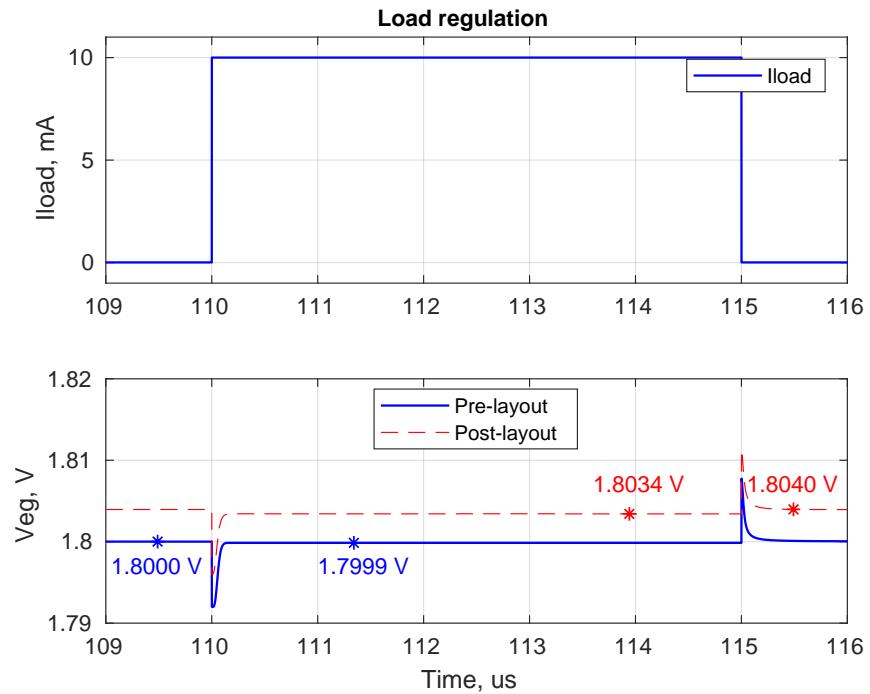


Figure 2.5: LDO step load regulation

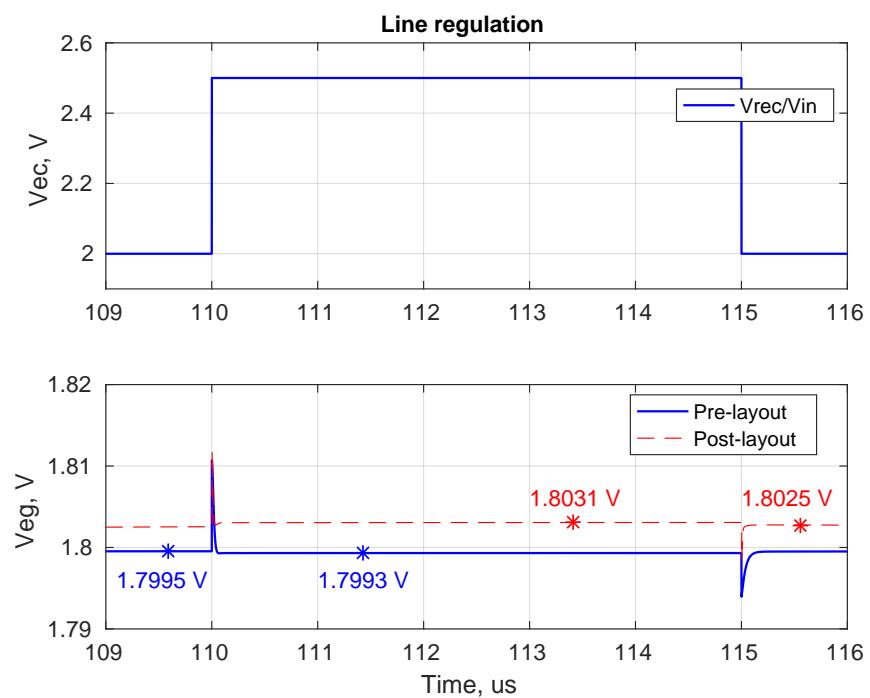


Figure 2.6: LDO step line regulation

2.3.2 DC response

Figure 2.7 and 2.8 show LDO response to input voltage, V_{rec} sweep and output load, I_{load} sweep. As seen in 2.7, the regulator is turned off for input below 1.85 V. Since the input is also the supply for the entire design, higher voltage is required for creating proper biasing of internal folded cascode error amplifier. However after turning on, it requires only 100 mV drop for proper regulation for maximum load and is even lesser for lighter load. This shows that minimum value of supply required for LDO to function properly is 1.95 V. In 2.8, it is seen that regulated output voltage for post layout simulation is 3.7 mV higher than for schematic. Since $V_{reg} = (1 + R_1/R_2) * V_{ref}$, the mismatch in the resistors has resulted in slightly higher ratio, consequently increasing the close loop gain.

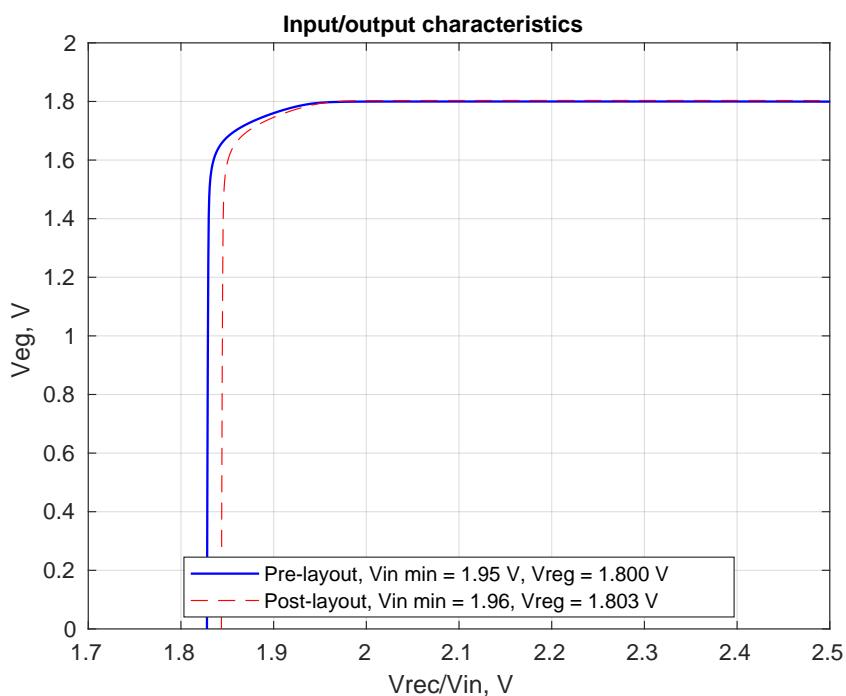


Figure 2.7: Regulated voltage with supply variation

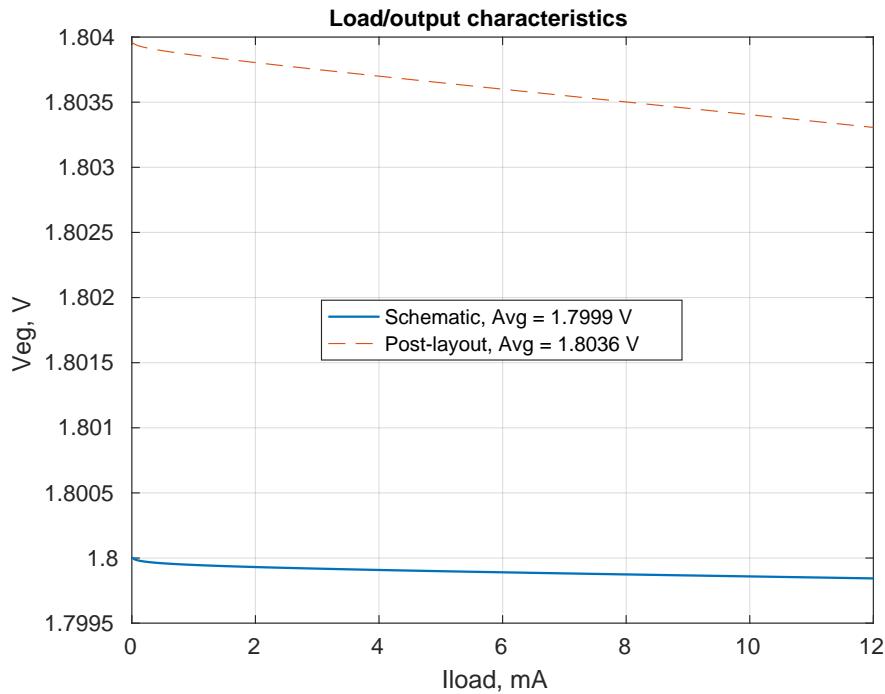


Figure 2.8: Regulated voltage with load variation

2.3.3 AC response

Figure 2.9 is open loop gain and phase margin of LDO without and with compensation. In the upper uncompensated bode plot, two poles below UGF are seen: the first one at 300 KHz due to output resistance of pass device and its parasitic capacitance, and the second one at 60 MHz due to buffer output resistance and gate capacitance of pass device. UGF is at 100 MHz. Due to these two poles both occurring below UGF, the PM fallen to -45°. For making the LDO stable, as discussed in the beginning, a capacitor, C_{load} , 2.5 uF with specific series equivalent resistance, R_{esr} , 0.8 Ω is used at the output. C_{load} and pass device output resistance creates the dominant pole at 1 KHz and R_{esr} and C_{load} creates a left half plane zero below UGF which cancels the non dominant pole. This eventually gives 75°PM and 30 dB GM.

Likewise figure 2.10 is the plot showing PSSR of this LDO. It can be seen that it has poor PSSR performance for frequency higher than 200 KHz. Low frequency noise like 50Hz supply ripple is effectively rejected. In this design 13.56 MHz ripple and its first harmonics is expected in the input of LDO because rectified output from rectifier operating at 13.56 MHz as input signal is used as supply and/or input for this LDO. Unfortunately, PSSR performance is worst around this frequencies. However the ripple rejection is still -36 dB at 13.56 MHz which is decent. As seen in figure 2.9, the open loop gain of LDO feedback circuit is 90 dB, which has contributed in achieving decent PSSR even

at higher frequency[11]. This paper also discusses that UGF frequency corresponds to the roll off frequency of PSSR, which can also been seen by comparing plots 2.9 and 2.10. The stability technique in this design also gives adverse effect on PSSR performance as UGF is significantly lowered by large output capacitor.

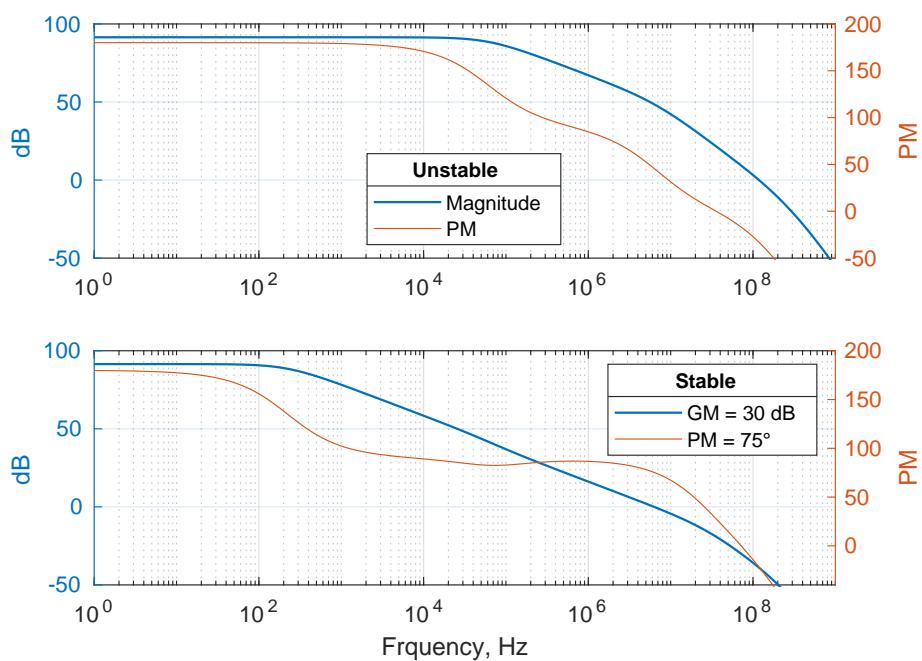


Figure 2.9: LDO stability before and after compensation

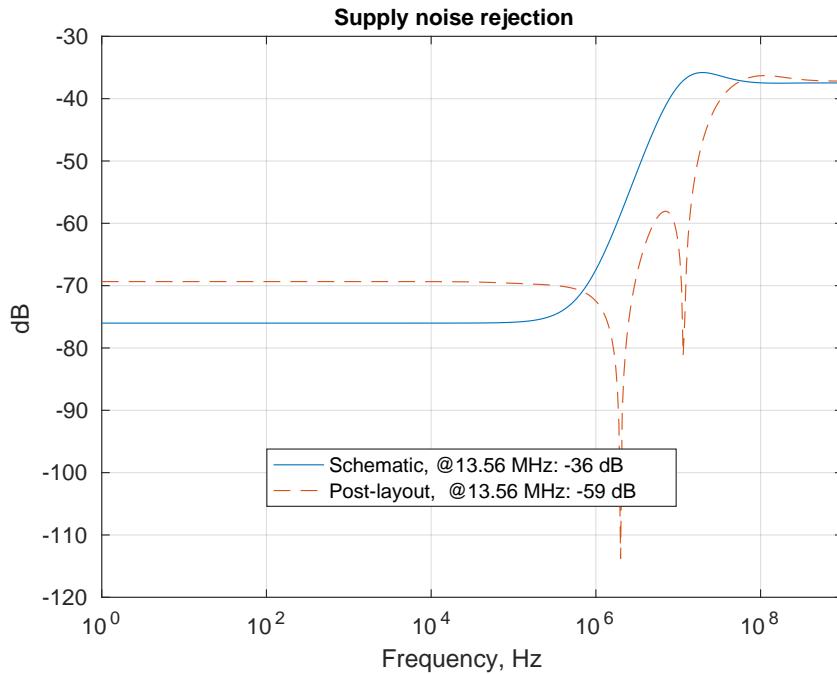


Figure 2.10: PSSR performance

Table 2.2 summarizes the performance of LDO regulator discussed above. Power efficiency is calculated as power delivered to load to power consumed from the source. Quiescent current includes biasing currents for error amplifier, feedback resistors and buffer which is obtained by taking the difference of current drawn from the source and current delivered to the load. Both power efficiency and quiescent current is calculated for maximum load operation.

Table 2.2: LDO performance summary

	Schematic	Post-layout
PSSR	-36 dB @ 13.56 MHz	-59 dB @ 13.56 MHz
Phase margin	75°	
Gain margin	30 dB	
Power efficiency	80.9 %	81 %
Quiescent current	105 uA	114 uA
Load regulation	17 uV/mA	53 uV/mA
Line regulation	435 uV/V	-1.162 mV/V

Chapter 3

Antenna Design

3.1 Introduction

All the components discussed above are part of any power management system which takes DC input from power line and creates regulated output as required. However, the objective here is to replace direct power line connection with wireless link. Since the intention is to just create a wireless power transfer link, the option which is easier to implement, convenient to operate and gives higher transfer efficiency is the primary choice here. And the literatures in wireless power transfer studies show inductive coupling meets all these requirement.

Inductive coupling boils down to principle of electromagnetic induction. When alternating electric current is passed through a coil, say primary, it generates alternating magnetic field. If another coil, say secondary, is placed in this changing magnetic field, alternating voltage/current is induced in the coil. In other word, power from primary coil is transferred wirelessly to secondary coil through magnetic field and this is popularly known as inductive power transfer link. And this induced ac voltage is rectified and then used to power up the load.

The energy transfer efficiency between the coils depends on how much of the magnetic field generated by the primary is captured by the secondary coil. And the capture of magnetic field by the secondary coil in turn depends on shape and size of two coils, their separation and alignment. All these factors influencing the transfer efficiency collectively gives a quantity called coupling factor, k . A perfect inductive link has a coupling factor 1, which means all the magnetic flux generated by primary is captured by secondary. However normally achieved coupling factor in practical inductive link is 0.3 and at best 0.5. So for better transfer of efficiency, some improvisation is done to the inductive link, so that efficiency is less affected by coil separation and alignment. This is done by tuning both the primary and secondary coil to same frequency i.e. creating resonance at some frequency so that coil coupling

is the strongest at that frequency. This method of creating better wireless energy transfer link is popularly known as magnetic resonance coupling.

In this project, first an antenna coil is designed and characterised. Then inductive link created using that antenna is studied and finally magnetic resonance technique is implemented to increase transfer efficiency at the operating frequency. The antenna dimensions are provided by Nordic Semiconductor which is one of their design already used in some application. Since having similar shape and size of antennas is important in gaining more transfer efficiency, the same antenna type is used as both primary and secondary coils.

3.2 Inductor model

Figure 3.1 is a lumped model of a planar antenna/coil/inductor made on a PCB. R_p , series DC resistance of wire and C_p , inter-winding self capacitance. These parasitics determine quality factor and self resonance frequency, SRF of the antenna. The quality factor is given as $Q = \omega L / R_p$ and SRF as $SRF = 1 / (\sqrt{LC_p})$, for this simple model.

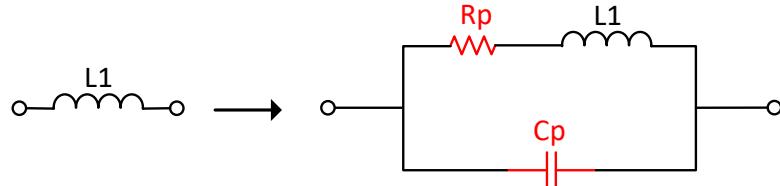


Figure 3.1: Real antenna model

For purpose of this work, with provided dimensions of the antenna, it is first modelled in HFSS as shown in figure 3.2a and its equivalent lumped circuit in figure 3.2b. It is important to note here that L1 in 3.2b is in fact 3.1. However, in the discussion ahead, these parasitics are not explicitly mentioned because the parameter extraction will include these factors too. To realise a real antenna, physical parameters of materials used for making printed antenna on a PCB are also given for the model. After completing model, frequency sweep is done for extracting S parameter of the antenna which was eventually used to estimate self inductance of the modelled coil. The performance estimation of single antenna here and couple system later is based on formulas in [12]. In order to check and compare the estimated inductance value from the model, Modified Wheeler Formula, a mathematical approximation model described in [13] is used. The qualities of antenna obtained

from extracted S-parameter are listed in table 3.1. The table shows that modelled inductance value is less than mathematically approximated value. This difference can be explained with two things. Firstly, mathematical calculation assumed that the antenna is spiral and rectangular with sharp edge but the model has rounded edge. Secondly, during modelling besides dimensions of the coils, physical parameters of coil materials are also used but these are not considered for mathematical calculation.

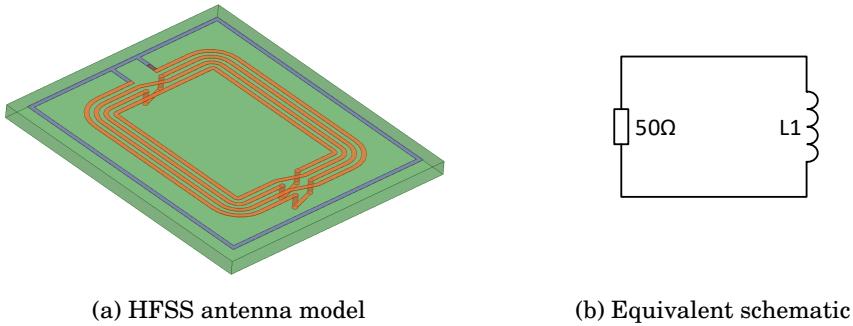


Figure 3.2: Antenna model

Table 3.1: Characterisation of antenna

	HFSS model	Modified Wheeler [13]
Self Inductance	448 nH	644 nH
SRF	125 MHz	
Quality factor		
Parasitic Resistance		
Parasitic Capacitance		

3.3 Inductive transfer link

In the next step, an inductive link is realised by using two antennas: one as primary and other as secondary, aligned one over other and separated by air gap as shown in figure 3.3a, equivalently shown as lumped schematic in figure 3.3b. Coupling system of these antennas is simulated for varying distance of magnetic field interaction to observe the difference in performance. The same procedure as used for single coil above, is used to extract self inductance of each coil, L_1 and L_2 , mutual inductance of two coils, L_{12} , coupling coefficient between the coils, k and quality factor, Q . The extracted values for coil separation of 1mm, 5mm and 10mm are listed in table 3.2 calculated at operating frequency of

13.56 MHz.

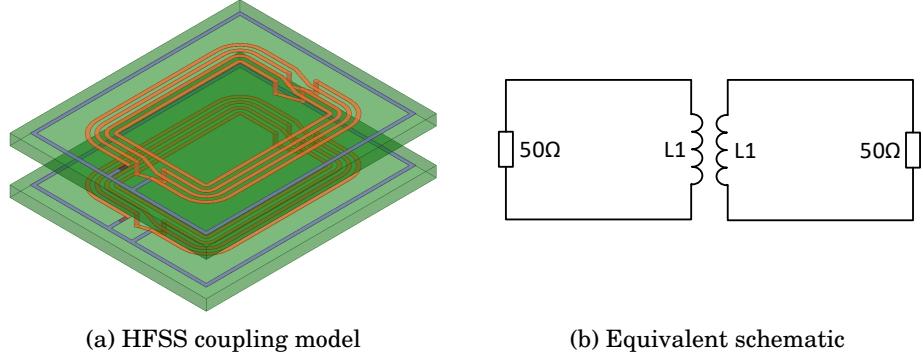


Figure 3.3: Antenna coupling model

Table 3.2: Coupling parameters for varying coils distance

Parameter	1 mm	5 mm	10 mm	mm
L1	-	-	-	nH
L2	-	-	-	nH
L12	-	-	-	nH
k	-	-	-	-
Q	-	-	-	-
SRF				

It is observed that $L1$ and $L2$ are same as in table 3.1 as it is the same coil used as primary and secondary. Similarly $L12$ and k , related as $L12 = k\sqrt{(L1L2)}$, are both decreasing with distance as expected. With increase in separation, less and less magnetic flux generated by primary coil is linked with the secondary, creating a loosely coupled inductive link.

The power transfer efficiency of the physical link created by coupled coils is very important. [CITE] states that efficiency depends k of coupling system and Q of coil and hence high k and high Q is always desirable and obviously coil optimisation is the most important part of coupling system design. [14] and [15] discusses some techniques to optimise transfer efficiency of inductive link: [14] about matching the load for better resonance whereas [15] about designing optimal coil geometry for higher Q . The former one compares the efficiency of general inductive coupling and conventional resonant coupling and their limitation in achieving higher efficiency. This eventually proposes optimal resonant load transformation which has better immunity to poor coupling and load variation. Likewise, the later one describes step by step iterative

process of designing an antenna with optimal geometry for the given design constraints.

3.4 Magnetic resonance coupling

In this project, conventional magnetic resonance coupling as in is implemented to tune both primary and secondary to the power career frequency. The purpose here is to match the impedance of primary antenna to source impedance and secondary antenna of coupling system to load impedance in order to maximize the power transmission from the source to the load.

For the purpose of making a resonant inductive link, the S parameter of coupled antenna system in HFSS is exported to ADS in order to design matching networks using capacitors only. Impedance of primary antenna is matched to 50Ω source resistance and impedance of secondary is matched to load impedance (50Ω load or input impedance chip(?)) as shown in 3.4. C_{p1} , series capacitor and C_{p2} , shunt capacitor together with L_1 created parallel resonant circuit at 13.56 MHz on the primary side and C_{s1} , shunt capacitor together with L_2 creates the secondary resonant circuit at same operating frequency. Thus a pair of LC tank circuit is made tuned at same frequency. Such matching network is designed for all three coil separation distances as above, but resonant coupling system with 5 mm separation is taken as a typical example and presented here.

The reflection power loss, S_{11} and S_{22} , at both primary and secondary terminal, power transfer gain, S_{21} , from primary to secondary and Q-factors for both antennas before and after creating resonance are shown in figure 3.5, this and this.

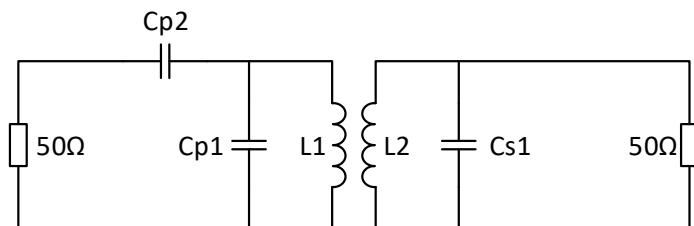


Figure 3.4: Resonant coupled inductive link

The performance of magnetic resonant coupling link designed in this work is summarises in table 3.3 below.

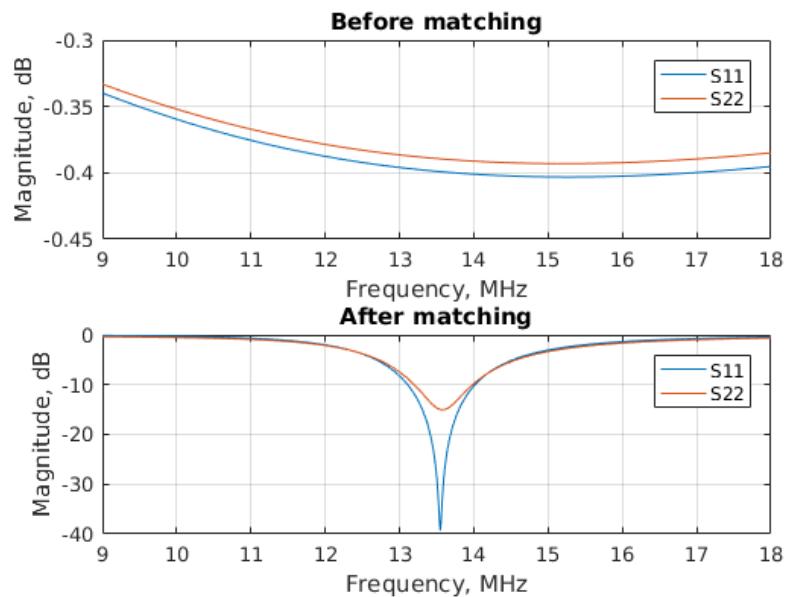


Figure 3.5: Power loss before and after matching

Table 3.3: Performance of resonant inductive link

C_{p1}	C_{p2} and C_{s1}	
Resonant frequency	13.56 MHz	
Primary reflection loss		
Secondary reflection loss		
Primary to secondary gaining		
Q-factor		

Part II

WPT System Design and Implementation

Chapter 4

Power Receiving Unit Design

4.1 Introduction

Wireless power transfer, WPT system always constitutes two main units: power transmitting unit, PTU and power receiving unit, PRU. Each unit comprises of resonator, power conditioner and control circuits as shown in figure 4.1. Both the resonators in PRU and PTU are tuned to operating frequency, which create a physical transfer link. Power conditioner circuit in PTU includes at least power amplifier and matching circuit, whereas in PRU, it includes matching circuit, rectifier and regulator. Similarly both these units have control block which facilitates transfer procedure and communication between these units. In this work, design and analysis of PRU is the main objective.

In figure 4.1 above, the block highlighted in blue is the PRU system in this design. Secondary coil, Rx is the receiver resonator, and rectifier and regulator is power conditioning block. The primary coil is driven by a power source and AC signal is generated at the secondary as discussed earlier in antenna design section. The rectifier then rectifies this AC signal to DC. The DC output of the rectifier is then fed to LDO to produce regulated DC output required to drive a load. The reference and biasing circuit generates required reference and biasing DC voltages for the LDO.

The PRU unit is broken down into two sub units for step wise analysis. As seen in the block diagram, it is functionally divided into Transfer Link and Power Management System (PMS). Firstly, PMS is simulated excluding the transfer link to characterise the performance of PMS. Secondly, the whole PRU system: PMS with transfer link created with coupled antenna, Tx and Rx, is simulated to observe the performance of whole PRU. Though it has already been told earlier, one important thing must be mentioned here again before going further. Even though reference and biasing circuit has been integrated into the PMS

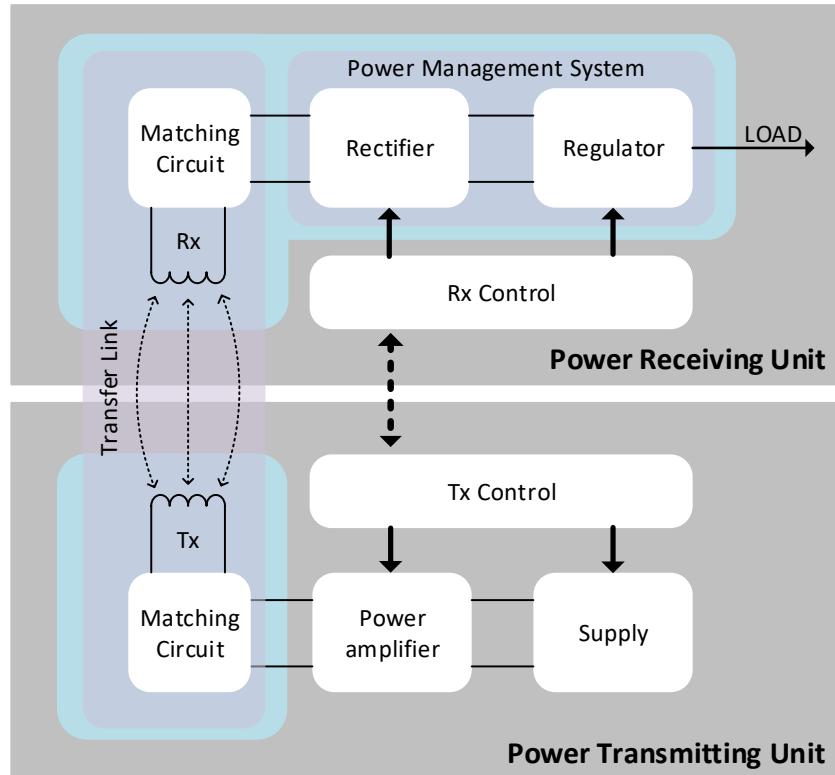


Figure 4.1: WPT block diagram

system, it has been designed with an option to override it externally. This externally supplied reference and biasing will be primarily used for the PRU system simulation. The result with on-system biases and reference will be explicitly noted when used.

4.2 Power Management System

Figure is the top level of PMS in this design. The purpose here is to see Vrec and Vreg outputs while driving maximum load. The voltage biases outputs to examine the performance of BGR circuit which is disable now with external control signal Vctl low. The test bench setup is a shown in figure .

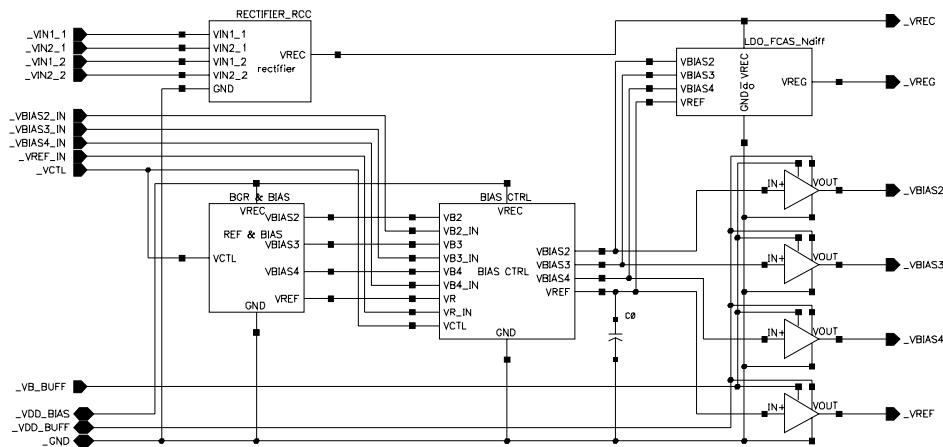


Figure 4.2: WPT PMS implementation

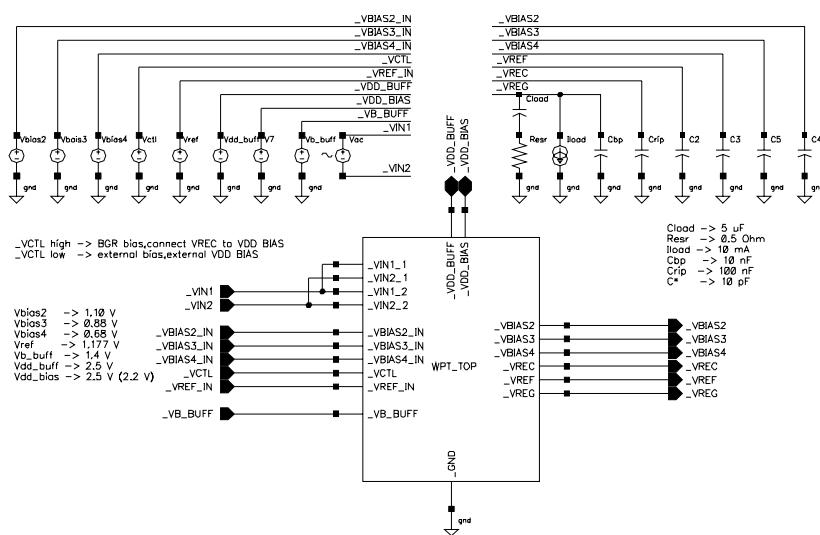


Figure 4.3: Test bench for PMS simulation

4.2.1 Transient Response

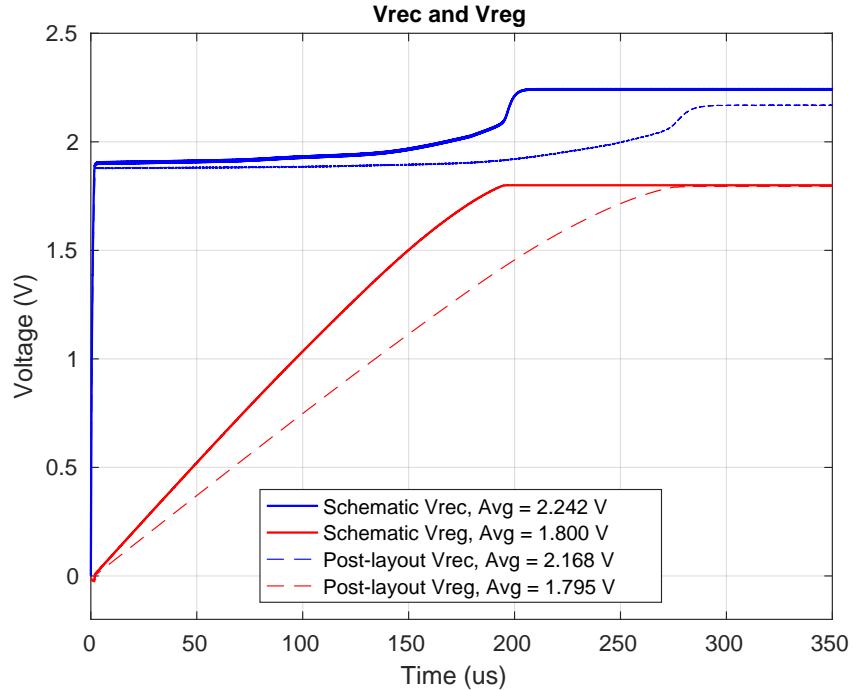


Figure 4.4: Transient

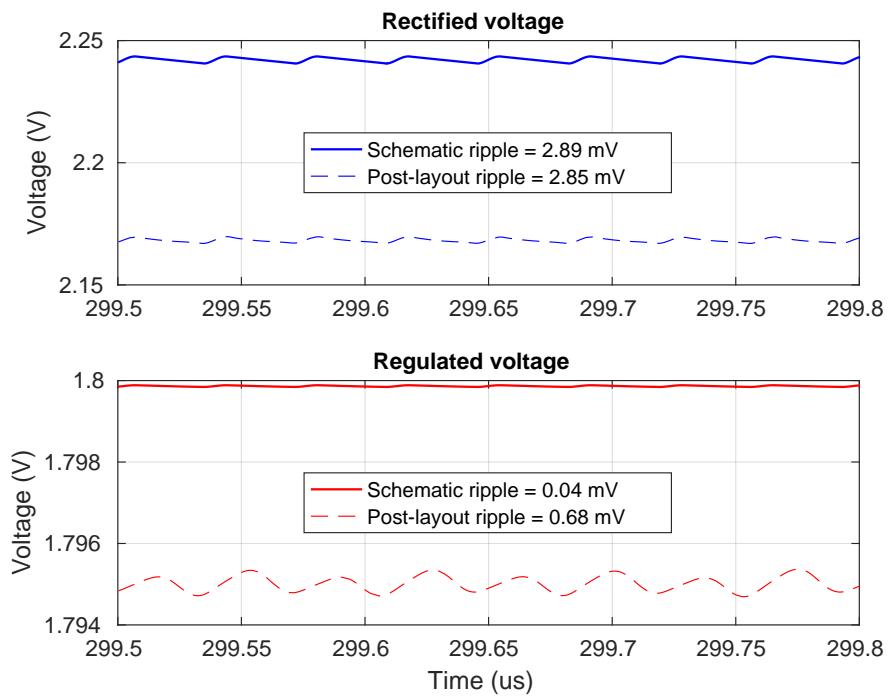


Figure 4.5: Ripple in V_{rec} and V_{reg}

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Acronyms

- CMOS** complementary metal-oxide-semiconductor
- DC** direct current
- ESR** equivalent series resistance
- GM** gain margin
- ICMR** input common mode range
- MOS** metal-oxide-semiconductor
- nMOS** n-channel MOS
- PCE** power conversion efficiency
- PM** phase margin
- pMOS** p-channel MOS
- PMS** Power Management System
- PRU** Power Receiving Unit
- PSSR** power supply rejection ratio
- PTU** Power Transfer Unit
- SMPS** switch mode power supply
- SRF** self resonance frequency
- UGF** unity gain frequency
- VCE** voltage conversion efficiency
- V_p** peak voltage
- V_{pp}** peak to peak voltage
- V_{tn}** thresold voltage of n-channel MOS
- V_{tp}** thresold voltage of p-channel MOS
- WPT** Wireless Power Transfer

