Application Notes

This issue features two Application Notes. The first can be found below, and the second starts on page 94 ("A 2.4-GHz Radio Front End in RF System-on-Package Technology" by S. Chakraborty, K. Lim, A. Sutono, E. Chen, S. Yoo, A. Obatoyinbo, S.-W. Yoon, M. Maeng, M.F. Davis, S. Pinel, and J. Laskar).

Quality Factor and Inductance in Differential IC Implementations

■ **Ryan L. Bunch, David I. Sanderson, Sanjay Raman**

Voltage-controlled oscillators (VCOs) are critical components for signal generation and frequency selection in RF/microwave transceivers. Recently, there has been considerable interest in monolithic integration of inductance-capacitance (*LC*) tank oscillators for highly integrated RF transceivers [1]. Technologies such as Si complimentary metal-oxide-semiconductor (CMOS) and Si/SiGe BiCMOS are of interest in light of the potential for integration with digital functions.

The operation of an oscillator can be described using the concept of "negative resistance." In an oscillator, an active network with negative transconductance, $-G_M$, is connected to an *LC*-tank circuit with an equivalent parallel resistance, R_p. The equivalent negative resistance ($1/-G_M$) looking back into the transconductor is chosen to cancel the equivalent parallel resistance of the tank circuit. R_p is obviously related to the quality factor Q of the L and C components. In Si technologies, the Q of the inductor is usually the limiting factor.

Differential topologies are advantageous in integrated circuits (ICs) because they offer common-mode rejection. Therefore, differential circuits are less susceptible to supply noise present in on-chip power rails. Many RF integrated circuits (RFICs) utilize double-balanced Gilbert-cell mixers because they offer conversion gain while minimizing local oscillator (LO)/intermediate frequency (IF) feedthrough and even-order mixing products. Differential VCO topologies avoid the need for single-ended to differential conversion circuitry for the LO drive of a Gilbert-cell mixer. Figure 1 shows a differential CMOS complementary $-G_M$ oscillator [2], [3]. In this case, the negative resistance seen by the tank is given by

$$R_{\text{negative}} = \frac{-2}{G_{Mn} + G_{Mp}}. \tag{1}$$

Some confusion exists in the literature regarding how the Q and L of a monolithic inductor should be defined, particularly with regard to differential (balanced) versus single-ended (unbalanced) implementations. A general model of a monolithic inductor is used in this article to show how Q and L are defined for both single-ended and differential configurations. This article focuses on modeling and characterizing monolithic differential inductors on low-resistivity Si substrates in a standard CMOS process. However, the techniques presented here are equally applicable to monolithic inductors in other technologies.

Inductance and Quality Factor

An important quantity in the characterization of resonant tank circuits is the Q, which is defined as

$$Q = 2\pi \frac{\text{maximum energy stored}}{\text{energy dissipated per cycle}}. \tag{2}$$

The resonator Q strongly influences both the phase noise and power consumption of an oscillator. The inductor in an *LC* oscillator is usually the most critical circuit element in the design. Typically, the Q of the inductor dominates the total Q of the tank circuit. In addition, the tuning range of a VCO is strongly affected by the self-resonant frequency (f_{sr}) of an inductor. The self-resonant frequency is that frequency at which the induc-

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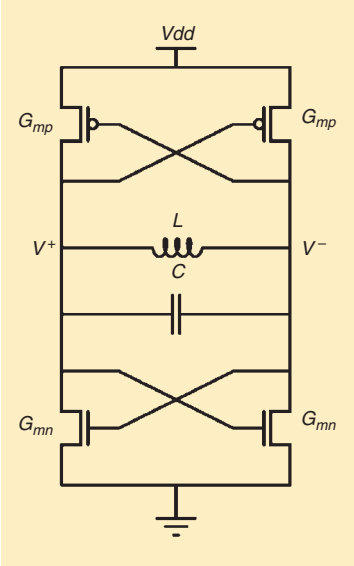

Figure 1. *A CMOS complementary -G_M oscillator.*

tor's capacitive parasitics result in a zero-net reactance; beyond this frequency the inductor appears capacitive.

Traditionally, inductors have been incorporated as discrete components located off-chip, often as small surface-mount parts. While such inductors can have extremely good performance, it is desirable to eliminate as many off-chip discrete components as possible. This reduces the board-level complexity and component count, which in turn leads to a direct reduction in cost. As an alternative to off-chip inductors, some RFICs have utilized bonding wires as hybrid inductors [1], [4]. While bonding wires can have a relatively high Q (on the order of 50), they can also suffer from large variations in L, since wire bonding is a mechanical process that cannot be as tightly controlled as a photolithographic processes.

Monolithic inductors fabricated as simple planar spirals are widely used on GaAs substrates with Qs in the range of 20-40. However, inductor Qs on standard (low-ρ) Si substrates are much lower. The L of a monolithic inductor is defined solely by its geometry. Since modern photolithographic processes provide extremely tight geometric tolerances, monolithic inductors have very small variations in their performance.

Monolithic Inductor Geometries

There are many ways to lay out a planar spiral inductor. The optimum structure is a circular spiral. This structure places the largest amount of conductors in the smallest possible area, reducing the series resistance (R_s) of the spiral. This structure, however, is often not used because it is not supported by many mask generation systems. Many of these systems are able to only generate Manhattan geometries (and possibly 45° angles as well). Manhattan-style layouts only contain structures with 90° angles, like the streets of Manhattan (New York, USA). While the curved metal traces can be approximated in a step-wise fashion, a simpler solution is to approximate the circle with a polygon. An octagonal spiral has a Q that is slightly lower than the circular structure but is much easier to lay out. For the CMOS process used here, non-Manhattan shapes are allowed but not recommended. For this reason, the standard square spiral structure of Figure 2 was chosen. The square spiral structure does not have the best performance, but it is one of the easiest structures to lay out and simulate.

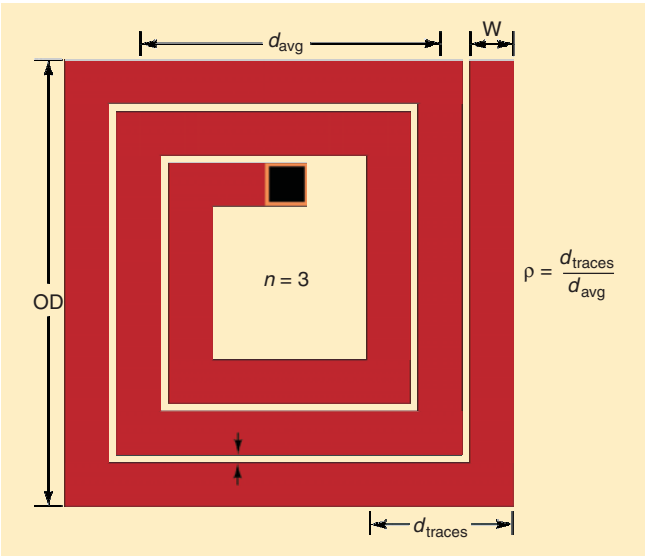

Figure 2. *A square spiral inductor.*

The square spiral inductor has been studied extensively [5]-[7]. The following expression has demonstrated good accuracy for predicting the L of a square spiral [8]

$$L = \frac{2\mu_0 n^2 d_{avg}}{\pi}\left[\ln\left(\frac{2.067}{\rho}\right) + 0.178\rho + 0.125\rho^2\right] \quad (3)$$

where n is the number of turns in the spiral, μ_0 is the permeability of free space, d_{avg} represents the average diameter of the spiral, and ρ represents the percentage of the inductor area that is filled by metal traces. The parameters d_{avg} and ρ are defined in Figure 2. Equation (3) is based on a current sheet approximation of the spiral structure, and is valid only for square spirals ([8] also presents a range of expressions that are valid for other geometries). Predicting parameters, such as inductor Q and f_{sr}, generally cannot be done with a simple formula. These parameters are usually obtained through full-wave electromagnetic (EM) simulation.

Losses in Spiral Inductors

There are several sources of loss in a spiral inductor. The most obvious loss mechanism is the series winding resistance, R_s. The interconnect metal used in most CMOS processes has typically been aluminum (however, copper interconnection is now in widespread use). Depending on the metalization thickness and particular aluminum alloy used, the sheet resistivity can be anywhere from 30-70 mΩ/□. The dc resistance of the spiral is easily calculated as the product of this sheet resistance and the number of squares in the spiral. However, at higher frequencies, the resistance of the spiral increases due to the skin effect and "current crowding" at the corners of each turn.

The introduction of copper metalization and thick upper-level interconnect have yielded improvements in maximum inductor Qs reported in silicon [5]. In addition, multiple levels of metalization may be strapped together to create a spiral with a lower dc winding resistance [9]. However, standard CMOS substrate losses ultimately remain the limiting factor, even when the conductivity of the spiral windings is no longer an issue. Since the silicon substrate is neither a perfect

conductor nor insulator, there are resulting losses in the reactive fields that surround the windings of the spiral.

In a CMOS process, the windings of the spiral are separated from the substrate by a thin layer of silicon dioxide (SiO_2). This creates capacitance between the spiral and the surface of the substrate. In most modern CMOS processes, this substrate is a heavily doped p-type material and is tied to ground potential. Thus, the substrate appears as a grounded resistor in series with this capacitance. This substrate capacitance has two detrimental effects on a monolithic inductor: 1) it allows RF currents to interact with the substrate, lowering the inductor; and 2) it increases parasitic capacitances, reducing the f_{sr}. Reducing the trace width can decrease this capacitance, but this, in turn, will increase the series resistance of the inductor. This is an important tradeoff since wide traces are generally used in inductors on silicon to overcome the low thin-film conductivity of the metalization. This also limits the feasibility of creating arbitrarily large valued inductances.

There are also losses due to the magnetic field in the inductor structure. The magnetic field extends around the windings of the spiral and into the substrate. Faraday's Law states that this time-varying magnetic field induces an electric field in the substrate. This field forces an image current to flow in the substrate in the opposite direction of the current in the winding directly above it. These image currents can account for 50% or more of the losses in a CMOS inductor [1]. This effect can also be thought of as a parasitic transformer, where the substrate represents an unwanted secondary winding. Larger inductors have magnetic fields that penetrate deeper into the substrate, and, therefore, suffer from higher substrate losses. This effect is in opposition to the goal of limiting series resistance with wide spiral traces. Use of nonstandard high-resistivity Si substrates [9], or a post-process micromachining step to etch the substrate away under the inductor [10], can minimize these substrate effects.

The magnetic field not only penetrates into the substrate but also into the other windings of the coil, further increasing the loss [1]. Eddy currents generated in the center of a winding cause the inner turns of the inductor to contribute much more loss to the inductor, while having a minimal impact on the actual L. This phenomenon is sometimes referred to as "current crowding" [11], [12]. In [11], a nine turn inductor was simulated using a finite-element field solver. It was found that the resistance of the outer turn at 2 GHz was 18% higher than its dc value; however, the resistance of the inner turn at 2 GHz increased by 480% over its dc value. For this reason spiral inductors on silicon typically utilize "hollow" centers in order to increase their Q [1].

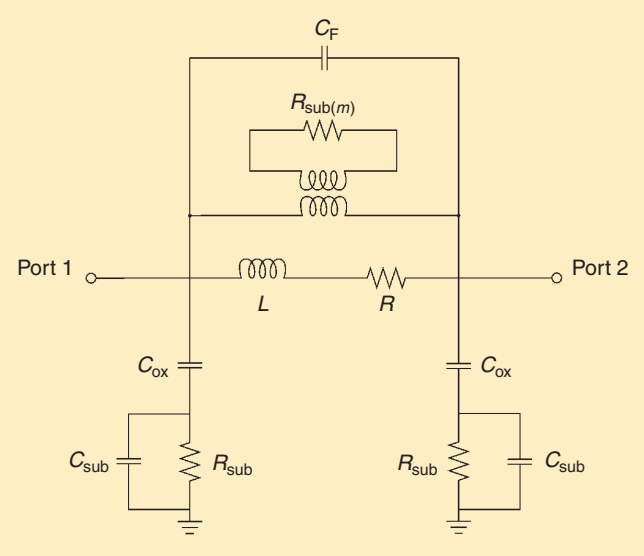

Figure 3. *General spiral inductor lumped circuit model.*

Inductor Circuit Models

A general circuit model for a monolithic inductor on a low-resistivity substrate is shown in Figure 3 [7]. This model includes circuit elements that model the loss mechanisms that were discussed in the previous section. This circuit accurately models inductors on low resistivity silicon substrates because it includes the effect of the magnetic eddy currents. The magnetic substrate loss is represented in this model as an ideal transformer coupled to the resistor, R_m.

Typically, the L of a monolithic inductor is calculated by converting measured or simulated S-parameters into Y-parameters. These Y-parameters are then used to extract the value of L and Q. In cases where one side of the inductor is grounded (i.e. single-ended or unbalanced), L is often defined as

$$L = \mathrm{Im}\left(\frac{1/Y_{11}}{2\pi f}\right). \tag{4}$$

In other cases where the inductor is used differentially (i.e., balanced), L is often defined [6], [7], [13] as

$$L = \mathrm{Im}\left(\frac{1/Y_{12}}{2\pi f}\right). \tag{5}$$

Depending upon the specific inductor application, either of these expressions may be acceptable.

To understand the difference between the above definitions, it is helpful to look at the π-equivalent of a two-port network (Figure 4). This circuit model expresses the two-port, Y-parameters as admittances in a π-network. For a passive reciprocal network, $Y_{12} = Y_{21}$; if the network is symmetric, $Y_{11} = Y_{22}$. To define L and Q, this π-model must be reduced to a single element (i.e., an L in series or parallel with a resistance). For the case of a simple series element $R \neq jX$,

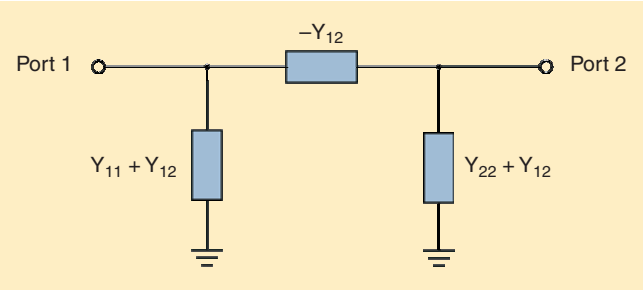

Figure 4. *π-equivalent circuit for a two-port network.*

$$L = \frac{X}{2\pi f} \tag{6}$$

and

$$Q = \frac{X}{R}. \tag{7}$$

There are two simple methods of reducing the π-circuit to the series element, $R+jX$ (Figure 5). If port 2 of the π-circuit is grounded, the $Y_{22}+Y_{12}$ element is bypassed, and the circuit looking into port 1 reduces to the admittance Y_{11} connected to ground (since admittances add in parallel, Y_{12} is eliminated). Converting admittance to impedance, $R+jX$ becomes

$$R + jX = \frac{1}{Y_{11}}. \tag{8}$$

If this assumption is valid, L is defined using (4), and

$$Q = \frac{\mathrm{Im}\left(1/Y_{11}\right)}{\mathrm{Re}\left(1/Y_{11}\right)}. \tag{9}$$

This method is valid if the inductor will be used in a circuit where one terminal of the inductor is connected to ac ground. This is often the case in many RF circuits, particularly in low-noise amplifiers (LNAs) and mixers where inductors are used for degeneration or loading. This method is also equivalent to taking one-port S-parameter measurements with one terminal of the inductor grounded and converting the measured reflection coefficient Γ into an input impedance. The series impedance is given by

$$R + jX = Z_{\mathrm{in}} = Z_0 \frac{1+\Gamma_1}{1-\Gamma_1}, \tag{10}$$

where

$$\Gamma_1 = S_{11}.$$

On the other hand, if the inductor will be used in a differential configuration (i.e., neither port is at ac ground potential) a different approach is required. The *floating* impedance, $R+jX$, seen between ports 1 and 2 of the π-network is

$$R + jX = \left(-\frac{1}{Y_{12}}\right) \Big\| \left(\frac{1}{Y_{11}+Y_{12}} + \frac{1}{Y_{22}+Y_{12}}\right) = \frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2}. \tag{11}$$

The impedance calculated in (11) is referred to as *floating* since it ignores the ground connection in the equivalent circuit. This is valid because, if the inductor is connected in this manner, the ground (as represented in Figure 4) is no longer explicit and exists only as a "virtual ground." Inductors connected in this manner are often referred to as "floating" or "differential." In this case, the shunt elements $Y_{11}+Y_{12}$ and $Y_{22}+Y_{12}$ of the π-network are the parasitic capacitances to ground [perhaps in series with a substrate resistance (Figure 3)]. These shunt elements are often ignored, particularly in technologies using semi-insulating substrates; in this case, L is calculated using (5), and Q is calculated using

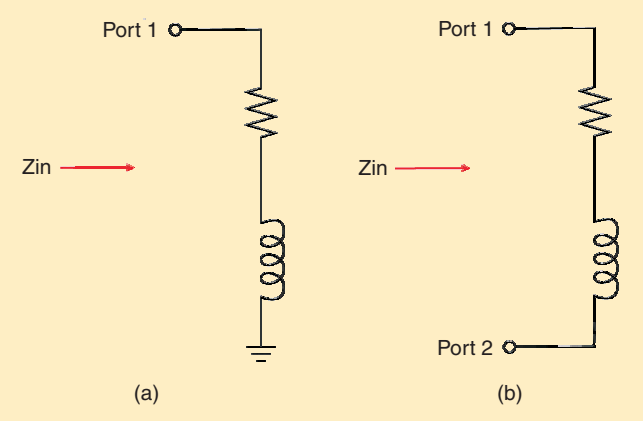

Figure 5. *Two methods of reducing the π-network (a) single-ended and (b) differential configurations.*

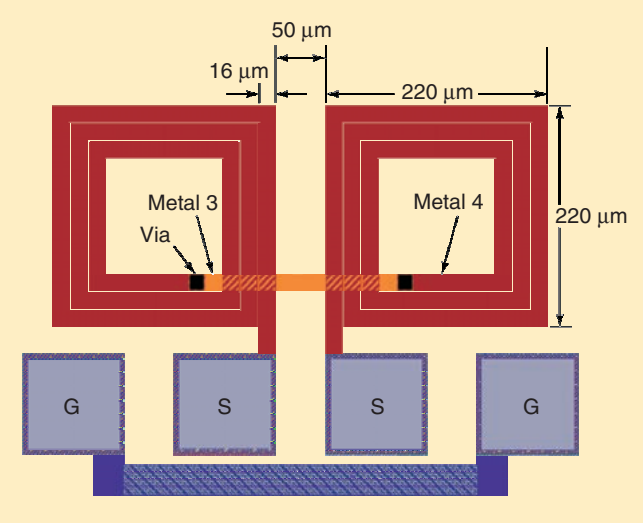

Figure 6. *Series connected differential inductor used in a complementary G_M LC VCO.*

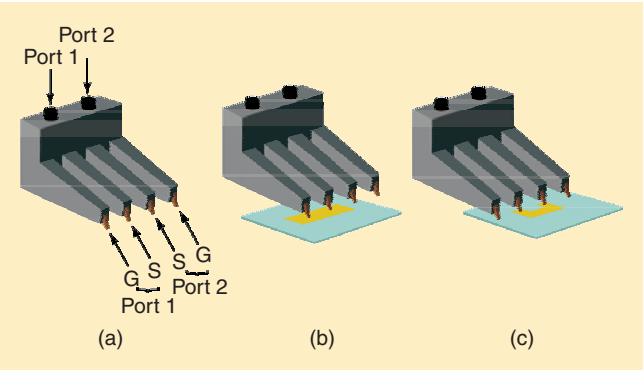

Figure 7. *GS/SG probe two-port SOLT calibration: (a) definition of ports; (b) an example of measuring short standard across port one (the load measurement is done in the same manner using the 50-Ω load standard; the open standard is measured with the probes off the substrate); and (c) an example of measuring the thru standard.*

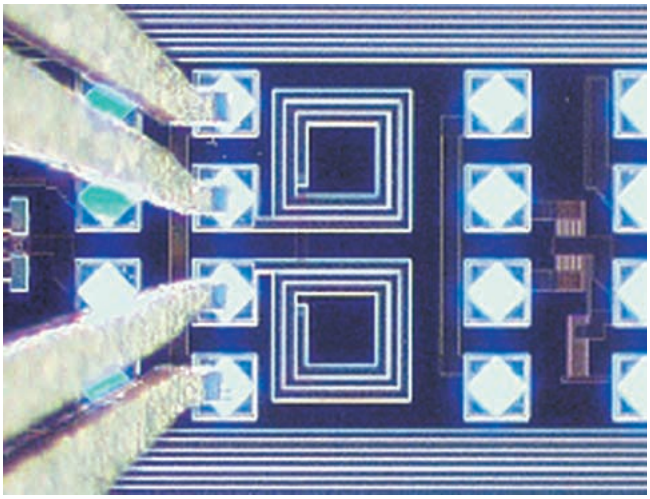

Figure 8. *GS/SG probe two-port S-parameter measurement of a differential inductor.*

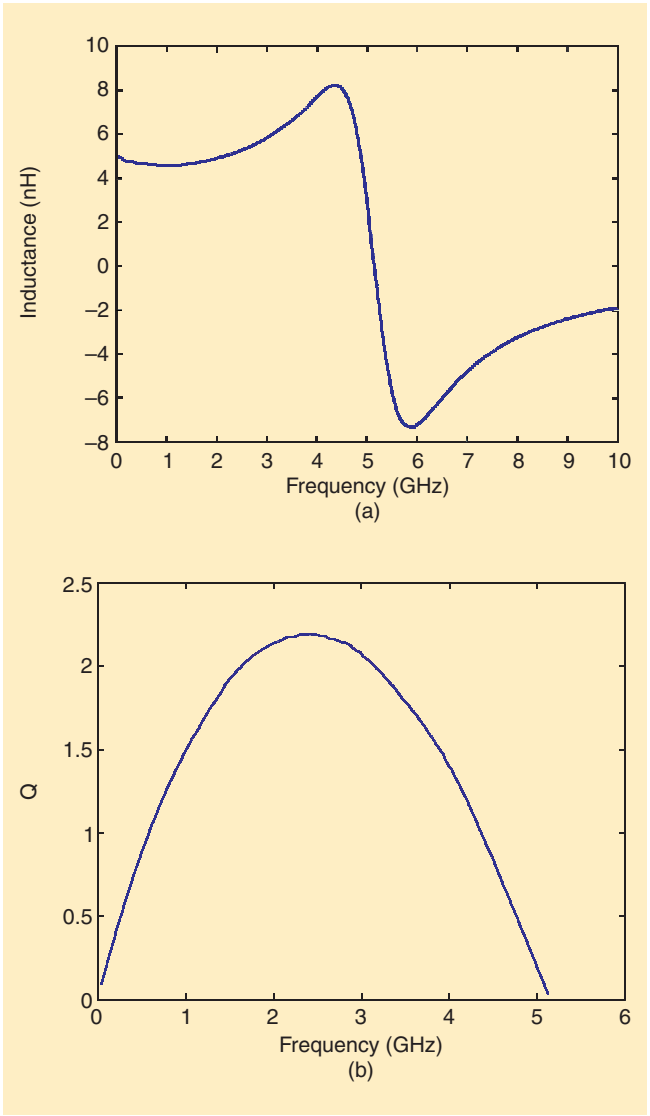

Figure 9. *Plot of the measured (a) inductance and (b) Q of the example differential inductor.*

$$Q = \frac{\mathrm{Im}\left(1/Y_{12}\right)}{\mathrm{Re}\left(1/Y_{12}\right)}. \tag{12}$$

In most cases, the differential Q measured using this method will be slightly higher (3-5%) than in the grounded, one-port case. If the shunt elements $Y_{11}+Y_{12}$ and $Y_{22}+Y_{12}$ are not negligible (as is the case in standard CMOS), it is more accurate to use (11) in conjunction with (6) and (7) to calculate L and Q, rather than using (5) and (12). It has also been shown [14] that *geometrically symemetric* inductors (as opposed to a pair of individual asymmetric inductors mirrored about the plane of symmetry) can have Qs on the order of 50% greater with differential excitation versus single-ended excitation.

Example Differential Inductor Measurement

A differential inductor was fabricated in a 0.35-µm single-poly, four-metal CMOS process (Figure 6). This inductor is a breakout of the differential inductor in the tank circuit of a CMOS complementary $-G_M$ LC VCO [3]. In this VCO, the total tank circuit L is implemented by connecting two inductors in series. This is done so that the differential oscillator will see a symmetric reactive load. The inductor is a three-turn spiral, with an outer diameter of 220 µm, a width of 16 µm, and spacing of 2 µm. Metal 4 is used for the square spirals because it is the thickest of the metals (~1 µm) and provides the lowest loss (0.05 Ω/□). Metal 3 is used to connect the inner loops of the two spirals. Full-wave EM simulations predicted a differential Q of 3.1 and L of 4.6 nH at 2.5 GHz.

The inductor layout requires a single ground-signal/signal-ground (GS/SG) probe to measure the two-port S-parameters [Figure 7(a)]. The short-open-load-through (SOLT) calibration of this configuration is done by measuring the short, open, and load standards across each individual port of the probe as in a normal GS and SG calibration using a Cascade impedance standard substrate [Figure 7(b)]. The thru standard is measured using a u-shaped structure to connect the two signal probe tips [Figure 7(c)]. Because the ground probe tips are connected internally to the probe body at RF frequencies, it is not necessary to have the two ground probe tips connected through a metal trace on the substrate; at higher microwave frequencies, a parallel ground path on the substrate connecting the two ground probe tips is advisable.

After performing the two-port GS/SG SOLT calibration on the network analyzer and probe station, a single GS/SG probe was used to measure the two-port S-parameters (Figure 8). The S-parameters were then converted to Y-parameters [15] for use in (6), (7) and (11) to find the inductor's L and Q. Figure 9 shows the resulting L and Q plotted versus frequency. The results match reasonably well with EM simulation with the exception of self-resonant frequency. This deviation is most likely due to the fact that the planar-EM solver does not account for finite side-wall thickness of the inductor traces, thereby underestimating the interwinding capacitance.

In [14], a procedure for calibrating and measuring symmetric inductor structures using a signal-ground-signal (SGS) probe configuration is presented.

Summary

Monolithic inductors are widely used in microwave ICs and RFICs. Design considerations for inductors on low-resistivity substrates have been described. A π-equivalent model, used to account for various loss mechanisms, can be helpful in understanding differences in the definition of L and Q for single-ended and differential structures that exist in the literature. Specific uses for the equations in this article have been outlined. The L and Q for an example monolithic, differential inductor were extracted from measured two-port S-parameters using equations for differential configurations on low-resistivity substrates. More details on this and related topics can be found in [16].

Acknowledgements

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