Poly-Si

Poly-Si Applications

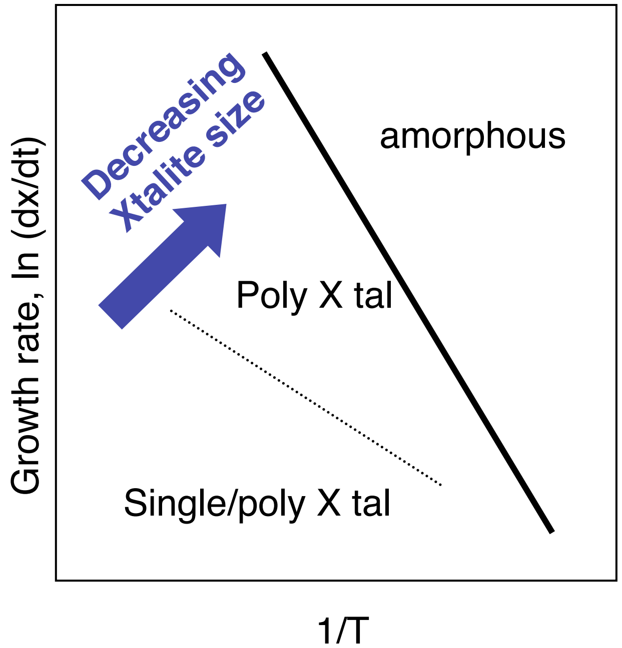
Gate in MOS transistor
Emitter contacts
Conducting paths in VLSI (=metallization)
Conducting plugs and vias
Resistors
Diffusion source for shallow junction
Structural thin film material in MEMS membranes/plates

Poly-Si preparation

In VLSI = CVD deposition

Film structure include grain size can in principle be varied by The temperature of deposition

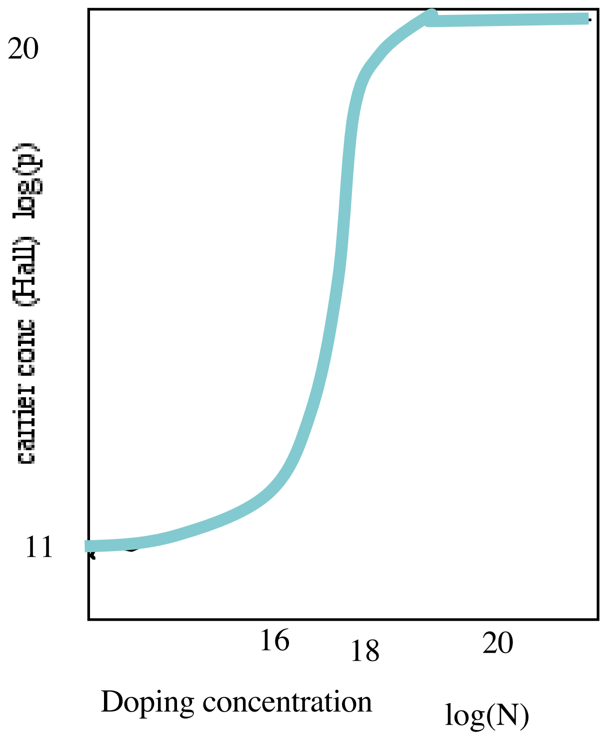
(supersaturation depends on *T* and deposition rate)

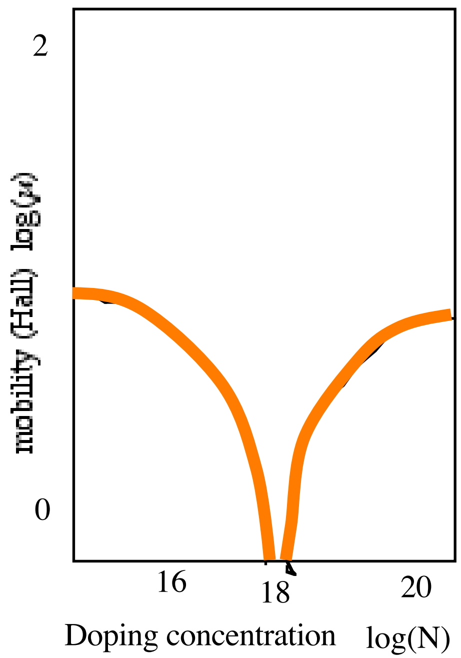


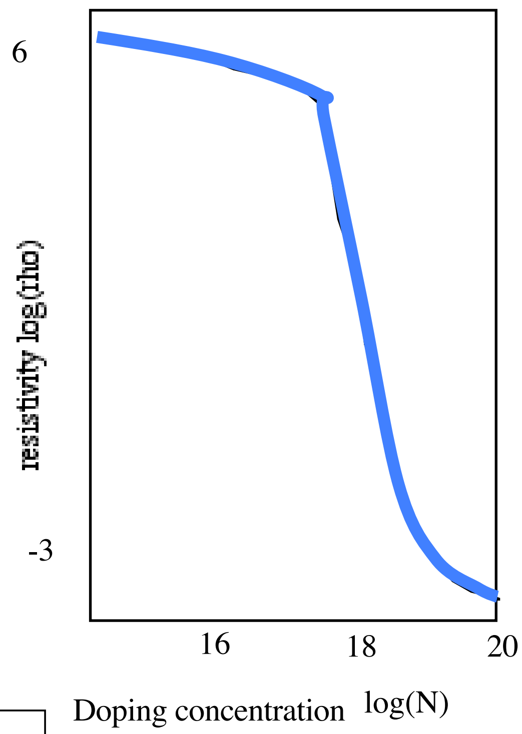
Poly-Si electrical properties

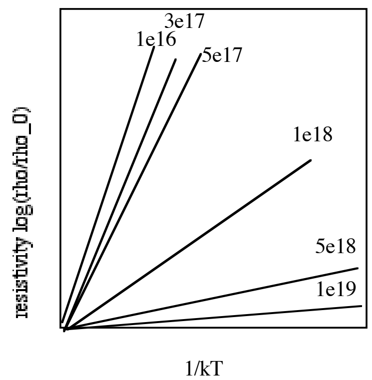
$$\rho = \frac{1}{\sigma} = \frac{1}{q\,\bar{n}\,\bar{\mu}}$$

Schematical reproduction of some experimental data



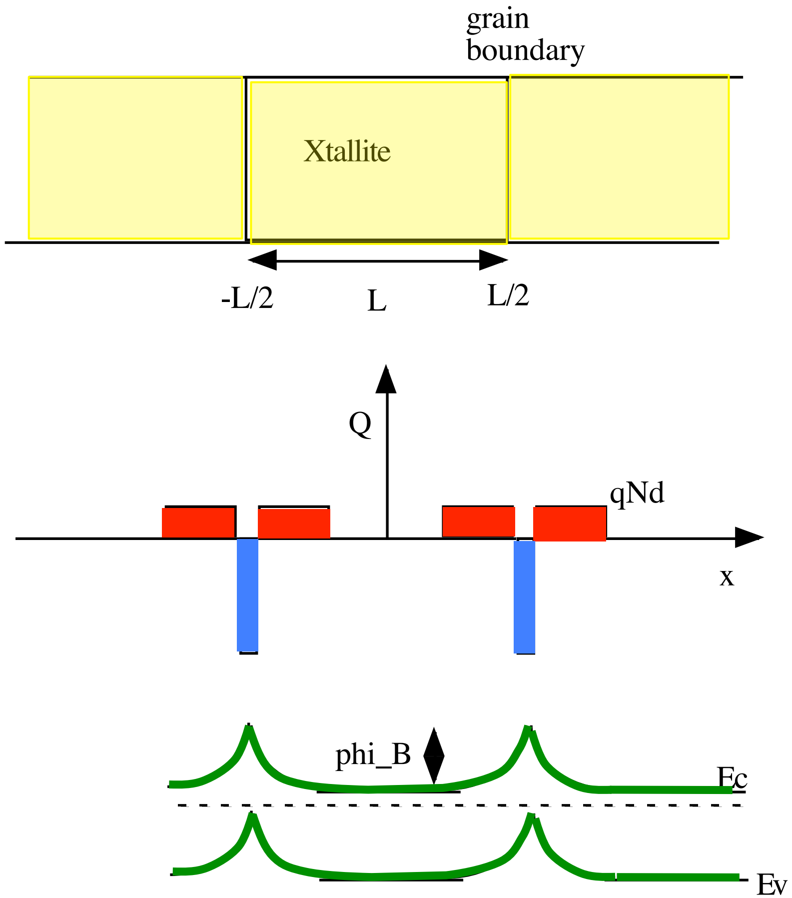




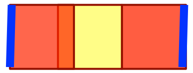


Poly-Si electrical properties - simple model

Schematic



$N_d * L > Qt$

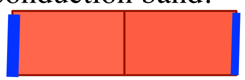


We have Poisson's equation $\dfrac{\partial^2 \phi}{\partial x^2} = \dfrac{qN_d}{K\varepsilon_o}$

The solution of this with the appropriate boundary conditions are

$$\phi(x) = \left(\frac{qN_d}{K\varepsilon_o}\right)(x - l)^2 + \phi_{co} \quad for \quad l < |x| < L/2$$

When $L*Nd < Qt$ we have, If we can arbitrary reference phi to the conduction band.



$$\phi(x) = \phi_{co} + \left(\frac{qN_d}{K\varepsilon_o}\right)x^2$$

The energy barrier is thus $\quad {}_B = |\phi(0) - \phi(L/2)| = \dfrac{qL^2}{8K\varepsilon_o}N_d$

Since the electron concentration depends on the distance between the Fermi level and the conduction band we can calculate its distribution in the grain $\quad n(x) = N_c \exp(\dfrac{-q\phi(x) - E_F}{kT})$

and the “average” electron concentration is $\quad \bar{n} = \dfrac{1}{L}\displaystyle\int_{-L/2}^{L/2} n(x)dx$

The position of the Fermi level is found from the condition of charge neutrality

We can now draw a graph showing how the barrier varies with donor concentration