

# FYS 4310/9310

Administrative:

welcome

language

contact

www

times

formular

textbook

other texts

handouts

Course introductions:

Course overviews:

1st Lecture

by Terje G. Finstad

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228-56109

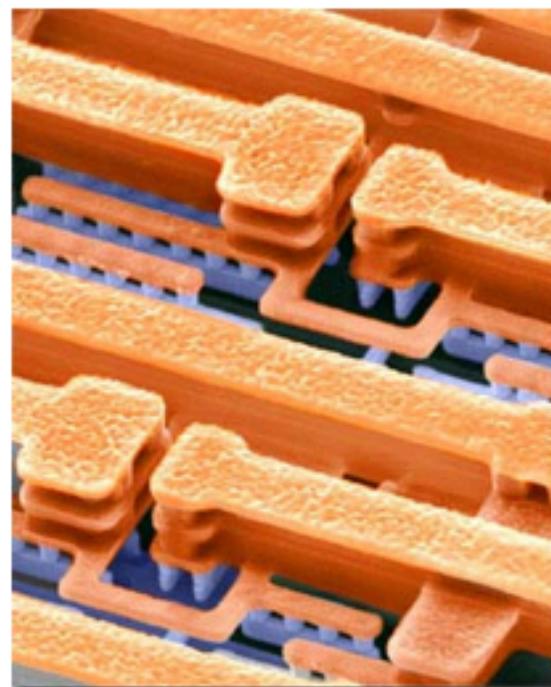
terje.finstad AT fys.uio.no

Office 3<sup>rd</sup> floor, LENS in IFI1

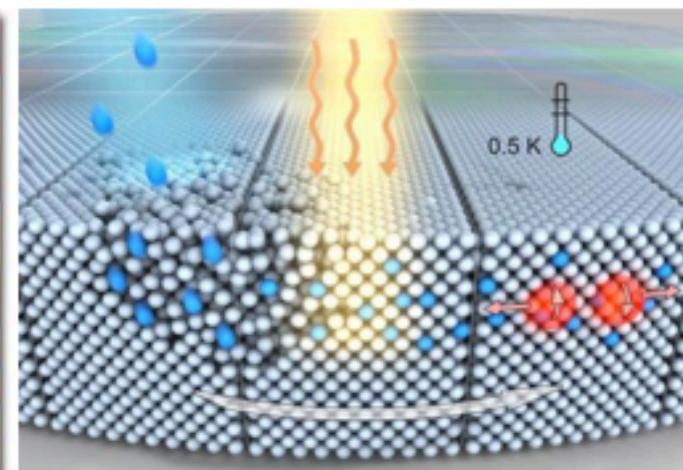
# FYS 4310/9310 Materials Science of Semiconductors

[Course Home Page](#) | [Message Board](#) | [Plan by Week](#) |

<a href="#"><u>Course description</u></a>
<a href="#"><u>Teachers</u></a>
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<a href="#"><u>Text Books</u></a>
<a href="#"><u>Curriculum</u></a>



SEM view of Copper Interconnect  
(IBM Microelectronics)



FYS 4310



Textbook



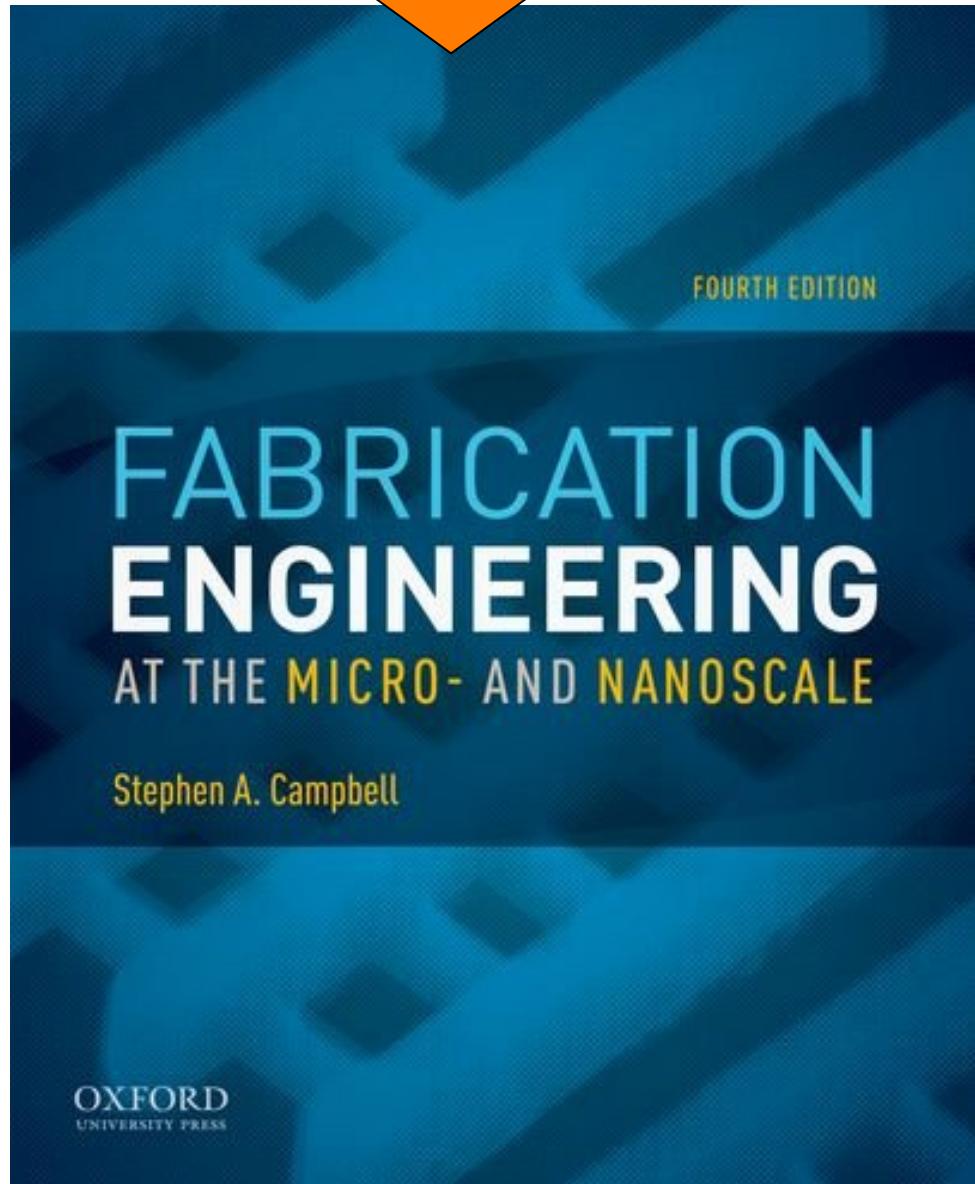
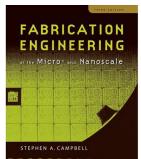
## Other books

Electronic Materials Science:  
for Integrated Circuits in Si and GaAs,  
J. W. Mayer and S. S. Lau,  
Macmillan, ISBN 0-02-378140-8

VLSI Technology, 2nd Edition,  
S.M. Sze,  
McGraw Hill, ISBN 0-07-100347-9

Physics of Semiconductor Devices, 2nd Edition,  
S.M. Sze,  
Wiley, ISBN 0-471-09837-X

see course www pages for more



**FYS 4310**



Textbook

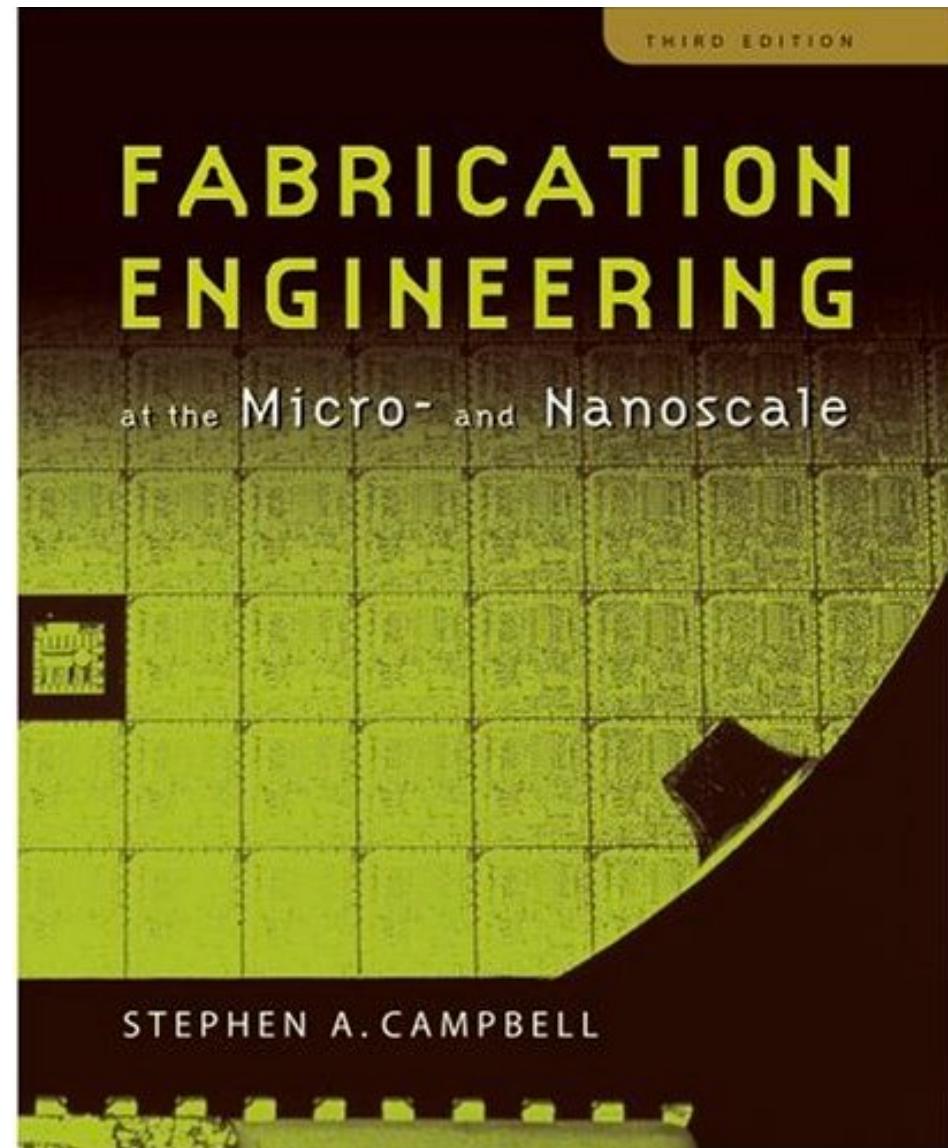
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**FYS 4310**



**2009 Textbook**

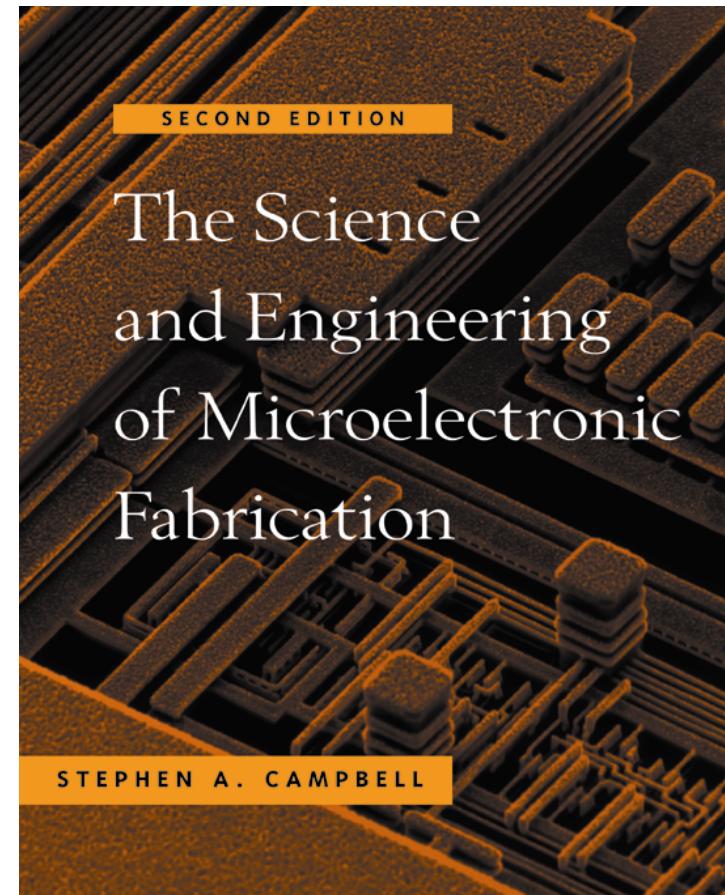
This book title describes  
the course better

**note**

Microelectronic  
= microscopic electronics

**Includes**

Nanoelectronic  
= electronics with nm  
feature size



**FYS 4310**



Overview I

What you learn

**FYS 4310/9310**

**Materials Science of Semiconductors**

**and Semiconductor Devices**

Present, past, future..

LSI, VLSI, ULSI, GLSI, RLSI..

MEMS, single, IR detector, Solar cell, Laser ...

Who take the course

YOU      WHO ?

- you all

MSc/PhD Physical Electronics  
Microelectronics  
Chemistry  
Mat.Sci  
Physics

Motivation profile

Overview -what to do with a 1/2 con to measure x

Circuit design

Are you not on the list?

FYS 4310



What we learn

Help and overview to work in the lab

Support for publication reading

Higher education - Growing up

Microelectronics fantastic and fascinating development

History - not for history's own sake

Research - decades behind and in front of development

Industry

Reflection on interplay; locomotives in technology society

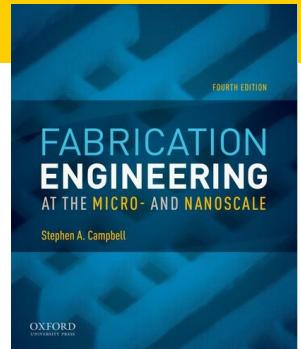
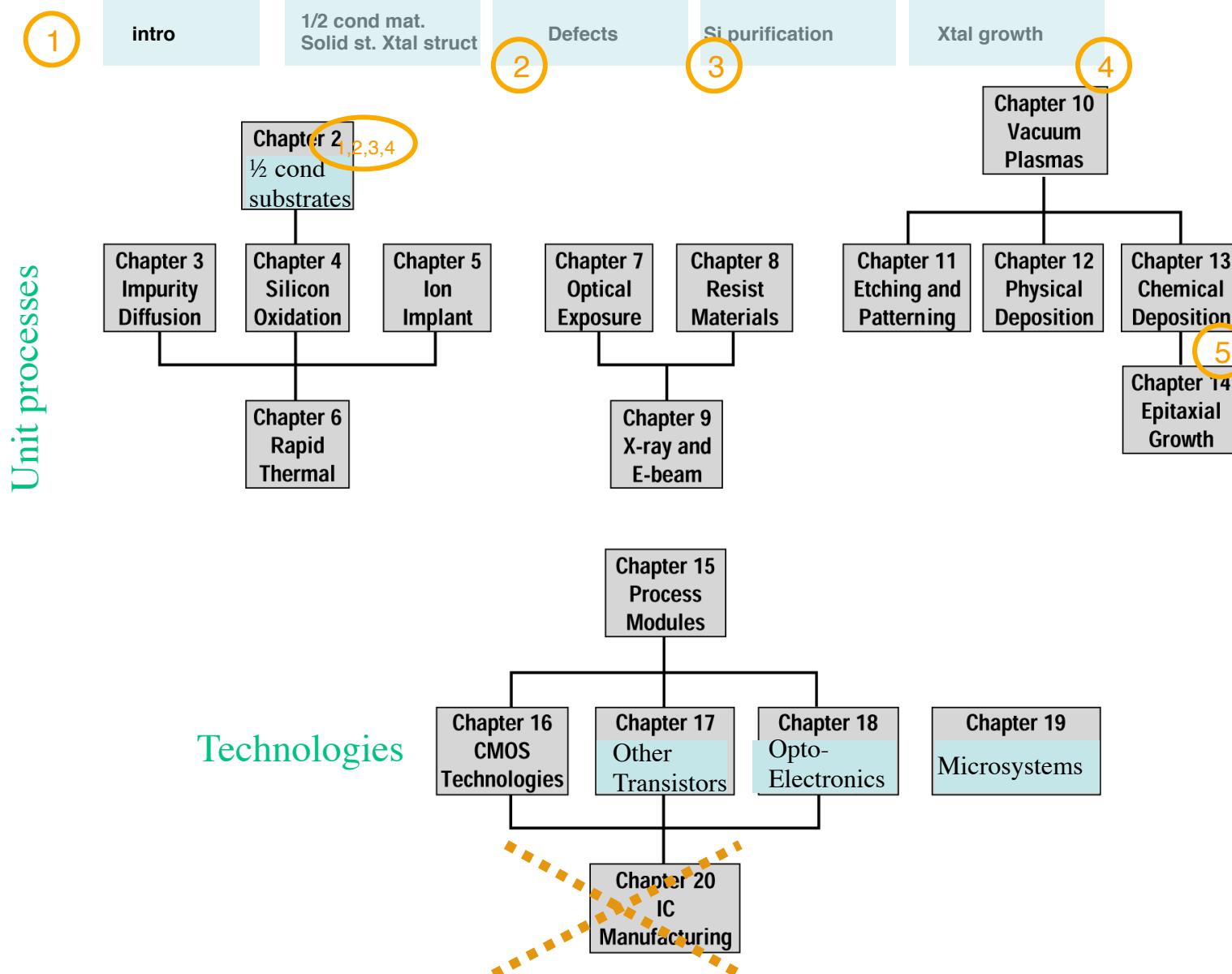


Figure 1.7 A roadmap for the course indicating the relationships between the chapters.

# FYS 4310

# Tentative Weekly-plan

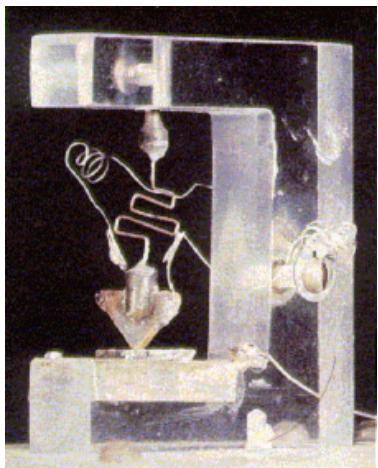
NB always Tentative/ preliminary

See [Message board](#) for more "updated" info and rush announcements

Week	Dates	"Problem solving exercises"	Lecture
1	tbd	Get text-book and curriculum	NO LECTURE
2	01.11	No problems	Overview; Unity-processes, Device technologies,Solid state physics, Xtals, Xtal defects, Charged vacancy model Si, Si purification, Xtal growth, Segregation,Oxygen in Si, Denuded zone, Gettering,
3	01.18	Problem 200.1 .. 200.7	Xtal growth, Oxygen in Si, Denuded zone, Gettering, Unit process Epitaxi, CVD, MBE,
4	01.25	Problems 200-9, -13, -18, -19,	Unit process Epitaxi, MBE, SPE, Case GaAs on Si, SiGe,
5	02.01	1400-1 , -2, -4,10,-9 (-,6) <b>Oblig1[ 200-8-10, -20, 1400-3, -5 [200-11, 200-12]</b>	Unit process Oxidation
6	02.08	Oblig 1 discuss	Unit process Diffusion
7	02.15	<b>do Summary_test 1, at 'home'</b>	Unit process Diffusion
8	02.22	Problems , 300-2, -6 Discuss Quiz_1,	Unit process Ion implantation,
9	02.29	Problem 300-6, 7,-8, -9; 400-6,-7,-8 4.13,	Unit process Ion implantation, RTP
10	03.07	<b>Oblig 2[300-3, -10, 400-3. 500-2, 500-3 [300-1,300-5]</b>	Unit process Dry etch, Sputtering, Pattern transfer,
11	03.14	Oblig 2 discuss,	Technical education, Vacuum, Plasma, Thin Film deposition
12	03.21	 EASTER	 EASTER
13	03.28	 EASTER	 EASTER
14	04.04	500-6, -7, 600-1 ,-3	Unit Metallization, Thin Film interdiffusion,
14	04.11	<b>do Summary_test2, at 'home'</b>	poly Si, Unit process pattern transfer, lithography
16	04.18	discuss test 2	Process Integration, Isolation
17	04.25		Process Integration, Bipolars,
18	05.02	<b>do oblig3: [ 800-1, 900-1, 900-2, 1500-1,1500-4, 1500-5 ] [15000-2, 1500-3 ]</b>	Process Integration MOS, CMOS
19	05.09	discuss oblig 3	MEMS Process Integration
20	05.16	<b>Holiday</b> (Pentecost monday) <b>do repetitions 1500-6..8, 300-4, 400-1,-2, -10, at home in that week</b>	<b>Holiday</b> (Pentecost monday) no lecture
21	05.23	 Project presentations - 20 min pr person .	Time , schedule and location TBA
22	<b>30 may</b>		<b>Oral Exam 30 may (TENTATIVE)</b>
23	6th Jun	Reading for fun and pleasure with no pressure!	TBA

See the web page

# First Transistor



1947

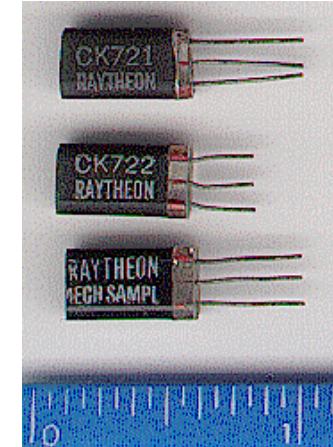
1st transistor  
AT&T Bell Lab



3 inventors (John Bardeen,  
Walter Brattain, and  
William Shockley) share  
Nobel prize

1st commercially  
successful TR  
Raytheon CK722,  
1953

Ge-based pnp low  
power TR

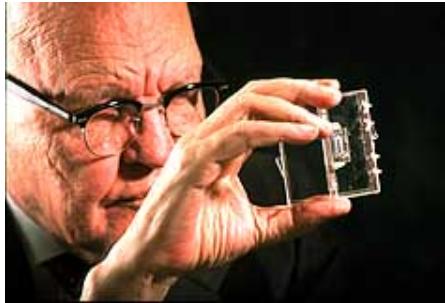


1st Si transistor made  
by Gordon Teal at TI  
in  
1954

Source: <http://www.lucent.com/minds/transistor/>

Sources: <http://roiconnect.com/transistor.htm>  
<http://www.pbs.org/transistor/science/events/silicont1.html>

# First Integrated Circuit

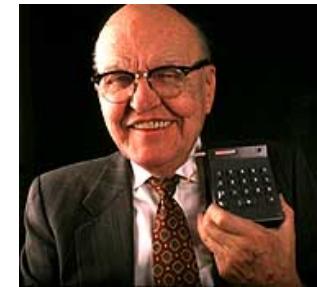


1958, Jack Kilby,  
Texas Instrument



## Integrated Circuit (IC):

a large number of individual components (transistors, resistors, capacitors, etc.) fabricated side by side on a common substrate and wired together to perform a particular circuit function.



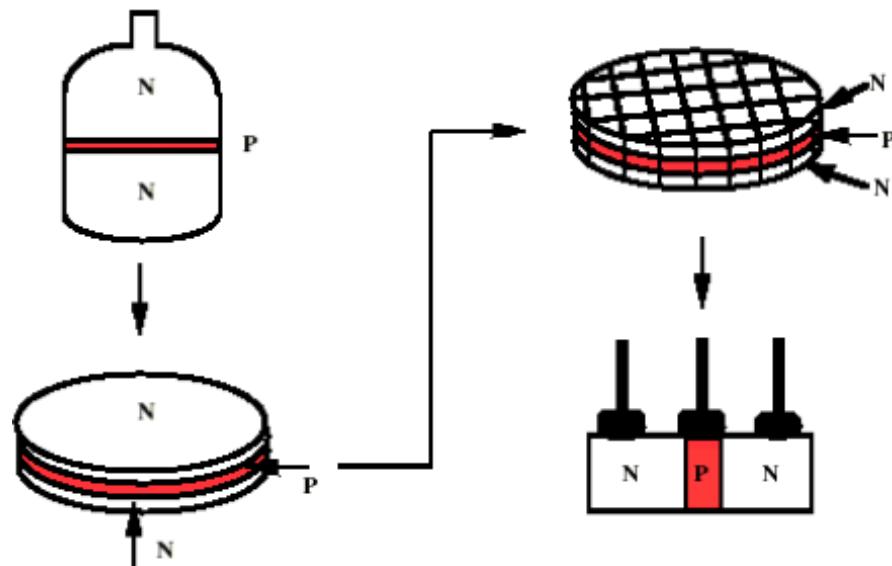
In 1962, Steven Hofstein and Fredric Heiman at the RCA research laboratory in Princeton, New Jersey, invented a new family of devices called metal-oxide semiconductor *field-effect transistors* (MOS FETs for short). Although these transistors were somewhat slower than bipolar transistors, they were cheaper, smaller and used less power. Also of interest was the fact that modified metal-oxide semiconductor structures could be made to act as capacitors or resistors.

## Sources:

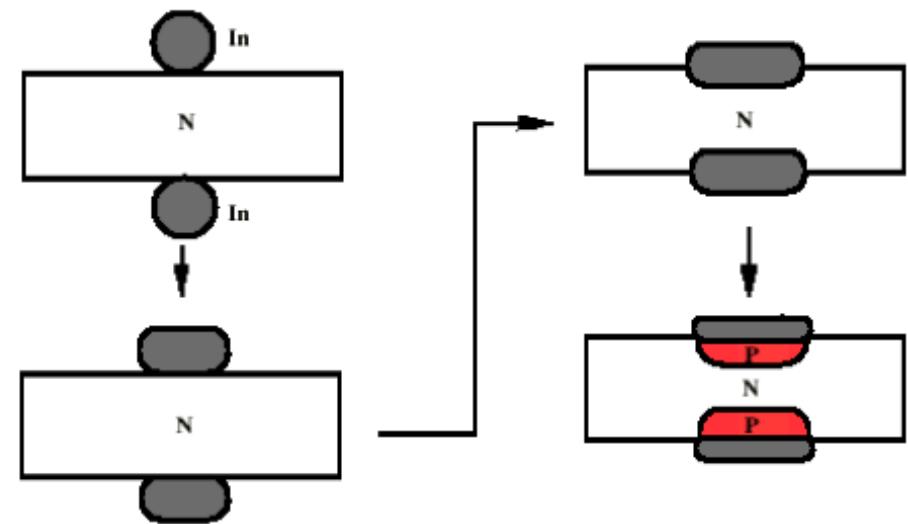
- <http://www.ti.com/corp/docs/kilbyctr/jackbuilt.shtml>
- <http://www.maxmon.com/1926ad.htm>

# Old school-device

Early Discrete Bipolar Transistor Technology



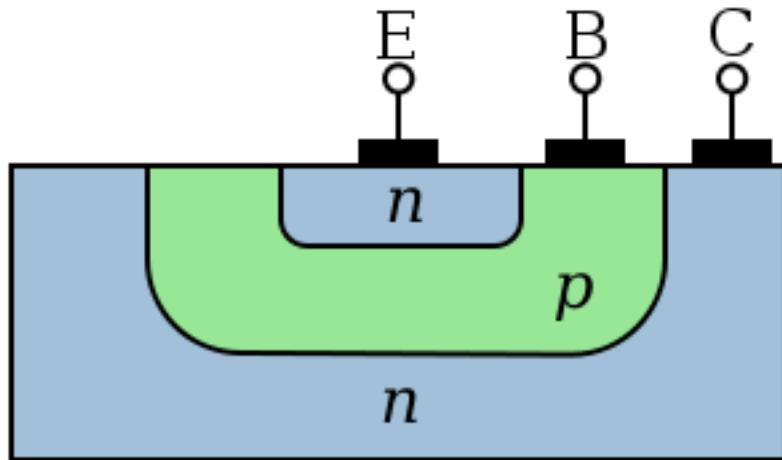
Grown junction transistor technology  
of the 1950s.



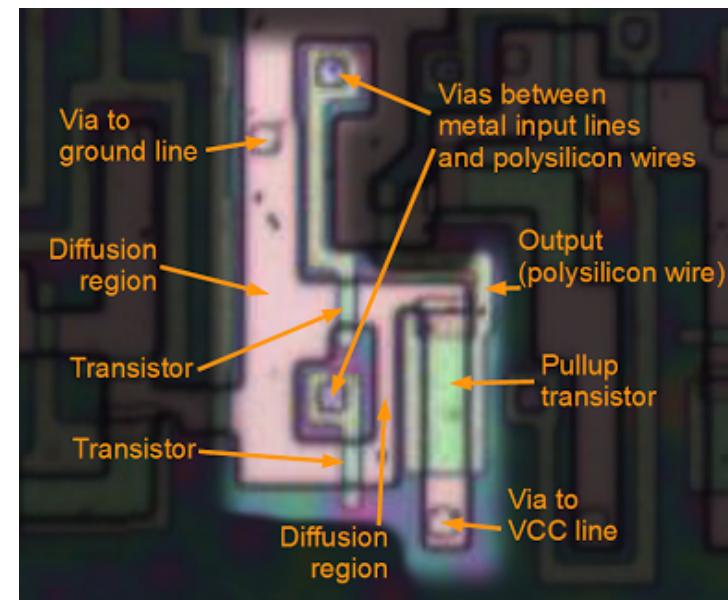
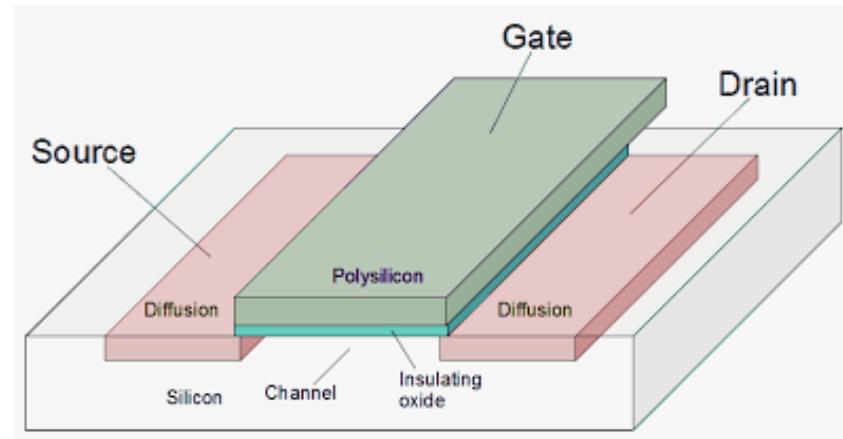
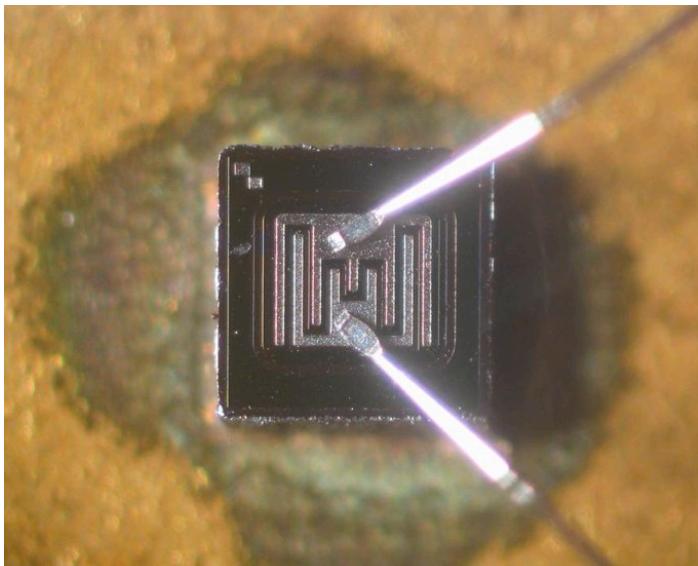
Alloy junction technology of the 1950s.

- Ge was the dominant technology
- devices were useful but junctions were exposed and there was no way to interconnect multiple devices

# planar-device



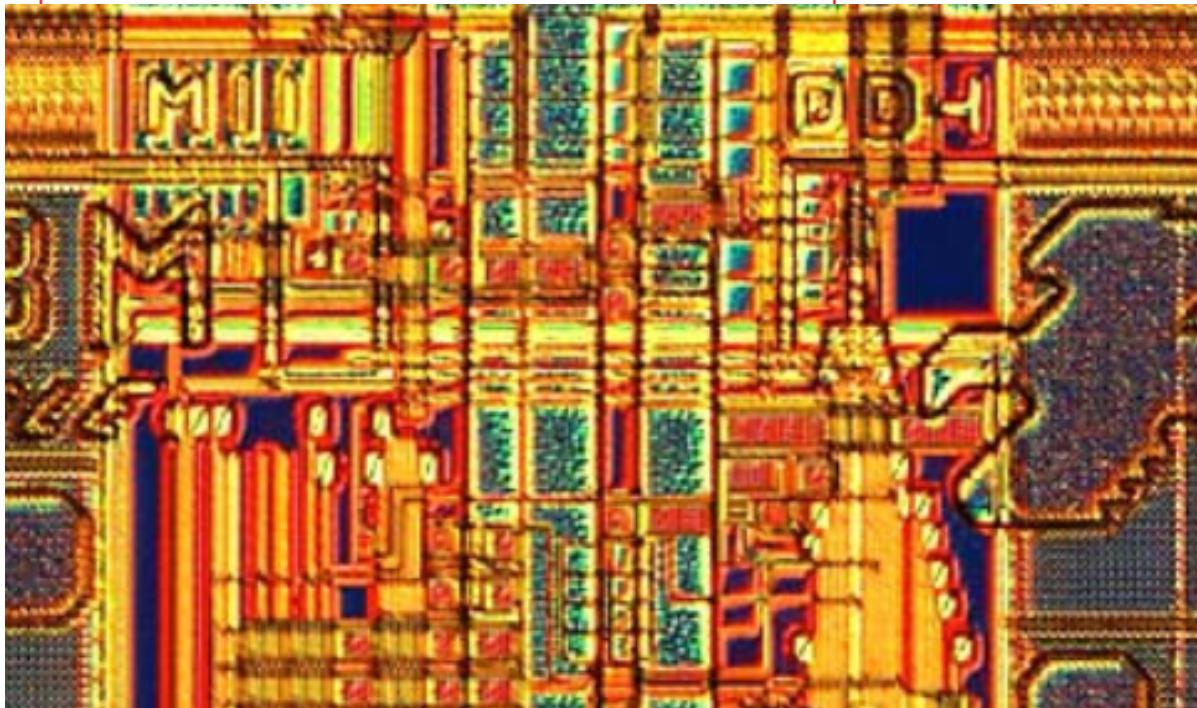
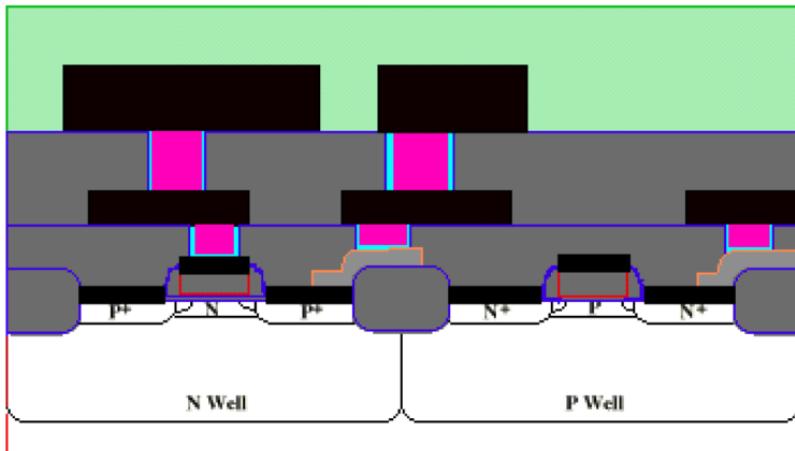
Single bipolar npn transistor



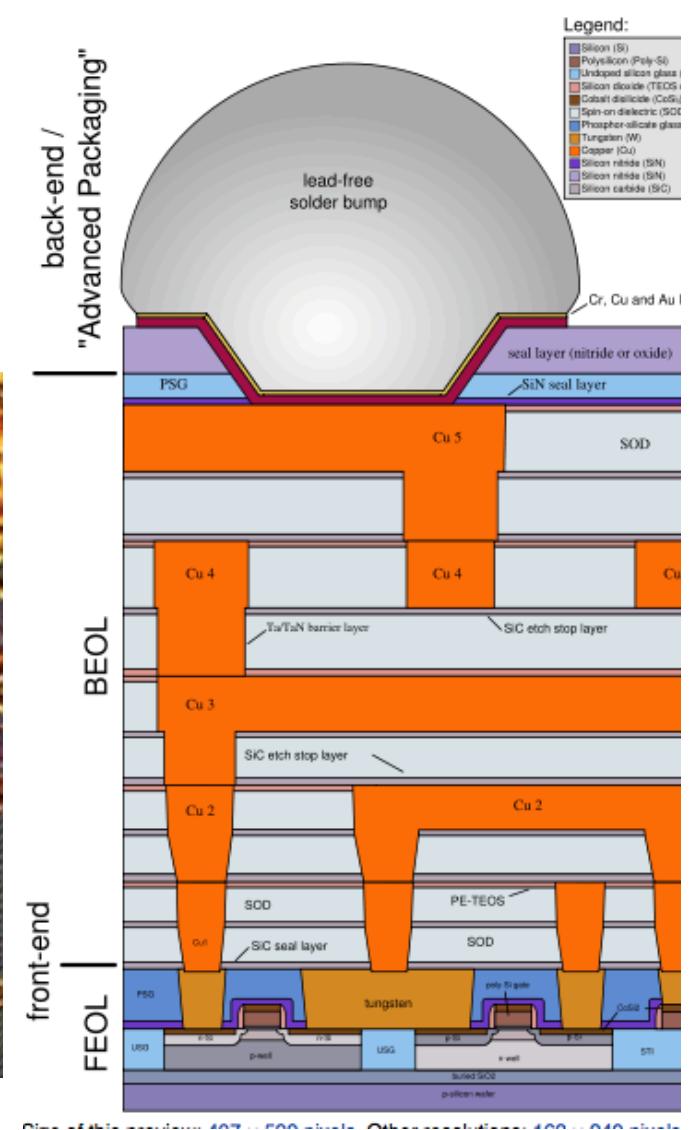
Nor –gate plan view

# Planar MOS devices

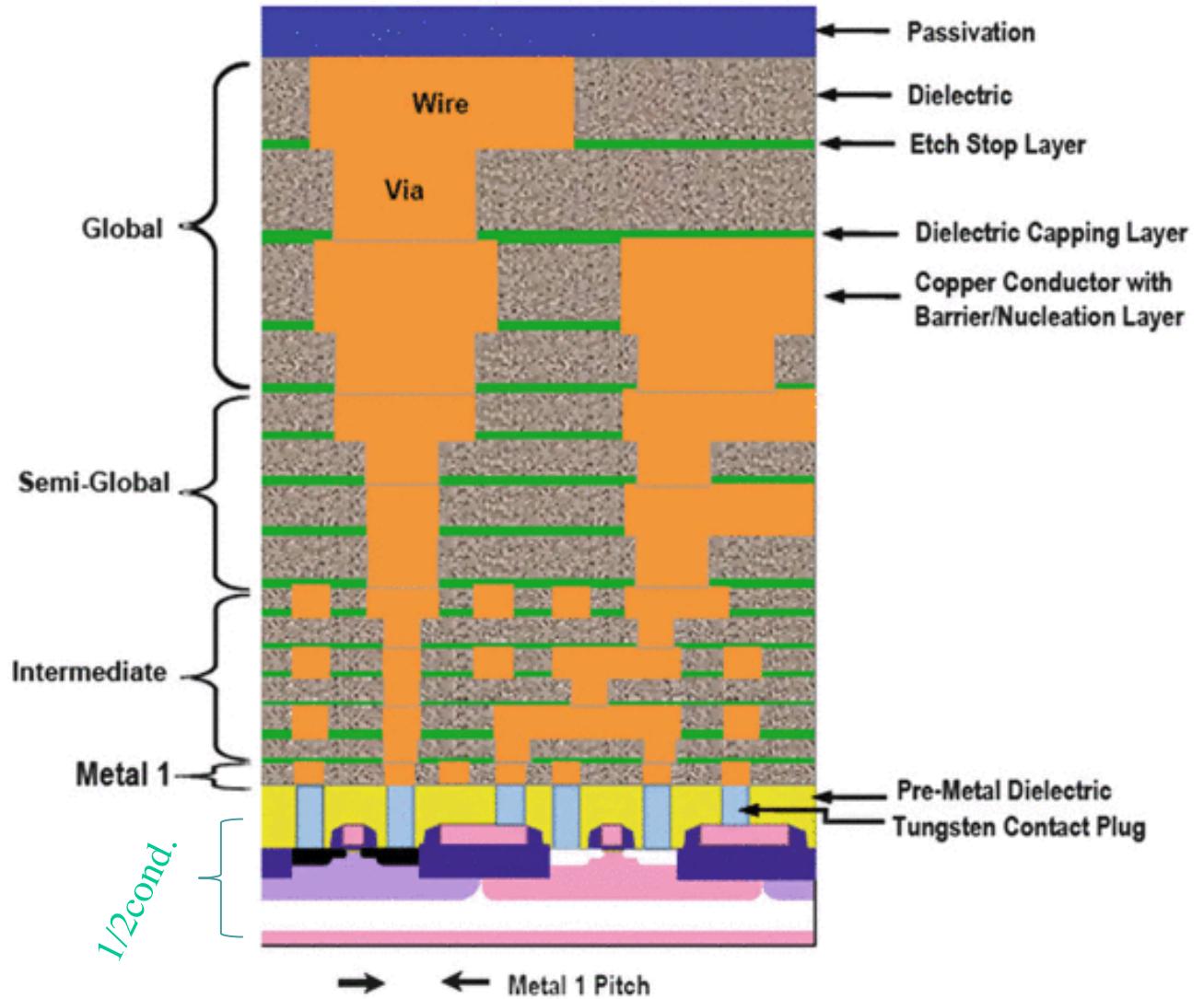
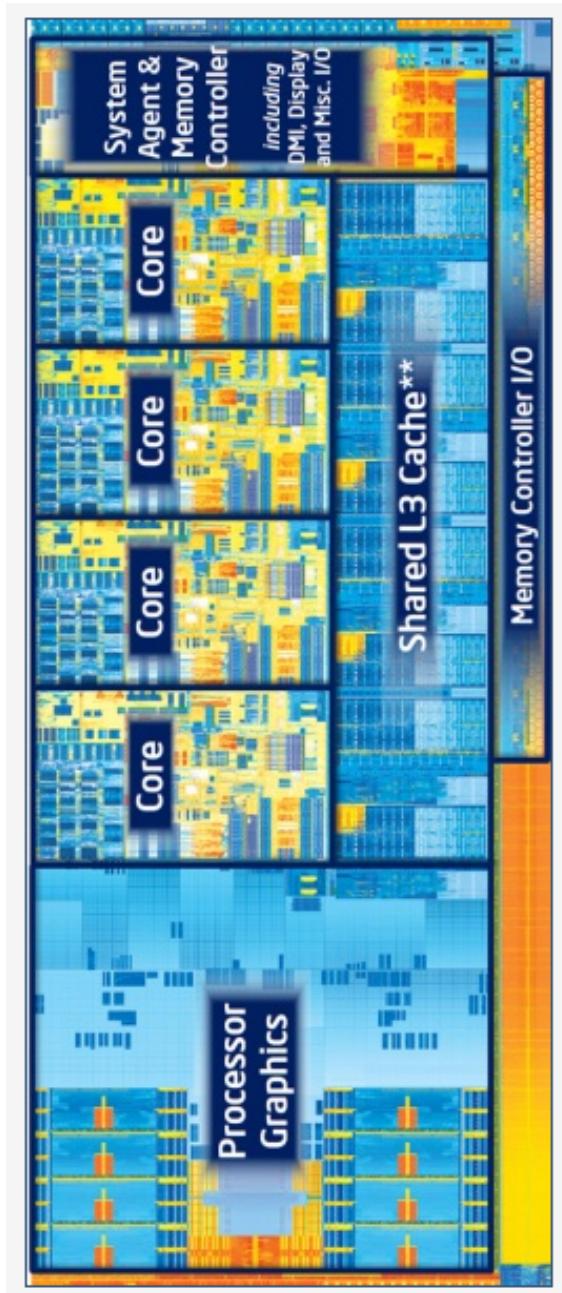
Schematic Cross Section of a Modern Silicon IC



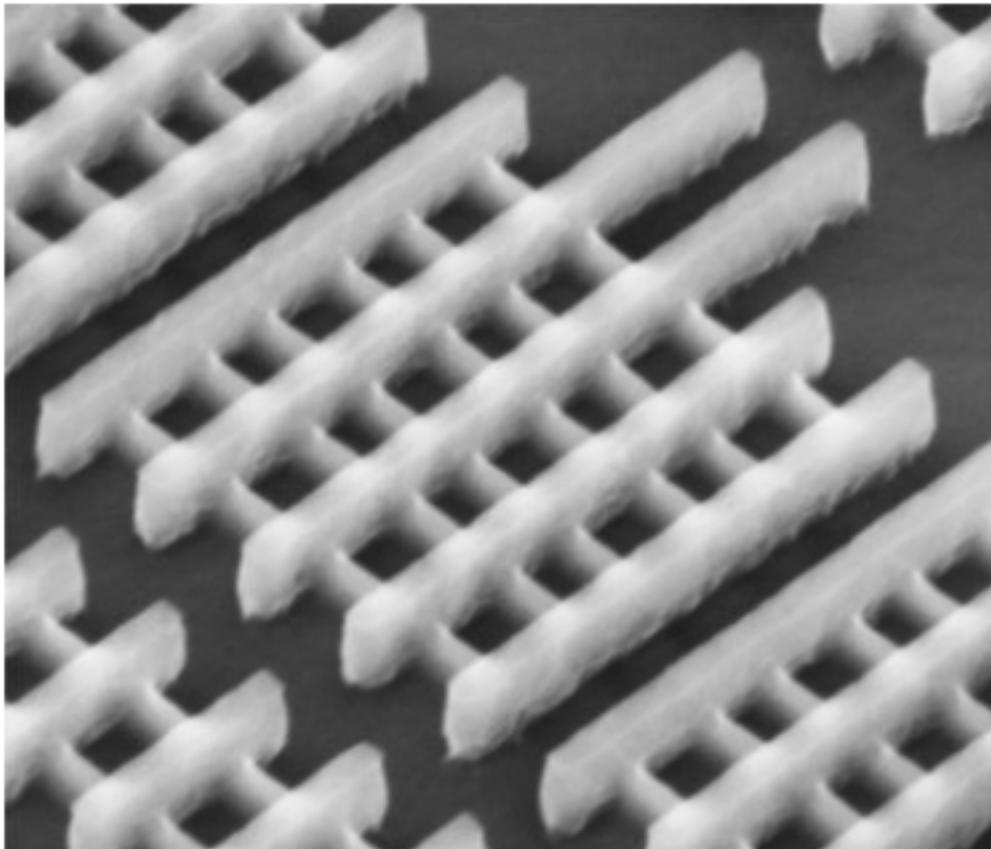
*Historic The Eagle Memory chip from IBM*



# “modern”-device

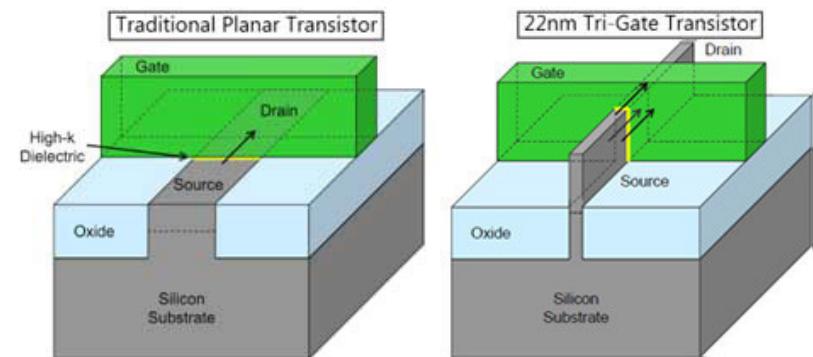


# “next generation”-device



Intel photo

A microscope image shows vertical "fins" on Intel's new Tri-Gate transistor in Intel's new Ivy Bridge microprocessor.

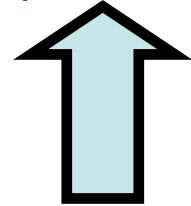


fins 20-30 atoms across – a fabrication challenge be careful not to touch!

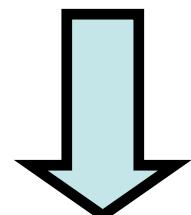
# Moore's law

- Gordon Moore: a co-founder of Intel

“Component counts per unit area doubles every two years.”

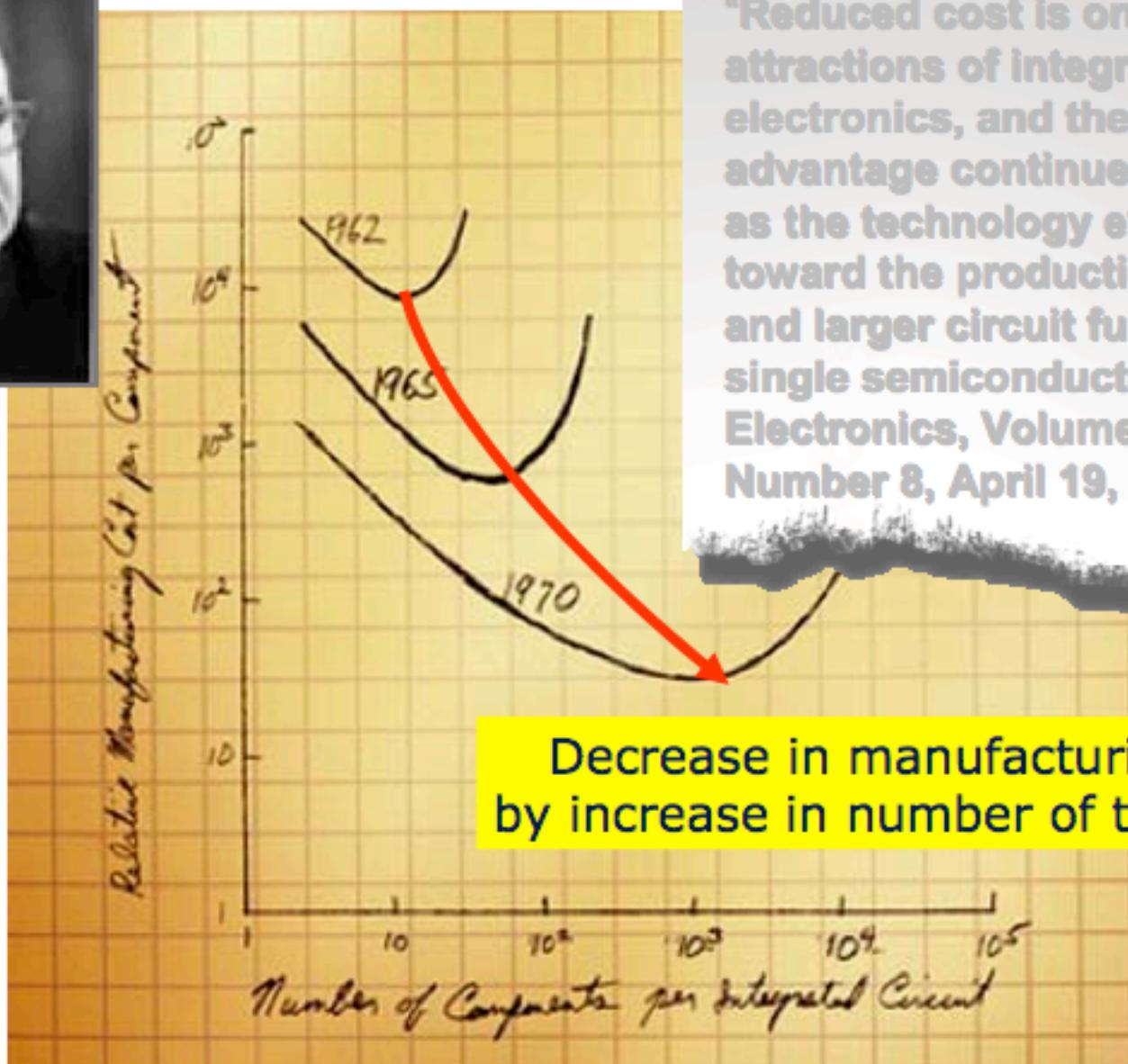


- Feature size reduction enables the increase of complexity.



	# of devices
SSI (Small scale IC)	1 ~ 100
MSI (Medium scale IC)	$10^2 \sim 10^3$
LSI (Large scale IC)	$10^3 \sim 10^5$
VLSI (Very Large scale IC)	$10^5 \sim 10^6$
ULSI (Ultra Large scale IC)	$10^6 \sim 10^9$
GSI (Giga scale integration)	$10^9 \sim$
RLSI (Ridiculously Large scale IC) ?	Next to GSI

# Gordon Moore, 1965



"Reduced cost is one of the big attractions of integrated electronics, and the cost advantage continues to increase as the technology evolves toward the production of larger and larger circuit functions on a single semiconductor substrate."

Electronics, Volume 38, Number 8, April 19, 1965

Decrease in manufacturing cost by increase in number of transistors

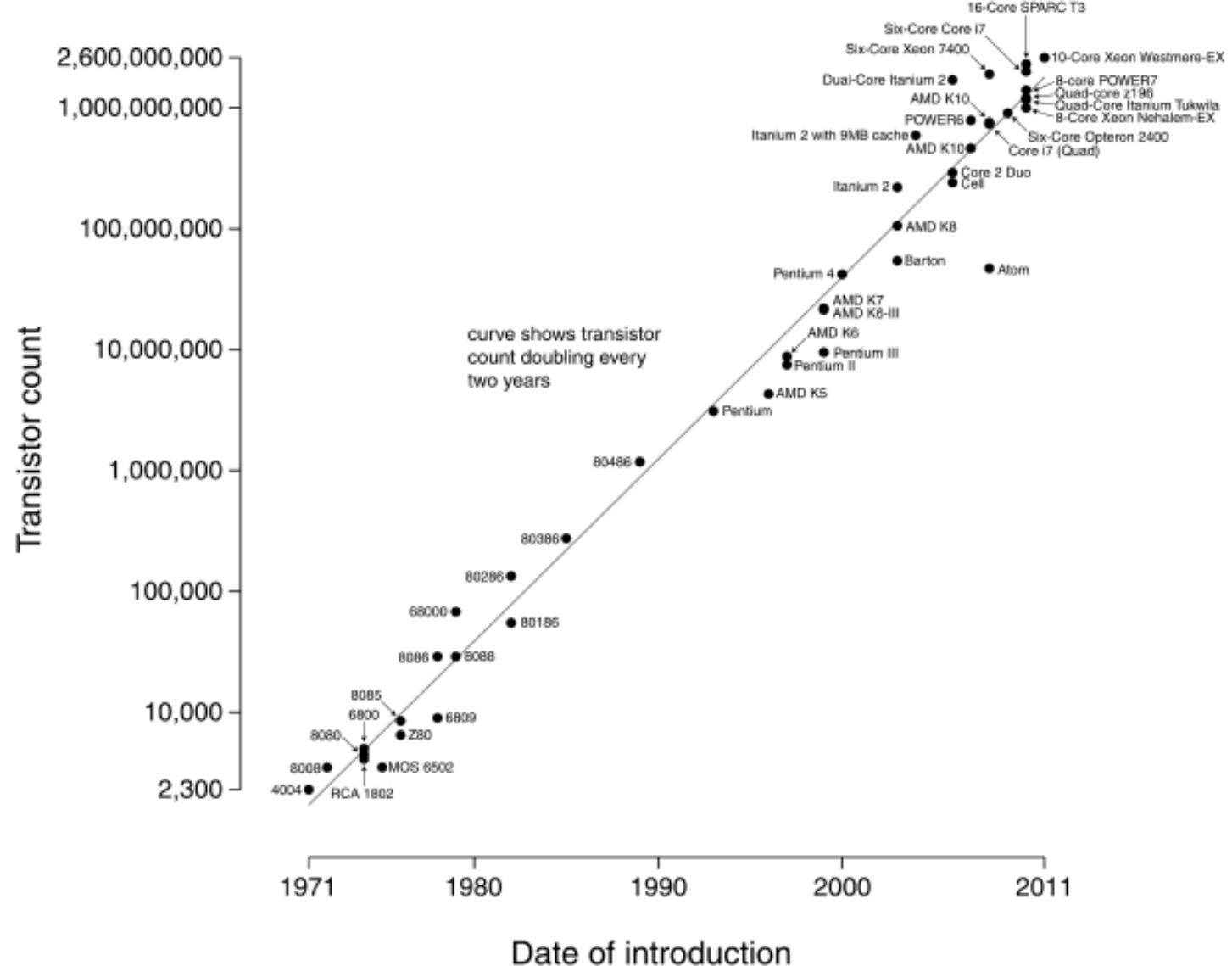
# History of IC: Increase of complexity

Microprocessor Transistor Counts 1971-2011 & Moore's Law

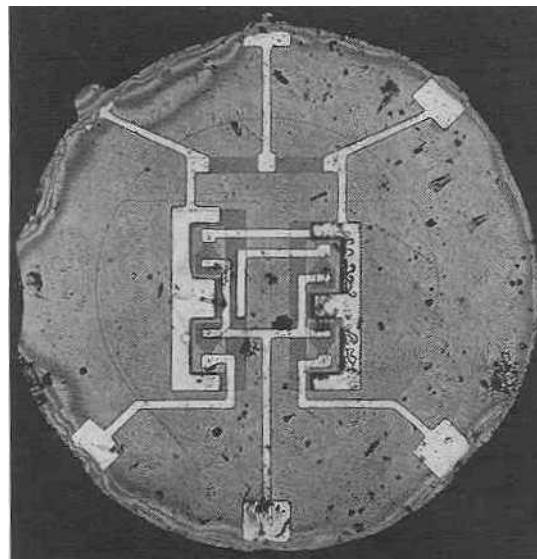
130 nm->99 nm-65 nm  
->45 nm -> 32 nm->22nm

A "Normal" PC  
Intel Core i7 2011  
Intel Sandy Bridge,  
32nm technology  
>>500Mill transistors

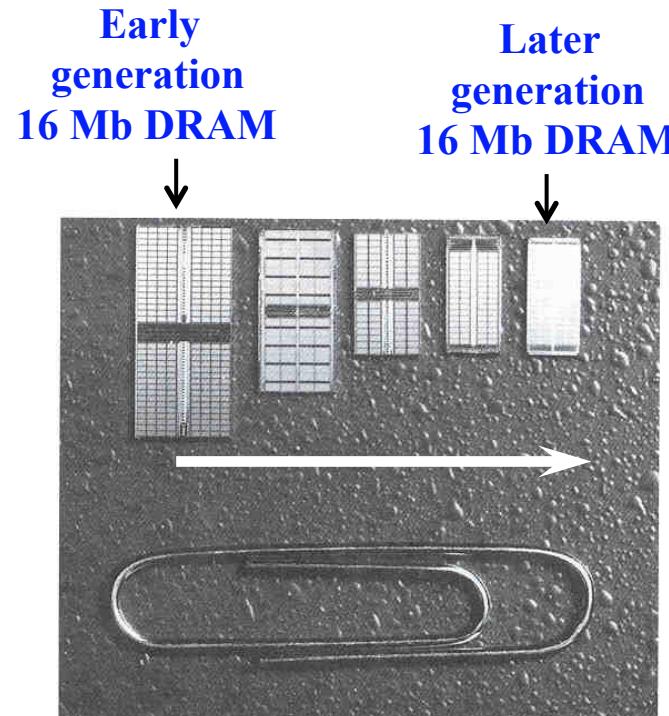
Intel Skylake, 2015  
14 nm technology



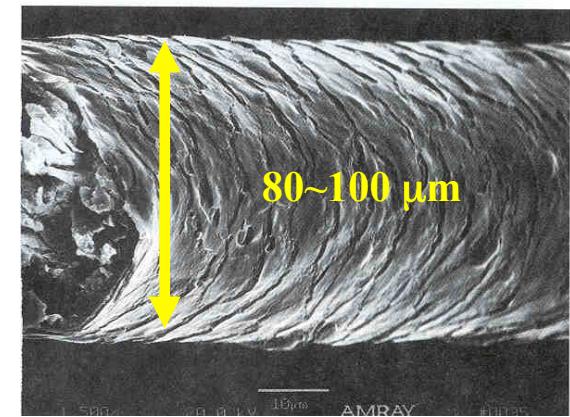
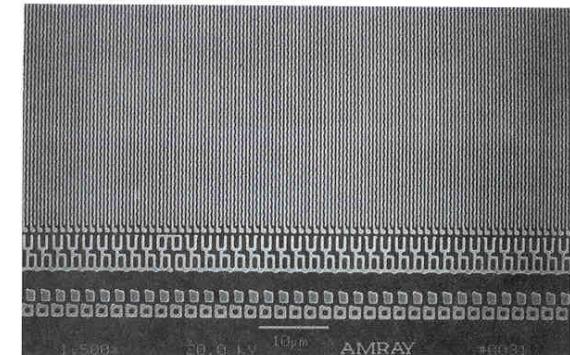
# The smaller feature size the better!



Early 1960s IC  
4 TRs and several resistors

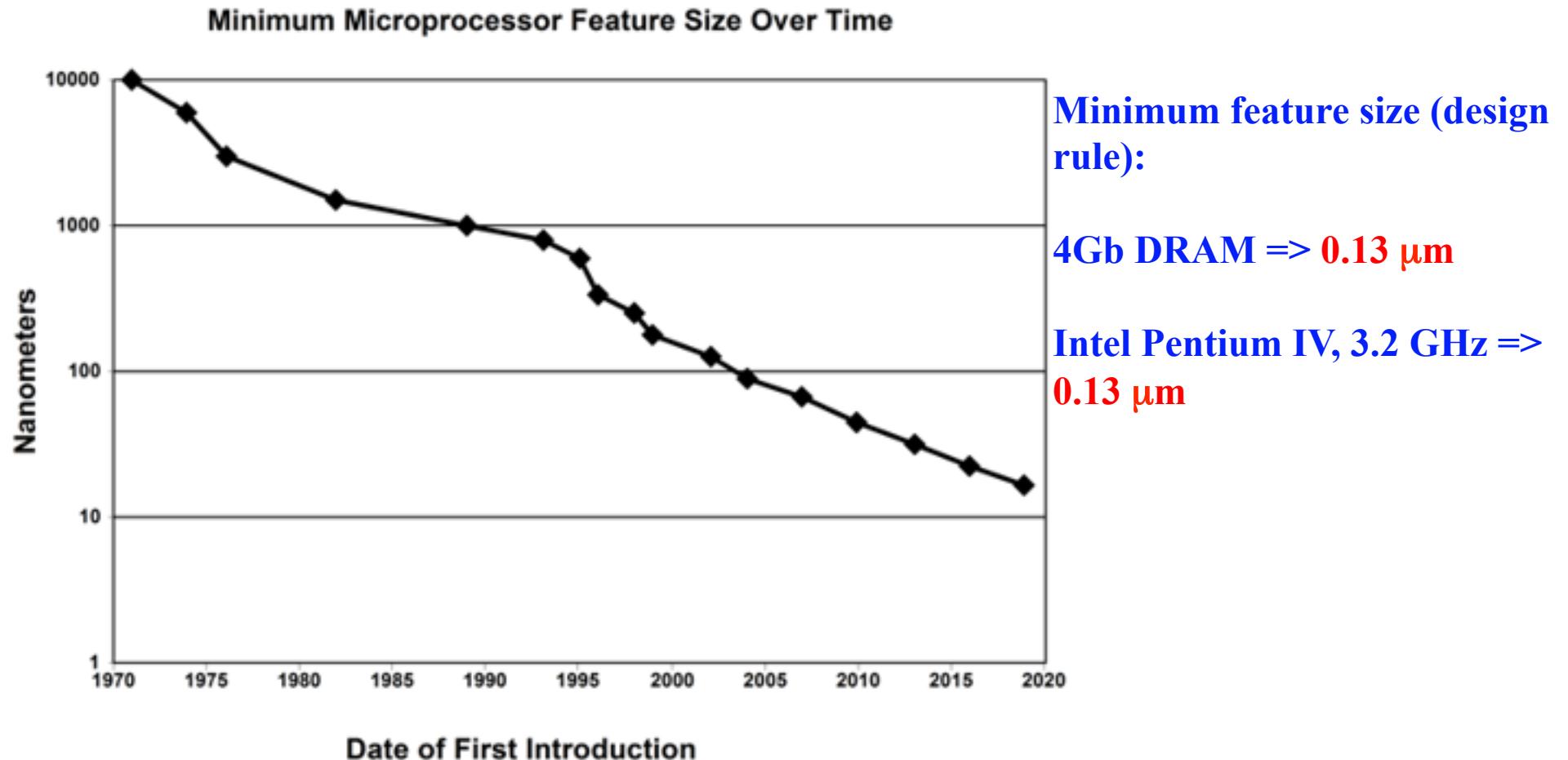


Paper clip and  
16 Mb DRAM

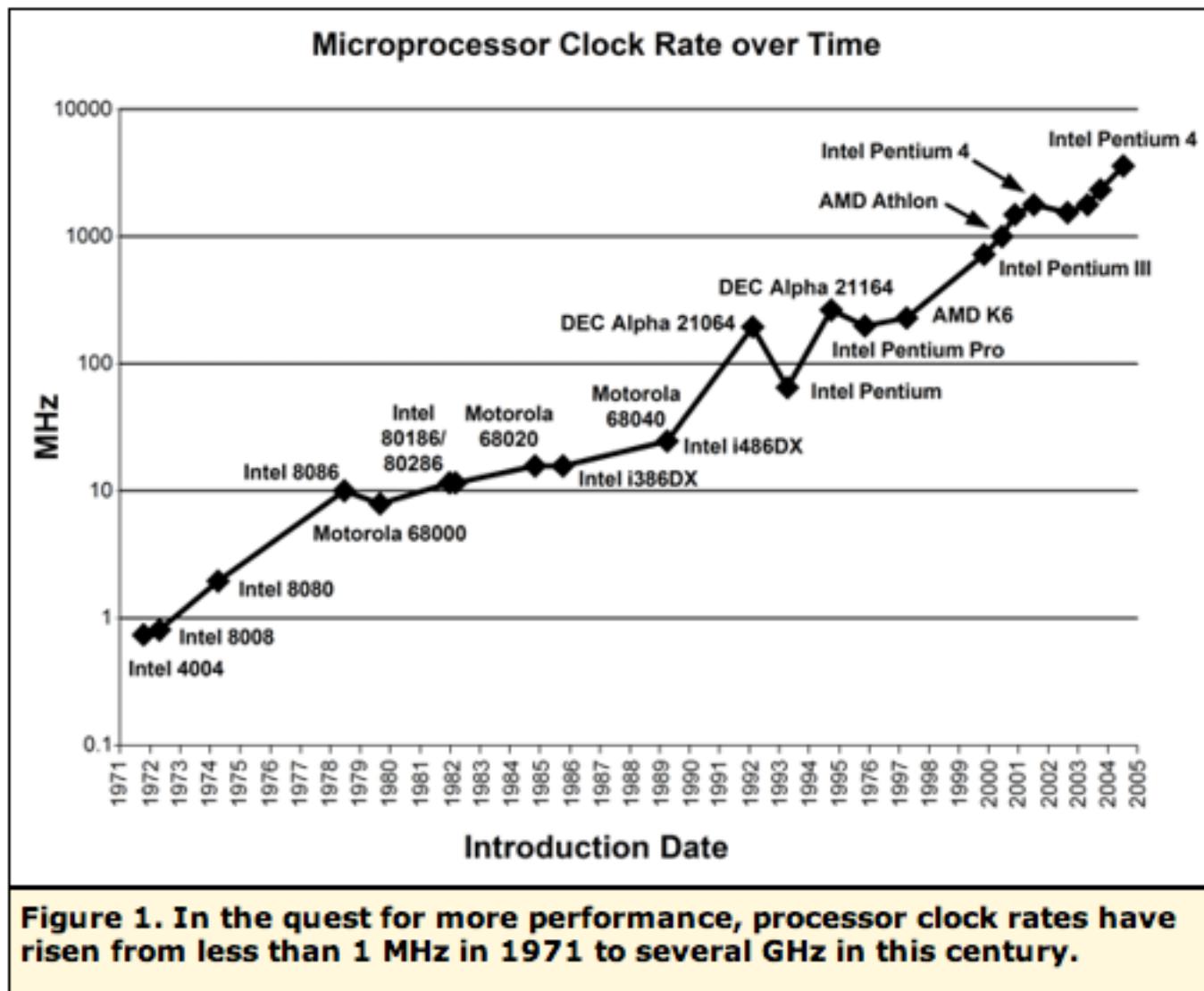


0.18  $\mu\text{m}$  lines  
in 64 Mb DRAM  
and human hair

# History of IC: Decrease of feature size



# History of IC: increase speed

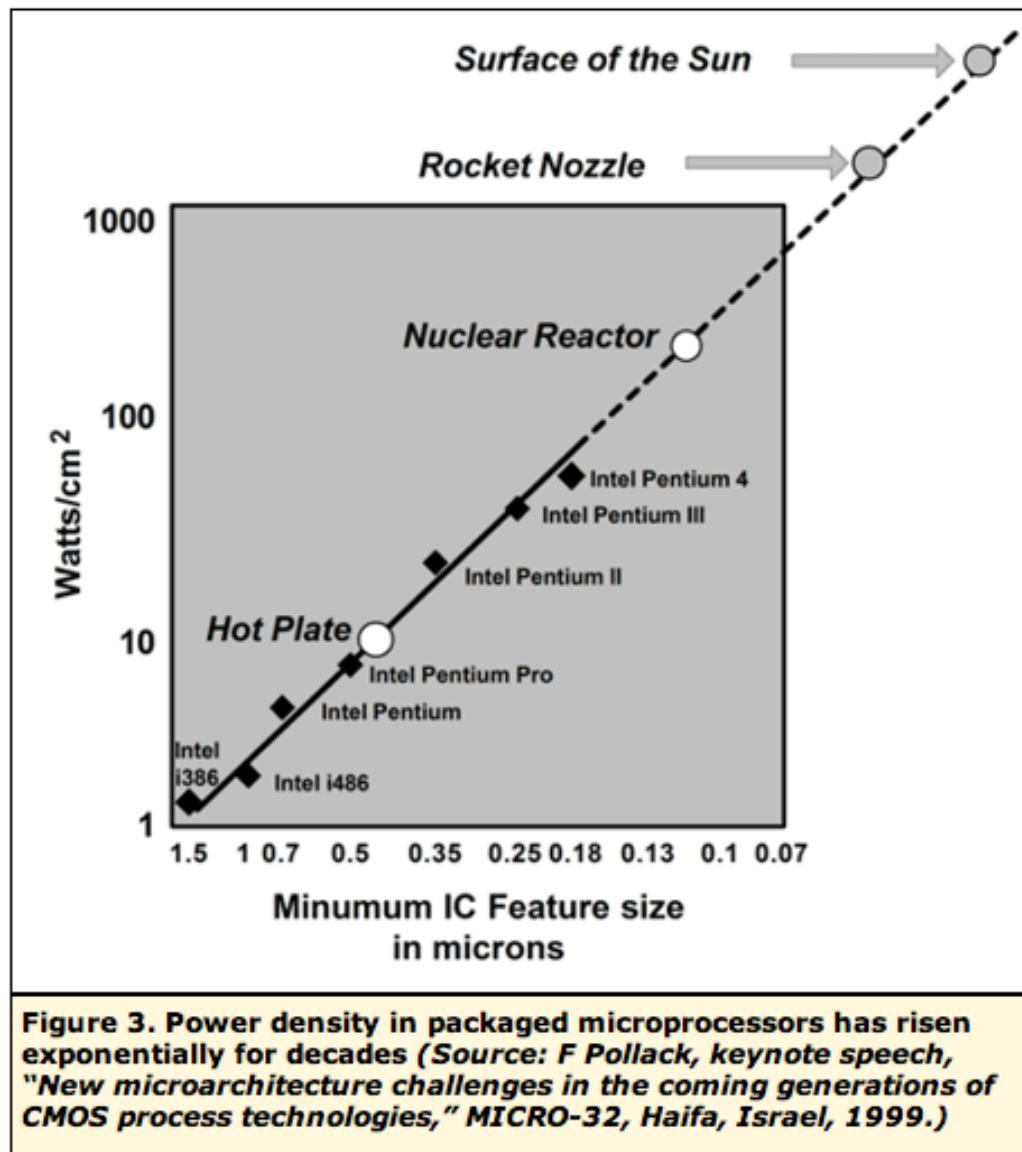


*World's fastest transistor?*  
2009 31.3 Northrop Co 1THz  
InP and InGaAs  
pseudomorph graded base and coll  
basewidth 12.5 nm

*Graphene t transistor?*  
2010 24-12 IBMo 300GHz

Press release World fastes 2011  
26 GHz 550 nm Figure of Merit

# History of IC: increase power



# History of IC: increase power

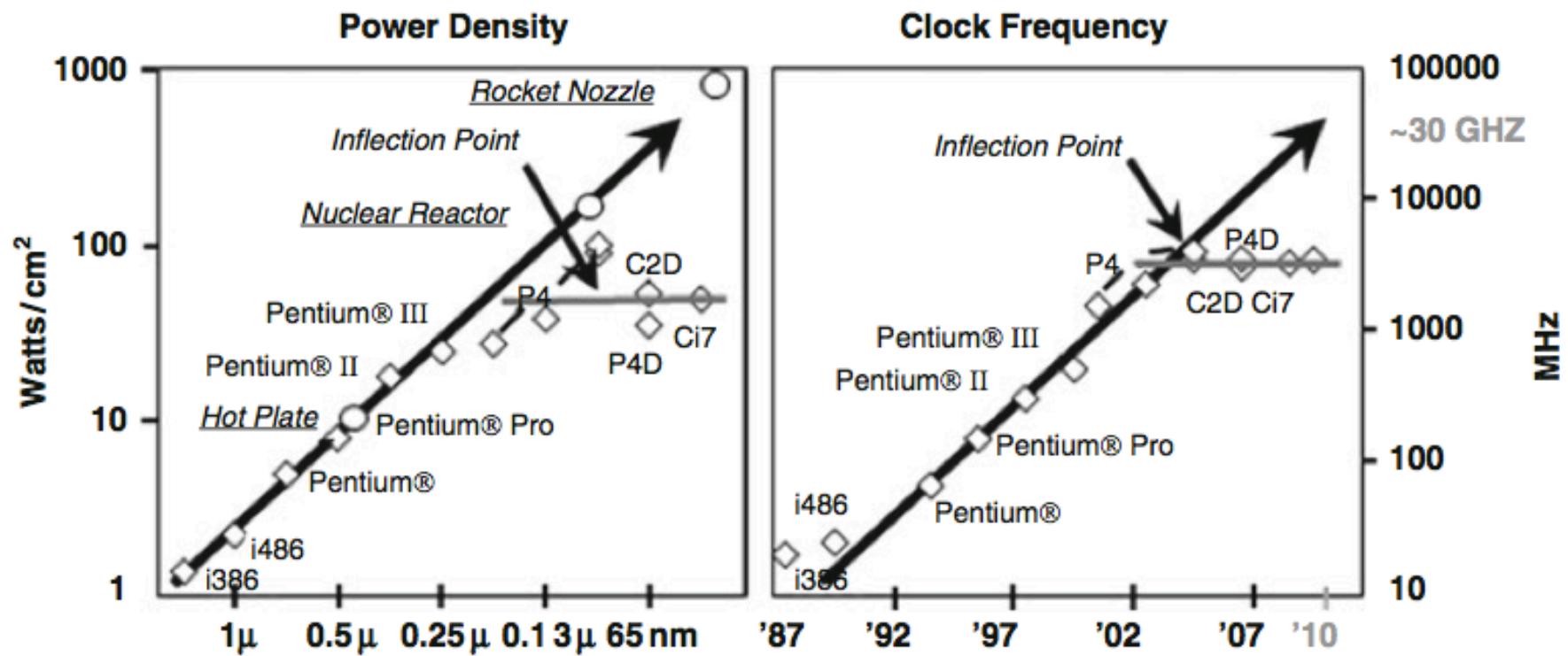
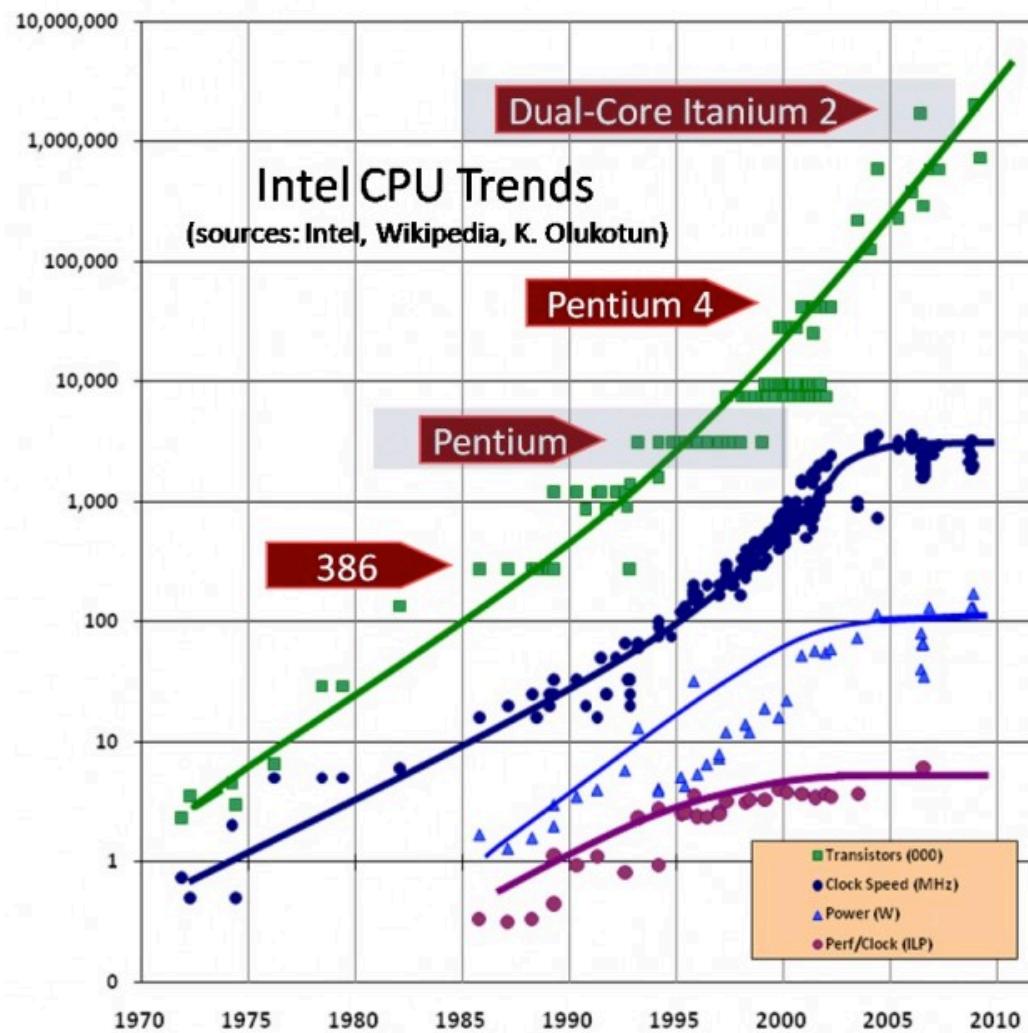


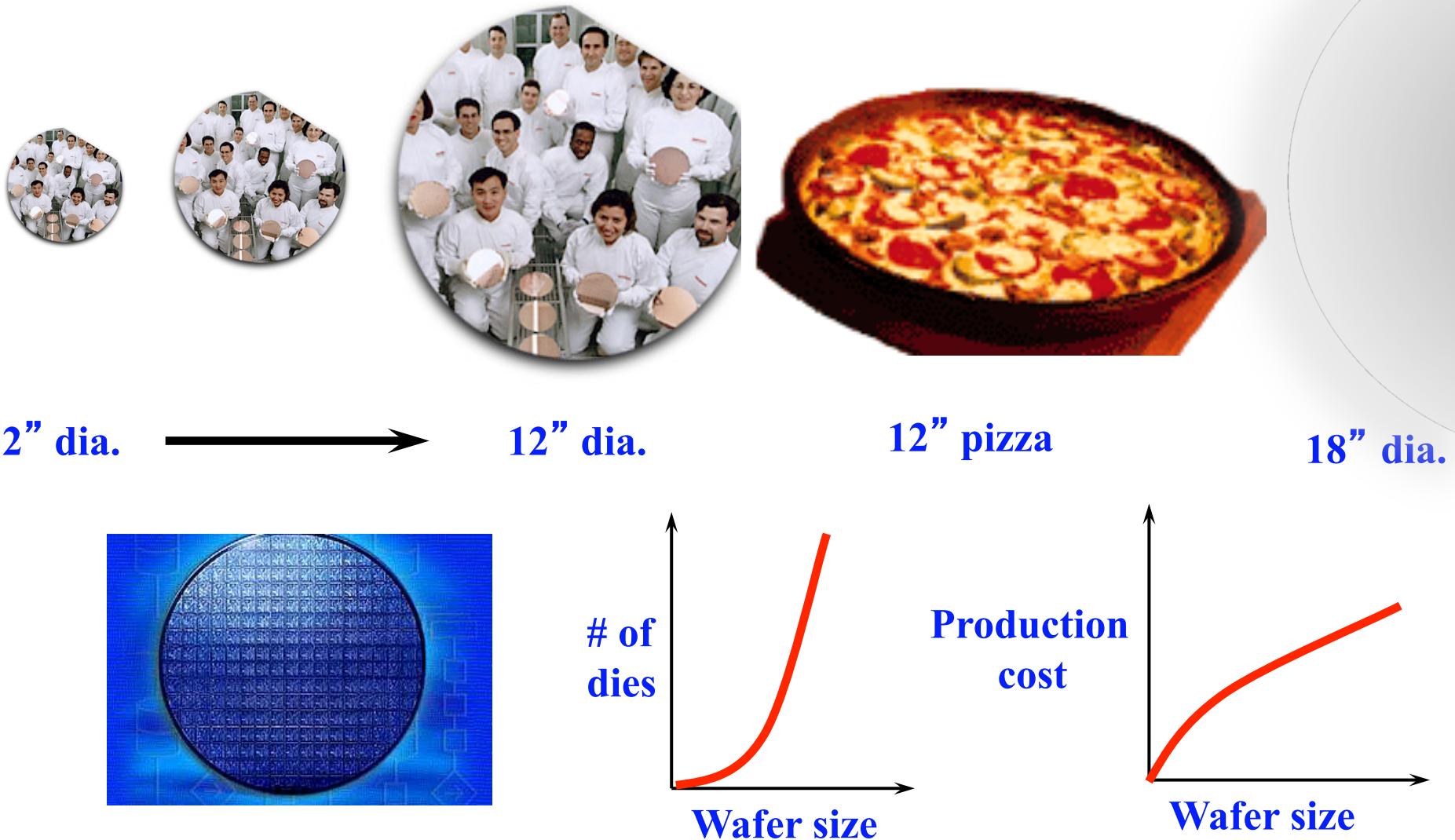
Fig. 9.3 Inflection point for power density and clock frequency

# History of IC: increase power



CPU scaling showing transistor density, power consumption, and efficiency. Chart originally from *The Free Lunch Is Over: A Fundamental Turn Toward Concurrency in Software*

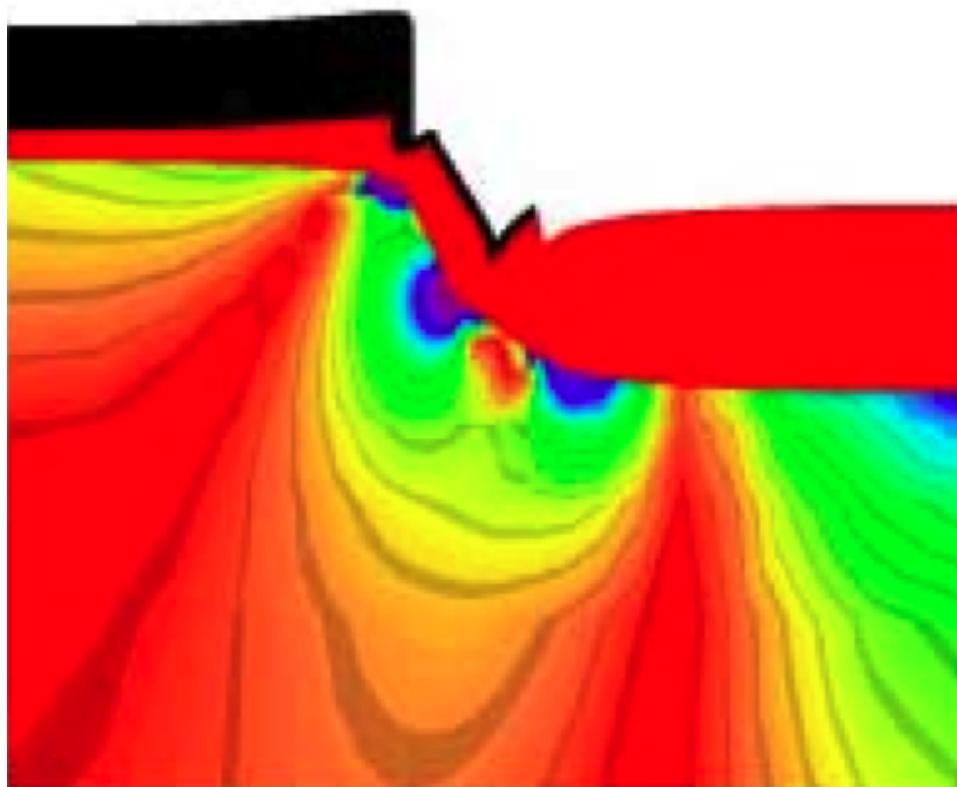
# The larger wafer the better !



# Device development -tools

Technology Computer Aided Design (TCAD)

- most of the basic IC fabrication processes can be simulated (different levels of physical accuracy)
- simulation is used for:
  - designing new processes and devices (link process to device simulation)
  - exploring limits of semiconductor devices and technology (R&D)
  - solving manufacturing problems (what-if?)



# ITRS (International Technology Roadmap for Semiconductors)

	<b>1997</b>	<b>1999</b>	<b>2001</b>	<b>2003</b>	<b>2006</b>	<b>2009</b>	<b>2012</b>	
<b>DRAM (half-pitch)</b>	0.25μ	0.18μ	0.15μ	0.13μ	0.10μ	0.07μ	0.05μ	
<b>MPU (gate length)</b>	0.20μ	0.14μ	0.12μ	0.10μ	0.07μ	0.05μ	0.035μ	
<b>DRAMs Samples</b>	256-Mbit	1-Gbit	-----	4-Gbit	16-Gbit	64-Gbit	256-Gbit	
<b>Logic transistors/cm<sup>2</sup></b>								
MPUs	3.7 M	6.2 M	10 M	18 M	39 M	84 M	180 M	
ASICs	8 M	14 M	16 M	24 M	40 M	64 M	100 M	
<b>Voltage (V)</b>	1.8-2.5	1.5-1.8	1.2-1.5	1.2-1.5	0.9-1.2	0.6-0.9	0.5-0.6	
<b>Wafer size (mm)</b>	200 (8")	300 (12")	300	300	300	450 (18")	450	

Source: [http://public.itrs.net/files/1999\\_SIA\\_Roadmap/Home.htm](http://public.itrs.net/files/1999_SIA_Roadmap/Home.htm)

# 2003 International Technology Roadmap – Bulk Si Requirements

*Table 69a Starting Materials Technology Requirement—Near-term*

Year of Production	2003	2004	2005	2006	2007	2008	2009	Driver
Technology Node		<i>hp90</i>			<i>hp65</i>			
DRAM $\frac{1}{2}$ Pitch (nm)	100	90	80	70	65	57	50	D %
MPU/ASIC Physical Gate Length (nm)	45	38	32	28	25	23	20	M
DRAM Total Chip Area ( $\text{mm}^2$ )	139	110	82	122	97	131	104	D %
DRAM Active Transistor Area ( $\text{mm}^2$ )	36.7	29.1	22.7	35.5	28.2	43.3	34.3	D %
MPU High-Performance Total Chip Area ( $\text{mm}^2$ )	310	310	310	310	310	310	310	M
MPU High-Performance Active Transistor Area ( $\text{mm}^2$ )	32.6	32.1	31.7	31.7	31.7	31.7	31.7	M
<i>General Characteristics * (99% Chip Yield) [A,B,C]</i>								
Wafer diameter (mm) **	300***	300***	300	300	300	300	300	D %, M
Edge exclusion (mm)	2	2	2	2	2	2	2	D %, M
Front surface particle size (nm), latex sphere equivalent [D]	$\geq 90$	D %, M						
Particles ( $\text{cm}^{-2}$ ) [E]	$\leq 0.35$	$\leq 0.35$	$\leq 0.35$	$\leq 0.18$	$\leq 0.18$	$\leq 0.09$	$\leq 0.09$	D %
Particles (#/wf)	$\leq 238$	$\leq 238$	$\leq 241$	$\leq 123$	$\leq 123$	$\leq 63$	$\leq 63$	D %
Site flatness (nm), SFQR 26 mm $\times$ 8 mm site size [F, R]	$\leq 101$	$\leq 90$	$\leq 80$	$\leq 71$	$\leq 64$	$\leq 57$	$\leq 51$	D %, M
Nanotopography, p-v, 2 mm diameter analysis area [Q]	$\leq 25$	$\leq 23$	$\leq 20$	$\leq 18$	$\leq 16$	$\leq 14$	$\leq 13$	M
<i>Polished Wafer * (99% Chip Yield)</i>								
<i>The LLS requirement is specified for particles only; discrimination between particles and COPs is required (see General Characteristics) [D,E]</i>								
Oxidation stacking faults (OSF) (DRAM) ( $\text{cm}^{-2}$ ) [G]	$\leq 1.9$	$\leq 1.6$	$\leq 1.4$	$\leq 1.2$	$\leq 1.0$	$\leq 0.8$	$\leq 0.7$	D %
Oxidation stacking faults (OSF) (MPU) ( $\text{cm}^{-2}$ ) [G]	$\leq 0.6$	$\leq 0.5$	$\leq 0.4$	$\leq 0.3$	$\leq 0.3$	$\leq 0.2$	$\leq 0.2$	M

Solutions being optimized  
 Manufacturable solutions known  
 Manufacturable solutions NOT known



# 2003 International Technology Roadmap – FEP Parameters

Table 71a Thermal and Thin Film, Doping and Etching Technology Requirements—Near-term

Year of Production	2003	2004	2005	2006	2007	2008	2009	Driver
Technology Node		hp90			hp65			
DRAM $\frac{1}{2}$ Pitch (nm)	100	90	80	70	65	57	50	DRAM
MPU/ASIC $\frac{1}{2}$ Pitch (nm)	107	90	80	70	65	57	50	MPU
MPU Printed Gate Length (nm)	65	53	45	40	35	32	28	MPU
MPU Physical Gate Length (nm)	45	37	32	28	25	22	20	MPU
Equivalent physical oxide thickness for MPU/ASIC $T_{ox}$ (nm) [A, A1]	1.3	1.2	1.1	1.0	0.9	0.8	0.8	MPU
Gate dielectric leakage at 100°C (nA/ $\mu$ m) High-performance [B, B1, B2]	100	170	170	170	230	230	230	MPU
Physical gate length low operating power (LOP) (nm)	65	53	45	37	32	28	25	Low Power
Physical gate length low standby power (LSTP) (nm)	75	65	53	45	37	32	28	LSTP
Equivalent physical oxide thickness for low operating power $T_{ox}$ (nm) [A, A1]	1.6	1.5	1.4	1.3	1.2	1.1	1.0	LOP
Gate dielectric leakage (nA/ $\mu$ m) LOP [B, B1, B2]	0.33	1.0	1.0	1.0	1.67	1.67	1.67	LOP
Equivalent physical oxide thickness for low standby power $T_{ox}$ (nm) [A, A1]	2.2	2.1	2.1	1.9	1.6	1.5	1.4	LSTP
Gate dielectric leakage (pA/ $\mu$ m) LSTP [B, B1, B2]	3	3	5	7	8	10	13	LSTP
Thickness control EOT (% 3 $\sigma$ ) [C]	<±4	<±4	<±4	<±4	<±4	<±4	<±4	MPU/ASIC
Gate etch bias (nm) [D]	20	16	14	12	10	10	8	MPU/ASIC
$L_{gate}$ 3 $\sigma$ variation (nm) [E]	4.46	3.75	3.15	2.81	2.5	2.2	2	MPU/ASIC
Total maximum allowable lithography 3 $\sigma$ (nm) [F]	3.99	3.35	2.82	2.51	2.24	1.97	1.79	MPU/ASIC
Total maximum allowable etch 3 $\sigma$ (nm), including photoresist trim and gate etch [F]	◆ 1.99	◆ 1.68	1.41	1.26	1.12	0.98	0.89	MPU/ASIC

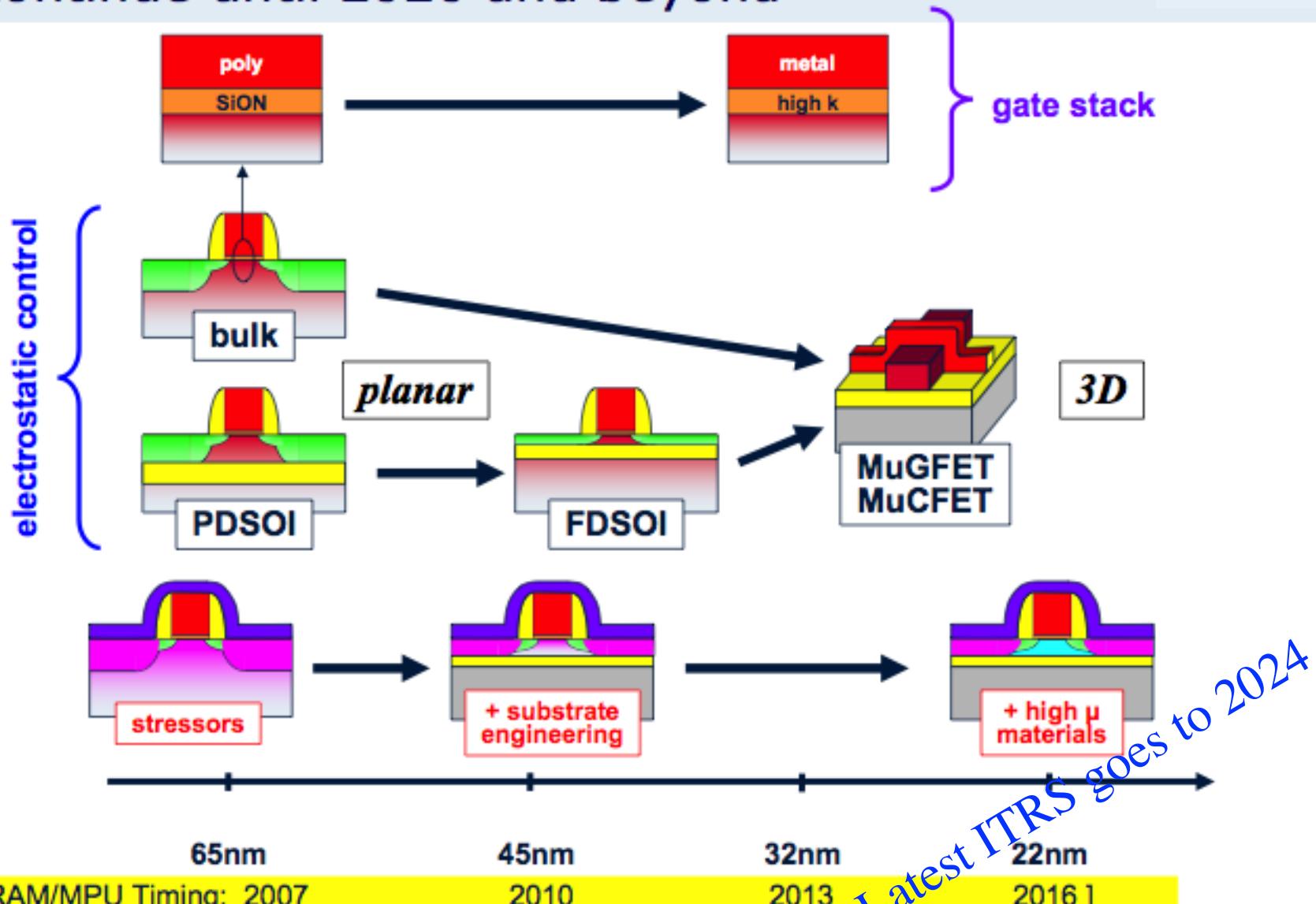
Table 71b Thermal and Thin Film, Doping and Etching Technology Requirements—Long-term

Year of Production	2010	2012	2013	2015	2016	2018	Driver
Technology Node	hp45		hp32		hp22		
DRAM % Pitch (nm)	45	35	32	25	22	18	DRAM
MPU/ASIC % Pitch (nm)	45	35	32	25	22	18	MPU
MPU Printed Gate Length (nm)	25	20	18	14	13	10	MPU
MPU Physical Gate Length (nm)	18	14	13	10	9	7	MPU
Equivalent physical oxide thickness for MPU/ASIC $T_{ox}$ (nm) [A, A1]	0.7	0.7	0.6	0.6	0.5	0.5	MPU/ASIC
Gate dielectric leakage at 100°C ( $\mu\text{A}/\mu\text{m}$ ) high-performance [B, B1, B2]	0.33	0.33	1	1.00	1.67	1.67	MPU/ASIC
Physical gate length operating low operating power (LOP) (nm)	22	18	16	13	11	9	LOP
Physical gate length low standby power (LSTP) (nm)	25	20	18	14	13	10	LSTP
Equivalent physical oxide thickness for low operating power $T_{ox}$ (nm) [A, A1]	0.9	0.9	0.8	0.8	0.7	0.7	LOP
Gate dielectric leakage ( $\text{nA}/\mu\text{m}$ ) LOP [B, B1, B2]	2.33	2.33	3.33	3.33	10	10	LOP
Equivalent physical oxide thickness for low standby power $T_{ox}$ (nm) [A, A1]	1.3	1.2	1.1	1.1	1.0	0.9	
Gate dielectric leakage ( $\text{pA}/\mu\text{m}$ ) LSTP [B, B1, B2]	20	20	27	27	33	33	
Thickness control EOT (% 3σ) [C]	<±4	<±4	<±4	<±4	<±4	<±4	MPU/ASIC
Gate etch bias (nm) [D]	7.1	6	5	4	3.6	3	MPU/ASIC
$L_{gate}$ 3σ variation (nm) [E]	1.8	1.40	1.30	1.00	0.90	0.70	MPU/ASIC
Total allowable lithography 3σ (nm) [F]	1.61	1.25	1.16	0.89	0.80	0.63	MPU/ASIC
Total allowable etch 3σ (nm), including photoresist trim and gate etch [F]	0.8	0.63	0.58	0.45	0.40	0.31	MPU/ASIC
Resist trim allowable 3σ (nm) [G]	0.46	0.36	0.34	0.26	0.23	0.18	MPU/ASIC
Gate etch allowable 3σ (nm) [G]	0.66	0.51	0.47	0.37	0.33	0.26	MPU/ASIC
CD bias between dense and isolated lines [H]	≤15%	≤15%	≤15%	≤15%	≤15%	≤15%	MPU/ASIC
Minimum measurable gate dielectric remaining (post gate etch clean) [I]	>0	>0	>0	>0	>0	>0	MPU/ASIC
Profile control (side wall angle) [J]	90	90	90	90	90	90	MPU/ASIC
PIDS Assumed Device Structure *	FDSOI *		FDSOI, Multi-Gate *				
Drain extension $X_d$ (nm) [K]	7.2	11.2	10.4	8.0	7.2	5.1	MPU/ASIC
Maximum drain extension sheet resistance (PMOS) ( $\Omega/\text{sq}$ ) [L]	1875	518	514	550	549	584	MPU/ASIC
Maximum drain extension sheet resistance (NMOS) ( $\Omega/\text{sq}$ ) [L]	875	242	240	257	256	272	MPU/ASIC

2003 ITRS

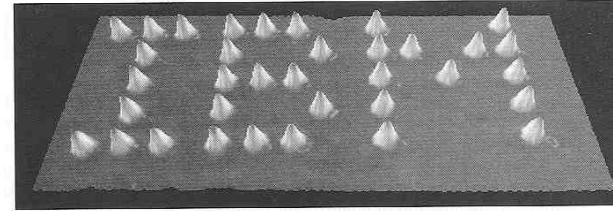
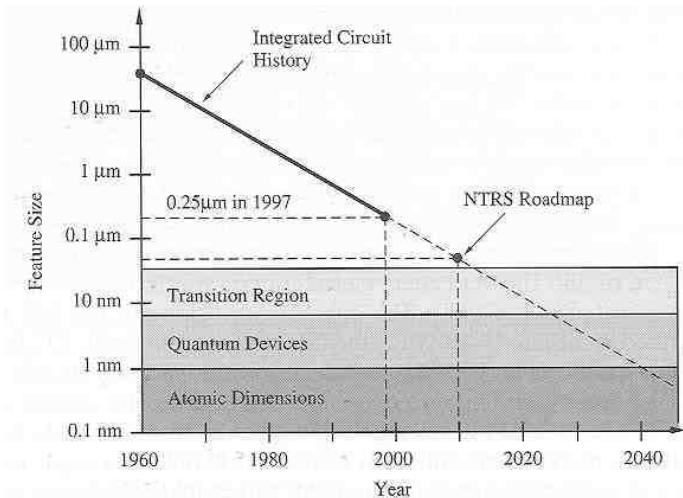
The “red brick wall”

## Roadmap predicts scaling of transistors to continue until 2020 and beyond



Source: ITRS, European Nanoelectronics Initiative Advisory Council (ENIAC)

# ITRS Roadmap: Beyond CMOS

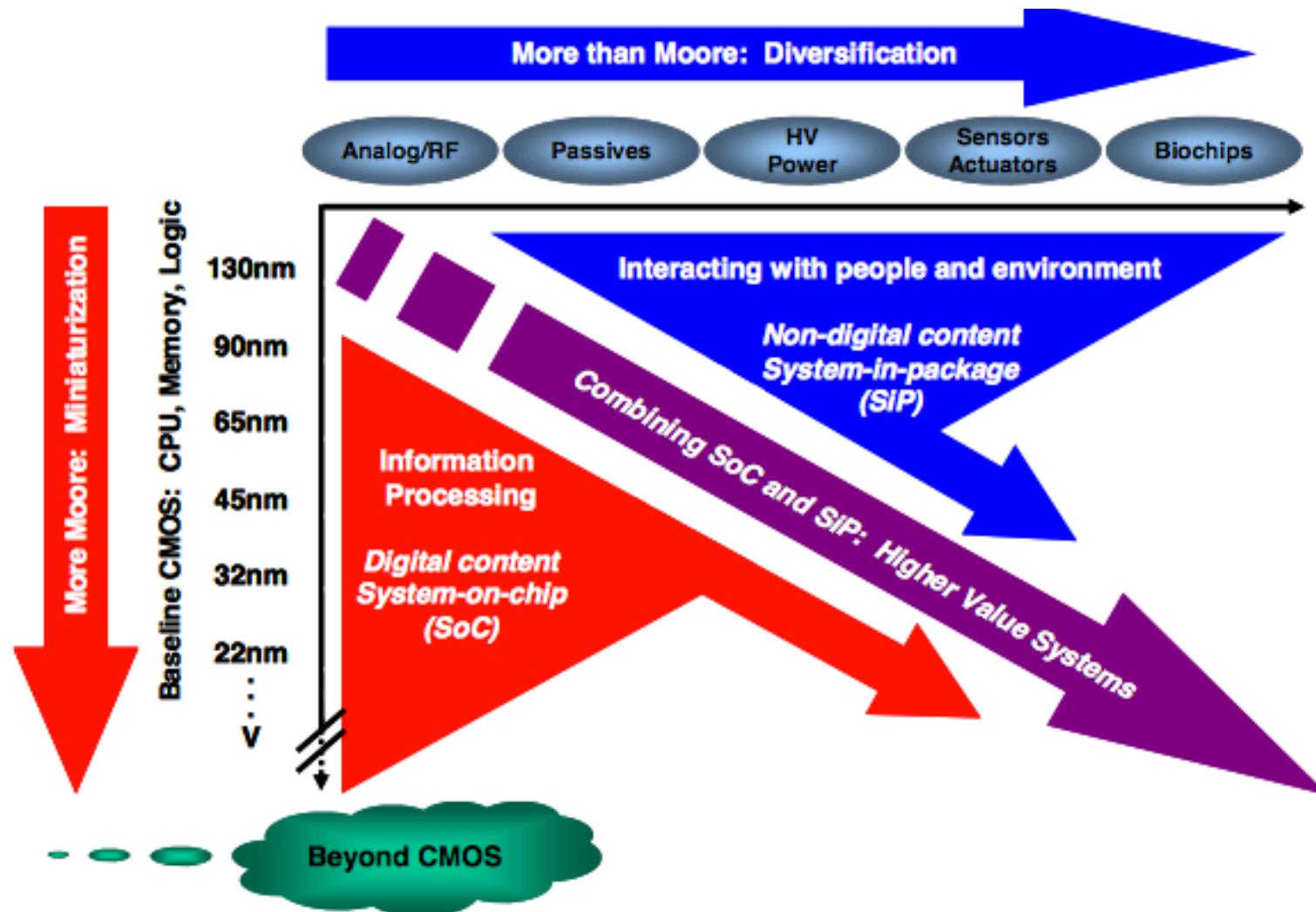


**Xe atoms individually placed on a Ni single crystal surface.**

Beyond CMOS: What's next? Quantum devices (QDs)?

In fact, state-of-the-art semiconductor structures will soon be plagued by dopant fluctuation and particle noise problems as well as quantum mechanical effects such as state discretization and tunneling. Quantum dots are beyond the ITRS roadmap, since it remains focused silicon scaling. However, QDs do offer near-term applications to far infrared detectors and sources in other material systems. In fact QDs have been developed since the late 1980's and several implementations have already reached room temperature operation. Quantum dot device and circuit concepts utilize rather than fight the discreteness of the electron charge and they offer a possible breakthrough in device and circuit technology.

Source: [http://hpc.jpl.nasa.gov/PEP/gekco/nemo3D/SIA\\_roadmap\\_leap.html](http://hpc.jpl.nasa.gov/PEP/gekco/nemo3D/SIA_roadmap_leap.html)

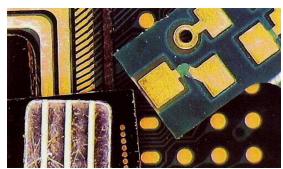


**Fig. 3 –** The combined need for digital and non-digital functionalities in an integrated system is translated as a dual trend in the International Technology Roadmap for Semiconductors: miniaturization of the digital functions (“More Moore”) and functional diversification (“More-than-Moore”).

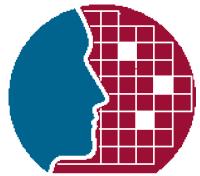
For an informative book on  $\mu$ -electronics to 2024 see:

Bernd Hoefflinger (ed), *Chips 2020: A Guide to the Future of Nanoelectronics*, Springer  
<http://link.springer.com/book/10.1007%2F978-3-642-23096-7>

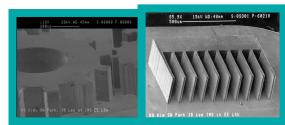
# Electronics and Nature



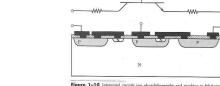
PCB



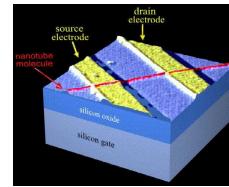
Diced chip



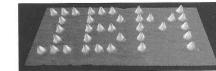
MEMS devices



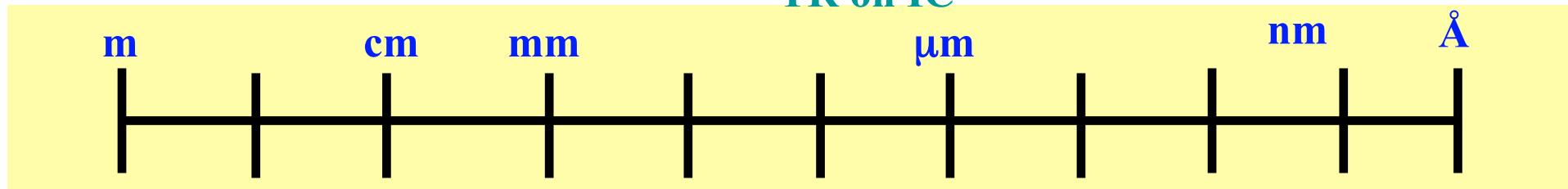
TR on IC



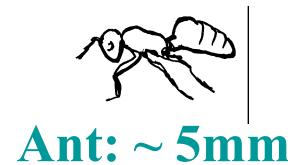
Nanotube FET



Nano manipulation



Human:  
~ 2 m

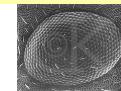


Ant: ~ 5mm

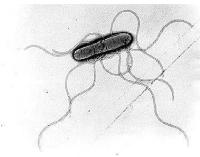
Grain of sand:  
~ 1 mm



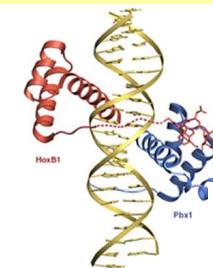
Hair: ~  
100 μm



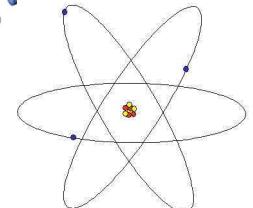
Ant eye  
segment:  
~ 5 μm



Bacteria:  
~ 0.1 μm



DNA:  
~ nm



Atom:  
~ Å

about sizes somewhat relevant to technology

# \$ Dollars & Sense

- Electronics market
  - ~ \$ 1.2 trillion
  - IC sales (annual worldwide)
    - ~ \$ 345 billion (2003)
    - exponential increase with time over the past 3 decades
    - cost for electronic function exponentially decreases
  - Personal computers
    - 100 ~ 200 millions sold
- So, what does it mean to me?
  - Yeah, there are plenty of high salary jobs !!!! 😊
- Automobiles sales
  - ~ 50 million cars sold

