FYS4310

RTA

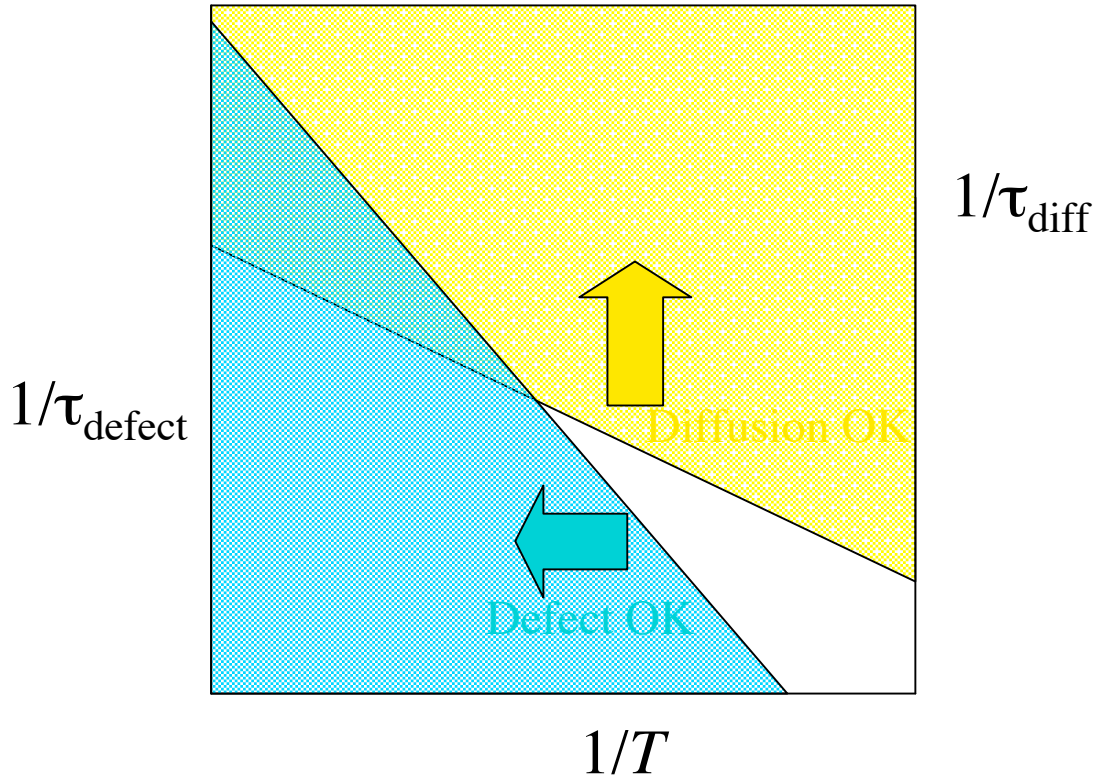
Rapid Thermal Annealing

'History of fast thermal processing:'

Laserzapping, Ion beam zap, Laser scan, Q switch, CW, Electron Beam Zap,

Why RTA

The selling argument for I^2 annealing:



What is RTA

600-1200°C

2s-60s

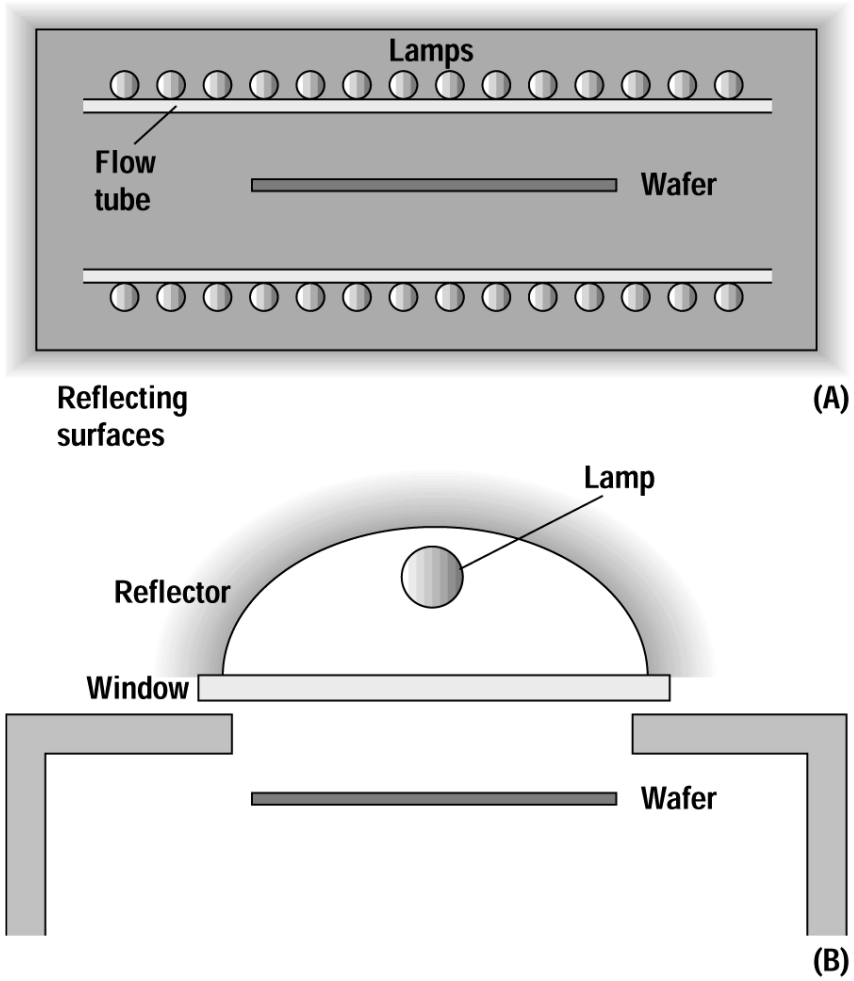


Figure 6.4 Various chamber designs include (A) the reflecting cavity and (B) a windowed system using an intense source and a shaped reflector.

Industrial heating lamps

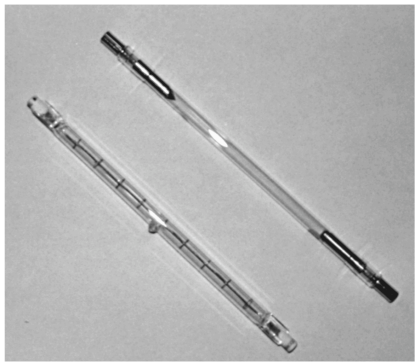


Figure 6.3 Tungsten–halogen lamps (left) and noble gas arc lamps (right) for use in rapid thermal systems.

What is RTA II

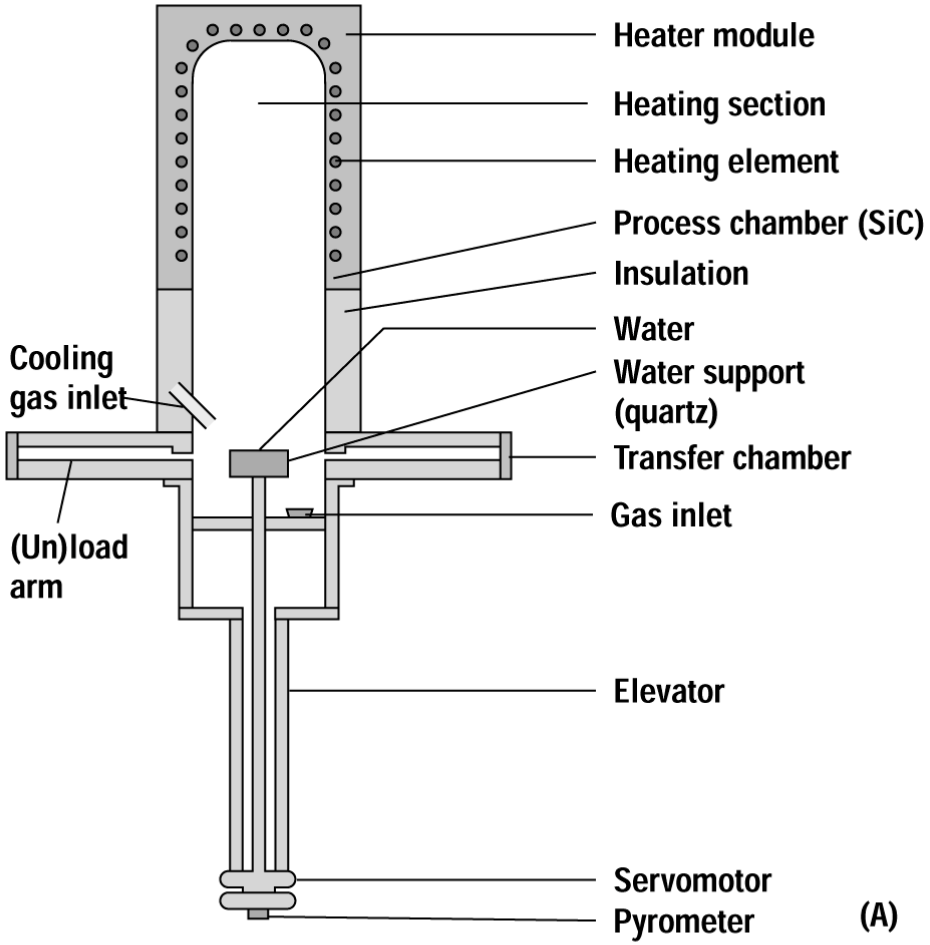


Figure 6.15 New designs for high uniformity RTP include the hot wall system *(after Roozeboom and Parekh).*

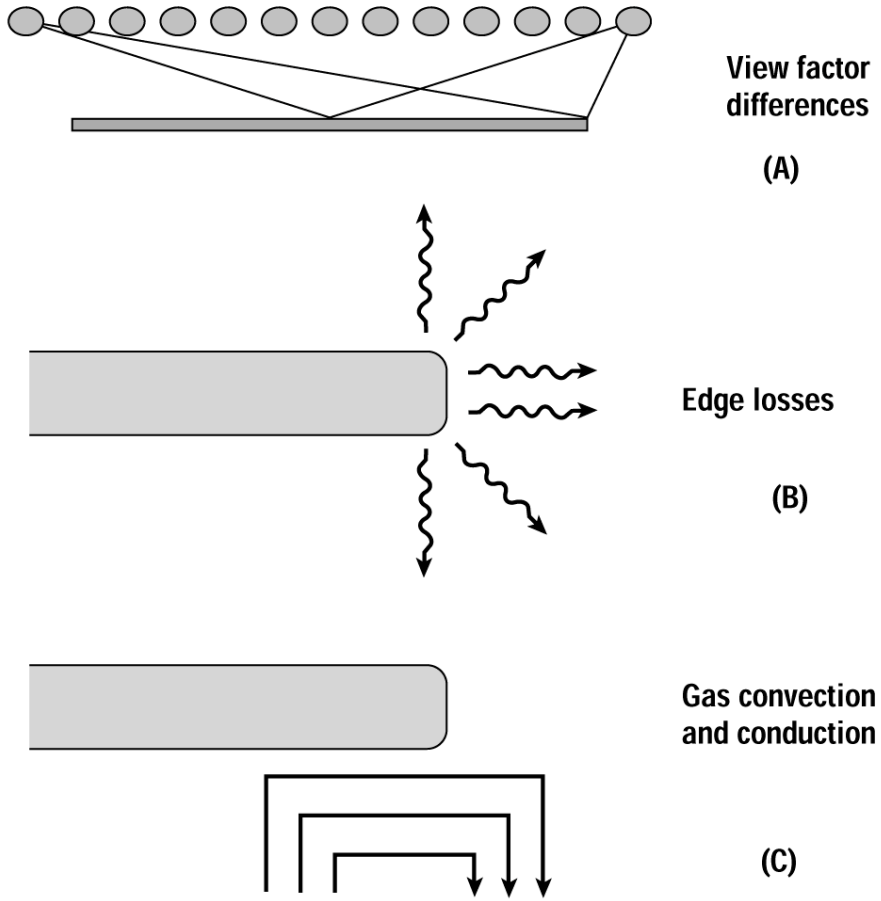


Figure 6.5 Causes of thermal nonuniformity include (A) a reduced view factor to the lamp array for large *r*, (B) very small view factors along the wafer edge, and (C) nonuniform gas phase heat transfer *(after Campbell, 1994).*

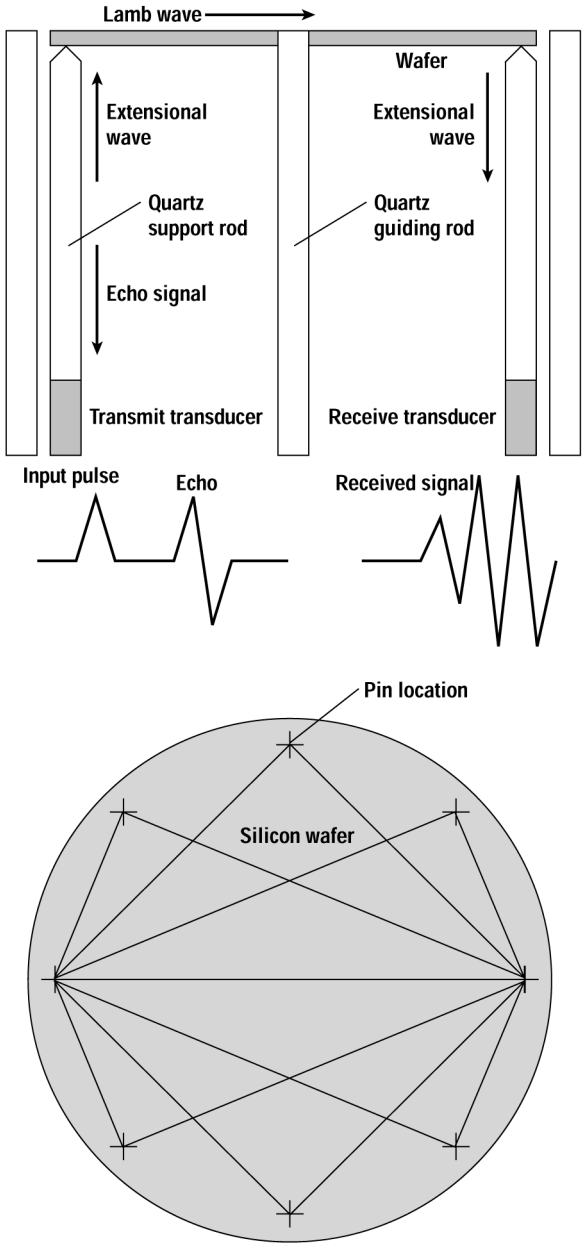


Figure 6.9 Acoustic temperature measurement side and top views *(after Degertekin et al., used by permission, Materials Research Society).*

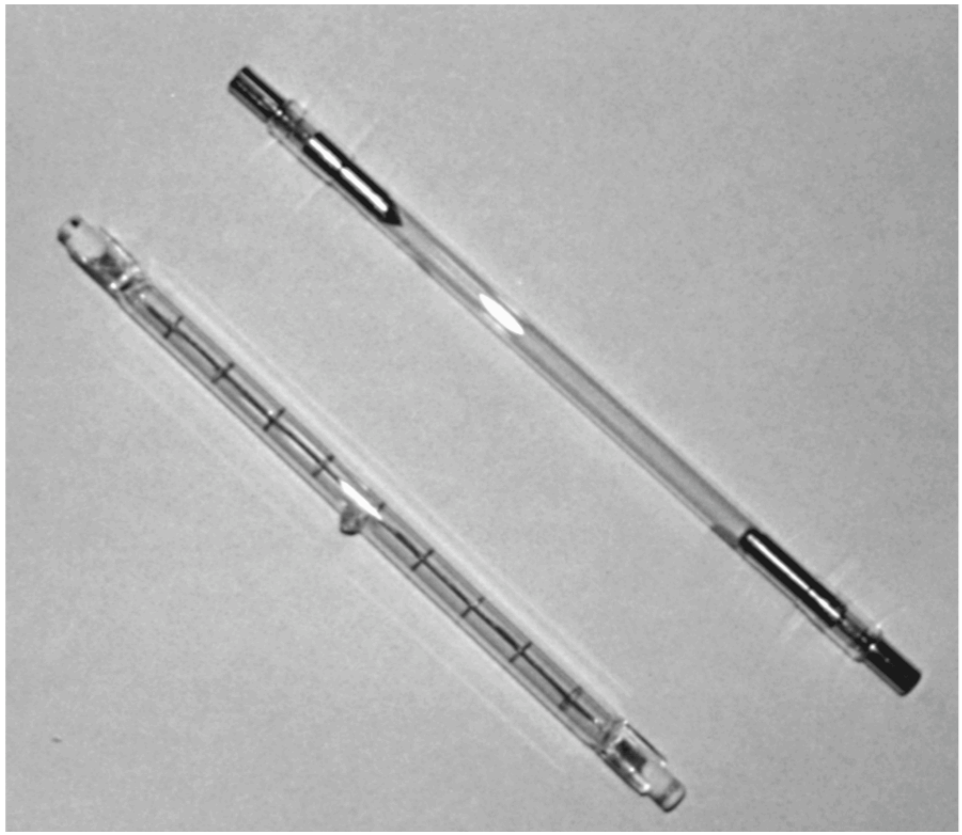


Figure 6.3 Tungsten–halogen lamps (left) and noble gas arc lamps (right) for use in rapid thermal systems.

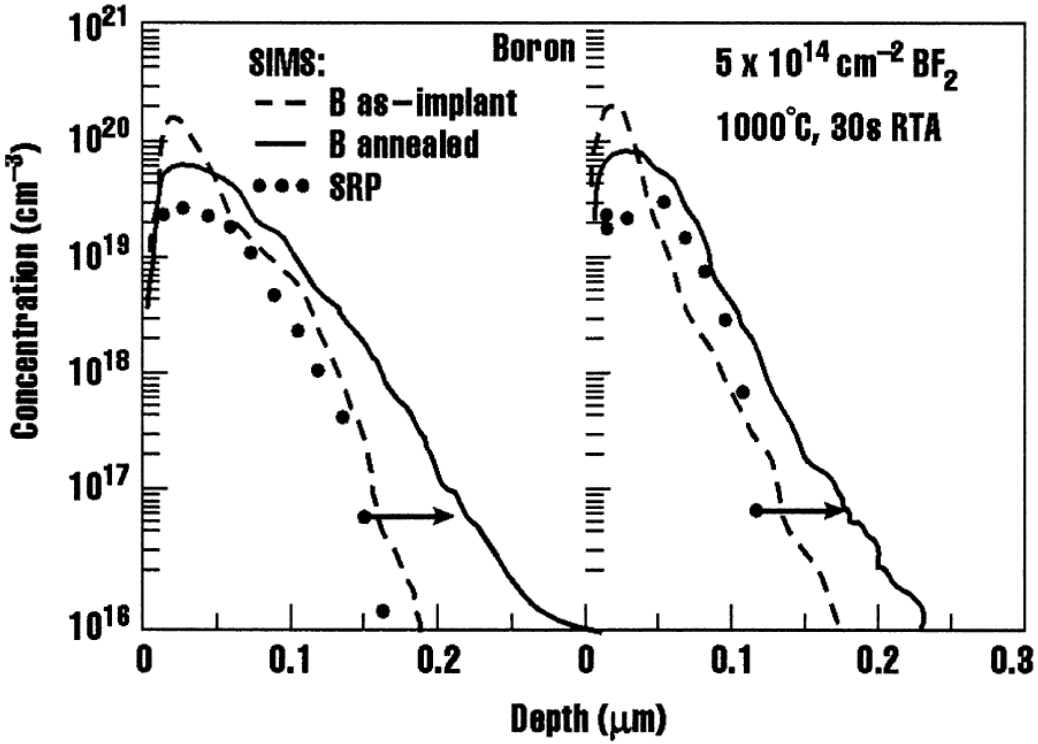


Figure 6.11 Chemical and active boron profiles after incomplete activation in RTP *(after Kinoshita et al., used by permission, Materials Research Society).*

Transient enhanced diffusion

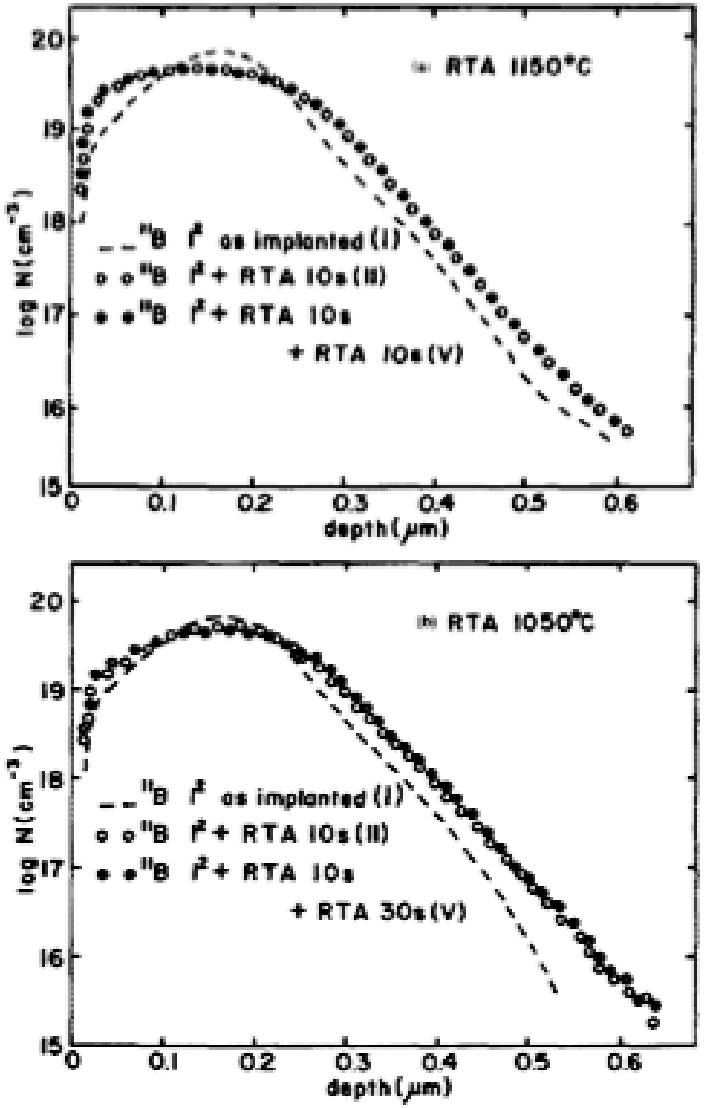


FIG. 1. SIMS profiles of ^{11}B implanted (50 keV, 1×10^{15}) into Si. The figure compares the as-implanted profiles with those after a single RTA (sample type II, Table I) or a double RTA (type V): (a) 1150 °C, (b) 1050 °C.

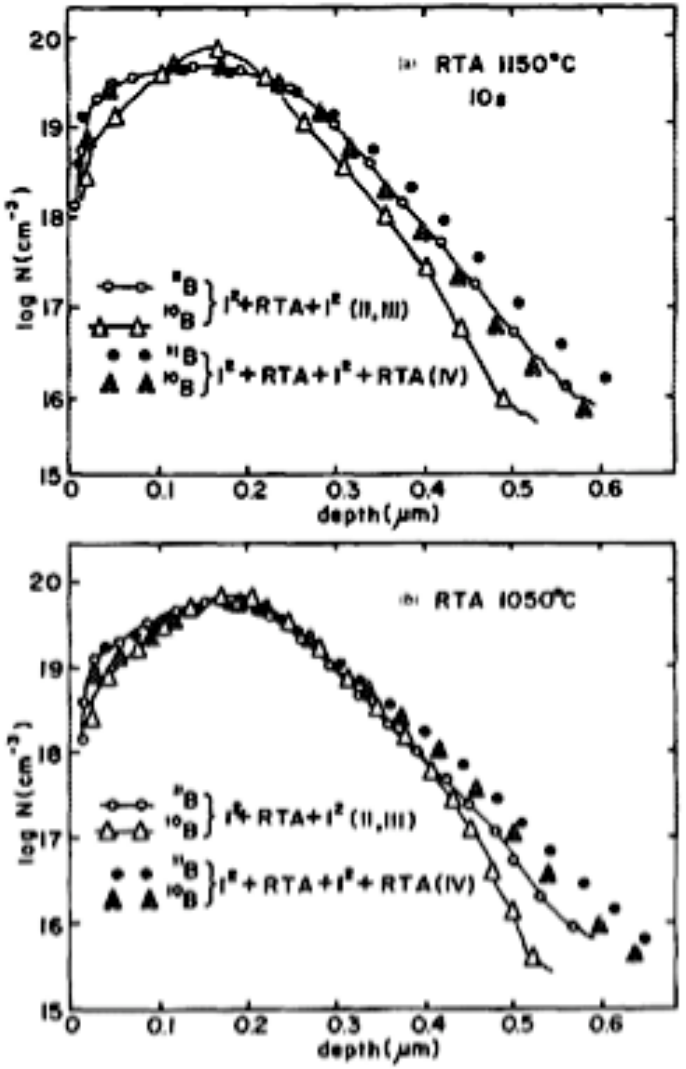


FIG. 2. SIMS profiles of ^{10}B and ^{11}B (both 50 keV, 1×10^{15}) after different RTA cycles (sample types II, III, IV): (a) (O–O–O) ^{11}B profiles of sample type (II): ^{11}B + RTA (1150 °C/10 s) and (III): ^{11}B + RTA + ^{10}B. (△–△–△) ^{10}B profiles of sample type (III): ^{11}B + RTA + ^{10}B. Solid symbols are the ^{11}B (●) and ^{10}B (▲) profiles of sample type (IV): ^{11}B + RTA + ^{10}B + RTA. (b) Same as (a) except the RTA temperature is 1050 °C.

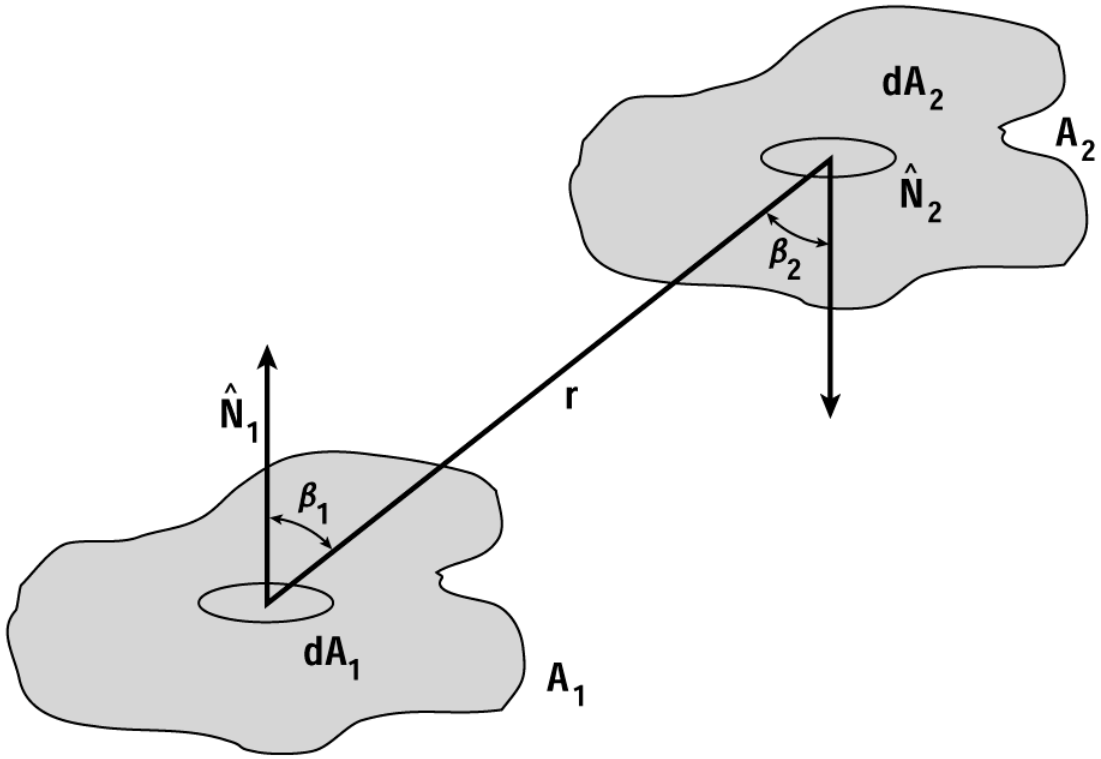


Figure 6.1 Geometry for calculating the view factors between two surfaces, A_1 and A_2.

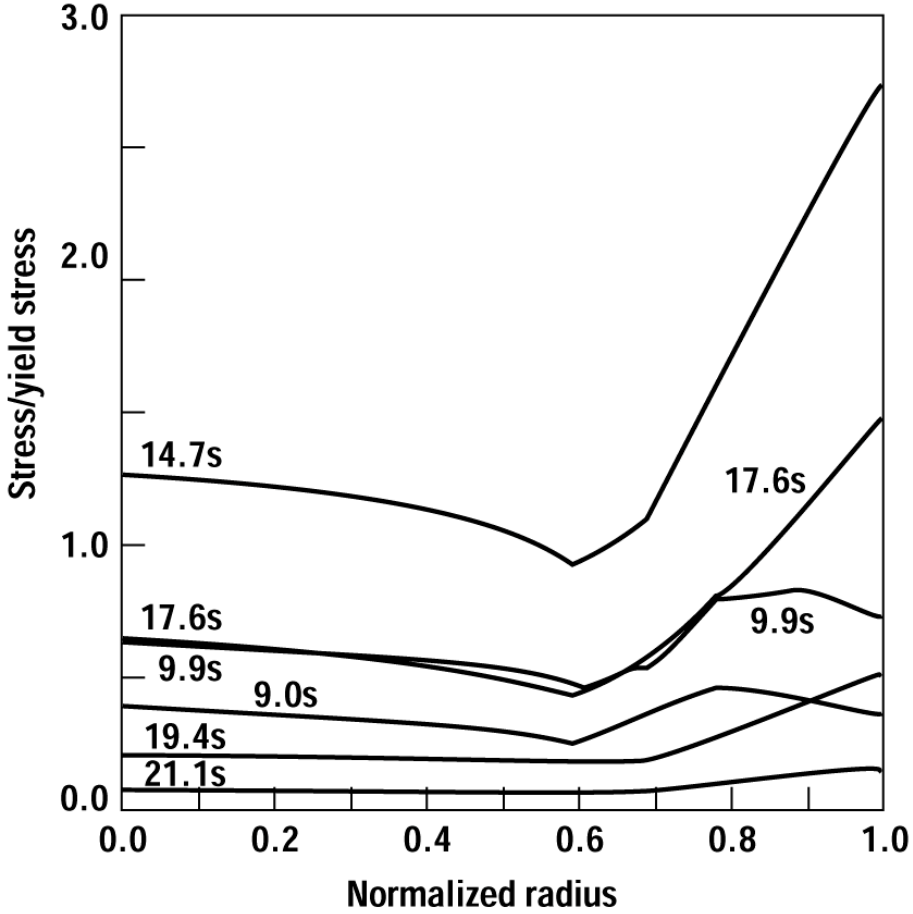


Figure 6.10 Normalized stress versus position on a wafer during a heating transient *(after Lord, © 1988, IEEE).*

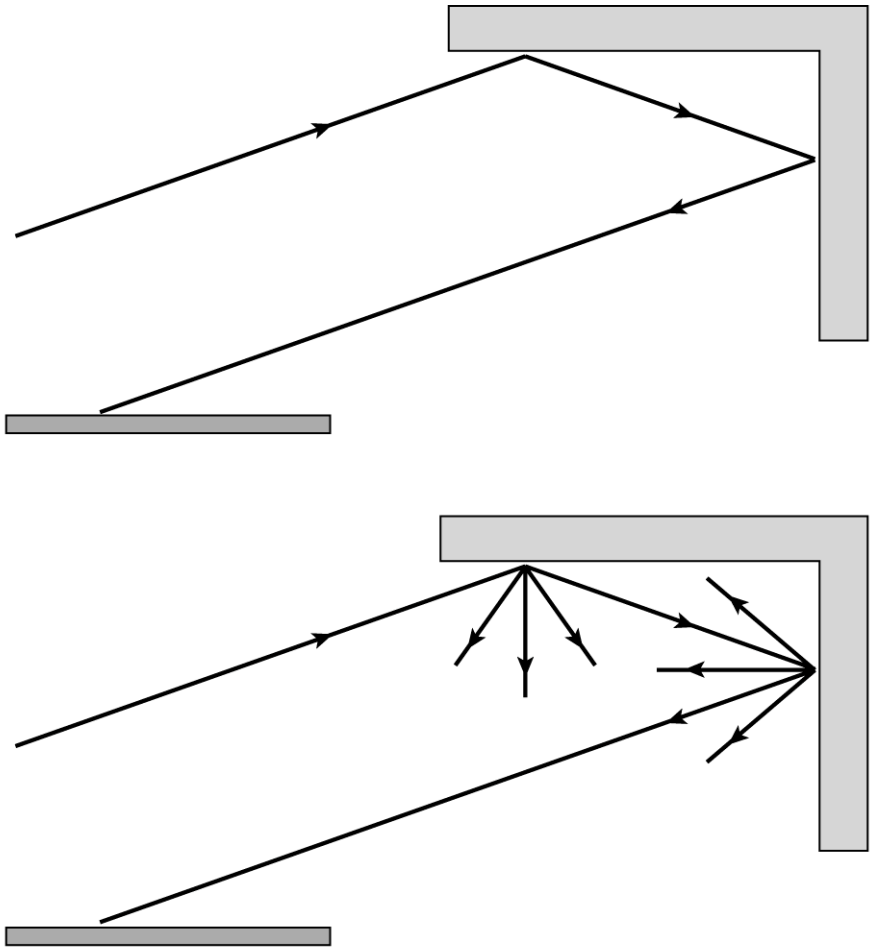


Figure 6.2 Possible optical paths among three surfaces including only single reflections. This diagram assumes diffuse reflections.

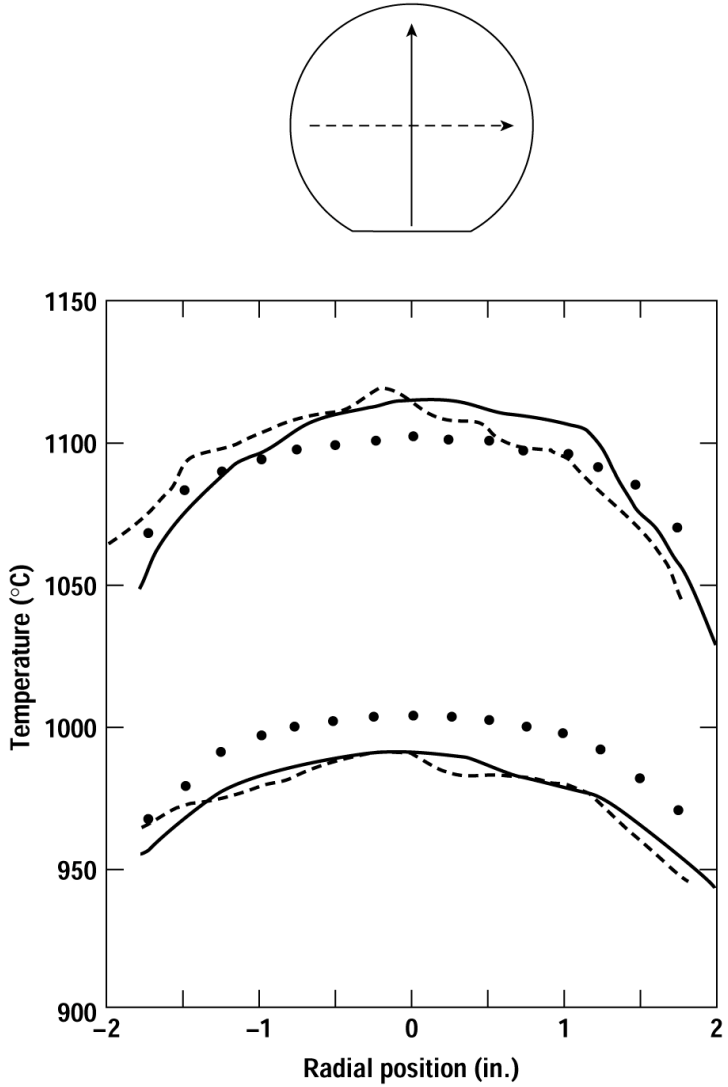


Figure 6.6 Typical wafer temperature distributions across the wafer in an early-generation rapid thermal system (*after Lord, © 1988 IEEE*).

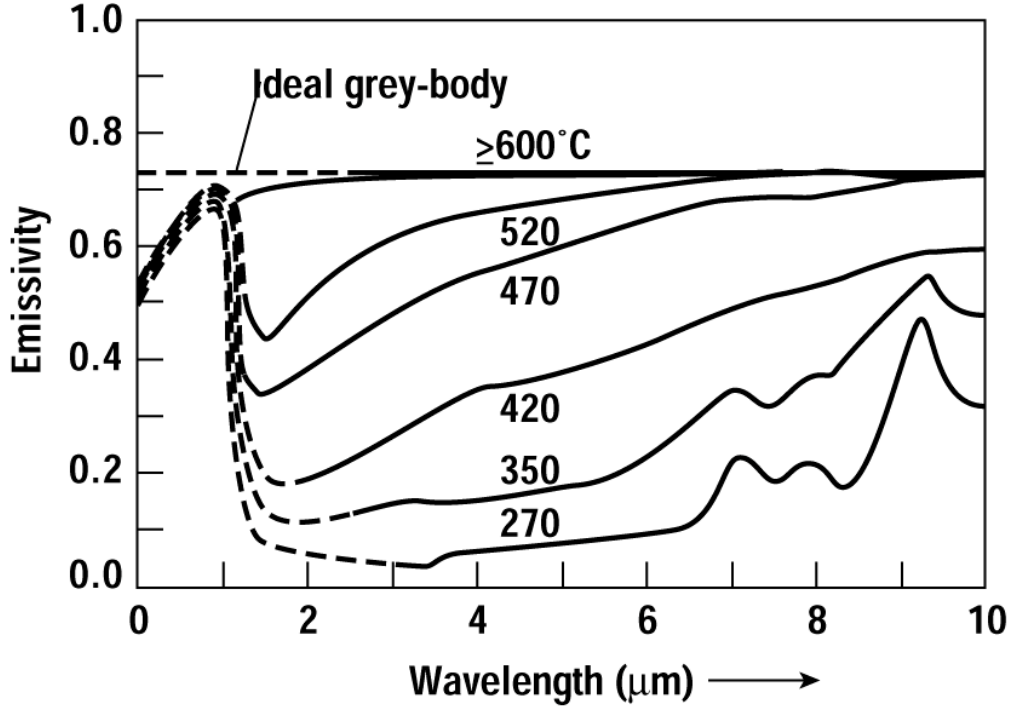


Figure 6.7 The emissivity of silicon as a function of wavelength with temperature as a parameter. Above 600°C the wafer is intrinsic *(after Sato, reprinted by permission, Japan. J. Appl. Phys.).*

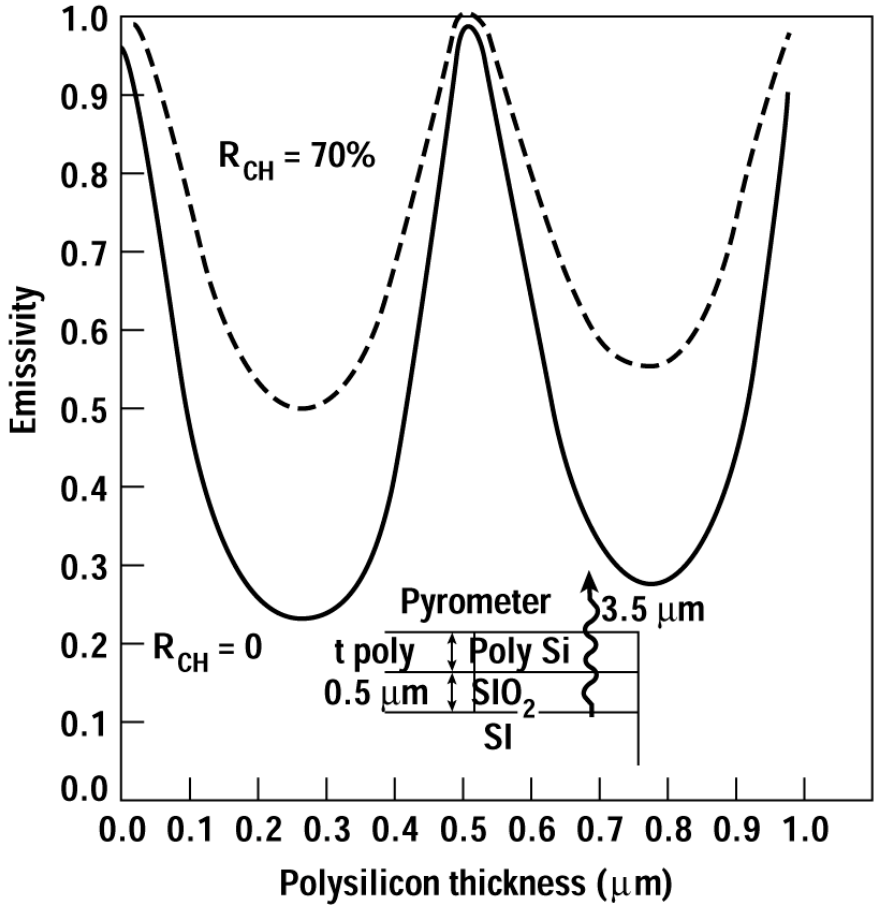


Figure 6.8 The effect of polysilicon thickness on effective emissivity for a polysilicon/SiO_2/silicon structure in nonreflective and 70% reflective cavities *(after Hill and Boys, reprinted by permission, Plenum Publishing).*

RTO-Rapid thermal oxidation

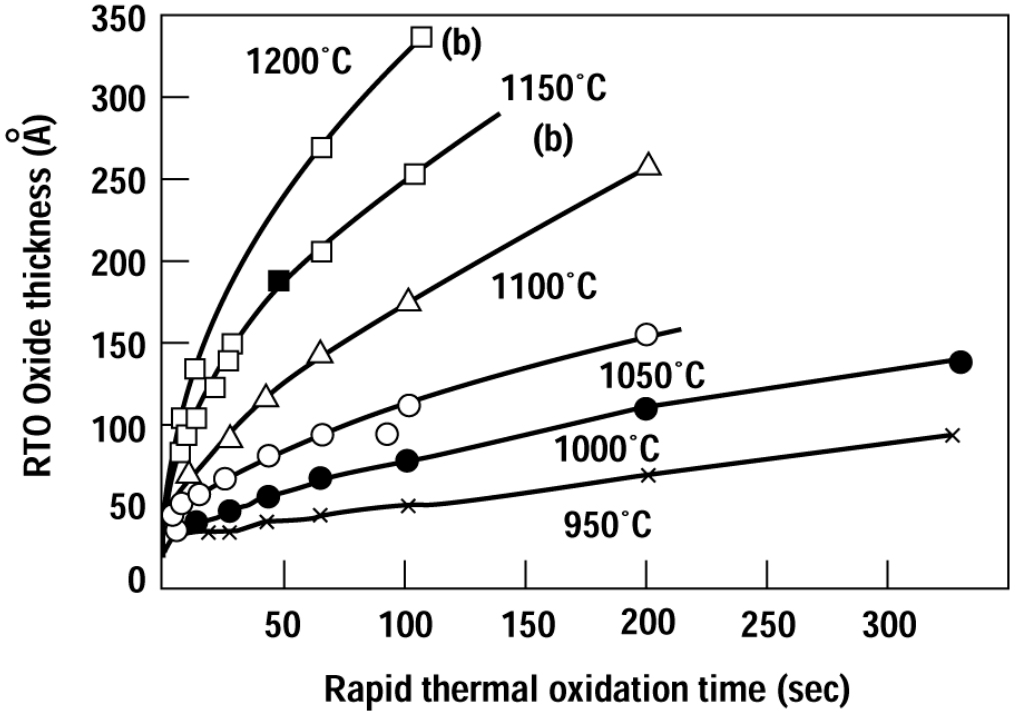


Figure 6.13 Typical data for oxide thickness as a function of time for a rapid thermal oxidation process *(after Moslehi et al., 1985).*