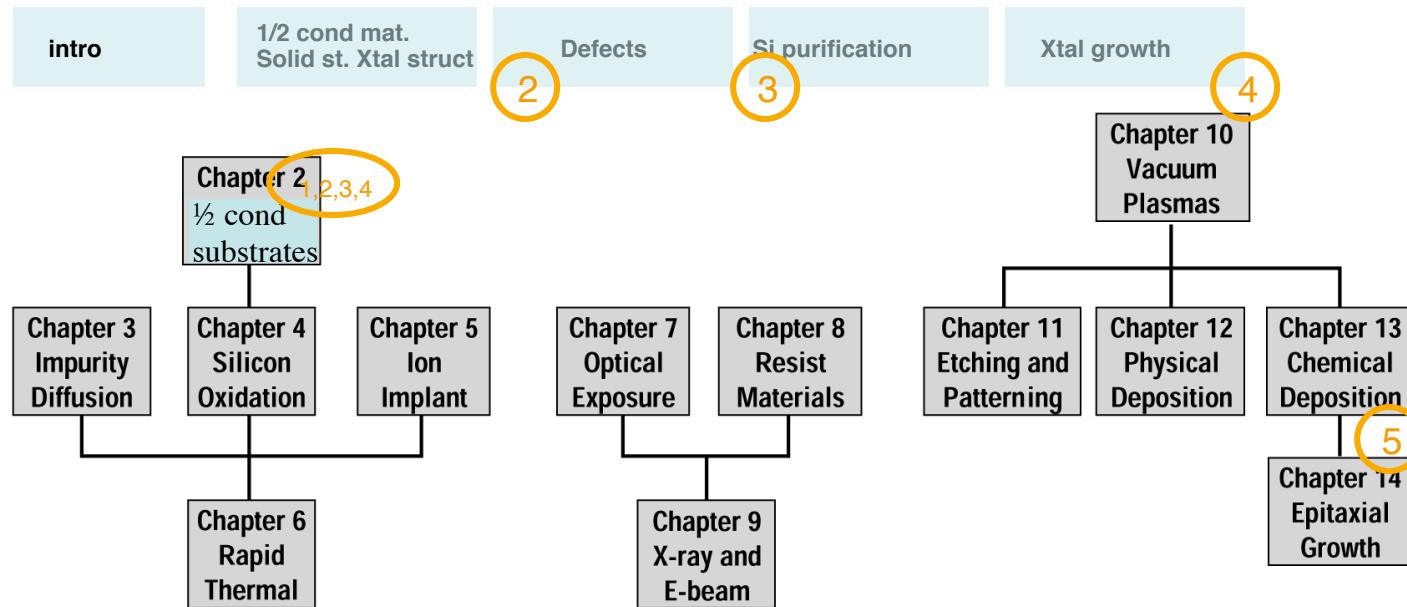


FYS4310

Process integration

Unit processes



Technologies

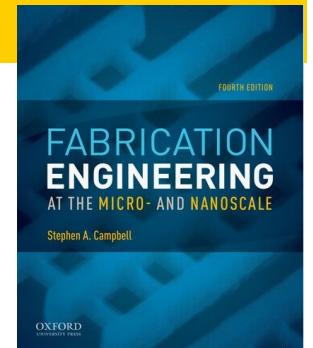
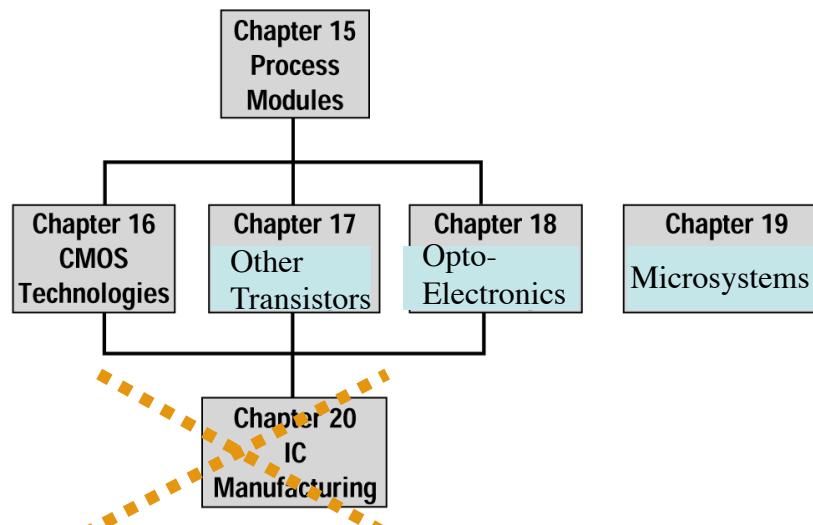


Figure 1.7 A roadmap for the course indicating the relationships between the chapters.

Process module Device Isolation

Purpose:

Isolate individual devices, such as transistors, in a circuit so that they will work independent of each other

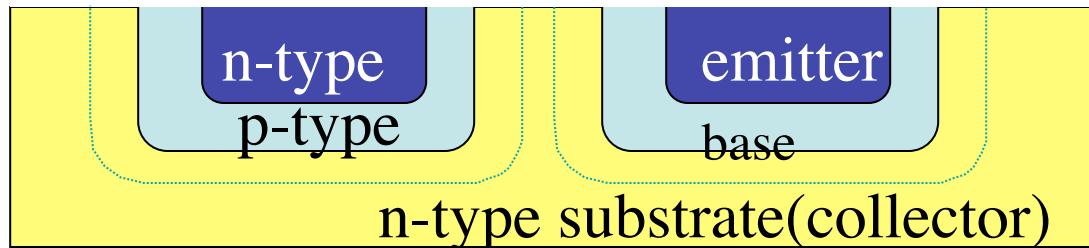
Simplest: p-n junction isolation,
Other: oxide insulation

Device isolation 2

pn junction isolation

Example, two bipolar transistors:

Common collector



Depletion layer width

$$W_D = \sqrt{\frac{2k_s \epsilon_0}{qN_D} (V_{bi} + V_{CB})} \quad V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right)$$

Example $N_D=10^{16} \text{ cm}^{-3}$: $W_D \approx 0.36 \mu\text{m} \sqrt{(V_{bi} + V_{CB})}$

$V_{BC}=0..10\text{V}; 2W_D=2.4 \mu\text{m}$

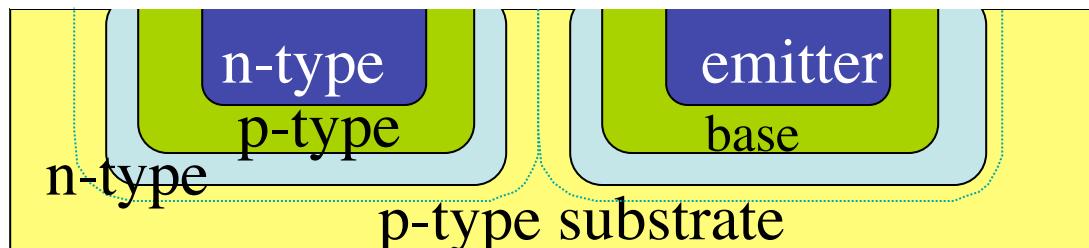
Device isolation 3

pn junction isolation

Example, two bipolar transistors:

Complete isolation

*first practical isolation
patented 1959*



Depletion layer width

$$\text{Example } N_A = 10^{15} \text{ cm}^{-3} : \quad W_D \approx 1.14 \mu\text{m} \sqrt{(V_{bi} + V_{cs})}$$

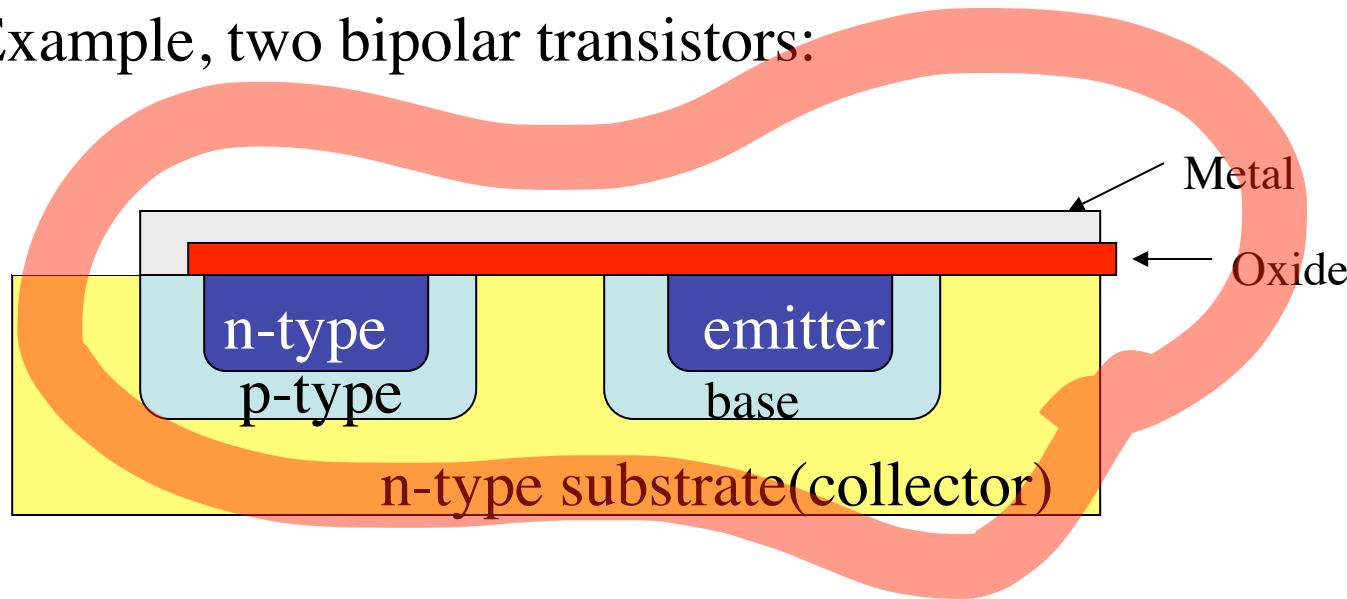
$$V_{cs} = 0..10\text{V}; 2W_D = 4 \mu\text{m}$$

This influences area packing density; above example gives $10^5/\text{cm}^2$:

Device isolation 4

pn junction isolation

Example, two bipolar transistors:



Parasitic MOS transistor!

$$V_T = \phi_{MS} + 2\phi_f + \frac{k_s t_{ox}}{k_{ox}} \sqrt{\frac{4qN_D}{k_s \epsilon_0}} \phi_f \quad \phi_f = \frac{kT}{q} \ln\left(\frac{N_D}{n_i}\right)$$

:

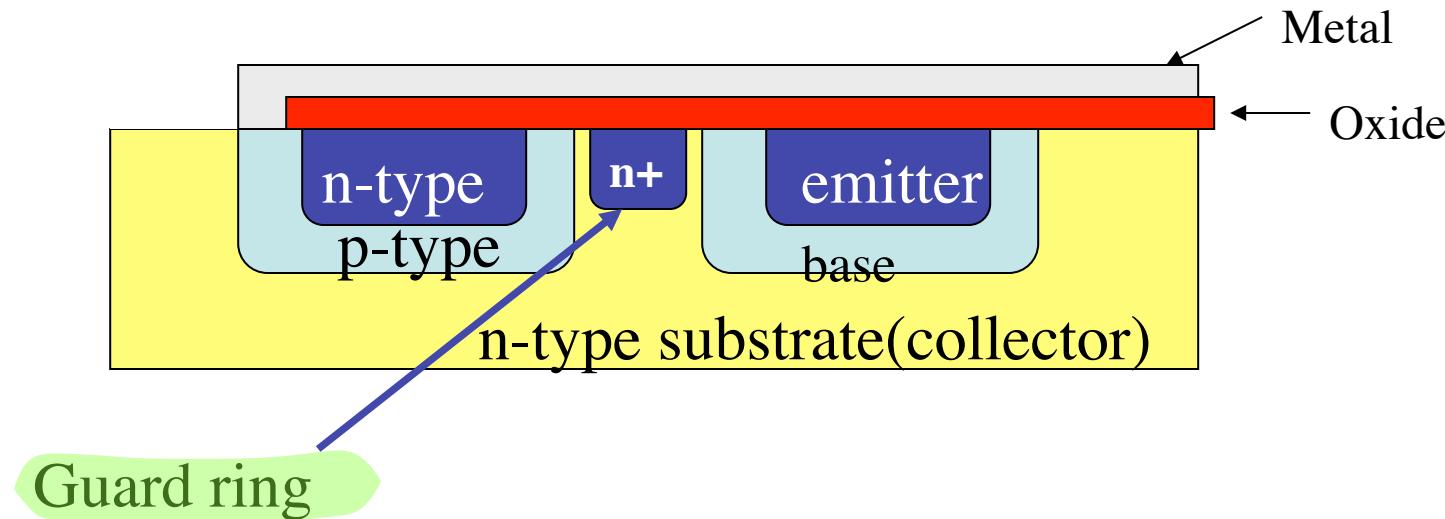
One must select a thick oxide and/or large substrate concentration.

The large substrate concentration degrades performance due to junction capacitance.

Device isolation 5

pn junction isolation

Example, two bipolar transistors:



:

Device isolation 6

pn junction isolation summary

It is simple - can expect a high yield

Produce a planar isolation

Density not very large - trade off parasitic cap

Used for low density, low cost applications



Device isolation 7

Insulation

We need thick oxide for device isolation

Could have been: first grow thick SiO_2
then open holes - why not?

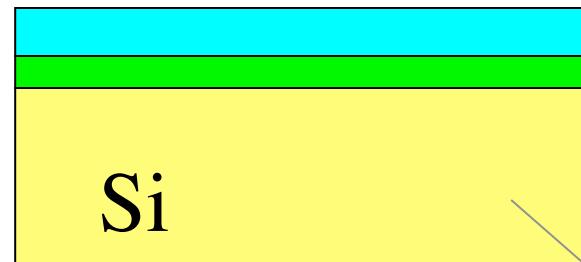
The standard is LOCOS,
Local Oxidation of Si/semicond.
Addresses isolation and parasitic

FYS4310

Device isolation 8

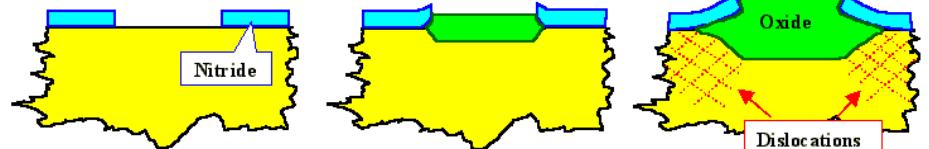
LOCOS, the process steps

Si_3N_4



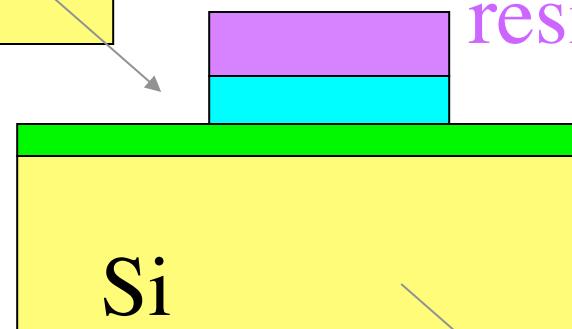
SiO_2

Si



Oxide

Dislocations

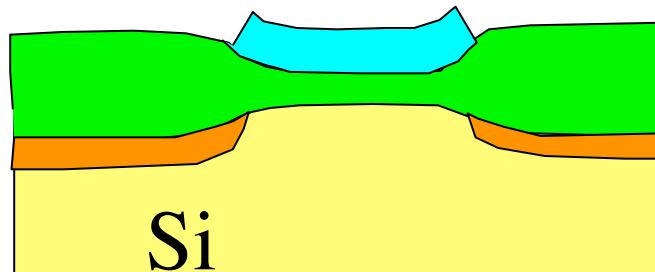


resist

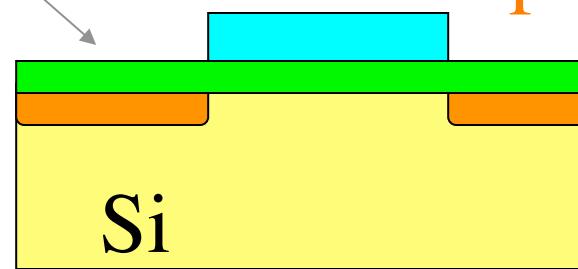
Si

implant

oxidation



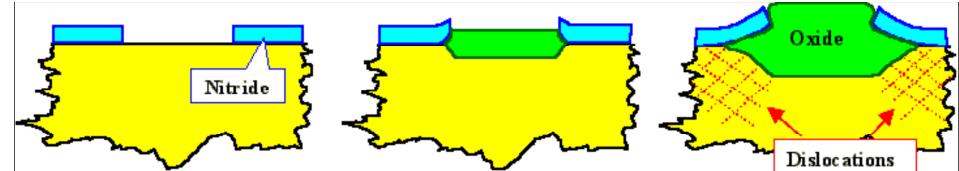
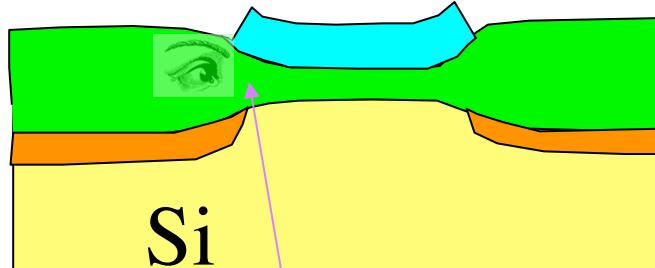
Si



Si

Device isolation 9

LOCOS, the process steps 2



Why thin SiO_2 pad oxide?

Reduce stress. Why stress?

Thermal expansion Si_3N_4 and Si.

Volume mismatch Si SiO_2 during oxidation

Viscous flow at high T reduce the stress and the latter effect

Dislocations could be produced

Tradeoff thick pad oxide less stress in substrate

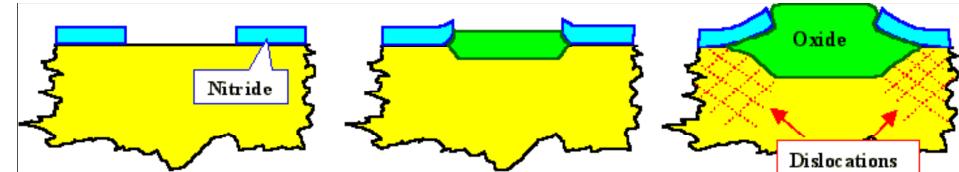
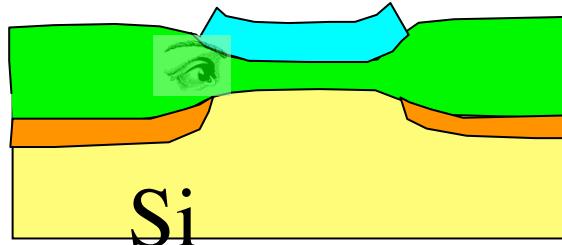
more lateral encroachment

Birds beak, want as small as possible for increased packing dens

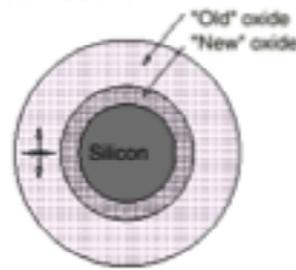
White ribbon effect (=detail)

Device isolation 9b

LOCOS, stress



- Oxide growing on a curved surface must flow



- Resulting deformations (and stresses) can be large! LOCOS top surface must stretch by 15-20%



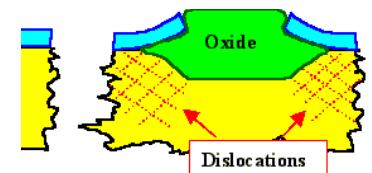
Several physical mechanisms are important in explaining these results:

- Crystal orientation -impacts oxidation rate in the thin oxide regime
- 2D oxidant diffusion -numerical techniques required to solve diffusion equation in multiple dimensions (simple to implement in a 2D simulator)
- Stress due to volume expansion: Oxide layers formed on silicon are under compressive stress, even in the planar case. These stresses can be much larger on curved surfaces, because the volume expansion is dimensionally confined.

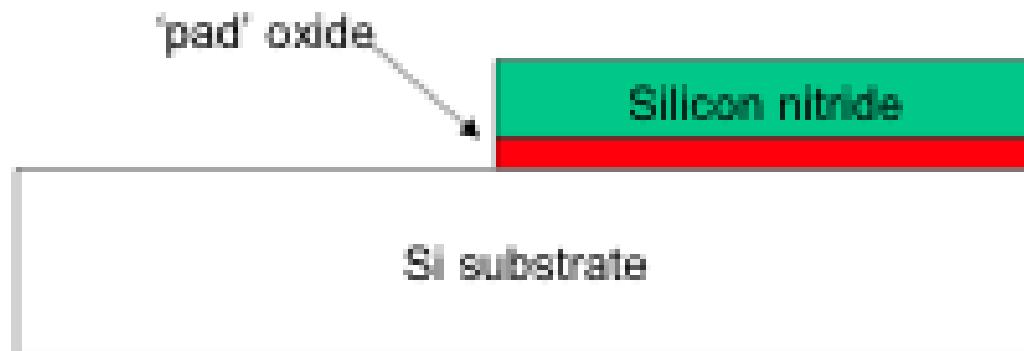
Device isolation 9c

LOCOS, stress

Since the shape of the growing oxide changes with time, k_s (stress), D (stress), and η (stress) all change with time during the oxidation. Numerical simulation is therefore required. This has been implemented in SUPREM IV, which can model oxide shapes on curved surfaces.



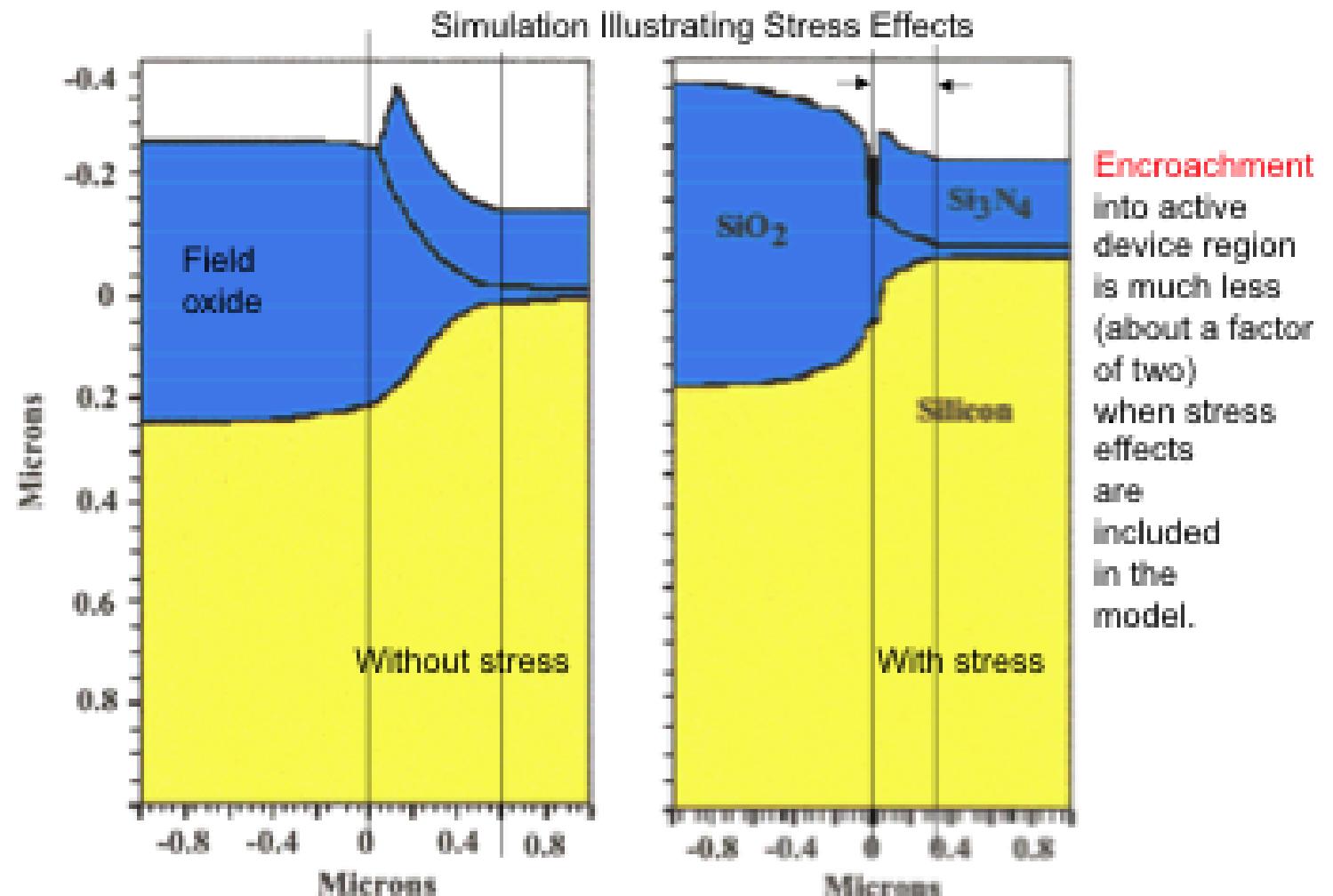
Isolation processes often involve oxidation of shaped surfaces:
LOCOS, poly-buffered LOCOS, shallow trench oxidation



LOCOS example (starting structure, before oxidation)

Device isolation 9d

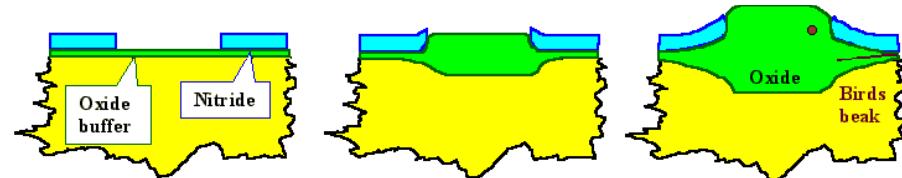
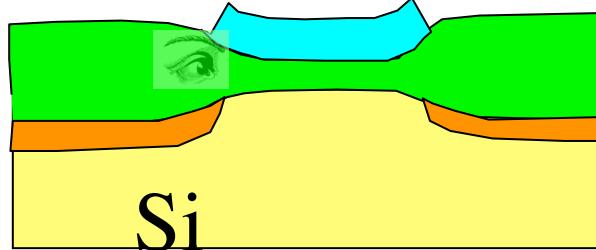
LOCOS, stress, encroachment



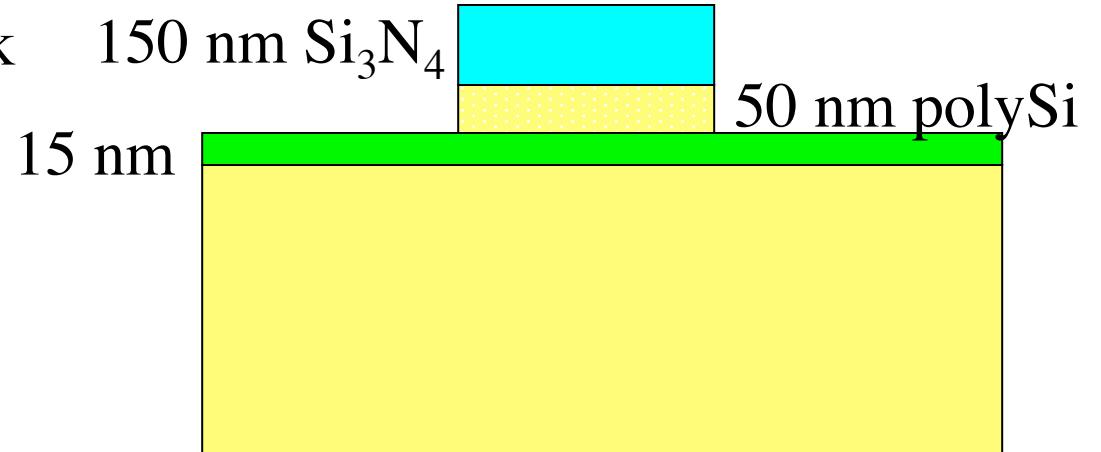
90 min. LOCOS at 1000C, using 20 nm pad-oxide and 150 nm-nitride
(start with Planar surface)

Device isolation 10

LOCOS, alternative process 1



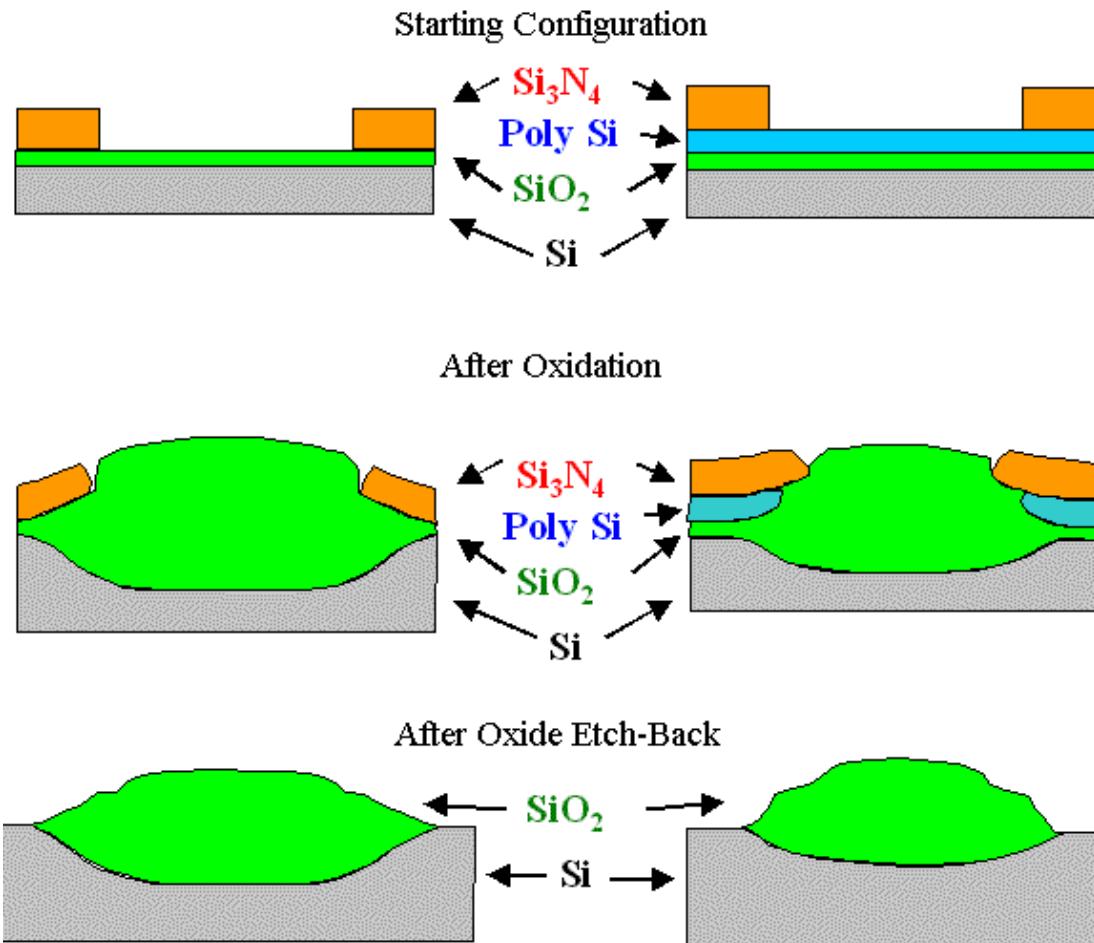
Want to reduce bird's beak
 $\text{SiO}_2 + \text{polySi}$
poly Si takes up stress



It does work! See also next page
Why?

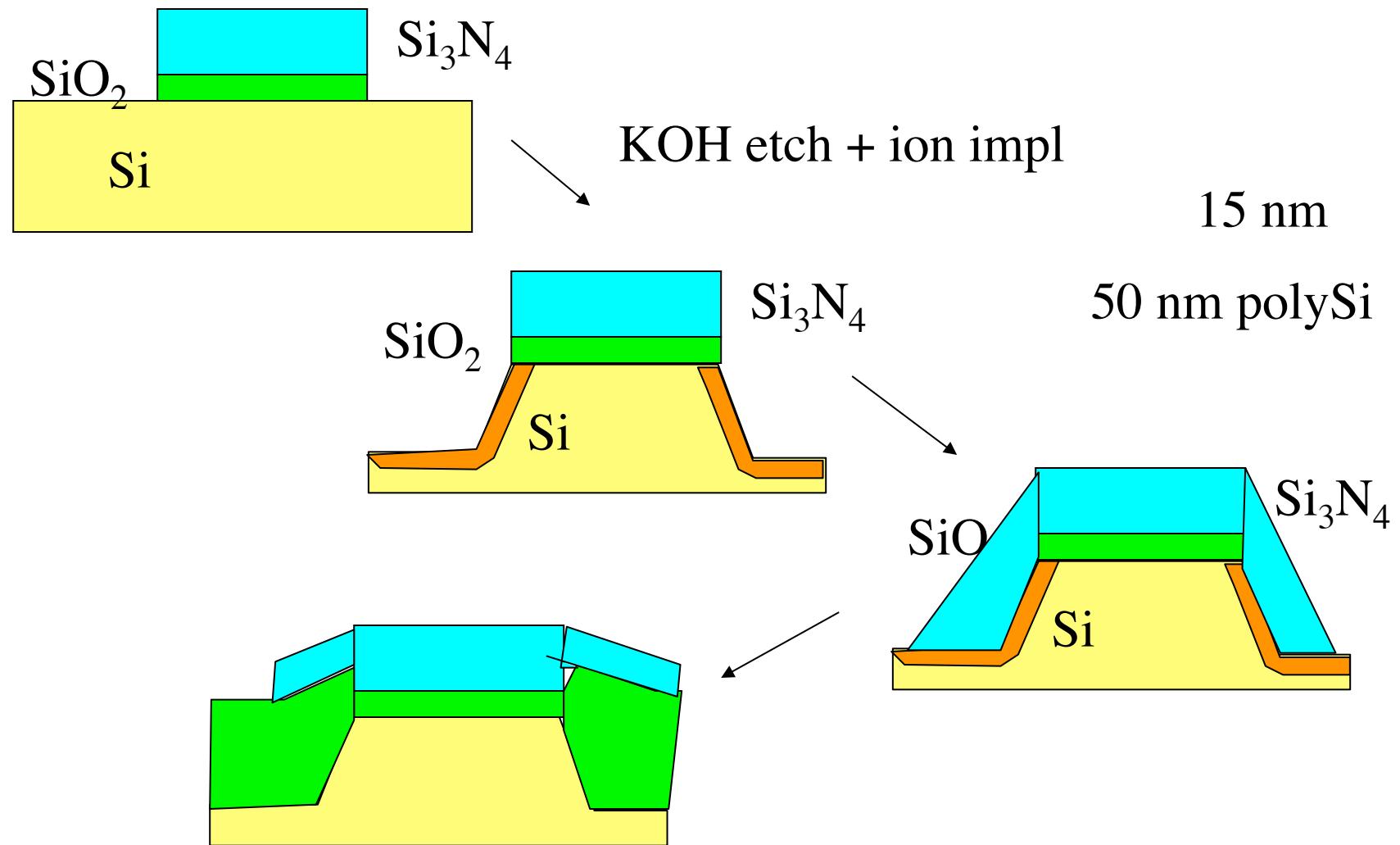
Device isolation 10b

LOCOS, alternative process 1



Device isolation 11 LOCOS, alternative process 2

SWAMI - Side Wall Masked Isolation

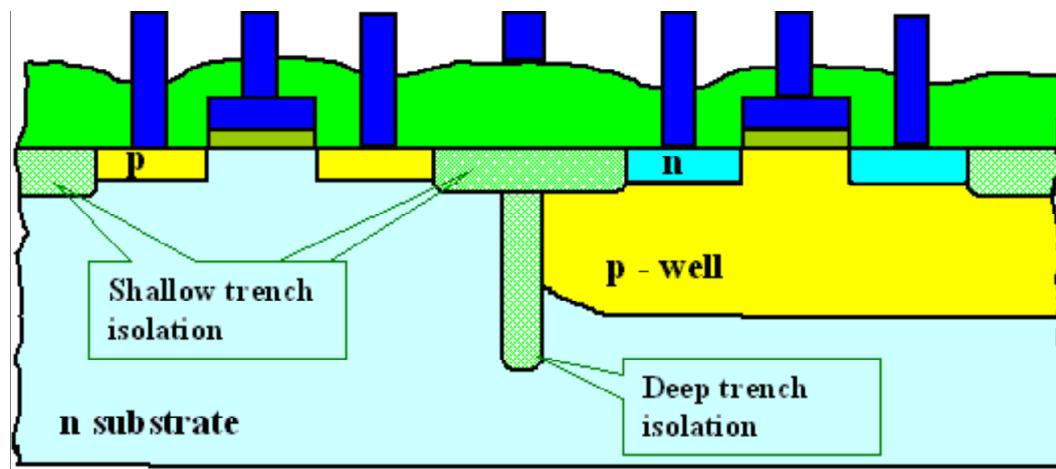


Device isolation 12

Trench Isolation

LOCOS variations not OK above 10^7 trans/cm²

Other approaches; Etch away part of surface and fill it
BOX isolation

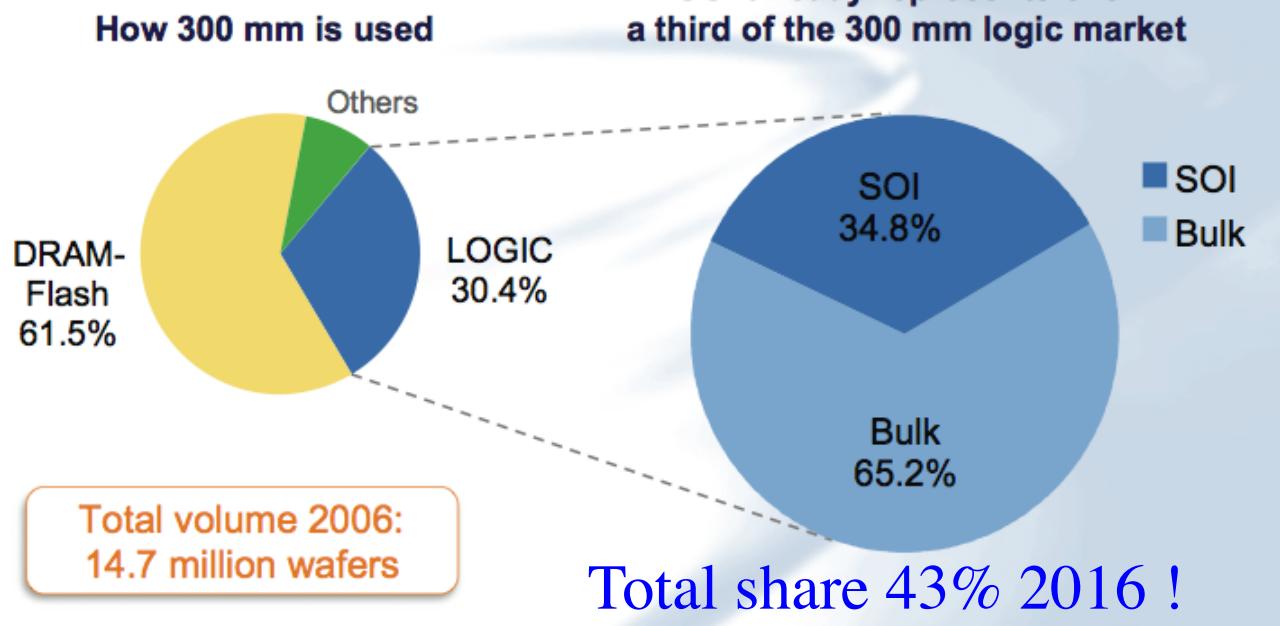


Device isolation 13 SOI

Silicon on Insulators

Isolation etch grooves in top Si, Reduce capacitance to substrate
Ion Impl SOI,
Bonded SoI,
Smart Cut,
PSi jet cut etc..

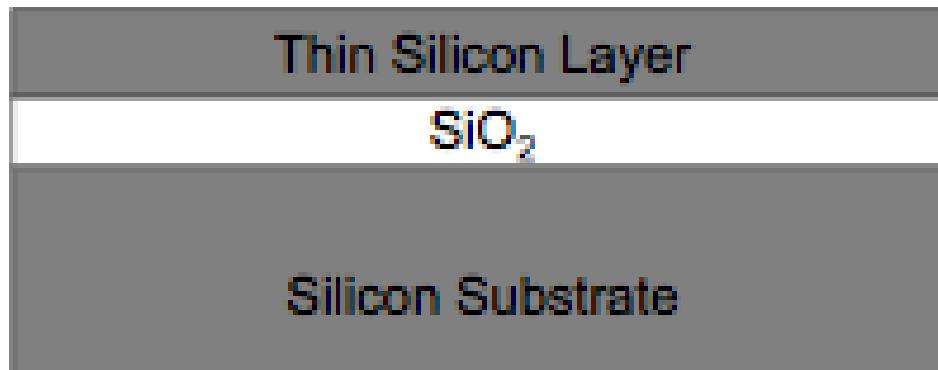
...and a fast growing share of 300mm Logic (in \$ value)



Device isolation 13a

SOI

- ▶ SOI — silicon on insulator, refers to placing a thin layer of silicon on top of an insulator such as SiO_2 .
- ▶ The devices will be built on top of the thin layer of silicon.
- ▶ The basic idea of SOI is to reduced the parasitic capacitance and hence faster switching speed.



Device isolation 13b

SOI

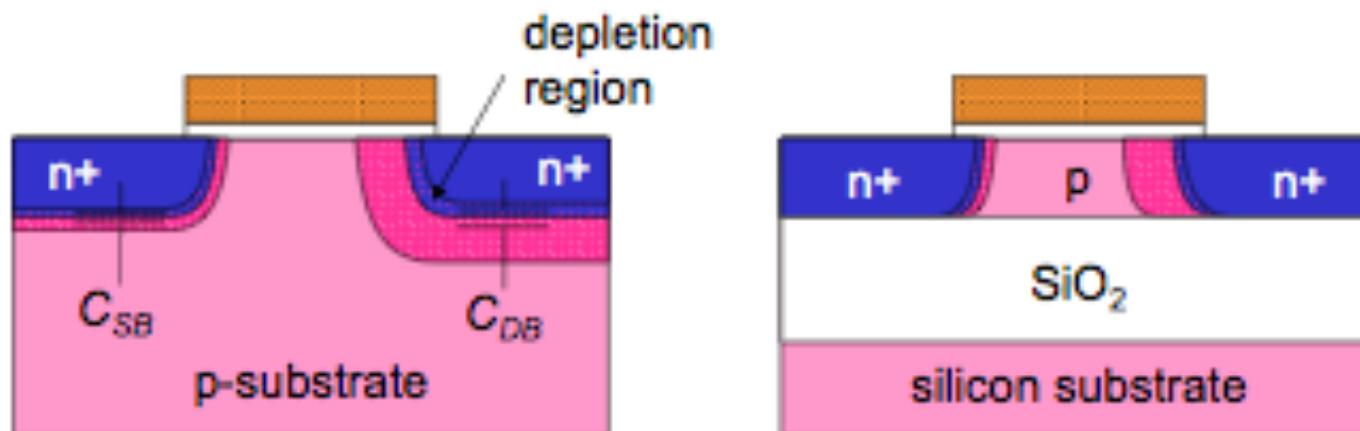
Parasitic Capacitance

- ▶ Every time a transistor is turned on, it must first charge all of its internal (parasitic) capacitance before it can begin to conduct.
- ▶ The time it takes to charge up and discharge (turn off) the parasitic capacitance is much longer than the actual turn on and off of the transistor.
- ▶ If the parasitic capacitance can be reduced, the transistor can be switched faster — performance.
- ▶ One of the major source of parasitic capacitance is from the source and drain to substrate junctions.

Device isolation 13 c SOI

Parasitic Capacitance (cont'd)

- ▶ The ultimate goal is to develop a SOI substrate that can be used as the starting material in mainstream CMOS fabrication technology.
- ▶ SOI can reduce the capacitance at the source and drain junctions significantly — by eliminating the depletion regions extending into the substrate.



Device isolation 13 c SOI

Parasitic Capacitance (cont'd)

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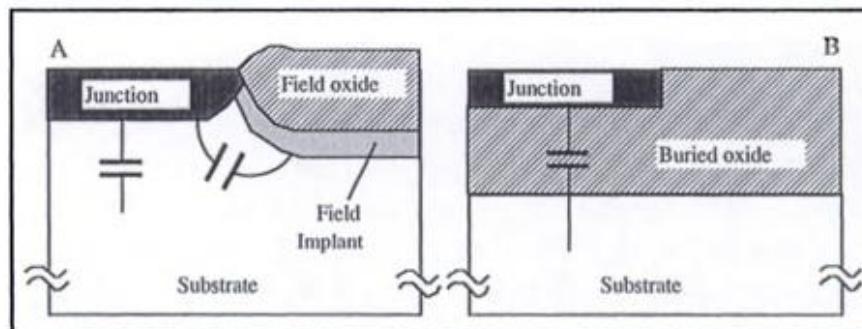
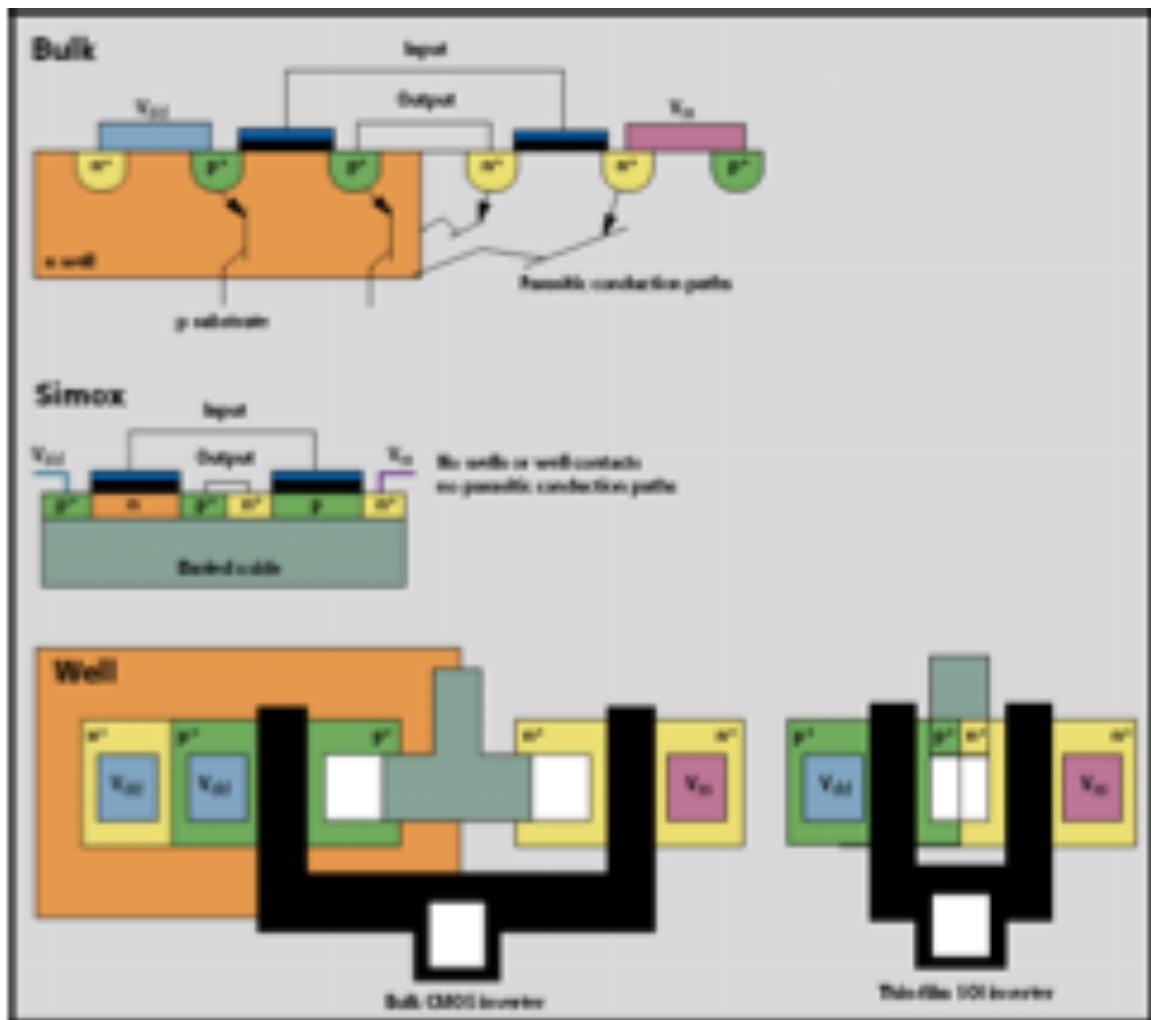


Figure 5-1. Junction capacitances. A: Capacitance between a junction and the substrate and between the junction and the field (channel-stop) implant in a bulk device. B: Capacitance between a junction and the substrate, across the buried oxide, in an SOI device.

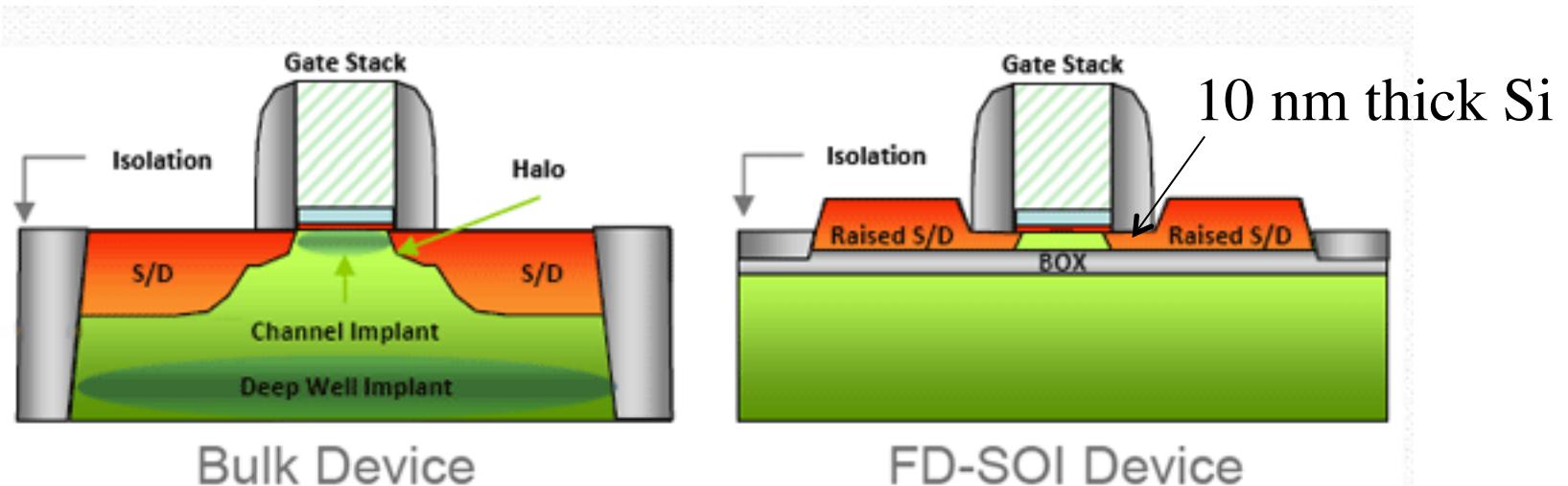
Device isolation 13d SOI

Area Saving

- ▶ Comparing the cross sections of inverters fabricated on bulk silicon and SOI substrates, SOI can eliminate the parasitic bipolar devices and latch-up paths in the substrates and reduce circuit size with its simpler isolation structures.



Device isolation 13di SOI



The fully depleted SOI transistor at 20 nm is significantly simpler than even a simplified version of the bulk CMOS transistor.

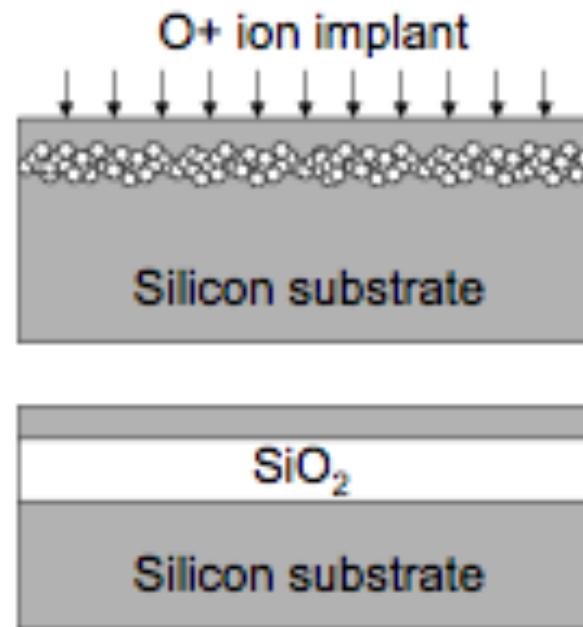
The ARM announcement adds a significant new data point to the debate over the future of process technology at 20 nm and beyond. With FDSOI showing the potential for superior performance, simpler and more robust design, and no need for problematic structures such as finFETs, the weight of the argument for an FDSOI future appears to be growing.

FD-SOI fully depleted s

Device isolation 13e SOI

► SIMOX (Separation by Implantation of Oxygen) uses the following key processes

- ⇒ An oxygen implantation step using a dedicated machine (100mA, 200keV of O⁺ ions) to locate underneath the initial silicon surface a high concentration of oxygen.
- ⇒ A high temperature anneal to regenerate the crystalline quality of the silicon layer remaining over the oxide; this anneal also drives the chemical reaction which forms the stoichiometric oxide buried in the silicon wafer.
- ⇒ A last step should be a touch polishing.



Device isolation 13f

SOI

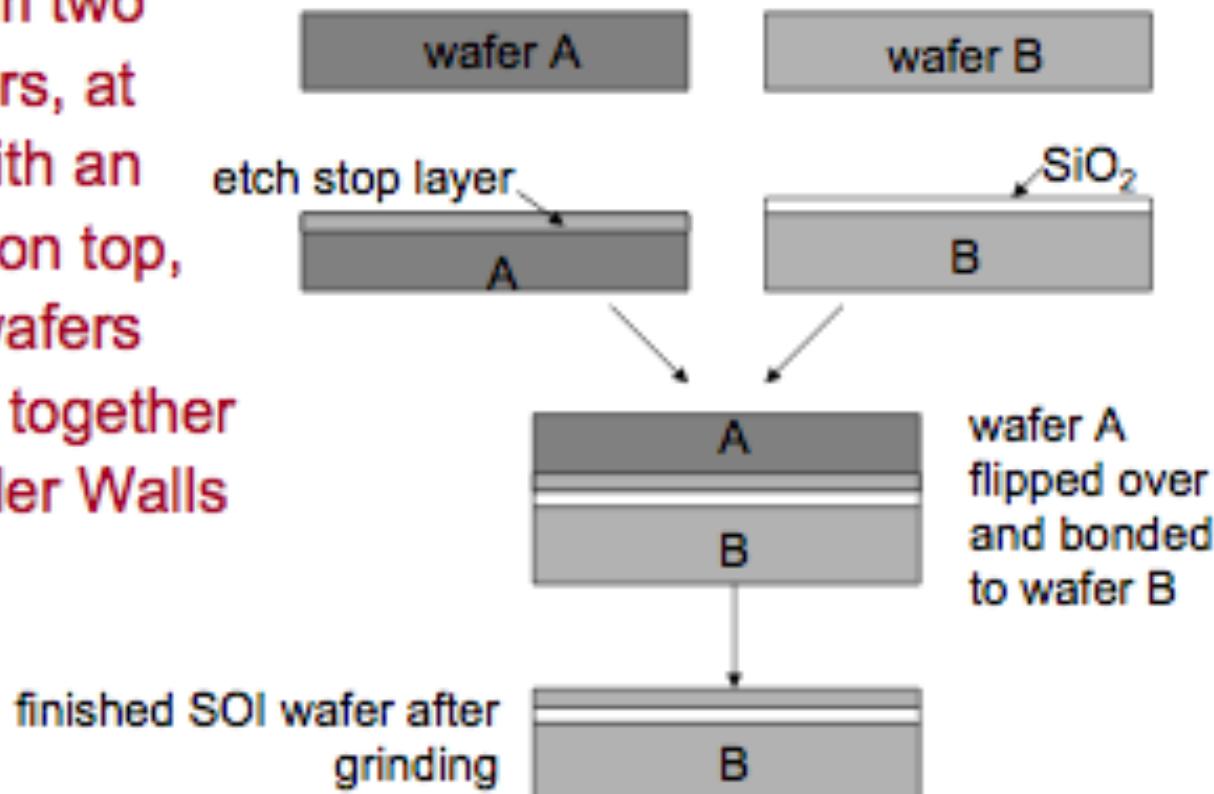
SIMOX (cont'd)

- ▶ The new trend in the SIMOX development is the use of low oxygen implantation doses to obtain a low cost SOI material.
- ▶ This has drastically improved the top silicon film crystalline quality. However the pin-hole defect density of the buried oxide still needs to be improved.
- ▶ The implantation dose is approximately $4 \times 10^{17} \text{ O}^+/\text{cm}^2$ limits the buried oxide thickness to 800-1000Å range.
- ▶ The main disadvantages of the SIMOX technology is the use of non standard equipment and the need of $>1300^\circ\text{C}$ annealing which could be a limitation for 300mm (8") wafer size.

Device isolation 13g SOI

Wafer Bonding

- ▶ Direct wafer bonding is an inexpensive technique for manufacturing thick film of both oxide and silicon.
- ▶ Starting from two silicon wafers, at least one with an oxide layer on top, these two wafers are bonded together using Van der Walls forces.



Wafer Bonding (cont'd)

- ▶ Subsequent annealing increases the mechanical strength of the bonded interface by the chemical reaction which can occur at this interface.
- ▶ One of the substrates is then thinned down to $1\mu\text{m}$ starting from several $100\mu\text{m}$; mechanical grinding and polishing can achieve SOI films of $1\mu\text{m}$ within 10 to 30% uniformity.
- ▶ However, to compete with thin film (e.g. for fully depleted devices), chemical etch stop techniques have been developed.
- ▶ Several etch stops have been reported: Boron doped layer, Si-Ge, carbon implanted, and porous silicon.

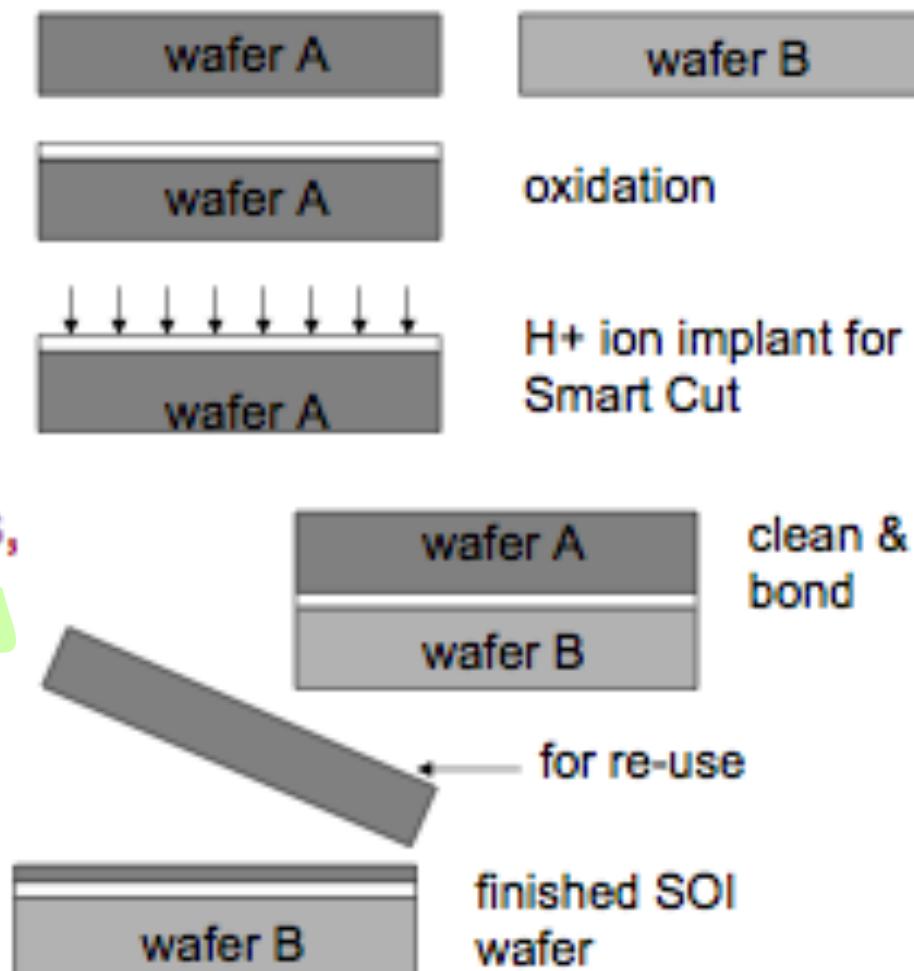
Wafer Bonding (cont'd)

- ▶ However, only a few are compatible with high temperature treatment.
- ▶ The uniformity depends on the selectivity of the last etching which varies from 10 to 10^5 , depending on the etch stop.
- ▶ To avoid the selectivity problem boron doped technique has been used with a localized plasma etch (RIE).
- ▶ Starting from a non-uniform wafer, an accurate measurement of the top silicon film is performed; then a localized plasma etch is used to reduce the variation of the topography.

Device isolation 13 j SOI

Smart Cut

- ▶ The most recent technique is named Smart Cut. This technology is based both on ion implantation and wafer bonding technologies.
- ▶ While the process starts with two wafers, the second wafer is not lost, but recycled to create a second SOI wafer.



Device isolation 13 k SOI

Smart Cut (cont'd)

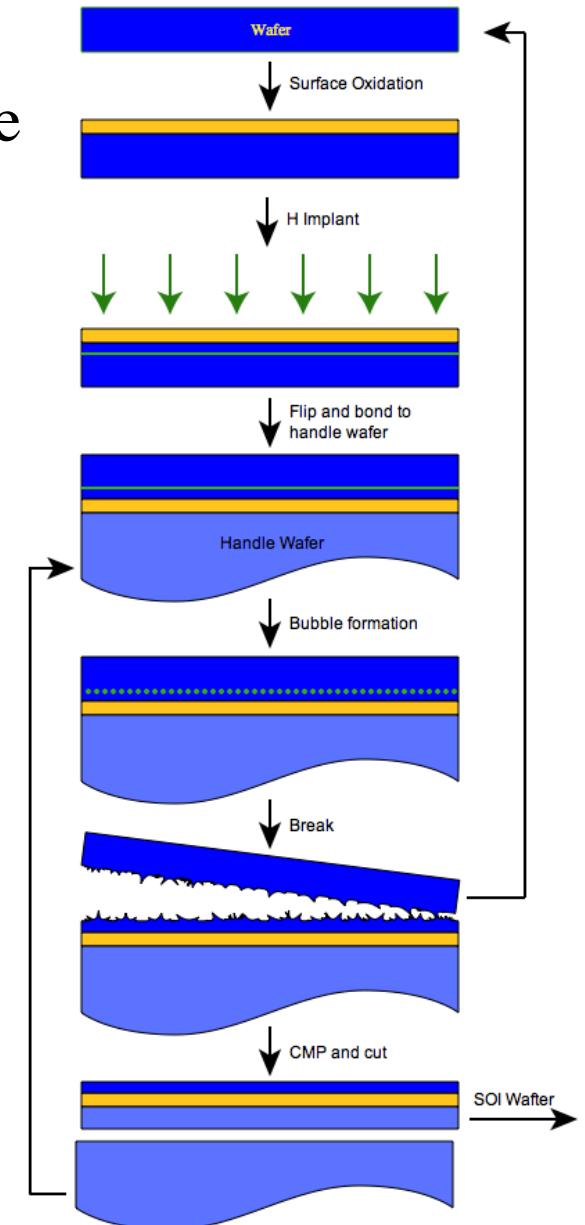
- ▶ The ion implantation step assures uniformity of the SOI film. The bonding steps assures use of a thermally grown buried oxide and the perfect crystalline quality of the top silicon film.
- ▶ Key equipment used to perform the process are a standard high current implanter and a chemical mechanical polisher (CMP).
- ▶ This use of standard equipment is a tremendous advantage to reduce the lead time for capacity increase and to be sure that SOI material will profit from the mainstream improvement to semiconductor manufacturing equipment such as the 300mm wafer.

FYS4310

Smart Cut (cont'd)

Device isolation 13 1 SOI

Wikipedia figure



Device isolation 13 1 SOI

ELTRAN (Canon)

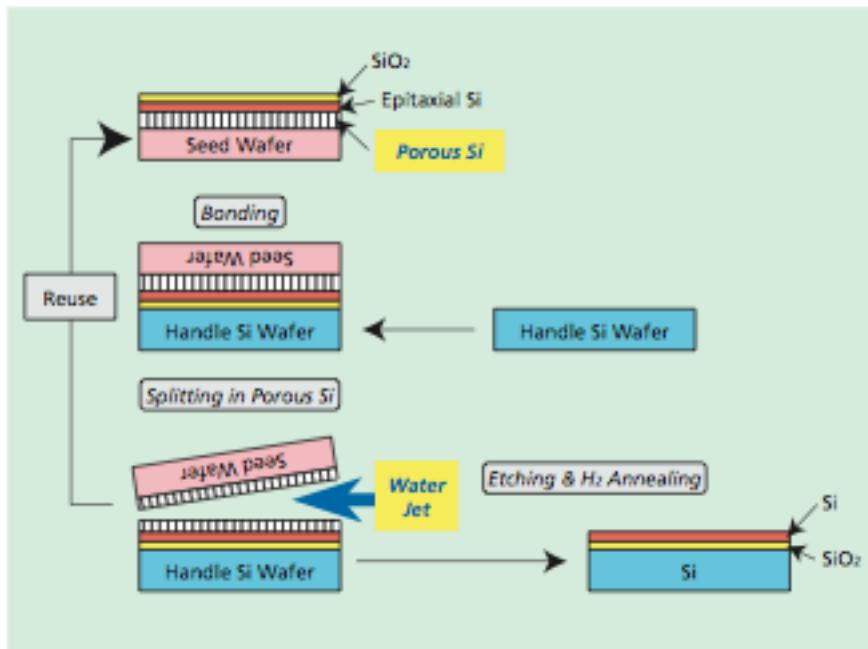


Fig.3 ELTRAN® process flow based on seed wafer reuse.



Figure 3. Ultra Clean Room for ELTRAN manufacturing

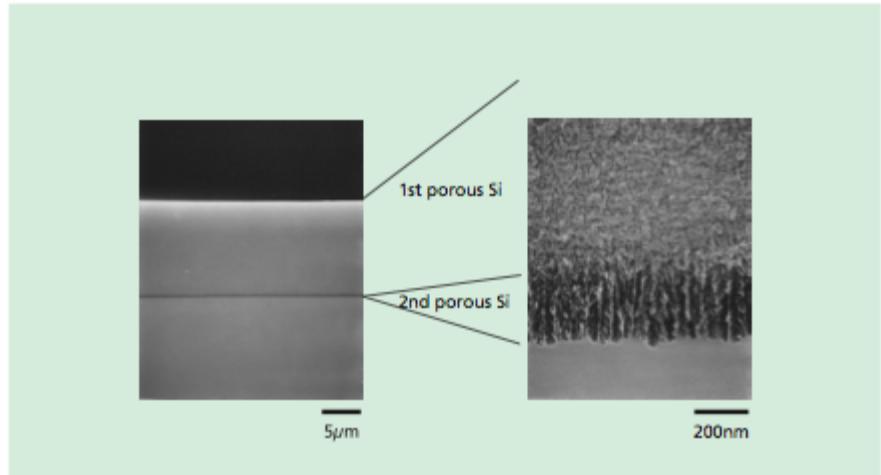
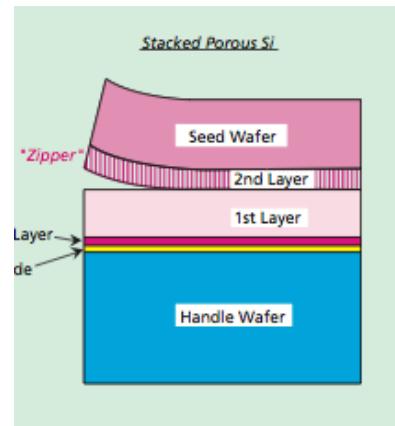


Fig.4 Cross-sectional micrographs of double-layered porous Si formed by changing anodic current.



Fig.11 Side-view photograph during splitting.