

IARPA SuperTools Deliverable

ColdFlux RSFQ Logic Cell Library for MIT-LL SFQ Process

Submitted by

**ColdFlux Team
Stellenbosch University**

Version 3.0

Version History

Version 3.0

This is the version of the cell library for Phase 3 release to the Test & Evaluation teams. The key changes for the RSFQ cell library are as follows:

- Complete migration of schematic/symbol/netlist data from previous Xic formats to the gEDA gschem formats.
- Re-designed cells with PTL interconnects to use $160 \mu\text{A}$ input junctions and $250 \mu\text{A}$ output junctions.
- Updated junction parasitic inductance to use 0.5 pH instead of 0.2 pH .
- Complete re-design of NOT, NOTT and XNOR cells.
- Compacted cell layouts and changed the biasing structure of cells with PTL interconnects to bring in the biasing on M5 at the top and bottom of the cells from external bias lines .

Version 2.1

This is an updated version of the cell library for Phase 2B after taking into account feedback from the Test & Evaluation teams. The key changes for the RSFQ cell library are as follows:

- Minor updates to cell layouts to adhere to latest DRC rules.
- LEF files, extracted using qPALACE, are included in the library.

Version 2.1

This version is the ColdFlux cell library deliverable for SuperTools Phase 2B. The key changes for the RSFQ cell library are as follows:

- RSFQ cells were redesigned from first principles using phase-based equations.
- Cell versions both with and without integrated PTL transmitters and receivers are included in version 2.1.
- Base circuit netlists are included to show how the base cell is designed. An optimized circuit netlist represents the optimized circuit, as extracted from the layout using InductEx.

- A testbench for each cell is included for easy user verification of cell functionality.
- The mesh file is also included in version 2.1 to allow the user to view the 3D layout as generated by TTH/InductEx.
- An XNOR and XNORT cell was developed.
- Additional Always0 (both synchronous and asynchronous) and Always0T cells were developed.
- Parameterized cell layouts are in development, exposing parameters such as inductor widths and track pitch. This allows scaling and regeneration of layouts while maintaining inductance.

Version 2.0

Updated the RSFQ logic cell libraries for SuperTools Phase 2A.

Version 1.1

Previous release of RSFQ Logic cell library document.

Acknowledgment

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1. Introduction and Setup

1.1 Introduction

This RSFQ cell library is developed under the IARPA SuperTools/ColdFlux contract via the U.S. Army Research Office grant W911NF-17-1-0120. The aim is to create a generic and open-source cell library with RSFQ logic [1] as part of the IARPA SuperTools Program [2], [3]. The cell library is continually updated and the latest version of the library can soon be found at: <https://github.com/sunmagnetics/RSFQlib>.

The free and open-source tools *gschem* [4], *JoSIM* [5], [6], *JoSIM-tools* [7], *KLayout* [8] and *TimEx* [9], [10] are used to develop and test the RSFQ cells. The circuit schematics are drawn using *gschem*. *JoSIM* is used as the SPICE engine for simulating the cells, while *JoSIM-tools* is used for operating margin analysis as well as cell parameter optimization. *KLayout* is used to construct the cell layouts. *TimEx* is used to extract the characteristics of the cell to generate the Mealy Finite State Machine diagram and Verilog files. Icarus *Verilog* [11] and *GTKWave* [12] can be used to simulate and view the verilog files for each cell. Additionally, *InductEx* [13], [14] is used for impedance extraction during cell layout design and *InductEx-LVS* is used for Layout Versus Schematic checking. A free version of *InductEx* is available, but has limited capacity.

Version 3.0 of the RSFQ cell library includes two versions of each cell: one with standard connections designed to be connected directly with other cells, and a version designed to be connected to Passive Transmission Lines (PTLs). The version of the cell designed to be connected to PTLs includes integrated PTL transmitter and receiver cells. To indicate the integration of PTL transmitters and receivers within a cell, the letter ‘T’ is added at the end of a cell name, for example the DFF with integrated PTL transmitters and receivers will be referred to as DFFT. The cell library is designed for PTLs with characteristic impedance 5Ω . Version 3.0 of the cell library does not include an XNOR cell with integrated PTL transmitter and receiver.

The following core cells are included in the RSFQ cell library:

- Interconnects: JTL, JTTL, SPLIT, SPLITT, MERGE, MERGET, PTLTX, PTLRX, Always0 (synchronous and asynchronous) and Always0T (synchronous and asynchronous).
- Logic cells: AND2, AND2T, OR2, OR2T, XOR, XORT, NOT, NOTT, XNOR.
- Buffers: DFF, DFFT, NDRO, NDROT, BUFF and BUFFT.
- Interfacing cells: DCSFQ, DCSFQ-PTLTX, PTLRX-SFQDC and SFQDC.

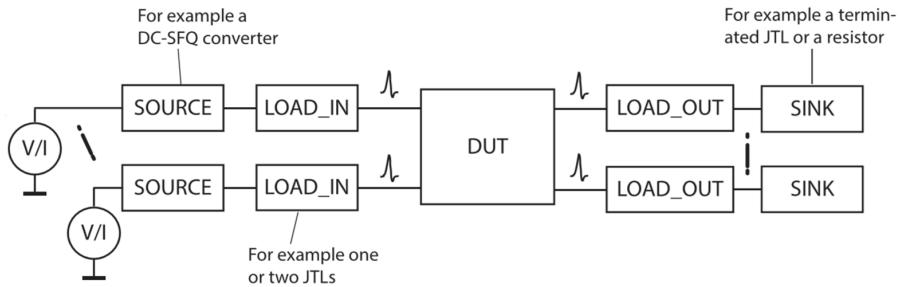


Figure 1.1: Testbench for functionality verification of the RSFQ cell library.

More complex functions can be constructed through connecting several core cells. The cells are currently optimized to run at a maximum clock frequency of 50 GHz.

A testbench for each cell is included within the RSFQ cell library. The testbench circuit is constructed through the circuit in Fig. 1.1 with the DUT representing the device-under-test. The SOURCE cell represents either the DCSFQ or DCSFQ-PTLTX cell, depending on whether a cell with integrated PTL transmitters and receivers are under test. The LOAD_IN and LOAD_OUT cells represent either a JTL or PTL and the SINK cell represents either a resistor or a JTLT terminated through a resistor. The functionality of the DUT is only confirmed if it is able to drive the LOAD_OUT cell (or SINK_OUT cell in the case of PTL cells) successfully. Future versions of the cell library will also require the DUT to drive the LOAD_OUT cell within a specified time. This will constrain the maximum throughput delay of the DUT to minimize timing violations when the cell is used to synthesize larger circuits.

Each delivered cell is documented in 5 parts:

1. **Schematic:** The schematic of a cell is constructed using *gschem* and is delivered in the native circuit schematic format.
2. **Layout:** The physical layout of the cells is constructed using *KLayout* and is delivered in standard GDSII format.
3. **Analog model:**
 - (a) **Netlist:** The netlist presents the device-level construction of a circuit. Each cell is delivered with a “base” and “extracted” circuit netlist files. The base netlist shows how the cell is designed from first principles using phase-based equations. The cells are then optimized before the physical layout is done. The extracted circuit netlists provides the back-annotated optimized netlist extracted through *InductEx*. The extracted netlist is the one included in this document.
 - (b) **Pin list:** The pin labels and function of each pin is listed.
 - (c) **Simulation results:** JoSIM is used for all circuit simulations. The simulation uses the cell testbench to verify cell functionality.
4. **Digital model:**

- (a) **Verilog model:** The behavior-level model of a cell with timing specifications included within the model. The verilog models are delivered in two parts – a basic verilog model accompanied by a SDF file to include timing delays, and a self-contained verilog model which contains the timing delays of the cell within the verilog model itself. All verilog models are extracted using *TimEx* and is delivered in standard HDL Verilog format. The verilog model included within this document is the self-contained verilog model.
- (b) **Simulation results:** The digital simulation testbench is generated through *TimEx* and is run using *Icarus Verilog* and wave viewer *GTKWave*. Each edge event indicates an SFQ pulse.
- (c) **Mealy finite state machine diagram:** The state machine diagram is extracted using *TimEx* and is delivered in standard PDF format.
5. **Power consumption:** The power consumption of each cell is calculated in terms of static and dynamic power consumption. As a rough estimate, it is assumed that each junction switches with every clock signal. For asynchronous cells, the power consumption is calculated through assuming that an input pulse train is applied at the same frequency as the specified clock frequency. Following [15], dynamic power consumption can be calculated as $P_d = f\Phi_0 I_c$ and static power consumption can be calculated as $P_s = I_b V_b$.

1.2 Setup

The latest version of the RSFQ cell library can be found at: <https://github.com/sunmagnetics/RSFQlib>. The RSFQ cell library is simulated and tested using several free and/or open-source tools:

- *gschem* is part of the *gEDA* project and can be found at <http://www.geda-project.org/>.
- *JoSIM* can be found at <https://github.com/JoeyDelp/JoSIM/>.
- *JoSIM-tools* can be found at <https://github.com/pleroux0/josim-tools>.
- *TimEx* can be found at <https://github.com/sunmagnetics/TimEx>.
- *KLayout* can be found at <https://www.klayout.de/>.
- *InductEx* can be found at <https://www.inductex.info>. *InductEx-LVS* is included with *InductEx*.
- *Icarus Verilog* can be found at <http://iverilog.icarus.com/>.
- *GTKWave* can be found at <http://gtkwave.sourceforge.net/>.

No additional setup is required to use the RSFQ cell library.

1.3 License

The generic RSFQ cell library is free to distribute and/or modify under the terms of the MIT license.

2. RSFQ Cell Library: Standard Connections

2.1 Interconnects

2.1.1 JTL

The JTL, Josephson transmission line, cell is commonly used to re-establish and propagate SFQ pulses. The cell is not designed to be directly connected to a PTL.

Schematic

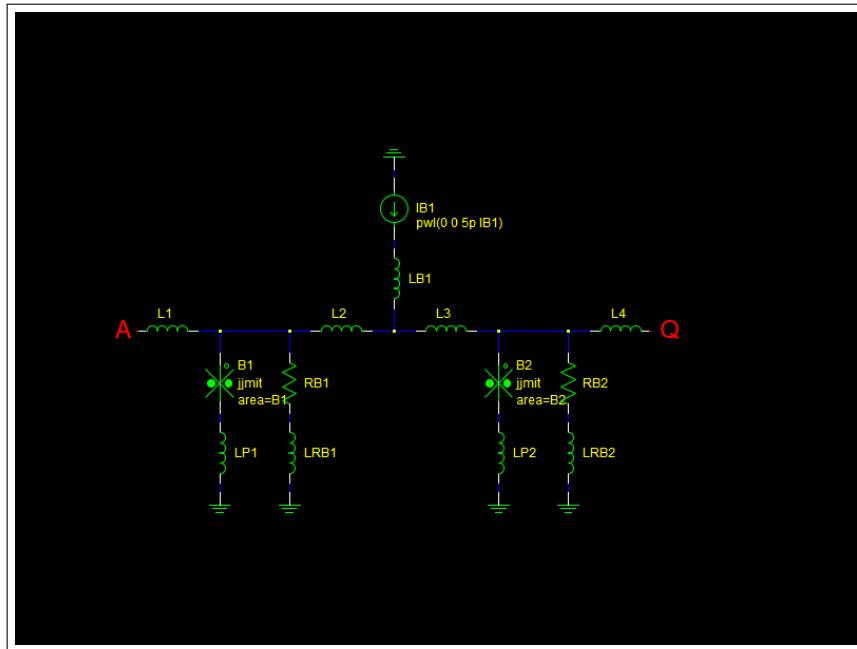


Figure 2.1: Schematic of RSFQ JTL.

Layout

The physical layout of the RSFQ JTL is shown in Fig. 2.2. The layout height is $70 \mu\text{m}$ and the width is $20 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. A bias pillar from M0 to M6 connects the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

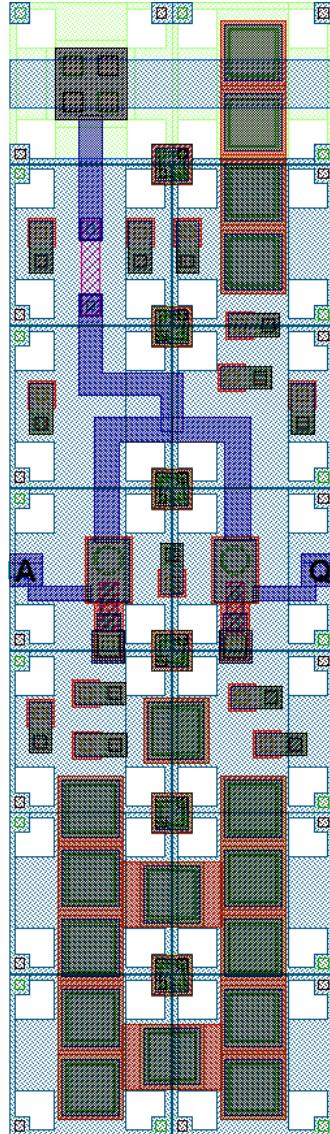


Figure 2.2: RSFQ JTL Layout

Analog model

```

1 * Back-annotated simulation file written by InductEx v.6.1.52 on 2022/07/25.
2 * Author: L. Schindler
3 * Version: 3.0
4 * Last modification date: 21 July 2022
5 * Last modification by: T. Hall
6
7 *$Ports      a      q
8 .subckt THmitll_JTL a q
9 .model jjmit jj(rtype=1, vg=2.8mV, cap=0.07pF, r0=160, rn=16, icrit=0.1mA)
10 .param Phi0=2.067833848E-15
11 .param B0=1
12 .param Ic0=0.0001
13 .param IcRs=100u*6.859904418
14 .param B0Rs=IcRs/Ic0*B0
15 .param Rsheet=2
16 .param Lsheet=1.13e-12
17 .param LP=0.5p
18 .param IC=2.5
19 .param LB=2p
20 .param BiasCoef=0.7
21
22 .param B1=IC
23 .param B2=IC
24
25 .param IB1=(B1+B2)*Ic0*BiasCoef
26
27 .param LB1=LB
28
29 .param L1=Phi0/(4*B1*Ic0)
30 .param L2=Phi0/(4*B1*Ic0)
31 .param L3=Phi0/(4*B2*Ic0)
32 .param L4=Phi0/(4*B2*Ic0)
33
34 .param LP1=LP
35 .param LP2=LP
36
37 .param RB1=B0Rs/B1
38 .param RB2=B0Rs/B2
39
40 .param LRB1=(RB1/Rsheet)*Lsheet+LP
41 .param LRB2=(RB2/Rsheet)*Lsheet+LP
42
43 B1 1 2 jjmit area=B1
44 B2 5 6 jjmit area=B2
45
46 IB1 0 4 pwl(0 0 5p IB1)
47
48 LB1 4 3 2.336E-012
49
50 L1 a 1 2.07E-012
51 L2 1 3 2.088E-012
52 L3 3 5 2.082E-012
53 L4 5 q 2.072E-012
54
55 LP1 2 0 3.137E-013
56 LP2 6 0 3.123E-013
57
58 RB1 1 101 RB1
59 LRB1 101 0 LRB1
60 RB2 5 105 RB2
61 LRB2 105 0 LRB2
62 .ends

```

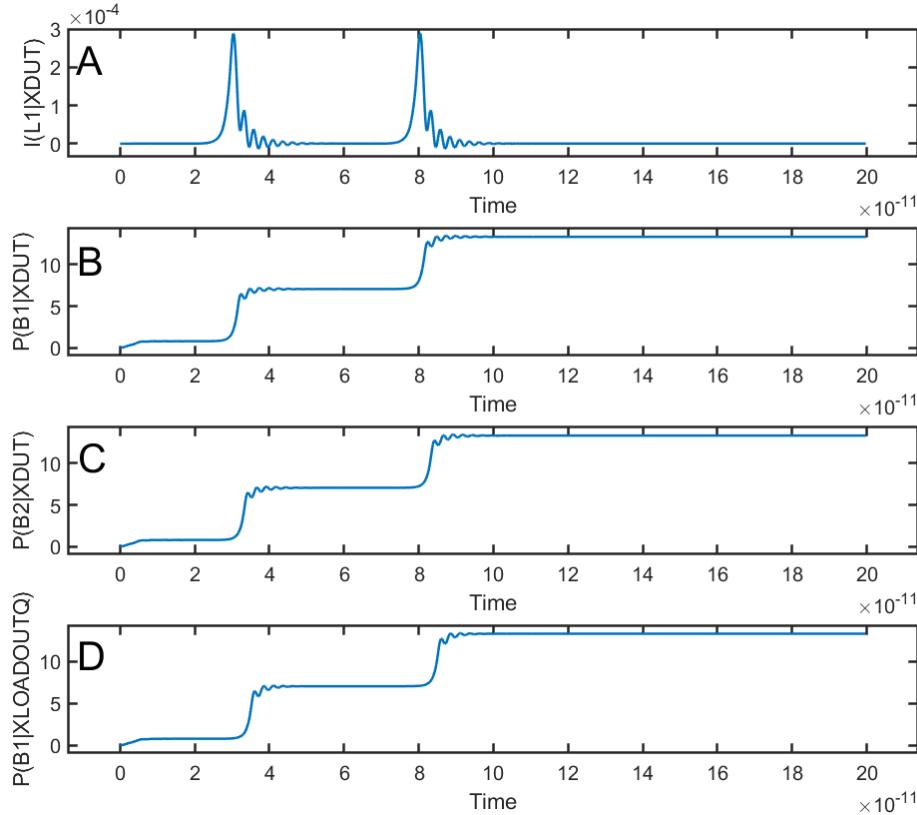
Listing 2.1: RSFQ JTL JoSIM netlist.

Table 2.1: RSFQ JTL pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ JTL using JoSIM is shown in Fig. 2.3. The testbench is included within the cell library for user verification. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit.

**Figure 2.3:** RSFQ JTL analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 25 July 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_JTL_v3p0_extracted (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 3.5,
21   ct_state0_a_a = 5.2;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q = 0; // All outputs start at 0
35 end
36
37 always @(posedge a or negedge a) // execute at positive and negative edges of input
38 begin
39   if ($time>4) // arbitrary steady-state time)
40     begin
41       if (errorsignal_a == 1'b1) // A critical timing is active for this input
42         begin
43           outfile = $fopen("errors.txt", "a");
44           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
45           ↪ ", $stime);
46           $fclose(outfile);
47           q <= 1'bX; // Set all outputs to unknown
48         end
49       if (errorsignal_a == 0)
50         begin
51           case (cell_state)
52             0: begin
53               q <= #(delay_state0_a_q) !q;
54               errorsignal_a = 1; // Critical timing on this input; assign
55               ↪ immediately
56               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
57               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 2.2: RSFQ JTL verilog model with self-contained timing.

The digital simulation results for the RSFQ JTL is shown in Fig. 2.4 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 2.5.

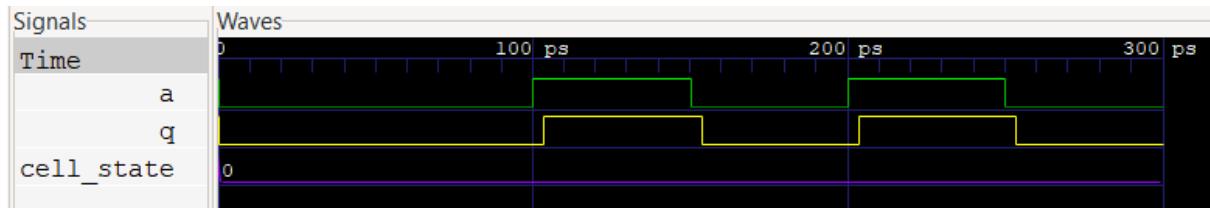


Figure 2.4: RSFQ JTL digital simulation results.

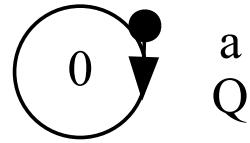


Figure 2.5: RSFQ JTL Mealy finite state machine diagram.

Power Consumption

Table 2.2: RSFQ JTL power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	910	1.03
2	910	2.07
5	910	5.17
10	910	10.3
20	910	20.7
50	910	51.7

2.1.2 SPLIT

The SPLIT cell is used to split a single pulse signal line into two duplicate output pulse signal lines. The cell is not designed to be directly connected to a PTL.

Schematic

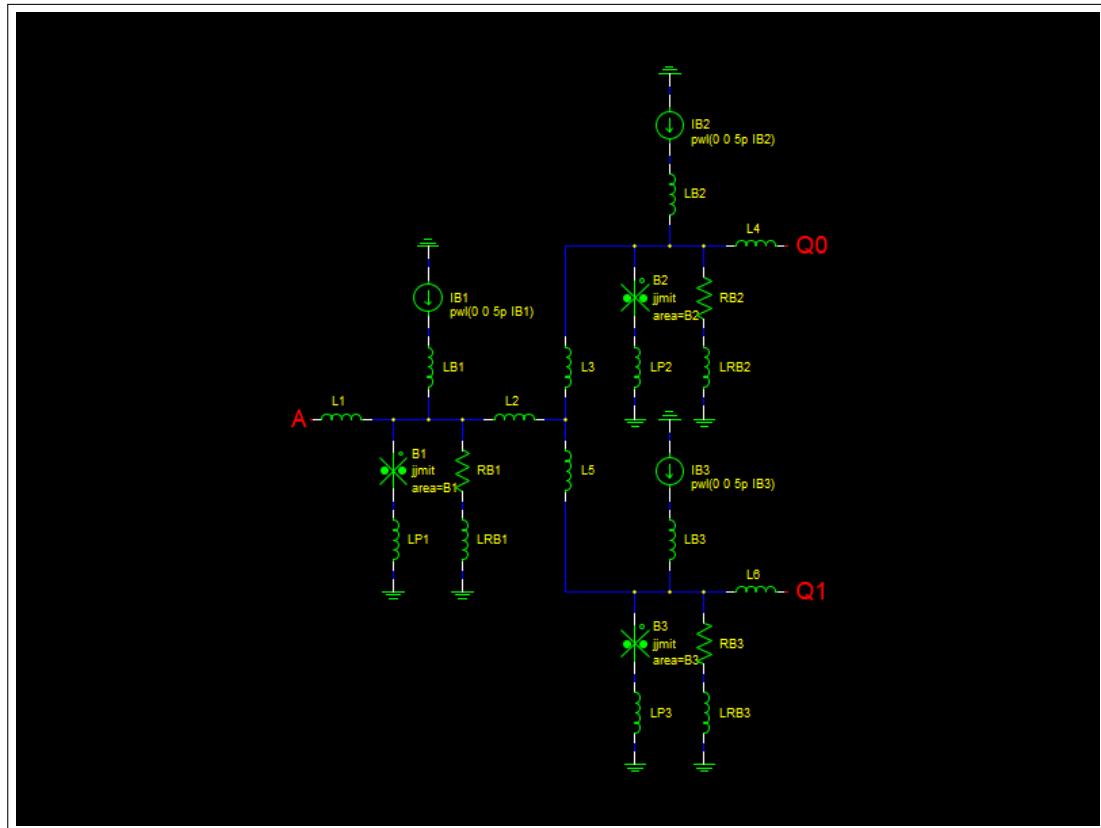


Figure 2.6: Schematic of RSFQ SPLIT.

Layout

The physical layout of the RSFQ SPLIT is shown in Fig. 2.7. The layout height is $70 \mu\text{m}$ and the width is $20 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

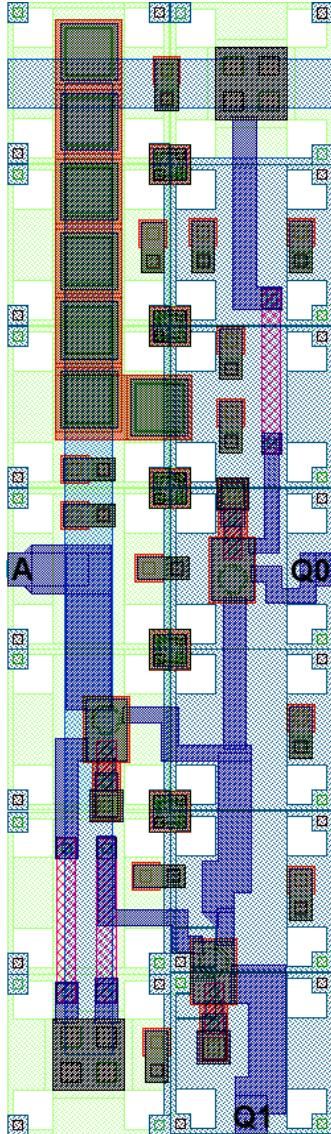


Figure 2.7: RSFQ SPLIT layout.

Analog model

```

1  * Back-annotated simulation file written      42 | .param LP2=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/07/25.    43 | .param LP3=LP
3  * Author: L. Schindler                      44 |
4  * Version: 3.0                                45 | .param RB1=B0Rs/B1
5  * Last modification date: 25 July 2022       46 | .param RB2=B0Rs/B2
6  * Last modification by: T. Hall              47 | .param RB3=B0Rs/B3
7  *$Ports a          q0          q1           48 |
8 .subckt THmitll_SPLIT a q0 q1               49 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
9 .model jjmit jj(rtype=1, vg=2.8mV, cap     50 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
10    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    51 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
11    ↪ )                                         52 |
12 .param Phi0=2.067833848E-15                 53 | B1 1 2 jjmit area=B1
13 .param B0=1                                    54 | B2 5 6 jjmit area=B2
14 .param Ic0=0.0001                            55 | B3 8 9 jjmit area=B3
15 .param IcRs=100u*6.859904418                  56 |
16 .param B0Rs=IcRs/Ic0*B0                     57 | IB1 0 3 pwl(0 0 5p IB1)
17 .param Rsheet=2                             58 | IB2 0 7 pwl(0 0 5p IB2)
18 .param Lsheet=1.13e-12                      59 | IB3 0 10 pwl(0 0 5p IB3)
19 .param LP=0.5p                               60 |
20 .param IC=2.5                                61 | LB1 3 1 1.712E-012
21 .param LB=2p                                 62 | LB2 7 5 2.279E-012
22 .param BiasCoef=0.7                         63 | LB3 10 8 2.858E-012
23 .param B1=IC                                 64 |
24 .param B2=IC                                 65 | L1 a 1 2.062E-012
25 .param B3=IC                                 66 | L2 1 4 2.06E-012
26 .param IB1=BiasCoef*Ic0*B1                 67 | L3 5 4 2.079E-012
27 .param IB2=BiasCoef*Ic0*B2                 68 | L4 5 q0 2.081E-012
28 .param IB3=IB2                             69 | L5 4 8 2.076E-012
29 .param LB1=LB                               70 | L6 8 q1 2.086E-012
30 .param LB2=LB                               71 |
31 .param LB3=LB                               72 | LP1 2 0 4.263E-013
32 .param L1=Phi0/(4*IC*Ic0)                   73 | LP2 6 0 3.75E-013
33 .param L2=(Phi0/(2*B1*Ic0))/2             74 | LP3 9 0 4.312E-013
34 .param L3=L2                                75 |
35 .param L4=Phi0/(4*IC*Ic0)                   76 | RB1 1 101 RB1
36 .param L5=L3                                77 | LRB1 101 0 LRB1
37 .param L6=L4                                78 | RB2 5 105 RB2
38 .param LP1=LP                               79 | LRB2 105 0 LRB2
39 .param LP=LP                                 80 | RB3 8 108 RB3
40 .param LP2=LP                               81 | LRB3 108 0 LRB3
41 .param LP3=LP                               82 | .ends

```

Listing 2.3: RSFQ SPLIT JoSIM netlist.

Table 2.3: RSFQ SPLIT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ SPLIT are shown in Fig. 2.8. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q0**,
- (d) the phase over the output JJ of pin **q1**,
- (e) the phase over the input JJ of the load cell connected to pin **q0**, and
- (f) the phase over the input JJ of the load cell connected to pin **q1**.

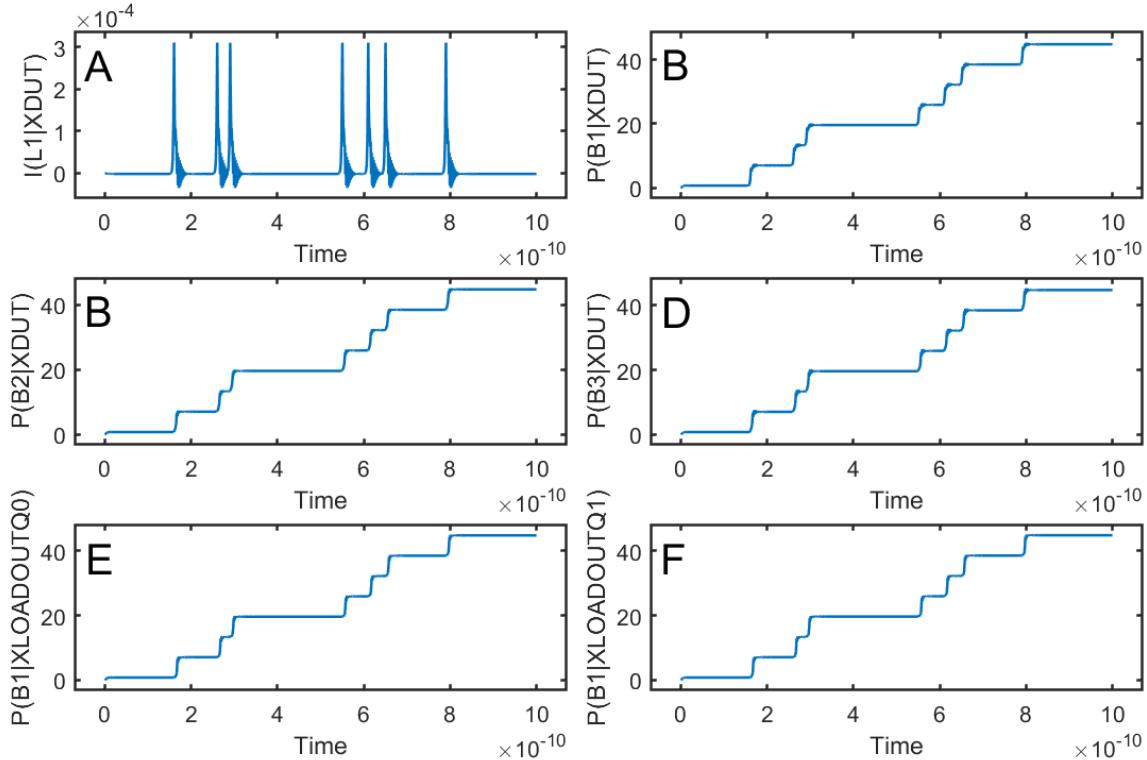


Figure 2.8: RSFQ SPLIT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 25 July 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_SPLIT_v3p0_extracted (a, q0, q1);
9
10 input
11   a;
12
13 output
14   q0, q1;
15
16 reg
17   q0, q1;
18
19 real
20   delay_state0_a_q0 = 6.3,
21   delay_state0_a_q1 = 6.3,
22   ct_state0_a_a = 7.0;
23
24 reg
25   errorsignal_a;
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q0 = 0; // All outputs start at 0
35   q1 = 0; // All outputs start at 0
36 end
37
38 always @(posedge a or negedge a) // execute at positive and negative edges of input
39 begin
40   if ($time>4) // arbitrary steady-state time)
41     begin
42       if (errorsignal_a == 1'b1) // A critical timing is active for this input
43         begin
44           outfile = $fopen("errors.txt", "a");
45           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
46           ↪ ", $stime);
47           $fclose(outfile);
48           q0 <= 1'bX; // Set all outputs to unknown
49           q1 <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q0 <= #(delay_state0_a_q0) !q0;
56               q1 <= #(delay_state0_a_q1) !q1;
57               errorsignal_a = 1; // Critical timing on this input; assign
               ↪ immediately
               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 2.4: RSFQ SPLIT verilog model.

The digital simulation results for the RSFQ SPLIT is shown in Fig. 2.9 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.10.

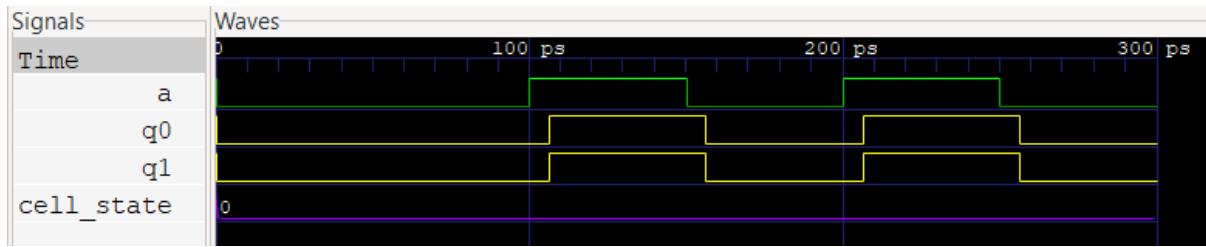


Figure 2.9: RSFQ SPLIT digital simulation results.

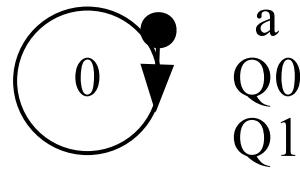


Figure 2.10: RSFQ SPLIT Mealy finite state diagram.

Power consumption

Table 2.4: RSFQ SPLIT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1370	1.55
2	1370	3.10
5	1370	7.75
10	1370	15.5
20	1370	31.0
50	1370	77.5

2.1.3 MERGE

The MERGE joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input line, the MERGE will generate a pulse on the output signal line. The cell is not designed to be directly connected to a PTL.

Schematic

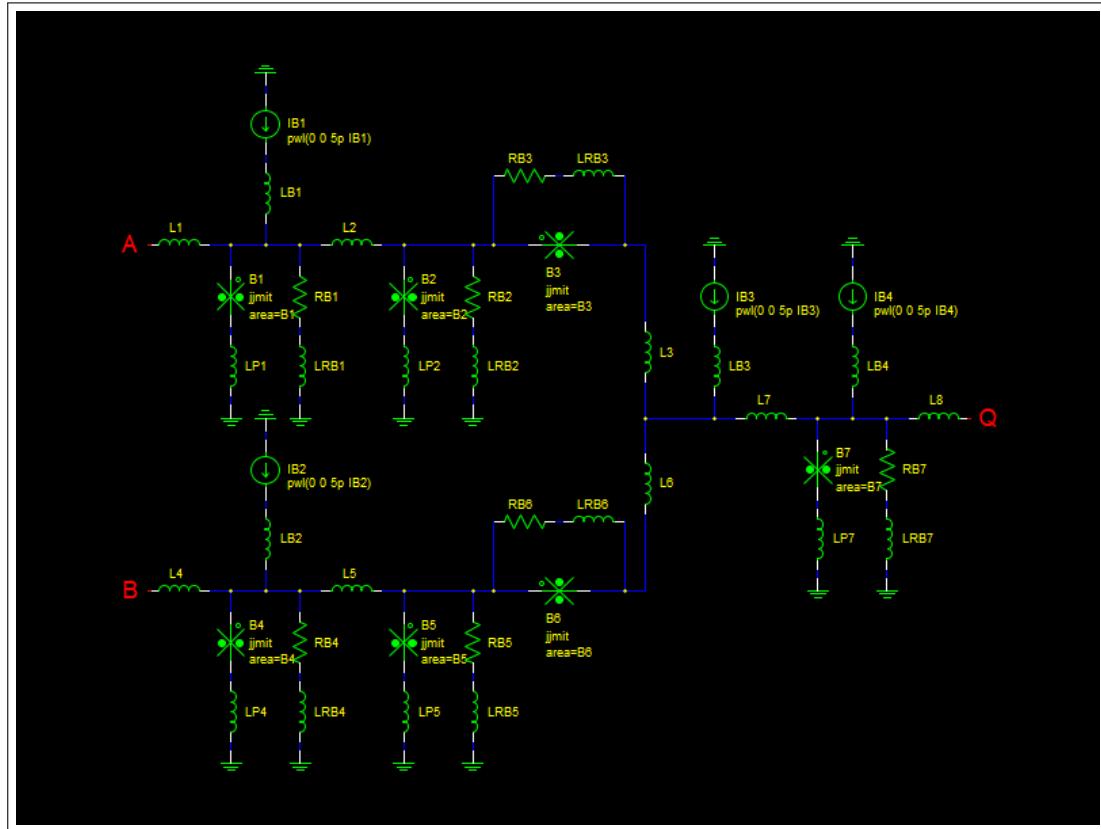


Figure 2.11: Schematic of RSFQ MERGE.

Layout

The physical layout of the RSFQ MERGE is shown in Fig. 2.12. The height of the layout is $70 \mu m$ and the width is $30 \mu m$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

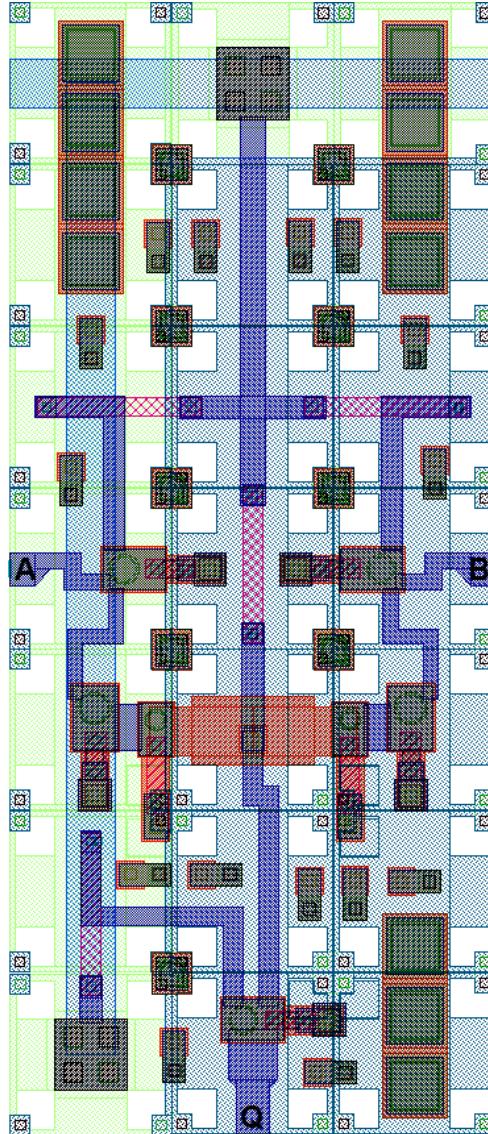


Figure 2.12: RSFQ MERGE layout.

Analog model

```

1  * Back-annotated simulation file written      60  .param RB6=B0Rs/B6
2   ↪ by InductEx v.6.1.52 on 2022/07/29.      61  .param RB7=B0Rs/B7
3  * Author: L. Schindler                      62
4  * Version: 3.0                               63  .param LRB1=(RB1/Rsheet)*Lsheet+LP
5  * Last modification date: 29 July 2022       64  .param LRB2=(RB2/Rsheet)*Lsheet+LP
6  * Last modification by: T. Hall             65  .param LRB3=(RB3/Rsheet)*Lsheet
7  *$Ports a         b         q               66  .param LRB4=(RB4/Rsheet)*Lsheet+LP
8  .subckt THmitll_MERGE a b q               67  .param LRB5=(RB5/Rsheet)*Lsheet+LP
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    68  .param LRB6=(RB6/Rsheet)*Lsheet
10  ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     69  .param LRB7=(RB7/Rsheet)*Lsheet+LP
11  ↪ )
12  .param Phi0=2.067833848E-15                 70
13  .param B0=1                                 71  B1 1 2 jjmit area=B1
14  .param Ic0=0.0001                           72  B2 4 5 jjmit area=B2
15  .param IcRs=100u*6.859904418                73  B3 4 6 jjmit area=B3
16  .param B0Rs=IcRs/Ic0*B0                     74  B4 8 9 jjmit area=B4
17  .param Rsheet=2                            75  B5 11 12 jjmit area=B5
18  .param Lsheet=1.13e-12                      76  B6 11 13 jjmit area=B6
19  .param LP=0.5p                             77  B7 15 16 jjmit area=B7
20  .param IC=2.5                             78
21  .param LB=2p                             79  IB1 0 3 pwl(0 0 5p IB1)
22  .param BiasCoef=0.7'                      80  IB2 0 10 pwl(0 0 5p IB2)
23  .param B1=2.5                            81  IB3 0 14 pwl(0 0 5p IB3)
24  .param B2=3.01                           82  IB4 0 17 pwl(0 0 5p IB4)
25  .param B3=1.18                           83
26  .param B4=2.5                            84  LB1 3 1 LB1
27  .param B5=3.01                           85  LB2 10 8 LB2
28  .param B6=1.18                           86  LB3 14 7 LB3
29  .param B7=2.5                            87  LB4 17 15 LB4
30  .param IB1=175u                           88
31  .param IB2=175u                           89  L1 a 1 2.048E-012
32  .param IB3=183u                           90  L2 1 4 2.485E-012
33  .param IB4=175u                           91  L3 6 7 9.486E-013
34                                         92  L4 b 8 2.059E-012
35  .param L1=2.0465p                         93  L5 8 11 2.473E-012
36  .param L2=2.4953p                         94  L6 7 13 9.53E-013
37  .param L3=0.9488p                         95  L7 7 15 3.697E-012
38  .param L4=2.0465p                         96  L8 15 q 1.377E-012
39  .param L5=2.4953p                         97
40  .param L6=0.9488p                         98  LP1 2 0 4.88E-013
41  .param L7=3.6821p                         99  LP2 5 0 3.854E-013
42  .param L8=1.3761p                         100 LP4 9 0 4.857E-013
43                                         101 LP5 12 0 3.834E-013
44  .param LB1=LB                            102 LP7 16 0 3.61E-013
45  .param LB2=LB                            103
46  .param LB3=LB                            104 RB1 1 101 RB1
47  .param LB4=LB                            105 LRB1 101 0 LRB1
48                                         106 RB2 4 104 RB2
49  .param LP1=LP                            107 LRB2 104 0 LRB2
50  .param LP2=LP                            108 RB3 4 106 RB3
51  .param LP4=LP                            109 LRB3 106 6 LRB3
52  .param LP5=LP                            110 RB4 8 108 RB4
53  .param LP7=LP                            111 LRB4 108 0 LRB4
54                                         112 RB5 11 111 RB5
55  .param RB1=B0Rs/B1                      113 LRB5 111 0 LRB5
56  .param RB2=B0Rs/B2                      114 RB6 11 113 RB6
57  .param RB3=B0Rs/B3                      115 LRB6 113 13 LRB6
58  .param RB4=B0Rs/B4                      116 RB7 15 115 RB7
59  .param RB5=B0Rs/B5                      117 LRB7 115 0 LRB7
60                                         118 .ends

```

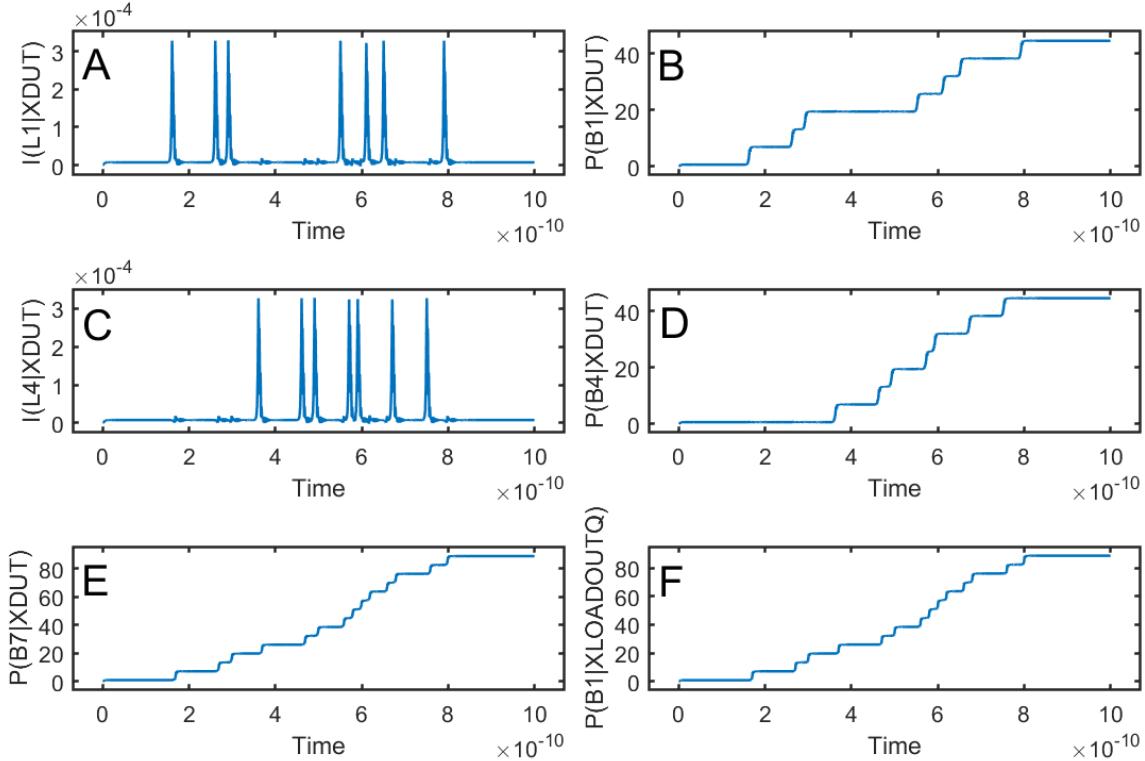
Listing 2.5: RSFQ MERGE JoSIM netlist.

Table 2.5: RSFQ MERGE pin list.

Pin	Description
a	Data input
b	Data input
q	Data output

The JoSIM simulation results for the RSFQ MERGE are shown in Fig. 2.13. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load cell connected to pin **q**.

**Figure 2.13:** RSFQ MERGE analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 29 July 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_MERGE_v3p0_extracted (a, b, q);
9
10 input
11   a, b;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 9.0,
21   delay_state0_b_q = 9.0,
22   ct_state0_a_a = 10.2,
23   ct_state0_a_b = 2.3,
24   ct_state0_b_a = 2.2,
25   ct_state0_b_b = 10.2;
26
27 reg
28   errorsignal_a,
29   errorsignal_b;
30
31 integer
32   outfile,
33   cell_state; // internal state of the cell
34
35 initial
36 begin
37   errorsignal_a = 0;
38   errorsignal_b = 0;
39   cell_state = 0; // Startup state
40   q = 0; // All outputs start at 0
41 end
42
43 always @(posedge a or negedge a) // execute at positive and negative edges of input
44 begin
45   if ($time>4) // arbitrary steady-state time)
46     begin
47       if (errorsignal_a == 1'b1) // A critical timing is active for this input
48         begin
49           outfile = $fopen("errors.txt", "a");
50           $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
51           ↪ ", $stime);
52           $fclose(outfile);
53           q <= 1'bX; // Set all outputs to unknown
54         end
55       if (errorsignal_a == 0)
56         begin
57           case (cell_state)
58             0: begin
59               q <= #(delay_state0_a_q) !q;
60               errorsignal_a = 1; // Critical timing on this input; assign
61               ↪ immediately
62               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
63               ↪ after critical timing expires
64               errorsignal_b = 1; // Critical timing on this input; assign
65               ↪ immediately
66               errorsignal_b <= #(ct_state0_a_b) 0; // Clear error signal
67               ↪ after critical timing expires

```

```

63           end
64       endcase
65     end
66   end
67 end
68
69 always @(posedge b or negedge b) // execute at positive and negative edges of input
70 begin
71   if ($time>4) // arbitrary steady-state time)
72 begin
73   if (errorsignal_b == 1'b1) // A critical timing is active for this input
74 begin
75     outfile = $fopen("errors.txt", "a");
76     $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
77     ↪ ", $stime);
78     $fclose(outfile);
79     q <= 1'bX; // Set all outputs to unknown
80   end
81   if (errorsignal_b == 0)
82 begin
83     case (cell_state)
84     0: begin
85       q <= #(delay_state0_b_q) !q;
86       errorsignal_a = 1; // Critical timing on this input; assign
87       ↪ immediately
88       errorsignal_a <= #(ct_state0_b_a) 0; // Clear error signal
89       ↪ after critical timing expires
90       errorsignal_b = 1; // Critical timing on this input; assign
91       ↪ immediately
92       errorsignal_b <= #(ct_state0_b_b) 0; // Clear error signal
93       ↪ after critical timing expires
94     end
95   endcase
96 end
97 end
98
99 endmodule

```

Listing 2.6: RSFQ MERGE verilog model.

The digital simulation results for the RSFQ MERGE is shown in Fig. 2.14 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.15.

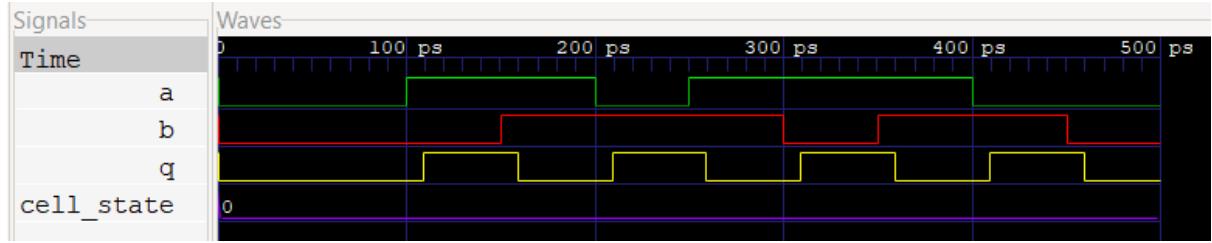


Figure 2.14: RSFQ MERGE digital simulation results.

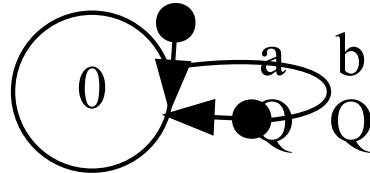


Figure 2.15: RSFQ MERGE Mealy finite state diagram.

Power consumption

Table 2.6: RSFQ MERGE power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1840	3.28
2	1840	6.57
5	1840	16.4
10	1840	32.8
20	1840	65.7
50	1840	164

2.1.4 PTLTX

The RSFQ PTLTX is a cell which transmits a pulse signal over a PTL. It is connected to a cell which is not designed to connect to PTLs, if a PTL connection is required.

Schematic

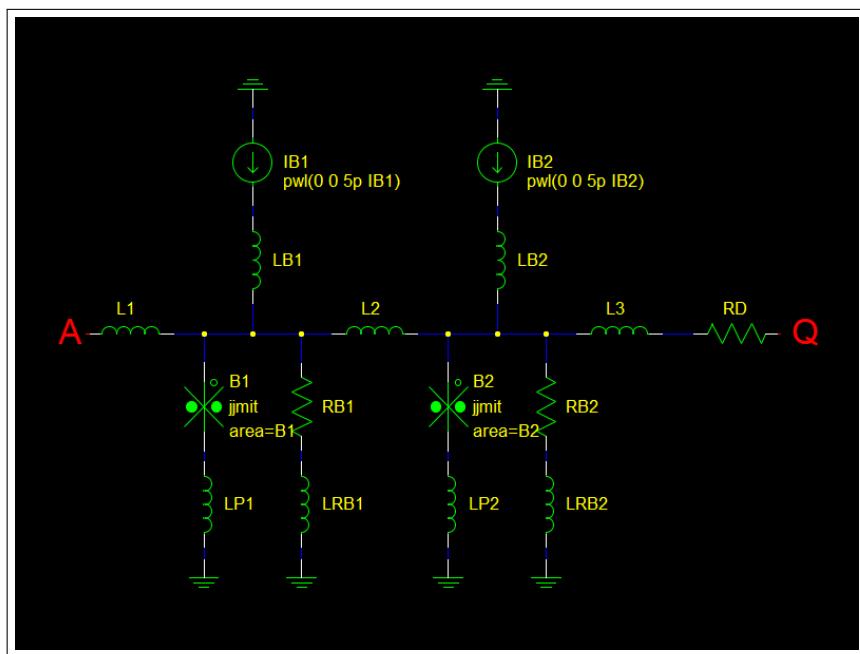


Figure 2.16: Schematic of RSFQ PTLTX.

Layout

The physical layout of the RSFQ PTLTX is shown in Fig. 2.17. The layout height is $70 \mu m$ and the width is $20 \mu m$. The biasing is brought in on M5 from an external bias line at the top of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

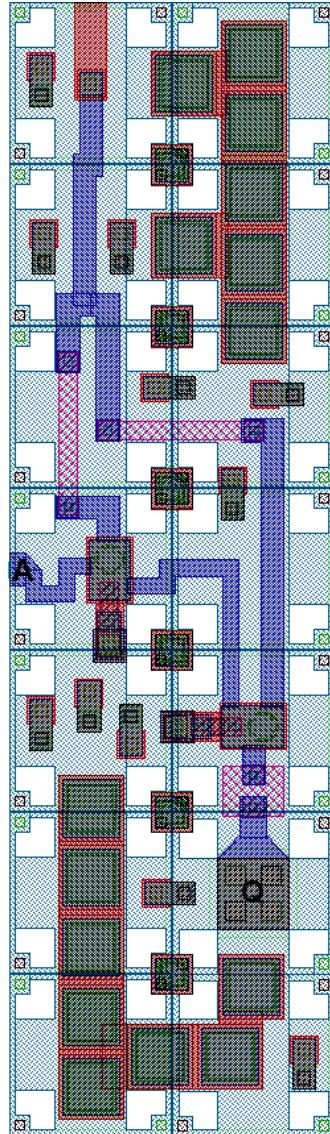


Figure 2.17: RSFQ PTLTX Layout.

Analog model

```

1  * Back-annotated simulation file written      35 | .param L2=Phi0/(2*B1*Ic0)
2  *   ↪ by InductEx v.6.1.52 on 2022/08/15.    36 | .param L3=Lptl
3  * Author: L. Schindler                      37 |
4  * Version: 3.0                                38 | .param LP1=LP
5  * Last modification date: 4 August 2022       39 | .param LP2=LP
6  * Last modification by: T. Hall               40 |
7  *$Ports          a      q                   41 | .param RB1=B0Rs/B1
8  .subckt THmitll_PTLTX a q                 42 | .param RB2=B0Rs/B2
9  .model jjmit jj(rtype=1, vg=2.8mV, cap     43 |
10 *   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    44 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
11 .param Phi0=2.067833848E-15                45 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
12 .param B0=1                                 46 |
13 .param Ic0=0.0001                           47 | B1 1 2 jjmit area=B1
14 .param IcRs=100u*6.859904418                48 | B2 4 5 jjmit area=B2
15 .param B0Rs=IcRs/Ic0*B0                     49 |
16 .param Rsheet=2                            50 | IB1 0 3 pwl(0 0 5p IB1)
17 .param Lsheet=1.13e-12                      51 | IB2 0 6 pwl(0 0 5p IB2)
18 .param LP=0.5p                             52 |
19 .param IC=2.5                             53 | LB1 3 1 1.003E-012
20 .param LB=2p                               54 | LB2 6 4 3.702E-012
21 .param BiasCoef=0.7                        55 |
22 .param Lptl=2p                            56 | L1 a 1 2.061E-012
23 .param RD=1.36                            57 | L2 1 4 4.1E-012
24 .param B1=IC                               58 | L3 4 7 6.098E-013
25 .param B2=ICtrans                         59 |
26 .param Lptl=2p                            60 | LP1 2 0 4.298E-013
27 .param RD=1.36                            61 | LP2 5 0 3.112E-013
28 .param IB1=BiasCoef*Ic0*B1                62 |
29 .param IB2=BiasCoef*Ic0*B2                63 | RD 7 q RD
30 .param LB1=LB                             64 |
31 .param LB2=LB                             65 | RB1 1 101 RB1
32 .param LB2=LB                             66 | LRB1 101 0 LRB1
33 .param L1=Phi0/(4*B1*Ic0)                  67 | RB2 4 104 RB2
34 .param L1=Phi0/(4*B1*Ic0)                  68 | LRB2 104 0 LRB2
34 | .ends

```

Listing 2.7: RSFQ PTLTX JoSIM netlist.

Table 2.7: RSFQ PTLTX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLTX using JoSIM is shown in Fig. 2.18. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected via a PTL to the PTLTX.

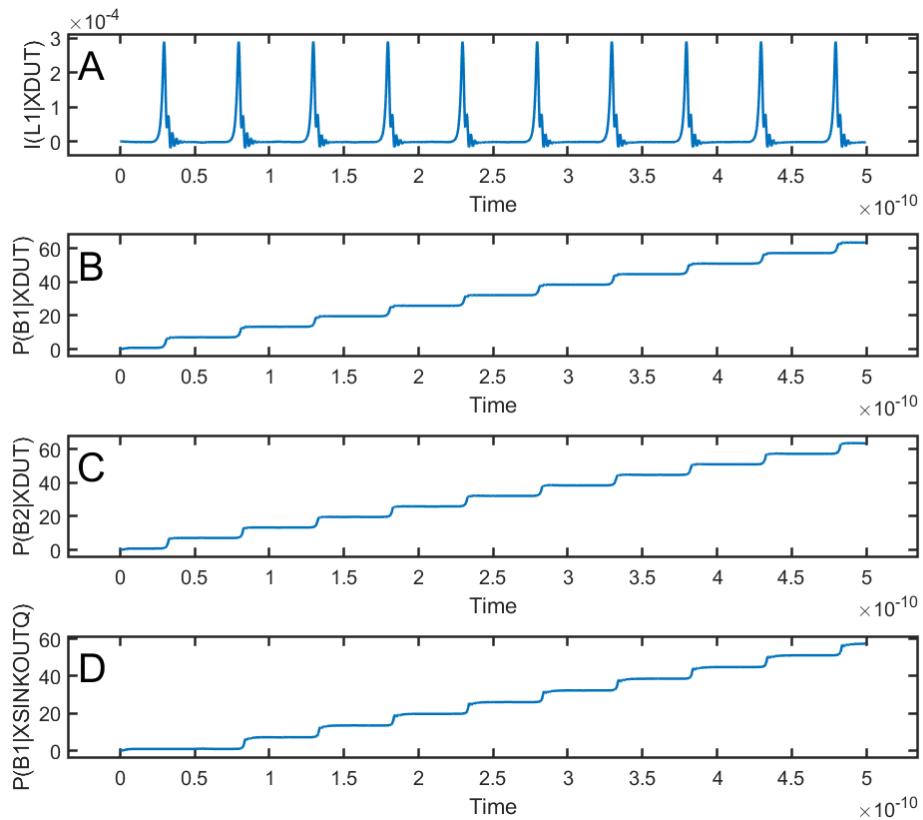


Figure 2.18: RSFQ PTLTX analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 15 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_PTLTX_v3p0_extracted (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 3.3,
21   ct_state0_a_a = 5.2;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q = 0; // All outputs start at 0
35 end
36
37 always @(posedge a or negedge a) // execute at positive and negative edges of input
38 begin
39   if ($time>4) // arbitrary steady-state time)
40     begin
41       if (errorsignal_a == 1'b1) // A critical timing is active for this input
42         begin
43           outfile = $fopen("errors.txt", "a");
44           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
45           ↪ ", $stime);
46           $fclose(outfile);
47           q <= 1'bX; // Set all outputs to unknown
48         end
49       if (errorsignal_a == 0)
50         begin
51           case (cell_state)
52             0: begin
53               q <= #(delay_state0_a_q) !q;
54               errorsignal_a = 1; // Critical timing on this input; assign
55               ↪ immediately
56               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
57               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 2.8: RSFQ PTLTX verilog model.

The digital simulation results for the RSFQ PTLTX is shown in Fig. 2.19 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.20.

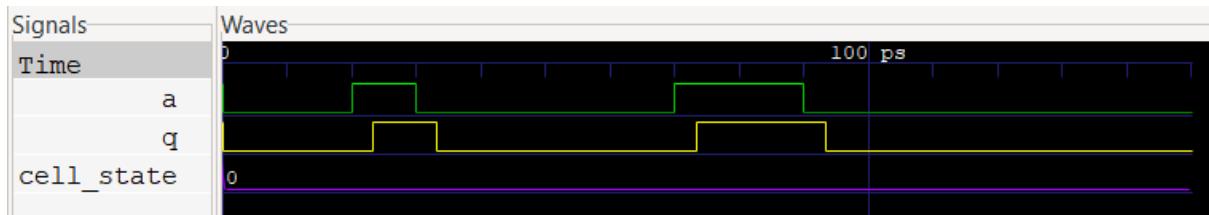


Figure 2.19: RSFQ PTLTX digital simulation results.

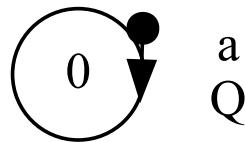


Figure 2.20: RSFQ PTLTX Mealy finite state machine diagram.

Power Consumption

Table 2.8: RSFQ PTLTX power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	910	1.03
2	910	2.07
5	910	5.17
10	910	10.3
20	910	20.7
50	910	51.7

2.1.5 PTLRX

The PTLRX is a receiver cell which receives a pulse signal from a PTL. It is connected to cells that are not designed to connect to PTLs when a PTL connection is required.

Schematic

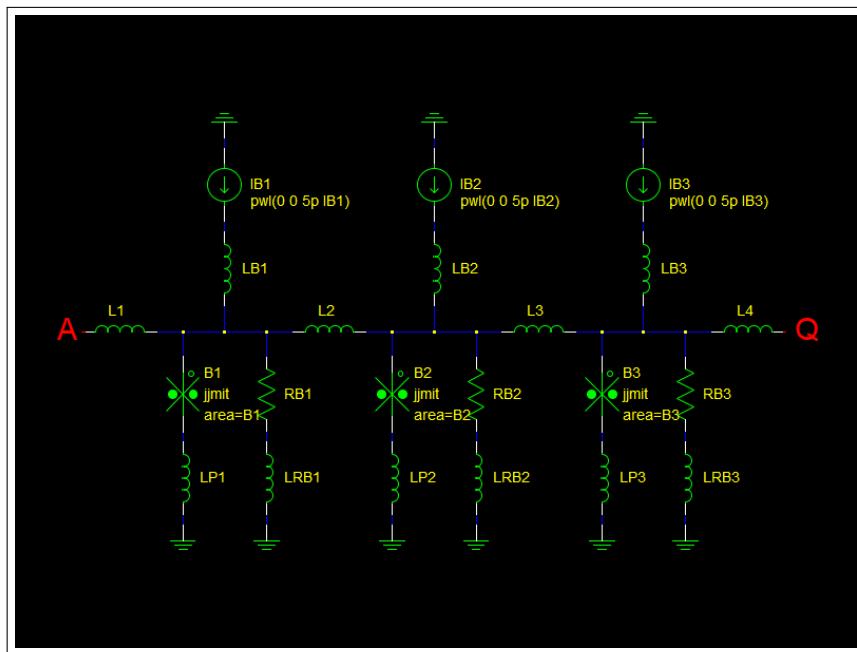


Figure 2.21: Schematic of RSFQ PTLRX.

Layout

The physical layout of the RSFQ PTLRX is shown in Fig. 2.22. The layout height is $70 \mu m$ and the width is $20 \mu m$. The biasing is brought in on M5 from an external bias line at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

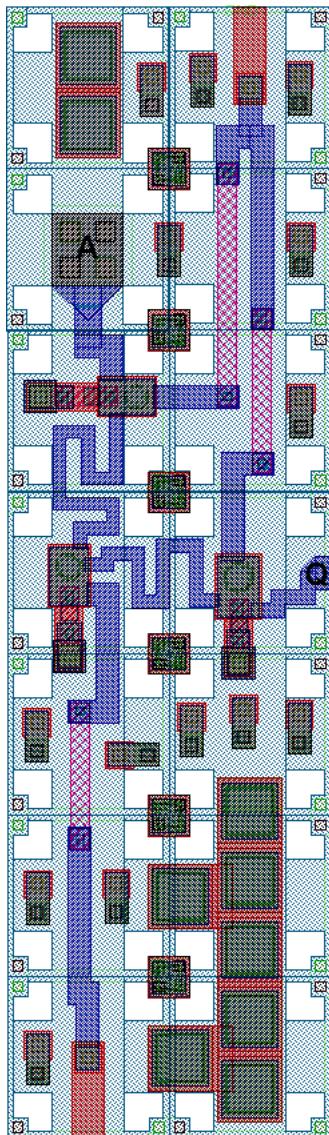


Figure 2.22: RSFQ PTLRX Layout.

Analog model

```

1  * Back-annotated simulation file written      41 | .param LP1=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/08/23.    42 | .param LP2=LP
3  * Author: L. Schindler                      43 | .param LP3=LP
4  * Version: 3.0                                44 |
5  * Last modification date: 23 August 2022     45 | .param RB1=B0Rs/B1
6  * Last modification by: T. Hall              46 | .param RB2=B0Rs/B2
7  *$Ports      a      q                      47 | .param RB3=B0Rs/B3
8  .subckt THmitll_PTLRX a q                  48 |
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    49 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
10    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA   50 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
11    ↪ )                                     51 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
12 .param Phi0=2.067833848E-15                52 |
13 .param B0=1                                  53 | B1 1 2 jjmit area=B1
14 .param Ic0=0.0001                            54 | B2 4 5 jjmit area=B2
15 .param IcRs=100u*6.859904418                 55 | B3 7 8 jjmit area=B3
16 .param B0Rs=IcRs/Ic0*B0                     56 |
17 .param Rsheet=2                             57 | IB1 0 3 pwl(0 0 5p IB1)
18 .param Lsheet=1.13e-12                      58 | IB2 0 6 pwl(0 0 5p IB2)
19 .param LP=0.5p                             59 | IB3 0 9 pwl(0 0 5p IB3)
20 .param IC=2.5                               60 |
21 .param ICreceive=1.6                        61 | LB1 3 1 1.265E-012
22 .param LB=2p                               62 | LB2 6 4 2.061E-012
23 .param BiasCoef=0.7                         63 | LB3 9 7 1.659E-012
24 .param B1=ICreceive                        64 |
25 .param B2=IC/1.25                           65 | L1 a 1 1.414E-012
26 .param B3=IC                               66 | L2 1 4 6.505E-012
27 .param IB1=BiasCoef*Ic0*B1                 67 | L3 4 7 5.179E-012
28 .param IB2=Ic0*B2                          68 | L4 7 q 2.06E-012
29 .param IB3=BiasCoef*Ic0*B3                 69 |
30 .param LB1=LB                               70 | LP1 2 0 3.679E-013
31 .param LB2=LB                               71 | LP2 5 0 4.598E-013
32 .param LB3=LB                               72 | LP3 8 0 3.89E-013
33 .param L1=Lptl                            73 |
34 .param L2=Phi0/(2*B1*Ic0)                   74 | RB1 1 101 RB1
35 .param L3=Phi0/(2*B2*Ic0)                   75 | LRB1 101 0 LRB1
36 .param L4=Phi0/(4*IC*Ic0)                   76 | RB2 4 104 RB2
37 .param L5=Phi0/(4*IC*Ic0)                   77 | LRB2 104 0 LRB2
38 .param L6=Phi0/(4*IC*Ic0)                   78 | RB3 7 107 RB3
39 .param L7=Phi0/(4*IC*Ic0)                   79 | LRB3 107 0 LRB3
40 .param L8=Phi0/(4*IC*Ic0)                   80 | .ends

```

Listing 2.9: RSFQ PTLRX JoSIM netlist.

Table 2.9: RSFQ PTLRX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLRX using JoSIM is shown in Fig. 2.23. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected to pin **q**.

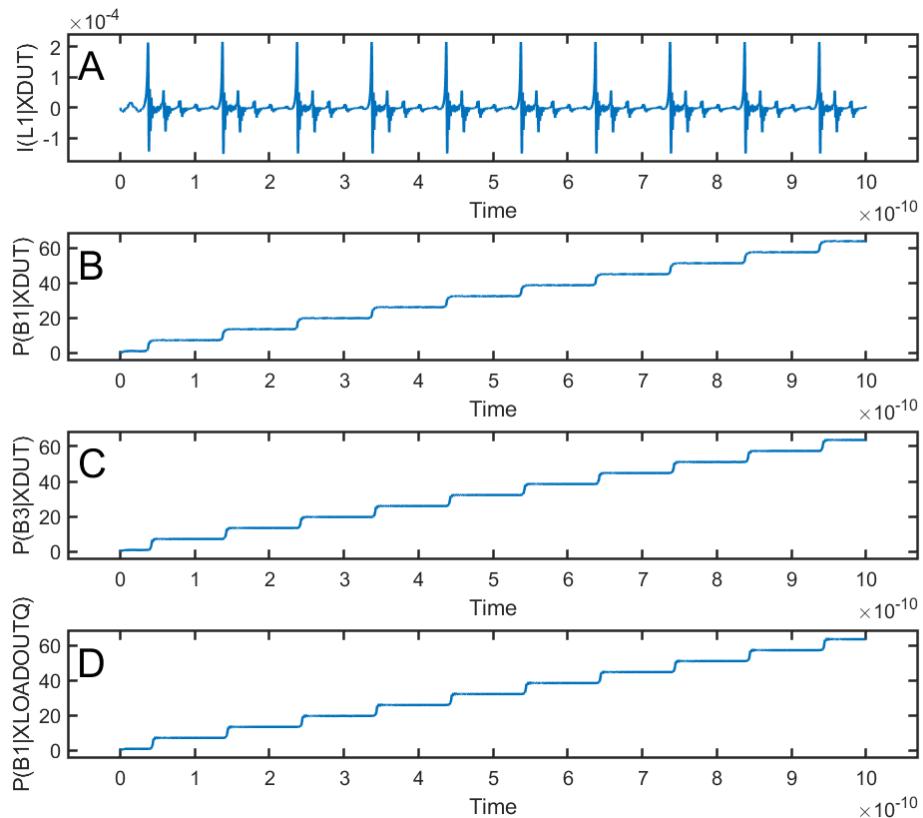


Figure 2.23: RSFQ PTLRX analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 23 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_PTLRX_v3p0_extracted (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 5.3,
21   ct_state0_a_a = 5.4;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q = 0; // All outputs start at 0
35 end
36
37 always @(posedge a or negedge a) // execute at positive and negative edges of input
38 begin
39   if ($time>4) // arbitrary steady-state time)
40     begin
41       if (errorsignal_a == 1'b1) // A critical timing is active for this input
42         begin
43           outfile = $fopen("errors.txt", "a");
44           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
45           ↪ ", $stime);
46           $fclose(outfile);
47           q <= 1'bX; // Set all outputs to unknown
48         end
49       if (errorsignal_a == 0)
50         begin
51           case (cell_state)
52             0: begin
53               q <= #(delay_state0_a_q) !q;
54               errorsignal_a = 1; // Critical timing on this input; assign
55               ↪ immediately
56               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
57               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 2.10: RSFQ PTLRX verilog model.

The digital simulation results for the RSFQ PTLRX is shown in Fig. 2.24 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.25.

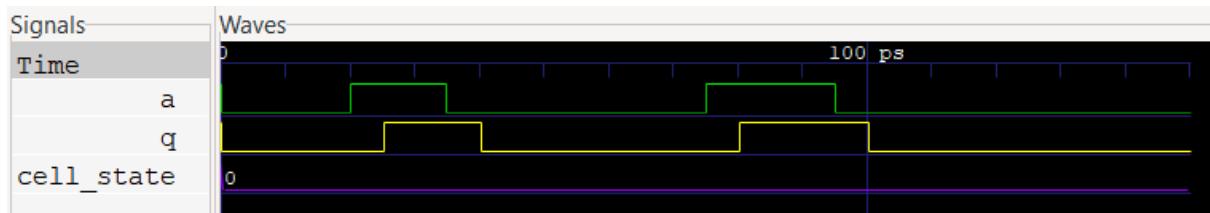


Figure 2.24: RSFQ PTLRX digital simulation results.

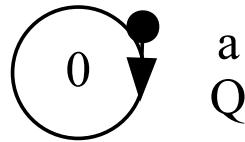


Figure 2.25: RSFQ PTLRX Mealy finite state machine diagram.

Power Consumption

Table 2.10: RSFQ PTLRX power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1270	1.26
2	1270	2.52
5	1270	6.31
10	1270	12.6
20	1270	25.2
50	1270	63.1

2.1.6 Always0 Asynchronous

The Always0 Asynchronous cell provides an output which is always zero. Two versions of the cell exist: One with an **a** input port, as seen in Fig. 2.26, and one without an **a** input port, as seen in Fig. 2.27. The cell is not designed to be directly connected to a PTL.

Schematic

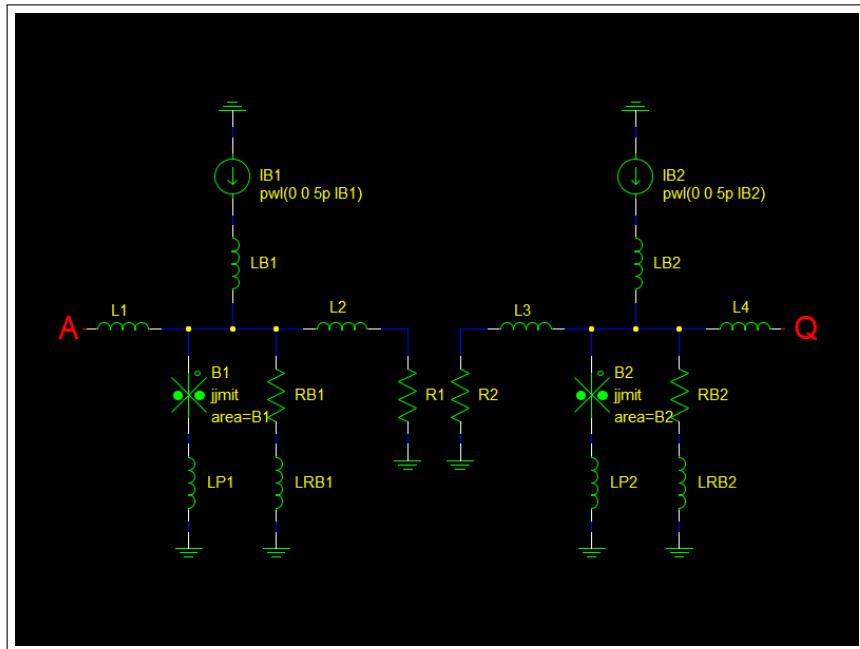


Figure 2.26: Schematic of RSFQ Always0 Asynchronous.

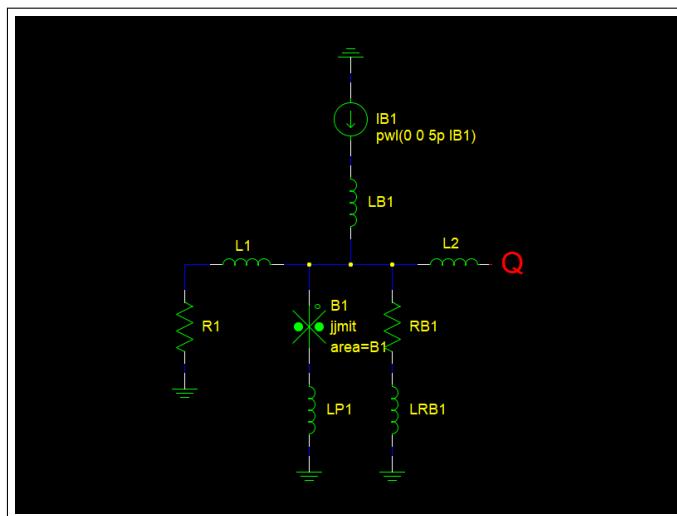


Figure 2.27: Schematic of RSFQ Always0 Asynchronous without an **a** input port.

Layout

The physical layouts of the two RSFQ Always0 Asynchronous cell versions are shown in Fig. 2.28a and 2.28b respectively. The height of the Always0 Asynchronous layout is $70 \mu\text{m}$ and the width is $20 \mu\text{m}$. For the version without the **a** input port, the width of the layout is $10 \mu\text{m}$. The cells include an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

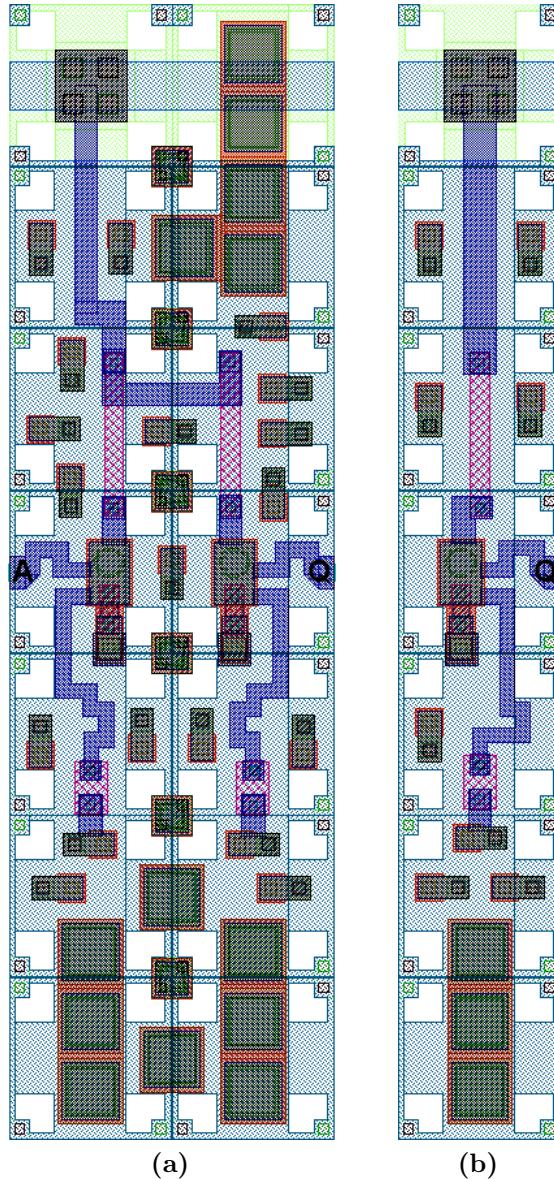


Figure 2.28: The physical layouts for (a) the RSFQ Always0 Asynchronous and (b) the RSFQ Always0 Asynchronous without an **a** input port.

Analog model

```

1  * Back-annotated simulation file written      37 | .param R2=2
2  *   ↪ by InductEx v.6.1.52 on 2022/08/23.    38 | .param LP1=LP
3  * Author: L. Schindler                      39 | .param LP2=LP
4  * Version: 3.0                                40 | .param RB1=B0Rs/B1
5  * Last modification date: 3 August 2022       41 | .param RB2=B0Rs/B2
6  * Last modification by: T. Hall               42 |
7  *$Ports      a      q                         43 |
8 .subckt THmitll_ALWAYS0_ASYNC a q             44 |
9 .model jjmit jj(rtype=1, vg=2.8mV, cap      45 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
10    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     46 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
11    ↪ )                                         47 |
12 .param Phi0=2.067833848E-15                  48 | B1 1 2 jjmit area=B1
13 .param B0=1                                    49 | B2 6 7 jjmit area=B2
14 .param Ic0=0.0001                            50 |
15 .param IcRs=100u*6.859904418                 51 | IB1 0 3 pwl(0 0 5p IB1)
16 .param B0Rs=IcRs/Ic0*B0                     52 | IB2 0 8 pwl(0 0 5p IB2)
17 .param Rsheet=2                             53 |
18 .param Lsheet=1.13e-12                       54 | LB1 3 1 7.025E-013
19 .param LP=0.5p                             55 | LB2 8 6 6.963E-013
20 .param IC=2.5                               56 |
21 .param LB=2p                               57 | L1 a 1 2.08E-012
22 .param BiasCoef=0.7                        58 | L2 1 4 4.162E-012
23 .param B1=IC                               59 | L3 5 6 4.149E-012
24 .param B2=IC                               60 | L4 6 q 2.083E-012
25 .param IB1=B1*Ic0*BiasCoef                61 |
26 .param IB2=B2*Ic0*BiasCoef                62 | R1 4 0 R1
27                                         63 | R2 5 0 R2
28 .param LB1=LB                             64 |
29 .param LB2=LB                             65 | LP1 2 0 3.835E-013
30                                         66 | LP2 7 0 3.846E-013
31 .param L1=Phi0/(4*B1*Ic0)                  67 |
32 .param L2=Phi0/(2*B1*Ic0)                  68 | RB1 1 101 RB1
33 .param L3=Phi0/(2*B2*Ic0)                  69 | LRB1 101 0 LRB1
34 .param L4=Phi0/(4*B2*Ic0)                  70 | RB2 6 106 RB2
35                                         71 | LRB2 106 0 LRB2
36 .param R1=2                                72 | .ends

```

Listing 2.11: RSFQ Always0 Asynchronous JoSIM netlist.

Table 2.11: RSFQ Always0 Asynchronous pin list.

Pin	Description
a	Data input
q	Data output

```

1  * Back-annotated simulation file written      28 | .param L1=Phi0/(2*B1*Ic0)
2  *      ↪ by InductEx v.6.1.52 on 2022/08/23.   29 | .param L2=Phi0/(4*B1*Ic0)
3  * Author: L. Schindler                      30 |
4  * Version: 3.0                                31 | .param R1=2
5  * Last modification date: 3 August 2022       32 |
6  * Last modification by: T. Hall               33 | .param LP1=LP
7  *$Ports          q                           34 |
8  .subckt THmitll_ALWAYS0_ASYNC_NOA q         35 | .param RB1=B0Rs/B1
9  .model jjmit jj(rtype=1, vg=2.8mV, cap     36 |
10    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    37 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
11    ↪ )                                         38 |
12 .param Phi0=2.067833848E-15                  39 | B1 2 3 jjmit area=B1
13 .param B0=1                                    40 |
14 .param Ic0=0.0001                             41 | IB1 0 4 pwl(0 0 5p IB1)
15 .param IcRs=100u*6.859904418                 42 |
16 .param B0Rs=IcRs/Ic0*B0                     43 | LB1 4 2 7.52E-013
17 .param Rsheet=2                               44 |
18 .param LP=0.5p                                45 | LP1 3 0 4.232E-013
19 .param IC=2.5                                46 |
20 .param LB=2p                                 47 | L1 1 2 4.162E-012
21 .param BiasCoef=0.7                          48 | L2 2 q 2.078E-012
22 .param B1=IC                                 49 |
23 .param IB1=B1*Ic0*BiasCoef                 50 | R1 1 0 R1
24 .param LB1=LB                                51 |
25 .param LRB1=RB1*Lsheet+LP                   52 | RB1 2 102 RB1
26 .param .ends                                  53 | LRB1 102 0 LRB1
27

```

Listing 2.12: RSFQ Always0 Asynchronous, without an **a** input port, JoSIM netlist.

Table 2.12: RSFQ Always0 Asynchronous, without an **a** input port, pin list.

Pin	Description
q	Data output

Digital model

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 23 August 2022
5 // Last modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_ALWAYS0_ASYNC (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 initial
20   begin
21     q = 0; // Output always 0
22   end
23
24 always
25   begin
26     #10 q = 0; // Output always 0
27   end
28 endmodule

```

Listing 2.13: RSFQ Always0 Asynchronous verilog model.

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 23 August 2022
5 // Last modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_ALWAYS0_ASYNC_NOA (q);
9
10 output
11   q;
12
13 reg
14   q;
15
16 initial
17   begin
18     q = 0; // Output always 0
19   end
20
21 always
22   begin
23     #10 q = 0; // Output always 0
24   end
25
26 endmodule

```

Listing 2.14: RSFQ Always0 Asynchronous, without an **a** input port, verilog model.

Power consumption

Table 2.13: RSFQ Always0 Asynchronous power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	910	0.52
2	910	1.03
5	910	2.58
10	910	5.17
20	910	10.3
50	910	25.8

Table 2.14: RSFQ Always0 Asynchronous, without an **a** input port, power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	455	N/A
2	455	N/A
5	455	N/A
10	455	N/A
20	455	N/A
50	455	N/A

2.1.7 Always0 Synchronous

The Always0 Synchronous cell provides an output which is always zero synchronous to a clock signal. Two versions of the cell exist: One with an **a** input port, as seen in Fig. 2.29, and one without an **a** input port, as seen in Fig. 2.30. The Always0 Synchronous is not designed to be directly connected to a PTL.

Schematic

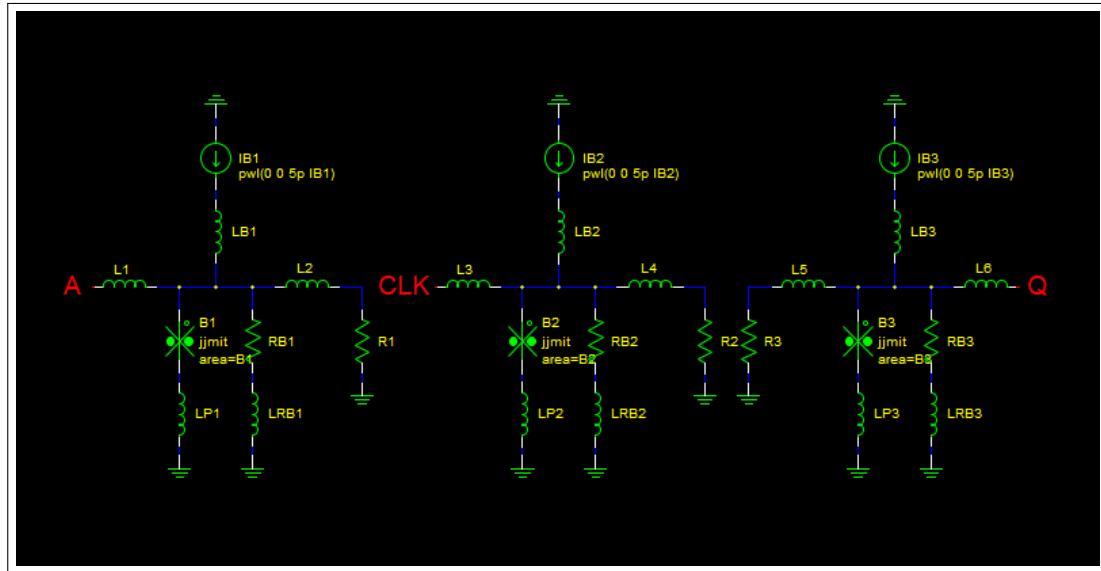


Figure 2.29: Schematic of RSFQ Always0 Synchronous.

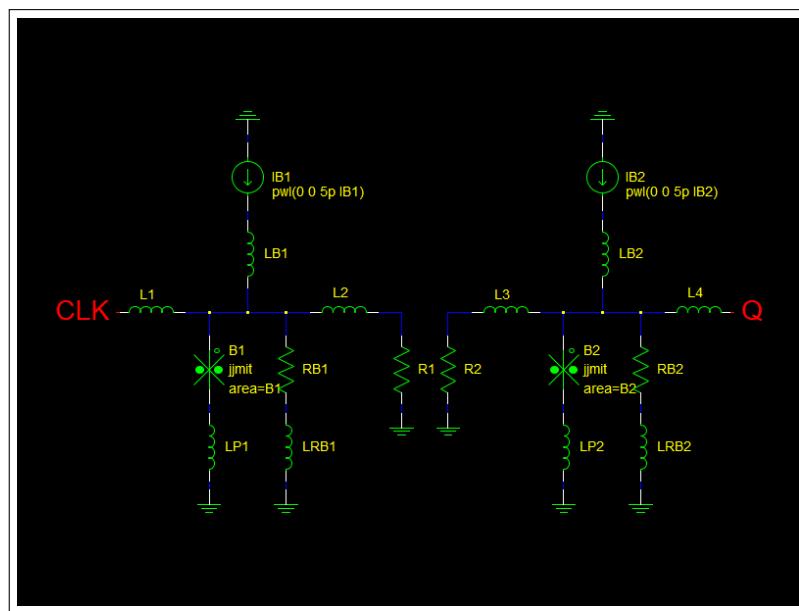


Figure 2.30: Schematic of RSFQ Always0 Synchronous without an **a** input port.

Layout

The physical layouts of the two RSFQ Always0 Synchronous cell versions are shown in Fig. 2.31a and 2.31b respectively. The height of the Always0 Synchronous layout is $70 \mu\text{m}$ and the width is $20 \mu\text{m}$. For the version without the **a** input port, the width of the layout is $20 \mu\text{m}$. The cells include an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

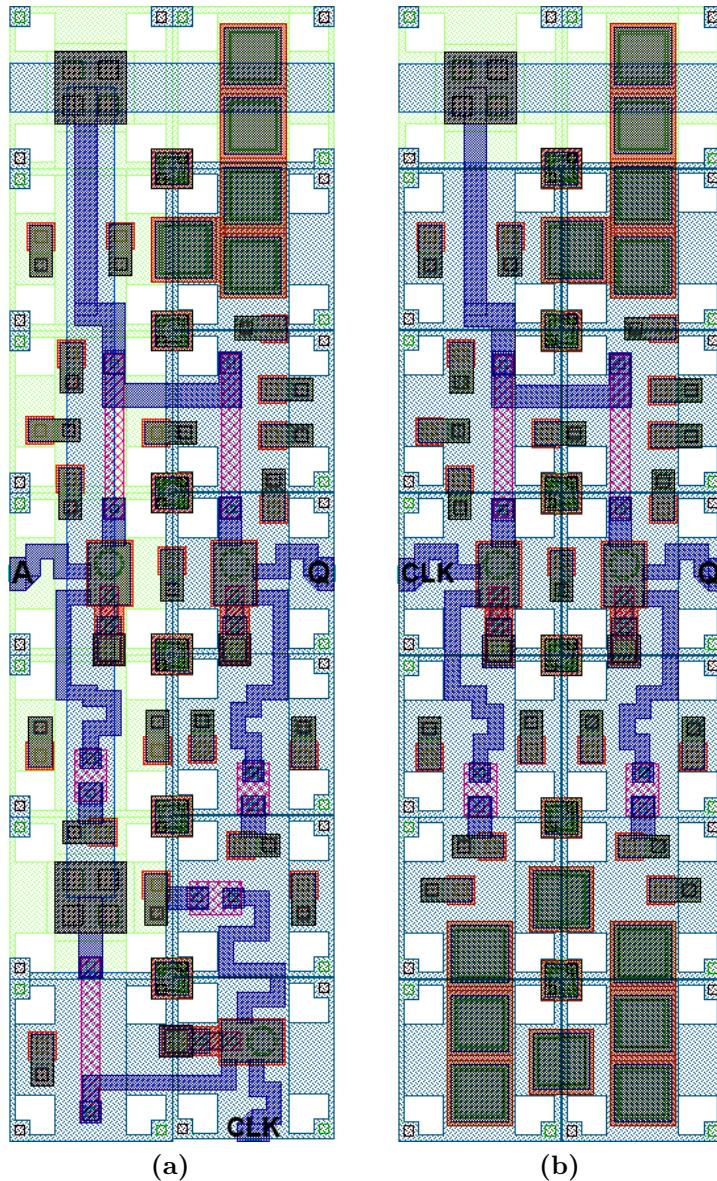


Figure 2.31: The physical layouts for (a) the RSFQ Always0 Synchronous and (b) the RSFQ Always0 Synchronous without an **a** input port.

Analog model

```

1 * Back-annotated simulation file written      46 .param LP2=LP
2   ↪ by InductEx v.6.1.52 on 2022/08/23.      47 .param LP3=LP
3 * Author: L. Schindler                      48
4 * Version: 3.0                                49 .param RB1=B0Rs/B1
5 * Last modification date: 3 August 2022       50 .param RB2=B0Rs/B2
6 * Last modification by: T. Hall               51 .param RB3=B0Rs/B3
7
8 *$Ports          a      clk      q           52
9 .subckt THmitll_ALWAYS0_SYNC a clk q         53 .param LRB1=(RB1/Rsheet)*Lsheet+LP
10 .model jjmit jj(rtype=1, vg=2.8mV, cap     54 .param LRB2=(RB2/Rsheet)*Lsheet+LP
11   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    55 .param LRB3=(RB3/Rsheet)*Lsheet+LP
12   ↪ )                                         56
13 .param Phi0=2.067833848E-15                 57 B1 1 2 jjmit area=B1
14 .param B0=1                                    58 B2 5 6 jjmit area=B2
15 .param Ic0=0.0001                             59 B3 10 11 jjmit area=B3
16 .param IcRs=100u*6.859904418                  60
17 .param B0Rs=IcRs/Ic0*B0                      61 IB1 0 3 pwl(0 0 5p IB1)
18 .param Rsheet=2                               62 IB2 0 7 pwl(0 0 5p IB2)
19 .param Lsheet=1.13e-12                         63 IB3 0 12 pwl(0 0 5p IB3)
20 .param LP=0.5p                                64
21 .param IC=2.5                                 65 LB1 3 1 7.02E-013
22 .param LB=2p                                  66 LB2 7 5 3.529E-012
23 .param BiasCoef=0.7                          67 LB3 12 10 6.962E-013
24 .param B1=IC                                 68
25 .param B2=IC                                 69 LP1 2 0 3.842E-013
26 .param B3=IC                                 70 LP2 6 0 3.469E-013
27 .param IB1=B1*Ic0*BiasCoef                  71 LP3 11 0 3.849E-013
28 .param IB2=B2*Ic0*BiasCoef                  72
29 .param IB3=B3*Ic0*BiasCoef                  73 L1 a 1 2.08E-012
30 .param LB1=LB                                74 L2 1 4 4.129E-012
31 .param LB2=LB                                75 L3 clk 5 2.057E-012
32 .param LB3=LB                                76 L4 5 8 4.116E-012
33 .param L1=Phi0/(4*B1*Ic0)                   77 L5 9 10 4.148E-012
34 .param L2=Phi0/(2*B1*Ic0)                   78 L6 10 q 2.082E-012
35 .param L3=Phi0/(4*B2*Ic0)                   79
36 .param L4=Phi0/(2*B2*Ic0)                   80 R1 4 0 R1
37 .param L5=Phi0/(2*B3*Ic0)                   81 R2 8 0 R2
38 .param L6=Phi0/(4*B3*Ic0)                   82 R3 9 0 R3
39 .param R1=2                                  83
40 .param R2=2                                  84 RB1 1 101 RB1
41 .param R3=2                                  85 LRB1 101 0 LRB1
42 .param LP1=LP                                86 RB2 5 105 RB2
43 .param LP2=LP                                87 LRB2 105 0 LRB2
44 .param LP3=LP                                88 RB3 10 110 RB3
45 .param LRB1=(RB1/Rsheet)*Lsheet+LP          89 LRB3 110 0 LRB3
46 .param LRB2=(RB2/Rsheet)*Lsheet+LP          90 .ends

```

Listing 2.15: RSFQ Always0 Synchronous JoSIM netlist.

Table 2.15: RSFQ Always0 Synchronous pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

```

1  * Back-annotated simulation file written      37 | .param R2=2
2  *   ↪ by InductEx v.6.1.52 on 2022/08/23.    38 | .param LP1=LP
3  * Author: L. Schindler                      39 | .param LP2=LP
4  * Version: 3.0                                40 | .param RB1=B0Rs/B1
5  * Last modification date: 23 August 2022     41 | .param RB2=B0Rs/B2
6  * Last modification by: T. Hall              42 |
7  *$Ports          clk      q                  43 |
8  .subckt THmitll_ALWAYS0_SYNC_NOA clk q      44 |
9  .model jjmit jj(rtype=1, vg=2.8mV, cap      45 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
10 .        ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA 46 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
11 .        ↪ )                               47 | B1 1 2 jjmit area=B1
12 .param Phi0=2.067833848E-15                 48 | B2 6 7 jjmit area=B2
13 .param B0=1                                  49 |
14 .param Ic0=0.0001                            50 |
15 .param IcRs=100u*6.859904418                51 | IB1 0 3 pwl(0 0 5p IB1)
16 .param B0Rs=IcRs/Ic0*B0                     52 | IB2 0 8 pwl(0 0 5p IB2)
17 .param Rsheet=2                             53 |
18 .param Lsheet=1.13e-12                      54 | LB1 3 1 7.025E-013
19 .param LP=0.5p                             55 | LB2 8 6 6.963E-013
20 .param IC=2.5                             56 |
21 .param LB=2p                               57 | LP1 2 0 3.835E-013
22 .param BiasCoef=0.7                        58 | LP2 7 0 3.846E-013
23 .param B1=IC                               59 |
24 .param B2=IC                               60 | L1 clk 1 2.08E-012
25 .param IB1=B1*Ic0*BiasCoef                61 | L2 1 4 4.162E-012
26 .param IB2=B2*Ic0*BiasCoef                62 | L3 5 6 4.149E-012
27 .param LB1=LB                             63 | L4 6 q 2.083E-012
28 .param LB2=LB                             64 |
29 .param L1=Phi0/(4*B1*Ic0)                  65 | R1 4 0 R1
30 .param L2=Phi0/(2*B1*Ic0)                  66 | R2 5 0 R2
31 .param L3=Phi0/(2*B2*Ic0)                  67 |
32 .param L4=Phi0/(4*B2*Ic0)                  68 | RB1 1 101 RB1
33 .param R1=2                                69 | LRB1 101 0 LRB1
34 .param R2=2                                70 | RB2 6 106 RB2
35 .param R3=2                                71 | LRB2 106 0 LRB2
36 .param R4=2                                72 | .ends

```

Listing 2.16: RSFQ Always0 Synchronous, without an **a** input port, JoSIM netlist.

Table 2.16: RSFQ Always0 Synchronous, without an **a** input port, pin list.

Pin	Description
clk	Clock input
q	Data output

Digital model

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 23 August 2022
5 // Last modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_ALWAYS0_SYNC (a, clk, q);
9
10 input
11   a;
12   clk;
13
14 output
15   q;
16
17 reg
18   q;
19
20 initial
21 begin
22   q = 0; // Output always 0
23 end
24
25 always
26 begin
27   #10 q = 0; // Output always 0
28 end
29 endmodule

```

Listing 2.17: RSFQ Always0 Synchronous verilog model.

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 23 August 2022
5 // Last modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_ALWAYS0_SYNC_NOA (clk, q);
9
10 input
11   clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 initial
20 begin
21   q = 0; // Output always 0
22 end
23
24 always
25 begin
26   #10 q = 0; // Output always 0
27 end
28 endmodule

```

Listing 2.18: RSFQ Always0 Synchronous, without an **a** input port, verilog model.

Power consumption

Table 2.17: RSFQ Always0 Synchronous power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1365	1.03
2	1365	2.07
5	1365	5.17
10	1365	10.3
20	1365	20.7
50	1365	51.7

Table 2.18: RSFQ Always0 Synchronous, without an **a** input port, power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	910	0.52
2	910	1.03
5	910	2.58
10	910	5.17
20	910	10.3
50	910	25.8

2.2 Logic Cells

2.2.1 AND2

The RSFQ AND2 cell generates an output pulse if pulses from both input signal lines were received before the clock signal. The cell is not designed to be directly connected to a PTL.

Schematic

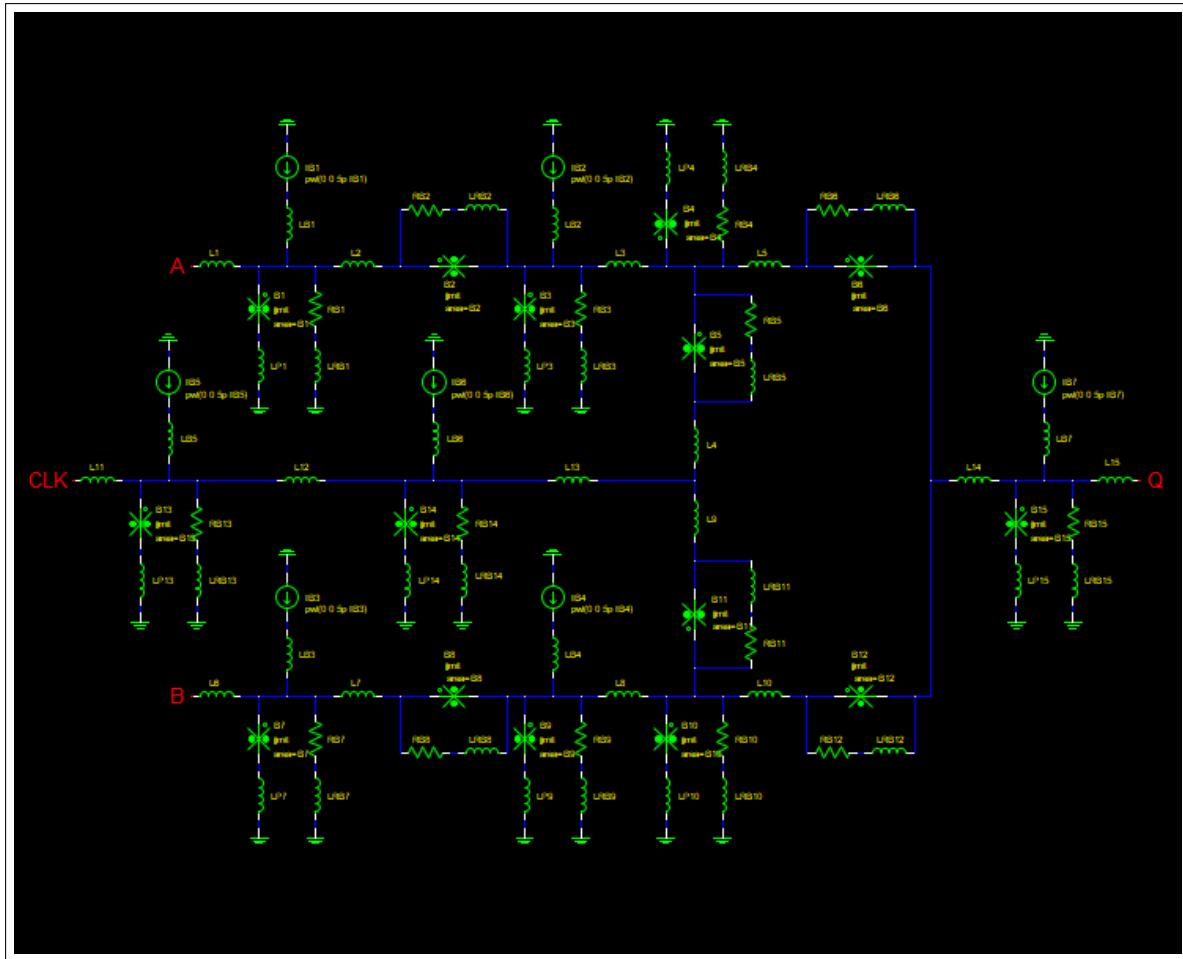


Figure 2.32: Schematic of RSFQ AND2.

Layout

The physical layout of the RSFQ AND2 is shown in Fig. 2.33. The layout height is $70 \mu\text{m}$ and the width is $50 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

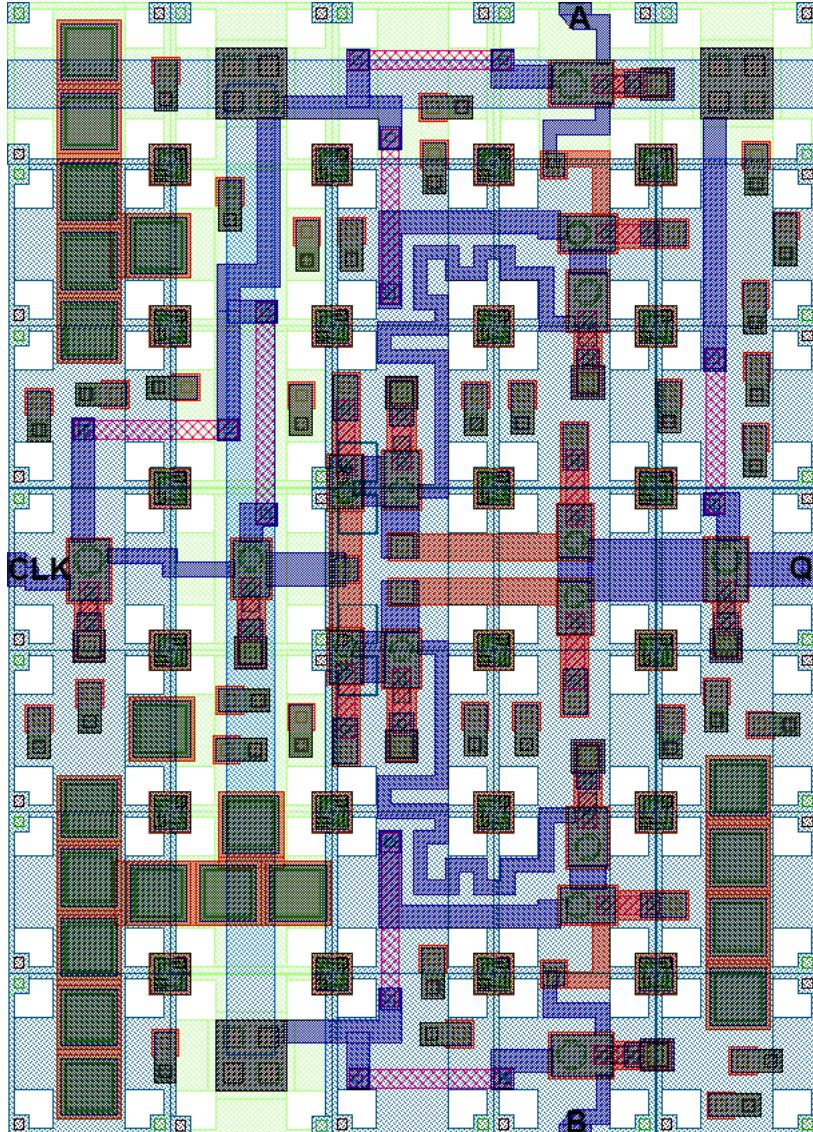


Figure 2.33: RSFQ AND2 Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param L11=1.5293p
2  *   ↪ by InductEx v.6.1.52 on 2022/08/09.    65  .param L12=2.6230p
3  * Author: L. Schindler                      66  .param L13=0.7965p
4  * Version: 3.0                                67  .param L14=0.7671p
5  * Last modification date: 4 August 2022       68  .param L15=1.2144p
6  * Last modification by: T. Hall               69
7  *$Ports      a      b      clk      q      70  .param LP1=LP
8  .subckt THmitll_AND2 a b clk q             71  .param LP3=LP
9  .model jjmit jj(rtype=1, vg=2.8mV, cap     72  .param LP4=LP
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param LP7=LP
   ↪ )                                         74  .param LP9=LP
10 .param Phi0=2.067833848E-15                75  .param LP10=LP
11 .param B0=1                                 76  .param LP13=LP
12 .param Ic0=0.0001                           77  .param LP14=LP
13 .param IcRs=100u*6.859904418                 78  .param LP15=LP
14 .param B0Rs=IcRs/Ic0*B0                     79
15 .param Rsheet=2                            80  .param RB1=B0Rs/B1
16 .param Lsheet=1.13e-12                      81  .param RB2=B0Rs/B2
17 .param LP=0.5p                             82  .param RB3=B0Rs/B3
18 .param IC=2.5                               83  .param RB4=B0Rs/B4
19 .param LB=2p                               84  .param RB5=B0Rs/B5
20 .param BiasCoef=0.7                         85  .param RB6=B0Rs/B6
21
22 .param B1=2.5                             86  .param RB7=B0Rs/B7
23 .param B2=1.60                            87  .param RB8=B0Rs/B8
24 .param B3=1.94                            88  .param RB9=B0Rs/B9
25 .param B4=1.57                            89  .param RB10=B0Rs/B10
26 .param B5=1.25                            90  .param RB11=B0Rs/B11
27 .param B6=1.25                            91  .param RB12=B0Rs/B12
28 .param B7=2.5                             92  .param RB13=B0Rs/B13
29 .param B8=1.60                            93  .param RB14=B0Rs/B14
30 .param B9=1.94                            94  .param RB15=B0Rs/B15
31 .param B10=1.57                           95
32 .param B11=1.25                           96  .param LRB1=(RB1/Rsheet)*Lsheet+LP
33 .param B12=1.25                           97  .param LRB2=(RB2/Rsheet)*Lsheet
34 .param B13=2.5                            98  .param LRB3=(RB3/Rsheet)*Lsheet+LP
35 .param B14=1.71                           99  .param LRB4=(RB4/Rsheet)*Lsheet+LP
36 .param B15=2.5                            100 .param LRB5=(RB5/Rsheet)*Lsheet
37
38 .param IB1=175u                           101 .param LRB6=(RB6/Rsheet)*Lsheet
39 .param IB2=162u                           102 .param LRB7=(RB7/Rsheet)*Lsheet+LP
40 .param IB3=175u                           103 .param LRB8=(RB8/Rsheet)*Lsheet
41 .param IB4=162u                           104 .param LRB9=(RB9/Rsheet)*Lsheet+LP
42 .param IB5=175u                           105 .param LRB10=(RB10/Rsheet)*Lsheet+LP
43 .param IB6=124u                           106 .param LRB11=(RB11/Rsheet)*Lsheet
44 .param IB7=175u                           107 .param LRB12=(RB12/Rsheet)*Lsheet
45
46 .param LB1=LB                            108 .param LRB13=(RB13/Rsheet)*Lsheet+LP
47 .param LB2=LB                            109 .param LRB14=(RB14/Rsheet)*Lsheet+LP
48 .param LB3=LB                            110 .param LRB15=(RB15/Rsheet)*Lsheet+LP
49 .param LB4=LB                            111
50 .param LB5=LB                            112 B1 1 2 jjmit area=B1
51 .param LB6=LB                            113 B2 4 5 jjmit area=B2
52 .param LB7=LB                            114 B3 5 6 jjmit area=B3
53
54 .param L1=1.8843p                         115 B4 8 9 jjmit area=B4
55 .param L2=4.2266p                         116 B5 8 10 jjmit area=B5
56 .param L3=9.6820p                         117 B6 12 13 jjmit area=B6
57 .param L4=0.9913p                         118 B7 14 15 jjmit area=B7
58 .param L5=2.5745p                         119 B8 17 18 jjmit area=B8
59 .param L6=1.8843p                         120 B9 18 19 jjmit area=B9
60 .param L7=4.2266p                         121 B10 21 22 jjmit area=B10
61 .param L8=9.6820p                         122 B11 21 23 jjmit area=B11
62 .param L9=0.9913p                         123 B12 24 13 jjmit area=B12
63 .param L10=2.5745p                        124 B13 25 26 jjmit area=B13
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```

130	IB3 0 16 pwl(0 0 5p IB3)	167	LP14 29 0 3.972E-013
131	IB4 0 20 pwl(0 0 5p IB4)	168	LP15 32 0 3.699E-013
132	IB5 0 27 pwl(0 0 5p IB5)	169	
133	IB6 0 30 pwl(0 0 5p IB6)	170	RB1 1 101 RB1
134	IB7 0 33 pwl(0 0 5p IB7)	171	LRB1 101 0 LRB1
135		172	RB2 4 104 RB2
136	LB1 3 1 1.032E-012	173	LRB2 104 5 LRB2
137	LB2 7 5 3.135E-012	174	RB3 5 105 RB3
138	LB3 16 14 1.016E-012	175	LRB3 105 0 LRB3
139	LB4 20 18 3.19E-012	176	RB4 108 8 RB4
140	LB5 27 25 1.708E-012	177	LRB4 0 108 LRB4
141	LB6 30 28 6.363E-013	178	RB5 8 110 RB5
142	LB7 33 31 7.55E-013	179	LRB5 110 10 LRB5
143		180	RB6 12 112 RB6
144	L1 a 1 1.874E-012	181	LRB6 112 13 LRB6
145	L2 1 4 4.249E-012	182	RB7 14 114 RB7
146	L3 5 8 9.672E-012	183	LRB7 114 0 LRB7
147	L4 10 11 9.976E-013	184	RB8 17 117 RB8
148	L5 8 12 2.561E-012	185	LRB8 117 18 LRB8
149	L6 b 14 1.875E-012	186	RB9 18 118 RB9
150	L7 14 17 4.233E-012	187	LRB9 118 0 LRB9
151	L8 18 21 9.691E-012	188	RB10 21 121 RB10
152	L9 11 23 9.928E-013	189	LRB10 121 0 LRB10
153	L10 21 24 2.556E-012	190	RB11 123 21 RB11
154	L11 clk 25 1.531E-012	191	LRB11 23 123 LRB11
155	L12 25 28 2.626E-012	192	RB12 24 124 RB12
156	L13 28 11 7.973E-013	193	LRB12 124 13 LRB12
157	L14 13 31 7.691E-013	194	RB13 25 125 RB13
158	L15 31 q 1.217E-012	195	LRB13 125 0 LRB13
159		196	RB14 28 128 RB14
160	LP1 2 0 3.464E-013	197	LRB14 128 0 LRB14
161	LP3 6 0 6.827E-013	198	RB15 31 131 RB15
162	LP4 0 9 4.723E-013	199	LRB15 131 0 LRB15
163	LP7 15 0 3.484E-013	200	.ends
164	LP9 19 0 6.81E-013		
165	LP10 22 0 4.756E-013		
166	LP13 26 0 3.392E-013		

Listing 2.19: RSFQ AND2 JoSIM netlist.**Table 2.19:** RSFQ AND2 pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ AND2 using JoSIM is shown in Fig. 2.34. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected to pin **q**.

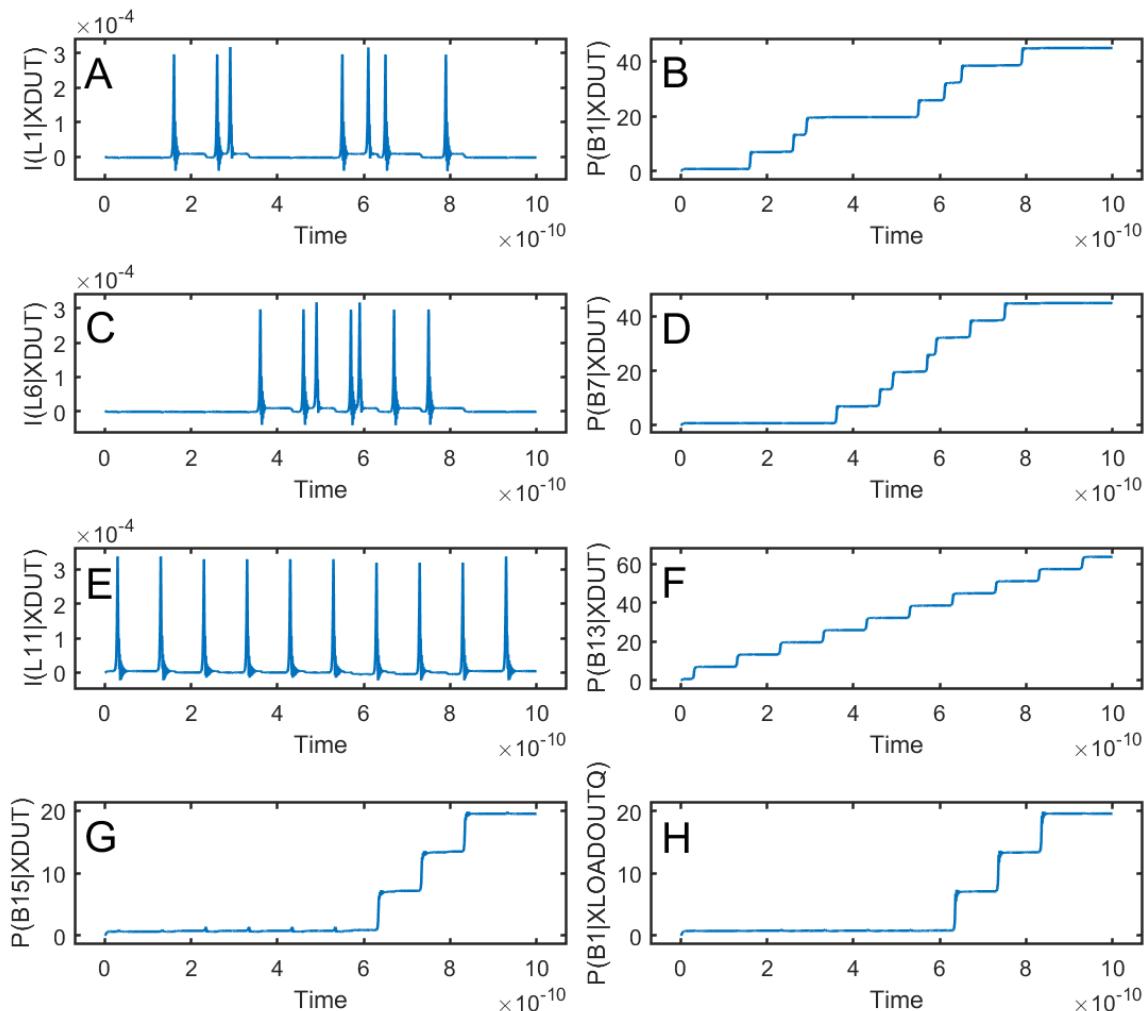


Figure 2.34: RSFQ AND2 analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 9 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_AND2_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state3_clk_q = 5.0,
21   ct_state0_clk_a = 1.2,
22   ct_state0_clk_b = 1.2,
23   ct_state1_clk_a = 1.6,
24   ct_state1_clk_b = 1.0,
25   ct_state2_clk_a = 1.0,
26   ct_state2_clk_b = 1.6,
27   ct_state3_clk_a = 0.7,
28   ct_state3_clk_b = 0.7;
29
30 reg
31   errorsignal_a,
32   errorsignal_b,
33   errorsignal_clk;
34
35 integer
36   outfile,
37   cell_state; // internal state of the cell
38
39 initial
40 begin
41   errorsignal_a = 0;
42   errorsignal_b = 0;
43   errorsignal_clk = 0;
44   cell_state = 0; // Startup state
45   q = 0; // All outputs start at 0
46 end
47
48 always @(posedge a or negedge a) // execute at positive and negative edges of input
49 begin
50   if ($time>4) // arbitrary steady-state time)
51     begin
52       if (errorsignal_a == 1'b1) // A critical timing is active for this input
53         begin
54           outfile = $fopen("errors.txt", "a");
55           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
56           ↪ ", $stime);
57           $fclose(outfile);
58           q <= 1'bX; // Set all outputs to unknown
59         end
60       if (errorsignal_a == 0)
61         begin
62           case (cell_state)
63             0: begin
64               cell_state = 1; // Blocking statement -- immediately
65             end
66             1: begin
67               end

```

```

67          2: begin
68              cell_state = 3; // Blocking statement -- immediately
69          end
70          3: begin
71              end
72          endcase
73      end
74  end
75
76
77 always @(posedge b or negedge b) // execute at positive and negative edges of input
78 begin
79     if ($time>4) // arbitrary steady-state time)
80     begin
81         if (errorsignal_b == 1'b1) // A critical timing is active for this input
82         begin
83             outfile = $fopen("errors.txt", "a");
84             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d.ps.\n"
85                         ↪ ", $stime);
86             $fclose(outfile);
87             q <= 1'bX; // Set all outputs to unknown
88         end
89         if (errorsignal_b == 0)
90         begin
91             case (cell_state)
92                 0: begin
93                     cell_state = 2; // Blocking statement -- immediately
94                 end
95                 1: begin
96                     cell_state = 3; // Blocking statement -- immediately
97                 end
98                 2: begin
99                     end
100                3: begin
101                    end
102                endcase
103            end
104        end
105    end
106
107 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
108 begin
109     if ($time>4) // arbitrary steady-state time)
110     begin
111         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
112         begin
113             outfile = $fopen("errors.txt", "a");
114             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d.ps.\n"
115                         ↪ ", $stime);
116             $fclose(outfile);
117             q <= 1'bX; // Set all outputs to unknown
118         end
119         if (errorsignal_clk == 0)
120         begin
121             case (cell_state)
122                 0: begin
123                     errorsignal_a = 1; // Critical timing on this input; assign
124                         ↪ immediately
125                     errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
126                         ↪ after critical timing expires
127                     errorsignal_b = 1; // Critical timing on this input; assign
128                         ↪ immediately
129                     errorsignal_b <= #(ct_state0_clk_b) 0; // Clear error signal
128                         ↪ after critical timing expires
130                 end
131                 1: begin
132                     cell_state = 0; // Blocking statement -- immediately
133                     errorsignal_a = 1; // Critical timing on this input; assign
134                         ↪ immediately
135                     errorsignal_a <= #(ct_state1_clk_a) 0; // Clear error signal
136                         ↪ after critical timing expires
137                 end
138             endcase
139         end
140     end
141 
```

```

130           → after critical timing expires
131           errorsignal_b = 1; // Critical timing on this input; assign
132           → immediately
133           errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
134           → after critical timing expires
135       end
136   begin
137       cell_state = 0; // Blocking statement -- immediately
138       errorsignal_a = 1; // Critical timing on this input; assign
139           → immediately
140           errorsignal_a <= #(ct_state2_clk_a) 0; // Clear error signal
141           → after critical timing expires
142           errorsignal_b = 1; // Critical timing on this input; assign
143           → immediately
144           errorsignal_b <= #(ct_state2_clk_b) 0; // Clear error signal
145           → after critical timing expires
146   begin
147       q <= #(delay_state3_clk_q) !q;
148       cell_state = 0; // Blocking statement -- immediately
149       errorsignal_a = 1; // Critical timing on this input; assign
150           → immediately
151           errorsignal_a <= #(ct_state3_clk_a) 0; // Clear error signal
152           → after critical timing expires
153           errorsignal_b = 1; // Critical timing on this input; assign
154           → immediately
155           errorsignal_b <= #(ct_state3_clk_b) 0; // Clear error signal
156           → after critical timing expires
157       end
158   endcase
159 end
160
161 end
162
163 endmodule

```

Listing 2.20: RSFQ AND2 verilog model.

The digital simulation results for the RSFQ AND2 is shown in Fig. 2.35 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.36.

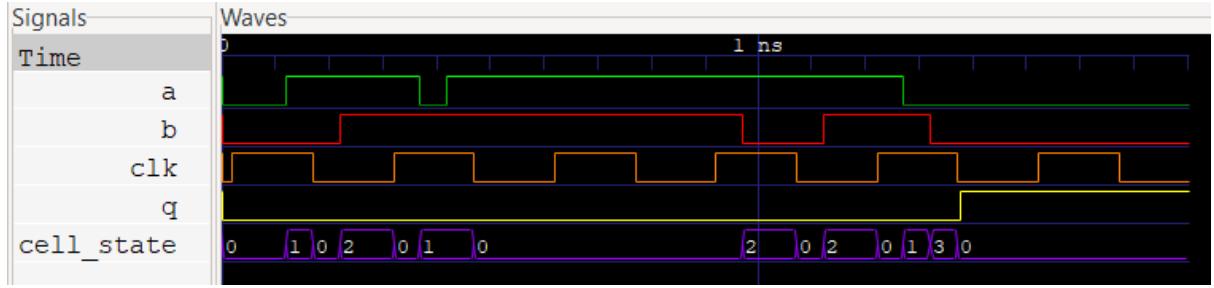


Figure 2.35: RSFQ AND2 digital simulation results.

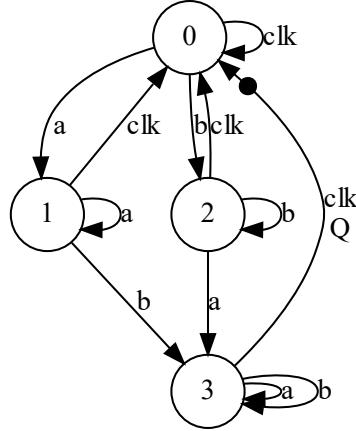


Figure 2.36: RSFQ AND2 Mealy finite state machine diagram.

Power Consumption

Table 2.20: RSFQ AND2 power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2980	5.57
2	2980	11.1
5	2980	27.8
10	2980	55.7
20	2980	111
50	2980	278

2.2.2 OR2

The RSFQ OR2 cell generates an output pulse if an input pulse from either input line was received before the clock signal. The cell is not designed to be directly connected to a PTL.

Schematic

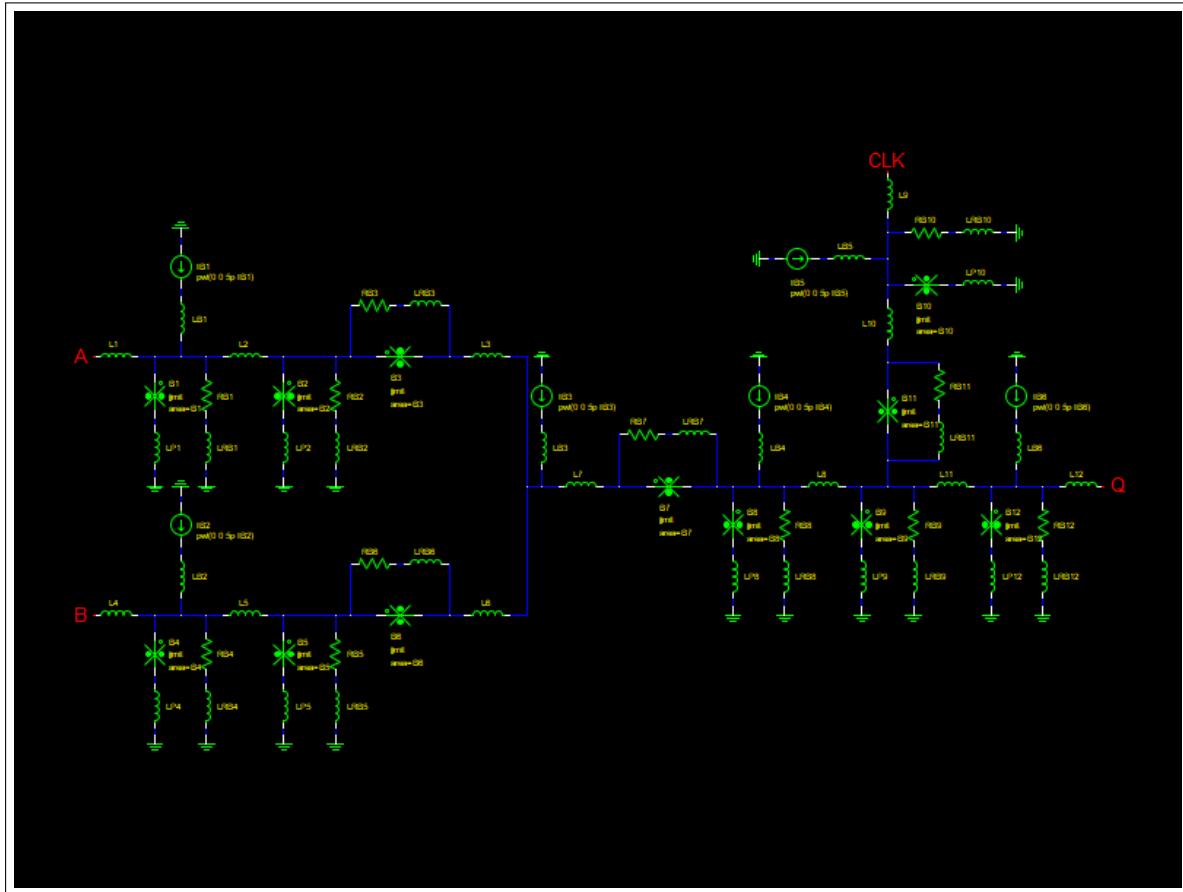


Figure 2.37: Schematic of RSFQ OR2.

Layout

The physical layout for the RSFQ OR2 is shown in Fig. 2.38. The layout height is $70 \mu\text{m}$ and the width is $40 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

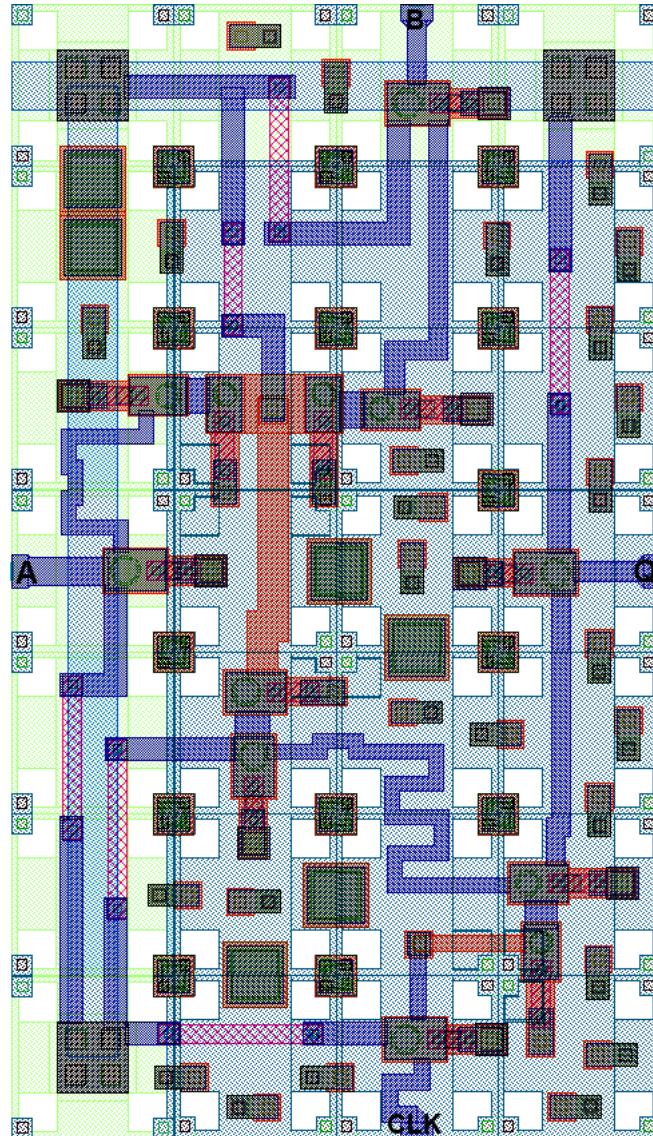


Figure 2.38: RSFQ OR2 Layout

Analog model

```

1  * Back-annotated simulation file written      64  .param LP4=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/08/07.    65  .param LP5=LP
3  * Author: L. Schindler                      66  .param LP8=LP
4  * Version: 3.0                                67  .param LP9=LP
5  * Last modification date: 4 August 2022       68  .param LP10=LP
6  * Last modification by: T. Hall                69  .param LP12=LP
7
8 *$Ports      a      b      clk      q      70
9 .subckt THmitll_OR2 a b clk q
10 .model jjmit jj(rtype=1, vg=2.8mV, cap
11   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
12   ↪ )
13 .param Phi0=2.067833848E-15
14 .param B0=1
15 .param Ic0=0.0001
16 .param IcRs=100u*6.859904418
17 .param B0Rs=IcRs/Ic0*B0
18 .param Rsheet=2
19 .param Lsheet=1.13e-12
20 .param LP=0.5p
21 .param IC=2.5
22 .param LB=2p
23 .param BiasCoef=0.7
24 .param B1=2.5
25 .param B2=1.67
26 .param B3=1.48
27 .param B4=2.5
28 .param B5=1.67
29 .param B6=1.48
30 .param B7=2.27
31 .param B8=2.36
32 .param B9=1.76
33 .param B10=2.5
34 .param B11=1.44
35 .param B12=2.5
36 .param IB1=175u
37 .param IB2=175u
38 .param IB3=283u
39 .param IB4=158u
40 .param IB5=175u
41 .param IB6=175u
42 .param LB1=LB
43 .param LB2=LB
44 .param LB3=LB
45 .param LB4=LB
46 .param LB5=LB
47 .param LB6=LB
48 .param L1=1.6049p
49 .param L2=4.4173p
50 .param L3=0.7163p
51 .param L4=1.6049p
52 .param L5=4.4173p
53 .param L6=0.7163p
54 .param L7=3.2947p
55 .param L8=8.7190p
56 .param L9=2.1422p
57 .param L10=3.7843p
58 .param L11=3.9628p
59 .param L12=1.6906p
60 .param LP1=LP
61 .param LP2=LP
62
63
64  .param LP4=LP
65  .param LP5=LP
66  .param LP8=LP
67  .param LP9=LP
68  .param LP10=LP
69  .param LP12=LP
70
71  .param RB1=B0Rs/B1
72  .param RB2=B0Rs/B2
73  .param RB3=B0Rs/B3
74  .param RB4=B0Rs/B4
75  .param RB5=B0Rs/B5
76  .param RB6=B0Rs/B6
77  .param RB7=B0Rs/B7
78  .param RB8=B0Rs/B8
79  .param RB9=B0Rs/B9
80  .param RB10=B0Rs/B10
81  .param RB11=B0Rs/B11
82  .param RB12=B0Rs/B12
83
84  .param LRB1=(RB1/Rsheet)*Lsheet+LP
85  .param LRB2=(RB2/Rsheet)*Lsheet+LP
86  .param LRB3=(RB3/Rsheet)*Lsheet
87  .param LRB4=(RB4/Rsheet)*Lsheet+LP
88  .param LRB5=(RB5/Rsheet)*Lsheet+LP
89  .param LRB6=(RB6/Rsheet)*Lsheet
90  .param LRB7=(RB7/Rsheet)*Lsheet
91  .param LRB8=(RB8/Rsheet)*Lsheet+LP
92  .param LRB9=(RB9/Rsheet)*Lsheet+LP
93  .param LRB10=(RB10/Rsheet)*Lsheet+LP
94  .param LRB11=(RB11/Rsheet)*Lsheet
95  .param LRB12=(RB12/Rsheet)*Lsheet+LP
96
97  B1 1 2 jjmit area=B1
98  B2 4 5 jjmit area=B2
99  B3 4 6 jjmit area=B3
100 B4 8 9 jjmit area=B4
101 B5 11 12 jjmit area=B5
102 B6 11 13 jjmit area=B6
103 B7 15 16 jjmit area=B7
104 B8 16 17 jjmit area=B8
105 B9 19 20 jjmit area=B9
106 B10 21 22 jjmit area=B10
107 B11 24 19 jjmit area=B11
108 B12 25 26 jjmit area=B12
109
110 IB1 0 3 pwl(0 0 5p IB1)
111 IB2 0 10 pwl(0 0 5p IB2)
112 IB3 0 14 pwl(0 0 5p IB3)
113 IB4 0 18 pwl(0 0 5p IB4)
114 IB5 0 23 pwl(0 0 5p IB5)
115 IB6 0 27 pwl(0 0 5p IB6)
116
117 LB1 3 1 LB1
118 LB2 10 8 LB2
119 LB3 14 7 LB3
120 LB4 18 16 LB4
121 LB5 23 21 LB5
122 LB6 27 25 LB6
123
124 L1 a 1 1.592E-012
125 L2 1 4 4.395E-012
126 L3 6 7 7.134E-013
127 L4 b 8 1.61E-012
128 L5 8 11 4.378E-012
129 L6 13 7 7.212E-013

```

```

130 | L7 7 15 3.29E-012
131 | L8 16 19 8.747E-012
132 | L9 clk 21 2.161E-012
133 | L10 21 24 3.766E-012
134 | L11 19 25 3.926E-012
135 | L12 25 q 1.675E-012
136 |
137 | LP1 2 0 4.683E-013
138 | LP2 5 0 4.125E-013
139 | LP4 9 0 3.472E-013
140 | LP5 12 0 4.43E-013
141 | LP8 17 0 4.666E-013
142 | LP9 20 0 4.384E-013
143 | LP10 22 0 3.63E-013
144 | LP12 26 0 4.421E-013
145 |
146 | RB1 1 101 RB1
147 | LRB1 101 0 LRB1
148 | RB2 4 104 RB2
149 | LRB2 104 0 LRB2
150 | RB3 4 106 RB3
151 | LRB3 106 6 LRB3
152 | RB4 8 108 RB4
153 | LRB4 108 0 LRB4
154 | RB5 11 111 RB5
155 | LRB5 111 0 LRB5
156 | RB6 11 113 RB6
157 | LRB6 113 13 LRB6
158 | RB7 15 115 RB7
159 | LRB7 115 16 LRB7
160 | RB8 16 116 RB8
161 | LRB8 116 0 LRB8
162 | RB9 19 119 RB9
163 | LRB9 119 0 LRB9
164 | RB10 21 121 RB10
165 | LRB10 121 0 LRB10
166 | RB11 24 124 RB11
167 | LRB11 124 19 LRB11
168 | RB12 25 125 RB12
169 | LRB12 125 0 LRB12
170 | .ends

```

Listing 2.21: RSFQ OR2 JoSIM netlist.**Table 2.21:** RSFQ OR2 pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ OR2 using JoSIM is shown in Fig. 2.39. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected to pin **q**.

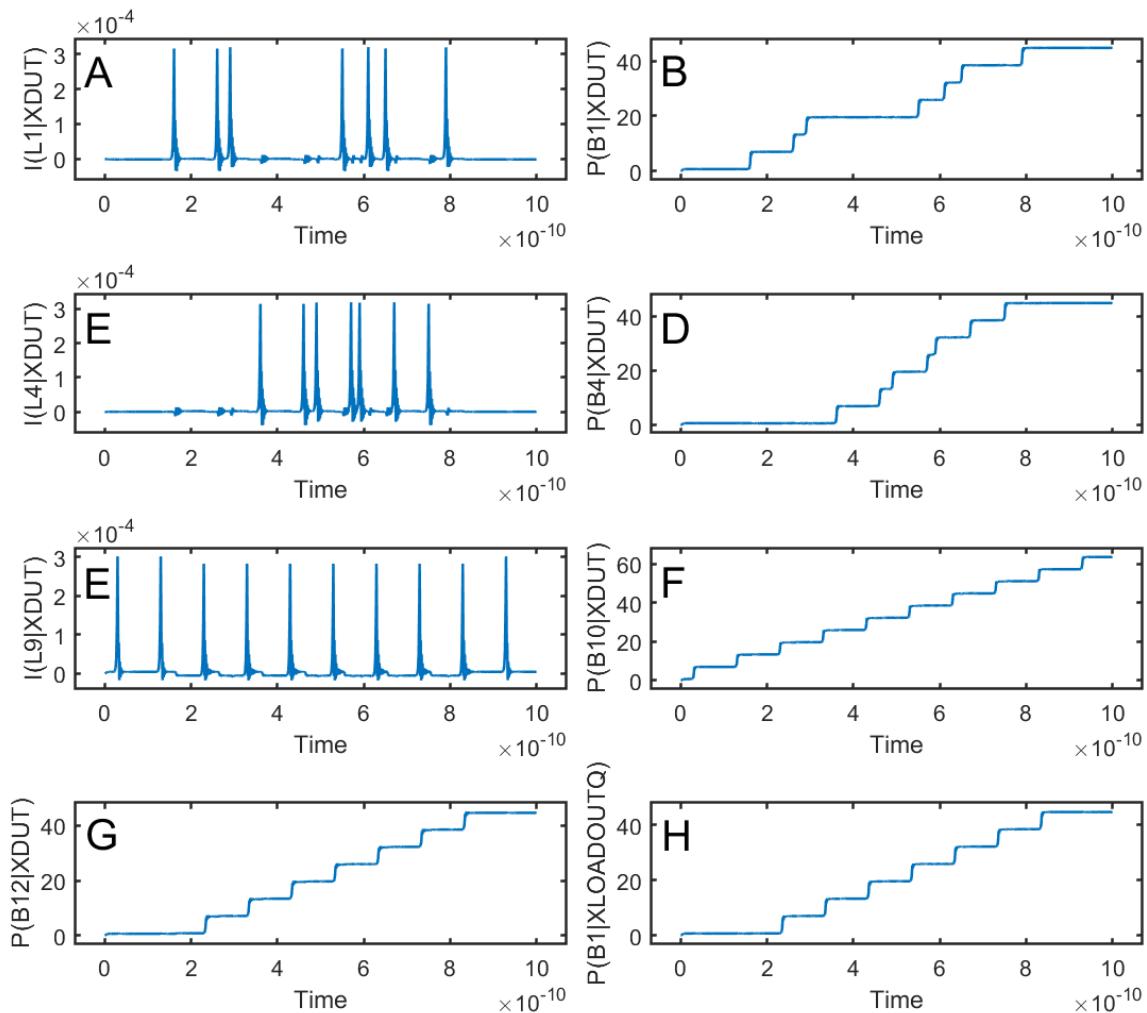


Figure 2.39: RSFQ OR2 analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 7 August 2022
5 // Last Modification by: T. Hall
6 // -----
7 `timescale 1ps/100fs
8 module THmitll_OR2_v3p0_extracted (a, b, clk, q);
9
10 input
11     a, b, clk;
12
13 output
14     q;
15
16 reg
17     q;
18
19 real
20     delay_state1_clk_q = 5.5,
21     ct_state0_a_clk = 2.9,
22     ct_state0_b_clk = 2.9,
23     ct_state1_a_clk = 3.8,
24     ct_state1_b_clk = 3.7;
25
26 reg
27     errorsignal_a,
28     errorsignal_b,
29     errorsignal_clk;
30
31 integer
32     outfile,
33     cell_state; // internal state of the cell
34
35 initial
36 begin
37     errorsignal_a = 0;
38     errorsignal_b = 0;
39     errorsignal_clk = 0;
40     cell_state = 0; // Startup state
41     q = 0; // All outputs start at 0
42 end
43
44 always @(posedge a or negedge a) // execute at positive and negative edges of input
45 begin
46     if ($time>4) // arbitrary steady-state time)
47         begin
48             if (errorsignal_a == 1'b1) // A critical timing is active for this input
49                 begin
50                     outfile = $fopen("errors.txt", "a");
51                     $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
52                                     ↪ ", $stime);
53                     $fclose(outfile);
54                     q <= 1'bX; // Set all outputs to unknown
55                 end
56             if (errorsignal_a == 0)
57                 begin
58                     case (cell_state)
59                         0: begin
60                             cell_state = 1; // Blocking statement -- immediately
61                             errorsignal_clk = 1; // Critical timing on this input; assign
62                                     ↪ immediately
63                             errorsignal_clk <= #(ct_state0_a_clk) 0; // Clear error signal
64                                     ↪ after critical timing expires
65                         end
66                     1: begin
67                         errorsignal_clk = 1; // Critical timing on this input; assign

```

```

65           → immediately
66           errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
67           → after critical timing expires
68       end
69   endcase
70 end
71
72 always @ (posedge b or negedge b) // execute at positive and negative edges of input
73 begin
74     if ($time>4) // arbitrary steady-state time)
75     begin
76         if (errorsignal_b == 1'b1) // A critical timing is active for this input
77         begin
78             outfile = $fopen("errors.txt", "a");
79             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
80             → ", $stime);
81             $fclose(outfile);
82             q <= 1'bX; // Set all outputs to unknown
83         end
84         if (errorsignal_b == 0)
85         begin
86             case (cell_state)
87                 0: begin
88                     cell_state = 1; // Blocking statement -- immediately
89                     errorsignal_clk = 1; // Critical timing on this input; assign
90                     → immediately
91                     errorsignal_clk <= #(ct_state0_b_clk) 0; // Clear error signal
92                     → after critical timing expires
93                 end
94             endcase
95         end
96     end
97 end
98
99
100 always @ (posedge clk or negedge clk) // execute at positive and negative edges of input
101 begin
102     if ($time>4) // arbitrary steady-state time)
103     begin
104         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
105         begin
106             outfile = $fopen("errors.txt", "a");
107             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
108             → ", $stime);
109             $fclose(outfile);
110             q <= 1'bX; // Set all outputs to unknown
111         end
112         if (errorsignal_clk == 0)
113         begin
114             case (cell_state)
115                 0: begin
116                     end
117                 1: begin
118                     q <= #(delay_state1_clk_q) !q;
119                     cell_state = 0; // Blocking statement -- immediately
120                     end
121             endcase
122         end
123     end
124 endmodule

```

Listing 2.22: RSFQ OR2 verilog model.

The digital simulation results for the RSFQ OR2 is shown in Fig. 2.40 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.41.

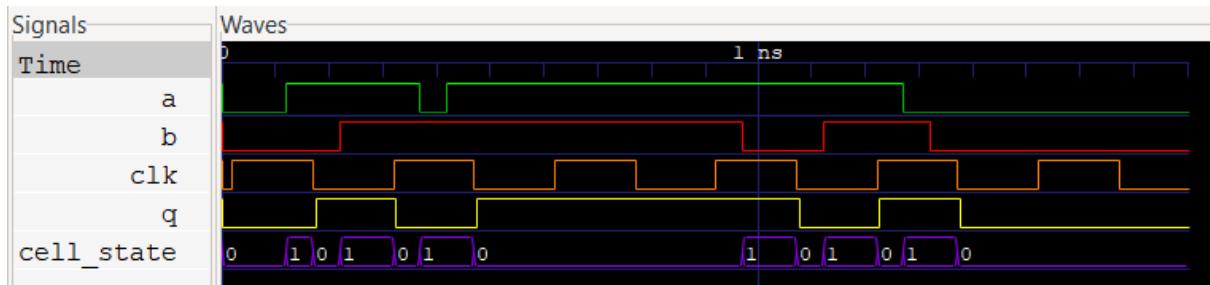


Figure 2.40: RSFQ OR2 digital simulation results.

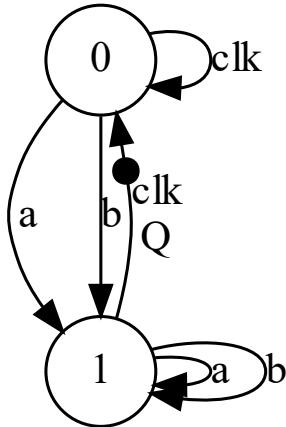


Figure 2.41: RSFQ OR2 Mealy finite state machine diagram.

Power Consumption

Table 2.22: RSFQ OR2 power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2970	4.99
2	2970	9.98
5	2970	24.9
10	2970	49.9
20	2970	99.8
50	2970	249

2.2.3 XOR

The RSFQ XOR cell generates an output pulse exclusively if a pulse from a single input line was received before the clock signal. The cell is not designed to be directly connected to a PTL.

Schematic

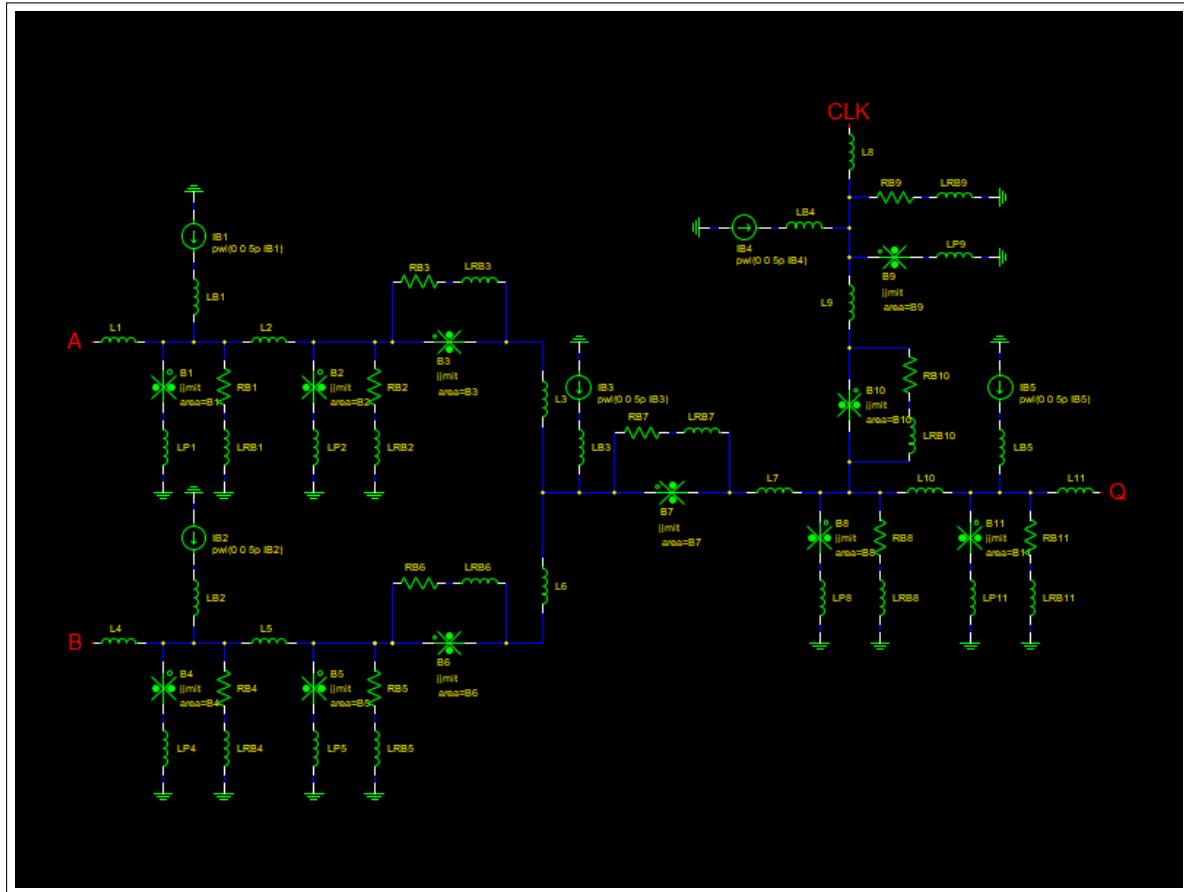


Figure 2.42: Schematic of RSFQ XOR.

Layout

The physical layout for the RSFQ XOR is shown in Fig. 2.43. The layout height is $70 \mu\text{m}$ and the width is $40 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

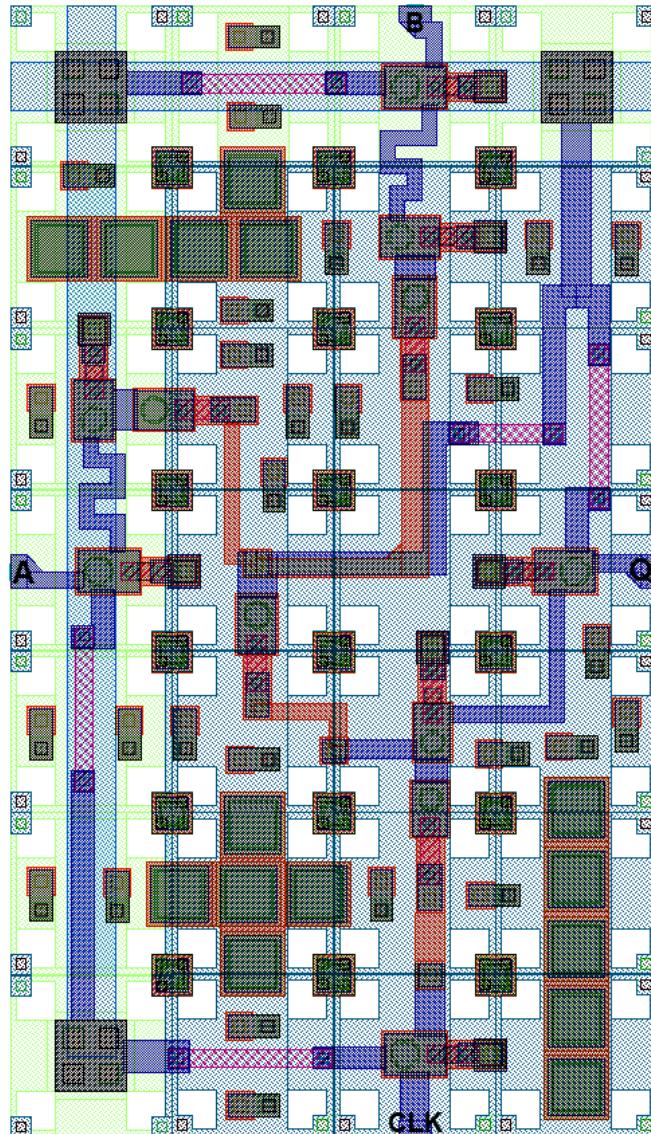


Figure 2.43: RSFQ XOR Layout.

Analog model

```

1  * Back-annotated simulation file written      64 | .param LP11=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/08/29.    65 | .param RB1=B0Rs/B1
3  * Author: L. Schindler                      66 | .param RB2=B0Rs/B2
4  * Version: 3.0                                67 | .param RB3=B0Rs/B3
5  * Last modification date: 28 August 2022     68 | .param RB4=B0Rs/B4
6  * Last modification by: T. Hall              69 | .param RB5=B0Rs/B5
7  *$Ports      a      b      clk      q      70 | .param RB6=B0Rs/B6
8  .subckt THmitll_XOR a b clk q             71 | .param RB7=B0Rs/B7
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72 | .param RB8=B0Rs/B8
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73 | .param RB9=B0Rs/B9
   ↪ )                                         74 | .param RB10=B0Rs/B10
10 .param Phi0=2.067833848E-15                75 | .param RB11=B0Rs/B11
11 .param B0=1                               76 |
12 .param Ic0=0.0001                         77 |
13 .param IcRs=100u*6.859904418               78 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
14 .param B0Rs=IcRs/Ic0*B0                   79 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
15 .param Rsheet=2                           80 | .param LRB3=(RB3/Rsheet)*Lsheet
16 .param Lsheet=1.13e-12                     81 | .param LRB4=(RB4/Rsheet)*Lsheet+LP
17 .param LP=0.5p                            82 | .param LRB5=(RB5/Rsheet)*Lsheet+LP
18 .param IC=2.5                            83 | .param LRB6=(RB6/Rsheet)*Lsheet
19 .param LB=2p                             84 | .param LRB7=(RB7/Rsheet)*Lsheet
20 .param BiasCoef=0.7                       85 | .param LRB8=(RB8/Rsheet)*Lsheet+LP
21 |                                         86 | .param LRB9=(RB9/Rsheet)*Lsheet+LP
22 .param B1=2.5                            87 | .param LRB10=(RB10/Rsheet)*Lsheet
23 .param B2=2.0                            88 | .param LRB11=(RB11/Rsheet)*Lsheet+LP
24 .param B3=2.02                           89 |
25 .param B4=2.5                            90 B1 1 2 jjmit area=B1
26 .param B5=2.0                            91 B2 4 5 jjmit area=B2
27 .param B6=2.02                           92 B3 4 6 jjmit area=B3
28 .param B7=1.96                           93 B4 8 9 jjmit area=B4
29 .param B8=1.65                           94 B5 11 12 jjmit area=B5
30 .param B9=2.5                            95 B6 11 13 jjmit area=B6
31 .param B10=1.46                          96 B7 7 15 jjmit area=B7
32 .param B11=2.5                           97 B8 16 17 jjmit area=B8
33 |                                         98 B9 18 19 jjmit area=B9
34 .param IB1=175u                           99 B10 21 16 jjmit area=B10
35 .param IB2=175u                           100 B11 22 23 jjmit area=B11
36 .param IB3=273u                           101 |
37 .param IB4=175u                           102 IB1 0 3 pwl(0 0 5p IB1)
38 .param IB5=175u                           103 IB2 0 10 pwl(0 0 5p IB2)
39 |                                         104 IB3 0 14 pwl(0 0 5p IB3)
40 .param LB1=LB                            105 IB4 0 20 pwl(0 0 5p IB4)
41 .param LB2=LB                            106 IB5 0 24 pwl(0 0 5p IB5)
42 .param LB3=LB                            107 |
43 .param LB4=LB                            108 LB1 3 1 8.314E-013
44 .param LB5=LB                            109 LB2 10 8 9.179E-013
45 |                                         110 LB3 14 7 3.234E-012
46 .param L1=1.5740p                         111 LB4 20 18 1.047E-012
47 .param L2=3.1407p                         112 LB5 24 22 1.004E-012
48 .param L3=4.7381p                         113 |
49 .param L4=1.5740p                         114 L1 a 1 1.57E-012
50 .param L5=3.1407p                         115 L2 1 4 3.128E-012
51 .param L6=4.7381p                         116 L3 6 7 4.746E-012
52 .param L7=4.7751p                         117 L4 b 8 1.578E-012
53 .param L8=1.1983p                         118 L5 8 11 3.145E-012
54 .param L9=3.2191p                         119 L6 7 13 4.763E-012
55 .param L10=3.7711p                        120 L7 15 16 4.74E-012
56 .param L11=1.4703p                        121 L8 clk 18 1.196E-012
57 |                                         122 L9 18 21 3.224E-012
58 .param LP1=LP                            123 L10 16 22 3.775E-012
59 .param LP2=LP                            124 L11 22 q 1.459E-012
60 .param LP4=LP                            125 |
61 .param LP5=LP                            126 LP1 2 0 4.215E-013
62 .param LP8=LP                            127 LP2 5 0 4.657E-013
63 .param LP9=LP                            128 LP4 9 0 3.32E-013
64 |                                         129 LP5 12 0 3.87E-013

```

```

130 | LP8 17 0 4.698E-013
131 | LP9 19 0 3.611E-013
132 | LP11 23 0 4.394E-013
133 |
134 | RB1 1 101 RB1
135 | LRB1 101 0 LRB1
136 | RB2 4 104 RB2
137 | LRB2 104 0 LRB2
138 | RB3 4 106 RB3
139 | LRB3 106 6 LRB3
140 | RB4 8 108 RB4
141 | LRB4 108 0 LRB4
142 | RB5 11 111 RB5
143 | LRB5 111 0 LRB5
144 | RB6 11 113 RB6
145 | LRB6 113 13 LRB6
146 | RB7 7 115 RB7
147 | LRB7 115 15 LRB7
148 | RB8 16 116 RB8
149 | LRB8 116 0 LRB8
150 | RB9 18 118 RB9
151 | LRB9 118 0 LRB9
152 | RB10 21 121 RB10
153 | LRB10 121 16 LRB10
154 | RB11 22 122 RB11
155 | LRB11 122 0 LRB11
156 | .ends

```

Listing 2.23: RSFQ XOR JoSIM netlist.**Table 2.23:** RSFQ XOR pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ XOR using JoSIM is shown in Fig. 2.44. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected to pin **q**.

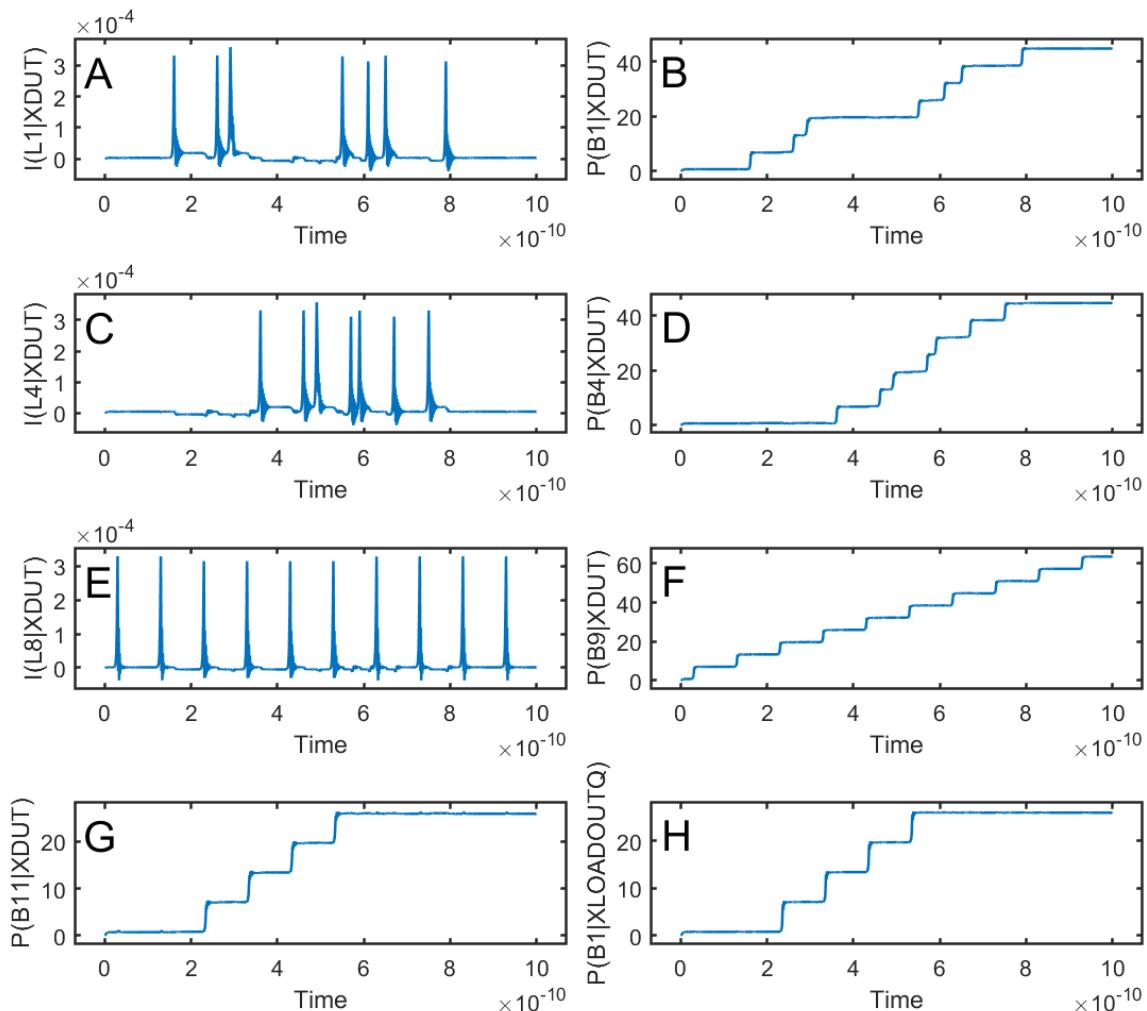


Figure 2.44: RSFQ XOR analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 29 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_XOR_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 5.0,
21   delay_state2_clk_q = 5.0,
22   ct_state0_a_clk = 0.5,
23   ct_state0_b_clk = 0.4,
24   ct_state1_a_b = 8.0,
25   ct_state1_a_clk = 7.3,
26   ct_state1_b_b = 5.2,
27   ct_state1_clk_b = 5.9,
28   ct_state2_a_a = 5.2,
29   ct_state2_b_a = 7.7,
30   ct_state2_b_clk = 7.0,
31   ct_state2_clk_a = 6.1;
32
33 reg
34   errorsignal_a,
35   errorsignal_b,
36   errorsignal_clk;
37
38 integer
39   outfile,
40   cell_state; // internal state of the cell
41
42 initial
43 begin
44   errorsignal_a = 0;
45   errorsignal_b = 0;
46   errorsignal_clk = 0;
47   cell_state = 0; // Startup state
48   q = 0; // All outputs start at 0
49 end
50
51 always @(posedge a or negedge a) // execute at positive and negative edges of input
52 begin
53   if ($time>4) // arbitrary steady-state time)
54     begin
55       if (errorsignal_a == 1'b1) // A critical timing is active for this input
56         begin
57           outfile = $fopen("errors.txt", "a");
58           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
59             ↪ ", $stime);
60           $fclose(outfile);
61           q <= 1'bX; // Set all outputs to unknown
62         end
63       if (errorsignal_a == 0)
64         begin
65           case (cell_state)
66             0: begin
67               cell_state = 1; // Blocking statement -- immediately

```

```

67          errorsignal_clk = 1; // Critical timing on this input; assign
68          ↪ immediately
69      end
70  1: begin
71          errorsignal_b = 1; // Critical timing on this input; assign
72          ↪ immediately
73          errorsignal_b <= #(ct_state1_a_b) 0; // Clear error signal
74          ↪ after critical timing expires
75      end
76  2: begin
77          cell_state = 0; // Blocking statement -- immediately
78          errorsignal_a = 1; // Critical timing on this input; assign
79          ↪ immediately
80          errorsignal_a <= #(ct_state2_a_a) 0; // Clear error signal
81          ↪ after critical timing expires
82      end
83  end
84 end
85
86 always @(posedge b or negedge b) // execute at positive and negative edges of input
87 begin
88     if ($time>4) // arbitrary steady-state time)
89     begin
90         if (errorsignal_b == 1'b1) // A critical timing is active for this input
91         begin
92             outfile = $fopen("errors.txt", "a");
93             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
94             ↪ ", $stime);
95             $fclose(outfile);
96             q <= 1'bX; // Set all outputs to unknown
97         end
98         if (errorsignal_b == 0)
99         begin
100            case (cell_state)
101                0: begin
102                    cell_state = 2; // Blocking statement -- immediately
103                    errorsignal_clk = 1; // Critical timing on this input; assign
104                    ↪ immediately
105                    errorsignal_clk <= #(ct_state0_b_clk) 0; // Clear error signal
106                    ↪ after critical timing expires
107                end
108                1: begin
109                    cell_state = 0; // Blocking statement -- immediately
110                    errorsignal_b = 1; // Critical timing on this input; assign
111                    ↪ immediately
112                    errorsignal_b <= #(ct_state1_b_b) 0; // Clear error signal
113                    ↪ after critical timing expires
114                end
115            end
116        endcase
117    end
118 end
119

```

```

120
121 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
122   begin
123     if ($time>4) // arbitrary steady-state time)
124       begin
125         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
126           begin
127             outfile = $fopen("errors.txt", "a");
128             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
129                         ↪ ", $time);
130             $fclose(outfile);
131             q <= 1'bX; // Set all outputs to unknown
132           end
133         if (errorsignal_clk == 0)
134           begin
135             case (cell_state)
136               0: begin
137                 end
138               1: begin
139                 q <= #(delay_state1_clk_q) !q;
140                 cell_state = 0; // Blocking statement -- immediately
141                 errorsignal_b = 1; // Critical timing on this input; assign
142                               ↪ immediately
143                 errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
144                               ↪ after critical timing expires
145               end
146               2: begin
147                 q <= #(delay_state2_clk_q) !q;
148                 cell_state = 0; // Blocking statement -- immediately
149                 errorsignal_a = 1; // Critical timing on this input; assign
150                               ↪ immediately
151                 errorsignal_a <= #(ct_state2_clk_a) 0; // Clear error signal
152                               ↪ after critical timing expires
153               end
154             endcase
155           end
156         end
157       end
158     end
159   endmodule

```

Listing 2.24: RSFQ XOR verilog model.

The digital simulation results for the RSFQ XOR is shown in Fig. 2.45 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.46.



Figure 2.45: RSFQ XOR digital simulation results.

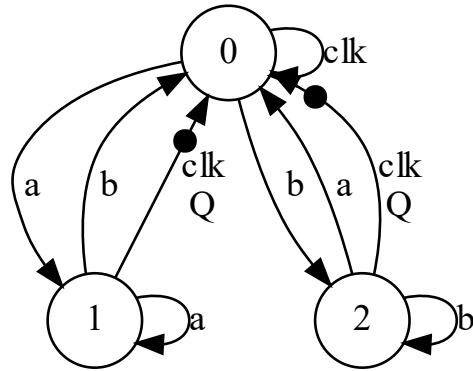


Figure 2.46: RSFQ XOR Mealy finite state machine diagram.

Power Consumption

Table 2.24: RSFQ XOR power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2530	4.78
2	2530	9.56
5	2530	23.9
10	2530	47.8
20	2530	95.6
50	2530	239

2.2.4 NOT

The RSFQ NOT cell is a signal inverting cell driven by a clock pulse signal line. The cell is not designed to be directly connected to a PTL.

Schematic

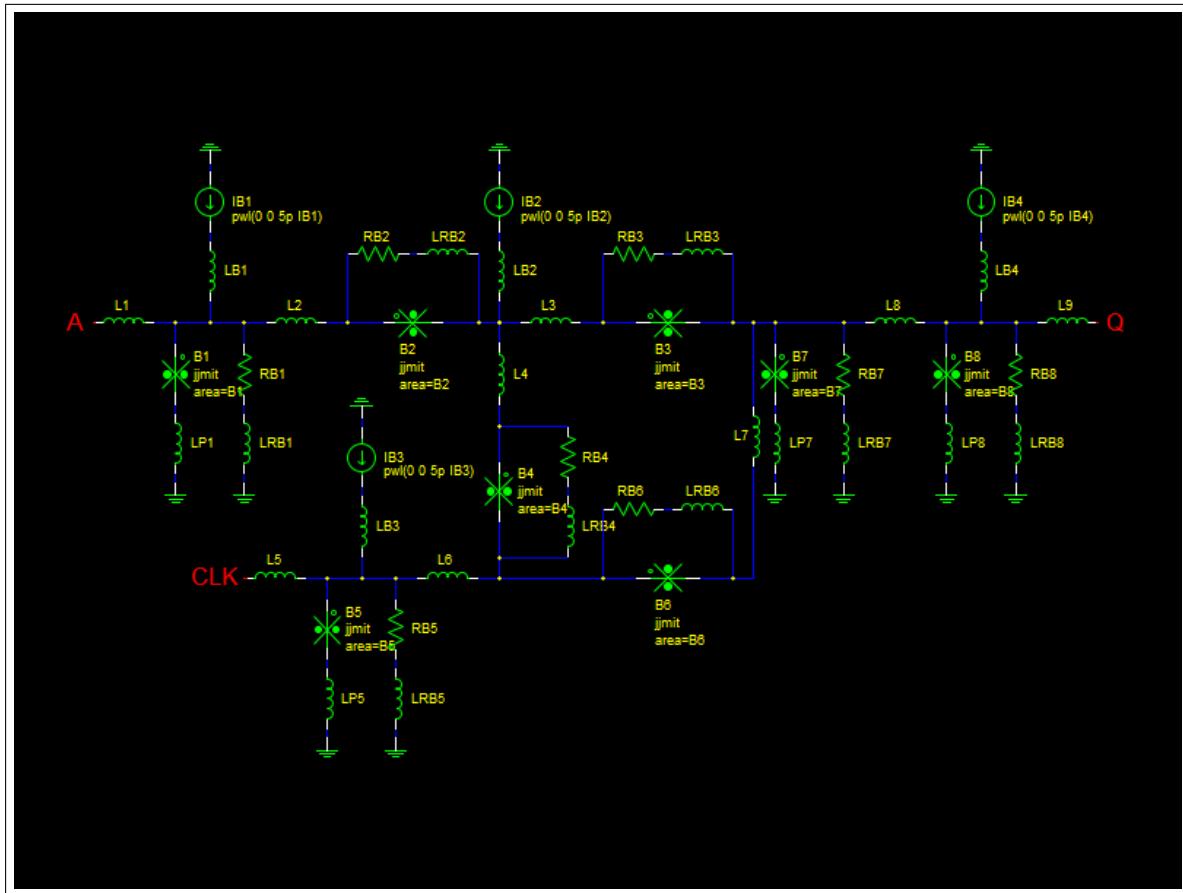


Figure 2.47: Schematic of RSFQ NOT.

Layout

The physical layout of the RSFQ NOT is shown in Fig. 2.48. The layout height is $70 \mu\text{m}$ and the width is $40 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

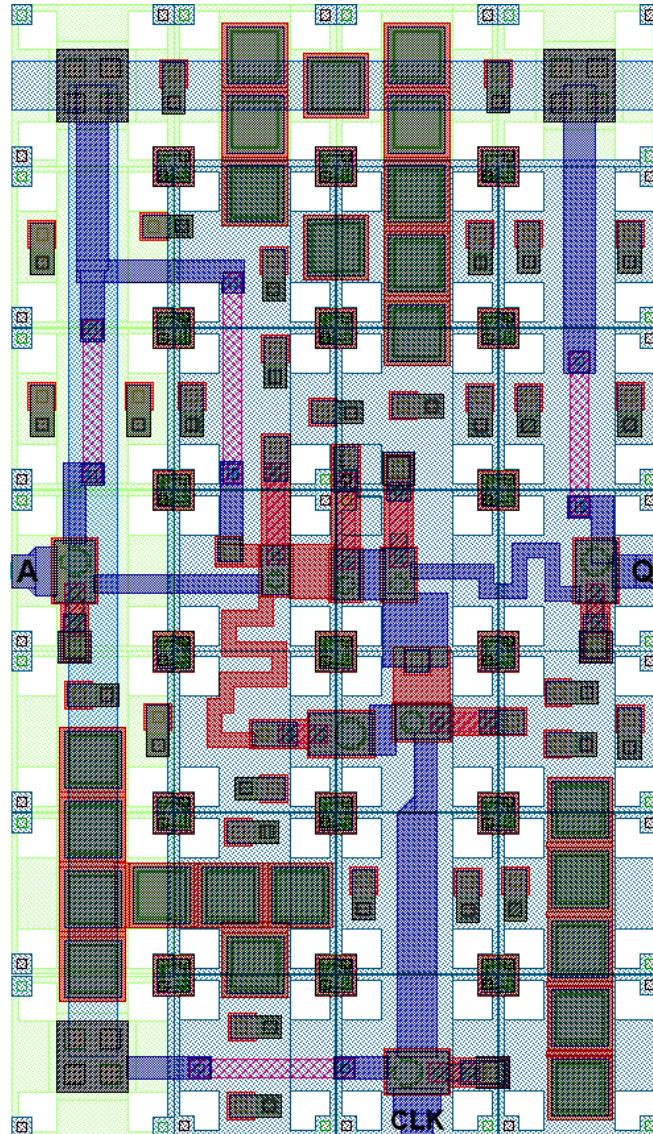


Figure 2.48: RSFQ NOT Layout.

Analog model

```

1  * Back-annotated simulation file written      63 | .param RB8=B0Rs/B8
2  *   ↪ by InductEx v.6.1.52 on 2022/08/25.    64 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
3  * Author: T. Hall                            65 | .param LRB2=(RB2/Rsheet)*Lsheet
4  * Version: 3.0                               66 | .param LRB3=(RB3/Rsheet)*Lsheet
5  * Last modification date: 24 August 2022     67 | .param LRB4=(RB4/Rsheet)*Lsheet
6  * Last modification by: T. Hall              68 | .param LRB5=(RB5/Rsheet)*Lsheet+LP
7  *$Ports      a      clk      q               69 | .param LRB6=(RB6/Rsheet)*Lsheet
8  .subckt THmitll_NOT a clk q                70 | .param LRB7=(RB7/Rsheet)*Lsheet+LP
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    71 | .param LRB8=(RB8/Rsheet)*Lsheet+LP
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    72 |
   ↪ )                                         73
10 .param Phi0=2.067833848E-15                 74 B1 1 2 jjmit area=B1
11 .param B0=1                                 75 B2 4 5 jjmit area=B2
12 .param Ic0=0.0001                           76 B3 7 8 jjmit area=B3
13 .param IcRs=100u*6.859904418                77 B4 9 10 jjmit area=B4
14 .param B0Rs=IcRs/Ic0*B0                     78 B5 11 12 jjmit area=B5
15 .param Rsheet=2                             79 B6 10 14 jjmit area=B6
16 .param Lsheet=1.13e-12                      80 B7 8 15 jjmit area=B7
17 .param LP=0.5p                             81 B8 16 17 jjmit area=B8
18 .param IC=2.5                               82
19 .param LB=2p                                83 IB1 0 3 pwl(0 0 5p IB1)
20 .param BiasCoef=0.7                         84 IB2 0 6 pwl(0 0 5p IB2)
21                                         85 IB3 0 13 pwl(0 0 5p IB3)
22 .param B1=2.5                               86 IB4 0 18 pwl(0 0 5p IB4)
23 .param B2=0.78                             87
24 .param B3=0.85                             88 LB1 3 1 1.246E-012
25 .param B4=2.69                             89 LB2 6 5 1.707E-012
26 .param B5=2.5                               90 LB3 13 11 8.002E-013
27 .param B6=1.42                             91 LB4 18 16 8.582E-013
28 .param B7=1.01                             92
29 .param B8=2.5                               93 L1 a 1 8.521E-013
30                                         94 L2 1 4 2.756E-012
31 .param IB1=175u                            95 L3 5 7 7.55E-013
32 .param IB2=131u                            96 L4 5 9 7.358E-012
33 .param IB3=175u                            97 L5 clk 11 8.595E-013
34 .param IB4=175u                            98 L6 11 10 3.051E-012
35                                         99 L7 8 14 9.435E-013
36 .param LB1=LB                             100 L8 8 16 4.287E-012
37 .param LB2=LB                             101 L9 16 q 9.3E-013
38 .param LB3=LB                             102
39 .param LB4=LB                             103 LP1 2 0 3.288E-013
40                                         104 LP5 12 0 3.499E-013
41 .param L1=0.8555p                         105 LP7 15 0 4.831E-013
42 .param L2=2.7537p                         106 LP8 17 0 3.407E-013
43 .param L3=0.7553p                         107
44 .param L4=7.3609p                          108 RB1 1 101 RB1
45 .param L5=0.8585p                          109 LRB1 101 0 LRB1
46 .param L6=3.0349p                          110 RB2 4 104 RB2
47 .param L7=0.9373p                          111 LRB2 104 5 LRB2
48 .param L8=4.2782p                          112 RB3 7 107 RB3
49 .param L9=0.9209p                          113 LRB3 107 8 LRB3
50                                         114 RB4 9 109 RB4
51 .param LP1=LP                            115 LRB4 109 10 LRB4
52 .param LP5=LP                            116 RB5 11 111 RB5
53 .param LP7=LP                            117 LRB5 111 0 LRB5
54 .param LP8=LP                            118 RB6 10 110 RB6
55                                         119 LRB6 110 14 LRB6
56 .param RB1=B0Rs/B1                      120 RB7 8 108 RB7
57 .param RB2=B0Rs/B2                      121 LRB7 108 0 LRB7
58 .param RB3=B0Rs/B3                      122 RB8 16 116 RB8
59 .param RB4=B0Rs/B4                      123 LRB8 116 0 LRB8
60 .param RB5=B0Rs/B5                      124 .ends
61 .param RB6=B0Rs/B6
62 .param RB7=B0Rs/B7

```

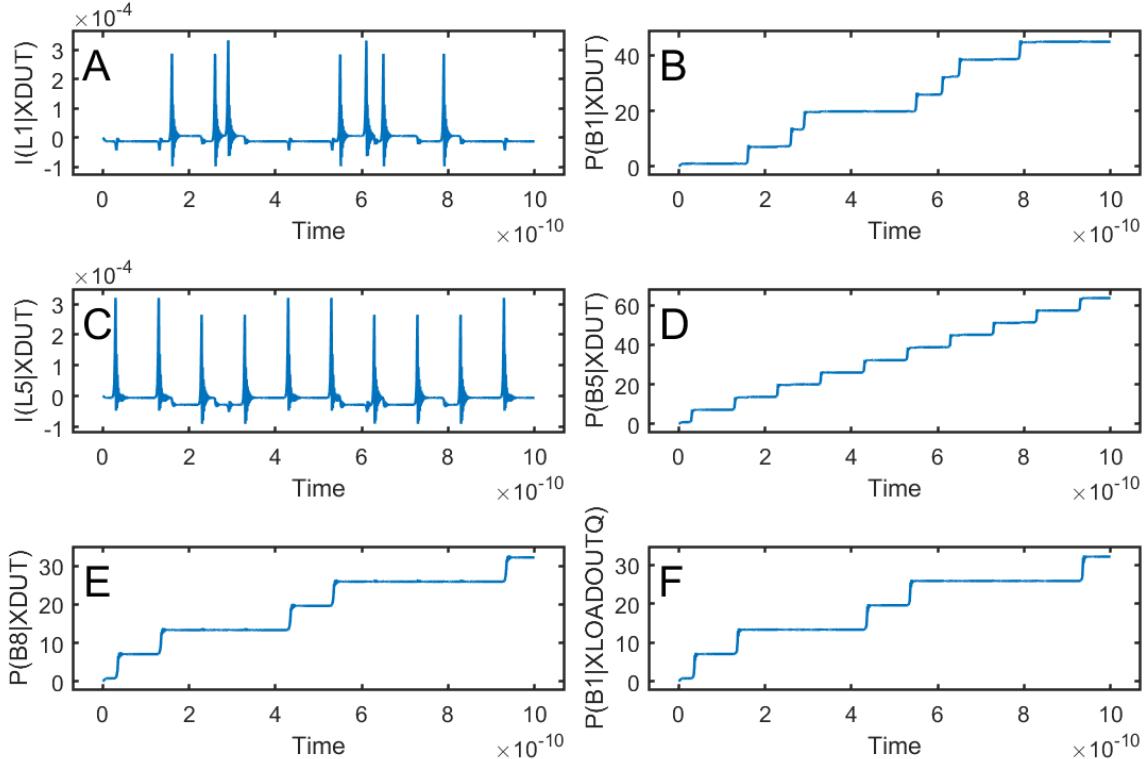
Listing 2.25: RSFQ NOT JoSIM netlist.

Table 2.25: RSFQ NOT pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ NOT using JoSIM is shown in Fig. 2.49. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **clk**,
- (d) the phase over the input JJ of pin **clk**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load circuit connected to pin **q**.

**Figure 2.49:** RSFQ NOT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 25 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_NOT_v3p0_extracted (a, clk, q);
9
10 input
11   a, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_clk_q = 5.5,
21   ct_state0_a_clk = 0.8,
22   ct_state0_clk_a = 4.5,
23   ct_state0_clk_clk = 5.2,
24   ct_state1_a_clk = 2.1;
25
26 reg
27   errorsignal_a,
28   errorsignal_clk;
29
30 integer
31   outfile,
32   cell_state; // internal state of the cell
33
34 initial
35 begin
36   errorsignal_a = 0;
37   errorsignal_clk = 0;
38   cell_state = 0; // Startup state
39   q = 0; // All outputs start at 0
40 end
41
42 always @ (posedge a or negedge a) // execute at positive and negative edges of input
43 begin
44   if ($time > 4) // arbitrary steady-state time)
45     begin
46       if (errorsignal_a == 1'b1) // A critical timing is active for this input
47         begin
48           outfile = $fopen("errors.txt", "a");
49           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
50           ↪ ", $stime);
51           $fclose(outfile);
52           q <= 1'bX; // Set all outputs to unknown
53         end
54       if (errorsignal_a == 0)
55         begin
56           case (cell_state)
57             0: begin
58               cell_state = 1; // Blocking statement -- immediately
59               errorsignal_clk = 1; // Critical timing on this input; assign
59               ↪ immediately
60               errorsignal_clk <= #(ct_state0_a_clk) 0; // Clear error signal
60               ↪ after critical timing expires
61             end
62             1: begin
63               errorsignal_clk = 1; // Critical timing on this input; assign
63               ↪ immediately
64               errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
64             end
65           endcase
66         end
67       end
68     end
69   end
70 endmodule

```

```

64           end
65       endcase
66   end
67 end
68
69
70 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
71 begin
72   if ($time>4) // arbitrary steady-state time)
73     begin
74       if (errorsignal_clk == 1'b1) // A critical timing is active for this input
75         begin
76           outfile = $fopen("errors.txt", "a");
77           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
78           ↪ ", $stime);
79           $fclose(outfile);
80           q <= 1'bX; // Set all outputs to unknown
81         end
82       if (errorsignal_clk == 0)
83         begin
84           case (cell_state)
85             0: begin
86               q <= #(delay_state0_clk_q) !q;
87               errorsignal_a = 1; // Critical timing on this input; assign
88               ↪ immediately
89               errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
90               ↪ after critical timing expires
91               errorsignal_clk = 1; // Critical timing on this input; assign
92               ↪ immediately
93               errorsignal_clk <= #(ct_state0_clk_clk) 0; // Clear error
94               ↪ signal after critical timing expires
95             end
96           1: begin
97             cell_state = 0; // Blocking statement -- immediately
98           end
99         endcase
100      end
101    end
102  endmodule

```

Listing 2.26: RSFQ NOT verilog model.

The digital simulation results for the RSFQ NOT is shown in Fig. 2.50 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.51.

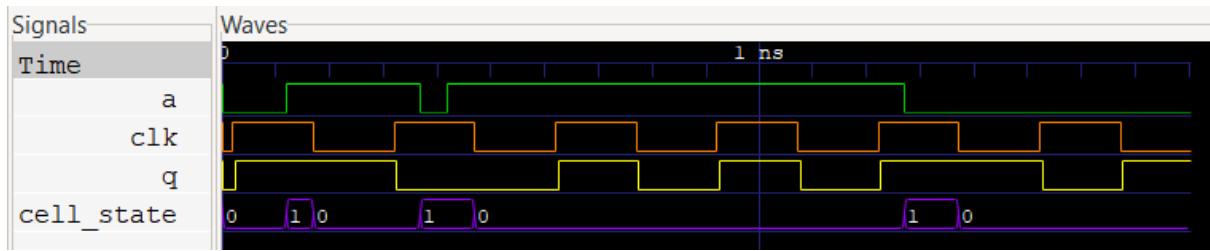


Figure 2.50: RSFQ NOT digital simulation results.

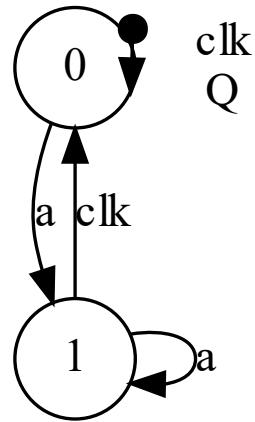


Figure 2.51: RSFQ NOT Mealy finite state machine diagram.

Power Consumption

Table 2.26: RSFQ NOT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1710	2.95
2	1710	5.89
5	1710	14.7
10	1710	29.5
20	1710	58.9
50	1710	147

2.2.5 XNOR

The RSFQ XNOR cell is a combination of a NOT and XOR cell. It generates an output pulse exclusively if no input pulse was received or if a pulse from both input lines was received before the clock signal. The cell is not designed to be directly connected to a PTL.

Schematic

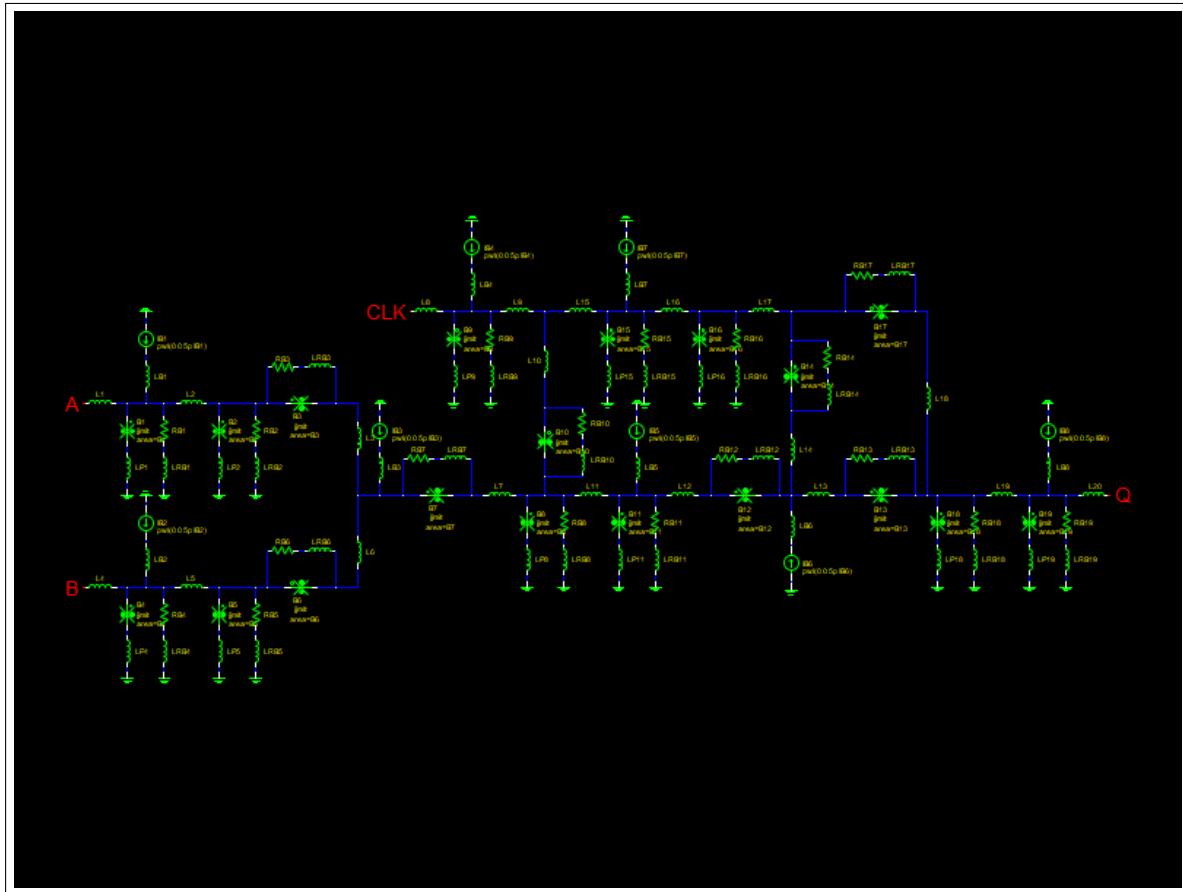


Figure 2.52: Schematic of RSFQ XNOR.

Layout

The physical layout for the RSFQ XNOR is shown in Fig. 2.53. The layout height is $70 \mu m$ and the width is $60 \mu m$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

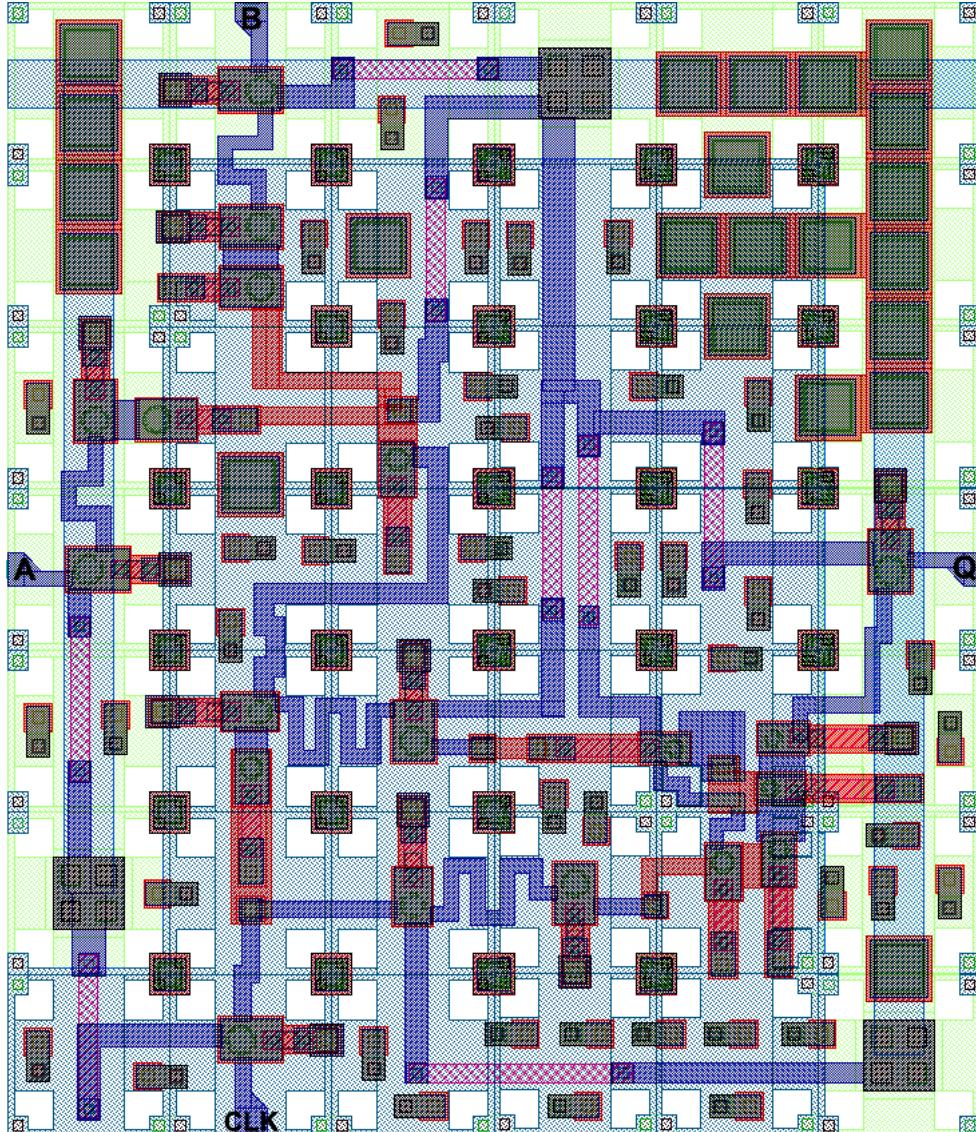


Figure 2.53: RSFQ XNOR Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param L5=2.7700p
2  *   ↪ by InductEx v.6.1.52 on 2022/09/07.    65  .param L6=3.6981p
3  * Author: L. Schindler                      66  .param L7=6.0060p
4  * Version: 3.0                                67  .param L8=1.5890p
5  * Last modification date: 6 September 2022   68  .param L9=1.8231p
6  * Last modification by: T. Hall              69  .param L10=1.6294p
7  *$Ports      a      b      clk      q      70  .param L11=4.5825p
8  .subckt THmitll_XNOR a b clk q            71  .param L12=3.3983p
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param L13=1.1575p
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param L14=3.0580p
   ↪ )                                         74  .param L15=2.1812p
10 .param Phi0=2.067833848E-15                75  .param L16=4.5604p
11 .param B0=1                                  76  .param L17=2.9745p
12 .param Ic0=0.0001                            77  .param L18=0.8577p
13 .param IcRs=100u*6.859904418               78  .param L19=3.5636p
14 .param B0Rs=IcRs/Ic0*B0                     79  .param L20=1.5943p
15 .param Rsheet=2                             80
16 .param Lsheet=1.13e-12                       81  .param LP1=LP
17 .param LP=0.5p                             82  .param LP2=LP
18 .param IC=2.5                               83  .param LP4=LP
19 .param LB=2p                                84  .param LP5=LP
20 .param BiasCoef=0.7                         85  .param LP8=LP
21
22 .param B1=2.5                               86  .param LP9=LP
23 .param B2=2.22                             87  .param LP11=LP
24 .param B3=2.12                             88  .param LP15=LP
25 .param B4=2.5                               89  .param LP16=LP
26 .param B5=2.22                             90  .param LP18=LP
27 .param B6=2.12                             91  .param LP19=LP
28 .param B7=1.39                               92
29 .param B8=1.57                               93  .param RB1=B0Rs/B1
30 .param B9=2.5                               94  .param RB2=B0Rs/B2
31 .param B10=1.28                             95  .param RB3=B0Rs/B3
32 .param B11=2.43                             96  .param RB4=B0Rs/B4
33 .param B12=0.77                             97  .param RB5=B0Rs/B5
34 .param B13=0.72                             98  .param RB6=B0Rs/B6
35 .param B14=1.34                             99  .param RB7=B0Rs/B7
36 .param B15=1.63                             100 .param RB8=B0Rs/B8
37 .param B16=2.15                             101 .param RB9=B0Rs/B9
38 .param B17=1.05                             102 .param RB10=B0Rs/B10
39 .param B18=0.83                             103 .param RB11=B0Rs/B11
40 .param B19=2.5                               104 .param RB12=B0Rs/B12
41
42 .param IB1=175u                             105 .param RB13=B0Rs/B13
43 .param IB2=175u                             106 .param RB14=B0Rs/B14
44 .param IB3=207u                             107 .param RB15=B0Rs/B15
45 .param IB4=175u                             108 .param RB16=B0Rs/B16
46 .param IB5=193u                             109 .param RB17=B0Rs/B17
47 .param IB6=147u                             110 .param RB18=B0Rs/B18
48 .param IB7=122u                             111 .param RB19=B0Rs/B19
49 .param IB8=175u                             112 .param LRB1=(RB1/Rsheet)*Lsheet+LP
50
51 .param LB1=LB                               113 .param LRB2=(RB2/Rsheet)*Lsheet+LP
52 .param LB2=LB                               114 .param LRB3=(RB3/Rsheet)*Lsheet
53 .param LB3=LB                               115 .param LRB4=(RB4/Rsheet)*Lsheet+LP
54 .param LB4=LB                               116 .param LRB5=(RB5/Rsheet)*Lsheet+LP
55 .param LB5=LB                               117 .param LRB6=(RB6/Rsheet)*Lsheet
56 .param LB6=LB                               118 .param LRB7=(RB7/Rsheet)*Lsheet
57 .param LB7=LB                               119 .param LRB8=(RB8/Rsheet)*Lsheet+LP
58 .param LB8=LB                               120 .param LRB9=(RB9/Rsheet)*Lsheet+LP
59
60 .param L1=1.4696p                           121 .param LRB10=(RB10/Rsheet)*Lsheet
61 .param L2=2.7700p                           122 .param LRB11=(RB11/Rsheet)*Lsheet+LP
62 .param L3=3.6981p                           123 .param LRB12=(RB12/Rsheet)*Lsheet
63 .param L4=1.4696p                           124 .param LRB13=(RB13/Rsheet)*Lsheet
                                         125 .param LRB14=(RB14/Rsheet)*Lsheet
                                         126 .param LRB15=(RB15/Rsheet)*Lsheet+LP
                                         127 .param LRB16=(RB16/Rsheet)*Lsheet+LP
                                         128 .param LRB17=(RB17/Rsheet)*Lsheet
                                         129 .param LRB18=(RB18/Rsheet)*Lsheet+LP

```

```

130 | .param LRB19=(RB19/Rsheet)*Lsheet+LP          187 | L18 38 30 8.576E-013
131 | B1 1 2 jjmit area=B1                         188 | L19 30 40 3.531E-012
132 | B2 4 5 jjmit area=B2                         189 | L20 40 q 1.583E-012
133 | B3 4 6 jjmit area=B3                         190
134 | B4 8 9 jjmit area=B4                         191 | LP1 2 0 4.616E-013
135 | B5 11 12 jjmit area=B5                        192 | LP2 5 0 4.744E-013
136 | B6 11 13 jjmit area=B6                        193 | LP4 9 0 3.882E-013
137 | B7 7 15 jjmit area=B7                        194 | LP5 12 0 3.984E-013
138 | B8 16 17 jjmit area=B8                        195 | LP8 17 0 4.778E-013
139 | B9 18 19 jjmit area=B9                        196 | LP9 19 0 3.834E-013
140 | B10 22 16 jjmit area=B10                       197 | LP11 24 0 4.104E-013
141 | B11 23 24 jjmit area=B11                      198 | LP15 34 0 5.341E-013
142 | B12 26 27 jjmit area=B12                      199 | LP16 37 0 3.884E-013
143 | B13 29 30 jjmit area=B13                      200 | LP18 39 0 4.944E-013
144 | B14 32 31 jjmit area=B14                      201 | LP19 41 0 3.606E-013
145 | B15 33 34 jjmit area=B15                      202
146 | B16 36 37 jjmit area=B16                      203 | RB1 1 101 RB1
147 | B17 32 38 jjmit area=B17                      204 | LRB1 101 0 LRB1
148 | B18 30 39 jjmit area=B18                      205 | RB2 4 104 RB2
149 | B19 40 41 jjmit area=B19                      206 | LRB2 104 0 LRB2
150 |
151 |
152 | IB1 0 3 pwl(0 0 5p IB1)                      207 | RB3 4 106 RB3
153 | IB2 0 10 pwl(0 0 5p IB2)                     208 | LRB3 106 6 LRB3
154 | IB3 0 14 pwl(0 0 5p IB3)                     209 | RB4 8 108 RB4
155 | IB4 0 20 pwl(0 0 5p IB4)                     210 | LRB4 108 0 LRB4
156 | IB5 0 25 pwl(0 0 5p IB5)                     211 | RB5 11 111 RB5
157 | IB6 0 28 pwl(0 0 5p IB6)                     212 | LRB5 111 0 LRB5
158 | IB7 0 35 pwl(0 0 5p IB7)                     213 | RB6 11 113 RB6
159 | IB8 0 42 pwl(0 0 5p IB8)                     214 | LRB6 113 13 LRB6
160 |
161 | LB1 3 1 5.929E-013                           215 | RB7 7 115 RB7
162 | LB2 10 8 1.279E-012                          216 | LRB7 115 15 LRB7
163 | LB3 14 7 1.737E-012                          217 | RB8 16 116 RB8
164 | LB4 20 18 2.846E-012                          218 | LRB8 116 0 LRB8
165 | LB5 25 23 3.286E-012                          219 | RB9 18 118 RB9
166 | LB6 27 28 2.4E-012                           220 | LRB9 118 0 LRB9
167 | LB7 35 33 1.996E-012                          221 | RB10 22 122 RB10
168 | LB8 42 40 2.415E-012                          222 | LRB10 122 16 LRB10
169 |
170 | L1 a 1 1.471E-012                           223 | RB11 23 123 RB11
171 | L2 1 4 2.745E-012                           224 | LRB11 123 0 LRB11
172 | L3 6 7 3.693E-012                           225 | RB12 26 126 RB12
173 | L4 b 8 1.476E-012                           226 | LRB12 126 27 LRB12
174 | L5 8 11 2.749E-012                          227 | RB13 29 129 RB13
175 | L6 7 13 3.671E-012                          228 | LRB13 129 30 LRB13
176 | L7 15 16 5.95E-012                           229 | RB14 32 131 RB14
177 | L8 clk 18 1.58E-012                          230 | LRB14 131 31 LRB14
178 | L9 18 21 1.818E-012                          231 | RB15 33 133 RB15
179 | L10 21 22 1.634E-012                          232 | LRB15 133 0 LRB15
180 | L11 16 23 4.569E-012                          233 | RB16 36 136 RB16
181 | L12 23 26 3.384E-012                          234 | LRB16 136 0 LRB16
182 | L13 27 29 1.168E-012                          235 | RB17 32 138 RB17
183 | L14 31 27 3.042E-012                          236 | LRB17 138 38 LRB17
184 | L15 21 33 2.198E-012                          237 | RB18 30 130 RB18
185 | L16 33 36 4.555E-012                          238 | LRB18 130 0 LRB18
186 | L17 36 32 2.964E-012                          239 | RB19 40 140 RB19
187 | .ends

```

Listing 2.27: RSFQ XNOR JoSIM netlist.**Table 2.27:** RSFQ XNOR pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ XNOR using JoSIM is shown in Fig. 2.54. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected to pin **q**.

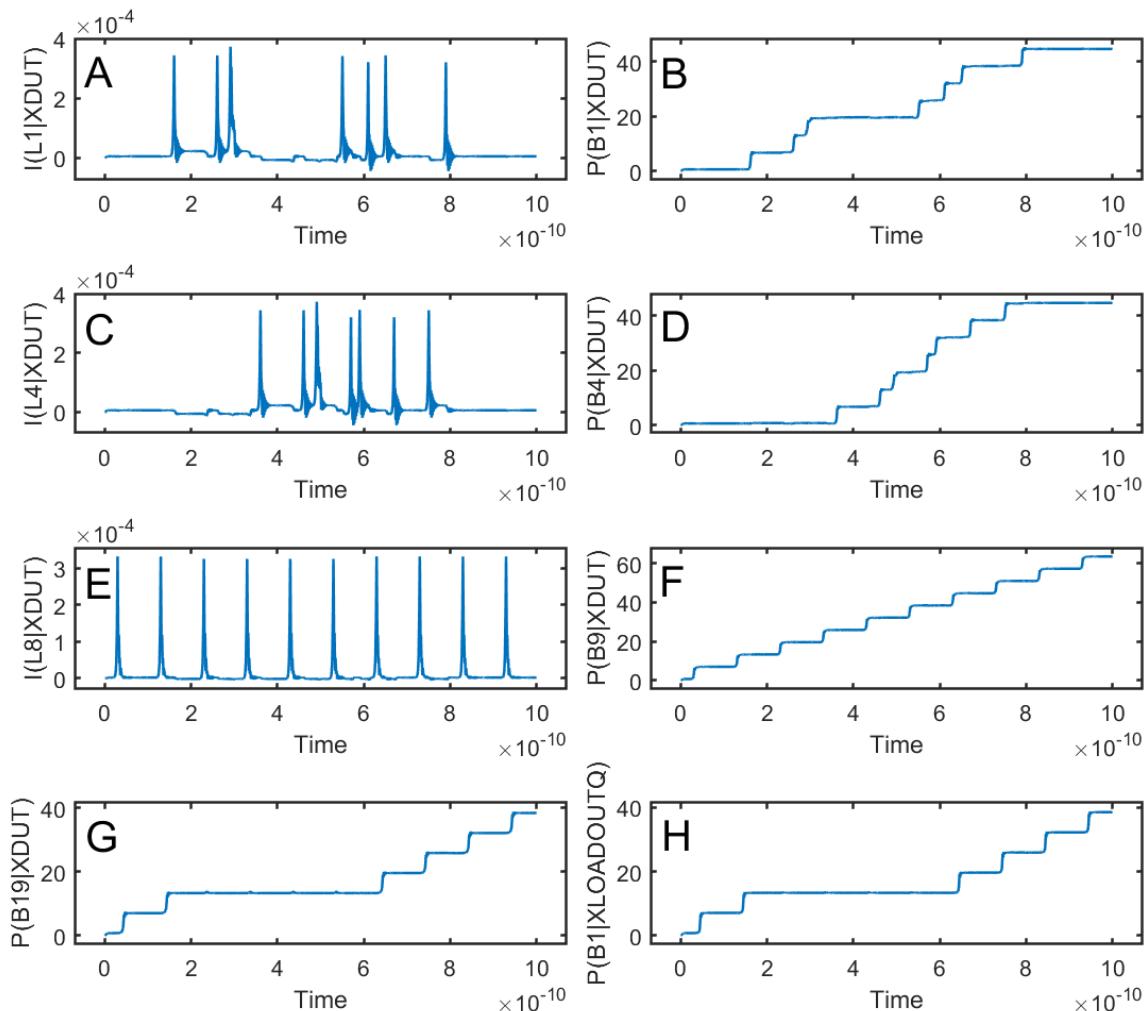


Figure 2.54: RSFQ XNOR analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 7 September 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_XNOR_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_clk_q = 14.3,
21   ct_state0_clk_a = 1.3,
22   ct_state0_clk_b = 1.2,
23   ct_state0_clk_clk = 10.5,
24   ct_state1_a_b = 9.2,
25   ct_state1_a_clk = 7.3,
26   ct_state1_b_b = 5.2,
27   ct_state1_clk_b = 7.7,
28   ct_state2_a_a = 5.2,
29   ct_state2_b_a = 9.2,
30   ct_state2_b_clk = 7.4,
31   ct_state2_clk_a = 7.7;
32
33 reg
34   errorsignal_a,
35   errorsignal_b,
36   errorsignal_clk;
37
38 integer
39   outfile,
40   cell_state; // internal state of the cell
41
42 initial
43 begin
44   errorsignal_a = 0;
45   errorsignal_b = 0;
46   errorsignal_clk = 0;
47   cell_state = 0; // Startup state
48   q = 0; // All outputs start at 0
49 end
50
51 always @(posedge a or negedge a) // execute at positive and negative edges of input
52 begin
53   if ($time>4) // arbitrary steady-state time)
54     begin
55       if (errorsignal_a == 1'b1) // A critical timing is active for this input
56         begin
57           outfile = $fopen("errors.txt", "a");
58           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
59             ↪ ", $stime);
60           $fclose(outfile);
61           q <= 1'bX; // Set all outputs to unknown
62         end
63       if (errorsignal_a == 0)
64         begin
65           case (cell_state)
66             0: begin
67               cell_state = 1; // Blocking statement -- immediately

```

```

67          end
68      1: begin
69          errorsignal_b = 1; // Critical timing on this input; assign
70          // immediately
71          errorsignal_b <= #(ct_state1_a_b) 0; // Clear error signal
72          // after critical timing expires
73          errorsignal_clk = 1; // Critical timing on this input; assign
74          // immediately
75          errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
76          // after critical timing expires
77      end
78  2: begin
79      cell_state = 0; // Blocking statement -- immediately
80      errorsignal_a = 1; // Critical timing on this input; assign
81      // immediately
82      errorsignal_a <= #(ct_state2_a_a) 0; // Clear error signal
83      // after critical timing expires
84      end
85  endcase
86 end
87
88 always @(posedge b or negedge b) // execute at positive and negative edges of input
89 begin
90     if ($time>4) // arbitrary steady-state time)
91     begin
92         if (errorsignal_b == 1'b1) // A critical timing is active for this input
93         begin
94             outfile = $fopen("errors.txt", "a");
95             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
96             // ", $stime);
97             $fclose(outfile);
98             q <= 1'bX; // Set all outputs to unknown
99         end
100        if (errorsignal_b == 0)
101        begin
102            case (cell_state)
103                0: begin
104                    cell_state = 2; // Blocking statement -- immediately
105                end
106                1: begin
107                    cell_state = 0; // Blocking statement -- immediately
108                    errorsignal_b = 1; // Critical timing on this input; assign
109                    // immediately
110                    errorsignal_b <= #(ct_state1_b_b) 0; // Clear error signal
111                    // after critical timing expires
112                end
113            endcase
114        end
115    end
116
117 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
118 begin
119     if ($time>4) // arbitrary steady-state time)
120     begin
121         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
122         begin
123             outfile = $fopen("errors.txt", "a");

```

```

124          $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
125                      ↪ ", $stime);
126          $fclose(outfile);
127          q <= 1'bX; // Set all outputs to unknown
128      end
129      if (errorsignal_clk == 0)
130      begin
131          case (cell_state)
132          0: begin
133              q <= #(delay_state0_clk_q) !q;
134              errorsignal_a = 1; // Critical timing on this input; assign
135                      ↪ immediately
136              errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
137                      ↪ after critical timing expires
138              errorsignal_b = 1; // Critical timing on this input; assign
139                      ↪ immediately
140              errorsignal_b <= #(ct_state0_clk_b) 0; // Clear error signal
141                      ↪ after critical timing expires
142              errorsignal_clk = 1; // Critical timing on this input; assign
143                      ↪ immediately
144              errorsignal_clk <= #(ct_state0_clk_clk) 0; // Clear error
145                      ↪ signal after critical timing expires
146          end
147          1: begin
148              cell_state = 0; // Blocking statement -- immediately
149              errorsignal_b = 1; // Critical timing on this input; assign
150                      ↪ immediately
151              errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
152                      ↪ after critical timing expires
153          end
154      endcase
155  end

```

Listing 2.28: RSFQ XNOR verilog model.

The digital simulation results for the RSFQ XNOR is shown in Fig. 2.55 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.56.



Figure 2.55: RSFQ XNOR digital simulation results.

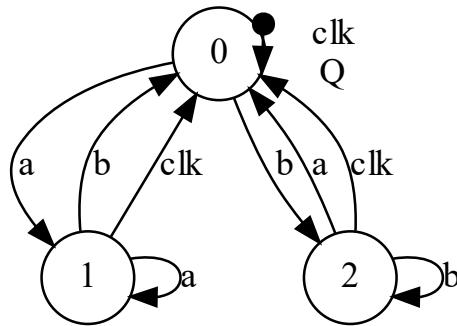


Figure 2.56: RSFQ XNOR Mealy finite state machine diagram.

Power Consumption

Table 2.28: RSFQ XNOR power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	3560	7.00
2	3560	14.0
5	3560	35.0
10	3560	70.0
20	3560	140
50	3560	350

2.3 Buffers

2.3.1 DFF

The RSFQ DFF, D flip-flop, is a multi-state device used to transmit an input set pulse synchronised with a reset (typically clock) signal. The cell is not designed to be directly connected to a PTL.

Schematic

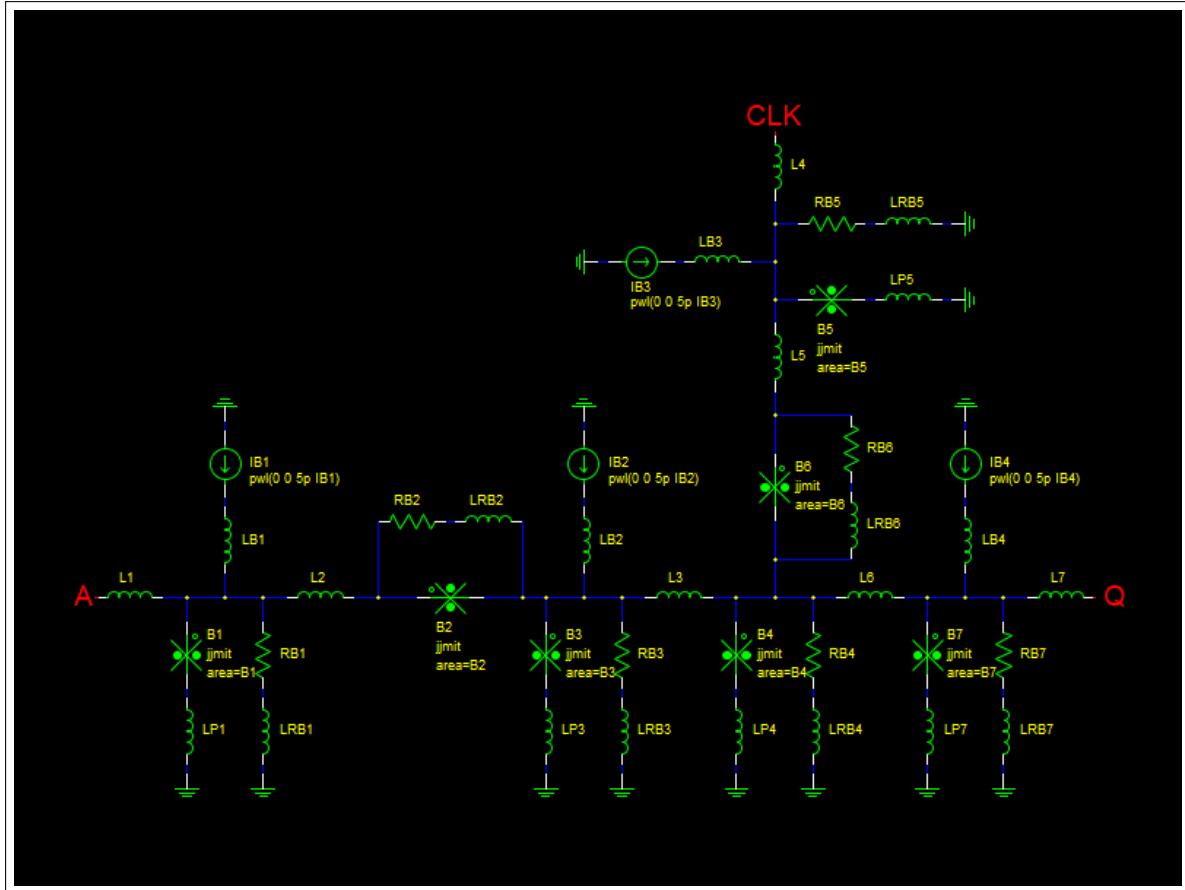


Figure 2.57: Schematic of RSFQ DFF.

Layout

The physical layout for the RSFQ DFF is shown in Fig. 2.58. The layout height is $70 \mu\text{m}$ and the width is $30 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

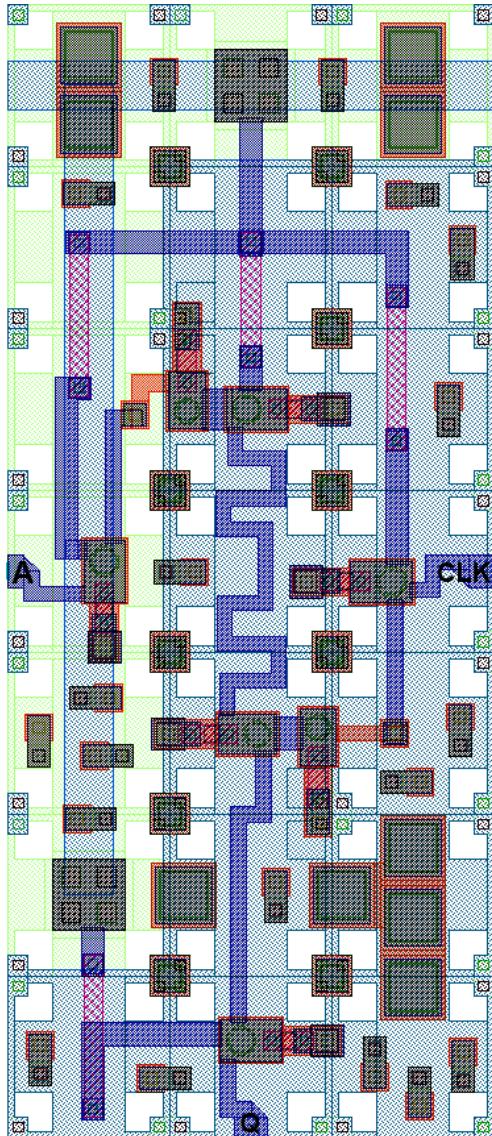


Figure 2.58: RSFQ DFF Layout.

Analog model

```

1  * Back-annotated simulation file written      59  .param RB6=B0Rs/B6
2   ↪ by InductEx v.6.1.52 on 2022/08/02.    60  .param RB7=B0Rs/B7
3  * Author: L. Schindler                   61
4  * Version: 3.0                         62  .param LRB1=(RB1/Rsheet)*Lsheet+LP
5  * Last modification date: 1 August 2022  63  .param LRB2=(RB2/Rsheet)*Lsheet
6  * Last modification by: T. Hall        64  .param LRB3=(RB3/Rsheet)*Lsheet+LP
7  *$Ports      a      clk      q          65  .param LRB4=(RB4/Rsheet)*Lsheet+LP
8  .subckt THmitll_DFF a clk q           66  .param LRB5=(RB5/Rsheet)*Lsheet+LP
9  .model jjmit jj(rtype=1, vg=2.8mV, cap  67  .param LRB6=(RB6/Rsheet)*Lsheet
10  ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA 68  .param LRB7=(RB7/Rsheet)*Lsheet+LP
11  ↪ )
12  .param Phi0=2.067833848E-15            69
13  .param B0=1                           70  B1 1 2 jjmit area=B1
14  .param Ic0=0.0001                     71  B2 4 5 jjmit area=B2
15  .param IcRs=100u*6.859904418          72  B3 5 6 jjmit area=B3
16  .param B0Rs=IcRs/Ic0*B0              73  B4 8 9 jjmit area=B4
17  .param Rsheet=2                      74  B5 10 11 jjmit area=B5
18  .param Lsheet=1.13e-12                75  B6 13 8 jjmit area=B6
19  .param LP=0.5p                       76  B7 14 15 jjmit area=B7
20  .param IC=2.5                        77
21  .param LB=2p                         78  IB1 0 3 pwl(0 0 5p IB1)
22  .param BiasCoef=0.7                 79  IB2 0 7 pwl(0 0 5p IB2)
23  .param B1=2.5                        80  IB3 0 12 pwl(0 0 5p IB3)
24  .param B2=1.67                       81  IB4 0 16 pwl(0 0 5p IB4)
25  .param B3=2.32                       82
26  .param B4=2.02                       83  LB1 3 1 LB1
27  .param B5=2.5                        84  LB2 7 5 LB2
28  .param B6=1.69                       85  LB3 12 10 LB3
29  .param B7=2.5                        86  LB4 16 14 LB4
30  .param IB1=175u                      87
31  .param IB2=222u                      88  L1 a 1 1.948E-012
32  .param IB3=175u                      89  L2 1 4 3.879E-012
33  .param IB4=175u                      90  L3 5 8 8.641E-012
34                                91  L4 clk 10 2.035E-012
35  .param LB1=LB                        92  L5 10 13 3.799E-012
36  .param LB2=LB                        93  L6 8 14 4.675E-012
37  .param LB3=LB                        94  L7 14 q 1.809E-012
38  .param LB4=LB                        95
39                                96  LP1 2 0 3.511E-013
40  .param L1=1.9553p                   97  LP3 6 0 3.717E-013
41  .param L2=3.8899p                   98  LP4 9 0 4.668E-013
42  .param L3=8.6023p                   99  LP5 11 0 4.339E-013
43  .param L4=2.0461p                   100 LP7 15 0 4.147E-013
44  .param L5=3.8124p                   101
45  .param L6=4.6626p                   102 RB1 1 101 RB1
46  .param L7=1.8248p                   103 LRB1 101 0 LRB1
47                                104 RB2 4 104 RB2
48  .param LP1=LP                      105 LRB2 104 5 LRB2
49  .param LP3=LP                      106 RB3 5 105 RB3
50  .param LP4=LP                      107 LRB3 105 0 LRB3
51  .param LP5=LP                      108 RB4 8 108 RB4
52  .param LP7=LP                      109 LRB4 108 0 LRB4
53                                110 RB5 10 110 RB5
54  .param RB1=B0Rs/B1                111 LRB5 110 0 LRB5
55  .param RB2=B0Rs/B2                112 RB6 13 113 RB6
56  .param RB3=B0Rs/B3                113 LRB6 113 8 LRB6
57  .param RB4=B0Rs/B4                114 RB7 14 114 RB7
58  .param RB5=B0Rs/B5                115 LRB7 114 0 LRB7
59                                116 .ends

```

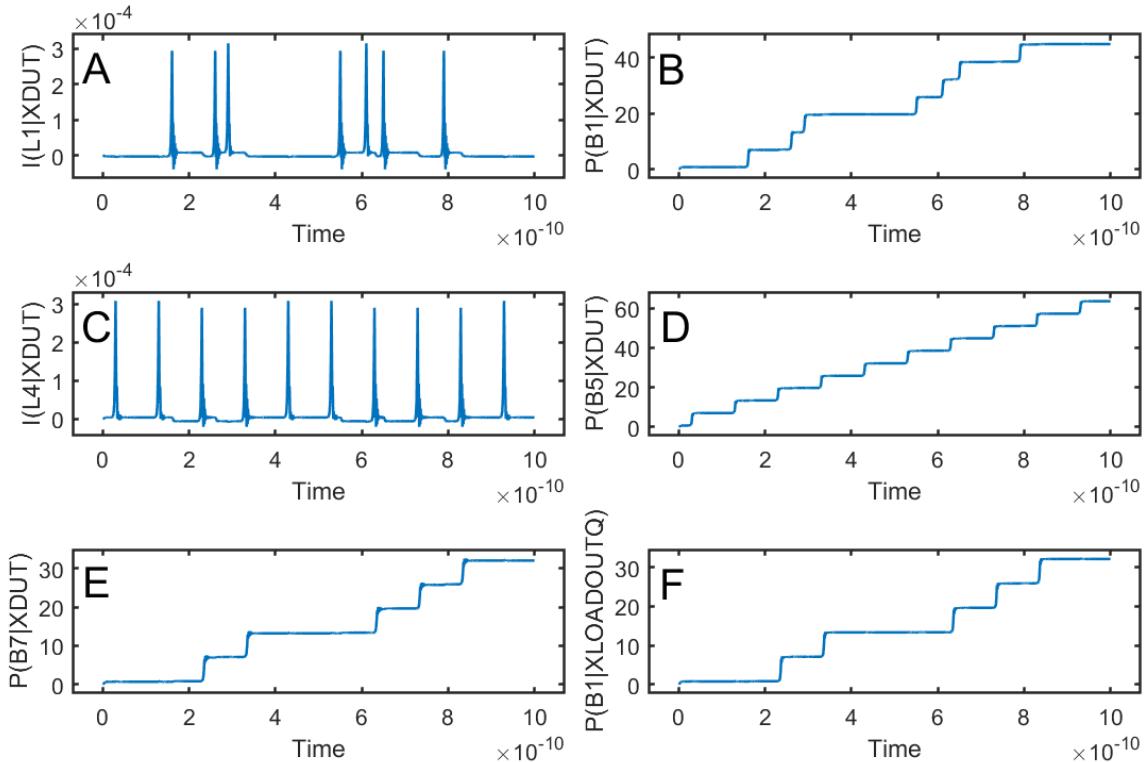
Listing 2.29: RSFQ DFF JoSIM netlist.

Table 2.29: RSFQ DFF pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ DFF using JoSIM is shown in Fig. 2.59. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **clk**,
- (d) the phase over the input JJ of pin **clk**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load circuit connected to pin **q**.

**Figure 2.59:** RSFQ DFF analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 2 August 2022
5 // Last Modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_DFF_v3p0_extracted (a, clk, q);
9
10 input
11   a, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 6.3,
21   ct_state0_clk_a = 0.4;
22
23 reg
24   errorsignal_a,
25   errorsignal_clk;
26
27 integer
28   outfile,
29   cell_state; // internal state of the cell
30
31 initial
32 begin
33   errorsignal_a = 0;
34   errorsignal_clk = 0;
35   cell_state = 0; // Startup state
36   q = 0; // All outputs start at 0
37 end
38
39 always @(posedge a or negedge a) // execute at positive and negative edges of input
40 begin
41   if ($time>4) // arbitrary steady-state time)
42     begin
43       if (errorsignal_a == 1'b1) // A critical timing is active for this input
44         begin
45           outfile = $fopen("errors.txt", "a");
46           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
47             ↪ ", $stime);
48           $fclose(outfile);
49           q <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               cell_state = 1; // Blocking statement -- immediately
56             end
57             1: begin
58               end
59             endcase
60           end
61         end
62     end
63   always @(posedge clk or negedge clk) // execute at positive and negative edges of input
64   begin
65     if ($time>4) // arbitrary steady-state time)
66       begin

```

```

67      if (errorsignal_clk == 1'b1) // A critical timing is active for this input
68      begin
69          outfile = $fopen("errors.txt", "a");
70          $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
71                      ↪ ", $stime);
72          $fclose(outfile);
73          q <= 1'bX; // Set all outputs to unknown
74      end
75      if (errorsignal_clk == 0)
76      begin
77          case (cell_state)
78              0: begin
79                  errorsignal_a = 1; // Critical timing on this input; assign
79                  ↪ immediately
80                  errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
80                  ↪ after critical timing expires
81              end
82              1: begin
83                  q <= #(delay_state1_clk_q) !q;
83                  cell_state = 0; // Blocking statement -- immediately
84                  end
85          endcase
86      end
87  end
88
89
90 endmodule

```

Listing 2.30: RSFQ DFF verilog model.

The digital simulation results for the RSFQ DFF is shown in Fig. 2.60 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 2.61.

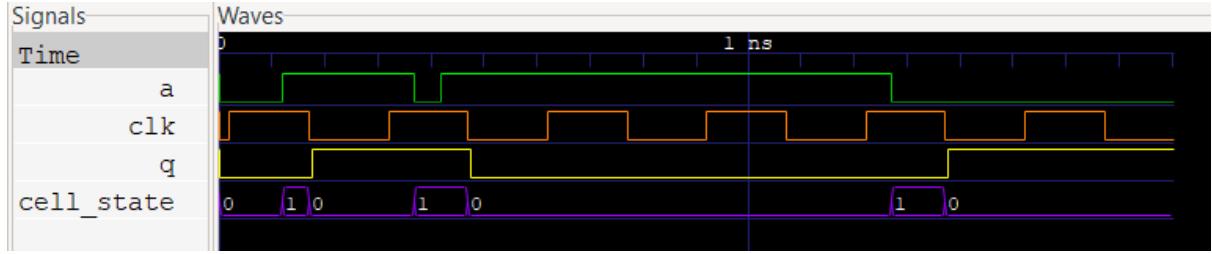


Figure 2.60: RSFQ DFF digital simulation results.

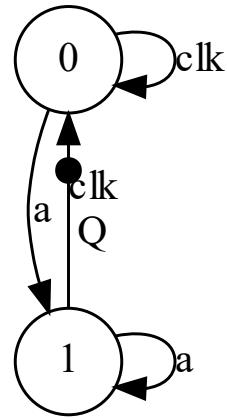


Figure 2.61: RSFQ DFF Mealy finite state machine diagram.

Power Consumption

Table 2.30: RSFQ DFF power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1940	3.14
2	1940	6.29
5	1940	15.7
10	1940	31.4
20	1940	62.9
50	1940	157

2.3.2 NDRO

The NDRO, non-destructive readout, cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDRO will generate an output pulse after each clock signal until an input reset signal is received. The cell is not designed to be directly connected to a PTL.

Schematic

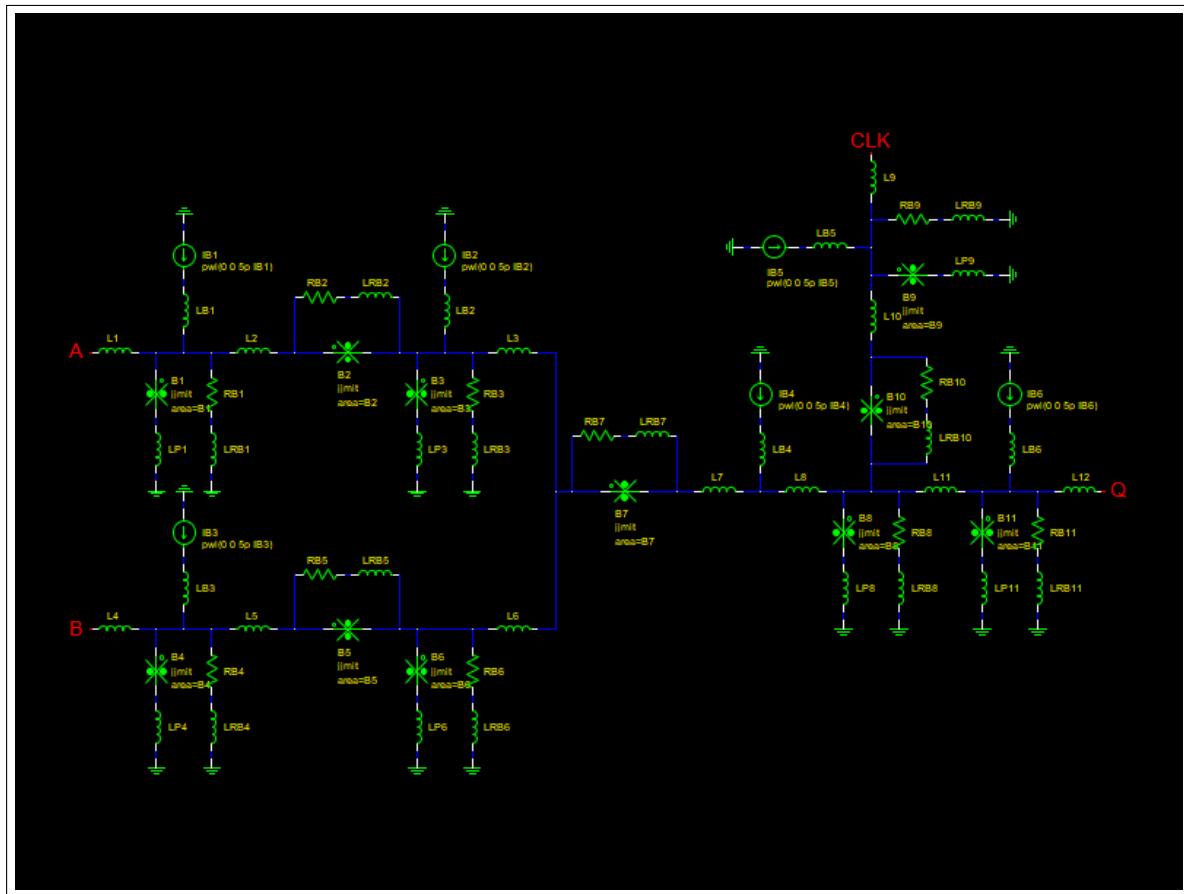


Figure 2.62: Schematic of RSFQ NDRO.

Layout

The physical layout of the RSFQ NDRO is shown in Fig. 2.63. The layout height is $70 \mu\text{m}$ and the width is $40 \mu\text{m}$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

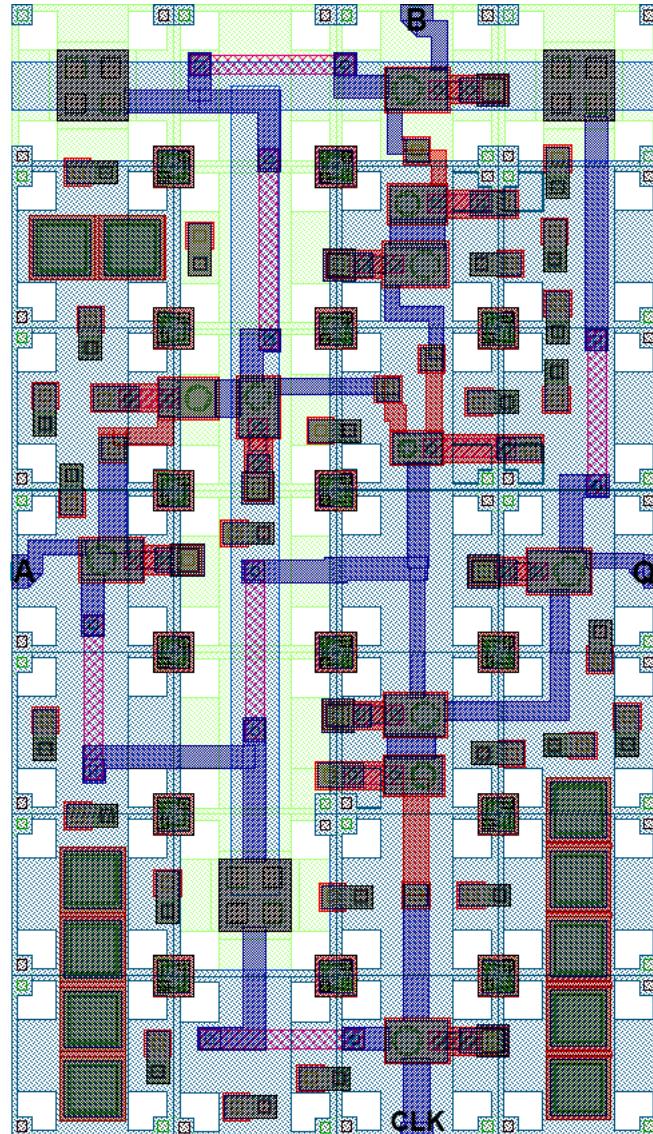


Figure 2.63: RSFQ NDRO Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param LP6=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/09/01.    65  .param LP8=LP
3  * Author: L. Schindler                      66  .param LP9=LP
4  * Version: 3.0                                67  .param LP11=LP
5  * Last modification date: 30 August 2022     68
6  * Last modification by: T. Hall              69  .param RB1=B0Rs/B1
7  *$Ports      a      b      clk      q        70  .param RB2=B0Rs/B2
8  .subckt THmitll_NDRO a b clk q             71  .param RB3=B0Rs/B3
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param RB4=B0Rs/B4
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param RB5=B0Rs/B5
   ↪ )                                         74  .param RB6=B0Rs/B6
10 .param Phi0=2.067833848E-15                75  .param RB7=B0Rs/B7
11 .param B0=1                                 76  .param RB8=B0Rs/B8
12 .param Ic0=0.0001                           77  .param RB9=B0Rs/B9
13 .param IcRs=100u*6.859904418               78  .param RB10=B0Rs/B10
14 .param B0Rs=IcRs/Ic0*B0                     79  .param RB11=B0Rs/B11
15 .param Rsheet=2                            80
16 .param Lsheet=1.13e-12                      81  .param LRB1=(RB1/Rsheet)*Lsheet+LP
17 .param LP=0.5p                            82  .param LRB2=(RB2/Rsheet)*Lsheet
18 .param IC=2.5                             83  .param LRB3=(RB3/Rsheet)*Lsheet+LP
19 .param LB=2p                             84  .param LRB4=(RB4/Rsheet)*Lsheet+LP
20 .param BiasCoef=0.7                        85  .param LRB5=(RB5/Rsheet)*Lsheet
21
22 .param B1=2.5                            86  .param LRB6=(RB6/Rsheet)*Lsheet+LP
23 .param B2=1.80                           87  .param LRB7=(RB7/Rsheet)*Lsheet
24 .param B3=2.01                           88  .param LRB8=(RB8/Rsheet)*Lsheet+LP
25 .param B4=2.5                            89  .param LRB9=(RB9/Rsheet)*Lsheet+LP
26 .param B5=1.64                           90  .param LRB10=(RB10/Rsheet)*Lsheet
27 .param B6=2.58                           91  .param LRB11=(RB11/Rsheet)*Lsheet+LP
28 .param B7=0.90                           92
29 .param B8=2.30                           93  B1 1 2 jjmit area=B1
30 .param B9=2.5                            94  B2 4 5 jjmit area=B2
31 .param B10=1.77                          95  B3 5 6 jjmit area=B3
32 .param B11=2.5                           96  B4 9 10 jjmit area=B4
33
34 .param IB1=175u                           97  B5 12 13 jjmit area=B5
35 .param IB2=139u                           98  B6 13 14 jjmit area=B6
36 .param IB3=175u                           99  B7 8 15 jjmit area=B7
37 .param IB4=158u                           100 B8 18 19 jjmit area=B8
38 .param IB5=175u                           101 B9 20 21 jjmit area=B9
39 .param IB6=175u                           102 B10 23 18 jjmit area=B10
40
41 .param LB1=LB                            103 B11 24 25 jjmit area=B11
42 .param LB2=LB                            104
43 .param LB3=LB                            105  IB1 0 3 pw1(0 0 5p IB1)
44 .param LB4=LB                            106  IB2 0 7 pw1(0 0 5p IB2)
45 .param LB5=LB                            107  IB3 0 11 pw1(0 0 5p IB3)
46 .param LB6=LB                            108  IB4 0 17 pw1(0 0 5p IB4)
47
48 .param L1=1.8663p                         109  IB5 0 22 pw1(0 0 5p IB5)
49 .param L2=3.1100p                         110  IB6 0 26 pw1(0 0 5p IB6)
50 .param L3=2.8212p                         111
51 .param L4=1.7117p                         112  LB1 3 1 7.35E-013
52 .param L5=2.7767p                         113  LB2 7 5 7.798E-013
53 .param L6=3.6623p                         114  LB3 11 9 1.023E-012
54 .param L7=1.4501p                         115  LB4 17 16 1.981E-012
55 .param L8=2.0153p                         116  LB5 22 20 6.382E-013
56 .param L9=1.3783p                         117  LB6 26 24 1.181E-012
57 .param L10=3.2508p                         118
58 .param L11=3.3341p                         119  L1 a 1 1.861E-012
59 .param L12=1.6989p                         120  L2 1 4 3.103E-012
60
61 .param LP1=LP                            121  L3 5 8 2.808E-012
62 .param LP3=LP                            122  L4 b 9 1.712E-012
63 .param LP4=LP                            123  L5 9 12 2.775E-012
64
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```

```

130 | L12 24 q 1.698E-012
131 | LP1 2 0 4.356E-013
132 | LP3 6 0 4.322E-013
133 | LP4 10 0 3.473E-013
134 | LP6 14 0 3.698E-013
135 | LP8 19 0 4.794E-013
136 | LP9 21 0 3.788E-013
137 | LP11 25 0 4.491E-013
138 |
139 |
140 | RB1 1 101 RB1
141 | LRB1 101 0 LRB1
142 | RB2 4 104 RB2
143 | LRB2 104 5 LRB2
144 | RB3 5 105 RB3
145 | LRB3 105 0 LRB3
146 | RB4 9 109 RB4
147 | LRB4 109 0 LRB4
148 | RB5 12 112 RB5
149 | LRB5 112 13 LRB5
150 | RB6 13 113 RB6
151 | LRB6 113 0 LRB6
152 | RB7 8 108 RB7
153 | LRB7 108 15 LRB7
154 | RB8 18 118 RB8
155 | LRB8 118 0 LRB8
156 | RB9 20 120 RB9
157 | LRB9 120 0 LRB9
158 | RB10 23 123 RB10
159 | LRB10 123 18 LRB10
160 | RB11 24 124 RB11
161 | LRB11 124 0 LRB11
162 .ends

```

Listing 2.31: RSFQ NDRO JoSIM netlist.**Table 2.31:** RSFQ NDRO pin list.

Pin	Description
a	Data input (set signal)
b	Data input (reset signal)
clk	Clock input
q	Data output

The simulation results for the RSFQ NDRO using JoSIM is shown in Fig. 2.64. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a** (set signal),
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b** (reset signal),
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected to pin **q**.

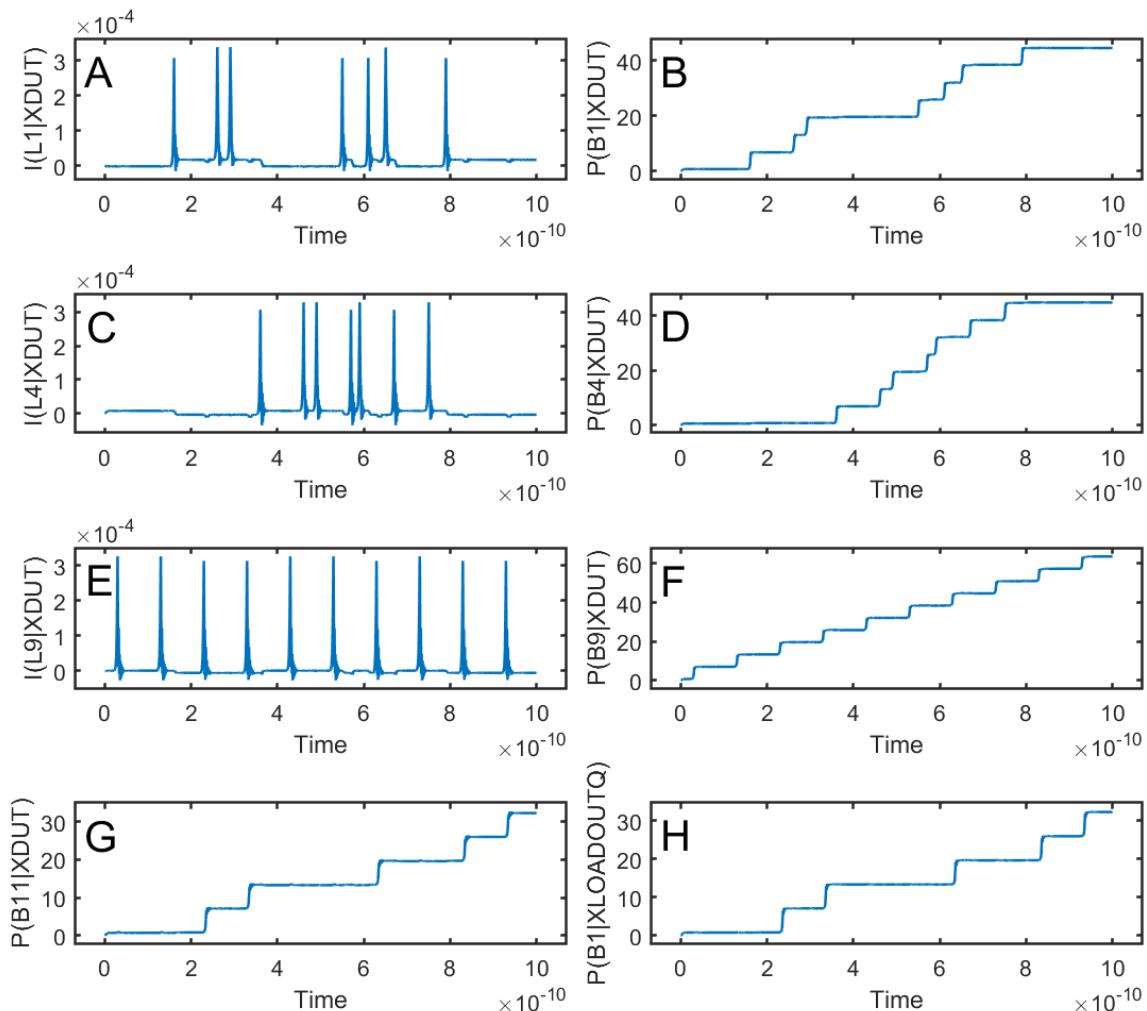


Figure 2.64: RSFQ NDRO analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 1 September 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_NDRO_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 5.5,
21   ct_state0_a_b = 0.9,
22   ct_state1_b_a = 1.9,
23   ct_state1_clk_clk = 9.1;
24
25 reg
26   errorsignal_a,
27   errorsignal_b,
28   errorsignal_clk;
29
30 integer
31   outfile,
32   cell_state; // internal state of the cell
33
34 initial
35 begin
36   errorsignal_a = 0;
37   errorsignal_b = 0;
38   errorsignal_clk = 0;
39   cell_state = 0; // Startup state
40   q = 0; // All outputs start at 0
41 end
42
43 always @(posedge a or negedge a) // execute at positive and negative edges of input
44 begin
45   if ($time>4) // arbitrary steady-state time)
46     begin
47       if (errorsignal_a == 1'b1) // A critical timing is active for this input
48         begin
49           outfile = $fopen("errors.txt", "a");
50           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
51           ↪ ", $stime);
52           $fclose(outfile);
53           q <= 1'bX; // Set all outputs to unknown
54         end
55       if (errorsignal_a == 0)
56         begin
57           case (cell_state)
58             0: begin
59               cell_state = 1; // Blocking statement -- immediately
60               errorsignal_b = 1; // Critical timing on this input; assign
61               ↪ immediately
62               errorsignal_b <= #(ct_state0_a_b) 0; // Clear error signal
63               ↪ after critical timing expires
64             end
65           1: begin
66             end
67           endcase

```

```

65           end
66       end
67   end
68
69 always @(posedge b or negedge b) // execute at positive and negative edges of input
70   begin
71     if ($time>4) // arbitrary steady-state time)
72     begin
73       if (errorsignal_b == 1'b1) // A critical timing is active for this input
74       begin
75         outfile = $fopen("errors.txt", "a");
76         $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
77                     ↪ ", $stime);
78         $fclose(outfile);
79         q <= 1'bX; // Set all outputs to unknown
80       end
81     if (errorsignal_b == 0)
82     begin
83       case (cell_state)
84         0: begin
85           end
86         1: begin
87           cell_state = 0; // Blocking statement -- immediately
88           errorsignal_a = 1; // Critical timing on this input; assign
89           ↪ immediately
90           errorsignal_a <= #(ct_state1_b_a) 0; // Clear error signal
91           ↪ after critical timing expires
92           end
93         endcase
94       end
95   end
96
97 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
98   begin
99     if ($time>4) // arbitrary steady-state time)
100    begin
101      if (errorsignal_clk == 1'b1) // A critical timing is active for this input
102      begin
103        outfile = $fopen("errors.txt", "a");
104        $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
105                     ↪ ", $stime);
106        $fclose(outfile);
107        q <= 1'bX; // Set all outputs to unknown
108      end
109    if (errorsignal_clk == 0)
110    begin
111      case (cell_state)
112        0: begin
113          end
114        1: begin
115          q <= #(delay_state1_clk_q) !q;
116          errorsignal_clk = 1; // Critical timing on this input; assign
117          ↪ immediately
118          errorsignal_clk <= #(ct_state1_clk_clk) 0; // Clear error
119          ↪ signal after critical timing expires
120          end
121        endcase
122      end
123    end
124  end
125 endmodule

```

Listing 2.32: RSFQ NDRO verilog model.

The digital simulation results for the RSFQ NDRO is shown in Fig. 2.65 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 2.66.

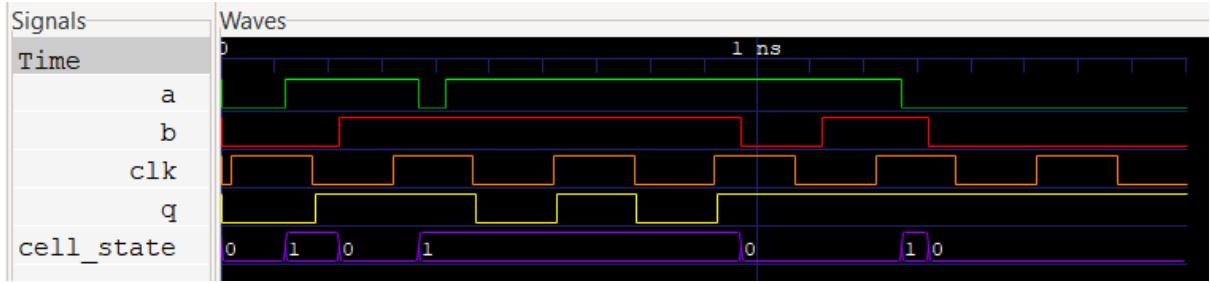


Figure 2.65: RSFQ NDRO digital simulation results.

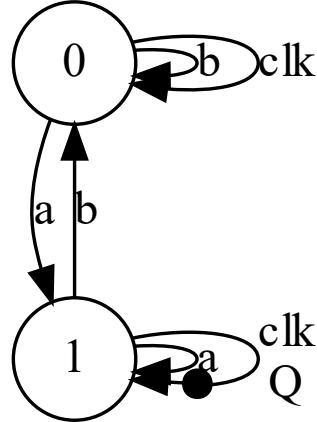


Figure 2.66: RSFQ NDRO Mealy finite state machine diagram.

Power Consumption

Table 2.32: RSFQ NDRO power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2590	4.76
2	2590	9.51
5	2590	23.8
10	2590	47.6
20	2590	95.1
50	2590	238

2.3.3 BUFF

The RSFQ BUFF cell is a buffer cell intended for clock balancing. It is designed to have the same a-to-q delay as the SPLIT cell. The cell is not designed to be directly connected to a PTL.

Schematic

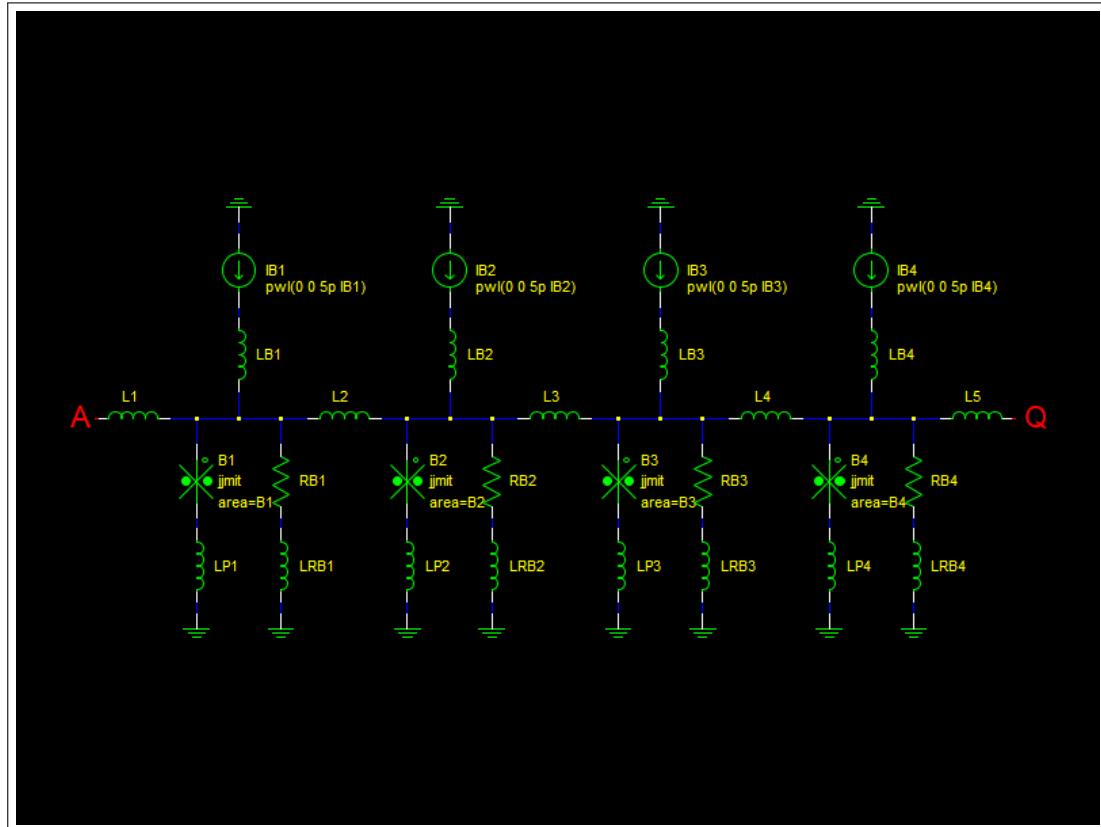


Figure 2.67: Schematic of RSFQ BUFF.

Layout

The physical layout of the RSFQ BUFF is shown in Fig. 2.68. The layout height is $70 \mu m$ and the width is $30 \mu m$. The cell includes an integrated bias line on M0 within the top row of track blocks. Bias pillars from M0 to M6 connect the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

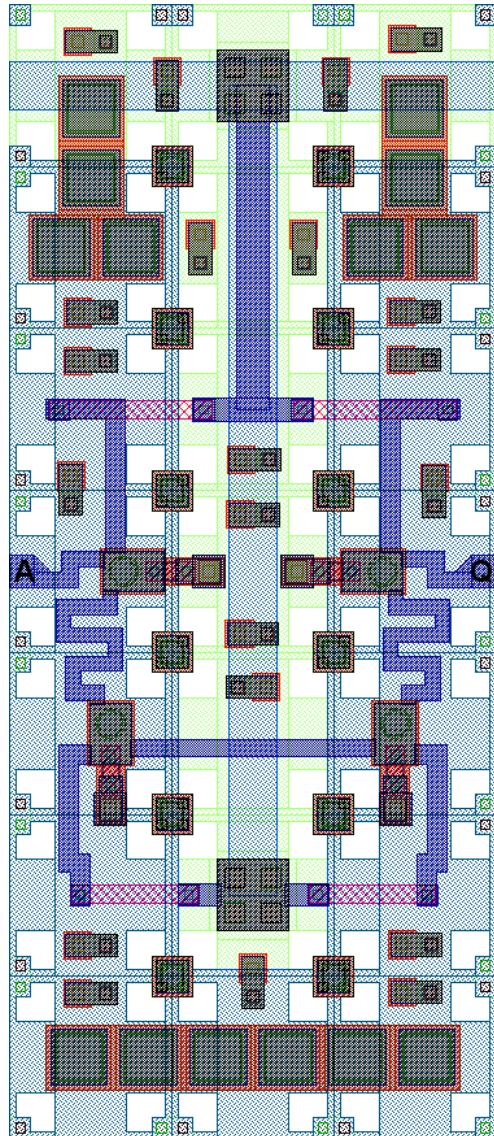


Figure 2.68: RSFQ BUFF Layout.

Analog model

```

1  * Back-annotated simulation file written      47
2  *   ↪ by InductEx v.6.1.52 on 2022/07/29.    48 .param RB1=B0Rs/B1
3  * Author: L. Schindler                      49 .param RB2=B0Rs/B2
4  * Version: 3.0                                50 .param RB3=B0Rs/B3
5  * Last modification date: 29 July 2022       51 .param RB4=B0Rs/B4
5  * Last modification by: T. Hall              52
6
7 *$Ports      a      q
8 .subckt THmitll_BUFF a q
9 .model jjmit jj(rtype=1, vg=2.8mV, cap
10   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
11   ↪ )
12 .param Phi0=2.067833848E-15
13 .param B0=1
14 .param Ic0=0.0001
15 .param IcRs=100u*6.859904418
16 .param B0Rs=IcRs/Ic0*B0
17 .param Rsheet=2
18 .param Lsheet=1.13e-12
19 .param LP=0.5p
20 .param IC=2.5
21 .param LB=2p
22 .param BiasCoef=0.7
23 .param B1=IC
24 .param B2=IC
25 .param B3=IC
26 .param B4=IC
27 .param IB1=B1*Ic0*BiasCoef
28 .param IB2=B2*Ic0*0.95
29 .param IB3=B3*Ic0*0.95
30 .param IB4=B4*Ic0*BiasCoef
31
32 .param LB1=LB
33 .param LB2=LB
34 .param LB3=LB
35 .param LB4=LB
36
37 .param L1=Phi0/(4*B1*Ic0)
38 .param L2=Phi0/(2*B1*Ic0)
39 .param L3=Phi0/(2*B2*Ic0)
40 .param L4=Phi0/(2*B3*Ic0)
41 .param L5=Phi0/(4*B4*Ic0)
42
43 .param LP1=LP
44 .param LP2=LP
45 .param LP3=LP
46 .param LP4=LP
47
48 .param RB1=B0Rs/B1
49 .param RB2=B0Rs/B2
50 .param RB3=B0Rs/B3
51 .param RB4=B0Rs/B4
52
53 .param LRB1=(RB1/Rsheet)*Lsheet+LP
54 .param LRB2=(RB2/Rsheet)*Lsheet+LP
55 .param LRB3=(RB3/Rsheet)*Lsheet+LP
56 .param LRB4=(RB4/Rsheet)*Lsheet+LP
57
58 B1 1 2 jjmit area=B1
59 B2 4 5 jjmit area=B2
60 B3 7 8 jjmit area=B3
61 B4 10 11 jjmit area=B4
62
63 IB1 0 3 pwl(0 0 5p IB1)
64 IB2 0 6 pwl(0 0 5p IB2)
65 IB3 0 9 pwl(0 0 5p IB3)
66 IB4 0 12 pwl(0 0 5p IB4)
67
68 LB1 3 1 LB1
69 LB2 6 4 LB2
70 LB3 9 7 LB3
71 LB4 12 10 LB4
72
73 L1 a 1 2.06E-012
74 L2 1 4 4.141E-012
75 L3 4 7 4.153E-012
76 L4 7 10 4.142E-012
77 L5 10 q 2.078E-012
78
79 LP1 2 0 4.709E-013
80 LP2 5 0 4.152E-013
81 LP3 8 0 4.425E-013
82 LP4 11 0 4.583E-013
83
84 RB1 1 101 RB1
85 LRB1 101 0 LRB1
86 RB2 4 104 RB2
87 LRB2 104 0 LRB2
88 RB3 7 107 RB3
89 LRB3 107 0 LRB3
90 RB4 10 110 RB4
91 LRB4 110 0 LRB4
92 .ends

```

Listing 2.33: RSFQ BUFF JoSIM netlist.

Table 2.33: RSFQ BUFF pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ BUFF using JoSIM is shown in Fig. 2.69. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected to pin **q**.

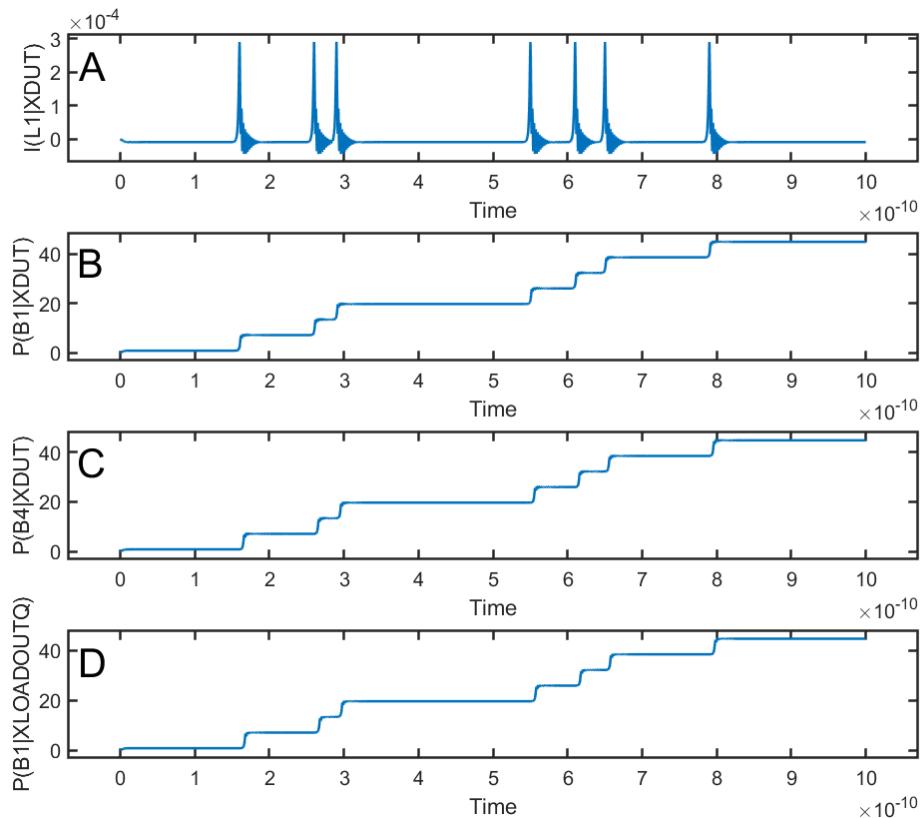


Figure 2.69: RSFQ BUFF analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 29 July 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_BUFF_v3p0_extracted (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 6.3,
21   ct_state0_a_a = 5.2;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q = 0; // All outputs start at 0
35 end
36
37 always @(posedge a or negedge a) // execute at positive and negative edges of input
38 begin
39   if ($time>4) // arbitrary steady-state time)
40     begin
41       if (errorsignal_a == 1'b1) // A critical timing is active for this input
42         begin
43           outfile = $fopen("errors.txt", "a");
44           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
45           ↪ ", $stime);
46           $fclose(outfile);
47           q <= 1'bX; // Set all outputs to unknown
48         end
49       if (errorsignal_a == 0)
50         begin
51           case (cell_state)
52             0: begin
53               q <= #(delay_state0_a_q) !q;
54               errorsignal_a = 1; // Critical timing on this input; assign
55               ↪ immediately
56               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
57               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 2.34: RSFQ BUFF verilog model.

The digital simulation results for the RSFQ BUFF is shown in Fig. 2.70 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 2.71.

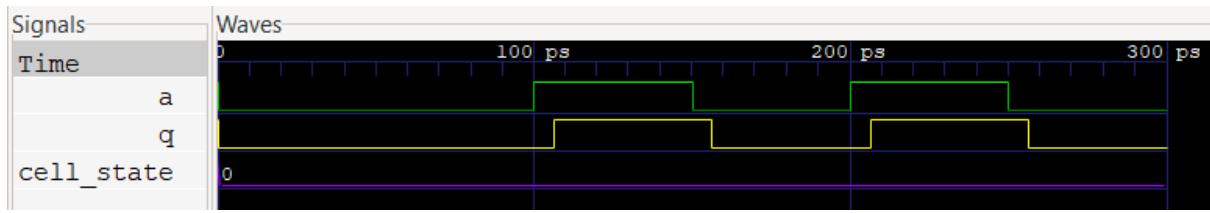


Figure 2.70: RSFQ BUFF digital simulation results.

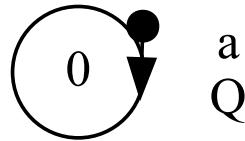


Figure 2.71: RSFQ BUFF Mealy finite state machine diagram.

Power Consumption

Table 2.34: RSFQ BUFF power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2150	2.07
2	2150	4.14
5	2150	10.3
10	2150	20.7
20	2150	41.4
50	2150	103

2.4 Interface Cells

2.4.1 DCSFQ

The RSFQ DCSFQ is an interface cell designed to convert input voltage pulses into SFQ pulses. The DCSFQ does not have an integrated PTL transmitter and is not intended to connect directly to a PTL output.

Schematic

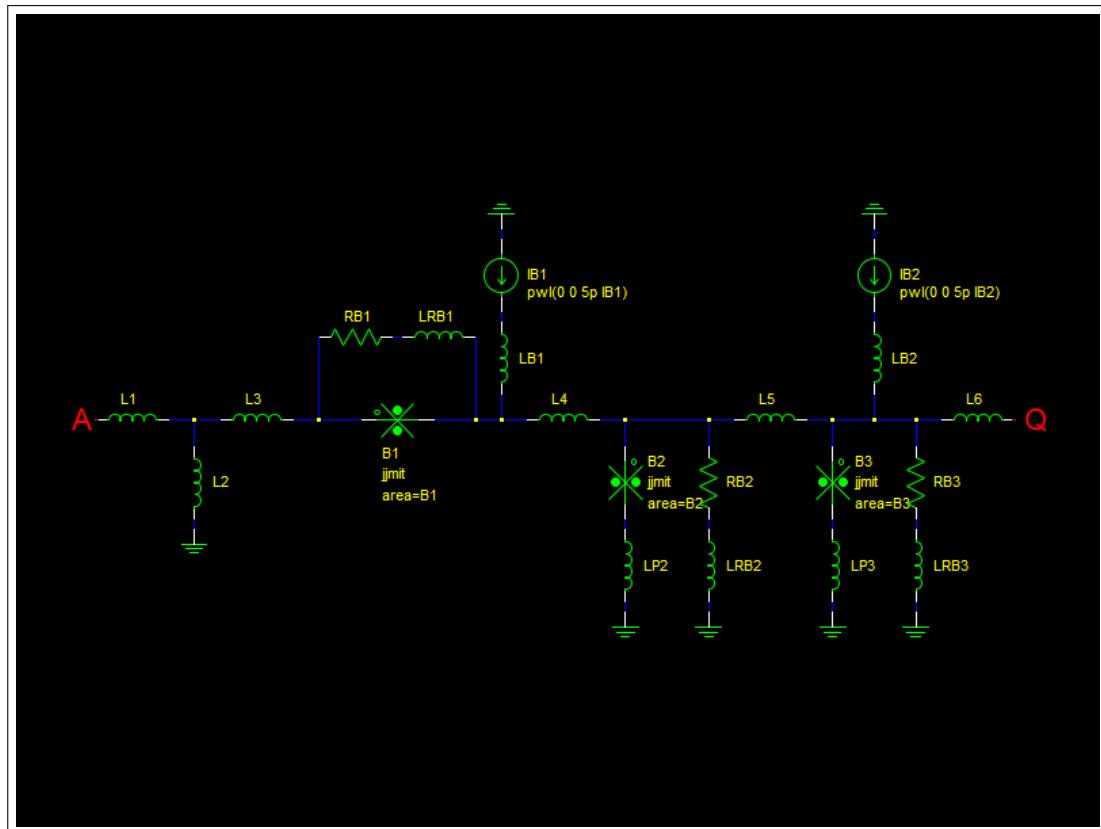


Figure 2.72: Schematic of RSFQ DCSFQ.

Layout

The physical layout of the RSFQ DCSFQ is shown in Fig. 2.73. The layout height is $70 \mu m$ and the width is $20 \mu m$. The cell includes an integrated bias line on M0 within the top row of track blocks. A bias pillar from M0 to M6 connects the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

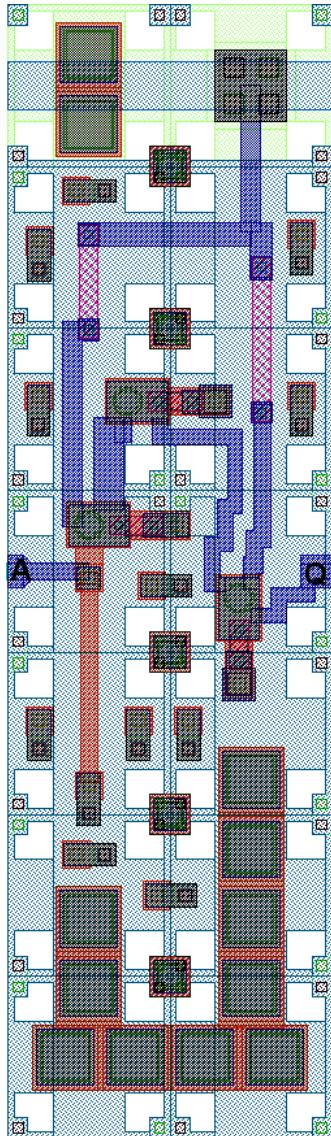


Figure 2.73: RSFQ DCSFQ Layout.

Analog model

```

1  * Back-annotated simulation file written      39 | .param LP2=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/07/25.    40 | .param LP3=LP
3  * Author: L. Schindler                      41 |
4  * Version: 3.0                                42 | .param RB1=B0Rs/B1
5  * Last modification date: 21 July 2022       43 | .param RB2=B0Rs/B2
6  * Last modification by: T. Hall              44 | .param RB3=B0Rs/B3
7  *$Ports          a      q                  45 |
8  .subckt THmitll_DCSFQ a q                 46 | .param LRB1=(RB1/Rsheet)*Lsheet
9  .model jjmit jj(rtype=1, vg=2.8mV, cap     47 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     48 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
   ↪ )                                         49 |
10 .param Phi0=2.067833848E-15                50 | B1 2 3 jjmit area=B1
11 .param B0=1                                 51 | B2 5 6 jjmit area=B2
12 .param Ic0=0.0001                           52 | B3 7 8 jjmit area=B3
13 .param IcRs=100u*6.859904418               53 |
14 .param B0Rs=IcRs/Ic0*B0                   54 | IB1 0 4 pwl(0 0 5p IB1)
15 .param Rsheet=2                            55 | IB2 0 9 pwl(0 0 5p IB2)
16 .param Lsheet=1.13e-12                     56 |
17 .param LP=0.5p                            57 | LB1 4 3 2.825E-012
18 .param IC=2.5                             58 | LB2 9 7 2.942E-012
19 .param LB=2p                            59 |
20 .param BiasCoef=0.7                      60 | L1 a 1 1.672E-012
21                               61 | L2 1 0 3.901E-012
22 .param B1=2.25                           62 | L3 1 2 5.953E-013
23 .param B2=2.25                           63 | L4 3 5 1.1E-012
24 .param B3=IC                            64 | L5 5 7 4.542E-012
25                               65 | L6 7 q 2.012E-012
26 .param IB1=275u                          66 |
27 .param IB2=B3*Ic0*BiasCoef             67 | LP2 6 0 3.924E-013
28                               68 | LP3 8 0 3.841E-013
29 .param LB1=LB                           69 |
30 .param LB2=LB                           70 | RB1 2 102 RB1
31                               71 | LRB1 102 3 LRB1
32 .param L1=1p                            72 | RB2 5 105 RB2
33 .param L2=3.9p                           73 | LRB2 105 0 LRB2
34 .param L3=0.6p                           74 | RB3 7 107 RB3
35 .param L4=1.1p                           75 | LRB3 107 0 LRB3
36 .param L5=4.5p                           76 | .ends
37 .param L6=Phi0/(4*IC*Ic0)               77 |
38

```

Listing 2.35: RSFQ DCSFQ JoSIM netlist.

Table 2.35: RSFQ DCSFQ pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ DCSFQ using JoSIM is shown in Fig. 2.74. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the current through the output inductor connected to pin **q**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected to pin **q**.

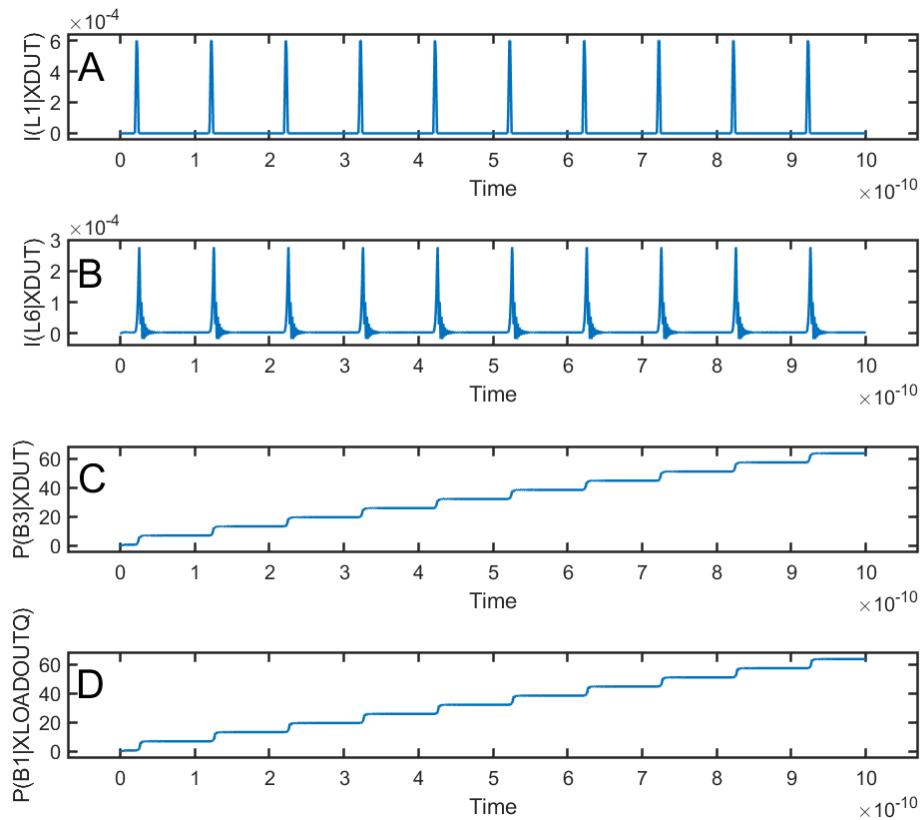


Figure 2.74: RSFQ DCSFQ analog simulation results.

2.4.2 SFQDC

The RSFQ SFQDC is an interface cell designed to convert SFQ pulses to an output voltage level which can be measured by standard equipment. The SFQDC does not have an integrated PTL receiver and is not intended to be connected directly to a PTL input.

Schematic

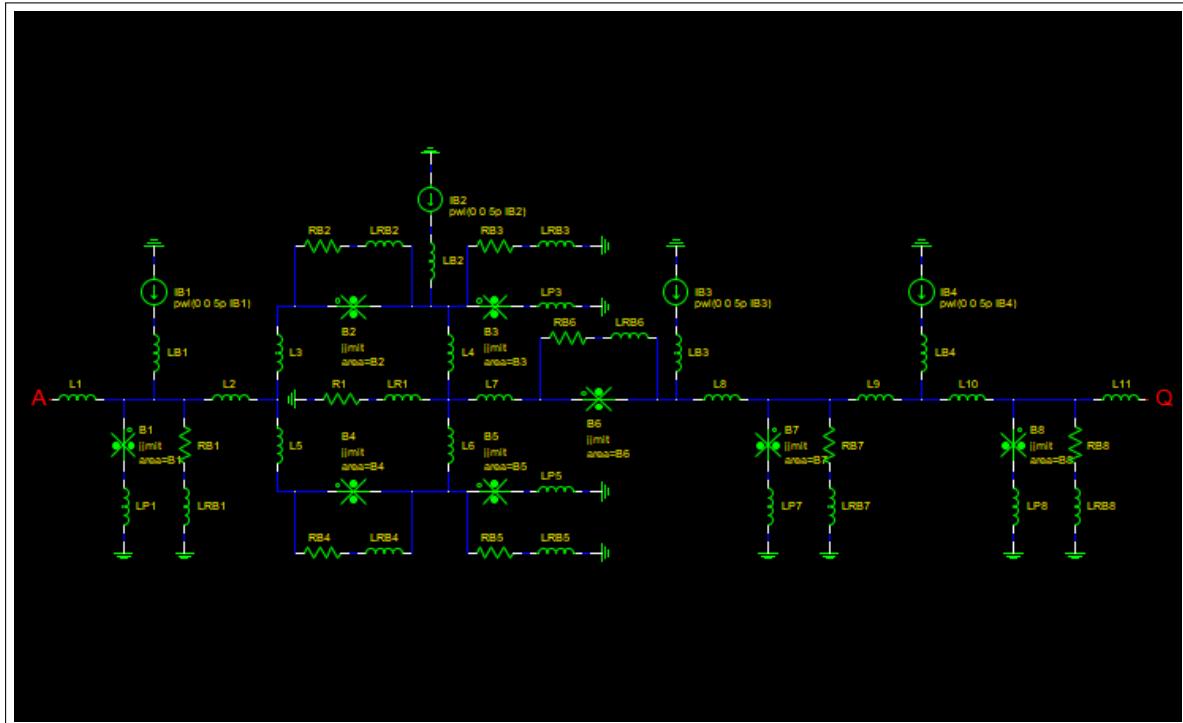


Figure 2.75: Schematic of RSFQ SFQDC.

Layout

The physical layout of the RSFQ SFQDC is shown in Fig. 2.76. The layout height is $70 \mu m$ and the width is $40 \mu m$. The cell includes an integrated bias line on M0 within the top row of track blocks. A bias pillar from M0 to M6 connects the circuit to the integrated bias line. All bias resistors are designed to be connected to a 2.6 mV voltage source.

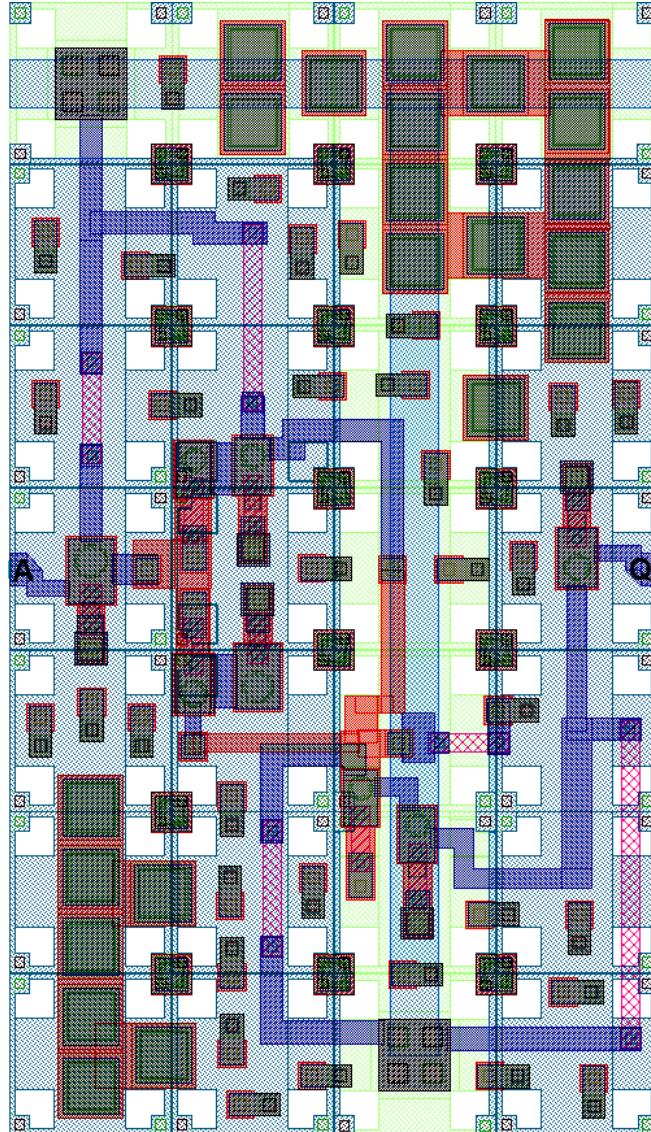


Figure 2.76: RSFQ SFQDC Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param RB2=B0Rs/B2
2   ↪ by InductEx v.6.1.52 on 2022/08/08.      65  .param RB3=B0Rs/B3
3  * Adapted from Fluxonics SDQDC_v5          66  .param RB4=B0Rs/B4
4  * Author: L. Schindler                     67  .param RB5=B0Rs/B5
5  * Version: 3.0                           68  .param RB6=B0Rs/B6
6  * Last modification date: 4 August 2022    69  .param RB7=B0Rs/B7
7  * Last modification by: T. Hall           70  .param RB8=B0Rs/B8
8
9  *$Ports      a      q
10 .subckt THmitll_SFQDC a q
11 .model jjmit jj(rtype=1, vg=2.8mV, cap
12   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA
13   ↪ )
14 .param Phi0=2.067833848E-15
15 .param B0=1
16 .param Ic0=0.0001
17 .param IcRs=100u*6.859904418
18 .param B0Rs=IcRs/Ic0*B0
19 .param Rsheet=2
20 .param Lsheet=1.13e-12
21 .param LP=0.5p
22 .param IC=2.5
23 .param LB=2p
24 .param BiasCoef=0.7
25 .param B1=3.25
26 .param B2=1.50
27 .param B3=1.75
28 .param B4=2.00
29 .param B5=3.00
30 .param B6=1.50
31 .param B7=1.50
32 .param B8=2.00
33 .param IB1=280u
34 .param IB2=150u
35 .param IB3=220u
36 .param IB4=80u
37 .param LB1=LB
38 .param LB2=LB
39 .param LB3=LB
40 .param LB4=LB
41 .param L1=1.522p
42 .param L2=0.827p
43 .param L3=1.12884p
44 .param L4=5.94p
45 .param L5=1.11098p
46 .param L6=3.216p
47 .param L7=0.215p
48 .param L8=0.954p
49 .param L9=3.699p
50 .param L10=2.010p
51 .param L11=1.510p
52 .param LR1=0.91p
53 .param R1=0.375
54 .param LP1=LP
55 .param LP3=LP
56 .param LP5=LP
57 .param LP7=LP
58 .param LP8=LP
59 .param RB1=B0Rs/B1
60
61
62
63
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
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```

```

130 | LRB5 111 0 LRB5
131 | RB6 14 114 RB6
132 | LRB6 114 15 LRB6
133 | RB7 17 117 RB7
134 | LRB7 117 0 LRB7

```

```

135 | RB8 21 121 RB8
136 | LRB8 121 0 LRB8
137 .ends

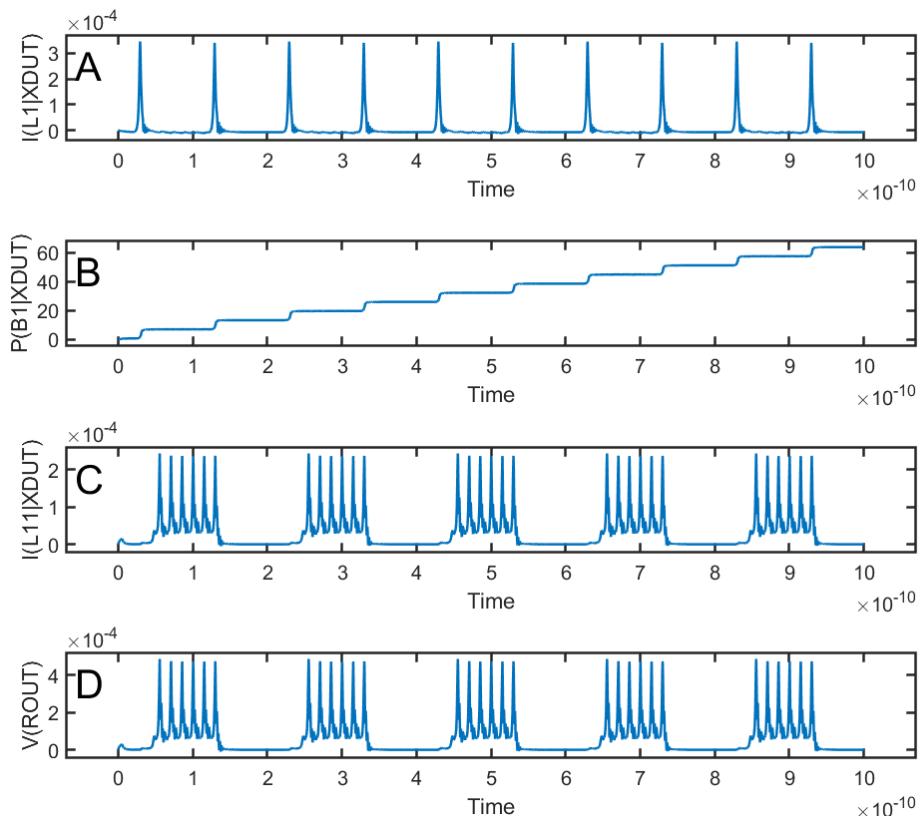
```

Listing 2.36: RSFQ SFQDC JoSIM netlist.**Table 2.36:** RSFQ SFQDC pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ SFQDC using JoSIM is shown in Fig. 2.77. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the output inductor connected to pin **q**, and
- (c) the voltage over the load resistor connected to pin **q**.

**Figure 2.77:** RSFQ SFQDC analog simulation results.

3. RSFQ Cell Library: PTL Connections

3.1 Interconnects

3.1.1 JTLT

The JTLT, Josephson transmission line, cell is commonly used to reestablish and propagate RSFQ pulses when long PTL connections are required. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

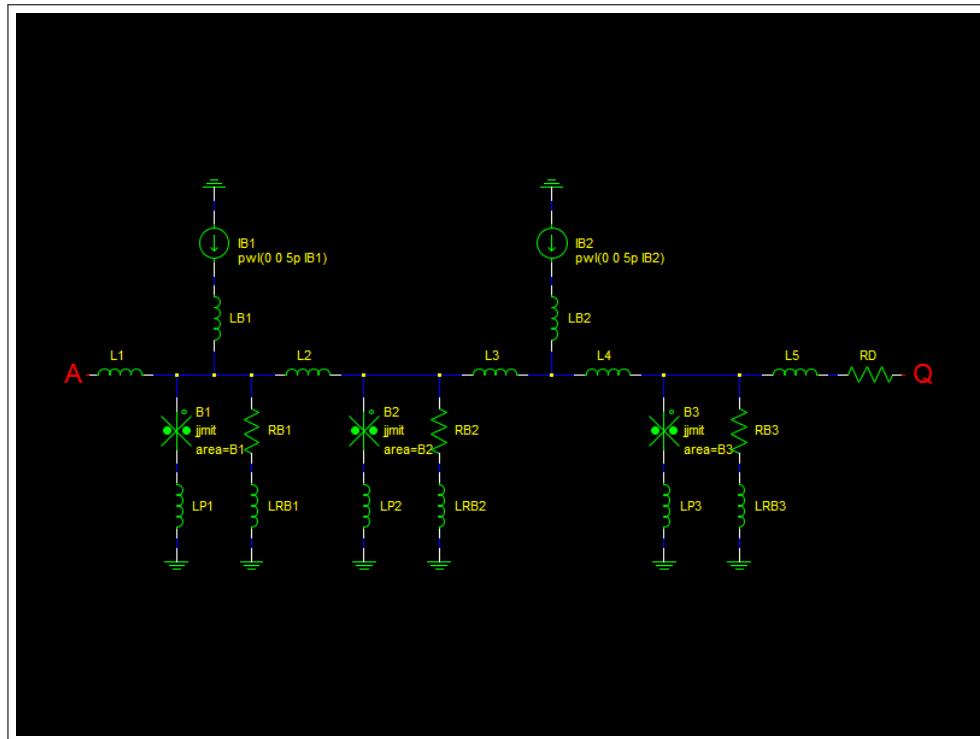


Figure 3.1: Schematic of RSFQ JTLT.

Layout

The physical layout of the RSFQ JTLT is shown in Fig. 3.2. The layout height is $70 \mu m$ and the width is $20 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

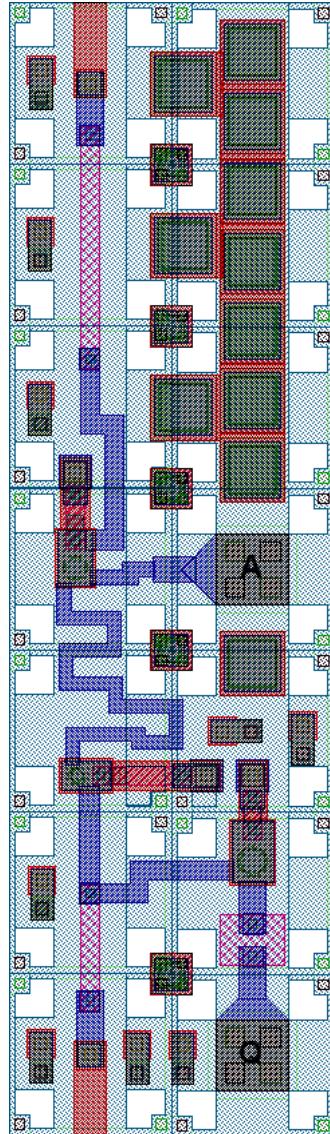


Figure 3.2: RSFQ JTLT Layout.

Analog model

```

1  * Back-annotated simulation file written      42 | .param LP1=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/08/10.    43 | .param LP2=LP
3  * Author: L. Schindler                      44 | .param LP3=LP
4  * Version: 3.0                                45 |
5  * Last modification date: 9 August 2022       46 | .param RB1=B0Rs/B1
6  * Last modification by: T. Hall              47 | .param RB2=B0Rs/B2
7  *$Ports      a      q                         48 | .param RB3=B0Rs/B3
8  .subckt THmitll_JTLLT a q                   49 |
9  .model jjmit jj(rtype=1, vg=2.8mV, cap     50 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA      51 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
   ↪ )                                         52 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
10 .param Phi0=2.067833848E-15                 53 |
11 .param B0=1                                    54 | B1 1 2 jjmit area=B1
12 .param Ic0=0.0001                            55 | B2 4 5 jjmit area=B2
13 .param IcRs=100u*6.859904418                  56 | B3 8 9 jjmit area=B3
14 .param B0Rs=IcRs/Ic0*B0                     57 |
15 .param Rsheet=2                             58 | IB1 0 3 pwl(0 0 5p IB1)
16 .param Lsheet=1.13e-12                      59 | IB2 0 7 pwl(0 0 5p IB2)
17 .param LP=0.5p                               60 |
18 .param IC=2.5                                61 | LB1 3 1 3.202E-012
19 .param ICreceive=1.6                         62 | LB2 7 6 2.142E-013
20 .param ICtrans=2.5                           63 |
21 .param LB=2p                                 64 | L1 a 1 1.986E-012
22 .param BiasCoef=0.7                          65 | L2 1 4 8.188E-012
23 .param Lptl=2p                               66 | L3 4 6 1.431E-012
24 .param RD=1.36                               67 | L4 6 8 2.254E-012
25                                     68 | L5 8 10 7.542E-013
26 .param B1=1.6                                69 |
27 .param B2=0.81                               70 | RD 10 q RD
28 .param B3=2.5                                71 |
29                                     72 | LP1 2 0 4.596E-013
30 .param IB1=112u                             73 | LP2 5 0 4.684E-013
31 .param IB2=239u                             74 | LP3 9 0 4.113E-013
32                                     75 |
33 .param LB1=LB                                76 | RB1 1 101 RB1
34 .param LB2=LB                                77 | LRB1 101 0 LRB1
35                                     78 | RB2 4 104 RB2
36 .param L1=Lptl                               79 | LRB2 104 0 LRB2
37 .param L2=8.2192p                            80 | RB3 8 108 RB3
38 .param L3=1.4265p                            81 | LRB3 108 0 LRB3
39 .param L4=2.2384p                            82 |
40 .param L5=Lptl                               83 | .ends
41

```

Listing 3.1: RSFQ JTLLT JoSIM netlist.

Table 3.1: RSFQ JTLLT pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ JTLT using JoSIM is shown in Fig. 3.3. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected via a PTL to the JTLT.

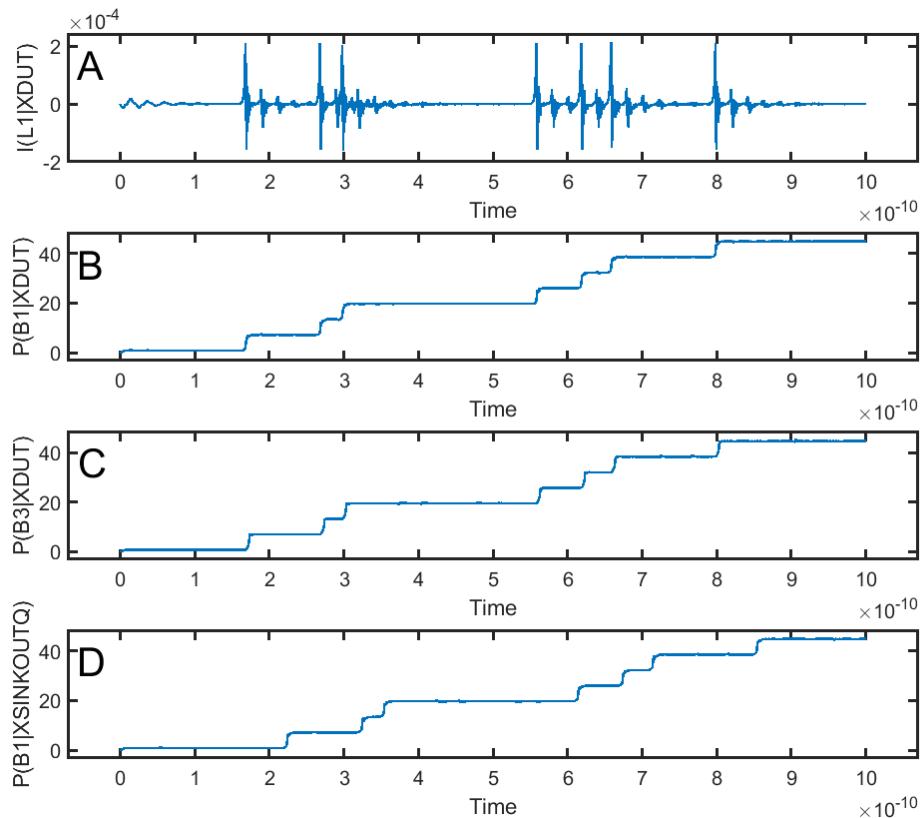


Figure 3.3: RSFQ JTLT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 10 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_JTLT_v3p0_extracted (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 4.5,
21   ct_state0_a_a = 20.1;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q = 0; // All outputs start at 0
35 end
36
37 always @(posedge a or negedge a) // execute at positive and negative edges of input
38 begin
39   if ($time>4) // arbitrary steady-state time)
40     begin
41       if (errorsignal_a == 1'b1) // A critical timing is active for this input
42         begin
43           outfile = $fopen("errors.txt", "a");
44           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
45           ↪ ", $stime);
46           $fclose(outfile);
47           q <= 1'bX; // Set all outputs to unknown
48         end
49       if (errorsignal_a == 0)
50         begin
51           case (cell_state)
52             0: begin
53               q <= #(delay_state0_a_q) !q;
54               errorsignal_a = 1; // Critical timing on this input; assign
55               ↪ immediately
56               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
57               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 3.2: RSFQ JTLT verilog model.

The digital simulation results for the RSFQ JTLT is shown in Fig. 3.4 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 3.5.

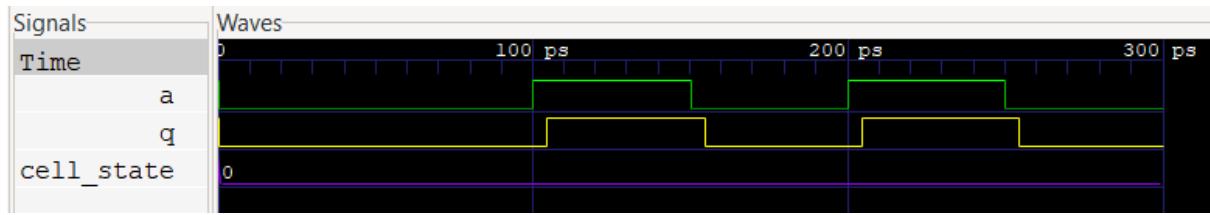


Figure 3.4: RSFQ JTLT digital simulation results.

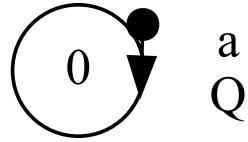


Figure 3.5: RSFQ JTLT Mealy finite state machine diagram.

Power Consumption

Table 3.2: RSFQ JTLT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	913	1.02
2	913	2.03
5	913	5.08
10	913	10.2
20	913	20.3
50	913	50.8

3.1.2 SPLITT

The SPLITT cell is used to split a single pulse signal line into two duplicate output pulse signal lines. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

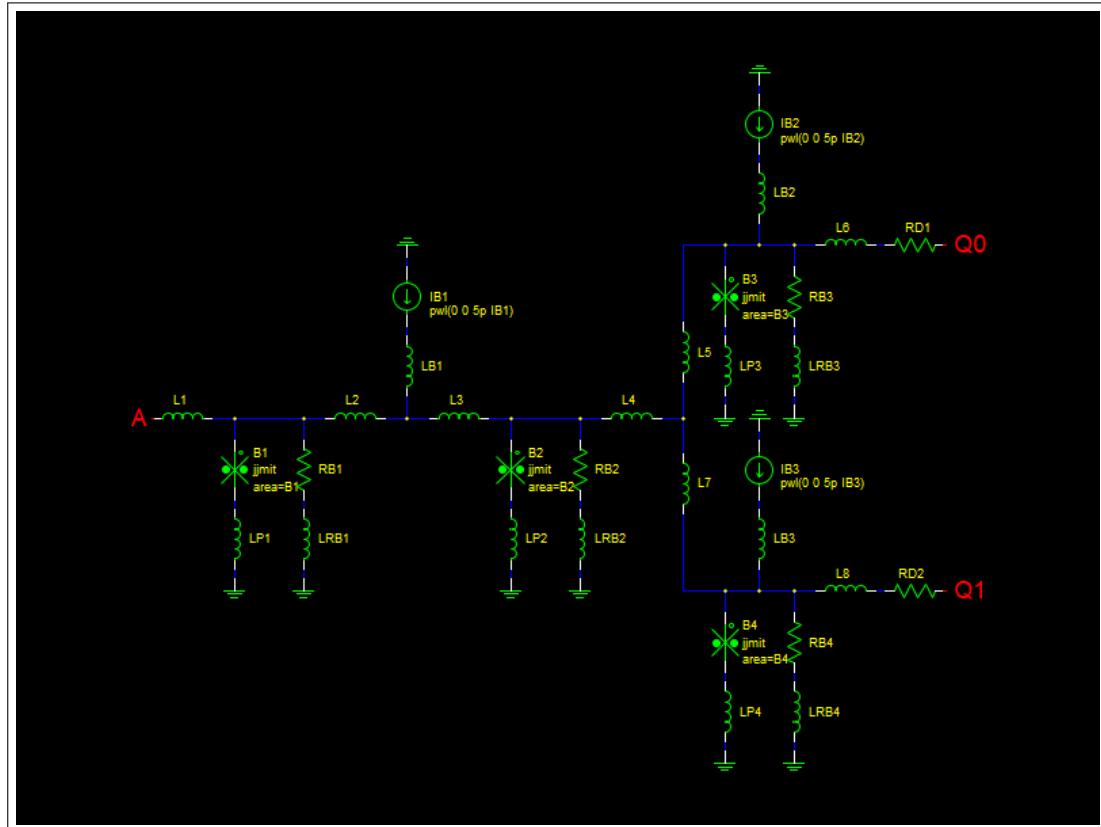


Figure 3.6: Schematic of RSFQ SPLITT.

Layout

The physical layout of the RSFQ SPLITT is shown in Fig. 3.7. The layout height is $70 \mu m$ and the width is $30 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

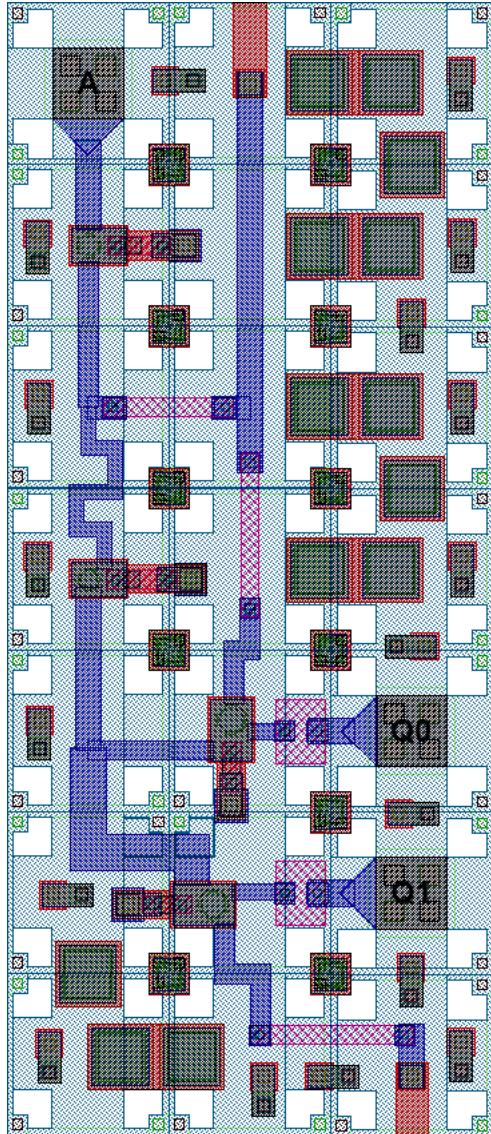


Figure 3.7: RSFQ SPLITT layout.

Analog model

```

1  * Back-annotated simulation file written      53 | .param LP3=LP
2   ↪ by InductEx v.6.1.52 on 2022/08/10.      54 | .param LP4=LP
3  * Author: L. Schindler                      55 |
4  * Version: 3.0                                56 | .param RB1=B0Rs/B1
5  * Last modification date: 10 August 2022     57 | .param RB2=B0Rs/B2
6  * Last modification by: T. Hall              58 | .param RB3=B0Rs/B3
7  *$Ports      a      q0      q1                59 | .param RB4=B0Rs/B4
8 .subckt THmitll_SPLITT a q0 q1              60 |
9 .model jjmit jj(rtype=1, vg=2.8mV, cap      61 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     62 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
   ↪ )                                         63 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
10 .param Phi0=2.067833848E-15                  64 | .param LRB4=(RB4/Rsheet)*Lsheet+LP
11 .param B0=1                                    65 |
12 .param Ic0=0.0001                            66 | B1 1 2 jjmit area=B1
13 .param IcRs=100u*6.859904418                 67 | B2 5 6 jjmit area=B2
14 .param B0Rs=IcRs/Ic0*B0                      68 | B3 8 9 jjmit area=B3
15 .param Rsheet=2                               69 | B4 12 13 jjmit area=B4
16 .param Lsheet=1.13e-12                         70 |
17 .param LP=0.5p                                71 | IB1 0 4 pwl(0 0 5p IB1)
18 .param IC=2.5                                 72 | IB2 0 10 pwl(0 0 5p IB2)
19 .param ICreceive=1.6                          73 | IB3 0 14 pwl(0 0 5p IB3)
20 .param ICtrans=2.5                           74 |
21 .param LB=2p                                  75 | LB1 4 3 4.087E-013
22 .param BiasCoef=0.7                          76 | LB2 10 8 1.617E-012
23 .param Lptl=2p                               77 | LB3 14 12 2.099E-012
24 .param RD=1.36                               78 |
25 |
26 .param B1=1.6                                79 | L1 a 1 1.432E-012
27 .param B2=1.36                               80 | L2 1 3 2.097E-012
28 .param B3=2.5                                81 | L3 3 5 3.589E-012
29 .param B4=2.5                                82 | L4 5 7 1.755E-012
30 |
31 .param IB1=231u                             83 | L5 8 7 1.82E-012
32 .param IB2=175u                             84 | L6 8 11 7.505E-013
33 .param IB3=175u                             85 | L7 7 12 1.805E-012
34 |
35 .param LB1=LB                                86 | L8 12 15 1.137E-012
36 .param LB2=LB                                87 |
37 .param LB3=LB                                88 | RD1 11 q0 RD1
38 |
39 .param L1=Lptl                               89 | RD2 15 q1 RD2
40 .param L2=2.1010p                            90 |
41 .param L3=3.6142p                            91 | LP1 2 0 3.952E-013
42 .param L4=1.7400p                            92 | LP2 6 0 4.754E-013
43 .param L5=1.8162p                            93 | LP3 9 0 3.421E-013
44 .param L6=Lptl                               94 | LP4 13 0 3.856E-013
45 .param L7=1.8162p                            95 |
46 .param L8=Lptl                               96 | RB1 1 101 RB1
47 |
48 .param RD1=RD                               97 | LRB1 101 0 LRB1
49 .param RD2=RD                               98 | RB2 5 105 RB2
50 |
51 .param LP1=LP                                99 | LRB2 105 0 LRB2
52 .param LP2=LP                                100 | RB3 8 108 RB3
          | LRB3 108 0 LRB3
          | RB4 12 112 RB4
          | LRB4 112 0 LRB4
          | .ends

```

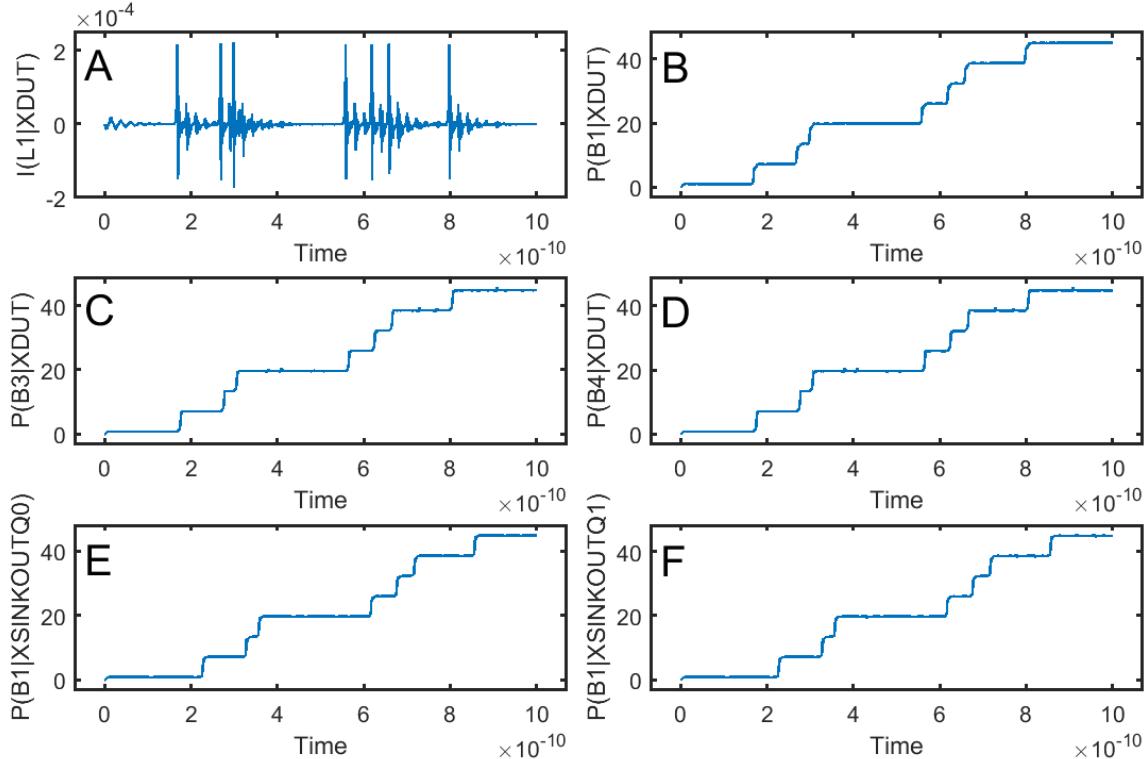
Listing 3.3: RSFQ SPLITT JoSIM netlist.

Table 3.3: RSFQ SPLITT pin list.

Pin	Description
a	Data input
q0	Data output
q1	Data output

The JoSIM simulation results for the RSFQ SPLITT are shown in Fig. 3.8. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q0**,
- (d) the phase over the output JJ of pin **q1**,
- (e) the phase over the input JJ of the load cell connected to pin q0 through a PTL, and
- (f) the phase over the input JJ of the load cell connected to pin q1 through a PTL.

**Figure 3.8:** RSFQ SPLITT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 10 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_SPLITT_v3p0_extracted (a, q0, q1);
9
10 input
11   a;
12
13 output
14   q0, q1;
15
16 reg
17   q0, q1;
18
19 real
20   delay_state0_a_q0 = 7.3,
21   delay_state0_a_q1 = 7.3,
22   ct_state0_a_a = 11.1;
23
24 reg
25   errorsignal_a;
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q0 = 0; // All outputs start at 0
35   q1 = 0; // All outputs start at 0
36 end
37
38 always @(posedge a or negedge a) // execute at positive and negative edges of input
39 begin
40   if ($time>4) // arbitrary steady-state time)
41     begin
42       if (errorsignal_a == 1'b1) // A critical timing is active for this input
43         begin
44           outfile = $fopen("errors.txt", "a");
45           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
46           ↪ ", $stime);
47           $fclose(outfile);
48           q0 <= 1'bX; // Set all outputs to unknown
49           q1 <= 1'bX; // Set all outputs to unknown
50         end
51       if (errorsignal_a == 0)
52         begin
53           case (cell_state)
54             0: begin
55               q0 <= #(delay_state0_a_q0) !q0;
56               q1 <= #(delay_state0_a_q1) !q1;
57               errorsignal_a = 1; // Critical timing on this input; assign
               ↪ immediately
               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 3.4: RSFQ SPLITT verilog model.

The digital simulation results for the RSFQ SPLITT is shown in Fig. 3.9 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.10.



Figure 3.9: RSFQ SPLITT digital simulation results.

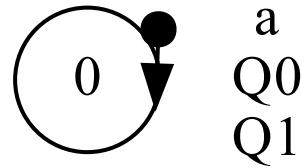


Figure 3.10: RSFQ SPLITT Mealy finite state diagram.

Power consumption

Table 3.4: RSFQ SPLITT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	1510	1.65
2	1510	3.29
5	1510	8.23
10	1510	16.5
20	1510	32.9
50	1510	82.3

3.1.3 MERGET

The MERGET joins two input pulse signal lines and provides a single output pulse signal line. If there is a pulse on either input lines, the MERGET will generate a pulse on the output signal line. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

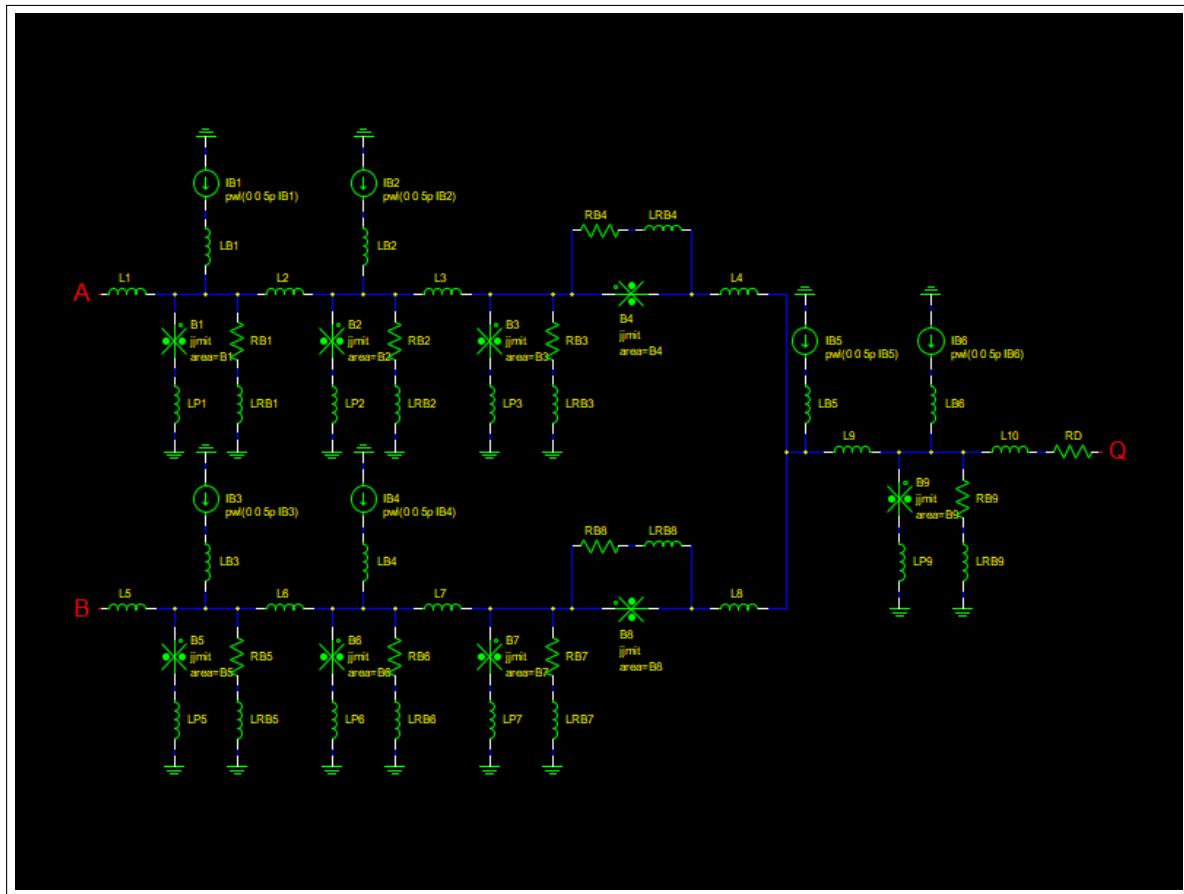


Figure 3.11: Schematic of RSFQ MERGET.

Layout

The physical layout of the RSFQ MERGET is shown in Fig. 3.12. The height of the layout is $70 \mu\text{m}$ and the width is $50 \mu\text{m}$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

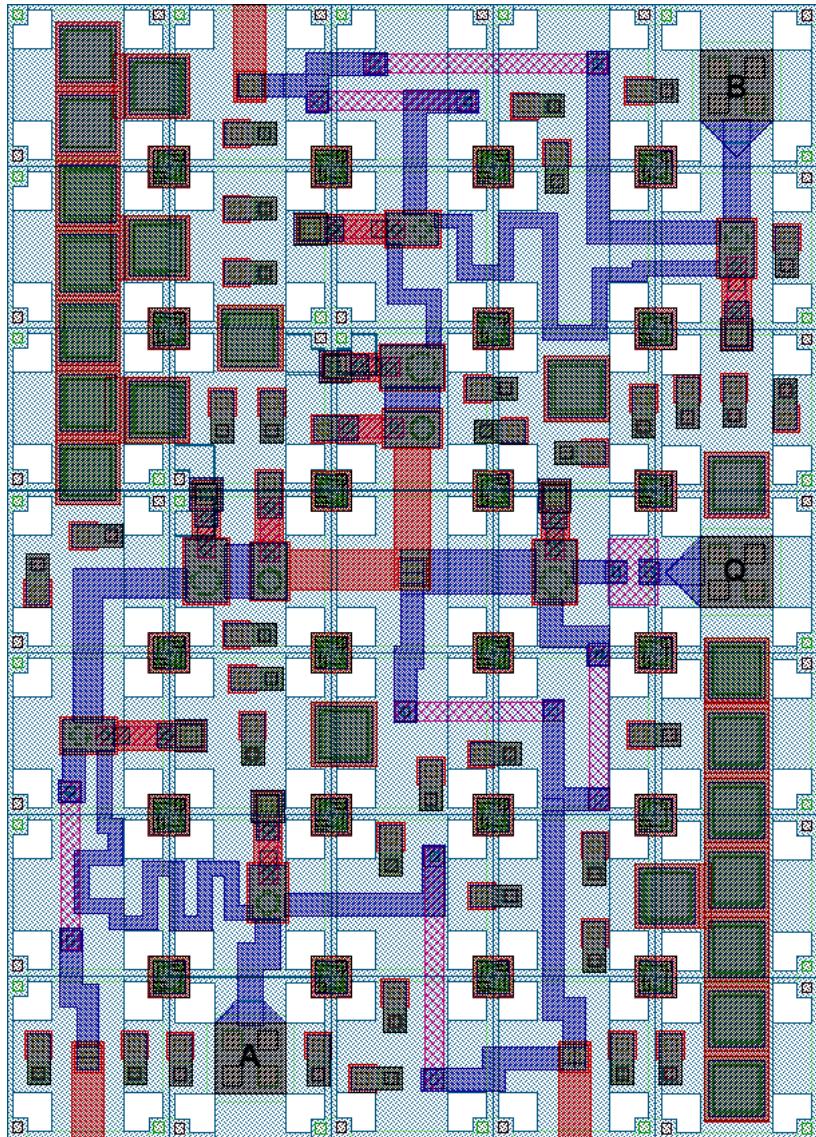


Figure 3.12: RSFQ MERGET layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param LP5=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/08/11.    65  .param LP6=LP
3  * Author: L. Schindler                      66  .param LP7=LP
4  * Version: 3.0                                67  .param LP9=LP
5  * Last modification date: 10 August 2022     68
6  * Last modification by: T. Hall              69  .param RB1=B0Rs/B1
7  *$Ports      a      b      q                 70  .param RB2=B0Rs/B2
8  .subckt THmitll_MERGET a b q               71  .param RB3=B0Rs/B3
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param RB4=B0Rs/B4
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param RB5=B0Rs/B5
   ↪ )                                         74  .param RB6=B0Rs/B6
10 .param Phi0=2.067833848E-15                75  .param RB7=B0Rs/B7
11 .param B0=1                                 76  .param RB8=B0Rs/B8
12 .param Ic0=0.0001                           77  .param RB9=B0Rs/B9
13 .param IcRs=100u*6.859904418                78
14 .param B0Rs=IcRs/Ic0*B0                     79  .param LRB1=(RB1/Rsheet)*Lsheet+LP
15 .param Rsheet=2                            80  .param LRB2=(RB2/Rsheet)*Lsheet+LP
16 .param Lsheet=1.13e-12                      81  .param LRB3=(RB3/Rsheet)*Lsheet+LP
17 .param LP=0.5p                            82  .param LRB4=(RB4/Rsheet)*Lsheet
18 .param IC=2.5                             83  .param LRB5=(RB5/Rsheet)*Lsheet+LP
19 .param ICreceive=1.6                       84  .param LRB6=(RB6/Rsheet)*Lsheet+LP
20 .param ICtrans=2.5                         85  .param LRB7=(RB7/Rsheet)*Lsheet+LP
21 .param LB=2p                             86  .param LRB8=(RB8/Rsheet)*Lsheet
22 .param BiasCoef=0.7                        87  .param LRB9=(RB9/Rsheet)*Lsheet+LP
23 .param Lptl=2p                           88
24 .param RD=1.36                           89  B1 1 2 jjmit area=B1
25                               90  B2 4 5 jjmit area=B2
26 .param B1=1.6                            91  B3 7 8 jjmit area=B3
27 .param B2=1.10                           92  B4 7 9 jjmit area=B4
28 .param B3=2.61                           93  B5 11 12 jjmit area=B5
29 .param B4=1.56                           94  B6 14 15 jjmit area=B6
30 .param B5=1.6                            95  B7 17 18 jjmit area=B7
31 .param B6=1.10                           96  B8 17 19 jjmit area=B8
32 .param B7=2.61                           97  B9 21 22 jjmit area=B9
33 .param B8=1.56                           98
34 .param B9=2.5                            99  IB1 0 3 pwl(0 0 5p IB1)
35                               100 IB2 0 6 pwl(0 0 5p IB2)
36 .param IB1=112u                           101 IB3 0 13 pwl(0 0 5p IB3)
37 .param IB2=170u                           102 IB4 0 16 pwl(0 0 5p IB4)
38 .param IB3=112u                           103 IB5 0 20 pwl(0 0 5p IB5)
39 .param IB4=170u                           104 IB6 0 23 pwl(0 0 5p IB6)
40 .param IB5=171u                           105
41 .param IB6=175u                           106 LB1 3 1 2.504E-012
42                               107 LB2 6 4 7.477E-013
43 .param LB1=LB                            108 LB3 13 11 3.72E-012
44 .param LB2=LB                            109 LB4 16 14 2.115E-012
45 .param LB3=LB                            110 LB5 20 10 1.701E-012
46 .param LB4=LB                            111 LB6 23 21 1.272E-012
47 .param LB5=LB                            112
48 .param LB6=LB                            113 L1 a 1 1.299E-012
49                               114 L2 1 4 8.804E-012
50 .param L1=Lptl                           115 L3 4 7 2.465E-012
51 .param L2=8.8600p                         116 L4 9 10 1.51E-012
52 .param L3=2.4587p                         117 L5 b 11 1.373E-012
53 .param L4=1.5077p                         118 L6 11 14 8.866E-012
54 .param L5=Lptl                           119 L7 14 17 2.459E-012
55 .param L6=8.8600p                         120 L8 19 10 1.516E-012
56 .param L7=2.4587p                         121 L9 10 21 1.002E-012
57 .param L8=1.5077p                         122 L10 21 24 7.408E-013
58 .param L9=1.0056p                         123
59 .param L10=Lptl                          124 RD 24 q RD
60                               125
61 .param LP1=LP                            126 LP1 2 0 4.76E-013
62 .param LP2=LP                            127 LP2 5 0 4.103E-013
63 .param LP3=LP                            128 LP3 8 0 4.056E-013
64                               129 LP5 12 0 3.991E-013

```

```

130 | LP6 15 0 5.058E-013
131 | LP7 18 0 4.187E-013
132 | LP9 22 0 3.717E-013
133 |
134 | RB1 1 101 RB1
135 | LRB1 101 0 LRB1
136 | RB2 4 104 RB2
137 | LRB2 104 0 LRB2
138 | RB3 7 107 RB3
139 | LRB3 107 0 LRB3
140 | RB4 7 109 RB4
141 | LRB4 109 9 LRB4
142 | RB5 11 111 RB5
143 | LRB5 111 0 LRB5
144 | RB6 14 114 RB6
145 | LRB6 114 0 LRB6
146 | RB7 17 117 RB7
147 | LRB7 117 0 LRB7
148 | RB8 17 119 RB8
149 | LRB8 119 19 LRB8
150 | RB9 21 121 RB9
151 | LRB9 121 0 LRB9
152 |
153 | .ends

```

Listing 3.5: RSFQ MERGET JoSIM netlist.**Table 3.5:** RSFQ MERGET pin list.

Pin	Description
a	Data input
b	Data input
q	Data output

The JoSIM simulation results for the RSFQ MERGET are shown in Fig. 3.13. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the phase over the output JJ of pin **q**,
- (f) the phase over the input JJ of the load cell connected to pin **q** via a PTL.

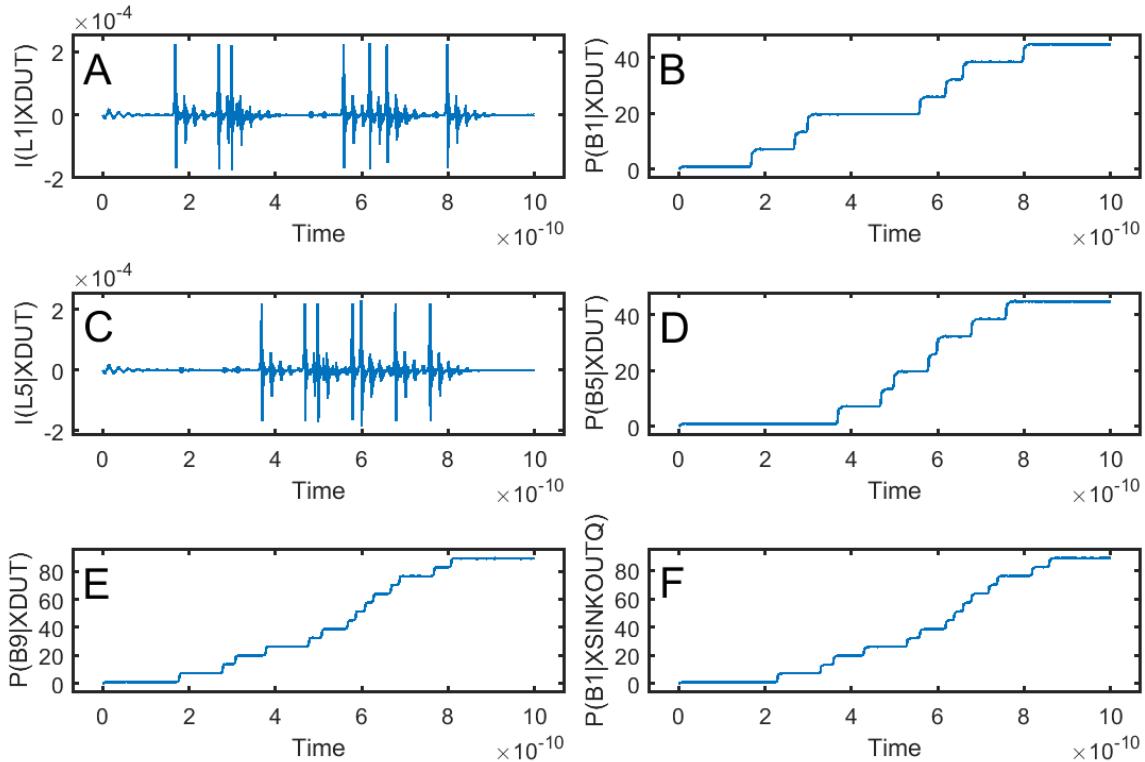


Figure 3.13: RSFQ MERGET analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 11 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_MERGET_v3p0_extracted (a, b, q);
9
10 input
11   a, b;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 9.3,
21   delay_state0_b_q = 9.5,
22   ct_state0_a_a = 9.3,
23   ct_state0_a_b = 3.3,
24   ct_state0_b_a = 3.9,
25   ct_state0_b_b = 9.3;
26
27 reg
28   errorsignal_a,
29   errorsignal_b;
30
31 integer
32   outfile,
33   cell_state; // internal state of the cell
34
35 initial
36 begin
37   errorsignal_a = 0;
38   errorsignal_b = 0;
39   cell_state = 0; // Startup state
40   q = 0; // All outputs start at 0
41 end
42
43 always @(posedge a or negedge a) // execute at positive and negative edges of input
44 begin
45   if ($time>4) // arbitrary steady-state time)
46     begin
47       if (errorsignal_a == 1'b1) // A critical timing is active for this input
48         begin
49           outfile = $fopen("errors.txt", "a");
50           $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n"
51           ↪ ", $stime);
52           $fclose(outfile);
53           q <= 1'bX; // Set all outputs to unknown
54         end
55       if (errorsignal_a == 0)
56         begin
57           case (cell_state)
58             0: begin
59               q <= #(delay_state0_a_q) !q;
60               errorsignal_a = 1; // Critical timing on this input; assign
61               ↪ immediately
62               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
63               ↪ after critical timing expires
64               errorsignal_b = 1; // Critical timing on this input; assign
65               ↪ immediately
66               errorsignal_b <= #(ct_state0_a_b) 0; // Clear error signal
67               ↪ after critical timing expires

```

```

63           end
64       endcase
65     end
66   end
67 end
68
69 always @(posedge b or negedge b) // execute at positive and negative edges of input
70 begin
71   if ($time>4) // arbitrary steady-state time)
72 begin
73   if (errorsignal_b == 1'b1) // A critical timing is active for this input
74 begin
75     outfile = $fopen("errors.txt", "a");
76     $fdisplay(outfile, "Violation of critical timing in module %m; %0d ps.\n
77     ↪ ", $stime);
78     $fclose(outfile);
79     q <= 1'bX; // Set all outputs to unknown
80   end
81   if (errorsignal_b == 0)
82 begin
83     case (cell_state)
84     0: begin
85       q <= #(delay_state0_b_q) !q;
86       errorsignal_a = 1; // Critical timing on this input; assign
87       ↪ immediately
88       errorsignal_a <= #(ct_state0_b_a) 0; // Clear error signal
89       ↪ after critical timing expires
90       errorsignal_b = 1; // Critical timing on this input; assign
91       ↪ immediately
92       errorsignal_b <= #(ct_state0_b_b) 0; // Clear error signal
93       ↪ after critical timing expires
94     end
95   endcase
96 end
97 end
98
99 endmodule

```

Listing 3.6: RSFQ MERGET verilog model.

The digital simulation results for the RSFQ MERGET is shown in Fig. 3.14 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.15.

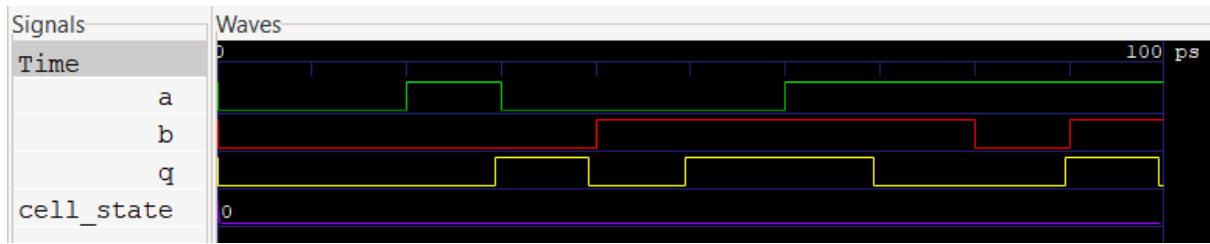


Figure 3.14: RSFQ MERGET digital simulation results.

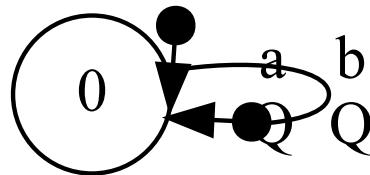


Figure 3.15: RSFQ MERGET Mealy finite state diagram.

Power consumption

Table 3.6: RSFQ MERGET power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2370	3.36
2	2370	6.72
5	2370	16.8
10	2370	33.6
20	2370	67.2
50	2370	168

3.1.4 Always0T Asynchronous

The Always0T Asynchronous cell provides an output which is always zero. Two versions of the cell exist: One with an **a** input port, as seen in Fig. 3.16, and one without an **a** input port, as seen in Fig. 3.17. The cell is designed to connect directly to a PTL.

Schematic

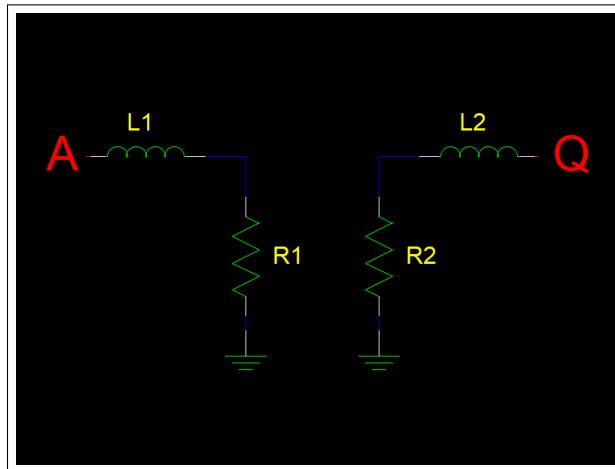


Figure 3.16: Schematic of RSFQ Always0T Asynchronous.

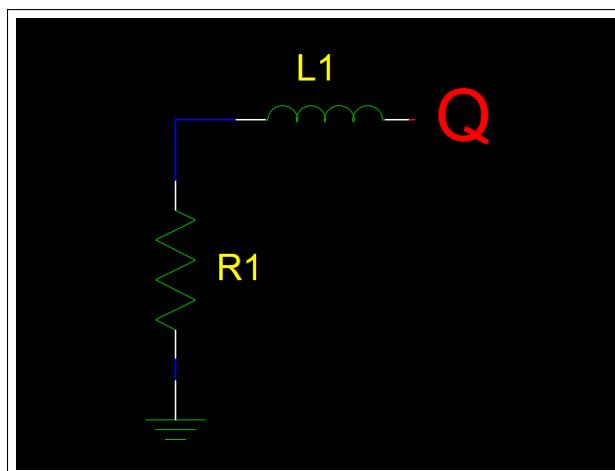


Figure 3.17: Schematic of RSFQ Always0T Asynchronous without an **a** input port.

Layout

The physical layouts of the two RSFQ Always0T Asynchronous cell versions are shown in Fig. 3.18a and 3.18b respectively. The height of the layout for both versions of the cell is $70 \mu m$ and the width is $10 \mu m$. The PTL connection extends to connect to a PTL on either M1 or M3.

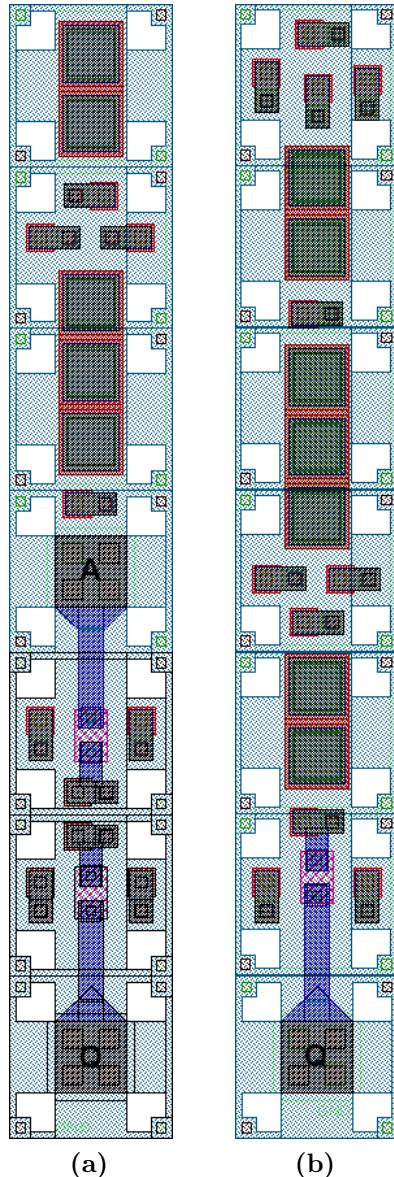


Figure 3.18: The physical layouts for (a) the RSFQ Always0T Asynchronous and (b) the RSFQ Always0T Asynchronous without an **a** input port.

Analog model

```

1 * Back-annotated simulation file written by InductEx v.6.1.52 on 2022/08/26.
2 * Author: L. Schindler
3 * Version: 3.0
4 * Last modification date: 26 August 2022
5 * Last modification by: T. Hall
6
7 *$Ports      a      q
8 .subckt THmitll_ALWAYS0T_ASYNC a q
9 .param Lptl=2p
10
11 .param L1=Lptl
12 .param L2=Lptl
13
14 .param R1=2
15 .param R2=2
16
17 L1 a 1 1.386E-012
18 L2 2 q 1.441E-012
19
20 R1 1 0 R1
21 R2 2 0 R2
22
23 .ends

```

Listing 3.7: RSFQ Always0T Asynchronous JoSIM netlist.

Table 3.7: RSFQ Always0T Asynchronous pin list.

Pin	Description
a	Data input
q	Data output

```

1 * Back-annotated simulation file written by InductEx v.6.1.52 on 2022/08/26.
2 * Author: L. Schindler
3 * Version: 3.0
4 * Last modification date: 26 August 2022
5 * Last modification by: T. Hall
6
7 *$Ports      a      q
8 .subckt THmitll_ALWAYS0T_ASYNC_NOA a q
9
10 .param Lptl=2p
11
12 .param L1=Lptl
13
14 .param RQ=2
15
16 L1 1 q 1.67E-012
17
18 R1 1 0 R1
19
20 .ends

```

Listing 3.8: RSFQ Always0T Asynchronous, without an **a** input port, JoSIM netlist.

Table 3.8: RSFQ Always0T Asynchronous, without an **a** input port, pin list.

Pin	Description
q	Data output

Digital model

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 26 August 2022
5 // Last modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_ALWAYS0T_ASYNC (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 initial
20   begin
21     q = 0; // Output always 0
22   end
23
24 always
25   begin
26     #10 q = 0; // Output always 0
27   end
28 endmodule

```

Listing 3.9: RSFQ Always0T Asynchronous verilog model.

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 26 August 2022
5 // Last modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_ALWAYS0T_ASYNC_NOA (q);
9
10 output
11   q;
12
13 reg
14   q;
15
16 initial
17   begin
18     q = 0; // Output always 0
19   end
20
21 always
22   begin
23     #10 q = 0; // Output always 0
24   end
25
26 endmodule

```

Listing 3.10: RSFQ Always0T Asynchronous, without an **a** input port, verilog model.

3.1.5 Always0T Synchronous

The Always0T Synchronous cell provides an output which is always zero synchronous to a clock signal. Two versions of the cell exist: One with an **a** input port, as seen in Fig. 3.19, and one without an **a** input port, as seen in Fig. 3.20. The cell is designed to connect directly to a PTL.

Schematic

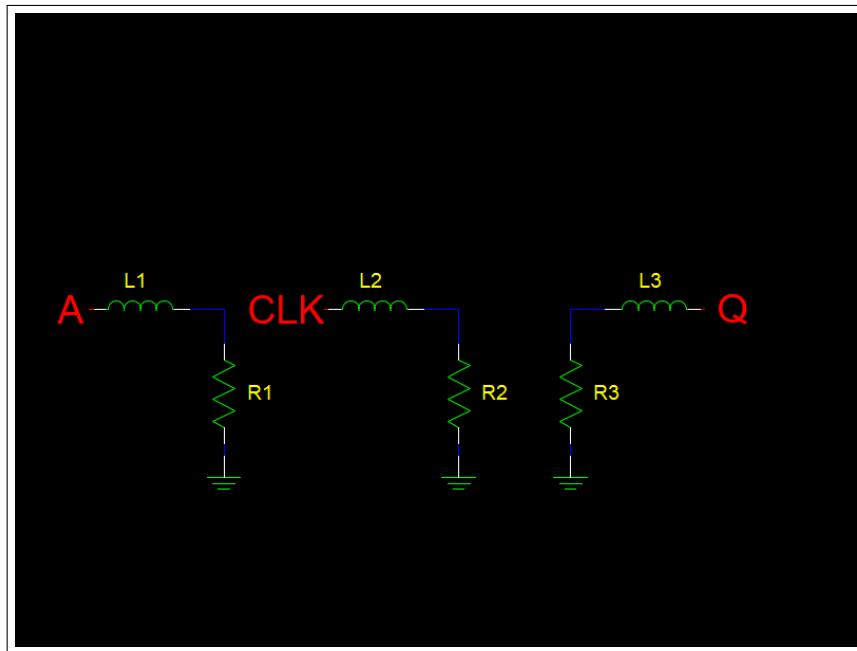


Figure 3.19: Schematic of RSFQ Always0T Synchronous.

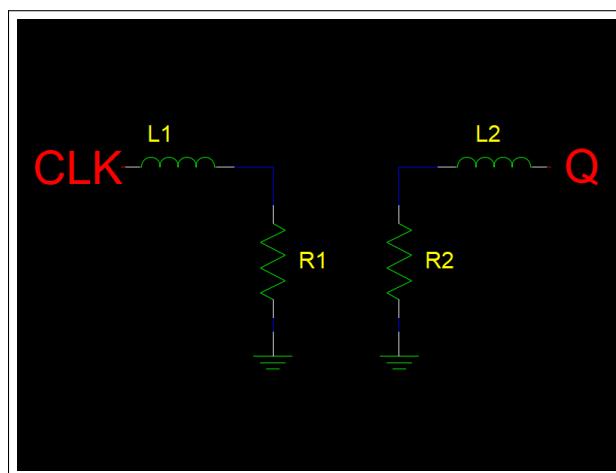


Figure 3.20: Schematic of RSFQ Always0T Synchronous without an **a** input port.

Layout

The physical layouts of the two RSFQ Always0T Synchronous cell versions are shown in Fig. 3.21a and 3.21b respectively. The height for both versions of the Always0T Synchronous layout is $70 \mu m$ and the width is $10 \mu m$. The PTL connection extends to connect to a PTL on either M1 or M3.

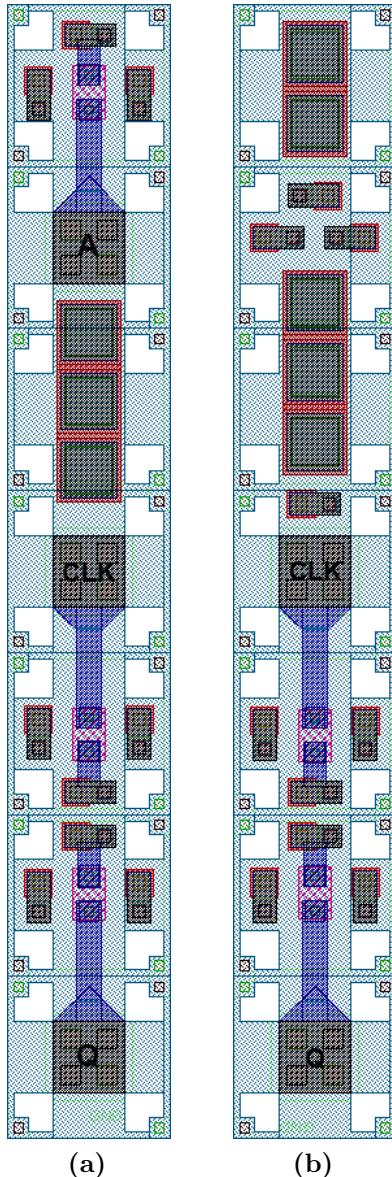


Figure 3.21: The physical layouts for (a) the RSFQ Always0T Synchronous and (b) the RSFQ Always0T Synchronous without an **a** input port.

Analog model

```

1 * Back-annotated simulation file written by InductEx v.6.1.52 on 2022/08/26.
2 * Author: L. Schindler
3 * Version: 3.0
4 * Last modification date: 26 August 2022
5 * Last modification by: T. Hall
6
7 *$Ports      a      q
8 .subckt THmitll_ALWAYS0T_SYNC a q
9 .param Lptl=2p
10 .param L1=Lptl
11 .param L2=Lptl
12 .param L3=Lptl
13 .param R1=2
14 .param R2=2
15 .param R3=2
16 L1 a 1 1.282E-012
17 L2 clk 2 1.401E-012
18 L3 3 q 1.428E-012
19 R1 1 0 R1
20 R2 2 0 R2
21 R3 3 0 R3
22 .ends

```

Listing 3.11: RSFQ Always0T Synchronous JoSIM netlist.

Table 3.9: RSFQ Always0T Synchronous pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

```

1 * Back-annotated simulation file written by InductEx v.6.1.52 on 2022/08/26.
2 * Author: L. Schindler
3 * Version: 3.0
4 * Last modification date: 26 August 2022
5 * Last modification by: T. Hall
6
7 *$Ports      a      q
8 .subckt THmitll_ALWAYS0T_SYNC_NOA a q
9 .param Lptl=2p
10 .param L1=Lptl
11 .param L2=Lptl
12 .param R1=2
13 .param R2=2
14 L1 clk 1 1.386E-012
15 L2 2 q 1.441E-012
16 R1 1 0 R1
17 R2 2 0 R2
18 .ends

```

Listing 3.12: RSFQ Always0T Synchronous, without an **a** input port, JoSIM netlist.

Table 3.10: RSFQ Always0T Synchronous, without an **a** input port, pin list.

Pin	Description
clk	Clock input
q	Data output

Digital model

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 26 August 2022
5 // Last modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_ALWAYS0T_SYNC (a, clk, q);
9
10 input
11   a, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 initial
20   begin
21     q = 0; // Output always 0
22   end
23
24 always @(posedge clk or negedge clk)
25   begin
26     #10 q = 0; // Output always 0
27   end
28 endmodule

```

Listing 3.13: RSFQ Always0T Synchronous verilog model.

```

1 // -----
2 // Author: L. Schindler
3 // Version: 3.0
4 // Last modification date: 26 August 2022
5 // Last modification by: T. Hall
6 //
7 `timescale 1ps/100fs
8 module THmitll_ALWAYS0T_SYNC_NOA ( clk, q);
9
10 input
11   clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 initial
20   begin
21     q = 0; // Output always 0
22   end
23
24 always @(posedge clk or negedge clk)
25   begin
26     #10 q = 0; // Output always 0
27   end
28 endmodule

```

Listing 3.14: RSFQ Always0T Synchronous, without an **a** input port, verilog model.

3.2 Logic Cells

3.2.1 AND2T

The RSFQ AND2T cell generates an output pulse if pulses from both input signal lines were received before the clock signal. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

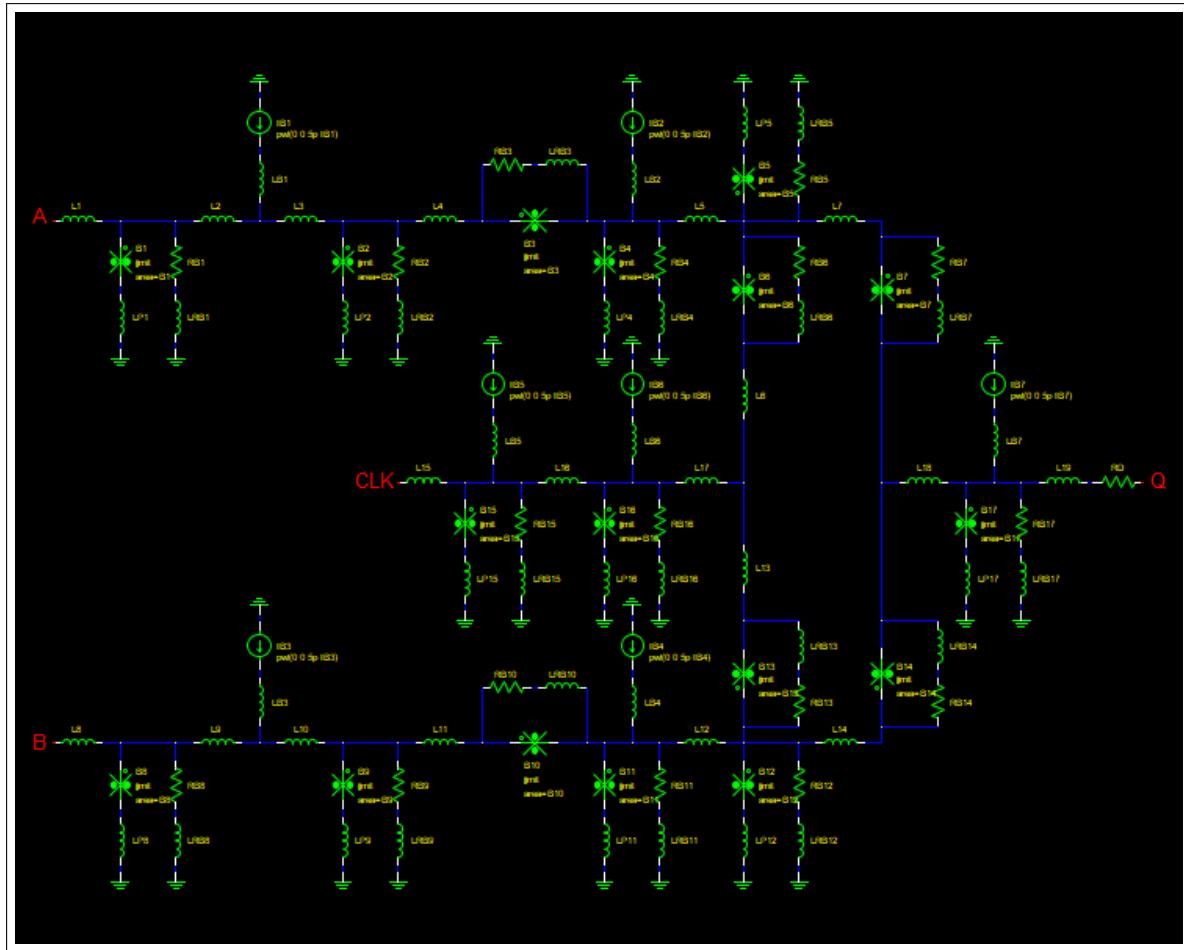


Figure 3.22: Schematic of RSFQ AND2T.

Layout

The physical layout of the RSFQ AND2T is shown in Fig. 3.23. The layout height is $70 \mu m$ and the width is $50 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

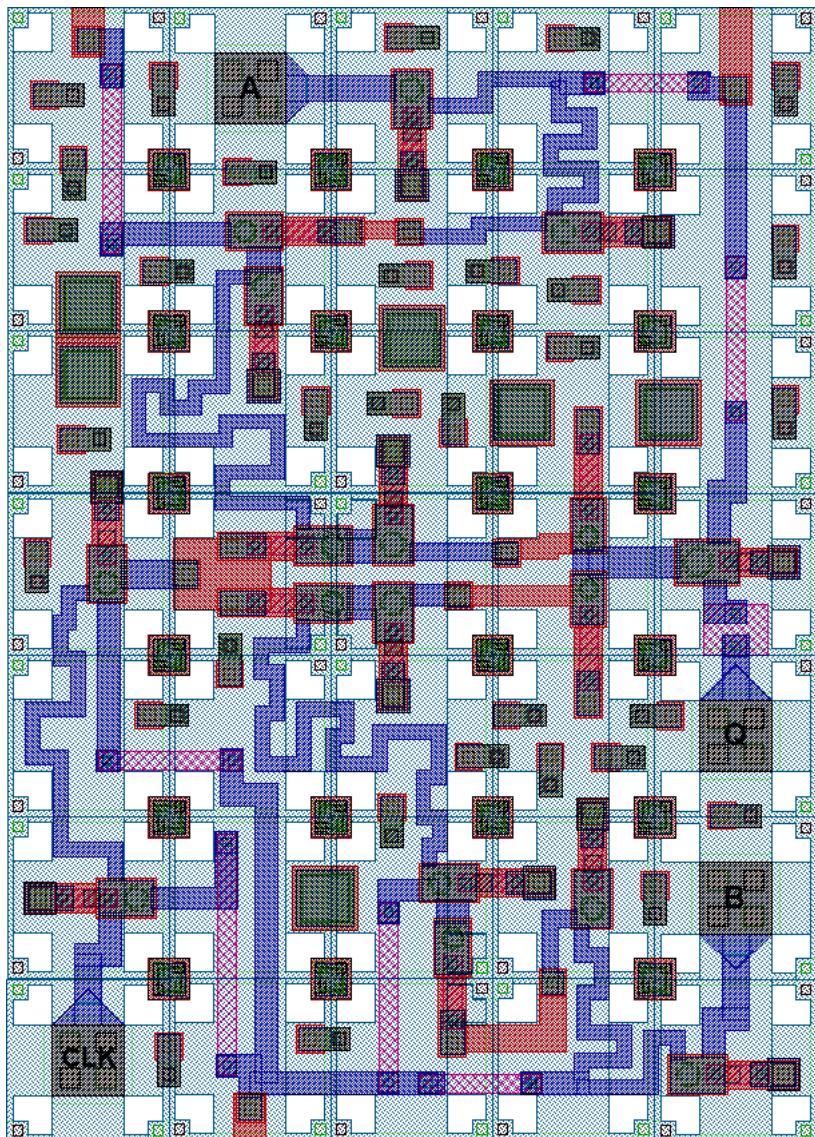


Figure 3.23: RSFQ AND2T Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param L5=10.8125p
2  *   ↪ by InductEx v.6.1.52 on 2022/08/23.    65  .param L6=0.8299p
3  * Author: L. Schindler                      66  .param L7=2.6546p
4  * Version: 3.0                                67  .param L8=Lptl
5  * Last modification date: 23 August 2022     68  .param L9=2.7125p
6  * Last modification by: T. Hall              69  .param L10=3.6844p
7  *$Ports      a      b      clk      q      70  .param L11=4.4946p
8  .subckt THmitll_AND2T a b clk q            71  .param L12=10.8125p
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param L13=0.8299p
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param L14=2.6546p
   ↪ )                                         74  .param L15=Lptl
10 .param Phi0=2.067833848E-15                75  .param L16=7.3588p
11 .param B0=1                                 76  .param L17=1.0183p
12 .param Ic0=0.0001                           77  .param L18=0.9951p
13 .param IcRs=100u*6.859904418               78  .param L19=Lptl
14 .param B0Rs=IcRs/Ic0*B0                   79
15 .param Rsheet=2                            80  .param LP1=LP
16 .param Lsheet=1.13e-12                     81  .param LP2=LP
17 .param LP=0.5p                            82  .param LP4=LP
18 .param IC=2.5                             83  .param LP5=LP
19 .param ICreceive=1.6                      84  .param LP8=LP
20 .param ICtrans=2.5                        85  .param LP9=LP
21 .param LB=2p                             86  .param LP11=LP
22 .param BiasCoef=0.7                      87  .param LP12=LP
23 .param Lptl=2p                           88  .param LP15=LP
24 .param RD=1.36                           89  .param LP16=LP
25                                     90  .param LP17=LP
26 .param B1=1.6                            91
27 .param B2=1.66                           92  .param RB1=B0Rs/B1
28 .param B3=1.26                           93  .param RB2=B0Rs/B2
29 .param B4=1.44                           94  .param RB3=B0Rs/B3
30 .param B5=1.79                           95  .param RB4=B0Rs/B4
31 .param B6=1.41                           96  .param RB5=B0Rs/B5
32 .param B7=1.03                           97  .param RB6=B0Rs/B6
33 .param B8=1.6                            98  .param RB7=B0Rs/B7
34 .param B9=1.66                           99  .param RB8=B0Rs/B8
35 .param B10=1.26                          100 .param RB9=B0Rs/B9
36 .param B11=1.44                          101 .param RB10=B0Rs/B10
37 .param B12=1.79                          102 .param RB11=B0Rs/B11
38 .param B13=1.41                          103 .param RB12=B0Rs/B12
39 .param B14=1.03                          104 .param RB13=B0Rs/B13
40 .param B15=1.6                           105 .param RB14=B0Rs/B14
41 .param B16=1.56                          106 .param RB15=B0Rs/B15
42 .param B17=2.5                           107 .param RB16=B0Rs/B16
43                                     108 .param RB17=B0Rs/B17
44 .param IB1=249u                           109
45 .param IB2=148u                           110 .param LRB1=(RB1/Rsheet)*Lsheet+LP
46 .param IB3=249u                           111 .param LRB2=(RB2/Rsheet)*Lsheet+LP
47 .param IB4=148u                           112 .param LRB3=(RB3/Rsheet)*Lsheet
48 .param IB5=112u                           113 .param LRB4=(RB4/Rsheet)*Lsheet+LP
49 .param IB6=203u                           114 .param LRB5=(RB5/Rsheet)*Lsheet+LP
50 .param IB7=175u                           115 .param LRB6=(RB6/Rsheet)*Lsheet
51                                     116 .param LRB7=(RB7/Rsheet)*Lsheet
52 .param LB1=LB                            117 .param LRB8=(RB8/Rsheet)*Lsheet+LP
53 .param LB2=LB                            118 .param LRB9=(RB9/Rsheet)*Lsheet+LP
54 .param LB3=LB                            119 .param LRB10=(RB10/Rsheet)*Lsheet
55 .param LB4=LB                            120 .param LRB11=(RB11/Rsheet)*Lsheet+LP
56 .param LB5=LB                            121 .param LRB12=(RB12/Rsheet)*Lsheet+LP
57 .param LB6=LB                            122 .param LRB13=(RB13/Rsheet)*Lsheet
58 .param LB7=LB                            123 .param LRB14=(RB14/Rsheet)*Lsheet
59                                     124 .param LRB15=(RB15/Rsheet)*Lsheet+LP
60 .param L1=Lptl                           125 .param LRB16=(RB16/Rsheet)*Lsheet+LP
61 .param L2=2.7125p                         126 .param LRB17=(RB17/Rsheet)*Lsheet+LP
62 .param L3=3.6844p                         127
63 .param L4=4.4946p                         128 B1 1 2 jjmit area=B1
                                         129 B2 5 6 jjmit area=B2

```

```

130 | B3 7 8 jjmit area=B3          182 | RD 40 q RD
131 | B4 8 9 jjmit area=B4          183 |
132 | B5 11 12 jjmit area=B5         184 | LP1 2 0 3.818E-013
133 | B6 11 13 jjmit area=B6         185 | LP2 6 0 5.451E-013
134 | B7 15 16 jjmit area=B7         186 | LP4 9 0 7.058E-013
135 | B8 17 18 jjmit area=B8         187 | LP5 0 12 7.873E-013
136 | B9 21 22 jjmit area=B9         188 | LP8 18 0 4.185E-013
137 | B10 23 24 jjmit area=B10        189 | LP9 22 0 5.92E-013
138 | B11 24 25 jjmit area=B11        190 | LP11 25 0 4.503E-013
139 | B12 27 28 jjmit area=B12        191 | LP12 28 0 7.626E-013
140 | B13 27 29 jjmit area=B13        192 | LP15 32 0 3.764E-013
141 | B14 30 16 jjmit area=B14        193 | LP16 35 0 5.096E-013
142 | B15 31 32 jjmit area=B15        194 | LP17 38 0 3.396E-013
143 | B16 34 35 jjmit area=B16        195 |
144 | B17 37 38 jjmit area=B17        196 | RB1 1 101 RB1
145 |                               197 | LRB1 101 0 LRB1
146 | IB1 0 4 pwl(0 0 5p IB1)        198 | RB2 5 105 RB2
147 | IB2 0 10 pwl(0 0 5p IB2)       199 | LRB2 105 0 LRB2
148 | IB3 0 20 pwl(0 0 5p IB3)       200 | RB3 7 107 RB3
149 | IB4 0 26 pwl(0 0 5p IB4)       201 | LRB3 107 8 LRB3
150 | IB5 0 33 pwl(0 0 5p IB5)       202 | RB4 8 108 RB4
151 | IB6 0 36 pwl(0 0 5p IB6)       203 | LRB4 108 0 LRB4
152 | IB7 0 39 pwl(0 0 5p IB7)       204 | RB5 111 11 RB5
153 |                               205 | LRB5 0 111 LRB5
154 | LB1 4 3 5.738E-013           206 | RB6 11 113 RB6
155 | LB2 10 8 1.925E-012          207 | LRB6 113 13 LRB6
156 | LB3 20 19 8.945E-013          208 | RB7 15 115 RB7
157 | LB4 26 24 8.334E-013          209 | LRB7 115 16 LRB7
158 | LB5 33 31 1.882E-012          210 | RB8 17 117 RB8
159 | LB6 36 34 2.156E-012          211 | LRB8 117 0 LRB8
160 | LB7 39 37 1.99E-012          212 | RB9 21 121 RB9
161 |                               213 | LRB9 121 0 LRB9
162 | L1 a 1 1.421E-012            214 | RB10 23 123 RB10
163 | L2 1 3 2.715E-012            215 | LRB10 123 24 LRB10
164 | L3 3 5 3.674E-012            216 | RB11 24 124 RB11
165 | L4 5 7 4.505E-012            217 | LRB11 124 0 LRB11
166 | L5 8 11 1.08E-011            218 | RB12 27 127 RB12
167 | L6 13 14 8.262E-013          219 | LRB12 127 0 LRB12
168 | L7 11 15 2.657E-012          220 | RB13 129 27 RB13
169 | L8 b 17 1.744E-012            221 | LRB13 129 29 LRB13
170 | L9 17 19 2.706E-012            222 | RB14 130 30 RB14
171 | L10 19 21 3.675E-012           223 | LRB14 16 130 LRB14
172 | L11 21 23 4.485E-012           224 | RB15 31 131 RB15
173 | L12 24 27 1.081E-011           225 | LRB15 131 0 LRB15
174 | L13 14 29 8.334E-013           226 | RB16 34 134 RB16
175 | L14 27 30 2.652E-012           227 | LRB16 134 0 LRB16
176 | L15 clk 31 1.606E-012           228 | RB17 37 137 RB17
177 | L16 31 34 7.368E-012           229 | LRB17 137 0 LRB17
178 | L17 34 14 1.014E-012           230 |
179 | L18 16 37 9.896E-013           231 | .ends
180 | L19 37 40 7.389E-013           181 |

```

Listing 3.15: RSFQ AND2T JoSIM netlist.**Table 3.11:** RSFQ AND2T pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ AND2T using JoSIM is shown in Fig. 3.24. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

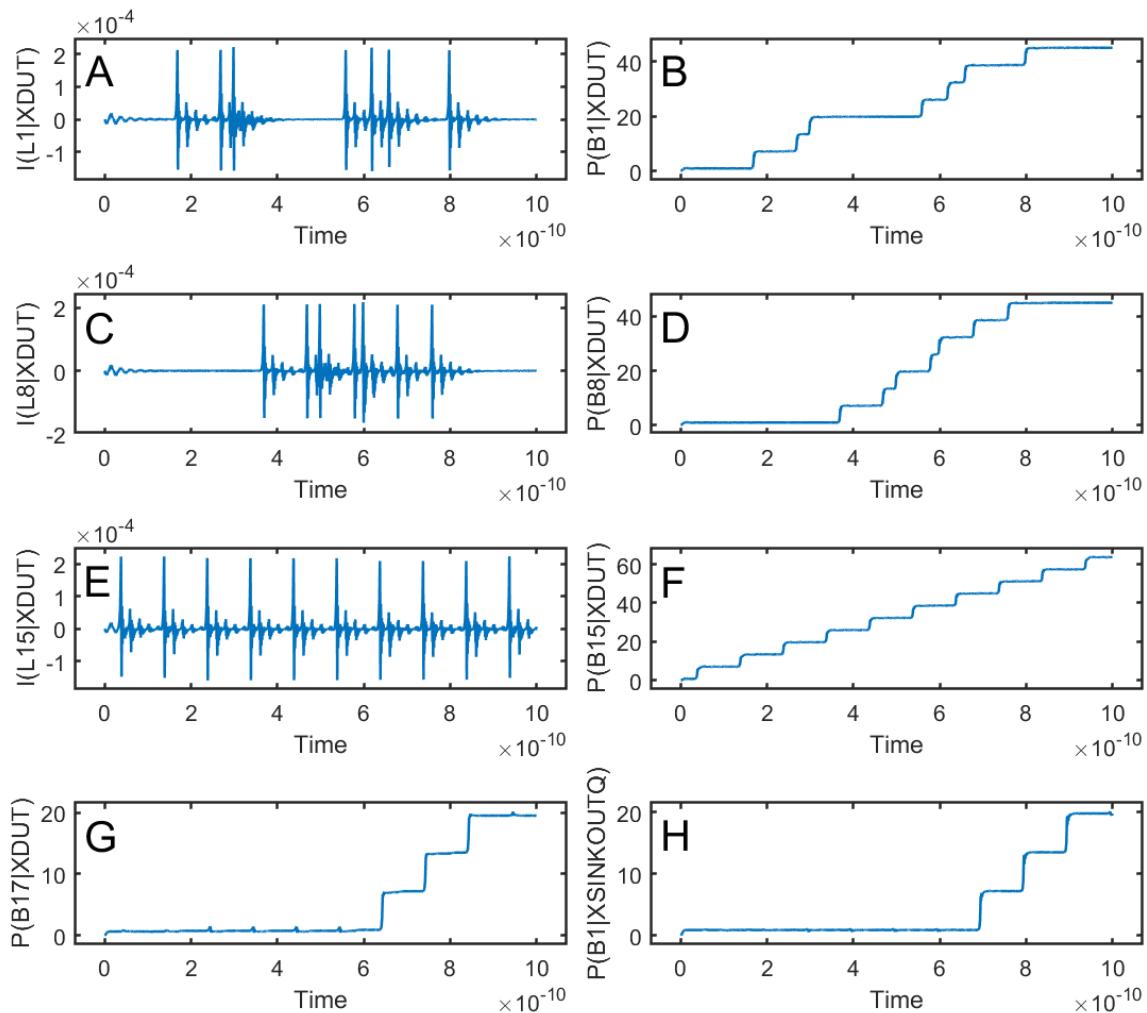


Figure 3.24: RSFQ AND2T analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 23 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_AND2T_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state3_clk_q = 5.7,
21   ct_state0_clk_a = 2.7,
22   ct_state0_clk_b = 2.7,
23   ct_state1_clk_a = 0.3,
24   ct_state1_clk_b = 1.0,
25   ct_state2_clk_a = 1.0,
26   ct_state3_a_clk = 1.4,
27   ct_state3_b_clk = 1.5;
28
29 reg
30   errorsignal_a,
31   errorsignal_b,
32   errorsignal_clk;
33
34 integer
35   outfile,
36   cell_state; // internal state of the cell
37
38 initial
39 begin
40   errorsignal_a = 0;
41   errorsignal_b = 0;
42   errorsignal_clk = 0;
43   cell_state = 0; // Startup state
44   q = 0; // All outputs start at 0
45 end
46
47 always @(posedge a or negedge a) // execute at positive and negative edges of input
48 begin
49   if ($time>4) // arbitrary steady-state time)
50     begin
51       if (errorsignal_a == 1'b1) // A critical timing is active for this input
52         begin
53           outfile = $fopen("errors.txt", "a");
54           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
55           ↪ ", $stime);
56           $fclose(outfile);
57           q <= 1'bX; // Set all outputs to unknown
58         end
59       if (errorsignal_a == 0)
60         begin
61           case (cell_state)
62             0: begin
63               cell_state = 1; // Blocking statement -- immediately
64             end
65             1: begin
66               end
67             2: begin

```

```

67           cell_state = 3; // Blocking statement -- immediately
68       end
69   3: begin
70       errorsignal_clk = 1; // Critical timing on this input; assign
71           ↪ immediately
72       errorsignal_clk <= #(ct_state3_a_clk) 0; // Clear error signal
73           ↪ after critical timing expires
74   endcase
75   end
76 end
77
78 always @(posedge b or negedge b) // execute at positive and negative edges of input
79 begin
80     if ($time>4) // arbitrary steady-state time)
81     begin
82         if (errorsignal_b == 1'b1) // A critical timing is active for this input
83         begin
84             outfile = $fopen("errors.txt", "a");
85             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
86                         ↪ ", $stime);
87             $fclose(outfile);
88             q <= 1'bX; // Set all outputs to unknown
89         end
90         if (errorsignal_b == 0)
91         begin
92             case (cell_state)
93                 0: begin
94                     cell_state = 2; // Blocking statement -- immediately
95                 end
96                 1: begin
97                     cell_state = 3; // Blocking statement -- immediately
98                 end
99                 2: begin
100                end
101                3: begin
102                    errorsignal_clk = 1; // Critical timing on this input; assign
103                        ↪ immediately
104                    errorsignal_clk <= #(ct_state3_b_clk) 0; // Clear error signal
105                        ↪ after critical timing expires
106                end
107            endcase
108        end
109    always @(posedge clk or negedge clk) // execute at positive and negative edges of input
110    begin
111        if ($time>4) // arbitrary steady-state time)
112        begin
113            if (errorsignal_clk == 1'b1) // A critical timing is active for this input
114            begin
115                outfile = $fopen("errors.txt", "a");
116                $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
117                            ↪ ", $stime);
118                $fclose(outfile);
119                q <= 1'bX; // Set all outputs to unknown
120            end
121            if (errorsignal_clk == 0)
122            begin
123                case (cell_state)
124                    0: begin
125                        errorsignal_a = 1; // Critical timing on this input; assign
126                            ↪ immediately
127                        errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
128                            ↪ after critical timing expires
129                        errorsignal_b = 1; // Critical timing on this input; assign
130                            ↪ immediately
131                        errorsignal_b <= #(ct_state0_clk_b) 0; // Clear error signal

```

```

128          ↪ after critical timing expires
129      end
130  1: begin
131      cell_state = 0; // Blocking statement -- immediately
132      errorsignal_a = 1; // Critical timing on this input; assign
133          ↪ immediately
134      errorsignal_a <= #(ct_state1_clk_a) 0; // Clear error signal
135          ↪ after critical timing expires
136      errorsignal_b = 1; // Critical timing on this input; assign
137          ↪ immediately
138      errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
139          ↪ after critical timing expires
140  end
141  2: begin
142      cell_state = 0; // Blocking statement -- immediately
143      errorsignal_a = 1; // Critical timing on this input; assign
144          ↪ immediately
145      errorsignal_a <= #(ct_state2_clk_a) 0; // Clear error signal
146          ↪ after critical timing expires
147  end
148  end
149 endmodule

```

Listing 3.16: RSFQ AND2T verilog model.

The digital simulation results for the RSFQ AND2T is shown in Fig. 3.25 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.26.

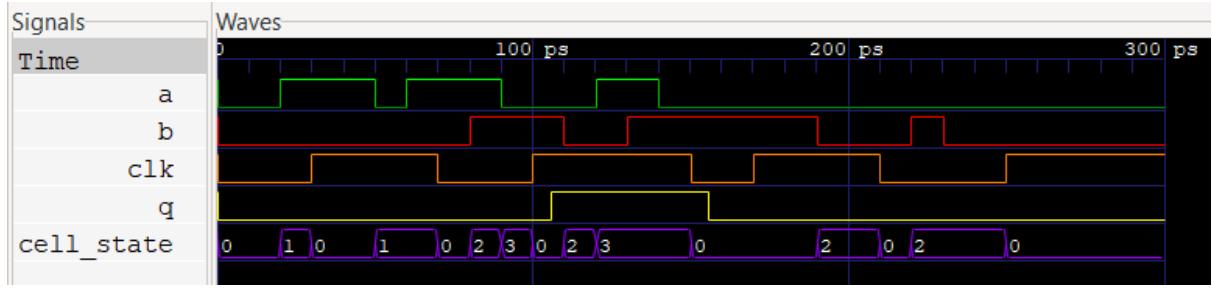


Figure 3.25: RSFQ AND2T digital simulation results.

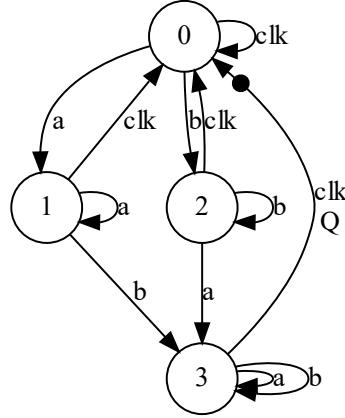


Figure 3.26: RSFQ AND2T Mealy finite state machine diagram.

Power Consumption

Table 3.12: RSFQ AND2T power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	3340	5.38
2	3340	10.8
5	3340	26.9
10	3340	53.8
20	3340	108
50	3340	269

3.2.2 OR2T

The RSFQ OR2T cell generates an output pulse if an input pulse from either input lines was received before the clock signal. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

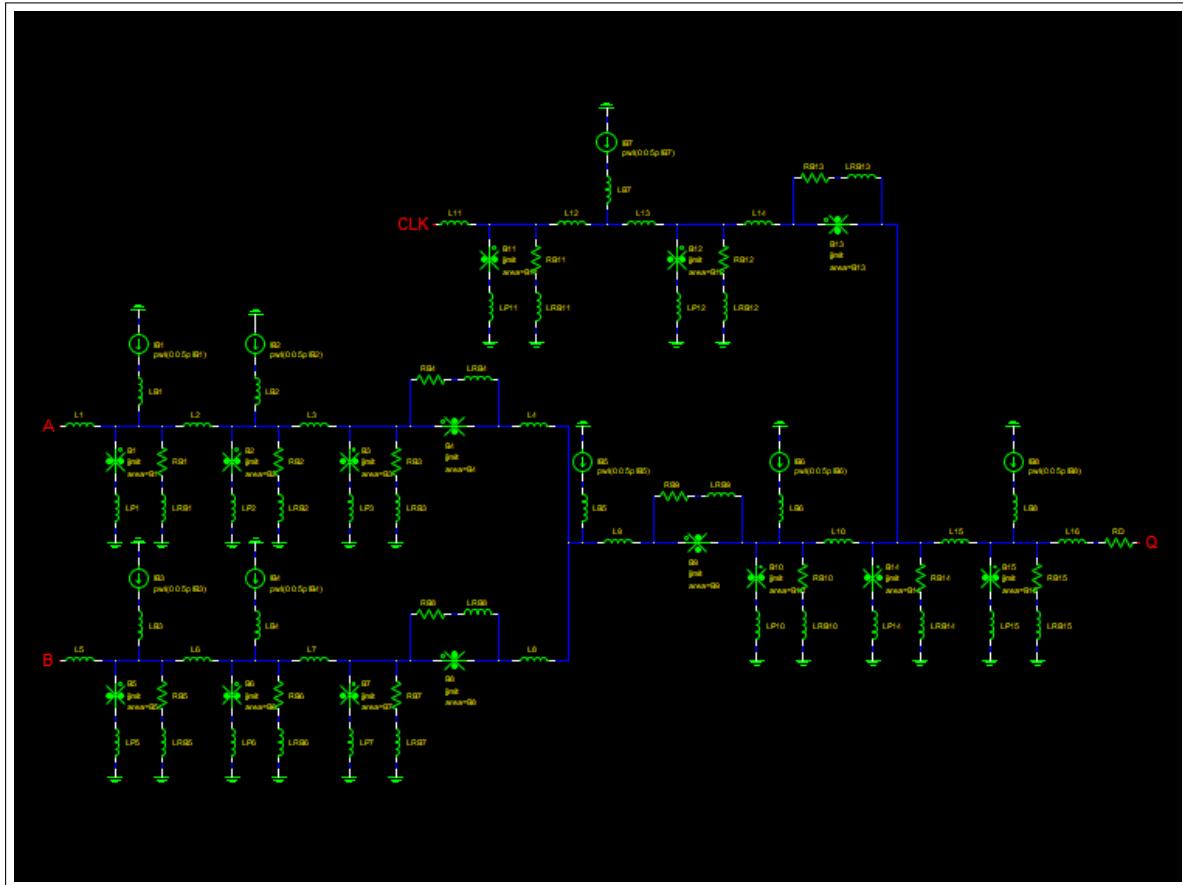


Figure 3.27: Schematic of RSFQ OR2T.

Layout

The physical layout for the RSFQ OR2T is shown in Fig. 3.28. The layout height is $70 \mu m$ and the width is $40 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

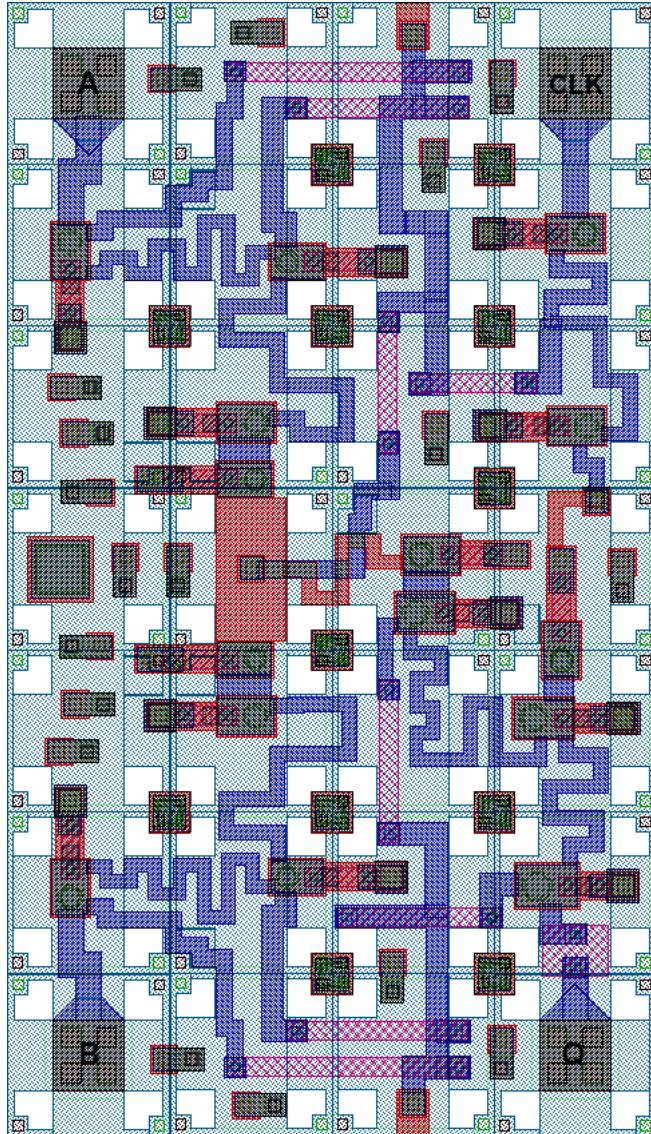


Figure 3.28: RSFQ OR2T Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param L5=Lptl
2   ↪ by InductEx v.6.1.52 on 2022/08/18.      65  .param L6=6.7019p
3  * Author: L. Schindler                      66  .param L7=6.2519p
4  * Version: 3.0                                67  .param L8=0.7723p
5  * Last modification date: 16 August 2022     68  .param L9=4.6089p
6  * Last modification by: T. Hall              69  .param L10=7.7141p
7  *$ports      a      b      clk      q      70  .param L11=Lptl
8  .subckt THmitll_OR2T a b clk q             71  .param L12=2.7407p
9   .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param L13=3.4070p
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     73  .param L14=4.5212p
   ↪ )                                         74  .param L15=4.5560p
10 .param Phi0=2.067833848E-15                75  .param L16=Lptl
11 .param B0=1                                 76
12 .param Ic0=0.0001                           77  .param LP1=LP
13 .param IcRs=100u*6.859904418               78  .param LP2=LP
14 .param B0Rs=IcRs/Ic0*B0                   79  .param LP3=LP
15 .param Rsheet=2                            80  .param LP5=LP
16 .param Lsheet=1.13e-12                     81  .param LP6=LP
17 .param LP=0.5p                            82  .param LP7=LP
18 .param IC=2.5                             83  .param LP10=LP
19 .param ICreceive=1.6                      84  .param LP11=LP
20 .param ICtrans=2.5                        85  .param LP12=LP
21 .param LB=2p                             86  .param LP14=LP
22 .param BiasCoef=0.7                      87  .param LP15=LP
23 .param Lptl=2p                           88
24 .param RD=1.36                           89  .param RB1=B0Rs/B1
25                               90  .param RB2=B0Rs/B2
26  .param B1=1.6                            91  .param RB3=B0Rs/B3
27  .param B2=1.28                           92  .param RB4=B0Rs/B4
28  .param B3=1.65                           93  .param RB5=B0Rs/B5
29  .param B4=1.25                           94  .param RB6=B0Rs/B6
30  .param B5=1.6                           95  .param RB7=B0Rs/B7
31  .param B6=1.28                           96  .param RB8=B0Rs/B8
32  .param B7=1.65                           97  .param RB9=B0Rs/B9
33  .param B8=1.25                           98  .param RB10=B0Rs/B10
34  .param B9=1.67                           99  .param RB11=B0Rs/B11
35  .param B10=1.95                          100 .param RB12=B0Rs/B12
36  .param B11=1.6                           101 .param RB13=B0Rs/B13
37  .param B12=1.59                          102 .param RB14=B0Rs/B14
38  .param B13=1.44                          103 .param RB15=B0Rs/B15
39  .param B14=2.09                          104
40  .param B15=2.5                           105 .param LRB1=(RB1/Rsheet)*Lsheet+LP
41                               106 .param LRB2=(RB2/Rsheet)*Lsheet+LP
42  .param IB1=112u                           107 .param LRB3=(RB3/Rsheet)*Lsheet+LP
43  .param IB2=156u                           108 .param LRB4=(RB4/Rsheet)*Lsheet
44  .param IB3=112u                           109 .param LRB5=(RB5/Rsheet)*Lsheet+LP
45  .param IB4=156u                           110 .param LRB6=(RB6/Rsheet)*Lsheet+LP
46  .param IB5=210u                           111 .param LRB7=(RB7/Rsheet)*Lsheet+LP
47  .param IB6=176u                           112 .param LRB8=(RB8/Rsheet)*Lsheet
48  .param IB7=242u                           113 .param LRB9=(RB9/Rsheet)*Lsheet
49  .param IB8=175u                           114 .param LRB10=(RB10/Rsheet)*Lsheet+LP
50                               115 .param LRB11=(RB11/Rsheet)*Lsheet+LP
51  .param LB1=LB                            116 .param LRB12=(RB12/Rsheet)*Lsheet+LP
52  .param LB2=LB                            117 .param LRB13=(RB13/Rsheet)*Lsheet
53  .param LB3=LB                            118 .param LRB14=(RB14/Rsheet)*Lsheet+LP
54  .param LB4=LB                            119 .param LRB15=(RB15/Rsheet)*Lsheet+LP
55  .param LB5=LB                           120
56  .param LB6=LB                           121 B1 1 2 jjmit area=B1
57  .param LB7=LB                           122 B2 4 5 jjmit area=B2
58  .param LB8=LB                           123 B3 7 8 jjmit area=B3
59                               124 B4 7 9 jjmit area=B4
60  .param L1=Lptl                           125 B5 11 12 jjmit area=B5
61  .param L2=6.7019p                         126 B6 14 15 jjmit area=B6
62  .param L3=6.2519p                         127 B7 17 18 jjmit area=B7
63  .param L4=0.7723p                         128 B8 17 19 jjmit area=B8
64                               129 B9 21 22 jjmit area=B9

```

```

130 | B10 22 23 jjmit area=B10
131 | B11 26 27 jjmit area=B11
132 | B12 30 31 jjmit area=B12
133 | B13 32 25 jjmit area=B13
134 | B14 25 33 jjmit area=B14
135 | B15 34 35 jjmit area=B15
136 |
137 | IB1 0 3 pwl(0 0 5p IB1)
138 | IB2 0 6 pwl(0 0 5p IB2)
139 | IB3 0 13 pwl(0 0 5p IB3)
140 | IB4 0 16 pwl(0 0 5p IB4)
141 | IB5 0 20 pwl(0 0 5p IB5)
142 | IB6 0 24 pwl(0 0 5p IB6)
143 | IB7 0 29 pwl(0 0 5p IB7)
144 | IB8 0 36 pwl(0 0 5p IB8)
145 |
146 | LB1 3 1 4.448E-012
147 | LB2 6 4 2.203E-012
148 | LB3 13 11 4.442E-012
149 | LB4 16 14 2.187E-012
150 | LB5 20 10 3.603E-012
151 | LB6 24 22 1.443E-012
152 | LB7 29 28 1.069E-012
153 | LB8 36 34 8.669E-013
154 |
155 | L1 a 1 1.444E-012
156 | L2 1 4 6.665E-012
157 | L3 4 7 6.254E-012
158 | L4 9 10 7.702E-013
159 | L5 b 11 1.443E-012
160 | L6 11 14 6.656E-012
161 | L7 14 17 6.244E-012
162 | L8 19 10 7.773E-013
163 | L9 10 21 4.573E-012
164 | L10 22 25 7.702E-012
165 | L11 clk 26 1.282E-012
166 | L12 26 28 2.735E-012
167 | L13 28 30 3.418E-012
168 | L14 30 32 4.48E-012
169 | L15 25 34 4.553E-012
170 | L16 34 37 8.104E-013
171 |
172 | RD 37 q RD
173 |
174 | LP1 2 0 4.195E-013
175 | LP2 5 0 5.813E-013
176 | LP3 8 0 4.455E-013
177 | LP5 12 0 4.193E-013
178 | LP6 15 0 5.831E-013
179 | LP7 18 0 4.774E-013
180 | LP10 23 0 4.819E-013
181 | LP11 27 0 3.541E-013
182 | LP12 31 0 4.657E-013
183 | LP14 33 0 4.19E-013
184 | LP15 35 0 3.333E-013
185 |
186 | RB1 1 101 RB1
187 | LRB1 101 0 LRB1
188 | RB2 4 104 RB2
189 | LRB2 104 0 LRB2
190 | RB3 7 107 RB3
191 | LRB3 107 0 LRB3
192 | RB4 7 109 RB4
193 | LRB4 109 9 LRB4
194 | RB5 11 111 RB5
195 | LRB5 111 0 LRB5
196 | RB6 14 114 RB6
197 | LRB6 114 0 LRB6
198 | RB7 17 117 RB7
199 | LRB7 117 0 LRB7
200 | RB8 17 119 RB8
201 | LRB8 119 19 LRB8
202 | RB9 21 121 RB9
203 | LRB9 121 22 LRB9
204 | RB10 22 122 RB10
205 | LRB10 122 0 LRB10
206 | RB11 26 126 RB11
207 | LRB11 126 0 LRB11
208 | RB12 30 130 RB12
209 | LRB12 130 0 LRB12
210 | RB13 32 132 RB13
211 | LRB13 132 25 LRB13
212 | RB14 25 125 RB14
213 | LRB14 125 0 LRB14
214 | RB15 34 134 RB15
215 | LRB15 134 0 LRB15
216 |
217 | .ends

```

Listing 3.17: RSFQ OR2T JoSIM netlist.**Table 3.13:** RSFQ OR2T pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ OR2T using JoSIM is shown in Fig. 3.29. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

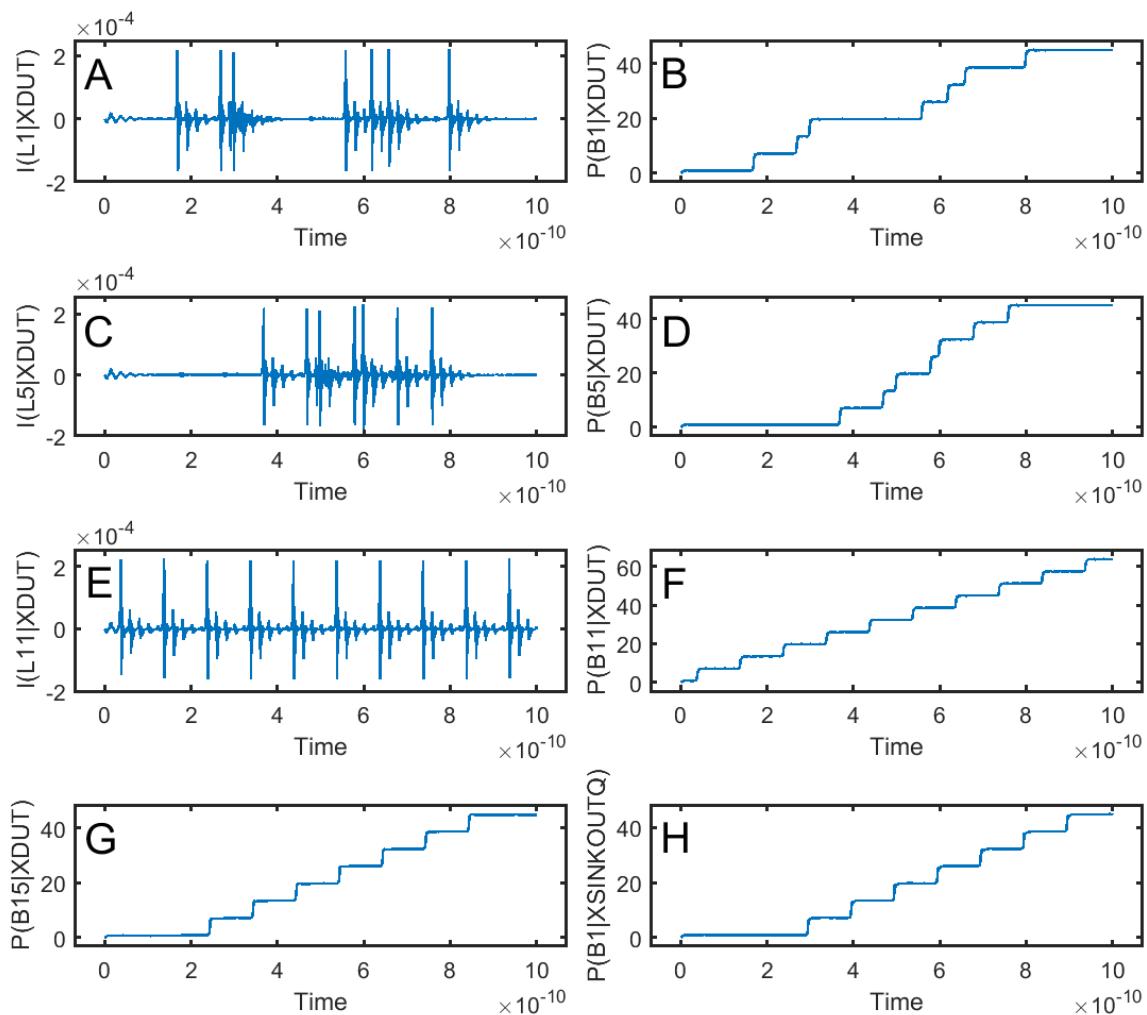


Figure 3.29: RSFQ OR2T analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 18 August 2022
5 // Last Modification by: T. Hall
6 // -----
7 `timescale 1ps/100fs
8 module THmitll_OR2T_v3p0_extracted (a, b, clk, q);
9
10 input
11     a, b, clk;
12
13 output
14     q;
15
16 reg
17     q;
18
19 real
20     delay_state1_clk_q = 6.5,
21     ct_state0_a_clk = 1.6,
22     ct_state0_b_clk = 1.6,
23     ct_state1_a_clk = 3.6,
24     ct_state1_b_clk = 3.7;
25
26 reg
27     errorsignal_a,
28     errorsignal_b,
29     errorsignal_clk;
30
31 integer
32     outfile,
33     cell_state; // internal state of the cell
34
35 initial
36 begin
37     errorsignal_a = 0;
38     errorsignal_b = 0;
39     errorsignal_clk = 0;
40     cell_state = 0; // Startup state
41     q = 0; // All outputs start at 0
42 end
43
44 always @(posedge a or negedge a) // execute at positive and negative edges of input
45 begin
46     if ($time>4) // arbitrary steady-state time)
47         begin
48             if (errorsignal_a == 1'b1) // A critical timing is active for this input
49                 begin
50                     outfile = $fopen("errors.txt", "a");
51                     $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
52                                     ↪ ", $stime);
53                     $fclose(outfile);
54                     q <= 1'bX; // Set all outputs to unknown
55                 end
56             if (errorsignal_a == 0)
57                 begin
58                     case (cell_state)
59                         0: begin
60                             cell_state = 1; // Blocking statement -- immediately
61                             errorsignal_clk = 1; // Critical timing on this input; assign
62                                     ↪ immediately
63                             errorsignal_clk <= #(ct_state0_a_clk) 0; // Clear error signal
64                                     ↪ after critical timing expires
65                         end
66                     1: begin
67                         errorsignal_clk = 1; // Critical timing on this input; assign

```

```

65           ↪ immediately
66           errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
67           ↪ after critical timing expires
68       end
69   endcase
70 end
71
72 always @ (posedge b or negedge b) // execute at positive and negative edges of input
73 begin
74     if ($time>4) // arbitrary steady-state time)
75     begin
76         if (errorsignal_b == 1'b1) // A critical timing is active for this input
77         begin
78             outfile = $fopen("errors.txt", "a");
79             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
80             ↪ ", $stime);
81             $fclose(outfile);
82             q <= 1'bX; // Set all outputs to unknown
83         end
84         if (errorsignal_b == 0)
85         begin
86             case (cell_state)
87                 0: begin
88                     cell_state = 1; // Blocking statement -- immediately
89                     errorsignal_clk = 1; // Critical timing on this input; assign
90                     ↪ immediately
91                     errorsignal_clk <= #(ct_state0_b_clk) 0; // Clear error signal
92                     ↪ after critical timing expires
93                 end
94             endcase
95         end
96     end
97 end
98
99
100 always @ (posedge clk or negedge clk) // execute at positive and negative edges of input
101 begin
102     if ($time>4) // arbitrary steady-state time)
103     begin
104         if (errorsignal_clk == 1'b1) // A critical timing is active for this input
105         begin
106             outfile = $fopen("errors.txt", "a");
107             $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
108             ↪ ", $stime);
109             $fclose(outfile);
110             q <= 1'bX; // Set all outputs to unknown
111         end
112         if (errorsignal_clk == 0)
113         begin
114             case (cell_state)
115                 0: begin
116                     end
117                 1: begin
118                     q <= #(delay_state1_clk_q) !q;
119                     cell_state = 0; // Blocking statement -- immediately
120                 end
121             endcase
122         end
123     end
124 endmodule

```

Listing 3.18: RSFQ OR2T verilog model.

The digital simulation results for the RSFQ OR2T is shown in Fig. 3.30 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.31.

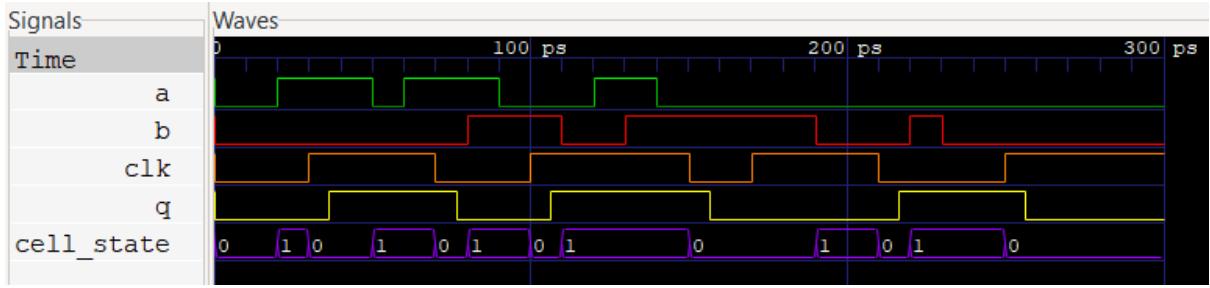


Figure 3.30: RSFQ OR2T digital simulation results.

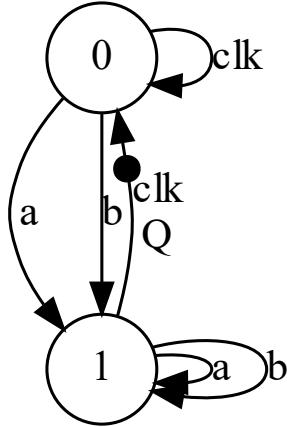


Figure 3.31: RSFQ OR2T Mealy finite state machine diagram.

Power Consumption

Table 3.14: RSFQ OR2T power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	3480	5.05
2	3480	10.1
5	3480	25.2
10	3480	50.5
20	3480	101
50	3480	252

3.2.3 XORT

The RSFQ XORT cell generates an output pulse exclusively if a pulse from a single input line was received before the clock signal. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

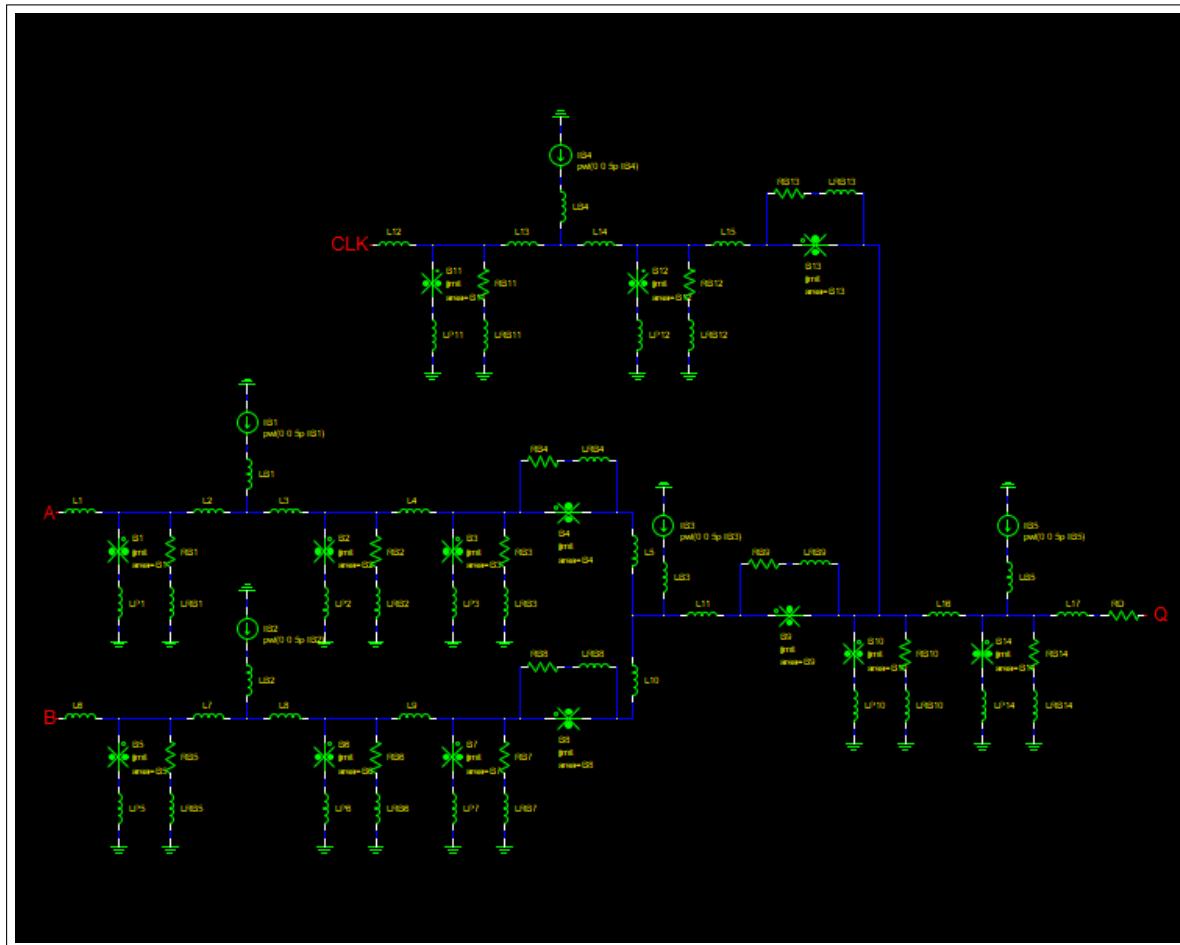


Figure 3.32: Schematic of RSFQ XORT.

Layout

The physical layout of the RSFQ XORT is shown in Fig. 3.33. The layout height is $70 \mu\text{m}$ and the width is $50 \mu\text{m}$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

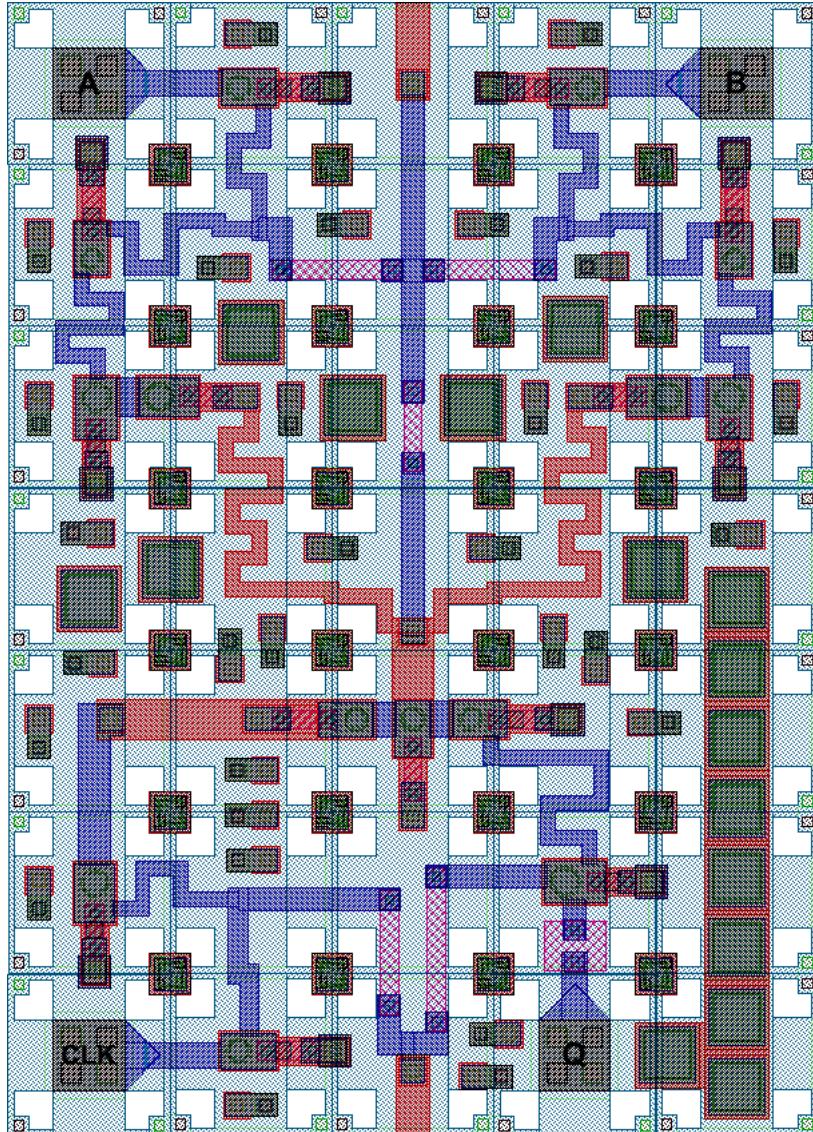


Figure 3.33: RSFQ XORT Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param L1=Lpt1
2  *   ↪ by InductEx v.6.1.52 on 2022/09/06.    65  .param L2=2.7271p
3  * Author: L. Schindler                      66  .param L3=3.7490p
4  * Version: 3.0                                67  .param L4=3.4856p
5  * Last modification date: 6 September 2022   68  .param L5=11.3746p
6  * Last modification by: T. Hall              69  .param L6=Lpt1
7  *$ports      a      b      clk      q      70  .param L7=2.7271p
8  .subckt THmitll_XORT a b clk q            71  .param L8=3.7490p
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param L9=3.4856p
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param L10=11.3746p
   ↪ )                                         74  .param L11=1.0849p
10 .param Phi0=2.067833848E-15                75  .param L12=Lpt1
11 .param B0=1                                 76  .param L13=1.8920p
12 .param Ic0=0.0001                           77  .param L14=2.9216p
13 .param IcRs=100u*6.859904418               78  .param L15=4.4126p
14 .param B0Rs=IcRs/Ic0*B0                   79  .param L16=5.1623p
15 .param Rsheet=2                            80  .param L17=Lpt1
16 .param Lsheet=1.13e-12                     81
17 .param LP=0.5p                             82  .param RB1=B0Rs/B1
18 .param IC=2.5                             83  .param RB2=B0Rs/B2
19 .param ICreceive=1.6                      84  .param RB3=B0Rs/B3
20 .param ICtrans=2.5                        85  .param RB4=B0Rs/B4
21 .param LB=2p                               86  .param RB5=B0Rs/B5
22 .param BiasCoef=0.7                      87  .param RB6=B0Rs/B6
23 .param Lpt1=2p                            88  .param RB7=B0Rs/B7
24 .param RD=1.36                           89  .param RB8=B0Rs/B8
25                                     90  .param RB9=B0Rs/B9
26 .param B1=1.6                            91  .param RB10=B0Rs/B10
27 .param B2=1.25                           92  .param RB11=B0Rs/B11
28 .param B3=2.45                           93  .param RB12=B0Rs/B12
29 .param B4=2.22                           94  .param RB13=B0Rs/B13
30 .param B5=1.6                            95  .param RB14=B0Rs/B14
31 .param B6=1.25                           96
32 .param B7=2.45                           97  .param LRB1=(RB1/Rsheet)*Lsheet+LP
33 .param B8=2.22                           98  .param LRB2=(RB2/Rsheet)*Lsheet+LP
34 .param B9=1.56                           99  .param LRB3=(RB3/Rsheet)*Lsheet+LP
35 .param B10=1.52                          100 .param LRB4=(RB4/Rsheet)*Lsheet+LP
36 .param B11=1.6                           101 .param LRB5=(RB5/Rsheet)*Lsheet+LP
37 .param B12=2.16                           102 .param LRB6=(RB6/Rsheet)*Lsheet+LP
38 .param B13=1.47                           103 .param LRB7=(RB7/Rsheet)*Lsheet+LP
39 .param B14=2.5                           104 .param LRB8=(RB8/Rsheet)*Lsheet
40                                     105 .param LRB9=(RB9/Rsheet)*Lsheet
41 .param IB1=230u                           106 .param LRB10=(RB10/Rsheet)*Lsheet+LP
42 .param IB2=230u                           107 .param LRB11=(RB11/Rsheet)*Lsheet+LP
43 .param IB3=373u                           108 .param LRB12=(RB12/Rsheet)*Lsheet+LP
44 .param IB4=245u                           109 .param LRB13=(RB13/Rsheet)*Lsheet
45 .param IB5=175u                           110 .param LRB14=(RB14/Rsheet)*Lsheet+LP
46                                     111
47 .param LB1=LB                            112 B1 1 2 jjmit area=B1
48 .param LB2=LB                            113 B2 5 6 jjmit area=B2
49 .param LB3=LB                            114 B3 7 8 jjmit area=B3
50 .param LB4=LB                            115 B4 7 9 jjmit area=B4
51 .param LB5=LB                            116 B5 11 12 jjmit area=B5
52                                     117 B6 15 16 jjmit area=B6
53 .param LP1=LP                            118 B7 17 18 jjmit area=B7
54 .param LP2=LP                            119 B8 17 19 jjmit area=B8
55 .param LP3=LP                            120 B9 21 22 jjmit area=B9
56 .param LP5=LP                            121 B10 22 23 jjmit area=B10
57 .param LP6=LP                            122 B11 24 25 jjmit area=B11
58 .param LP7=LP                            123 B12 28 29 jjmit area=B12
59 .param LP10=LP                           124 B13 30 22 jjmit area=B13
60 .param LP11=LP                           125 B14 31 32 jjmit area=B14
61 .param LP12=LP                           126
62 .param LP14=LP                           127 IB1 0 4 pwl(0 0 5p IB1)
63                                     128 IB2 0 14 pwl(0 0 5p IB2)
                                         129 IB3 0 20 pwl(0 0 5p IB3)

```

```

130 | IB4 0 27 pw1(0 0 5p IB4)
131 | IB5 0 33 pw1(0 0 5p IB5)
132 |
133 | LB1 4 3 8.211E-013
134 | LB2 14 13 8.097E-013
135 | LB3 20 10 2.305E-012
136 | LB4 27 26 2.017E-012
137 | LB5 33 31 1.71E-012
138 |
139 | L1 a 1 1.358E-012
140 | L2 1 3 2.704E-012
141 | L3 3 5 3.77E-012
142 | L4 5 7 3.482E-012
143 | L5 9 10 1.13E-011
144 | L6 b 11 1.36E-012
145 | L7 11 13 2.741E-012
146 | L8 13 15 3.753E-012
147 | L9 15 17 3.499E-012
148 | L10 10 19 1.147E-011
149 | L11 10 21 1.081E-012
150 | L12 clk 24 1.322E-012
151 | L13 24 26 1.894E-012
152 | L14 26 28 2.925E-012
153 | L15 28 30 4.408E-012
154 | L16 22 31 5.166E-012
155 | L17 31 34 5.652E-013
156 |
157 | RD 34 q RD
158 |
159 | LP1 2 0 3.691E-013
160 | LP2 6 0 4.306E-013
161 | LP3 8 0 4.459E-013
162 | LP5 12 0 3.668E-013
163 | LP6 16 0 4.344E-013
164 | LP7 18 0 4.281E-013
165 | LP10 23 0 4.896E-013
166 | LP11 25 0 4.012E-013
167 | LP12 29 0 4.248E-013
168 | LP14 32 0 3.342E-013
169 |
170 | RB1 1 101 RB1
171 | LRB1 101 0 LRB1
172 | RB2 5 105 RB2
173 | LRB2 105 0 LRB2
174 | RB3 7 107 RB3
175 | LRB3 107 0 LRB3
176 | RB4 7 109 RB4
177 | LRB4 109 9 LRB4
178 | RB5 11 111 RB5
179 | LRB5 111 0 LRB5
180 | RB6 15 115 RB6
181 | LRB6 115 0 LRB6
182 | RB7 17 117 RB7
183 | LRB7 117 0 LRB7
184 | RB8 17 119 RB8
185 | LRB8 119 19 LRB8
186 | RB9 21 121 RB9
187 | LRB9 121 22 LRB9
188 | RB10 22 122 RB10
189 | LRB10 122 0 LRB10
190 | RB11 24 124 RB11
191 | LRB11 124 0 LRB11
192 | RB12 28 128 RB12
193 | LRB12 128 0 LRB12
194 | RB13 30 130 RB13
195 | LRB13 130 22 LRB13
196 | RB14 31 131 RB14
197 | LRB14 131 0 LRB14
198 |
199 | .ends

```

Listing 3.19: RSFQ XORT JoSIM netlist.**Table 3.15:** RSFQ XORT pin list.

Pin	Description
a	Data input
b	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ XORT using JoSIM is shown in Fig. 3.34. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b**,
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

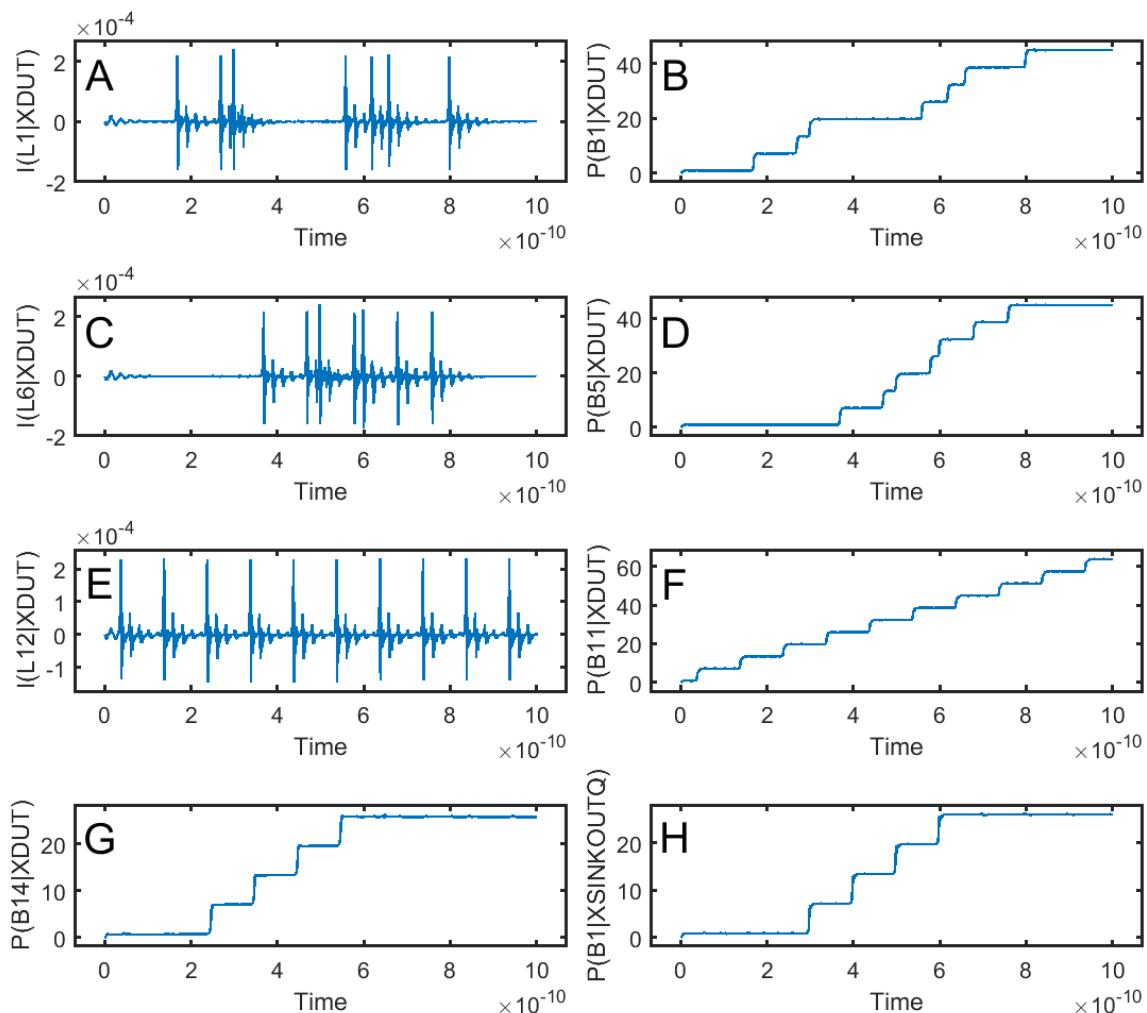


Figure 3.34: RSFQ XORT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 6 September 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_XORT_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 8.8,
21   delay_state2_clk_q = 8.8,
22   ct_state0_clk_a = 3.2,
23   ct_state0_clk_b = 3.1,
24   ct_state1_a_b = 9.5,
25   ct_state1_a_clk = 6.6,
26   ct_state1_b_b = 5.2,
27   ct_state1_clk_b = 7.8,
28   ct_state2_a_a = 5.2,
29   ct_state2_b_a = 9.5,
30   ct_state2_b_clk = 6.7,
31   ct_state2_clk_a = 7.6;
32
33 reg
34   errorsignal_a,
35   errorsignal_b,
36   errorsignal_clk;
37
38 integer
39   outfile,
40   cell_state; // internal state of the cell
41
42 initial
43 begin
44   errorsignal_a = 0;
45   errorsignal_b = 0;
46   errorsignal_clk = 0;
47   cell_state = 0; // Startup state
48   q = 0; // All outputs start at 0
49 end
50
51 always @ (posedge a or negedge a) // execute at positive and negative edges of input
52 begin
53   if ($time > 4) // arbitrary steady-state time)
54     begin
55       if (errorsignal_a == 1'b1) // A critical timing is active for this input
56         begin
57           outfile = $fopen("errors.txt", "a");
58           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
59             ↪ ", $stime);
60           $fclose(outfile);
61           q <= 1'bX; // Set all outputs to unknown
62         end
63       if (errorsignal_a == 0)
64         begin
65           case (cell_state)
66             0: begin
67               cell_state = 1; // Blocking statement -- immediately

```

```

67          end
68      1: begin
69          errorsignal_b = 1; // Critical timing on this input; assign
70          // immediately
71          errorsignal_b <= #(ct_state1_a_b) 0; // Clear error signal
72          // after critical timing expires
73          errorsignal_clk = 1; // Critical timing on this input; assign
74          // immediately
75          errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
76          // after critical timing expires
77      end
78  2: begin
79      cell_state = 0; // Blocking statement -- immediately
80      errorsignal_a = 1; // Critical timing on this input; assign
81      // immediately
82      errorsignal_a <= #(ct_state2_a_a) 0; // Clear error signal
83      // after critical timing expires
84      end
85  endcase
86 end
87
88 always @(posedge b or negedge b) // execute at positive and negative edges of input
89 begin
90     if ($time>4) // arbitrary steady-state time)
91         begin
92             if (errorsignal_b == 1'b1) // A critical timing is active for this input
93                 begin
94                     outfile = $fopen("errors.txt", "a");
95                     $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
96                     // ", $stime);
97                     $fclose(outfile);
98                     q <= 1'bX; // Set all outputs to unknown
99                 end
100            if (errorsignal_b == 0)
101                begin
102                    case (cell_state)
103                        0: begin
104                            cell_state = 2; // Blocking statement -- immediately
105                        end
106                        1: begin
107                            cell_state = 0; // Blocking statement -- immediately
108                            errorsignal_b = 1; // Critical timing on this input; assign
109                            // immediately
110                            errorsignal_b <= #(ct_state1_b_b) 0; // Clear error signal
111                            // after critical timing expires
112                        end
113                    endcase
114                end
115            end
116        begin
117            errorsignal_a = 1; // Critical timing on this input; assign
118            // immediately
119            errorsignal_a <= #(ct_state2_b_a) 0; // Clear error signal
120            // after critical timing expires
121            errorsignal_clk = 1; // Critical timing on this input; assign
122            // immediately
123            errorsignal_clk <= #(ct_state2_b_clk) 0; // Clear error signal
124            // after critical timing expires
125        end
126    endcase
127 end
128
129 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
130 begin
131     if ($time>4) // arbitrary steady-state time)
132         begin
133             if (errorsignal_clk == 1'b1) // A critical timing is active for this input
134                 begin
135                     outfile = $fopen("errors.txt", "a");

```

```

124         $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
125             ↪ ", $stime);
126         $fclose(outfile);
127         q <= 1'bX; // Set all outputs to unknown
128     end
129     if (errorsignal_clk == 0)
130     begin
131         case (cell_state)
132             0: begin
133                 errorsignal_a = 1; // Critical timing on this input; assign
134                     ↪ immediately
135                 errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
136                     ↪ after critical timing expires
137                 errorsignal_b = 1; // Critical timing on this input; assign
138                     ↪ immediately
139                 errorsignal_b <= #(ct_state0_clk_b) 0; // Clear error signal
140                     ↪ after critical timing expires
141             end
142             1: begin
143                 q <= #(delay_state1_clk_q) !q;
144                 cell_state = 0; // Blocking statement -- immediately
145                 errorsignal_b = 1; // Critical timing on this input; assign
146                     ↪ immediately
147                 errorsignal_b <= #(ct_state1_clk_b) 0; // Clear error signal
148                     ↪ after critical timing expires
149             end
150         endcase
151     end
152 end
153
154 endmodule

```

Listing 3.20: RSFQ XORT verilog model.

The digital simulation results for the RSFQ XORT is shown in Fig. 3.35 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.36.

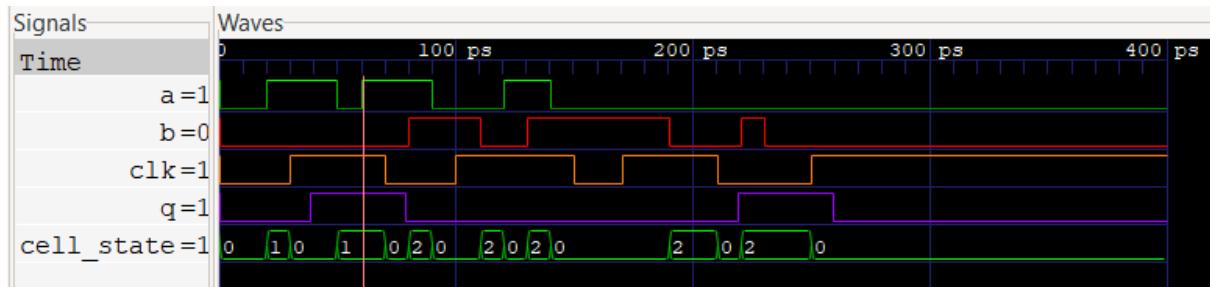


Figure 3.35: RSFQ XORT digital simulation results.

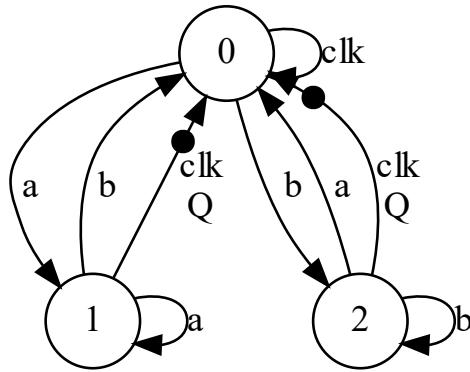


Figure 3.36: RSFQ XORT Mealy finite state machine diagram.

Power Consumption

Table 3.16: RSFQ XORT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	3260	5.35
2	3260	10.7
5	3260	26.7
10	3260	53.5
20	3260	107
50	3260	267

3.2.4 NOTT

The RSFQ NOTT cell is a signal inverting cell driven by a clock pulse signal line. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

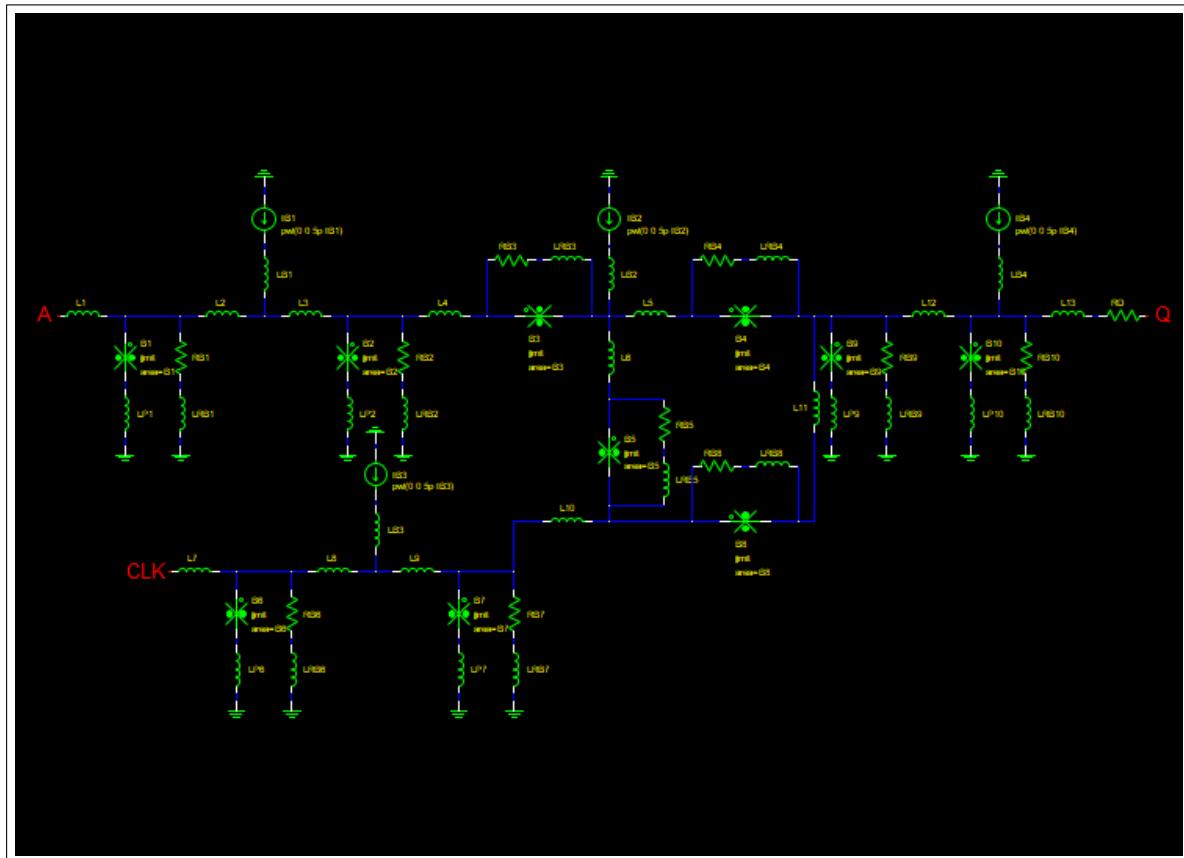


Figure 3.37: Schematic of RSFQ NOTT.

Layout

The physical layout of the RSFQ NOTT is shown in Fig. 3.38. The layout height is $70 \mu m$ and the width is $40 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

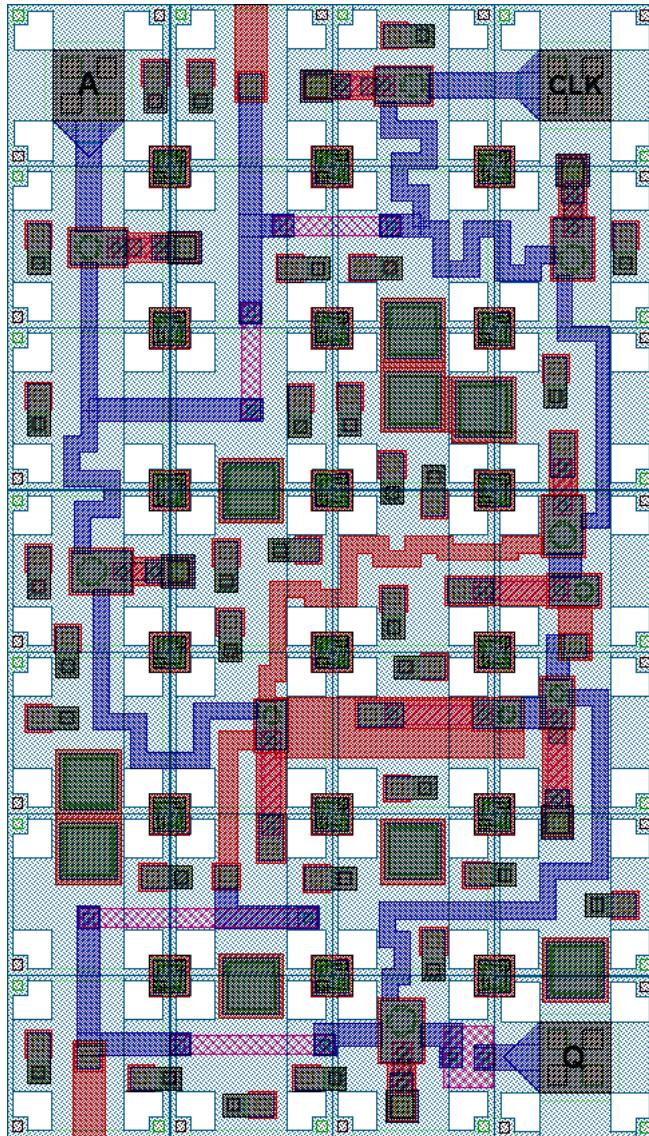


Figure 3.38: RSFQ NOTT Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param LP7=LP
2   ↪ by InductEx v.6.1.52 on 2022/08/25.      65  .param LP9=LP
3  * Author: T. Hall                           66  .param LP10=LP
4  * Version: 3.0                            67
5  * Last modification date: 24 August 2022    68  .param RB1=B0Rs/B1
6  * Last modification by: T. Hall           69  .param RB2=B0Rs/B2
7  *$Ports      a      clk      q             70  .param RB3=B0Rs/B3
8  .subckt THmitll_NOTT a clk q            71  .param RB4=B0Rs/B4
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param RB5=B0Rs/B5
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73  .param RB6=B0Rs/B6
   ↪ )                                         74  .param RB7=B0Rs/B7
10 .param Phi0=2.067833848E-15              75  .param RB8=B0Rs/B8
11 .param B0=1                               76  .param RB9=B0Rs/B9
12 .param Ic0=0.0001                         77  .param RB10=B0Rs/B10
13 .param IcRs=100u*6.859904418               78
14 .param B0Rs=IcRs/Ic0*B0                   79  .param LRB1=(RB1/Rsheet)*Lsheet+LP
15 .param Rsheet=2                          80  .param LRB2=(RB2/Rsheet)*Lsheet+LP
16 .param Lsheet=1.13e-12                    81  .param LRB3=(RB3/Rsheet)*Lsheet
17 .param LP=0.5p                           82  .param LRB4=(RB4/Rsheet)*Lsheet
18 .param IC=2.5                           83  .param LRB5=(RB5/Rsheet)*Lsheet
19 .param ICreceive=1.6                     84  .param LRB6=(RB6/Rsheet)*Lsheet+LP
20 .param ICtrans=2.5                      85  .param LRB7=(RB7/Rsheet)*Lsheet+LP
21 .param LB=2p                            86  .param LRB8=(RB8/Rsheet)*Lsheet
22 .param BiasCoef=0.7                     87  .param LRB9=(RB9/Rsheet)*Lsheet+LP
23 .param Lptl=2p                          88  .param LRB10=(RB10/Rsheet)*Lsheet+LP
24 .param RD=1.36                         89
25
26 .param B1=1.6                           90  B1 1 2 jjmit area=B1
27 .param B2=2.38                         91  B2 5 6 jjmit area=B2
28 .param B3=0.77                         92  B3 7 8 jjmit area=B3
29 .param B4=0.73                         93  B4 10 11 jjmit area=B4
30 .param B5=1.98                         94  B5 12 13 jjmit area=B5
31 .param B6=1.6                           95  B6 14 15 jjmit area=B6
32 .param B7=2.18                         96  B7 18 19 jjmit area=B7
33 .param B8=0.87                         97  B8 13 20 jjmit area=B8
34 .param B9=0.82                         98  B9 11 21 jjmit area=B9
35 .param B10=2.5                        99  B10 22 23 jjmit area=B10
36
37 .param IB1=267u                         100
38 .param IB2=114u                         101  IB1 0 4 pwl(0 0 5p IB1)
39 .param IB3=241u                         102  IB2 0 9 pwl(0 0 5p IB2)
40 .param IB4=175u                         103  IB3 0 17 pwl(0 0 5p IB3)
41
42 .param LB1=LB                           104  IB4 0 24 pwl(0 0 5p IB4)
43 .param LB2=LB                           105
44 .param LB3=LB                           106  LB1 4 3 2.006E-012
45 .param LB4=LB                           107  LB2 9 8 4.261E-012
46
47 .param L1=Lptl                         108  LB3 17 16 4.788E-013
48 .param L2=2.3963p                       109  LB4 24 22 1.011E-012
49 .param L3=2.9984p                       110
50 .param L4=5.5602p                       111  L1 a 1 1.41E-012
51 .param L5=1.8403p                       112  L2 1 3 2.393E-012
52 .param L6=8.5410p                       113  L3 3 5 3E-012
53 .param L7=Lptl                         114  L4 5 7 5.514E-012
54 .param L8=2.8313p                       115  L5 8 10 1.851E-012
55 .param L9=3.4874p                       116  L6 8 12 8.457E-012
56 .param L10=5.2166p                      117  L7 clk 14 1.492E-012
57 .param L11=1.5349p                      118  L8 14 16 2.817E-012
58 .param L12=8.5298p                      119  L9 16 18 3.474E-012
59 .param L13=Lptl                         120  L10 18 13 5.206E-012
60
61 .param LP1=LP                           121  L11 11 20 1.537E-012
62 .param LP2=LP                           122  L12 11 22 8.509E-012
63 .param LP6=LP                           123  L13 22 25 7.694E-013
64
65
66
67
68
69
70
71
72
73
74
75
76
77
78
79
80
81
82
83
84
85
86
87
88
89
90
91
92
93
94
95
96
97
98
99
100
101
102
103
104
105
106
107
108
109
110
111
112
113
114
115
116
117
118
119
120
121
122
123
124
125
126
127
128
129

```

```

130 | LP7 19 0 4.773E-013
131 | LP9 21 0 5.266E-013
132 | LP10 23 0 3.249E-013
133 |
134 | RB1 1 101 RB1
135 | LRB1 101 0 LRB1
136 | RB2 5 105 RB2
137 | LRB2 105 0 LRB2
138 | RB3 7 107 RB3
139 | LRB3 107 8 LRB3
140 | RB4 10 110 RB4
141 | LRB4 110 11 LRB4
142 | RB5 12 112 RB5
143 | LRB5 112 13 LRB5
144 | RB6 14 114 RB6
145 | LRB6 114 0 LRB6
146 | RB7 18 118 RB7
147 | LRB7 118 0 LRB7
148 | RB8 13 113 RB8
149 | LRB8 113 20 LRB8
150 | RB9 11 111 RB9
151 | LRB9 111 0 LRB9
152 | RB10 22 122 RB10
153 | LRB10 122 0 LRB10
154 |
155 | .ends

```

Listing 3.21: RSFQ NOTT JoSIM netlist.**Table 3.17:** RSFQ NOTT pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ NOTT using JoSIM is shown in Fig. 3.39. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **clk**,
- (d) the phase over the input JJ of pin **clk**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

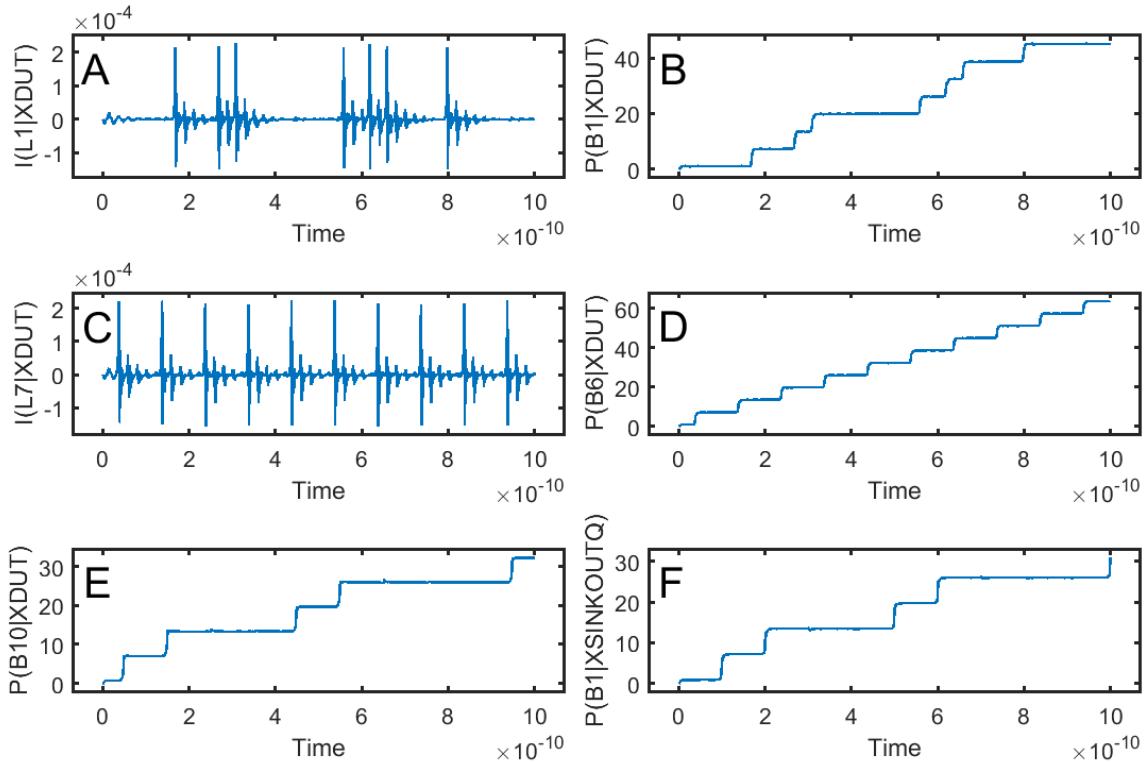


Figure 3.39: RSFQ NOTT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 25 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_NOTT_v3p0_extracted (a, clk, q);
9
10 input
11   a, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_clk_q = 10.5,
21   ct_state0_a_clk = 1.6,
22   ct_state0_clk_a = 6.9,
23   ct_state0_clk_clk = 8.4,
24   ct_state1_a_clk = 0.6;
25
26 reg
27   errorsignal_a,
28   errorsignal_clk;
29
30 integer
31   outfile,
32   cell_state; // internal state of the cell
33
34 initial
35 begin
36   errorsignal_a = 0;
37   errorsignal_clk = 0;
38   cell_state = 0; // Startup state
39   q = 0; // All outputs start at 0
40 end
41
42 always @ (posedge a or negedge a) // execute at positive and negative edges of input
43 begin
44   if ($time > 4) // arbitrary steady-state time)
45     begin
46       if (errorsignal_a == 1'b1) // A critical timing is active for this input
47         begin
48           outfile = $fopen("errors.txt", "a");
49           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
50           ↪ ", $stime);
51           $fclose(outfile);
52           q <= 1'bX; // Set all outputs to unknown
53         end
54       if (errorsignal_a == 0)
55         begin
56           case (cell_state)
57             0: begin
58               cell_state = 1; // Blocking statement -- immediately
59               errorsignal_clk = 1; // Critical timing on this input; assign
59               ↪ immediately
60               errorsignal_clk <= #(ct_state0_a_clk) 0; // Clear error signal
60               ↪ after critical timing expires
61             end
62             1: begin
63               errorsignal_clk = 1; // Critical timing on this input; assign
63               ↪ immediately
64               errorsignal_clk <= #(ct_state1_a_clk) 0; // Clear error signal
64             end
65           endcase
66         end
67       end
68     end
69   end
70 endmodule

```

```

64           end
65       endcase
66   end
67 end
68
69
70 always @ (posedge clk or negedge clk) // execute at positive and negative edges of input
71 begin
72   if ($time > 4) // arbitrary steady-state time)
73     begin
74       if (errorsignal_clk == 1'b1) // A critical timing is active for this input
75         begin
76           outfile = $fopen("errors.txt", "a");
77           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
78           ↪ ", $stime);
79           $fclose(outfile);
80           q <= 1'bX; // Set all outputs to unknown
81         end
82       if (errorsignal_clk == 0)
83         begin
84           case (cell_state)
85             0: begin
86               q <= #(delay_state0_clk_q) !q;
87               errorsignal_a = 1; // Critical timing on this input; assign
88               ↪ immediately
89               errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
90               ↪ after critical timing expires
91               errorsignal_clk = 1; // Critical timing on this input; assign
92               ↪ immediately
93               errorsignal_clk <= #(ct_state0_clk_clk) 0; // Clear error
94               ↪ signal after critical timing expires
95             end
96           1: begin
97             cell_state = 0; // Blocking statement -- immediately
98           end
99         endcase
100      end
101    end
102  endmodule

```

Listing 3.22: RSFQ NOTT verilog model.

The digital simulation results for the RSFQ NOTT is shown in Fig. 3.40 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.41.

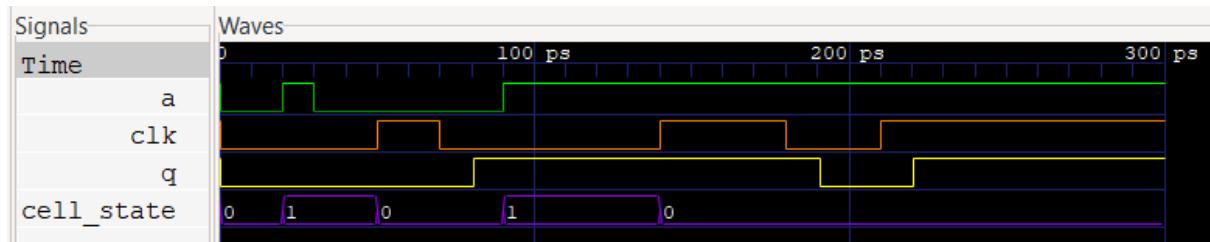


Figure 3.40: RSFQ NOTT digital simulation results.

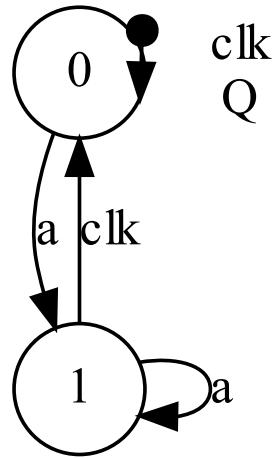


Figure 3.41: RSFQ NOTT Mealy finite state machine diagram.

Power Consumption

Table 3.18: RSFQ NOTT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2070	3.19
2	2070	6.38
5	2070	16.0
10	2070	31.9
20	2070	63.8
50	2070	160

3.3 Buffers

3.3.1 DFFT

The RSFQ DFFT, D flip-flop, is a multi-state device used to transmit an input set pulse synchronised with a reset (typically clock) signal. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

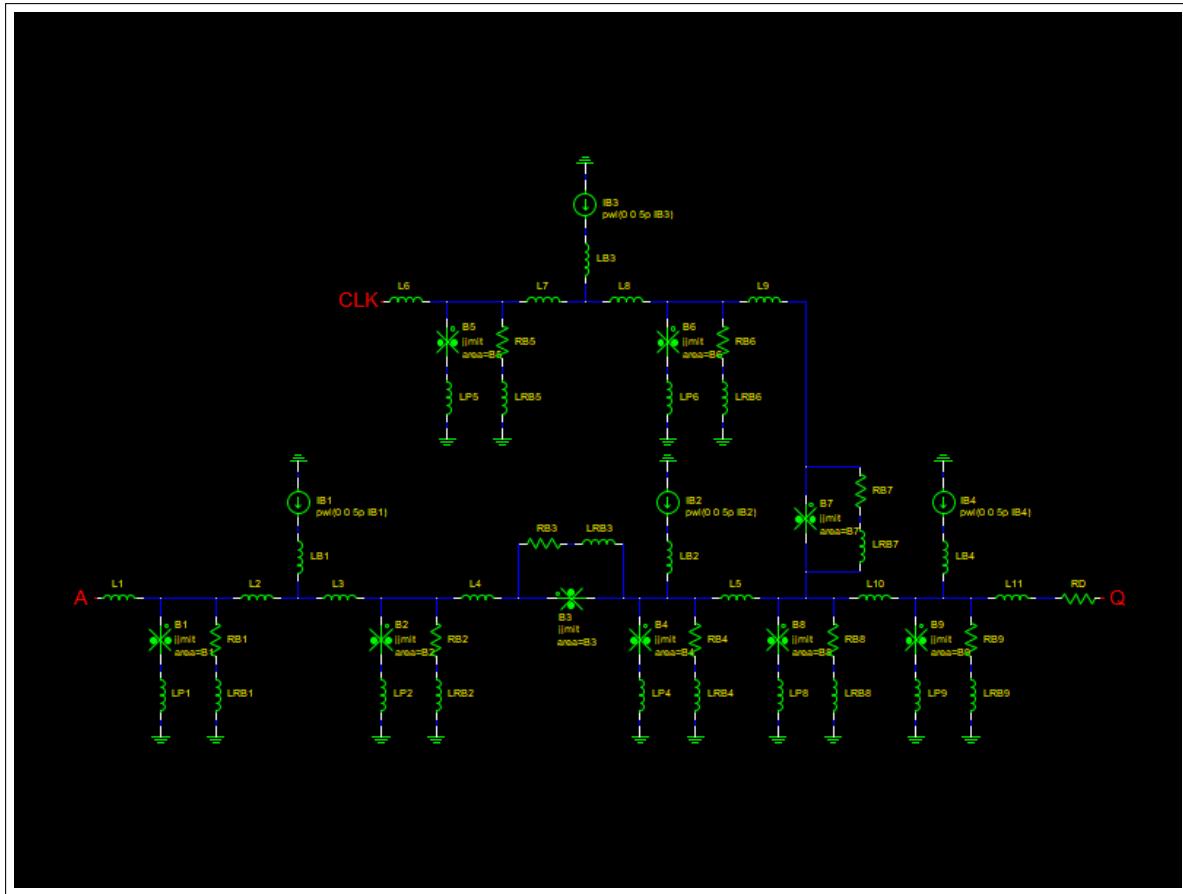


Figure 3.42: Schematic of RSFQ DFFT.

Layout

The physical layout of the RSFQ DFFT is shown in Fig. 3.43. The layout height is $70 \mu m$ and the width is $30 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

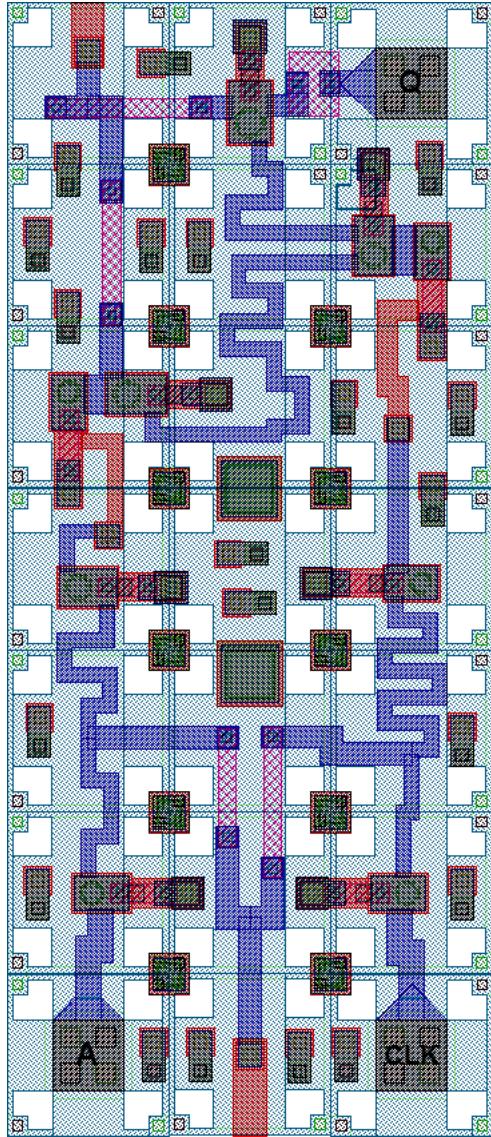


Figure 3.43: RSFQ DFFT Layout.

Analog model

```

1  * Back-annotated simulation file written      64  .param LP9=LP
2   * by InductEx v.6.1.52 on 2022/08/17.       65  .param RB1=B0Rs/B1
3  * Author: L. Schindler                      66  .param RB2=B0Rs/B2
4  * Version: 3.0                                67  .param RB3=B0Rs/B3
5  * Last modification date: 16 August 2022     68  .param RB4=B0Rs/B4
6  * Last modification by: T. Hall              69  .param RB5=B0Rs/B5
7  *$Ports      a      clk      q               70  .param RB6=B0Rs/B6
8  .subckt THmitll_DFFT a clk q                71  .param RB7=B0Rs/B7
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    72  .param RB8=B0Rs/B8
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     73  .param RB9=B0Rs/B9
   ↪ )                                         74
10 .param Phi0=2.067833848E-15                  75
11 .param B0=1                                    76  .param LRB1=(RB1/Rsheet)*Lsheet+LP
12 .param Ic0=0.0001                            77  .param LRB2=(RB2/Rsheet)*Lsheet+LP
13 .param IcRs=100u*6.859904418                 78  .param LRB3=(RB3/Rsheet)*Lsheet
14 .param B0Rs=IcRs/Ic0*B0                      79  .param LRB4=(RB4/Rsheet)*Lsheet+LP
15 .param Rsheet=2                               80  .param LRB5=(RB5/Rsheet)*Lsheet+LP
16 .param Lsheet=1.13e-12                         81  .param LRB6=(RB6/Rsheet)*Lsheet+LP
17 .param LP=0.5p                                82  .param LRB7=(RB7/Rsheet)*Lsheet
18 .param IC=2.5                                 83  .param LRB8=(RB8/Rsheet)*Lsheet+LP
19 .param ICreceive=1.6                          84  .param LRB9=(RB9/Rsheet)*Lsheet+LP
20 .param ICtrans=2.5                           85
21 .param LB=2p                                  86  B1 1 2 jjmit area=B1
22 .param BiasCoef=0.7                          87  B2 5 6 jjmit area=B2
23 .param Lptl=2p                               88  B3 7 8 jjmit area=B3
24 .param RD=1.36                               89  B4 8 9 jjmit area=B4
25                                         90  B5 12 13 jjmit area=B5
26 .param B1=1.6                                91  B6 16 17 jjmit area=B6
27 .param B2=1.82                               92  B7 18 11 jjmit area=B7
28 .param B3=1.36                               93  B8 11 19 jjmit area=B8
29 .param B4=2.07                               94  B9 20 21 jjmit area=B9
30 .param B5=1.6                                95
31 .param B6=1.27                               96  IB1 0 4 pwl(0 0 5p IB1)
32 .param B7=1.28                               97  IB2 0 10 pwl(0 0 5p IB2)
33 .param B8=1.89                               98  IB3 0 15 pwl(0 0 5p IB3)
34 .param B9=2.5                                99  IB4 0 22 pwl(0 0 5p IB4)
35                                         100
36 .param IB1=262u                             101  LB1 4 3 1.76E-012
37 .param IB2=206u                             102  LB2 10 8 1.06E-012
38 .param IB3=194u                             103  LB3 15 14 1.853E-012
39 .param IB4=175u                             104  LB4 22 20 6.105E-013
40                                         105
41 .param LB1=LB                               106  L1 a 1 1.401E-012
42 .param LB2=LB                               107  L2 1 3 2.877E-012
43 .param LB3=LB                               108  L3 3 5 3.673E-012
44 .param LB4=LB                               109  L4 5 7 4.739E-012
45                                         110  L5 8 11 9.527E-012
46 .param L1=Lptl                            111  L6 clk 12 1.422E-012
47 .param L2=2.8908p                          112  L7 12 14 2.188E-012
48 .param L3=3.6865p                          113  L8 14 16 5.588E-012
49 .param L4=4.7771p                          114  L9 16 18 5.337E-012
50 .param L5=9.5023p                          115  L10 11 20 4.566E-012
51 .param L6=Lptl                            116  L11 20 23 7.347E-013
52 .param L7=2.2014p                          117  RD 23 q RD
53 .param L8=5.6199p                          118
54 .param L9=5.3129p                          119  LP1 2 0 3.976E-013
55 .param L10=4.5588p                         120  LP2 6 0 4.101E-013
56 .param L11=Lptl                           121  LP4 9 0 4.172E-013
57                                         122  LP5 13 0 3.949E-013
58 .param LP1=LP                             123  LP6 17 0 5.178E-013
59 .param LP2=LP                             124  LP8 19 0 4.435E-013
60 .param LP4=LP                             125  LP9 21 0 3.068E-013
61 .param LP5=LP                             126
62 .param LP6=LP                             127  RB1 1 101 RB1
63 .param LP8=LP                             128  LRB1 101 0 LRB1
64                                         129  RB2 5 105 RB2

```

```

130 | LRB2 105 0 LRB2
131 | RB3 7 107 RB3
132 | LRB3 107 8 LRB3
133 | RB4 8 108 RB4
134 | LRB4 108 0 LRB4
135 | RB5 12 112 RB5
136 | LRB5 112 0 LRB5
137 | RB6 16 116 RB6
138 | LRB6 116 0 LRB6
139 | RB7 18 118 RB7
140 | LRB7 118 11 LRB7
141 | RB8 11 111 RB8
142 | LRB8 111 0 LRB8
143 | RB9 20 120 RB9
144 | LRB9 120 0 LRB9
145
146 .ends

```

Listing 3.23: RSFQ DFFT JoSIM netlist.**Table 3.19:** RSFQ DFFT pin list.

Pin	Description
a	Data input
clk	Clock input
q	Data output

The simulation results for the RSFQ DFFT using JoSIM is shown in Fig. 3.44. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **clk**,
- (d) the phase over the input JJ of pin **clk**,
- (e) the phase over the output JJ of pin **q**, and
- (f) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

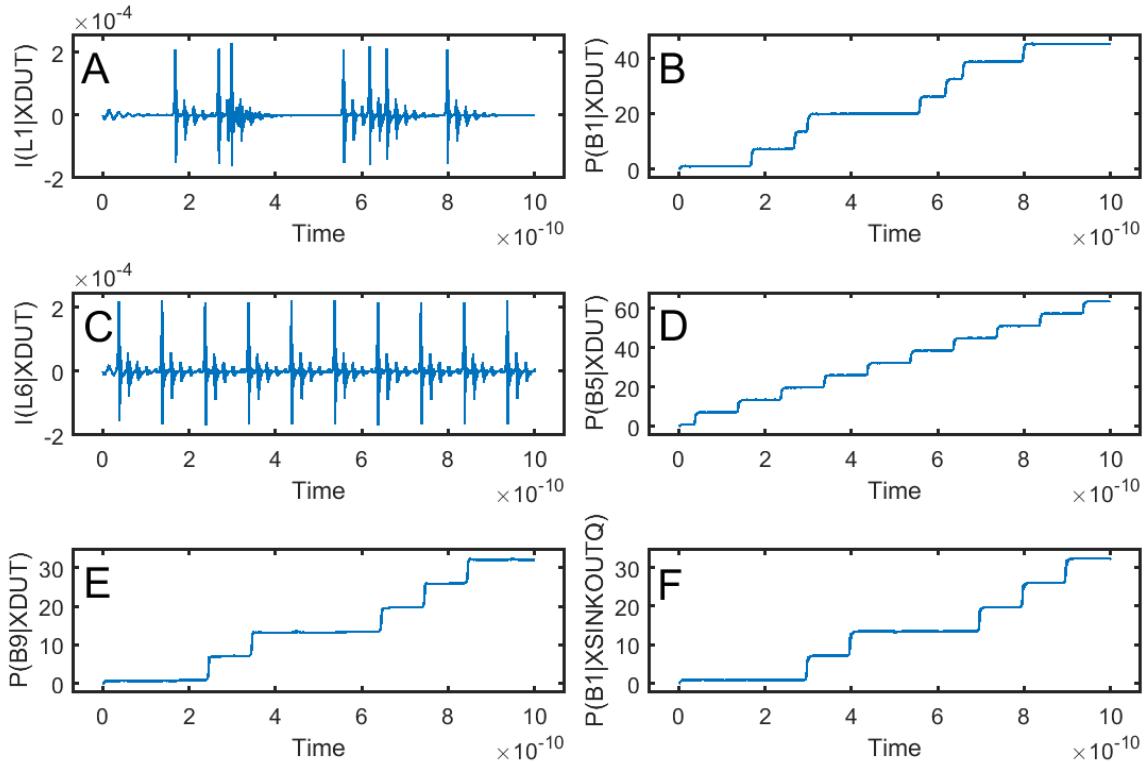


Figure 3.44: RSFQ DFFT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 17 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_DFFT_v3p0_extracted (a, clk, q);
9
10 input
11   a, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 8.0,
21   ct_state0_clk_a = 2.3,
22   ct_state1_clk_a = 0.7;
23
24 reg
25   errorsignal_a,
26   errorsignal_clk;
27
28 integer
29   outfile,
30   cell_state; // internal state of the cell
31
32 initial
33 begin
34   errorsignal_a = 0;
35   errorsignal_clk = 0;
36   cell_state = 0; // Startup state
37   q = 0; // All outputs start at 0
38 end
39
40 always @(posedge a or negedge a) // execute at positive and negative edges of input
41 begin
42   if ($time>4) // arbitrary steady-state time)
43   begin
44     if (errorsignal_a == 1'b1) // A critical timing is active for this input
45     begin
46       outfile = $fopen("errors.txt", "a");
47       $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
48                   " ", $stime);
49       $fclose(outfile);
50       q <= 1'bX; // Set all outputs to unknown
51     end
52     if (errorsignal_a == 0)
53     begin
54       case (cell_state)
55         0: begin
56           cell_state = 1; // Blocking statement -- immediately
57           end
58         1: begin
59           end
60         endcase
61       end
62     end
63   end
64 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
65 begin
66   if ($time>4) // arbitrary steady-state time)

```

```

67      begin
68        if (errorsignal_clk == 1'b1) // A critical timing is active for this input
69          begin
70            outfile = $fopen("errors.txt", "a");
71            $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m; %0d_ps.\n"
72                         ↪ ", $stime);
73            $fclose(outfile);
74            q <= 1'bX; // Set all outputs to unknown
75          end
76        if (errorsignal_clk == 0)
77          begin
78            case (cell_state)
79              0: begin
80                errorsignal_a = 1; // Critical timing on this input; assign
81                                ↪ immediately
82                errorsignal_a <= #(ct_state0_clk_a) 0; // Clear error signal
83                                ↪ after critical timing expires
84              end
85              1: begin
86                q <= #(delay_state1_clk_q) !q;
87                cell_state = 0; // Blocking statement -- immediately
88                errorsignal_a = 1; // Critical timing on this input; assign
89                                ↪ immediately
90                errorsignal_a <= #(ct_state1_clk_a) 0; // Clear error signal
91                                ↪ after critical timing expires
92              end
93            endcase
94          end
95      end
96    endmodule

```

Listing 3.24: RSFQ DFFT verilog model.

The digital simulation results for the RSFQ DFFT is shown in Fig. 3.45 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 3.46.

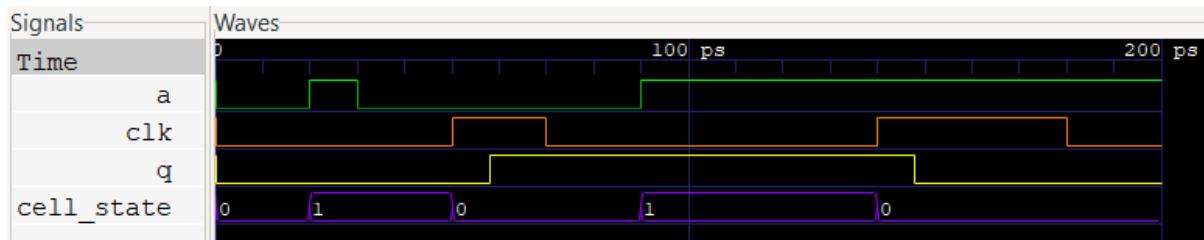


Figure 3.45: RSFQ DFFT digital simulation results.

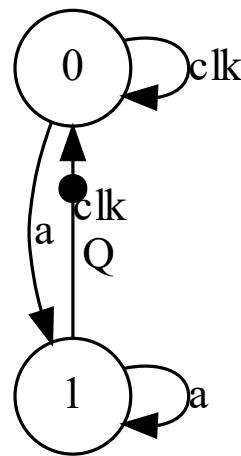


Figure 3.46: RSFQ DFFT Mealy finite state machine diagram.

Power Consumption

Table 3.20: RSFQ DFFT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	2180	3.18
2	2180	6.36
5	2180	15.9
10	2180	31.8
20	2180	63.6
50	2180	159

3.3.2 NDROT

The NDROT, non-destructive readout, cell is a memory device controlled by a set, reset and clock input signal. When an input set signal is received, the NDROT will generate an output pulse after each clock signal until an input reset signal is received. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

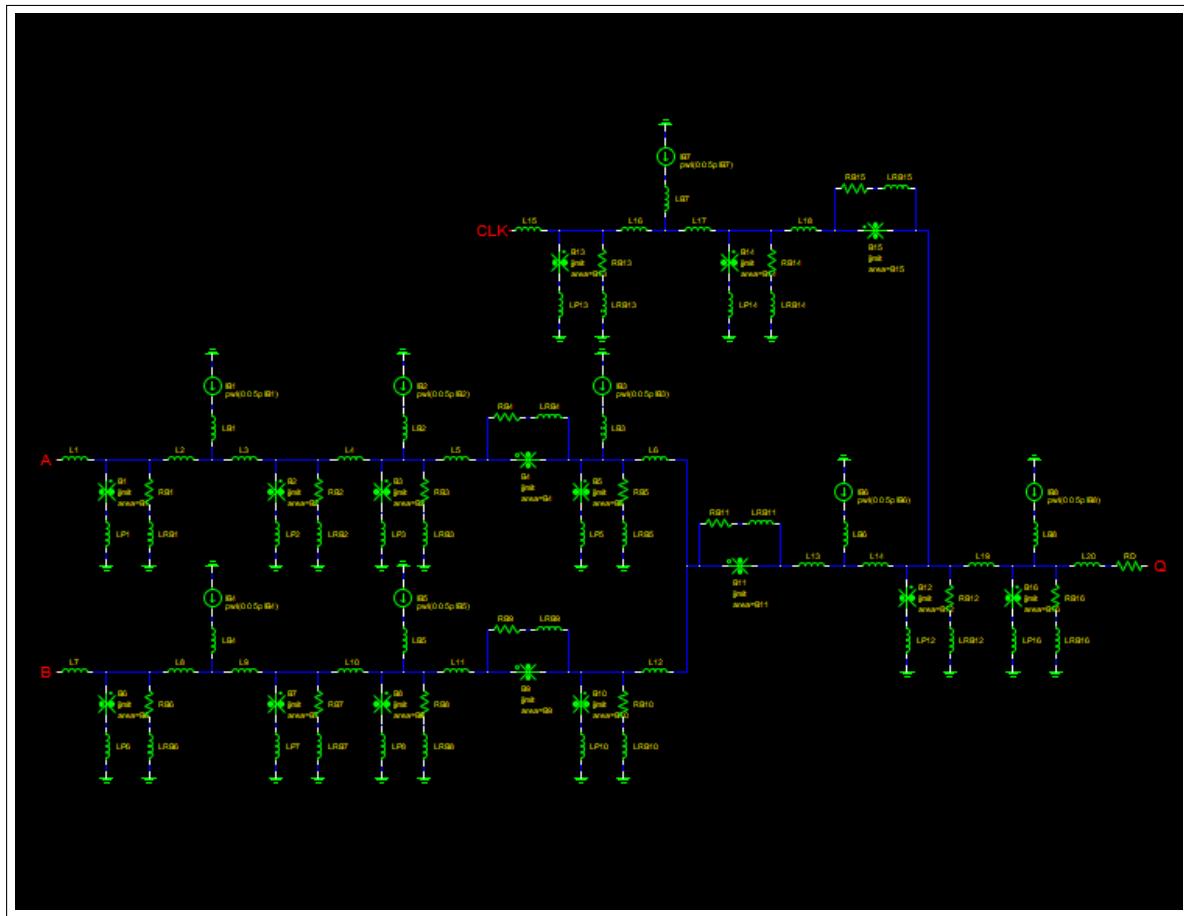


Figure 3.47: Schematic of RSFQ NDROT.

Layout

The physical layout of the RSFQ NDROT is shown in Fig. 3.48. The layout height is $70 \mu m$ and the width is $50 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

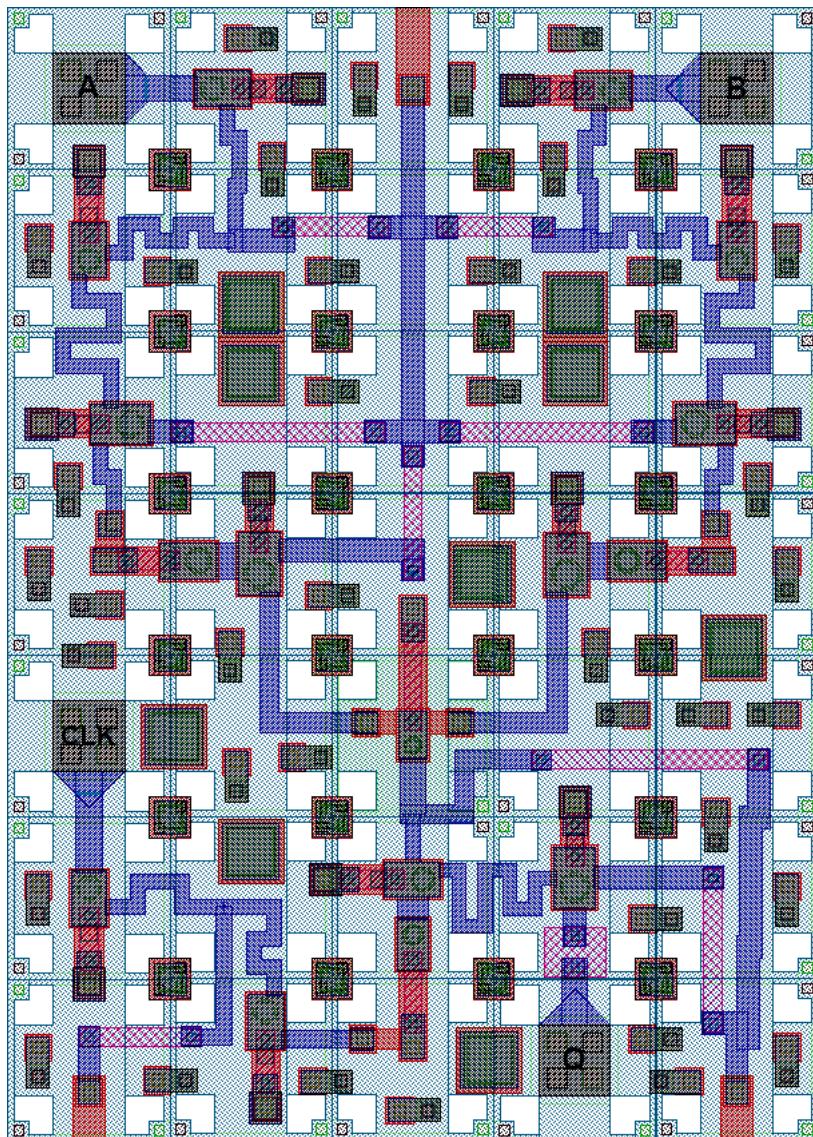


Figure 3.48: RSFQ NDROT Layout.

Analog model

```

1  * Back-annotated simulation file written      63 | .param L3=2.7660p
2  *   ↪ by InductEx v.6.1.52 on 2022/09/01.    64 | .param L4=4.1774p
3  * Author: L. Schindler                      65 | .param L5=3.2486p
4  * Version: 3.0                                66 | .param L6=3.7241p
5  * Last modification date: 30 August 2022     67 | .param L7=Lptl
6  * Last modification by: T. Hall              68 | .param L8=2.3873p
7  *$Ports      a      b      clk      q      69 | .param L9=2.7660p
8  *           ↪          ↪          ↪          ↪      70 | .param L10=4.1774p
9  .subckt THmitll_NDROT a b clk q            71 | .param L11=3.2486p
10 .model jjmit jj(rtype=1, vg=2.8mV, cap    72 | .param L12=3.7241p
11   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    73 | .param L13=0.8049p
12   ↪ )                                         74 | .param L14=0.8860p
13 .param Phi0=2.067833848E-15                 75 | .param L15=Lptl
14 .param B0=1                                 76 | .param L16=2.6122p
15 .param Ic0=0.0001                           77 | .param L17=2.6435p
16 .param IcRs=100u*6.859904418                78 | .param L18=3.5452p
17 .param B0Rs=IcRs/Ic0*B0                     79 | .param L19=4.6837p
18 .param Rsheet=2                            80 | .param L20=Lptl
19 .param LP=0.5p                             81
20 .param IC=2.5                               82 | .param LP1=LP
21 .param LB=2p                                83 | .param LP2=LP
22 .param BiasCoef=0.7                         84 | .param LP3=LP
23 .param Lptl=2p                             85 | .param LP5=LP
24 .param RD=1.36                             86 | .param LP6=LP
25                                     87 | .param LP7=LP
26 .param B1=1.6                               88 | .param LP8=LP
27 .param B2=1.45                             89 | .param LP10=LP
28 .param B3=2.15                             90 | .param LP12=LP
29 .param B4=1.73                             91 | .param LP13=LP
30 .param B5=2.54                             92 | .param LP14=LP
31 .param B6=1.6                               93 | .param LP16=LP
32 .param B7=1.45                             94
33 .param B8=2.15                             95 | .param RB1=B0Rs/B1
34 .param B9=1.73                             96 | .param RB2=B0Rs/B2
35 .param B10=2.54                            97 | .param RB3=B0Rs/B3
36 .param B11=0.74                            98 | .param RB4=B0Rs/B4
37 .param B12=1.57                            99 | .param RB5=B0Rs/B5
38 .param B13=1.6                               100 | .param RB6=B0Rs/B6
39 .param B14=1.6                               101 | .param RB7=B0Rs/B7
40 .param B15=1.08                            102 | .param RB8=B0Rs/B8
41 .param B16=2.5                               103 | .param RB9=B0Rs/B9
42                                     104 | .param RB10=B0Rs/B10
43 .param IB1=268u                            105 | .param RB11=B0Rs/B11
44 .param IB2=129u                            106 | .param RB12=B0Rs/B12
45 .param IB3=225u                            107 | .param RB13=B0Rs/B13
46 .param IB4=268u                            108 | .param RB14=B0Rs/B14
47 .param IB5=129u                            109 | .param RB15=B0Rs/B15
48 .param IB6=115u                            110 | .param RB16=B0Rs/B16
49 .param IB7=254u
50 .param IB8=175u
51
52 .param LB1=LB
53 .param LB2=LB
54 .param LB3=LB
55 .param LB4=LB
56 .param LB5=LB
57 .param LB6=LB
58 .param LB7=LB
59 .param LB8=LB
60
61 .param L1=Lptl
62 .param L2=2.3873p
63 | .param L3=2.7660p
64 | .param L4=4.1774p
65 | .param L5=3.2486p
66 | .param L6=3.7241p
67 | .param L7=Lptl
68 | .param L8=2.3873p
69 | .param L9=2.7660p
70 | .param L10=4.1774p
71 | .param L11=3.2486p
72 | .param L12=3.7241p
73 | .param L13=0.8049p
74 | .param L14=0.8860p
75 | .param L15=Lptl
76 | .param L16=2.6122p
77 | .param L17=2.6435p
78 | .param L18=3.5452p
79 | .param L19=4.6837p
80 | .param L20=Lptl
81
82 | .param LP1=LP
83 | .param LP2=LP
84 | .param LP3=LP
85 | .param LP5=LP
86 | .param LP6=LP
87 | .param LP7=LP
88 | .param LP8=LP
89 | .param LP10=LP
90 | .param LP12=LP
91 | .param LP13=LP
92 | .param LP14=LP
93 | .param LP16=LP
94
95 | .param RB1=B0Rs/B1
96 | .param RB2=B0Rs/B2
97 | .param RB3=B0Rs/B3
98 | .param RB4=B0Rs/B4
99 | .param RB5=B0Rs/B5
100 | .param RB6=B0Rs/B6
101 | .param RB7=B0Rs/B7
102 | .param RB8=B0Rs/B8
103 | .param RB9=B0Rs/B9
104 | .param RB10=B0Rs/B10
105 | .param RB11=B0Rs/B11
106 | .param RB12=B0Rs/B12
107 | .param RB13=B0Rs/B13
108 | .param RB14=B0Rs/B14
109 | .param RB15=B0Rs/B15
110 | .param RB16=B0Rs/B16
111
112 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
113 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
114 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
115 | .param LRB4=(RB4/Rsheet)*Lsheet
116 | .param LRB5=(RB5/Rsheet)*Lsheet+LP
117 | .param LRB6=(RB6/Rsheet)*Lsheet+LP
118 | .param LRB7=(RB7/Rsheet)*Lsheet+LP
119 | .param LRB8=(RB8/Rsheet)*Lsheet+LP
120 | .param LRB9=(RB9/Rsheet)*Lsheet
121 | .param LRB10=(RB10/Rsheet)*Lsheet+LP
122 | .param LRB11=(RB11/Rsheet)*Lsheet
123 | .param LRB12=(RB12/Rsheet)*Lsheet+LP
124 | .param LRB13=(RB13/Rsheet)*Lsheet+LP
125 | .param LRB14=(RB14/Rsheet)*Lsheet+LP
126 | .param LRB15=(RB15/Rsheet)*Lsheet
127 | .param LRB16=(RB16/Rsheet)*Lsheet+LP
128

```

```

129 | B1 1 2 jjmit area=B1          183 | L20 39 42 6.06E-013
130 | B2 5 6 jjmit area=B2          184 |
131 | B3 7 8 jjmit area=B3          185 | RD 42 q RD
132 | B4 10 11 jjmit area=B4         186 |
133 | B5 11 12 jjmit area=B5         187 | LP1 2 0 3.626E-013
134 | B6 15 16 jjmit area=B6         188 | LP2 6 0 4.608E-013
135 | B7 19 20 jjmit area=B7         189 | LP3 8 0 3.732E-013
136 | B8 21 22 jjmit area=B8         190 | LP5 12 0 4.072E-013
137 | B9 24 25 jjmit area=B9         191 | LP6 16 0 3.63E-013
138 | B10 25 26 jjmit area=B10        192 | LP7 20 0 4.592E-013
139 | B11 14 27 jjmit area=B11        193 | LP8 22 0 3.742E-013
140 | B12 30 31 jjmit area=B12        194 | LP10 26 0 3.912E-013
141 | B13 32 33 jjmit area=B13        195 | LP12 31 0 4.701E-013
142 | B14 36 37 jjmit area=B14        196 | LP13 33 0 3.832E-013
143 | B15 38 30 jjmit area=B15        197 | LP14 37 0 4.271E-013
144 | B16 39 40 jjmit area=B16        198 | LP16 40 0 3.764E-013
145 |
146 | IB1 0 4 pwl(0 0 5p IB1)        199 |
147 | IB2 0 9 pwl(0 0 5p IB2)        200 | RB1 1 101 RB1
148 | IB3 0 13 pwl(0 0 5p IB3)       201 | LRB1 101 0 LRB1
149 | IB4 0 18 pwl(0 0 5p IB4)       202 | RB2 5 105 RB2
150 | IB5 0 23 pwl(0 0 5p IB5)       203 | LRB2 105 0 LRB2
151 | IB6 0 29 pwl(0 0 5p IB6)       204 | RB3 7 107 RB3
152 | IB7 0 35 pwl(0 0 5p IB7)       205 | LRB3 107 0 LRB3
153 | IB8 0 41 pwl(0 0 5p IB8)       206 | RB4 10 110 RB4
154 |
155 | LB1 4 3 8.139E-013           207 | LRB4 110 11 LRB4
156 | LB2 9 7 6.905E-013           208 | RB5 11 111 RB5
157 | LB3 13 11 2.05E-012          209 | LRB5 111 0 LRB5
158 | LB4 18 17 7.93E-013          210 | RB6 15 115 RB6
159 | LB5 23 21 6.92E-013          211 | LRB6 115 0 LRB6
160 | LB6 29 28 2.339E-012          212 | RB7 19 119 RB7
161 | LB7 35 34 2.399E-012          213 | LRB7 119 0 LRB7
162 | LB8 41 39 1.726E-012          214 | RB8 21 121 RB8
163 |
164 | L1 a 1 1.001E-012            215 | LRB8 121 0 LRB8
165 | L2 1 3 2.395E-012            216 | RB9 24 124 RB9
166 | L3 3 5 2.766E-012            217 | LRB9 124 25 LRB9
167 | L4 5 7 4.17E-012             218 | RB10 25 125 RB10
168 | L5 7 10 3.25E-012            219 | LRB10 125 0 LRB10
169 | L6 11 14 3.695E-012           220 | RB11 14 127 RB11
170 | L7 b 15 1.003E-012           221 | LRB11 127 27 LRB11
171 | L8 15 17 2.401E-012           222 | RB12 30 130 RB12
172 | L9 17 19 2.779E-012           223 | LRB12 130 0 LRB12
173 | L10 19 21 4.183E-012          224 | RB13 32 132 RB13
174 | L11 21 24 3.255E-012          225 | LRB13 132 0 LRB13
175 | L12 25 14 3.713E-012          226 | RB14 36 136 RB14
176 | L13 27 28 8.093E-013          227 | LRB14 136 0 LRB14
177 | L14 28 30 8.804E-013          228 | RB15 38 138 RB15
178 | L15 clk 32 1.351E-012          229 | LRB15 138 30 LRB15
179 | L16 32 34 2.624E-012          230 | RB16 39 139 RB16
180 | L17 34 36 2.63E-012           231 | LRB16 139 0 LRB16
181 | L18 36 38 3.565E-012           232 |
182 | L19 30 39 4.674E-012           233 | .ends

```

Listing 3.25: RSFQ NDROT JoSIM netlist.**Table 3.21:** RSFQ NDROT pin list.

Pin	Description
a	Data input (set signal)
b	Data input (reset signal)
clk	Clock input
q	Data output

The simulation results for the RSFQ NDROT using JoSIM is shown in Fig. 3.49. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a** (set signal),
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the input inductor connected to pin **b** (reset signal),
- (d) the phase over the input JJ of pin **b**,
- (e) the current through the input inductor connected to pin **clk**,
- (f) the phase over the input JJ of pin **clk**,
- (g) the phase over the output JJ of pin **q**, and
- (h) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

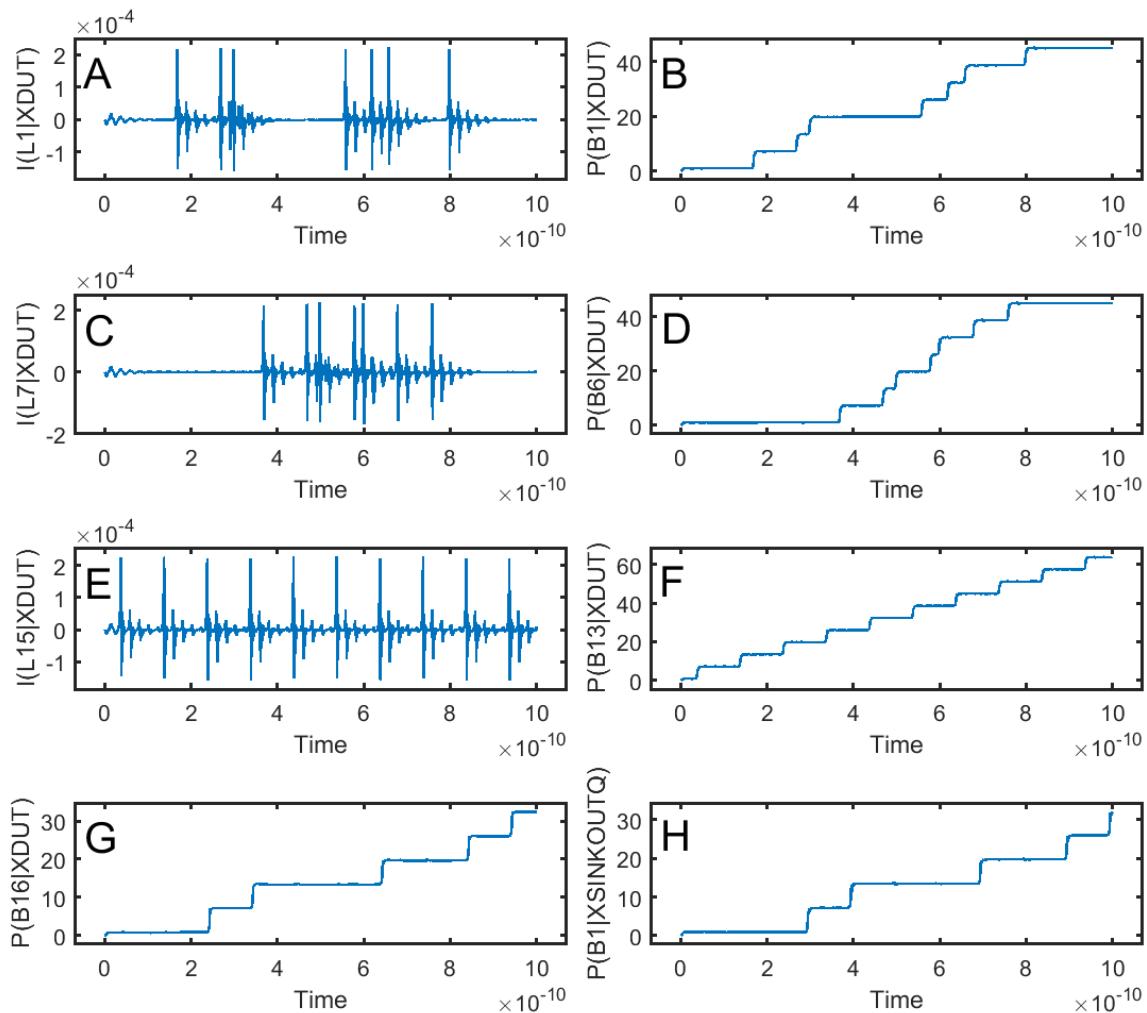


Figure 3.49: RSFQ NDROT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 1 September 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_NDROT_v3p0_extracted (a, b, clk, q);
9
10 input
11   a, b, clk;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state1_clk_q = 5.8,
21   ct_state0_a_b = 0.2,
22   ct_state1_b_a = 0.3,
23   ct_state1_clk_clk = 8.4;
24
25 reg
26   errorsignal_a,
27   errorsignal_b,
28   errorsignal_clk;
29
30 integer
31   outfile,
32   cell_state; // internal state of the cell
33
34 initial
35 begin
36   errorsignal_a = 0;
37   errorsignal_b = 0;
38   errorsignal_clk = 0;
39   cell_state = 0; // Startup state
40   q = 0; // All outputs start at 0
41 end
42
43 always @ (posedge a or negedge a) // execute at positive and negative edges of input
44 begin
45   if ($time > 4) // arbitrary steady-state time)
46     begin
47       if (errorsignal_a == 1'b1) // A critical timing is active for this input
48         begin
49           outfile = $fopen("errors.txt", "a");
50           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
51           ↪ ", $stime);
52           $fclose(outfile);
53           q <= 1'bX; // Set all outputs to unknown
54         end
55       if (errorsignal_a == 0)
56         begin
57           case (cell_state)
58             0: begin
59               cell_state = 1; // Blocking statement -- immediately
60               errorsignal_b = 1; // Critical timing on this input; assign
61               ↪ immediately
62               errorsignal_b <= #(ct_state0_a_b) 0; // Clear error signal
63               ↪ after critical timing expires
64             end
65           1: begin
66             end
67           endcase

```

```

65           end
66       end
67   end
68
69 always @(posedge b or negedge b) // execute at positive and negative edges of input
70   begin
71     if ($time>4) // arbitrary steady-state time)
72     begin
73       if (errorsignal_b == 1'b1) // A critical timing is active for this input
74       begin
75         outfile = $fopen("errors.txt", "a");
76         $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
77                     ↪ ", $stime);
78         $fclose(outfile);
79         q <= 1'bX; // Set all outputs to unknown
80       end
81     if (errorsignal_b == 0)
82     begin
83       case (cell_state)
84         0: begin
85           end
86         1: begin
87           cell_state = 0; // Blocking statement -- immediately
88           errorsignal_a = 1; // Critical timing on this input; assign
89           ↪ immediately
90           errorsignal_a <= #(ct_state1_b_a) 0; // Clear error signal
91           ↪ after critical timing expires
92           end
93         endcase
94       end
95   end
96
97 always @(posedge clk or negedge clk) // execute at positive and negative edges of input
98   begin
99     if ($time>4) // arbitrary steady-state time)
100    begin
101      if (errorsignal_clk == 1'b1) // A critical timing is active for this input
102      begin
103        outfile = $fopen("errors.txt", "a");
104        $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
105                     ↪ ", $stime);
106        $fclose(outfile);
107        q <= 1'bX; // Set all outputs to unknown
108      end
109    if (errorsignal_clk == 0)
110    begin
111      case (cell_state)
112        0: begin
113          end
114        1: begin
115          q <= #(delay_state1_clk_q) !q;
116          errorsignal_clk = 1; // Critical timing on this input; assign
117          ↪ immediately
118          errorsignal_clk <= #(ct_state1_clk_clk) 0; // Clear error
119          ↪ signal after critical timing expires
120          end
121        endcase
122      end
123    end
124  end
125 endmodule

```

Listing 3.26: RSFQ NDROT verilog model.

The digital simulation results for the RSFQ NDROT is shown in Fig. 3.50 and the Mealy finite state diagram, extracted using *TimEx*, is shown in Fig. 3.51.

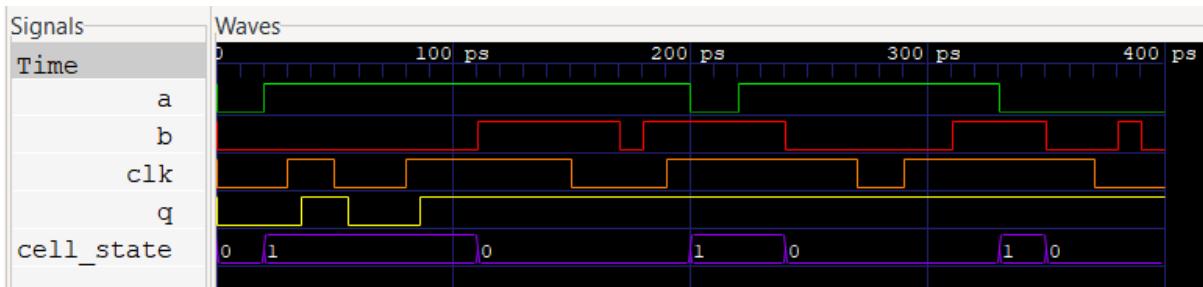


Figure 3.50: RSFQ NDROT digital simulation results.

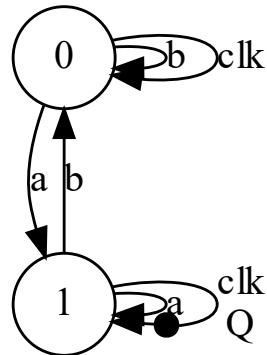


Figure 3.51: RSFQ NDROT Mealy finite state machine diagram.

Power Consumption

Table 3.22: RSFQ NDROT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	4060	5.80
2	4060	11.6
5	4060	29.0
10	4060	58.0
20	4060	116
50	4060	290

3.3.3 BUFFT

The RSFQ BUFFT cell is a buffer cell intended for clock balancing. It is designed to have the same a-to-q delay as the SPLITT cell. The cell has integrated PTL transmitters and receivers and is designed to connect directly to a PTL.

Schematic

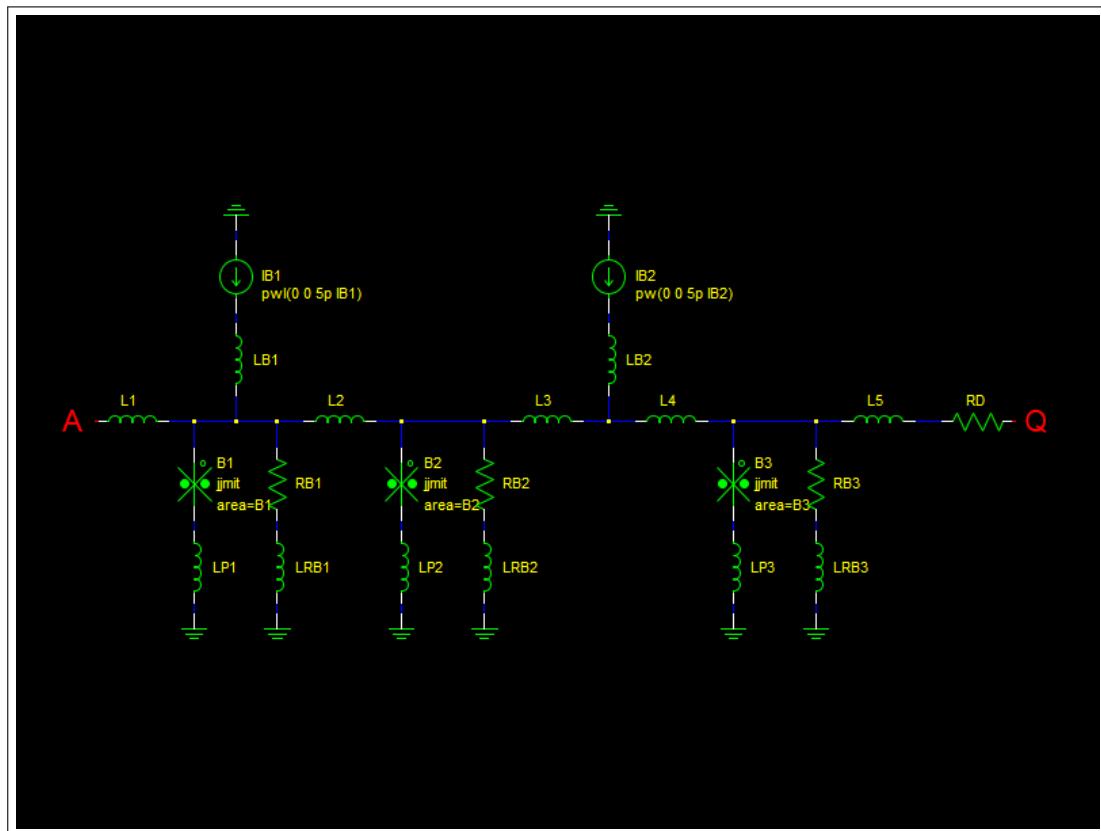


Figure 3.52: Schematic of RSFQ BUFFT.

Layout

The physical layout for the RSFQ BUFFT is shown in Fig. 3.53. The layout height is $70 \mu m$ and the width is $20 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

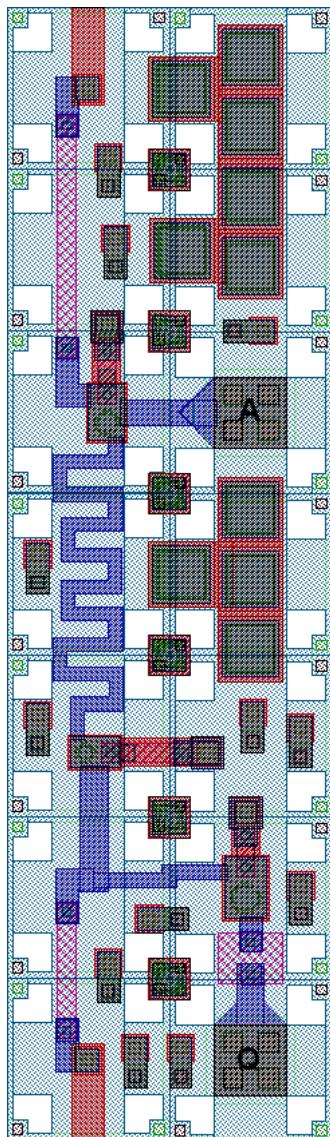


Figure 3.53: RSFQ BUFFT Layout.

Analog model

```

1  * Back-annotated simulation file written      42 | .param LP1=LP
2  *   ↪ by InductEx v.6.1.52 on 2022/08/11.    43 | .param LP2=LP
3  * Author: L. Schindler                      44 | .param LP3=LP
4  * Version: 3.0                                45 |
5  * Last modification date: 11 August 2022     46 | .param RB1=B0Rs/B1
6  * Last modification by: T. Hall              47 | .param RB2=B0Rs/B2
7  *$Ports      a      q                      48 | .param RB3=B0Rs/B3
8  .subckt THmitll_BUFFT a q                  49 |
9  .model jjmit jj(rtype=1, vg=2.8mV, cap    50 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA    51 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
   ↪ )                                         52 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
10 .param Phi0=2.067833848E-15                53 |
11 .param B0=1                                  54 | B1 1 2 jjmit area=B1
12 .param Ic0=0.0001                            55 | B2 4 5 jjmit area=B2
13 .param IcRs=100u*6.859904418                 56 | B3 8 9 jjmit area=B3
14 .param B0Rs=IcRs/Ic0*B0                     57 |
15 .param Rsheet=2                             58 | IB1 0 3 pwl(0 0 5p IB1)
16 .param Lsheet=1.13e-12                       59 | IB2 0 7 pwl(0 0 5p IB2)
17 .param LP=0.5p                             60 |
18 .param IC=2.5                               61 | LB1 3 1 1.087E-012
19 .param ICreceive=1.6                         62 | LB2 7 6 8.18E-013
20 .param ICtrans=2.5                          63 |
21 .param LB=2p                                64 | L1 a 1 1.138E-012
22 .param BiasCoef=0.7                         65 | L2 1 4 1.216E-011
23 .param Lptl=2p                             66 | L3 4 6 1.152E-012
24 .param RD=1.36                             67 | L4 6 8 2.432E-012
25                                     68 | L5 8 10 6.041E-013
26 .param B1=1.6                               69 |
27 .param B2=0.92                             70 | RD 10 q RD
28 .param B3=2.5                               71 |
29                                     72 | LP1 2 0 3.595E-013
30 .param IB1=112u                            73 | LP2 5 0 4.661E-013
31 .param IB2=218u                            74 | LP3 9 0 3.254E-013
32                                     75 |
33 .param LB1=LB                             76 | RB1 1 101 RB1
34 .param LB2=LB                             77 | LRB1 101 0 LRB1
35                                     78 | RB2 4 104 RB2
36 .param L1=Lptl                           79 | LRB2 104 0 LRB2
37 .param L2=12.2588p                        80 | RB3 8 108 RB3
38 .param L3=1.1532p                         81 | LRB3 108 0 LRB3
39 .param L4=2.4523p                         82 |
40 .param L5=Lptl                           83 | .ends
41

```

Listing 3.27: RSFQ BUFFT JoSIM netlist.

Table 3.23: RSFQ BUFFT pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ BUFFT using JoSIM is shown in Fig. 3.54. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected via a PTL to pin **q**.

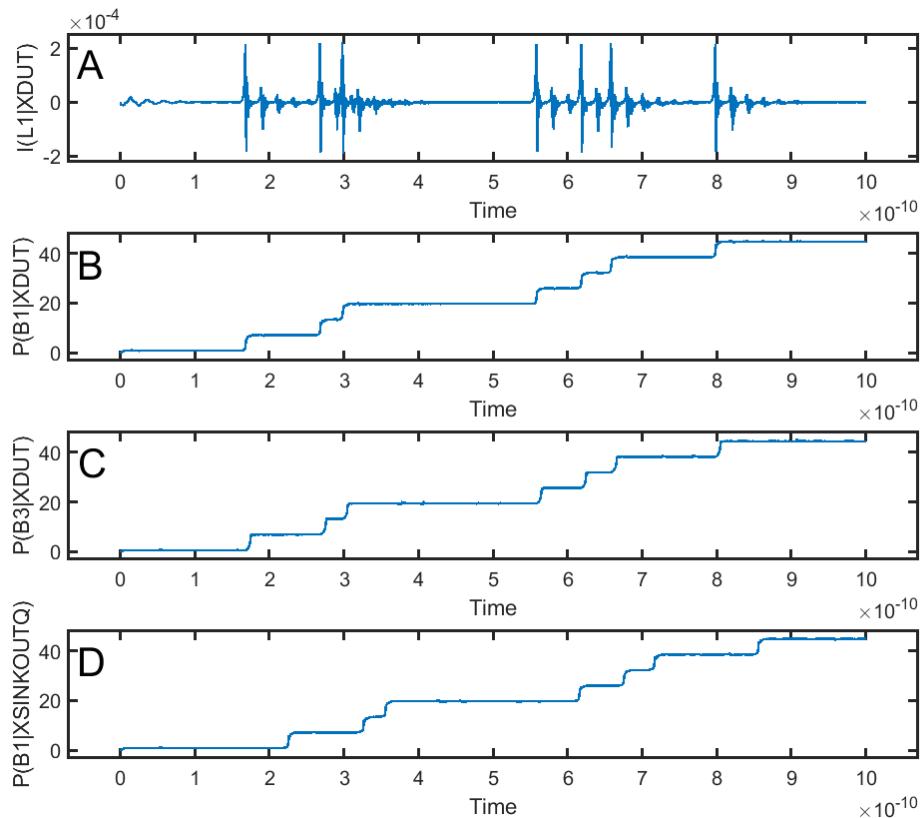


Figure 3.54: RSFQ BUFFT analog simulation results.

Digital model

```

1 // -----
2 // Author L. Schindler
3 // Version: 3.0
4 // Last Modification date: 11 August 2022
5 // Last Modification by: T. Hall
6 //
7 'timescale 1ps/100fs
8 module THmitll_BUFFT_v3p0_extracted (a, q);
9
10 input
11   a;
12
13 output
14   q;
15
16 reg
17   q;
18
19 real
20   delay_state0_a_q = 6.0,
21   ct_state0_a_a = 20.2;
22
23 reg
24   errorsignal_a;
25
26 integer
27   outfile,
28   cell_state; // internal state of the cell
29
30 initial
31 begin
32   errorsignal_a = 0;
33   cell_state = 0; // Startup state
34   q = 0; // All outputs start at 0
35 end
36
37 always @(posedge a or negedge a) // execute at positive and negative edges of input
38 begin
39   if ($time>4) // arbitrary steady-state time)
40     begin
41       if (errorsignal_a == 1'b1) // A critical timing is active for this input
42         begin
43           outfile = $fopen("errors.txt", "a");
44           $fdisplay(outfile, "Violation_of_critical_timing_in_module_%m;_%0d_ps.\n"
45           ↪ ", $stime);
46           $fclose(outfile);
47           q <= 1'bX; // Set all outputs to unknown
48         end
49       if (errorsignal_a == 0)
50         begin
51           case (cell_state)
52             0: begin
53               q <= #(delay_state0_a_q) !q;
54               errorsignal_a = 1; // Critical timing on this input; assign
55               ↪ immediately
56               errorsignal_a <= #(ct_state0_a_a) 0; // Clear error signal
57               ↪ after critical timing expires
58             end
59           endcase
60         end
61     end
62   end
63 endmodule

```

Listing 3.28: RSFQ BUFFT verilog model.

The digital simulation results for the RSFQ BUFFT is shown in Fig. 3.55 and the Mealy finite state machine diagram, extracted using *TimEx*, is shown in Fig. 3.56.

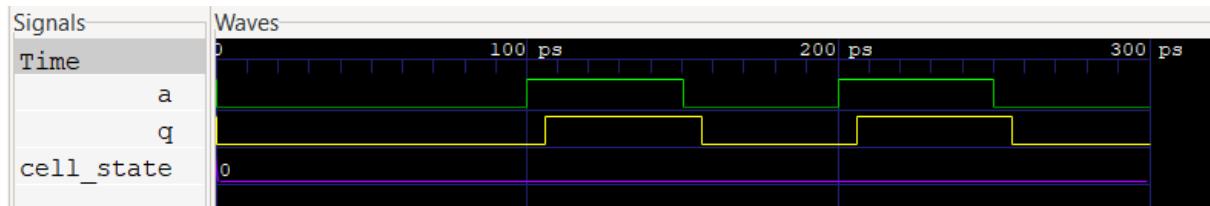


Figure 3.55: RSFQ BUFFT digital simulation results.

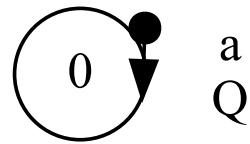


Figure 3.56: RSFQ BUFFT Mealy finite state machine diagram.

Power Consumption

Table 3.24: RSFQ BUFFT power consumption.

Clock rate (GHz)	Static power (nW)	Dynamic power (nW)
1	858	1.04
2	858	2.08
5	858	5.19
10	858	10.4
20	858	20.8
50	858	51.9

3.4 Interface Cells

3.4.1 DCSFQ-PTLTX

The RSFQ DCSFQ-PTLTX is an interface cell designed to convert input voltage pulses into SFQ pulses. The DCSFQ-PTLTX has an integrated PTL transmitter and is intended to connect directly to a PTL output.

Schematic

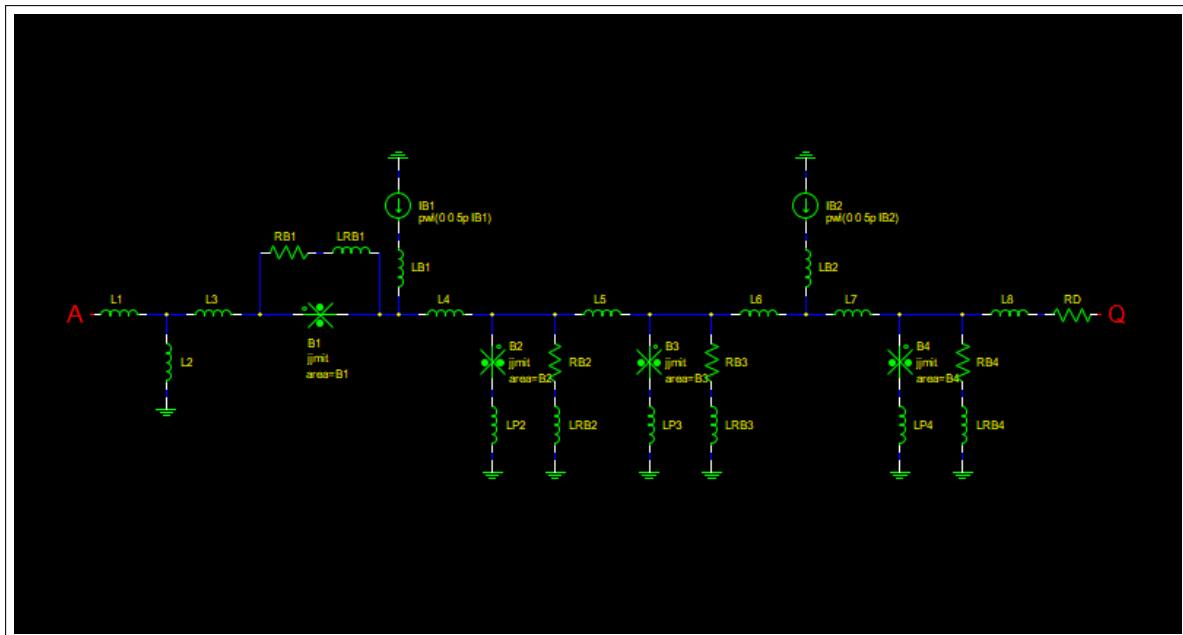


Figure 3.57: Schematic of RSFQ DCSFQ-PTLTX.

Layout

The physical layout for the RSFQ DCSFQ-PTLTX is shown in Fig. 3.58. The layout height is $70 \mu\text{m}$ and the width is $20 \mu\text{m}$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

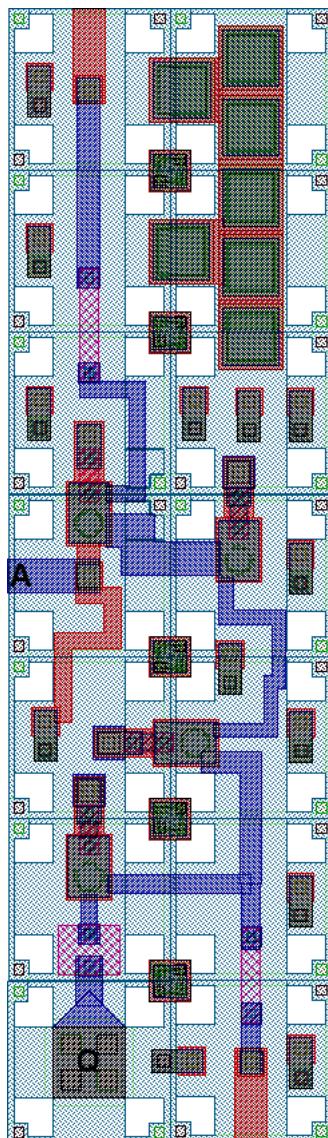


Figure 3.58: RSFQ DCSFQ-PTLTX Layout.

Analog model

```

1  * Back-annotated simulation file written      49 | .param RB1=B0Rs/B1
2  *   ↪ by InductEx v.6.1.52 on 2022/08/09.    50 | .param RB2=B0Rs/B2
3  * Author: L. Schindler                      51 | .param RB3=B0Rs/B3
4  * Version: 3.0                                52 | .param RB4=B0Rs/B4
5  * Last modification date: 14 April 2022       53 |
6  * Last modification by: T. Hall              54 |
7  *$Ports      a      q                         55 | .param LRB1=(RB1/Rsheet)*Lsheet
8 .subckt THmitll_DCSFQ-PTLTX a q             56 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
9 .model jjmit jj(rtype=1, vg=2.8mV, cap      57 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
10    ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA     58 | .param LRB4=(RB4/Rsheet)*Lsheet+LP
11    ↪ )                                         59 |
12 .param Phi0=2.067833848E-15                  60 | B1 2 3 jjmit area=B1
13 .param B0=1                                    61 | B2 5 6 jjmit area=B2
14 .param Ic0=0.0001                             62 | B3 7 8 jjmit area=B3
15 .param IcRs=100u*6.859904418                 63 | B4 11 12 jjmit area=B4
16 .param B0Rs=IcRs/Ic0*B0                     64 |
17 .param Rsheet=2                            65 | IB1 0 4 pw1(0 0 5p IB1)
18 .param Lsheet=1.13e-12                      66 | IB2 0 10 pw1(0 0 5p IB2)
19 .param LP=0.5p                           67 |
20 .param IC=2.5                            68 | LB1 4 3 3.12E-012
21 .param LB=2p                            69 | LB2 10 9 8.782E-013
22 .param BiasCoef=0.7                      70 |
23 .param Lptl=2p                           71 | LP2 6 0 5.209E-013
24 .param RD=1.36                           72 | LP3 8 0 5.058E-013
25                               73 | LP4 12 0 4.053E-013
26 .param B1=0.9*Ic                           74 |
27 .param B2=0.9*Ic                           75 | L1 a 1 1.322E-012
28 .param B3=IC                            76 | L2 1 0 3.879E-012
29 .param B4=ICtrans                        77 | L3 1 2 6.03E-013
30                               78 | L4 3 5 1.104E-012
31 .param IB1=(11/9)*Ic0*B2                79 | L5 5 7 4.572E-012
32 .param IB2=BiasCoef*Ic0*(B3+B4)          80 | L6 7 9 2.078E-012
33                               81 | L7 9 11 2.073E-012
34 .param LB1=LB                           82 | L8 11 13 8.436E-013
35 .param LB2=LB                           83 |
36                               84 | RD 13 q RD
37 .param LP2=LP                           85 |
38 .param LP3=LP                           86 | RB1 2 102 RB1
39 .param LP4=LP                           87 | LRB1 102 3 LRB1
40                               88 | RB2 5 105 RB2
41 .param L1=1p                            89 | LRB2 105 0 LRB2
42 .param L2=3.9p                           90 | RB3 7 107 RB3
43 .param L3=0.6p                           91 | LRB3 107 0 LRB3
44 .param L4=1.1p                           92 | RB4 11 111 RB4
45 .param L5=Phi0/(2*B2*Ic0)               93 | LRB4 111 0 LRB4
46 .param L6=Phi0/(4*B3*Ic0)               94 |
47 .param L7=Phi0/(4*B3*Ic0)               95 | .ends
48 .param L8=Lptl

```

Listing 3.29: RSFQ DCSFQ-PTLTX JoSIM netlist.

Table 3.25: RSFQ DCSFQ-PTLTX pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ DCSFQ-PTLTX using JoSIM is shown in Fig. 3.59. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the current through the output inductor connected to pin **q**,
- (c) the phase over the output JJ of pin **q**, and
- (d) the phase over the input JJ of the load circuit connected through a PTL to pin **q**.

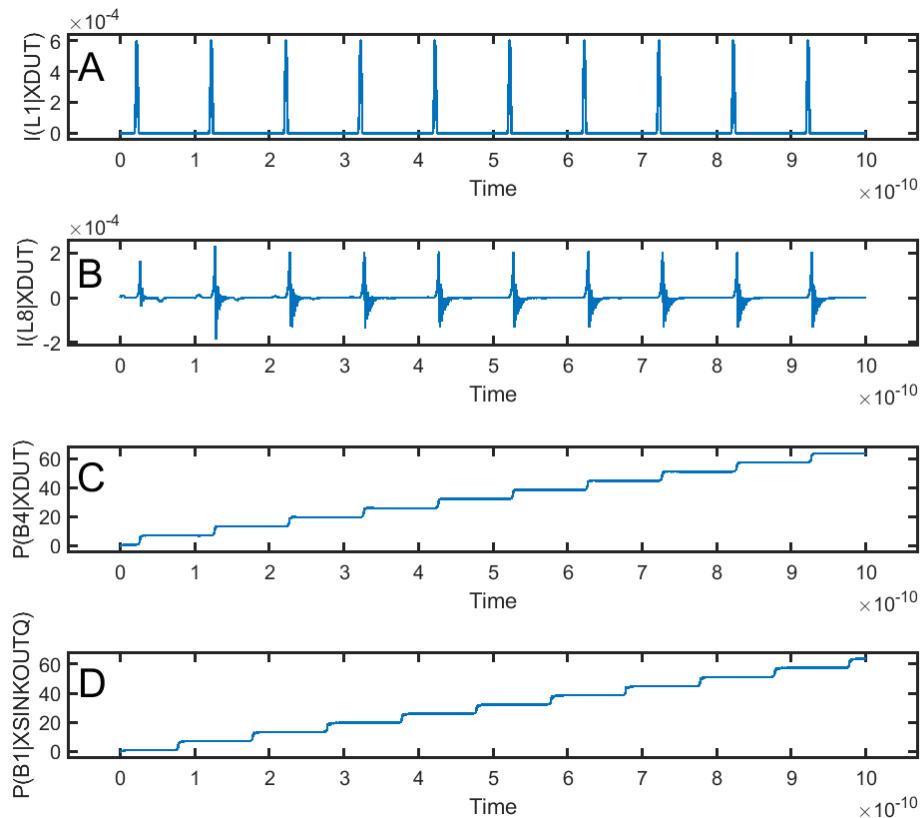


Figure 3.59: RSFQ DCSFQ-PTLTX analog simulation results.

3.4.2 PTLRX-SFQDC

The RSFQ PTLRX-SFQDC is an interface cell designed to convert SFQ pulses to an output voltage level which can be measured by standard equipment. The PTLRX-SFQDC has an integrated PTL receiver and is intended to be connected directly to a PTL input.

Schematic

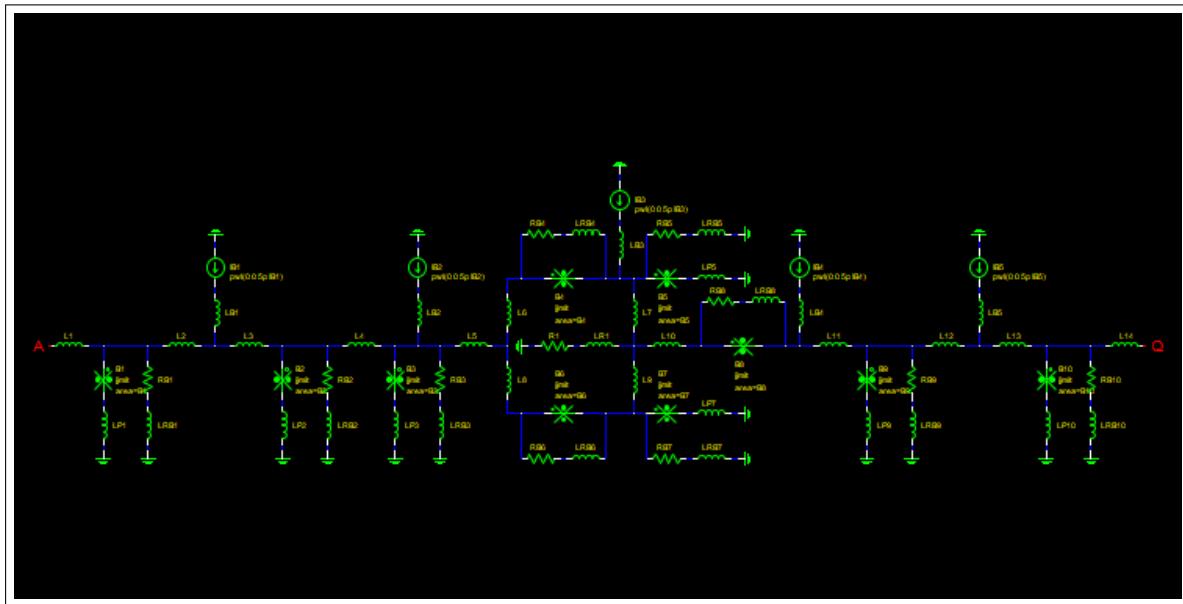


Figure 3.60: Schematic of RSFQ PTLRX-SFQDC.

Layout

The physical layout for the RSFQ PTLRX-SFQDC is shown in Fig. 3.61. The layout height is $70 \mu m$ and the width is $40 \mu m$. The biasing is brought in on M5 from external bias lines at the top and bottom of the cell. The PTL connection extends to connect to a PTL on either M1 or M3. All bias resistors are designed to be connected to a 2.6 mV voltage source.

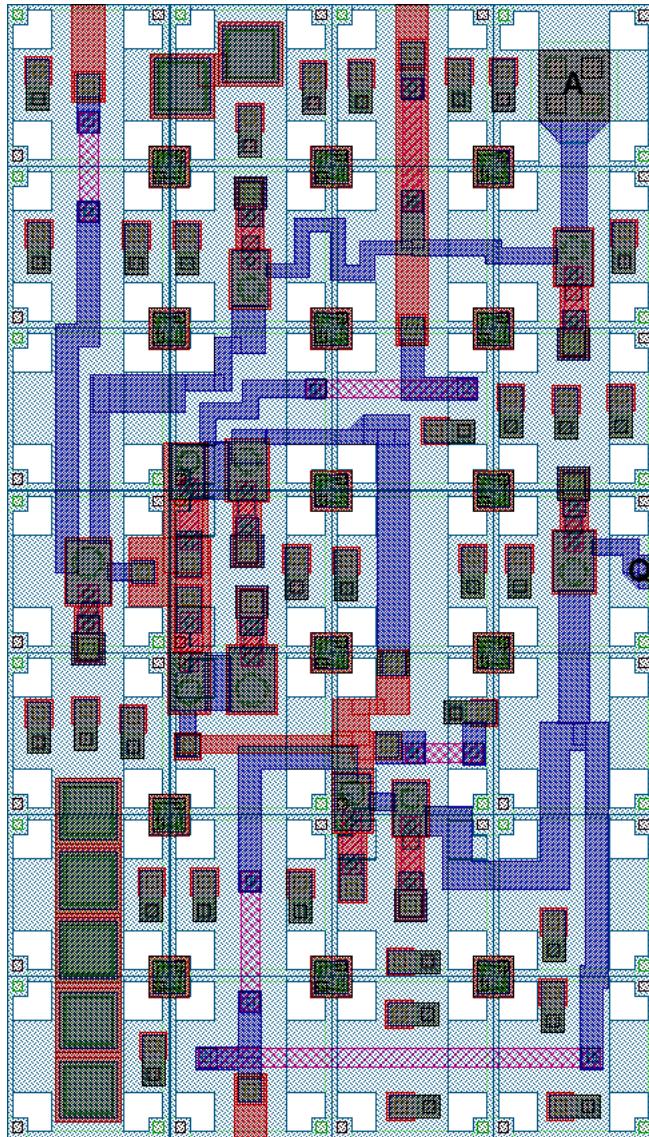


Figure 3.61: RSFQ PTLRX-SFQDC Layout.

Analog model

```

1  * Back-annotated simulation file written      64 | .param LR1=0.7066p
2  *   ↪ by InductEx v.6.1.52 on 2022/08/14.    65 | .param R1=5.74
3  * Adapted from Fluxonics SDQDC_v5          66 | .param LP1=LP
4  * Author: L. Schindler                     67 | .param LP2=LP
5  * Version: 3.0                           68 | .param LP3=LP
6  * Last modification date: 13 August 2022  69 | .param LP5=LP
7  * Last modification by: T. Hall           70 | .param LP7=LP
8  *$Ports      a      q                  71 | .param LP9=LP
9  .subckt THmitll_PTLRX-SFQDC a q          72 | .param LP10=LP
10 .model jjmit jj(rtype=1, vg=2.8mV, cap  73 | .param RB1=B0Rs/B1
11   ↪ =0.07pF, r0=160, rn=16, icrit=0.1mA 74 | .param RB2=B0Rs/B2
12 .param Phi0=2.067833848E-15            75 | .param RB3=B0Rs/B3
13 .param B0=1                            76 | .param RB4=B0Rs/B4
14 .param Ic0=0.0001                      77 | .param RB5=B0Rs/B5
15 .param IcRs=100u*6.859904418          78 | .param RB6=B0Rs/B6
16 .param B0Rs=IcRs/Ic0*B0              79 | .param RB7=B0Rs/B7
17 .param Rsheet=2                        80 | .param RB8=B0Rs/B8
18 .param Lsheet=1.13e-12                81 | .param RB9=B0Rs/B9
19 .param LP=0.5p                         82 | .param RB10=B0Rs/B10
20 .param IC=2.5                          83 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
21 .param ICreceive=1.6                 84 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
22 .param ICtrans=2.5                   85 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
23 .param LB=2p                          86 | .param LRB4=(RB4/Rsheet)*Lsheet
24 .param BiasCoef=0.7                 87 | .param LRB5=(RB5/Rsheet)*Lsheet+LP
25 .param Lptl=2p                       88 | .param LRB6=(RB6/Rsheet)*Lsheet
26 .param RD=1.36                        89 | .param LRB7=(RB7/Rsheet)*Lsheet+LP
27 .param B1=1.6                          90 | .param LRB8=(RB8/Rsheet)*Lsheet
28 .param B2=1.62                        91 | .param LRB9=(RB9/Rsheet)*Lsheet+LP
29 .param B3=2.76                        92 | .param LRB10=(RB10/Rsheet)*Lsheet+LP
30 .param B4=1.34
31 .param B5=1.98
32 .param B6=1.82
33 .param B7=3.15
34 .param B8=1.65
35 .param B9=1.22
36 .param B10=2.18
37 .param IB1=229u
38 .param IB2=292u
39 .param IB3=167u
40 .param IB4=212u
41 .param IB5=64u
42 .param LB1=LB
43 .param LB2=LB
44 .param LB3=LB
45 .param LB4=LB
46 .param LB5=LB
47 .param L1=Lptl
48 .param L2=2.3453p
49 .param L3=3.9596p
50 .param L4=4.5142p
51 .param L5=0.7362p
52 .param L6=0.9663p
53 .param L7=5.6790p
54 .param L8=0.8679p
55 .param L9=3.2739p
56 .param L10=0.2245p
57 .param L11=0.695p
58 .param L12=3.036p
59 .param L13=1.6165p
60 .param L14=1.510p
61
62
63
64 | .param LR1=0.7066p
65 | .param R1=5.74
66 | .param LP1=LP
67 | .param LP2=LP
68 | .param LP3=LP
69 | .param LP5=LP
70 | .param LP7=LP
71 | .param LP9=LP
72 | .param LP10=LP
73 | .param RB1=B0Rs/B1
74 | .param RB2=B0Rs/B2
75 | .param RB3=B0Rs/B3
76 | .param RB4=B0Rs/B4
77 | .param RB5=B0Rs/B5
78 | .param RB6=B0Rs/B6
79 | .param RB7=B0Rs/B7
80 | .param RB8=B0Rs/B8
81 | .param RB9=B0Rs/B9
82 | .param RB10=B0Rs/B10
83 | .param LRB1=(RB1/Rsheet)*Lsheet+LP
84 | .param LRB2=(RB2/Rsheet)*Lsheet+LP
85 | .param LRB3=(RB3/Rsheet)*Lsheet+LP
86 | .param LRB4=(RB4/Rsheet)*Lsheet
87 | .param LRB5=(RB5/Rsheet)*Lsheet+LP
88 | .param LRB6=(RB6/Rsheet)*Lsheet
89 | .param LRB7=(RB7/Rsheet)*Lsheet+LP
90 | .param LRB8=(RB8/Rsheet)*Lsheet
91 | .param LRB9=(RB9/Rsheet)*Lsheet+LP
92 | .param LRB10=(RB10/Rsheet)*Lsheet+LP
93 | .param B1 1 2 jjmit area=B1
94 | .param B2 5 6 jjmit area=B2
95 | .param B3 7 8 jjmit area=B3
96 | .param B4 11 12 jjmit area=B4
97 | .param B5 12 13 jjmit area=B5
98 | .param B6 16 17 jjmit area=B6
99 | .param B7 17 18 jjmit area=B7
100 | .param B8 20 21 jjmit area=B8
101 | .param B9 23 24 jjmit area=B9
102 | .param B10 27 28 jjmit area=B10
103 | .param IB1 0 4 pwl(0 0 5p IB1)
104 | .param IB2 0 9 pwl(0 0 5p IB2)
105 | .param IB3 0 14 pwl(0 0 5p IB3)
106 | .param IB4 0 22 pwl(0 0 5p IB4)
107 | .param IB5 0 26 pwl(0 0 5p IB5)
108
109 | .param LB1 4 3 6.848E-013
110 | .param LB2 9 7 4.296E-012
111 | .param LB3 0 14 pwl(0 0 5p LB1)
112 | .param LB4 0 22 pwl(0 0 5p LB2)
113 | .param LB5 0 26 pwl(0 0 5p LB3)
114
115 | .param L1 a 1 1.455E-012
116 | .param L2 1 3 2.346E-012
117 | .param L3 3 5 3.959E-012
118 | .param L4 5 7 4.522E-012
119 | .param L5 7 10 7.386E-013
120
121 | .param L6 11 10 9.705E-013
122 | .param L7 12 15 5.626E-012
123 | .param L8 10 16 8.718E-013
124 | .param L9 15 17 3.248E-012
125
126
127
128
129

```

```

130 | L10 15 20 2.239E-013
131 | L11 21 23 6.903E-013
132 | L12 23 25 3.044E-012
133 | L13 25 27 1.603E-012
134 | L14 27 q 1.635E-012
135
136 | LR1 19 15 7.057E-013
137 | R1 0 19 R1
138
139 | LP1 2 0 4.229E-013
140 | LP2 6 0 4.418E-013
141 | LP3 8 0 4.758E-013
142 | LP5 13 0 4.434E-013
143 | LP7 18 0 6.22E-013
144 | LP9 24 0 3.836E-013
145 | LP10 28 0 3.18E-013
146
147 | RB1 1 101 RB1
148 | LRB1 101 0 LRB1
149 | RB2 5 105 RB2
150 | LRB2 105 0 LRB2
151 | RB3 7 107 RB3
152 | LRB3 107 0 LRB3
153 | RB4 11 111 RB4
154 | LRB4 111 12 LRB4
155 | RB5 12 112 RB5
156 | LRB5 112 0 LRB5
157 | RB6 16 116 RB6
158 | LRB6 116 17 LRB6
159 | RB7 17 117 RB7
160 | LRB7 117 0 LRB7
161 | RB8 20 120 RB8
162 | LRB8 120 21 LRB8
163 | RB9 23 123 RB9
164 | LRB9 123 0 LRB9
165 | RB10 27 127 RB10
166 | LRB10 127 0 LRB10
167
168 | .ends

```

Listing 3.30: RSFQ PTLRX-SFQDC JoSIM netlist.

Table 3.26: RSFQ PTLRX-SFQDC pin list.

Pin	Description
a	Data input
q	Data output

The simulation results for the RSFQ PTLRX-SFQDC using JoSIM is shown in Fig. 3.62. The figure shows the graph for:

- (a) the current through the input inductor connected to pin **a**,
- (b) the phase over the input JJ of pin **a**,
- (c) the current through the output inductor connected to pin **q**, and
- (c) the voltage over the load resistor connected to pin **q**.

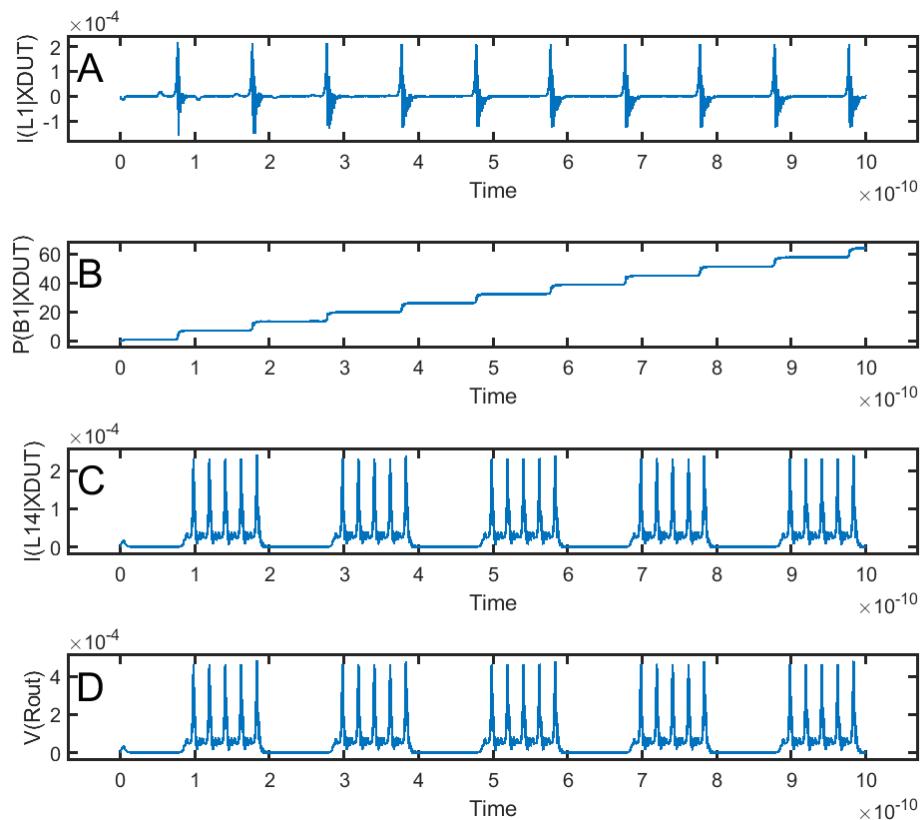


Figure 3.62: RSFQ PTLRX-SFQDC analog simulation results.

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