PHYS328W Notes

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1 DC Circuits

1.1 Ohm's Law and Ohmic Devices

The potential difference V between the terminals of an **Ohmic device** is directly proportional to the current I flowing through it,

$$V = IR \tag{1}$$

The constant of proportionality R is called the **resistance** of the device. Equation 1 is known as **Ohm's Law**. **Non-ohmic** devices do not follow the linear voltage-current relationship of Ohm's law. Examples include diodes, thermistors, photoresistors, and light-bulb filaments.

Ohmic devices called **resistors** are ubiquitous in electronic circuits. When current flows through a resistor, power is dissipated in the form of heat and light. The power dissipated in a resistor given by

$$P_{\text{diss}} = I^2 R = \frac{V^2}{R} \tag{2}$$

1.2 Resistors in Series and Parallel

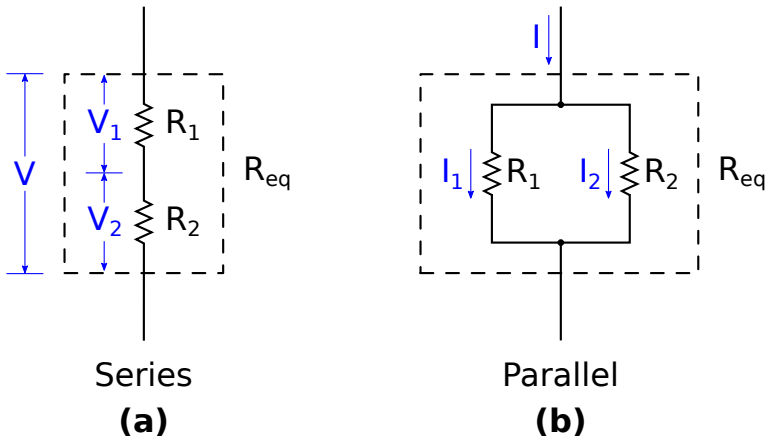

Figure 1: A pair of resistors connected (a) in series and (b) in parallel.

A pair of resistors can be connected either in **series** or in **parallel** as shown in Figure 1. Note that two wires emerge from each pair. The **equivalent resistance** R_{eq} of a pair of resistors is the resistance

between these two wires. The equivalent resistance of two or more resistors connected in series is given by

$$R_{eq} = R_1 + R_2 + R_3 + ... \tag{3}$$

and that of two or more resistors connected in parallel is given by

$$\frac{1}{R_{eq}} = \frac{1}{R_1} + \frac{1}{R_2} + \frac{1}{R_3} + ... \tag{4}$$

The notation $R_1||R_2||R_3...$ is sometimes used for the equivalent resistance of parallel resistors.

A pair of resistors connected in series as shown in panel (a) of Figure 1 is a **voltage divider**. The two resistors share the total potential difference V across the pair according to

$$V_1 = \frac{R_1}{R_1 + R_2} V \tag{5}$$

and

$$V_2 = \frac{R_2}{R_1 + R_2} V \tag{6}$$

A pair of resistors connected in parallel as shown in panel (b) of Figure 1 is a **current divider**. The two resistors share the total current I flowing into the pair according to

$$I_1 = \frac{R_2}{R_1 + R_2} I \tag{7}$$

and

$$I_2 = \frac{R_1}{R_1 + R_2} I \tag{8}$$

where I_1 is the current flowing through R_1 and I_2 is the current flowing through R_2.

These equivalent resistance, voltage division, and current division expressions can be proven using Kirchhoff's rules, introduced in Section 1.4.

1.3 Resistor Network Analysis

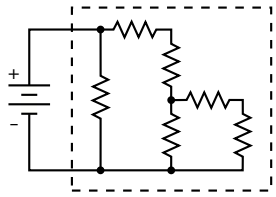

Figure 2: A resistor network powered by a voltage source.

A **resistor network** is a collection of resistors connected together as illustrated in Figure 2. Many resistor networks can be reduced to a single resistance between two points using Equations 3 and 4. If a network can be simplified in this way, the currents flowing through all of the resistors in the network can be calculated by working backward through the equivalent resistance calculation and applying the current division expression of Equation 7 at each step.

If a network includes one or more Δ configurations — three resistors connected by junctions — it cannot be simplified via series and parallel pairs. A **junction** is a point in a circuit where three or more

wires meet. Junctions are marked with • symbols in the schematics in these notes. However, any Δ configuration in a network can be replaced with an equivalent Y-shaped configuration via a $\Delta - Y$ transformation. This is easy to look up. We won't concern ourselves with this situation.

Resistor Network Analysis Summary

1. Use the equivalent resistance expressions (Equations 3 and 4) to find the equivalent resistance of the entire network.
2. Use Ohm's law to calculate the current flowing through the voltage source.
3. Use the current division expressions (Equations 7) at each node to determine the currents in the network.
4. Use Ohm's law to determine the voltage drops across the resistors and from these, the voltages of all of the nodes.

1.4 Kirchhoff's Rules

Kirchhoff's Rules are used in the analysis of DC circuits and AC circuits in the low-frequency limit — in which magnetic induction does not induce currents in the wires connecting elements in the circuit.

The first rule, the **loop rule**, states that the total change in electric potential around a closed loop must be zero. This means that the sum of the potential differences across all of the devices in a closed loop must be zero,

$$\sum_{\text{loop}} V_i = 0 \tag{9}$$

Signs are assigned to the V_i according to the conventions illustrated in Figure 3.

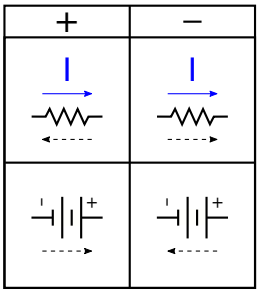

Figure 3: Sign conventions for the potential differences in Kirchhoff's loop rule equations. The blue arrows represent the direction of current flow. The black dashed arrows represent the direction the device is traversed in the process of generating the equation and therefore does not represent a physical quantity.

The second rule, known as the **junction rule**, applies to currents. This rule states that no net current enters or leaves a junction,

$$\sum_{\text{junction}} I_i = 0 \tag{10}$$

In the usual sign convention, currents flowing into a junction are positive, and currents flowing out of a junction are negative.

Circuit Analysis using Kirchhoff's Rules

1. Draw the circuit with arrows and labels representing all of the unique currents.
2. Construct a set of loop-rule equations including every device in the circuit at least once.
3. Construct a set junction-rule equations including every current in the circuit at least once.
4. Given enough known quantities (usually the properties of the devices in the circuit — resistances, capacitances, source voltages, e.g.), these equations can be combined algebraically to determine the unknown quantities (usually currents and potential differences in the circuit).

1.5 Thévenin's Theorem

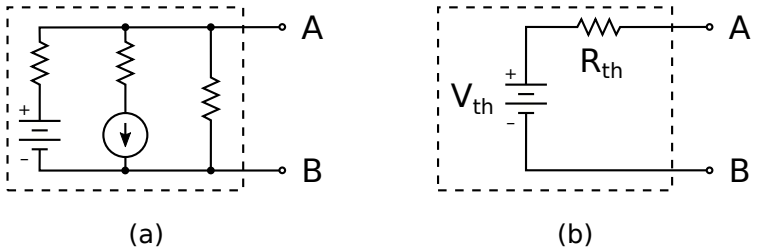

Figure 4: Illustration of the Thévenin equivalent circuit (b) for a circuit (a) designed to drive a load connected across terminals A and B.

Any DC circuit consisting solely of resistors and voltage and current sources can be replaced by a **Thévenin equivalent circuit** consisting of a single DC voltage source in series with a resistor as illustrated in Figure 4. The theorem also applies to the frequency response of AC circuits containing linear, passive devices — resistors, inductors, and capacitors.

Finding the Thévenin Equivalent of a Circuit

1. The Thévenin equivalent voltage V_{th} is the voltage across the output terminals A and B of the circuit with no load attached.
2. The Thévenin equivalent resistance R_{th} is the resistance of the circuit measured between the output terminals A and B, with all voltage and current sources replaced with their internal resistances. *Ideal voltage sources have zero resistance, and ideal current sources have infinite resistance.*

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2 AC Circuits

Alternating current (AC) circuits involve potential differences and currents which vary periodically — often sinusoidally — with time. The time-dependent response of an AC circuit to a sinusoidal driving signal consists of a transient component that dies off due to resistive losses, and a sinusoidal steady-state component. We will focus on the steady-state behavior of the AC circuits we consider.

2.1 Resistance, Reactance, and Impedance: the Complex Number Representation

When driven by a sinusoidal signal, the resulting currents through and potential differences across capacitors, inductors, and resistors are all sinusoidal as well, but with different, *constant*, phase relationships to each other.

CIVIL

> The mnemonic CIVIL can be used to remember that the voltage across a capacitor lags $\pi/2$ (half a period of oscillation) behind the current (CIV), and the voltage across an inductor leads the current by $\pi/2$ (VIL). The voltage across a resistor is always in phase with the current.

Ohm's law (Equation 1) gives the full relationship between current and voltage for a resistor. Capacitors and inductors are also linear devices, but they impede the flow of current in the circuit by temporarily storing energy in magnetic and electric fields instead of by dissipating energy. We refer to these non-dissipative devices as reactive devices, and we define quantities analogous to resistance and which play the same role as resistance in a generalized version of Ohm's law. The **inductive reactance** is given by

$$X_L = j\omega L \tag{11}$$

where, $\omega = 2\pi f$ is the driving frequency, and L is the inductance. In an electronics context, j is typically used to represent $\sqrt{-1}$ instead of i to avoid confusion with current. The **capacitive reactance**

$$X_C = -\frac{j}{\omega C} \tag{12}$$

where C is the capacitance. The factors of j account for the relative phases of the voltages and currents. Here, we are taking advantage of the fact that the phase relationships between the positive and negative imaginary axes and the real axis of the complex plane map onto those between signals in inductors, capacitors, and resistors, respectively.

Any network of linear devices — inductors, resistors, and capacitors — present a *complex* **impedance** Z to the flow of current. The total impedance can be found by combining the *real* resistances and *imaginary* reactances in the circuit in the same way that we determined equivalent resistance in Section 1.2. The inductive and capacitive reactances and hence the total impedance Z are frequency-dependent. In the low-frequency limit, capacitors dominate the impedance, while in the high-frequency limit, inductors dominate.

2.2 Phasor Analysis

We use complex numbers to represent impedance Z and complex functions to represent voltage and current as a bookkeeping tool that simplifies the mathematics involved in circuit analysis. The real-valued observable voltage and current are obtained by taking the real part of the complex voltage and

current functions.

$$\begin{aligned} v(t) &= Re\left(V\, e^{j(\omega t+\phi_v)}\right) = V\cos(\omega t+\phi_v) \\ i(t) &= Re\left(I\, e^{j(\omega t+\phi_i)}\right) = I\cos(\omega t+\phi_i) \end{aligned} \tag{13}$$

In many cases, we are only interested in the amplitudes V and I. In cases in which we do care about the phase, we typically consider either ϕ_i or ϕ_v to be zero and keep track of the relative phase.

The complex voltage and current functions share an identical time-dependent factor $e^{j\omega t}$, which cancels out of equations that relate them. It is therefore convenient to analyze AC circuits using **phasors**,

$$\begin{aligned} \mathbf{V} &= V\, e^{j\phi_v} \\ \mathbf{I} &= I\, e^{j\phi_i} \end{aligned} \tag{14}$$

We can express the real voltage and current functions in terms of phasors as

$$\begin{aligned} v(t) &= Re(\mathbf{V}\, e^{j\omega t}) \\ i(t) &= Re(\mathbf{I}\, e^{j\omega t}) \end{aligned} \tag{15}$$

and the generalized version of Ohm's law becomes

$$\mathbf{I} = \frac{\mathbf{V}}{Z} \tag{16}$$

The power in a component or network of components is given by

$$\mathbf{P} = \mathbf{I}^*\mathbf{V} = IV\, e^{j(\phi_v-\phi_i)} \tag{17}$$

The real part of the power is the power dissipated in resistors. The imaginary part is the **reactive power** stored in capacitors and inductors. Typically, we are interested in the average power dissipated

$$\langle P\rangle = \frac{IV}{2}\cos(\phi_v-\phi_i) = \frac{V^2}{2Z}\cos(\phi_v-\phi_i) \tag{18}$$

The factor of $1/2$ is the average value of $\cos^2(\omega t)$ — Equation 18 gives the root mean square power.

Notice that if the relative phase $\phi_v-\phi_i$ is either $\pi/2$ or $-\pi/2$, no power is dissipated. These relative phases are only possible if the impedance has no real part meaning there is no resistance present.

Phasor Analysis

- Equivalent impedance calculations work the same way as equivalent resistance calculations (Equations 3 and 4).
- Kirchhoff's rules work for phasors **V** and **I**.
- Thévenin's theorem applies to AC circuits containing only linear components. The Thévenin voltage and impedance are found via the process outlined in Section 1.5 with impedance in place of resistance.

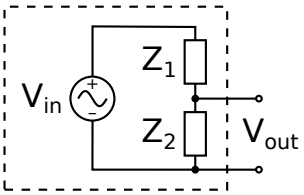

Figure 5: AC voltage divider between two linear devices, or networks of linear devices, with complex impedances Z_1 and Z_2.

2.3 AC Voltage Dividers

The AC voltage divider circuit shown in Figure 5 consists of two linear devices, which can be networks of linear devices, with complex impedances Z_1 and Z_2. This is a series circuit, so the current $\mathbf{I}$ flowing through all three components is the same.

The loop rule equation

$$\mathbf{V_{in}} - \mathbf{I}Z_1 - \mathbf{I}Z_2 = 0 \tag{19}$$

and the generalized Ohm's law for Z_2

$$\mathbf{V_{out}} = \mathbf{I}Z_2 \tag{20}$$

combine to give

$$\mathbf{V_{out}} = \frac{Z_2}{Z_1 + Z_2}\mathbf{V_{in}} \tag{21}$$

The real-valued amplitude of the output signal is the magnitude of the phasor $\mathbf{V_{out}}$,

$$V_{out} = \sqrt{\mathbf{V}^*_{\mathbf{out}}\mathbf{V_{out}}} \tag{22}$$

Phase Angle

The phase difference ϕ between $\mathbf{V_{out}}$ and $\mathbf{V_{in}}$ is the **phase angle** between these complex numbers in the complex plane. Since we are only looking for the *difference*, we are free to set the complex phase of $\mathbf{V_{in}}$ to zero. This makes it easier to see that the only contribution to the complex phase in Equation 21 comes from the impedances, and that the phase angle of $\mathbf{V_{out}}$ relative to $\mathbf{V_{in}}$ is determined by the real and imaginary parts of the impedance ratio,

$$\tan\phi = \frac{Im\left(\frac{Z_2}{Z_1+Z_2}\right)}{Re\left(\frac{Z_2}{Z_1+Z_2}\right)} \tag{23}$$

> *Note: The phase angle of an AC circuit is sometimes defined as the phase difference between* $\mathbf{V_{in}}$ *and* $\mathbf{I}$*, but we will Eq. 23, and these definitions are not in general equivalent.*

Voltage Gain

The **voltage gain** A_V of the circuit is the ratio V_{out}/V_{in}. It follows from Equation 21

$$A_V = \frac{V_{out}}{V_{in}} = \frac{|\mathbf{V_{out}}|}{|\mathbf{V_{in}}|} = \left|\frac{Z_2}{Z_1 + Z_2}\right| = \sqrt{\left(\frac{Z_2}{Z_1 + Z_2}\right)^*\left(\frac{Z_2}{Z_1 + Z_2}\right)} \tag{24}$$

We sometimes refer to the "3 dB point(s)" of a circuit. These are driving frequencies at which the *power* gain is $\frac{1}{2}$, which corresponds to voltage gain $A_v = \frac{1}{\sqrt{2}}$ (see Appendix E).

Example: Series RLC Circuit

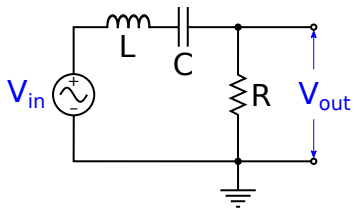

Figure 6: A series RLC circuit as an AC voltage divider.

A series RLC circuit is shown in Figure 6. We will treat this as a voltage divider between the series inductor-capacitor pair and the resistor. The resistor is by itself in the lower part of the divider, so $Z_2 = R$. The inductor and capacitor are connected in series, so we combine their reactances as we would series resistances (Equation 3)

$$Z_1 = j\left(\omega L - \frac{1}{\omega C}\right) \tag{25}$$

Equation 24 becomes

$$\frac{V_{out}}{V_{in}} = \sqrt{\frac{R^2}{R^2 + (\omega L - 1/\omega C)^2}} \tag{26}$$

To evaluate the phase angle, it is helpful to put the impedance ratio in Equation 22 in $a + jb$ form by multiplying the numerator and denominator by the complex conjugate of the denominator

$$\frac{Z_2}{Z_1 + Z_2} = \frac{R}{R + j\left(\omega L - \frac{1}{\omega C}\right)} = \frac{R^2 - jR\left(\omega L - \frac{1}{\omega C}\right)}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2} \tag{27}$$

which, with Equation 23, gives

$$\tan\phi = \frac{\frac{1}{\omega C} - \omega L}{R} \tag{28}$$

Figure 7 illustrates the potential differences across the resistor $v_{out}(t)$ and the AC voltage source $v_{in}(t)$ as they would appear on an oscilloscope. The phase angle ϕ is proportional to the time difference $\Delta t = t_{V_{out}} - t_{V_{in}}$ between the two signals, illustrated in panel (a) of the figure, as

$$\Delta t = -\frac{\phi}{\omega} = -\frac{\phi}{2\pi f} = -\frac{\phi}{2\pi} T \tag{29}$$

where T is the period of oscillation of the input signal. The minus sign in Eq. 29 is due to the fact that a positive time difference corresponds to a V_{out} that is delayed relative to V_{in}, corresponding to a negative (capacitive) phase angle. *Warning: if you use the automated Phase measurement on a digital oscilloscope, it will not account for this minus sign!*

There is a special frequency, called the **resonant frequency** ω_o of the circuit, at which the impedance Z_1 of the inductor-capacitor pair goes to zero, the current I is maximal, $V_{out} = V_{in}$ and the phase angle ϕ is zero. Combining Equations 11 and 12 to find the the frequency at which the capacitive and inductive reactances X_L and X_C have equal magnitudes and cancel out, yields

$$\omega_o = \frac{1}{\sqrt{LC}} \tag{30}$$

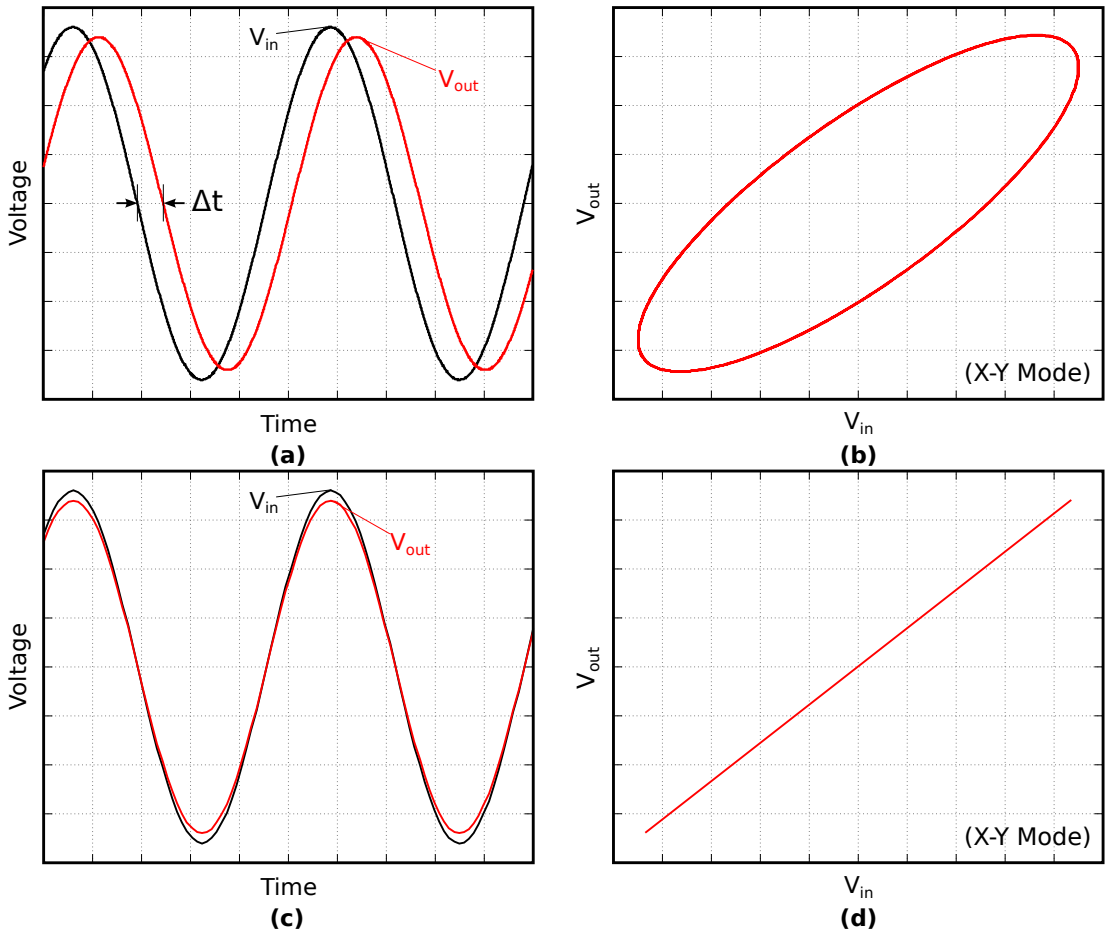

Figure 7: Oscilloscope displays of the potential differences across the resistor and AC power source in the series RLC voltage divider shown in Figure 6. Panels (a) and (b) show the potential vs. time and X-Y mode displays for the circuit at a non-resonant driving frequency. Panels (c) and (d) show the same displays at the resonant frequency ω_o of the circuit.

Panels (c) and (d) of Figure 7 illustrate the potential differences across the resistor $v_{out}(t)$ and the AC source $v_{in}(t)$ at resonance. The plots show V_{out} slightly less than V_{in} at resonance due to the internal resistance of a non-ideal inductor.

Figure 8 illustrates the frequency response of the circuit. The **voltage gain** $A_V = V_{out}/V_{in}$ is plotted in panel (a) and the phase angle ϕ is plotted in panel (b). This circuit acts as a **band pass filter**. It transmits the input signal in a range of frequencies. The **band width** of the filter is the difference between its 3 dB points. The phase angle plot shows that the impedance is dominated by the capacitor at low frequencies and by the inductor at high frequencies as we would expect based on the frequency dependence of the respective reactances (Equations 11 and 12).

We can also make sense of the qualitative behavior of the phase angle using the CIVIL mnemonic. At low frequencies, where the capacitor dominates, we expect the current to lead the voltage across the capacitor (CIV). In this circuit, v_{out} is the voltage across the resistor, which is in phase with the current, so we expect a positive phase angle at low frequencies. At high frequencies, the inductor dominates, and the current lags behind the voltage across the inductor (VIL). This gives a negative phase angle.

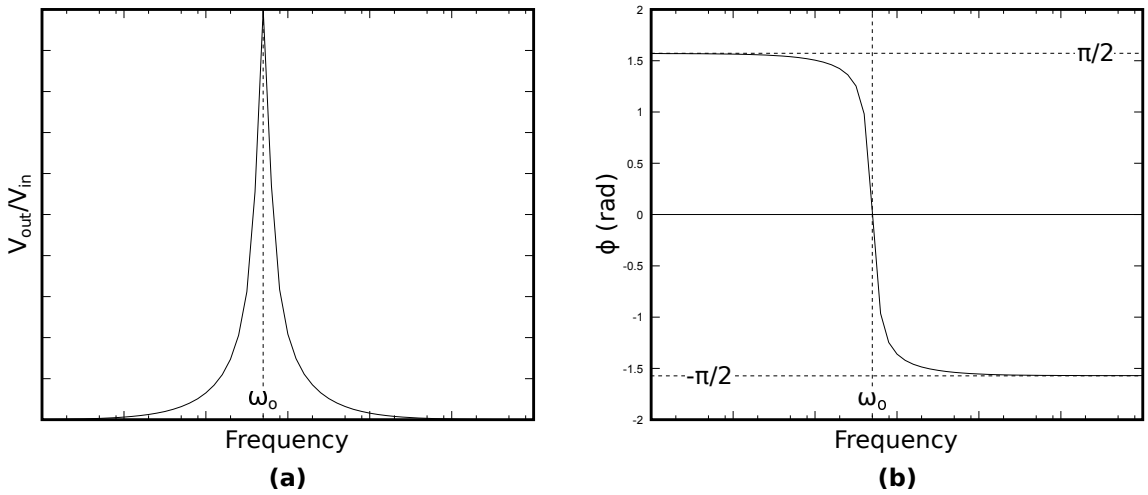

Figure 8: Frequency response — (a) gain V_{out}/V_{in} and (b) phase angle ϕ — of the series RLC voltage divider shown in Figure 6. Note that frequency is on a log scale in both plots.

Which of these situations is illustrated in panel (a) of Figure 7?

3 Diodes

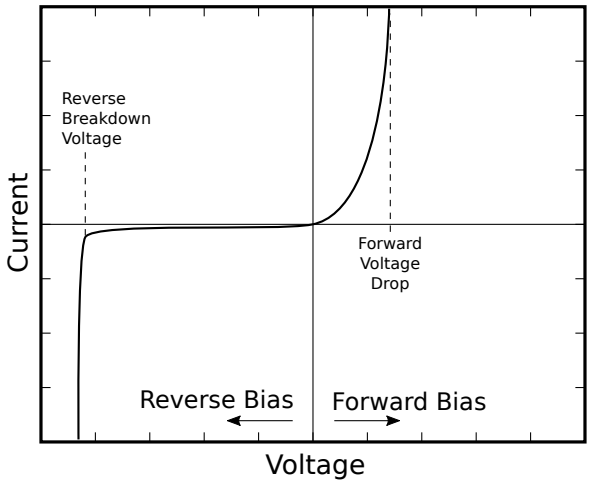

Figure 9: *Qualitative* V-I curve for a standard diode. *The scale on the reverse-bias side of the graph is roughly two orders of magnitude larger than the forward-bias side.*

Diodes are non-Ohmic, passive devices containing a junction between p-type and n-type semiconductor. The n-type (negative) region contains extra electrons and the p-type (positive) region contains extra electron vacancies. Electrons diffuse from the n-type region into the p-type region, and electron-vacancies in the p-type region diffuse into the n-type region, creating an electric field pointing toward the p-type region. The region of field is called the **depletion region**. The electric field in the depletion region acts as a "hill" in the potential-energy landscape. When a potential difference is applied to the device oriented to create an electric field in the "uphill" direction, toward the n-type region, the hill is reduced in height, and if the applied potential difference is larger than the height of the hill, called the **forward voltage drop**, current flows through the junction. If a potential difference is applied creating an electric field in the "downhill" direction, the height of the hill is increased, and the flow of current is blocked. There is a maximum "downhill" potential difference called the **reverse breakdown voltage** beyond which current flows backward across the junction. This damages standard diodes. The V vs. I curve of a standard diode is sketched qualitatively in Figure 9. The forward voltage drop and reverse breakdown voltage are labeled in the figure. The arrow in the schematic symbol for a diode ($\rightarrow\!\!|\!\!-$) points in the "forward" direction.

Standard diodes are designed to operate between the reverse breakdown voltage and the forward bias voltage. At the forward bias voltage, also called the **diode drop**, a diode behaves essentially like a wire with a built-in voltage drop. If a bias voltage below the diode drop (and above the reverse breakdown voltage) is applied, an ideal diode behaves essentially like an open switch or an infinite resistance. However, in a real diode, a tiny **leakage current** flows, as indicated by the shallow slope of the $V - I$ curve above breakdown in the reverse-bias region of Figure 9. The standard silicon diodes you will encounter in lab have forward voltage drops of about 0.7 V, reverse breakdown voltages of 100-1000 V, and leakage currents on the order of 10^{-8} A.

4 Transistors

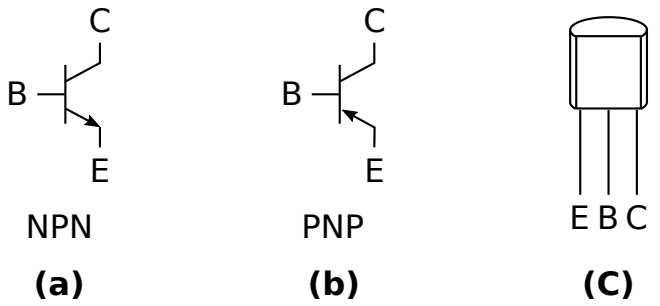

Figure 10: Schematic symbols for (a) NPN and (b) PNP bipolar junction transistors with labels on the collector (C), base (B), and emitter (E). (c) The plastic TO-92 transistor package we will use in lab with pins labeled.

A **transistor** is an **active device**, meaning that it enables the control of a current by an input signal. There are several different types of transistors, each suited to different applications. Here, we will focus on **bipolar junction transistors** (BJTs). Transistors have three terminals called the **emitter**, the **collector**, and the **base**. A BJT consists of two p-type – n-type junctions, like those in a diode. In an NPN transistor, the base is p-type semiconductor, and the emitter and collector are n-type. In a PNP transistor, the polarities are reversed.

Schematic symbols for BJTs and an illustration of the ordering of the pins on the transistors we will use in lab are shown in Figure 10. The arrows on the schematic symbols indicate the direction of the collector current I_C.

4.1 Transistor Behavior

Transistors operate in one of three states, which we will refer to here as "off", "on" (also "saturation"), and the "active region." In amplifiers, transistors operate in the active region. In digital and switching applications, transistors rapidly transition between "off" and "on" states. Transistors in voltage regulators stay in the the "on" state.

Active Region

The **Ebers-Moll equation** describes the relationship between the collector current I_C and the voltage drop from base to emitter V_{BE} by

$$I_C = I_o \left(e^{\frac{V_{BE}}{kT/e}} - 1 \right) \tag{31}$$

where I_o is the reverse leakage current from the emitter to the base, $e = 1.6 \times 10^{-19}$ C is the elementary unit of charge, $k = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, and T is the absolute temperature (in Kelvin). With typical doping levels, the leakage current arising from the "intrinsic" behavior of the pure semiconductor is very small, and the second term ($-I_o$) is negligible, giving a simple exponential dependence of I_C on V_{BE}.

This current-voltage relationship is the same as for the diode, plotted qualitatively in Figure 9. We usually operate diodes in **saturation**, at the forward voltage drop (≈ 0.7 V for silicon pn junctions). In some applications, like the transistor switch described in Section 4.2, we operate transistors in the same way. Below saturation in the **active region**, we need the Ebers-Moll equation to model transistor

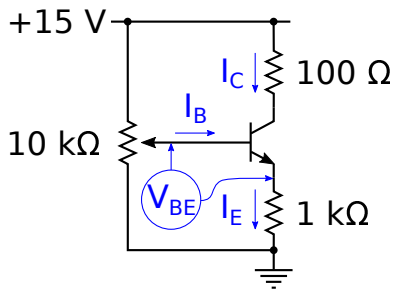

Figure 11: Schematic of the circuit you will use in lab to test the Ebers-Moll equation in the active region of an NPN BJT.

behavior. The schematic of the circuit you will use in lab to investigate the Ebers-Moll equation is shown in Figure 11. The variable resistor enables you to adjust V_{BE} from 0 V to saturation. The 100 Ω resistor gives you a way to determine the collector current I_C from a voltage measurement, and the 1 kΩ resistor keeps the collector and emitter currents under control to protect the transistor.

In the active region, the V_{BE} vs. I_C curve has a small, nonzero slope, which manifests itself as a small emitter resistance,

$$r_e = \frac{dV_{BE}}{dI_C} = \frac{kT/e}{I_C} \tag{32}$$

which at room temperature is $(25\ \Omega)/I_C[\text{mA}]$.

Transistor On (Saturation)

In a bipolar junction transistor, the diode drop across the collector-base junction is smaller than that of the base-emitter junction. This means that when a transistor is operating in **saturation**, the voltage drop from collector to emitter V_{CE} is smaller than V_{BE}. For a standard silicon transistor in saturation, $V_{CE} \approx 0.25$ V.

In saturation, the collector current I_C is greater than the current flowing from the base to the collector I_B by a factor h_{FE}, which is on the order of 100 and depends on temperature,

$$I_C = h_{FE} I_B \tag{33}$$

Transistor Off

When V_{BE} is significantly below 0.7 V, the exponential in Equation 31 is orders of magnitude smaller than its saturation value, and the collector and emitter currents I_C and I_E are effectively turned off.

For a given transistor, there are maximum rated values of I_C, I_B, and V_{CE}. If these values are exceeded, the transistor will fail. You might wonder, given the exponential relationship between V_{BE} and the collector current I_C of Equation 31, what keeps the current from growing beyond a safe level and destroying the transistor. When we operate a transistor in saturation, where the exponential really takes off, other devices in the circuit must limit the current, and we don't need to think about where we are on the exponential curve. The same is true for diodes.

Basic Transistor Behavior

- In order for a transistor to function, make $V_C > V_E$, and keep I_B, I_C, and V_{CE} below the rated maximum values of the transistor.
- **On:** In saturation, $V_{BE} \approx 0.7$ V, $V_{CE} \approx 0.25$ V, and $I_C = h_{FE} I_B$, where $h_{FE} \approx 100$.
- **Off:** If $V_{BE} < 0.7$ V (significantly), $I_C \approx 0$.
- **Active Region:** V_{BE} is between "off" and saturation. The collector current is governed by the Ebers-Moll equation (Equation 31). The emitter resistance at room temperature is $r_e = (25\ \Omega)/I_C[\text{mA}]$.

4.2 Application: Transistor Switch

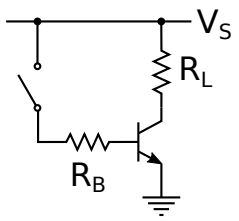

Figure 12: Schematic of a transistor switch circuit in which a small base current is used to deliver a larger current to a load.

The circuit shown in Figure 12 implements a transistor as a switch controlling power delivered to the load resistance R_L. Closing the mechanical switch drives a current from the base to the emitter. With a proper choice of R_B, the base current is large enough to saturate the transistor, bringing the base voltage to ≈ 0.7 V. The collector current produces a voltage drop across R_L of $\approx V_S$. The collector voltage is very close to the emitter (≈ 0.25 V), and the right branch of the circuit behaves as if the collector is grounded. Opening the switch brings V_{BE} significantly below 0.7 V, and the transistor shuts off power to the load.

What the point of this? Why not dispense with the transistor, and put the switch in series with the load, as is the case with household wiring? In applications in which the control switch is far away from a load that draws a large current, it is safer to run small control currents over long distances and keep the large currents close to the load.

Design

1. Set the supply voltage V_S to provide the current required by the load. The transistor will operate in saturation, so the collector-emitter voltage drop will be only ≈ 0.25 V, and the remainder of V_S will drive the load.
2. Choose a transistor rated to handle the required base current and power drawn by the load.
3. Set the value of R_B to keep the transistor in saturation while delivering the maximum desired current under all circumstances. Given possible variations in R_L and the range of h_{FE} among the

make/model of transistor used (see the data sheet from the manufacturer), it is generally good to use a generous base current ($\approx 10\ I_C/h_{fe}$).

As long as the supply voltage V_S is appropriate to the load, the load resistance will limit the current, so it does no harm to deliver a larger base current than is absolutely required, as long as it does not exceed the rated maximum base current.

4.3 Application: Emitter Follower

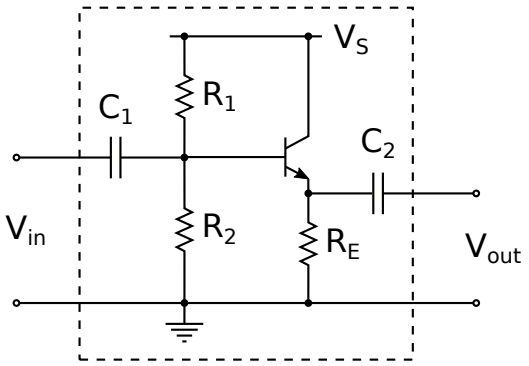

Figure 13: Schematic of an AC coupled emitter follower.

An **emitter follower** is a power amplifier. It has a voltage gain of $A_v \approx 1$ and a large current gain. It is useful in applications in which a load that draws high power is driven by a small signal — audio amplifiers, for example. The schematic of an AC coupled emitter follower is shown in Figure 13.

Design

1. The emitter voltage V_E is limited between ground and the source voltage V_S. Choose an emitter resistance R_E to center the quiescent[1] emitter voltage in this range, at the average current drawn by the load. Centering V_E allows the output signal vary in a symmetrical range.
2. Once V_E is established, set the values of the input bias resistors R_1 and R_2.
   (a) Their ratio R_1/R_2 must place V_{BE} in the active region of the transistor ($V_B \approx V_E + 0.6$ V).
   (b) Their parallel resistance must be small compared with that presented by the base-emitter junction so that they do not drag down the quiescent current $R_1||R_2 \approx h_{FE}R_E/10$.
3. The capacitors C_1 and C_2 are coupling capacitors that remove DC components from the input and output signals. They, along with the resistors in the input and output stages, act as high-pass filters. Their values are chosen such that they do not filter out frequencies of interest.

4.4 Application: Common Emitter Amplifier

A **common emitter amplifier** is an inverting voltage amplifier. The schematic of an AC coupled common emitter amplifier is shown in Figure 14. It has a voltage gain given by

$$A_v = -\frac{R_C}{R_E} \tag{34}$$

[1]The term **quiescent** refers to the state of the circuit when the input signal is not varying.

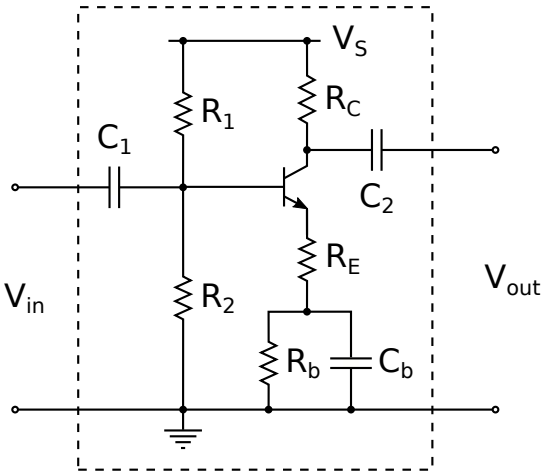

Figure 14: Schematic of an AC coupled common emitter amplifier.

Design

1. The collector resistor R_C is chosen to center the collector voltage between ground and V_S at the desired quiescent current.

2. The emitter resistor R_E is chosen to give the desired voltage gain (Equation 34).

   Keep in mind that the emitter resistance r_e in series with R_E acts to reduce the measured voltage gain relative to the prediction of Equation 34. The emitter resistance can be estimated using Equation 32 with the quiescent collector current.

3. The bias resistor R_b is set to place the quiescent emitter voltage at about 1 V.

   This greatly reduces the influence of the temperature-dependent (and very small) emitter resistance r_e on the stability of the quiescent base-emitter voltage V_{BE}, which must be kept in the active region of the transistor.

4. The bypass capacitor C_b is chosen to give very small capacitive reactance ($\approx \frac{R_b}{10}$ at the lowest signal frequency, thus shorting out the bias resistor so that only $R_E + r_e$ remain, yielding the desired voltage gain.

5. Once the emitter voltage V_E is established, set the values of the input bias resistors R_1 and R_2.

   (a) Their ratio R_1/R_2 must place V_{BE} in the active region of the transistor ($V_B \approx V_E + 0.6$ V).

   (b) Their parallel resistance must be small compared with that presented by the base-emitter junction so that they do not drag down the quiescent current $R_1||R_2 \approx h_{FE}(R_E + R_b)/10$.

6. The values of the coupling capacitors C_1 and C_2 are chosen so that they allow frequencies of interest to pass through. The input coupling capacitor C_1 and $R_1||R_2$ act as a high-pass filter on the input. Similarly, C_2 and $R_C||(R_E + R_b)$ act as a high-pass filter on the output.

5 Operational Amplifiers (Op Amps)

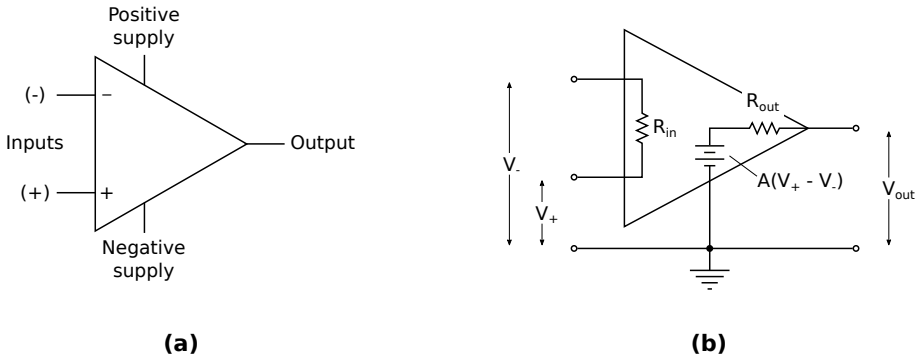

Figure 15: (a) Schematic symbol of an operational amplifier, and (b) a circuit model of an op amp.

We considered simple transistor amplifiers in Sections 4.3 and 4.4. Amplifier circuits with nice properties — high gain and high input impedance, for example — packaged as integrated circuits (ICs), are called **operational amplifiers** or op amps. They are called "operational" amplifiers, because they can be used to perform arithmetic operations like addition, subtraction, and multiplication with signals. In fact, op amps can also be used to integrate and differentiate signals.

The schematic symbol for an op amp is shown in panel (a) of Figure 15. A circuit model of an op amp is shown in panel (b) of Figure 15. The output voltage of the op amp is linearly proportional to the voltage difference between the inverting and non-inverting input terminals $V_+ - V_-$ by a factor of the gain A. However, the output voltage is limited to the range $-V_S \leq V_{out} \leq V_S$, where V_S is the supply voltage. The range $-V_S < V_{out} < V_S$ is often called the **linear region** of the amplifier, and when the output swings to V_S or $-V_S$, the op amp is said to be **saturated**. The output voltages of the transistor amplifiers described in Sections 4.3 and 4.4 are similarly limited by the supply voltage.

An ideal op amp has infinite gain ($A = \infty$), infinite input resistance ($R_{in} = \infty$), and zero output resistance ($R_{out} = 0$). You should use these assumptions to analyze op amp circuits. A consequence of the assumption of infinite gain is that, if the output voltage is within the finite linear region, we must have $V_+ = V_-$. A real op amp has a gain in the range 10^3-10^5, depending on the type, and hence actually maintains a very small difference in input terminal voltages when operating in its linear region. For most applications, we can get away with assuming $V_+ \approx V_-$. If the positive or negative input of an op amp is connected directly to ground, the other input will be held very close to ground and can be considered grounded in circuit analysis. This is referred to as a **virtual ground**.

Basic Op Amp Behavior

- $R_{in} = \infty,\ A = \infty,\ R_{out} = 0$
- **Linear region:** $V_+ = V_-,\ -V_S < V_{out} < V_S$
- **Saturation:** $V_+ > V_- \implies V_{out} = V_S$ or $V_+ < V_- \implies V_{out} = -V_S$

We stock two operational amplifiers in the lab, the `LM741`, a general purpose bipolar junction transistor (BJT) based amplifier with a typical input resistance of 2 MΩ, and the `LF411`, with field effect transistors

(FETs) at the inputs giving a much larger input resistance (10^{12} Ω). Data sheets for these devices are available on the Texas Instruments web site (`www.ti.com`). Of the two, the `LF411` comes closest to satisfying the assumptions associated with ideal op amp behavior. It costs more than the `LM741` ($1.84 vs. $0.94 as of fall 2021).

5.1 Application: Inverting Amplifier

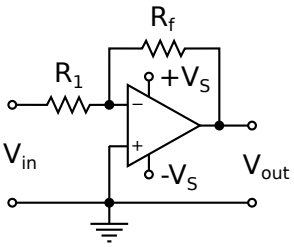

Figure 16: Schematic of an op amp based inverting amplifier.

In op amp based inverting amplifier is shown in Figure 16. The analysis of the behavior of the circuit is based on two very good approximations.

1. There is a virtual ground at the inputs of the op-amp.
2. The very large input impedance of the op amp means that it draws negligible current. Therefore, the current I flowing through the input resistor R_1 is the same as that flowing through the feedback resistor R_f.

It follows that

$$I = \frac{V_{in}}{R_1} = \frac{-V_{out}}{R_f} \tag{35}$$

which gives a voltage gain of

$$A_v = -\frac{R_f}{R_1} \tag{36}$$

The input resistor R_1 is connected directly to the virtual ground, so the input resistance of the circuit is R_1. The output resistance is $R_{oa}||R_f$, where R_{oa} is the very small output resistance of the op amp.

The inverting amplifier has the advantage of low noise due to the lower input impedance, relative to a non-inverting amplifier. It also has a relatively fast **slew rate***, the maximum rate of change of the signal.*

Design

1. The value of R_1 is chosen to give the desired input impedance.
2. The ratio R_f/R_1 is fixed by the desired voltage gain (Equation 36).

5.2 Application: Non-inverting Amplifier

An op amp based non-inverting amplifier is shown in Figure 17.

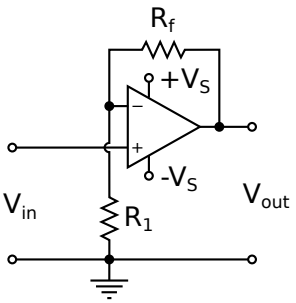

Figure 17: Schematic of an op amp based non-inverting amplifier.

The feedback loop of this amplifier is delivered by a voltage divider in which V_{out} is split by resistors R_f and R_1 and delivered to the negative input of the op amp, so that V_{in} and V_{out} are related by the voltage division expression

$$V_{in} = \frac{R_1}{R_1 + R_f} V_{out} \tag{37}$$

which gives a voltage gain of

$$A_v = 1 + \frac{R_f}{R_1} \tag{38}$$

The input is connected directly to the positive input of the op amp, so the input resistance of the circuit is that of the op amp. The output resistance is $R_{oa}||(R_1 + R_f)$, where R_{oa} is the very small output resistance of the op amp.

The non-inverting amplifier has the advantages of the op amp itself, large input impedance and small output impedance. It has the disadvantage that it is susceptible to positive feedback to the non-inverting input from via R_f which can lead to saturation.

Design

1. The ratio R_f/R_1 is fixed by the desired voltage gain (Equation 38).
2. The absolute values of R_f and R_1 are chosen to be large enough that the amplifier does not draw too much power and low enough that noise is not a problem. (The 10 kΩ - 500 kΩ range is reasonable.)

5.3 Application: Voltage Follower/Buffer

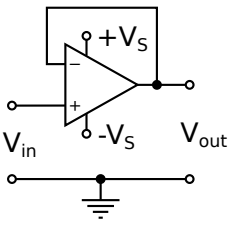

Figure 18: Schematic of an op amp based voltage follower/buffer.

The voltage follower or buffer, shown in Figure 18, is a special case of the non-inverting amplifier of Section 5.2 with $R_1 = \infty$ and $R_f = 0$, giving a voltage gain of $A_v = 1$. This is useful for mirroring signals from low-power sources at the output of the op amp, which has very small output impedance and can deliver higher power.

5.4 Application: Summing Amplifier

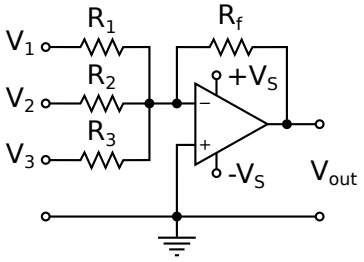

Figure 19: Schematic of an op amp based summing amplifier.

An op amp based summing amplifier is shown in Figure 19. The analysis of the circuit is very similar to that of the inverting amplifier in Section 5.1, with the additional complexity of multiple inputs. The virtual ground at the op-amp inputs gives simple expressions for the currents,

$$I_1 = \frac{V_1}{R_1} \tag{39}$$

$$I_2 = \frac{V_2}{R_2} \tag{40}$$

$$I_3 = \frac{V_3}{R_3} \tag{41}$$

$$I_f = \frac{V_{out}}{R_f} \tag{42}$$

which combine according to the junction rule at the inputs of the op amp

$$I_1 + I_2 + I_3 = I_f \tag{43}$$

Combining Eqs. 39 - 43 yields the output voltage

$$V_{out} = -\left(\frac{R_1}{R_f}V_1 + \frac{R_2}{R_f}V_2 + \frac{R_3}{R_f}V_3\right) \tag{44}$$

As we would expect based on the analysis of the inverting amplifier in Section 5.1, the input resistance "seen" by each input signal is that of the corresponding input resistor. The output resistance is $R_{oa}||R_f$, where R_{oa} is the very small output resistance of the op amp.

Design

- The ratios R_1/R_f, R_1/R_f, and R_1/R_f are determined by the desired coefficients of the output sum (Eq. 44).
- The absolute values of the resistors are chosen to give acceptable input resistances.

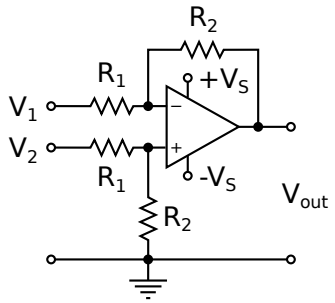

Figure 20: Schematic of an op amp based differential amplifier.

5.5 Application: Differential Amplifier

An op amp based differential amplifier is shown in Figure 20. The analysis of the circuit can be done using the junction rule for the virtual junction at the op-amp inputs

$$I_1 + I_2 = I_3 + I_4 \tag{45}$$

where the four unique currents carried by the resistors are

$$I_1 = \frac{V_1 - V_-}{R_1} \tag{46}$$

$$I_2 = \frac{V_2 - V_+}{R_1} \tag{47}$$

$$I_3 = \frac{V_- - V_{out}}{R_2} \tag{48}$$

$$I_4 = \frac{V_+}{R_2} \tag{49}$$

combined with the voltage division expression for the positive input,

$$V_+ = \frac{R_2}{R_1 + R_2} V_2 \tag{50}$$

Combining Eqs. 46 - 50 with the assumption the $V_- = V_+$ gives the output voltage

$$V_{out} = -\frac{R_2}{R_1}(V_1 - V_2) \tag{51}$$

Design

- The ratio R_1/R_2 is determined by the desired voltage gain.
- Matching the values of the two R_1 resistors and the two R_2 resistors is important to getting the gain right. Moreover, if V_1 and V_2 have a common DC component, mismatched resistors will introduce a DC component to the output.

5.6 Application: Differentiator

An op amp based differentiator is shown in Figure 21. The optional feedback capacitor $C_f < C$ is often needed to damp oscillations in the output. The following analysis ignores C_f.

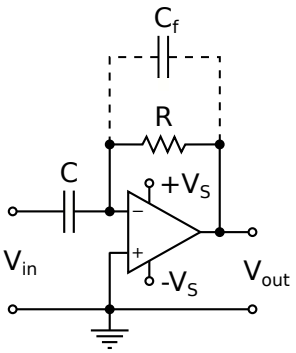

Figure 21: Schematic of an op amp based differentiator.

This circuit has a virtual ground at the op-amp inputs. It follows that

$$V_{out} = -IR \tag{52}$$

and also that the charge on the capacitor is related to the input voltage by

$$V_{in} = \frac{Q}{C} \tag{53}$$

The current I flowing through the resistor is to a good approximation equal to that of the capacitor, which we can relate to the charge on the capacitor via the definition of current

$$I \equiv \frac{dQ}{dt} \tag{54}$$

Combining Eqs. 52 - 54 yields

$$V_{out} = -RC\frac{dV_{in}}{dt} \tag{55}$$

Design

- The values of R and C are chosen to roughly match the desired time scale RC of the differentiation.
- If high-frequency oscillation is observed in the output, the feedback capacitor is needed. Its value is set to damp the oscillation without also damping the desired output.

5.7 Application: Integrator

An op amp based integrator circuit is shown in Figure 22. The optional feedback resistor R_f is needed to drain the feedback capacitor in order to prevent the saturation of the op amp. The feedback resistor is ignored in the following analysis.

This circuit has a virtual ground at the op-amp inputs. It follows that the current flowing through the input resistor is related to the input voltage by

$$I = \frac{V_{in}}{R} \tag{56}$$

and the charge on the capacitor is related to the output voltage by

$$V_{out} = -\frac{Q}{C} \tag{57}$$

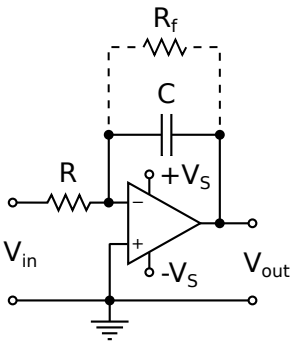

Figure 22: Schematic of an op amp based integrator.

Using the definition of current ($I \equiv dQ/dt$), Eq. 56 can be integrated to find the charge on the capacitor.

$$Q = \int dQ = \frac{1}{R} \int V_{in}\, dt + \text{constant} \tag{58}$$

Combining Eqs. 57 and 58 yields

$$V_{out} = -\frac{1}{RC} \int V_{in}\, dt + C \tag{59}$$

Design

- The values of R and C are chosen to give a time constant RC shorter than the period of the slowest signal to be integrated.
- The value of the feedback resistor R_f is chosen to discharge the capacitor on an acceptable time scale without distorting the output of the integrator.

A Reading Electronics Schematics

Schematic Symbols

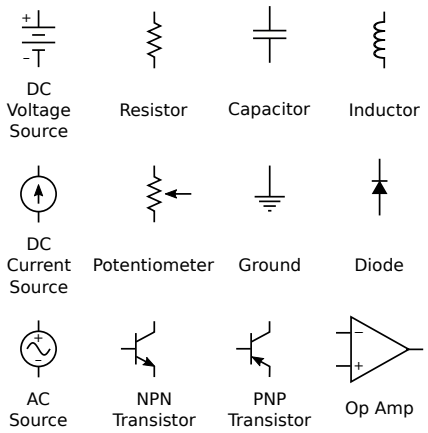

Figure 23: Schematic symbols.

The schematic symbols used in these notes are shown in Figure 23. An adjustable component, like the variable capacitor in a tuner circuit, is represented with the standard symbol with an arrow through it:

An Example

An electronics diagram or **schematic** is designed to communicate a specific way of connecting electronics components. Lines between components represent wires. Schematics usually have a rectangular layout, but this layout rarely represents how things are oriented in reality. Nothing is drawn to scale. Wires can follow curved three-dimensional paths. Components can be oriented differently than they appear. All that really matters is the way components are wires are connected. For example, a circuit schematic is shown in Figure 24(a), and one way a real version of the circuit might look is shown in Figure 24(b).

Junctions and Branches

It is useful to pay attention to points in a circuit where three or more wires meet in a circuit. These are called **junctions**. They are important in circuit analysis, because currents combine or divide at these points. They are marked with • symbols in the schematics in these notes. Junctions are connected by **branches**. A branch might contain multiple wires and components, but in carries a single current, because all of the components and wires in a branch are connected in series. In single-loop circuits, there are no junctions — a single current flows through all components. There are two junctions and three branches in the example circuit in Figure 24. It follows from the latter that there are three unique currents flowing in the circuit.

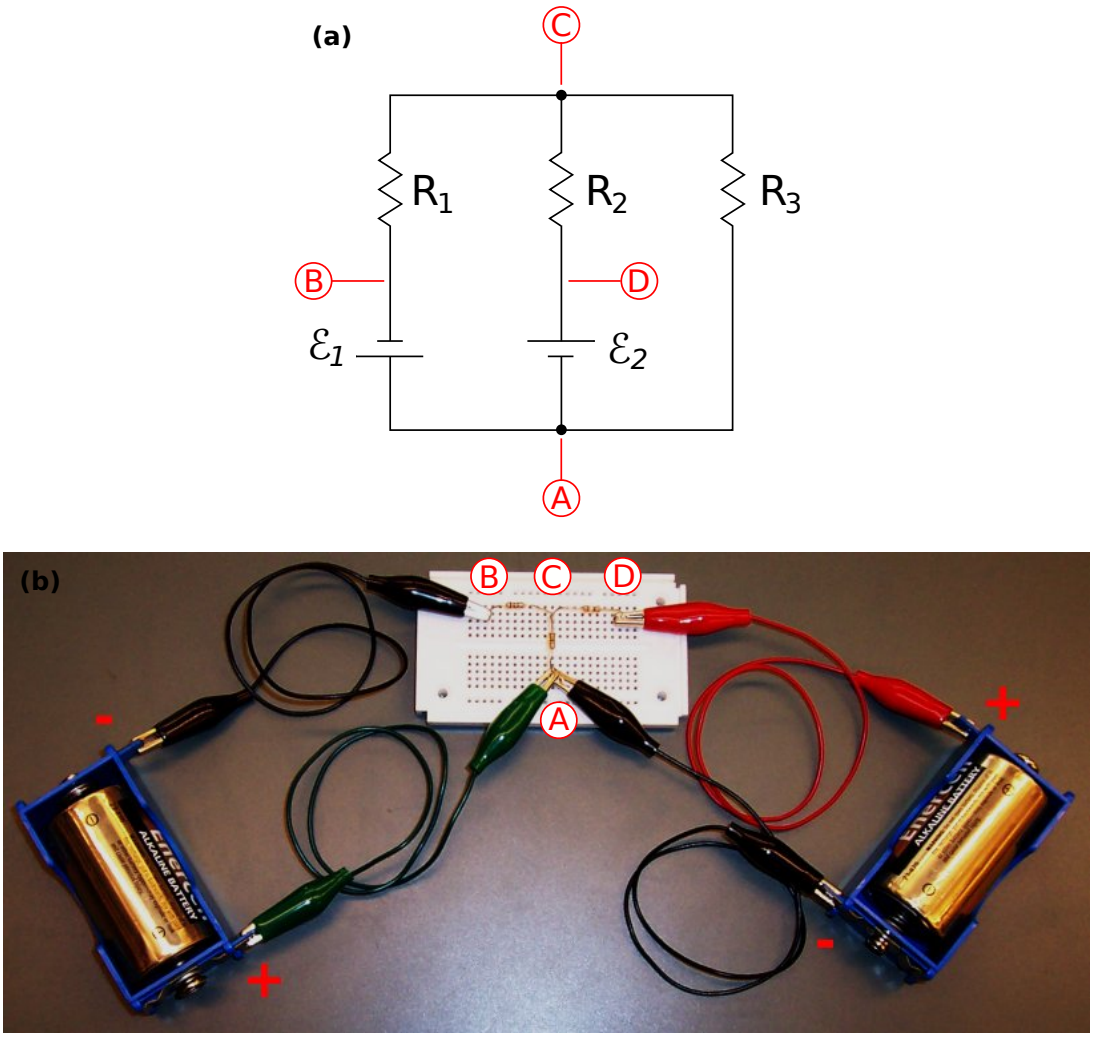

Figure 24: (a) Example of an electronics schematic. (b) One way the circuit might really look.

B The Breadboard

A **breadboard** allows for easy, temporary assembly and modification of a circuit by sliding components and wires into the various sockets. The sockets are linked in an easily recognizable pattern that allows for the components and wires to be connected in a circuit. This pattern is indicated by the shaded rectangles in Figure 25. The long distribution strips in the figure are meant for conveniently distributing power to components. These strips must be connected to power sources. They can also be used to distribute a connection to a common ground. The terminal strips are connected in groups of five. They are not connected across the channel. Integrated circuits (ICs) can be plugged in across the channel so that each pin is connected to a single terminal strip to allow for easy connections to other components.

C Resistor Color Codes

Most resistors you will encounter are marked with a set of bands, according to a standard color code, summarized in Figure 26, which you can use to determine their resistances. There are ten colors

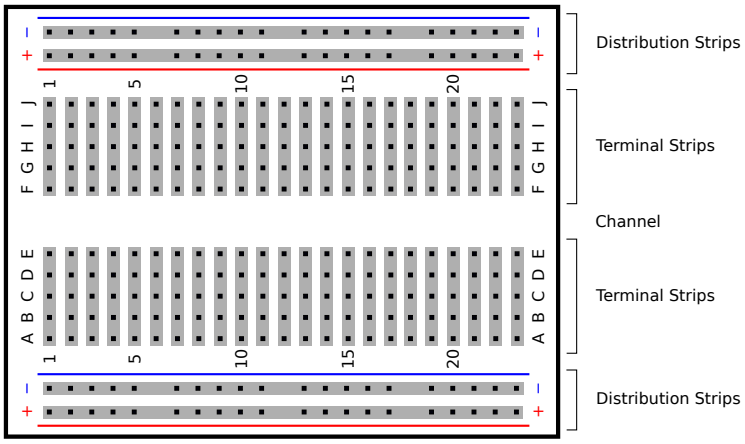

Figure 25: Schematic of a breadboard with shaded rectangles showing conducting connections between the sockets.

color	black	brown	red	orange	yellow	green	blue	violet	gray	white
digit	0	1	2	3	4	5	6	7	8	9
multiplier	1	10	100	1k	10k	100k	1M	10M	100M	1000M

$$R = [\text{band1}][\text{band2}] \times 10^{[\text{band3}]} \quad \begin{matrix} \pm & 5\% \text{ (gold)} \\ \pm & 10\% \text{ (silver)} \end{matrix}$$

Figure 26: Guide to resistor color codes.

corresponding to numerical digits 0-9 (See the table below.), and gold and silver bands indicating 5% and 10% accuracy in the coded resistance, respectively. Starting at the far end of the resistor from the gold/silver band, the first two bands are the first two digits in the resistance. The third band gives the power of ten by which you multiply the first two digits to obtain the resistance. For example, Blue Yellow Red Gold gives $R = 64 \times 10^2\ \Omega = 64 \times 100\ \Omega = 6400\ \Omega$ with a tolerance of 5%, or $\pm 320\ \Omega$.

D Digital Multimeter (DMM) Guide

D.1 Measuring Potential Difference (Voltage Drop)

- Plug the probes into the `COM` and `V Ω` ports on the DMM.
- Switch the DMM to one of the voltage scales.
- Connect the DMM in parallel with the resistor as shown in panel (a) of Figure 27, and it will display the measured potential difference.
- Find the voltage scale that gives you the most precise reading — the one with the upper bound larger than, but closest to, the measured potential difference.

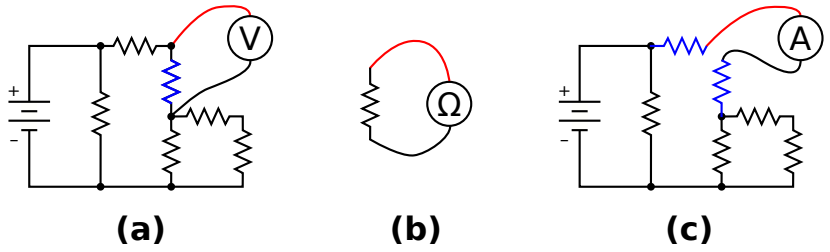

Figure 27: Schematics illustrating how a multimeter is connected to measure (a) the voltage drop across the resistor highlighted in blue, (b) the resistance of a resistor, and (c) the current flowing through the branch of the circuit highlighted in blue.

D.2 Measuring Resistance

The resistor must not be connected to a circuit while you are measuring its resistance.

- Plug the probes into the `COM` and `V Ω` ports on the DMM.
- Switch the DMM to one of the resistance scales.
- Connect the DMM leads to the leads of the resistor as illustrated in panel (b) of Figure 27, and it will display the measured resistance.
- Find the resistance scale that gives you the most precise reading — the one with the upper bound larger than, but closest to, the measured resistance.

D.3 Measuring Current

Never connect the DMM in parallel with anything while measuring current. In current-measuring mode, the resistance of the DMM is very small, and it acts as a wire. Connecting the DMM in parallel with a component will short it out, possibly drawing enough current to blow a fuse in the DMM.

- Plug the probes into the `COM` and current ports of the DMM. There are two current ports (usually labeled `A` and `mA` with their maximum current ratings). Choose the one appropriate to the current you plan to measure. When in doubt, use the high current port, and switch to the more sensitive one if you determine that the current is low enough.
- Switch the DMM to one of the current scales corresponding to the current port you are using.
- Connect the DMM in series with the branch of the circuit through which you want to measure the current as illustrated in panel (c) of Figure 27.
- Find the current scale that gives you the most precise reading — the one with the upper bound larger than, but closest to, the measured current.

E Decibels

It is convenient, when comparing two quantities, call them $Thing_1$ and $Thing_2$, that differ by several orders of magnitude, to use a logarithmic scale for the comparison. One such approach is the **decibel**

scale.

$$dB = 10 \log \left(\frac{\text{Thing}_2}{\text{Thing}_1} \right) \tag{60}$$

For example, if Thing_2 is 10^8 times larger than Thing_1, we can say Thing_2 is 80 dB above Thing_1. Where Thing_2 is the intensity of sound in an environment, and Thing_1 is the threshold of human hearing (10^{-12} W/m^2), this is called the **sound level**.

In the electronics context, we use decibels to compare signal amplitude and power. Often, the **3 dB point** is used to characterize electronic filters. That is the frequency at which the power transmitted by the filter is reduced by a factor 2 relative to the incident power

$$10 \log \left(\frac{P_{out}}{P_{in}} \right) = 10 \log \left(\frac{1}{2} \right) = 10(-0.3010) = -3.01$$

The power is proportional to the square of the voltage, so the 3 dB point is the frequency (or frequencies) at which the voltage gain $A_v = |V_{out}|/|V_{in}|$ is $1/\sqrt{2}$. Some circuits have a maximum voltage gain that is different than 1. In these cases, the 3 dB points are the frequencies at which $|A_v|/|A_{v_{max}}|$ is $1/\sqrt{2}$.