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ECE 542

HW #4

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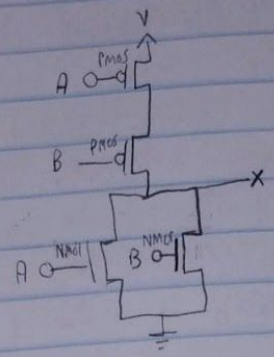
① Draw the schematic for a 2-input Nor gate, Using 2 NMOS & 2 PMOS transistors. This schematic Sim to fig 5.4

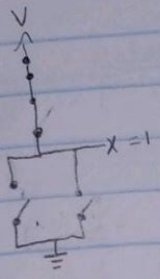
NMOS 1 flows, 0 stops

PMOS 0 flows, 1 stops

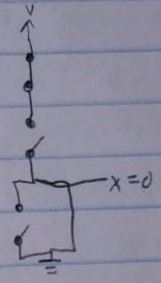
A	B	X
0	0	1
0	1	0
1	0	0
1	1	0



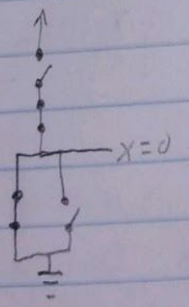
Case: A=0=B



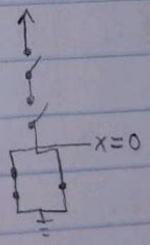
Case: A=0, B=1



Case: A=1, B=0



Case: A=1, B=1



(a) A Silicon with substrate $N_A = 10^{17}\,cm^{-3}$ is biased in such a way that it is in depletion. The depletion region width is 0.1 Nm.

a) What is the volume charge density in depletion region, C/cm^3?

$$\rho = -q N_A^- = -1.6 \cdot 10^{-19} C (10^{17}\,cm^{-3}) = \boxed{-0.016\ C/cm^3}$$

(b) By integrating volume charge density, what is the surface charge density in C/cm^2?

$$Q = SP = -0.016 X = (-0.016\ \tfrac{C}{cm^3})(0.0001\,cm) \quad (X = 0.1 \cdot 10^{-4})$$

$$= \boxed{-1.6 \cdot 10^{-7}\ \tfrac{C}{cm^2}}$$

(c) if the E-field drops to 0 at depth of 0.1 Nm, what is the electric field at Silicon surface?

$$(0.1 \cdot 10^{-6})\,m \left(\frac{10^2\,cm}{m}\right) = 0.1 \cdot 10^{-4}\,cm$$

$$\mathcal{E}(x) = \int_0^{0.1\cdot10^{-4}} \frac{\rho(x)}{\varepsilon_r \varepsilon_0}\,dE = \int_0^{0.1\cdot10^{-4}} \frac{-0.016\ C/cm^3}{(8.85\cdot10^{-12}\,\frac{F}{m})(11.7)(\frac{1m}{10^2cm})} = \boxed{154,522.2\ \tfrac{V}{cm}}$$

$\varepsilon_{r_{silicon}} = 11.7$

$$= \frac{-0.016\ C/cm^3\,(0.1\cdot10^{-4})}{(8.85\cdot10^{-12}\,\frac{F}{m})(\frac{1m}{10^2cm})(11.7)} \quad \int^{\uparrow} \text{ because from 0}$$

(d) There is an SiO_2 layer on top of Silicon. What is the E-field within the SiO_2 layer? Note: you have to consider boundary between Si & SiO_2.

$\varepsilon_{r_{SiO_2}} = 3.9$

$$\varepsilon_1 E_1 = \varepsilon_2 E_2 \Rightarrow E_2 = \frac{\varepsilon_1 E_1}{\varepsilon_2} = \frac{11.7}{3.9}\left(154,522.2\ \tfrac{V}{cm}\right) = \boxed{463,566.6\ \tfrac{V}{cm}}$$

(e) A good quality layer of SiO_2 can support an E-field of 1.5 V/nm before breakdown occurs. Does breakdown occur in SiO_2 for this device?

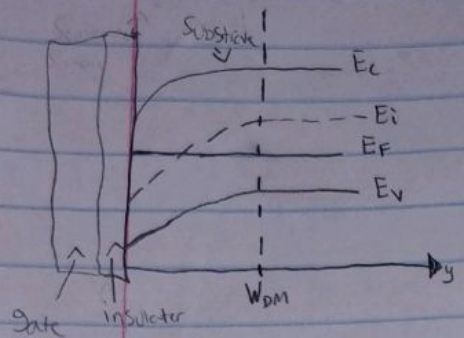
$$1.5\ \tfrac{V}{nm} > \left(463,566.6\ \tfrac{V}{cm}\right)\left(\frac{10^2\,cm}{m}\right)\left(\frac{1m}{10^9\,nm}\right)$$

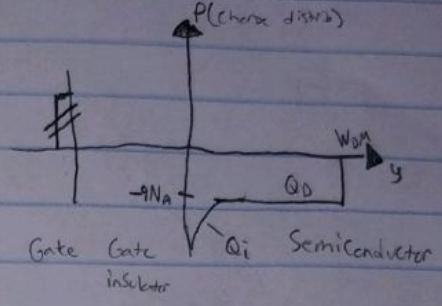
$$= 0.046356665\ \tfrac{V}{nm}$$

$\therefore$ there is **no** breakdown

(3) Make 2 graphs for NMOS Strong inversion. (a) Draw energy band diagram, (b) draw Charge distribution vs distance

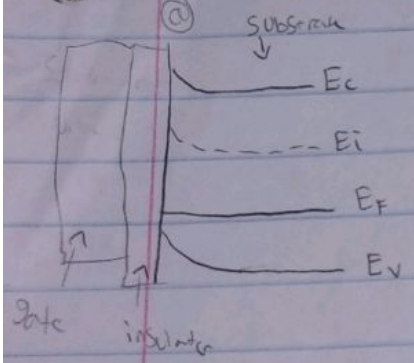
(a) NMOS Strong Inversion (Energy Band) (b) Charge distribution VS. distance





(4) Make 2 graphs NMOS Accumulation. (a) Draw energy band (b) draw Charge distribution VS. distance.

(a)



(b)