Counter Chip

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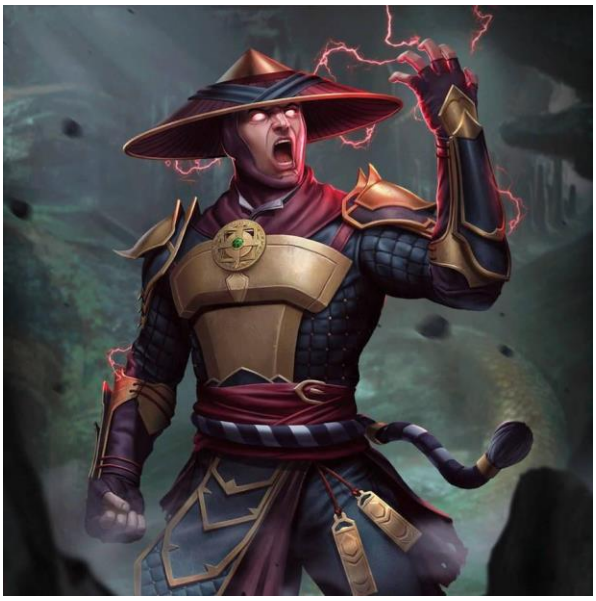

Abstract:

This documentation provides a comprehensive guide for the Counter VHDL Project, which implements a counter chip with a maximum value of 63 using a finite state design model. The counter responds to signals such as X (increment), Y (decrement), reset (reset to 0), and max_occupancy (set the maximum count value). The document aims to offer users a clear understanding of the project, its functionality, and integration guidelines.

Introduction:

The Counter VHDL Project introduces a versatile counter chip designed with a finite state design model, ensuring efficient and reliable operation. The primary signals that control the counter include X for incrementing, Y for decrementing, reset for resetting to zero, and max_occupancy for defining the maximum count value.

In this document, you will find detailed information on the project files, usage instructions, and an example integration guide. Whether you are simulating the project using a VHDL simulator or integrating it into a larger VHDL project, this documentation will guide you through the necessary steps.

Description:

Signal Behavior:

Result: Synchronized with the data stored in the register.

X: Adds one to the count on the rising edge.

Y: Removes one from the count on the rising edge.

reset: Resets the count to 0.

Z: Set to 1 when the count reaches its maximum value (63).

max_occupancy: Sets the maximum number that the counter can reach.

The counter operates in three distinct states:

1-init:

1.1-Triggered by the reset signal.

1.2-Sets the counter register to zero and the maximum occupancy register to the received signal value.

2-idle:

2.1-Normal state of the machine.

2.2-Waits for incoming signals to initiate a change.

3-Change:

3.1-Triggered when X or Y is turned on.

3.2-Activated if either X or Y is on (not both) and if the count has not reached the maximum

3.3-Functions as a signed adder, incrementing or decrementing based on the activating signal.

Using the Counter:

To initiate its operation, activate the reset signal initially and ensure the receipt of the max_occupancy signal. Subsequently, deactivate the reset signal, and the counter will be ready for use.

Schematics & Simulations:

The Schematics and a sample simulation are provided in Separate files. Furthermore, A testbench is also provided for testing.