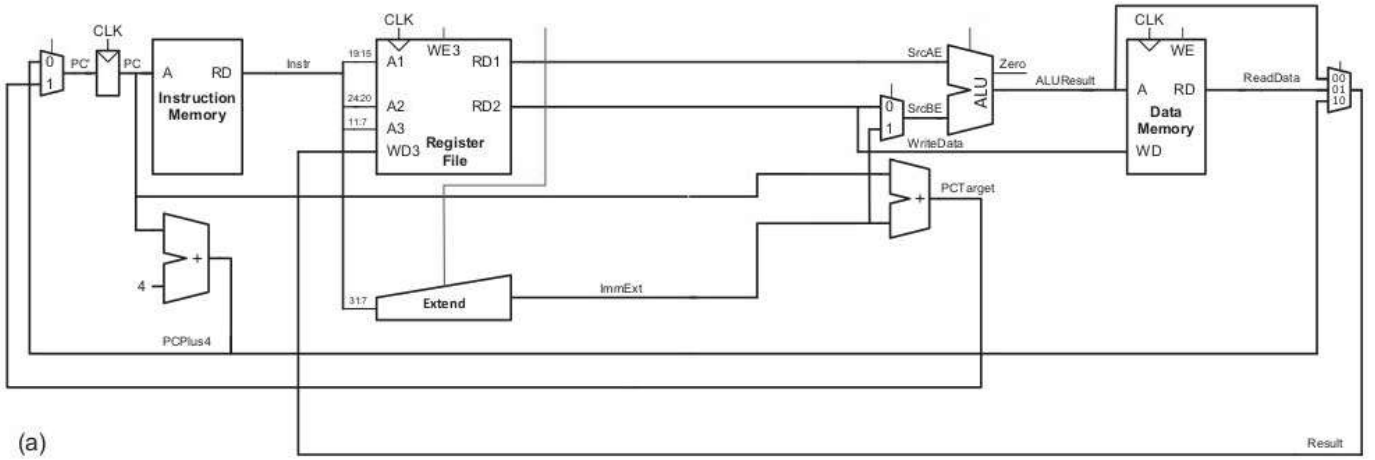
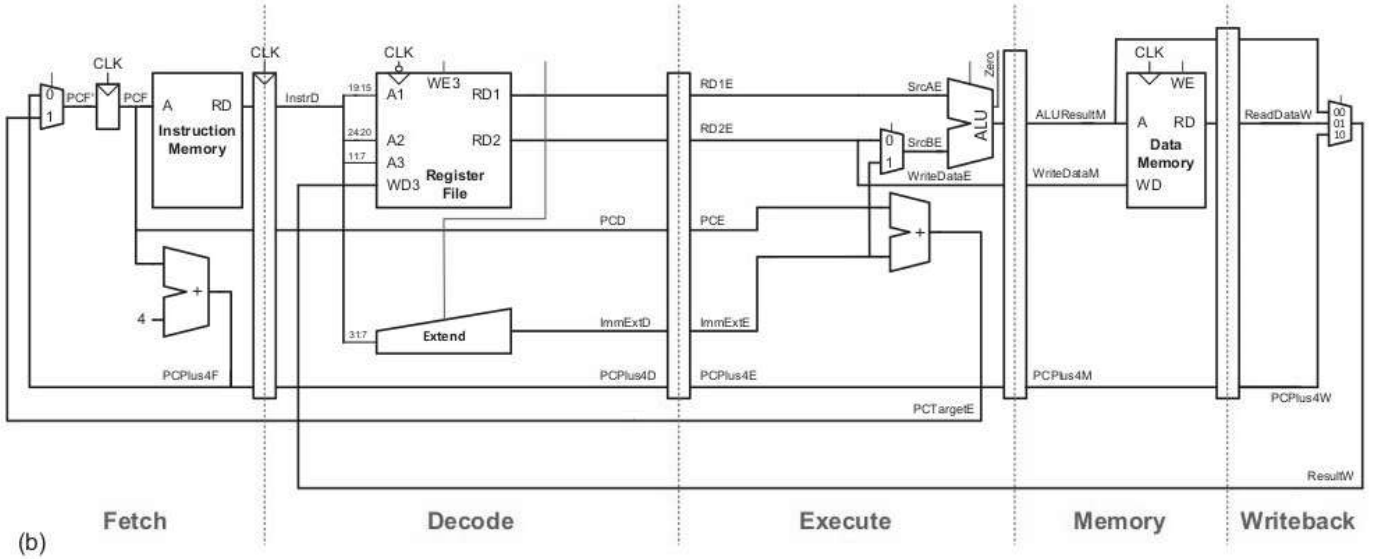
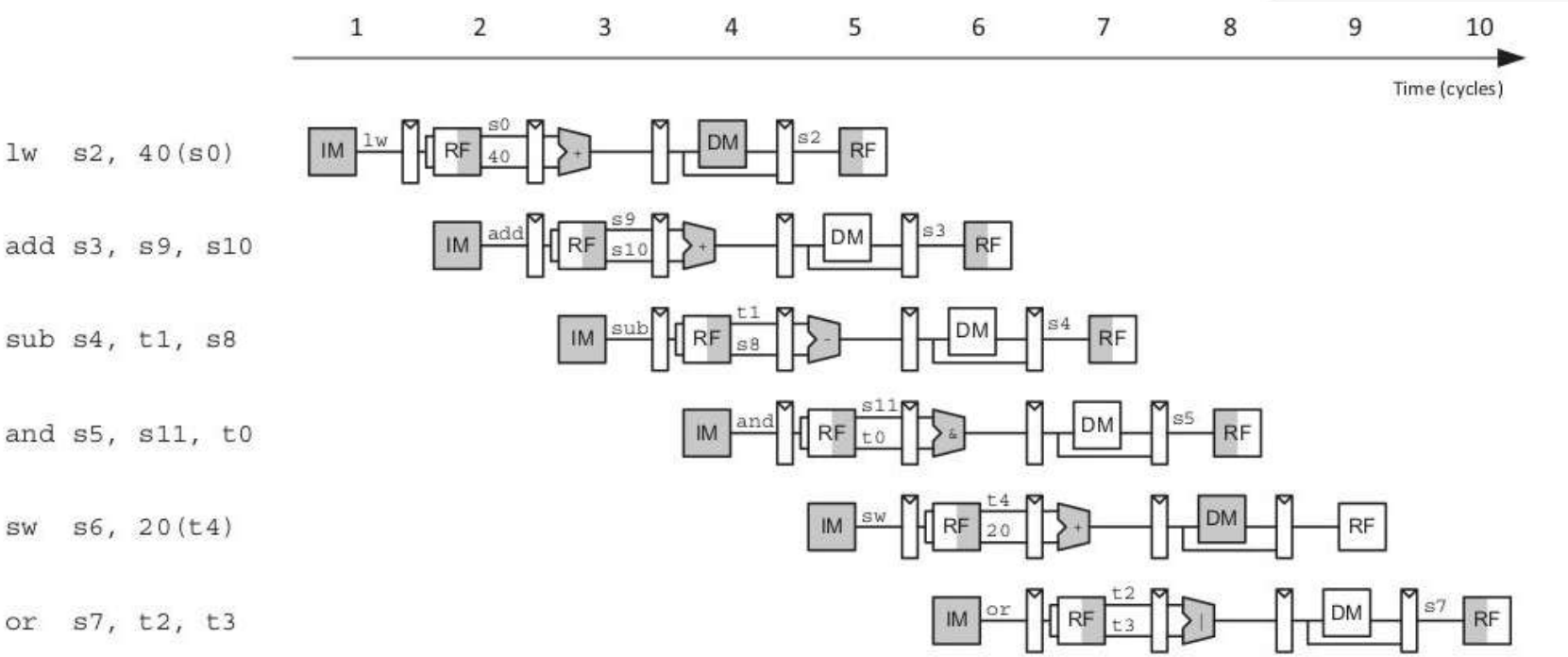
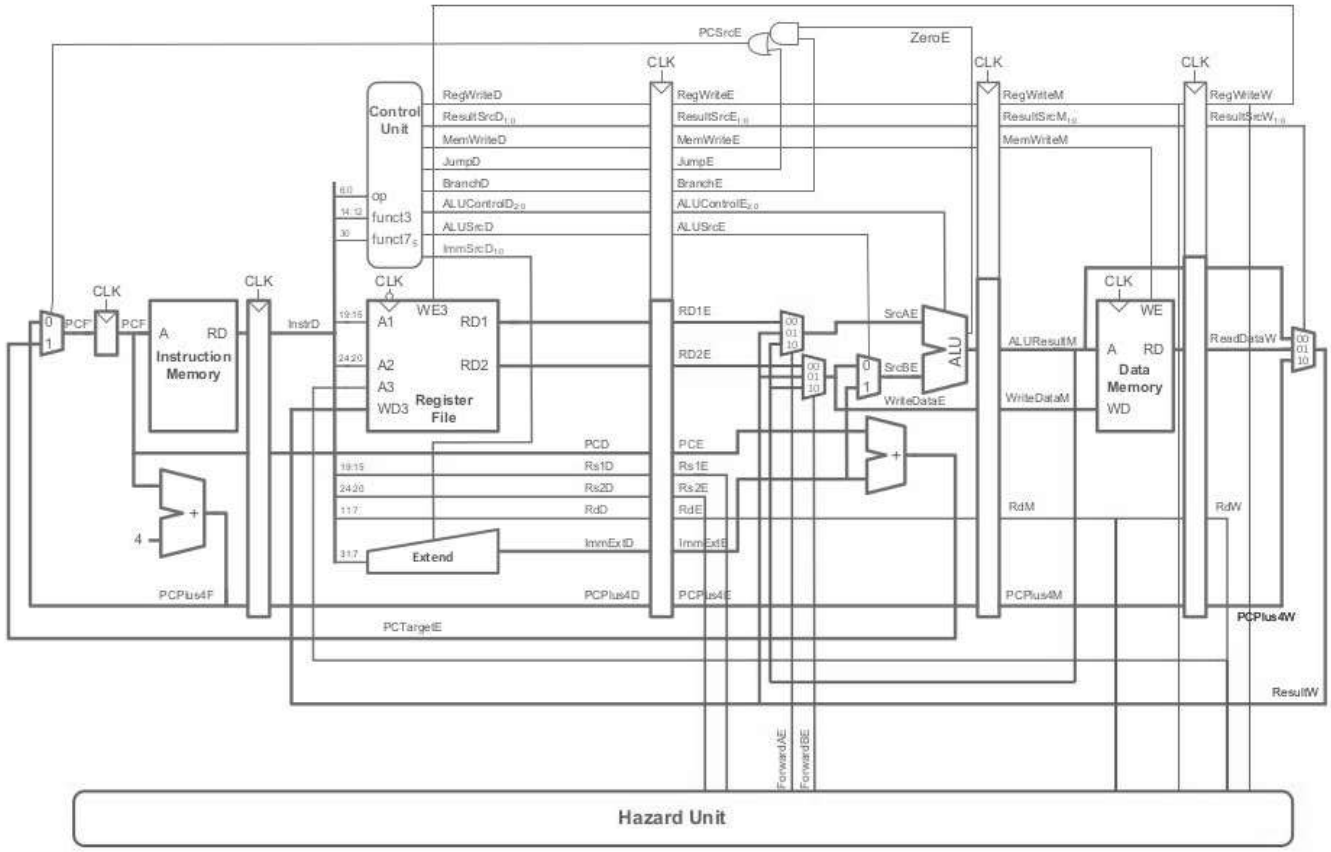
Pipelining


CLK
PC'
PC
A
RD
Instruction Memory
Instr
19:15
24:20
11:7
A1
A2
A3
WD3
WE3
RD1
RD2
Register File
SrcAE
SrcBE
ALU
Zero
ALUResult
WriteData
WE
Data Memory
WD
ReadData
PCTarget
4
PCPlus4
31:7
Extend
ImmExt
Result
(a)


CLK
PCF'
PCF
InstrD
RD1E
RD2E
PCD
PCE
ImmExtD
ImmExtE
PCPlus4F
PCPlus4D
PCPlus4E
PCTargetE
ALUResultM
WriteDataM
WriteDataE
ReadDataW
PCPlus4M
PCPlus4W
ResultW
Fetch
Decode
Execute
Memory
Writeback
(b)

Abstract View of Pipelining



Updated Pipeline Top Architecture