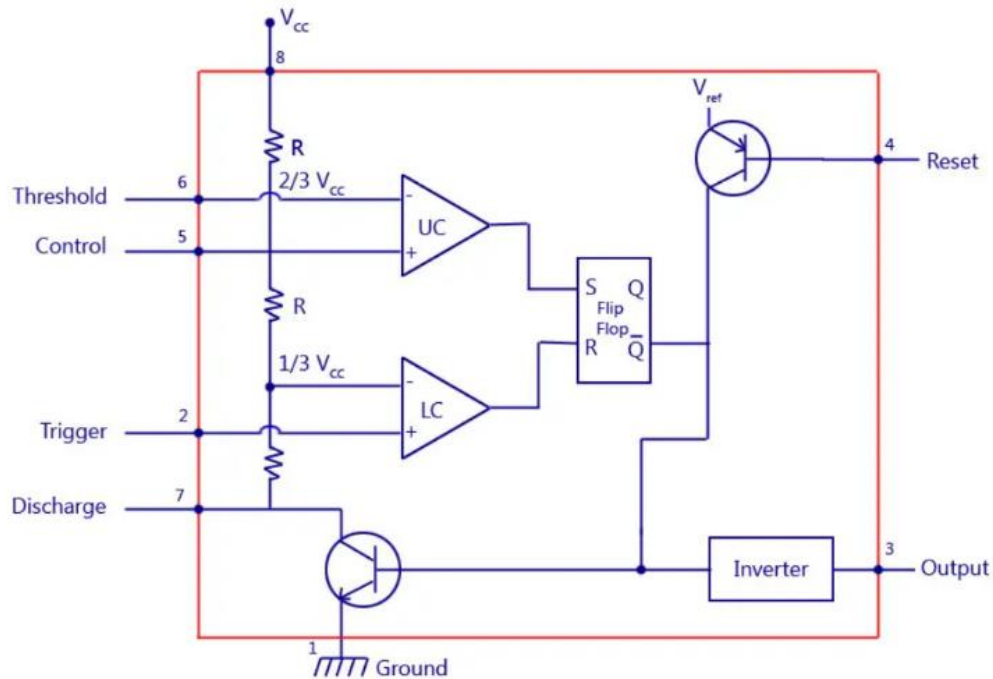


## Task-1 (Part-A)

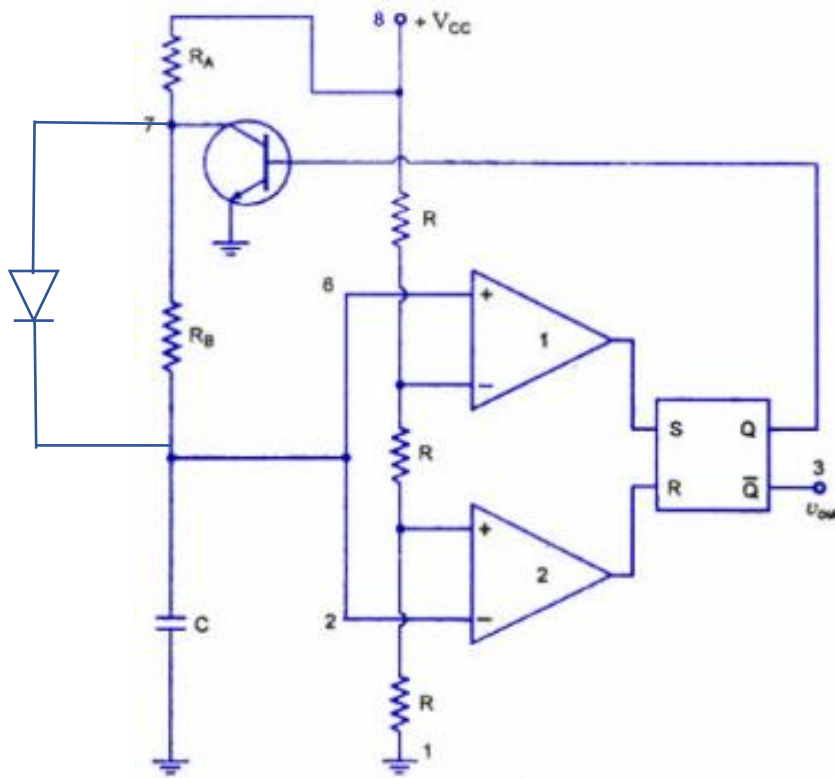
### Designing a Signal Generator with a 555 Timer

555 IC Timer Block Diagram



Given is the internal circuit diagram of the 555-timer IC. It is a 8-pin IC with the pin names given in the diagram. The 3 internal resistor values are 5kohm each. It also includes 2 comparators and 1 SR-flipflop as shown.

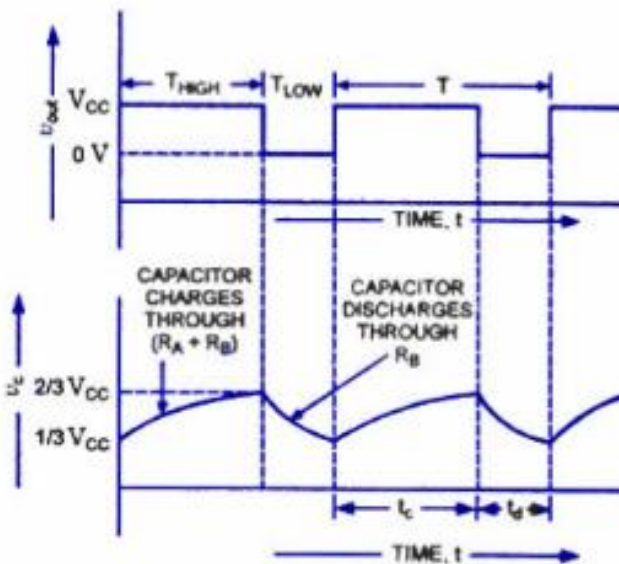
## Astable Mode of operation:-



**Without** the diode in parallel with  $R_B$ , the 555-timer IC circuit is governed by the equations:-

- Time High (Seconds)  $T_1 = 0.693 * (R_A + R_B) * C$
- Time Low (Seconds)  $T_2 = 0.693 * R_B * C$
- Time Period  $T = \text{Time High} + \text{Time Low} = 0.693 * (R_A + 2 * R_B) * C$
- Frequency  $f = 1/\text{Time Period} = 1/0.693 * (R_A + 2 * R_B) * C = 1.44 / (R_A + 2 * R_B) * C$
- Duty Cycle (the ratio of time for which the output is HIGH to the total time in %)=

$$(\text{Time HIGH} / \text{Total time}) * 100 = (T_1 / T) * 100 = (R_A + R_B) / (R_A + 2 * R_B) * 100$$



*Capacitor and Output Voltage Waveforms*

When we do not use the diode, the duty cycle of our operation will always be limited to greater than 50%. But to generate sine wave from the above circuit, we need to generate a square wave with 50% duty cycle at the output. So for that purpose, we have connected a diode in parallel with  $R_B$ .

Due to this, while the capacitor is charging, the current through  $V_{cc}$  will follow a low resistance path through the diode rather than  $R_B$ . So the equations changes to:

- Time High (Seconds)  $T_1 = 0.693 * R_A * C$
- Time Low (Seconds)  $T_2 = 0.693 * R_B * C$
- Time Period  $T = \text{Time High} + \text{Time Low} = 0.693 * (R_A + R_B) * C$
- Frequency  $f = 1/\text{Time Period} = 1 / 0.693 * (R_A + R_B) * C = 1.44 / (R_A + R_B) * C$
- Duty Cycle (the ratio of time for which the output is HIGH to the total time in %)=

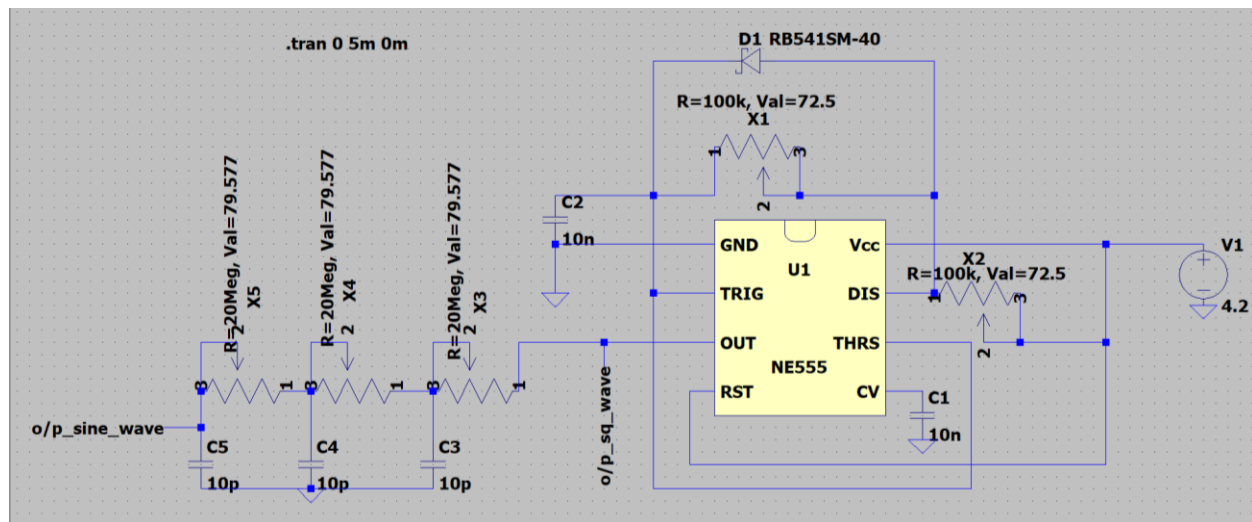
$$(\text{Time HIGH} / \text{Total time}) * 100 = (T_1 / T) * 100 = R_A / (R_A + R_B) * 100$$

By appropriate calculations, for 50% duty cycle, we get the relation:  $R_A = R_B = R$  (say)

So the frequency can be calculated as:  $f = 0.72 / (R * C)$

To generate sine wave from the square wave, we have connected a 3-stage RC-filter at the output pin.

The schematic of the circuit I've made is given below:-



The frequency of operation is related to the RC-filter as its cutoff frequency:-

$$f = 1 / (2 * \pi * R * C)$$

The capacitor values are set to **10nF** for both connected to 555-timer circuit. For the filter capacitors, we have chosen the value to be **10pF**.

And we have chosen **100kohm** potentiometers for  $R_A$  and  $R_B$ , and **20Mohm** potentiometers for the resistances of filter.

### **Certain Observations and explanation:-**

The capacitor value of the one connected directly to 555 timer is kept low (10nF), so that at higher frequencies, the resistance value(  $R_B$  ) does not fall so much that the leakage current through it becomes significant while charging of the capacitor. But keeping it further low increases the duty cycle.

For RC filters, higher resistor values generally result in lower current flow and increased signal attenuation. This can be advantageous in certain situations, such as when we want to achieve a steeper roll-off (greater attenuation of unwanted frequencies) or when dealing with high-frequency signals that require higher impedance. Higher resistor values can also help reduce the loading effect on the source signal.

So the resistor values of the RC filter are kept much high so that the square wave does not get deformed at higher frequencies.

**At very high frequencies the corners of the square wave becomes somewhat rounded and the duty cycle also decreases.** At higher frequencies, the time constant of the RC network becomes smaller, and the capacitor has less time to fully charge or discharge. This can cause the edges of the square wave to become less steep and rounded, resulting in waveform distortion. The rise and fall time of the output signal, which is the time it takes for the signal to transition between high and low levels, also plays a role. At higher frequencies, the rise and fall times can become longer, resulting in distorted edges of the square wave.

We have designed the circuit to operate in the frequency range of 1khz to 200Khz.

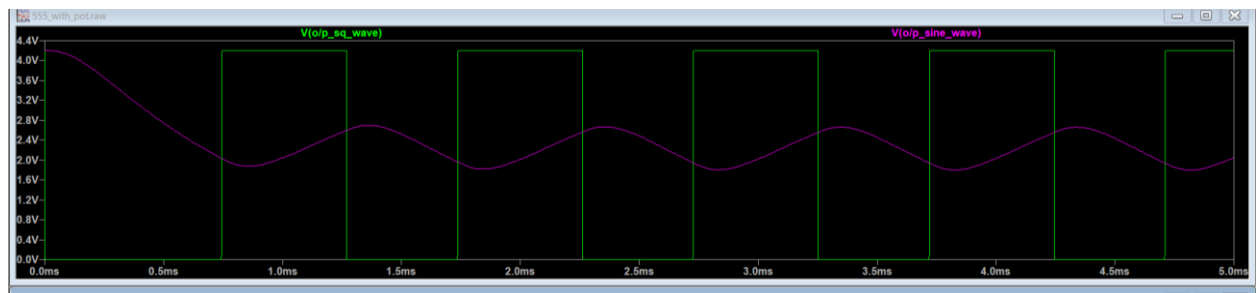
$$R_A=R_B=(x_1/100)*100\text{kohm}$$

$$\text{For the filter, } R_f=(x_2/100)*20\text{Mohm} \quad (x_1, x_2 \text{ given in percentage})$$

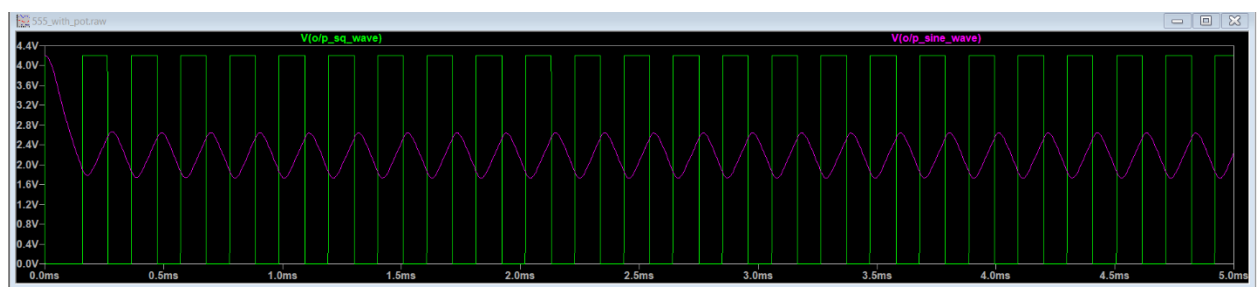
$R_A=R_B$ (ohm)	$x_1$ (%)	$R_f$ (ohm)	$x_2$ (%)	Frequency (khz)	Vpp of sine wave(V)
72.5k	72.5	15.91M	79.577	1	0.88
14.5k	14.5	3.183M	15.915	4.83	0.91
7.25k	7.25	1.592M	7.957	9.52	0.91
1.45k	1.45	318.3k	1.591	46.27	0.97
725	0.725	159k	0.795	90.04	1.02
362.5	0.362	79.5k	0.397	172.5	1.07

The waveforms we got are shown below:-

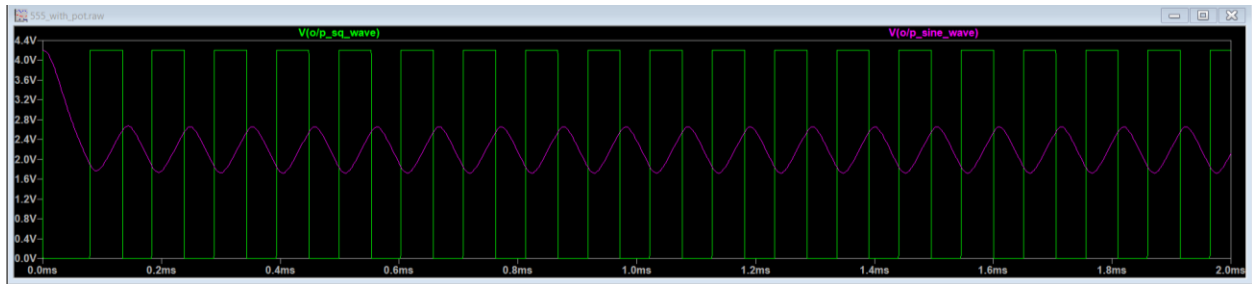
1)f=1Khz (0-5 ms)



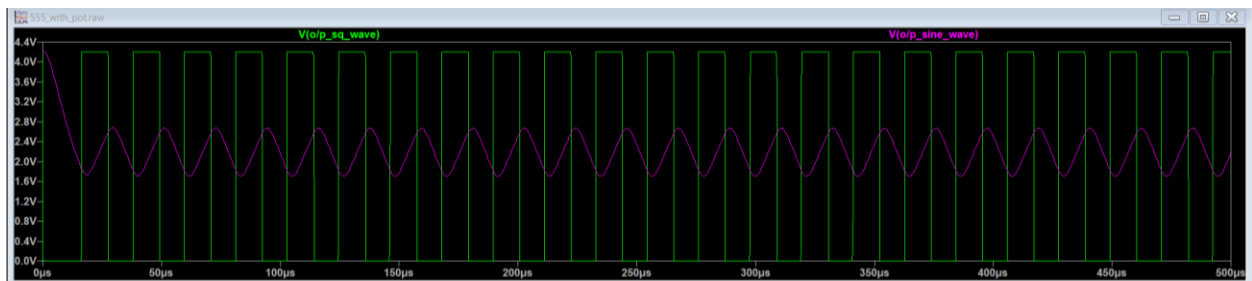
2)f=4.83khz (0-5 ms)



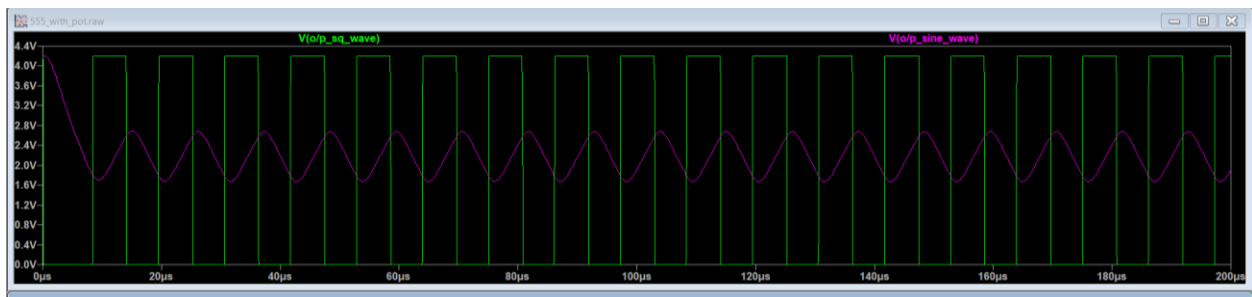
3)  $f=9.52\text{kHz}$  (0-2ms)



4)  $f=46.27\text{kHz}$  (0-500 µs)



5)  $f=90.04\text{kHz}$  (0-200 µs)



6)  $f=172.5\text{kHz}$  (0-200µs)

