LFU Cache Simulation Table

Step	Memory Access	Hit / Miss	Action Taken	Cache Status (with frequency)
1	A	Miss	Cache empty → Insert A	[A(1)]
2	B	Miss	Insert B	[A(1), B(1)]
3	C	Miss	Insert C	[A(1), B(1), C(1)]
4	A	**Hit**	Increase frequency of A	[A(2), B(1), C(1)]
5	B	**Hit**	Increase frequency of B	[A(2), B(2), C(1)]
6	C	**Hit**	Increase frequency of C	[A(2), B(2), C(2)]
7	D	Miss	Cache full → All freq=2 → Remove oldest (A), Insert D	[B(2), C(2), D(1)]
8	A	Miss	LFU = D(1) → Remove D, Insert A	[B(2), C(2), A(1)]
9	B	**Hit**	Increase frequency of B	[B(3), C(2), A(1)]

OUTPUT OF THE PROGRAM: -

```
LFU Cache Simulation
Final Cache Content:
B (Frequency: 3)
C (Frequency: 2)
A (Frequency: 1)
```