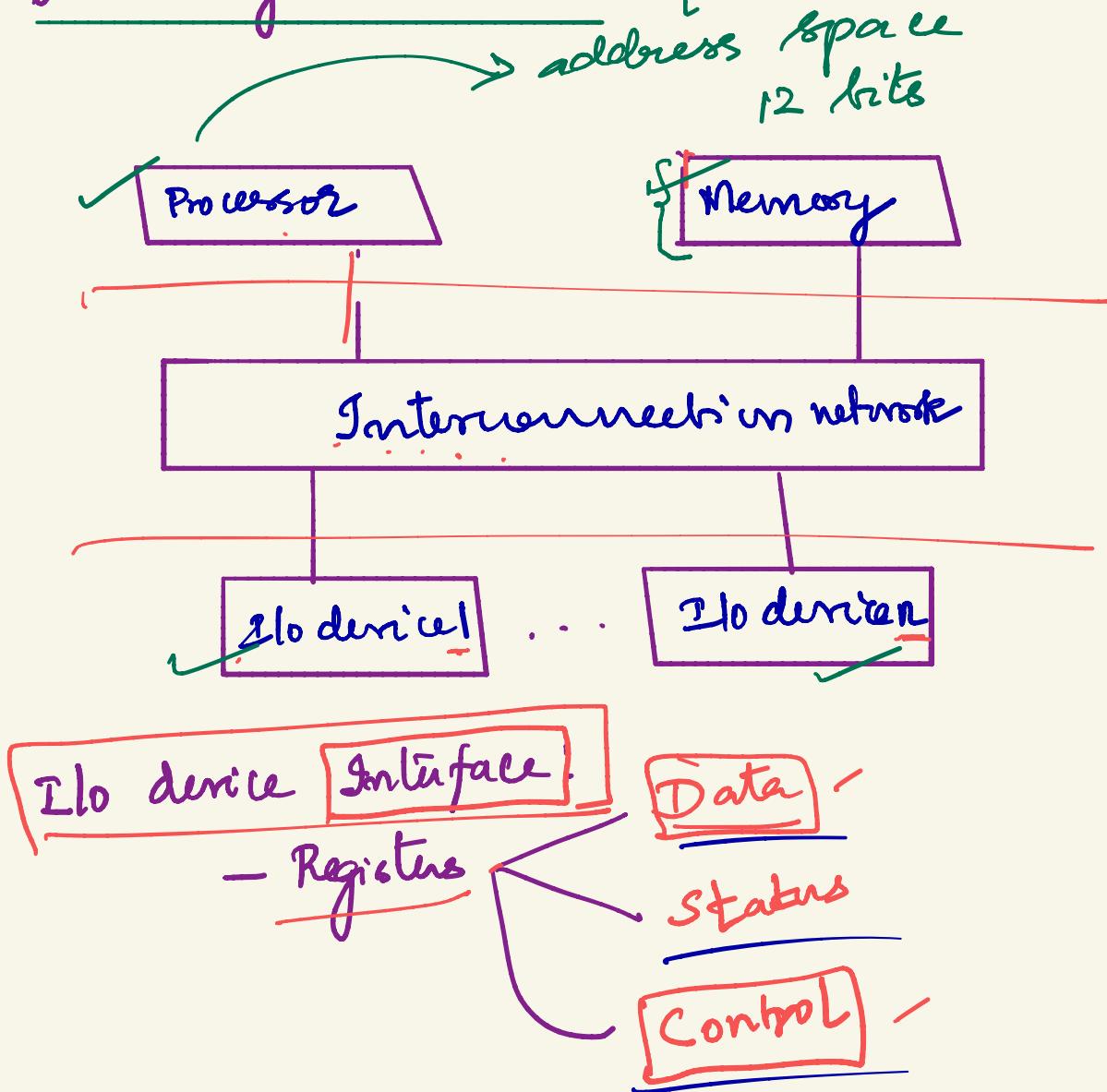



Accessing I/O Devices. { Module 5 }



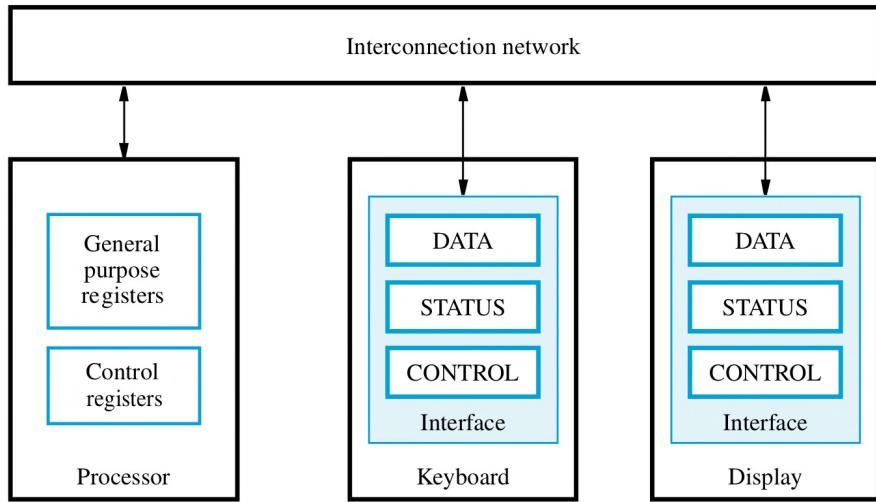
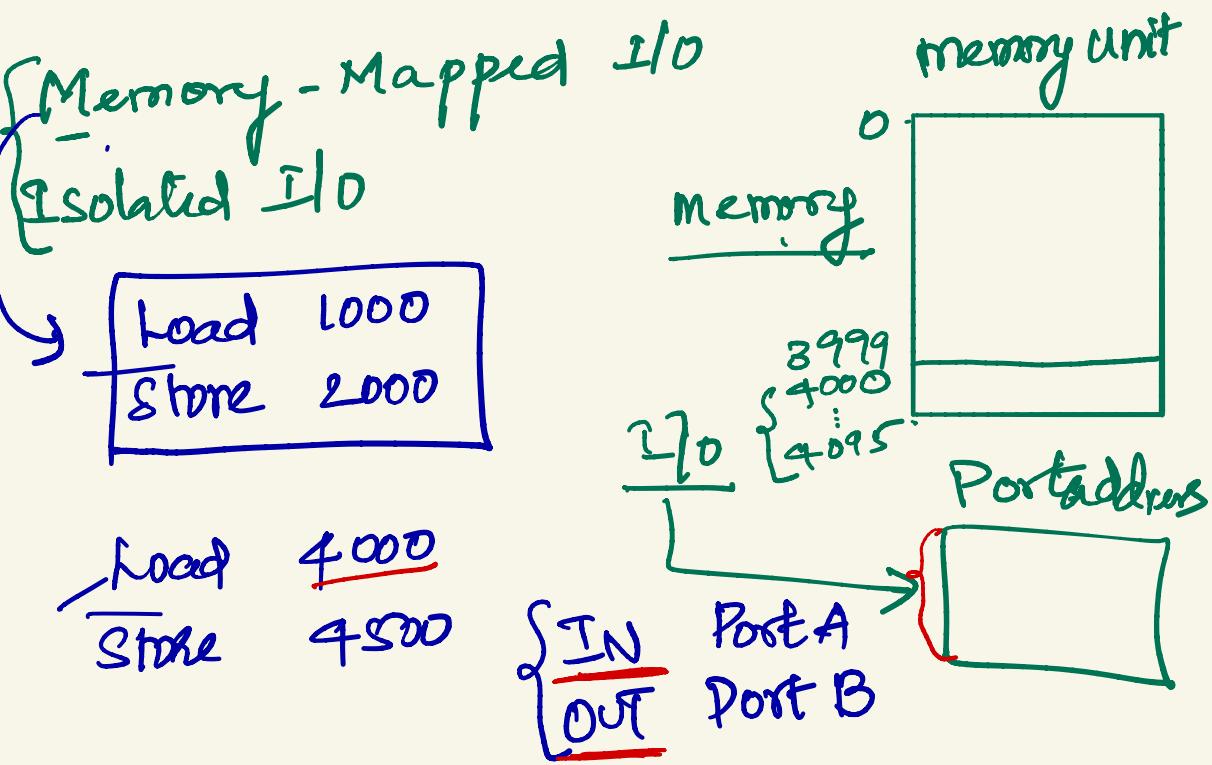


Figure 3.2 The connection for processor, keyboard, and display.



- memory mapped I/O
- a) Common bus { data, address, control }
 └ memory/I/O
- Isolated I/O
- b) Common bus { data, address }
 └ memory/I/O separate control lines
- c) Separate bus { memory & I/O }
 { data, address, control }

Memory mapped I/O

- ① memory port get reduced
- ② less complex
 - ↳ Normal address
 - ↳ same instruction
 - ↳ common connecting

Isolated I/O

- ① memory port can be utilized fully
- ② slightly more complex
 - ↳ foot address
 - ↳ different set
 - ↳ common connecting with dedicated lining

Memory-mapped I/O

- a) less complex
- common bus
 - same instruction (memory & I/O)

Load 4000

- b) memory become less
- address for
- become

Isolated I/O

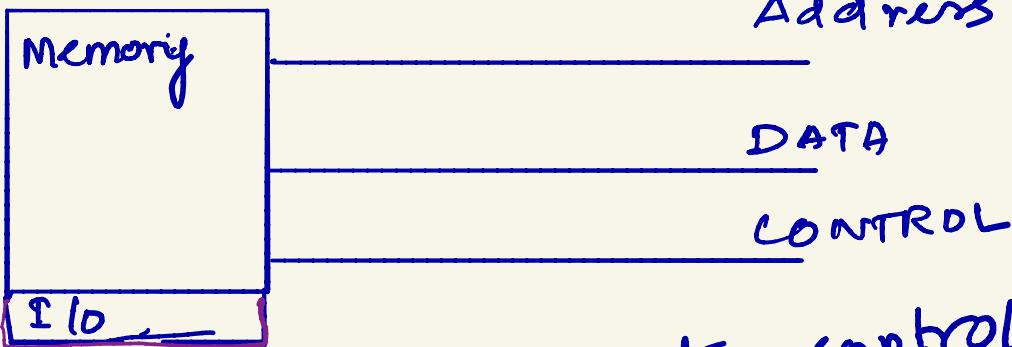
- a) More complex
- common addr/dat
 - separate ctrl lines

IN Port A
OUT Port B

memory can
be utilized
fully

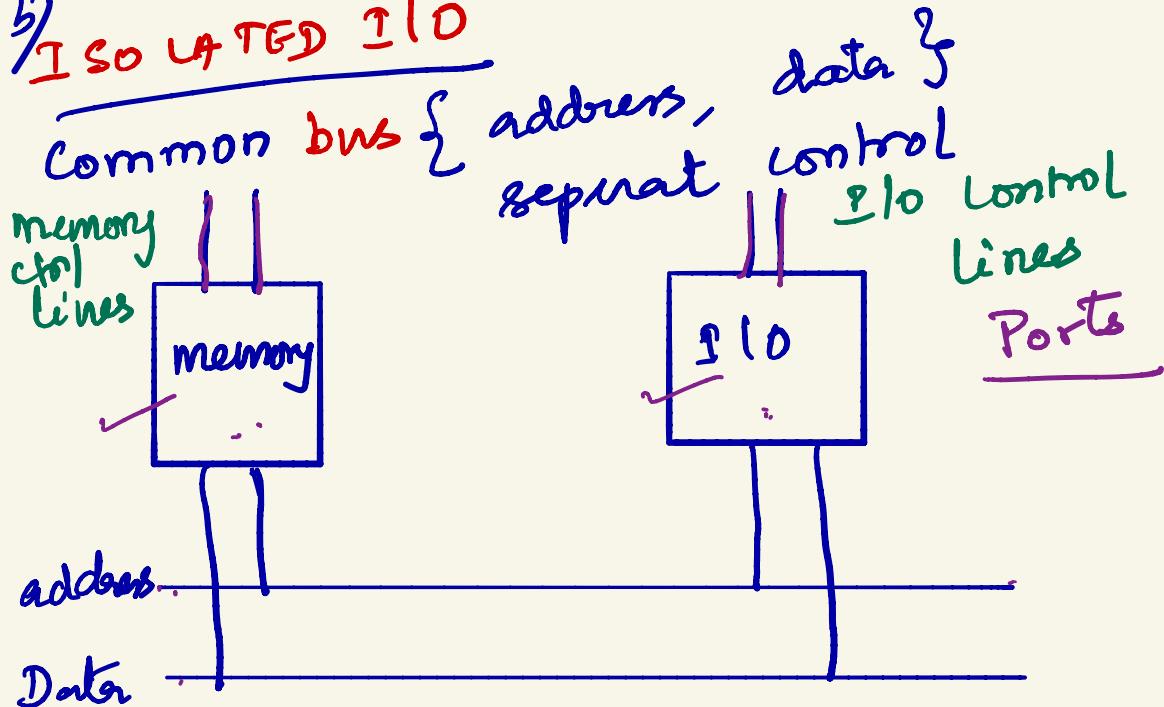
Memory-mapped I/O

a) Memory unit

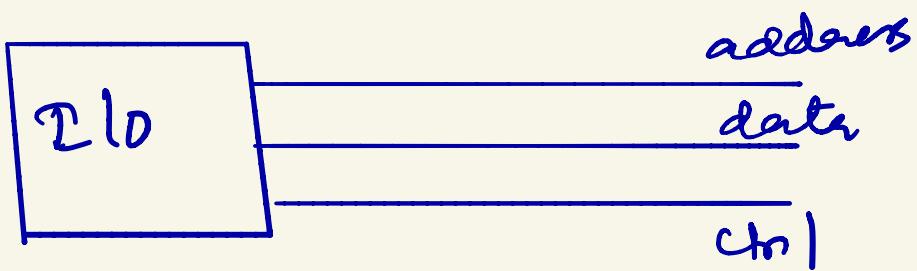
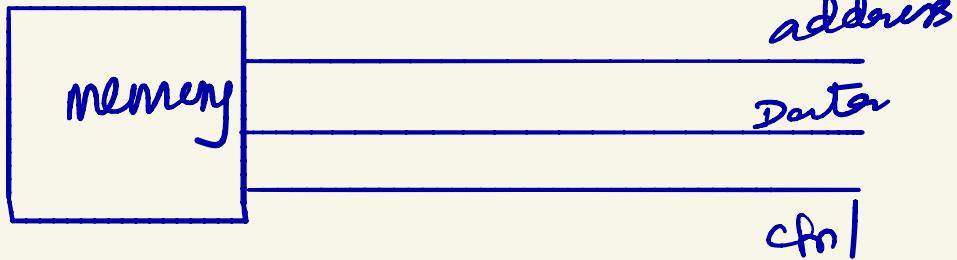


common bus { add, data, control }

b) ISOLATED I/O



c) separate bus for memory & I/O .



Address	7	6	5	4	3	2	1	0				
0x4000												
0x4004					KIN	KIRQ						
0x4008					KIE	KIREQ						
(a) Keyboard interface												
0x4010												
0x4014					DOUT	DIRQ						
0x4018					DIE	DIREQ						
(b) Display interface												

Figure 3.3 Registers in the keyboard and display interfaces.

→ PROGRAMMED I/O Program Control
 → INTERRUPT DRIVEN I/O
 → DMA

Address

7 6 5 4 3 2 1 0

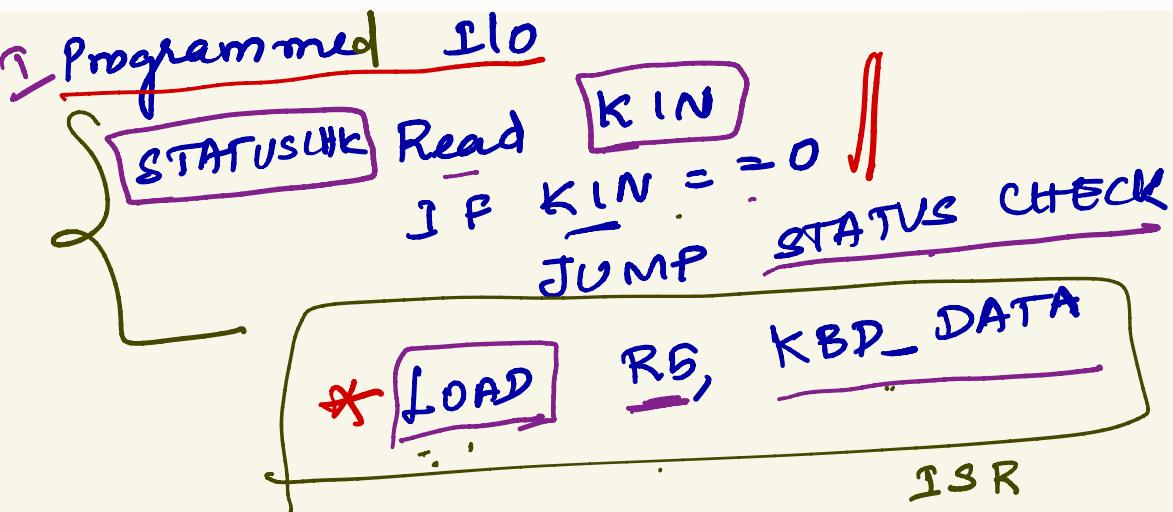
0x4000								KBD_DATA
0x4004								KBD_STATUS
0x4008								KBD_CONT

(a) Keyboard interface

7 6 5 4 3 2 1 0

0x4010								DISP_DATA
0x4014								DISP_STATUS
0x4018								DISP_CONT

(b) Display interface

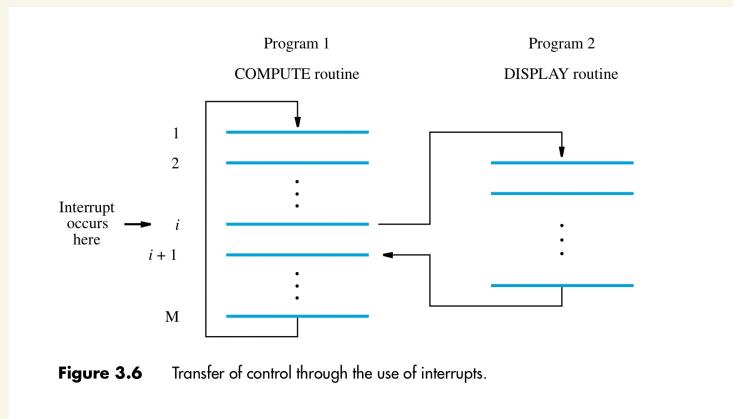
Figure 3.3 Registers in the keyboard and display interfaces.

STATUS CLK Read DOUT
IF DOUT == 0 //
JUMP STATUS CLK

STORE DISP - DATA, RS

<u>MOV</u>	- N ✓
<u>IN</u>	- T
<u>WRITE</u>	- A ✓
<u>STORE</u>	- <u>Somil</u> ✓

→ INTERRUPT DRIVEN I/O



Interrupt request

Interrupt acknowledge

Interrupt service routine

Shadow registers.

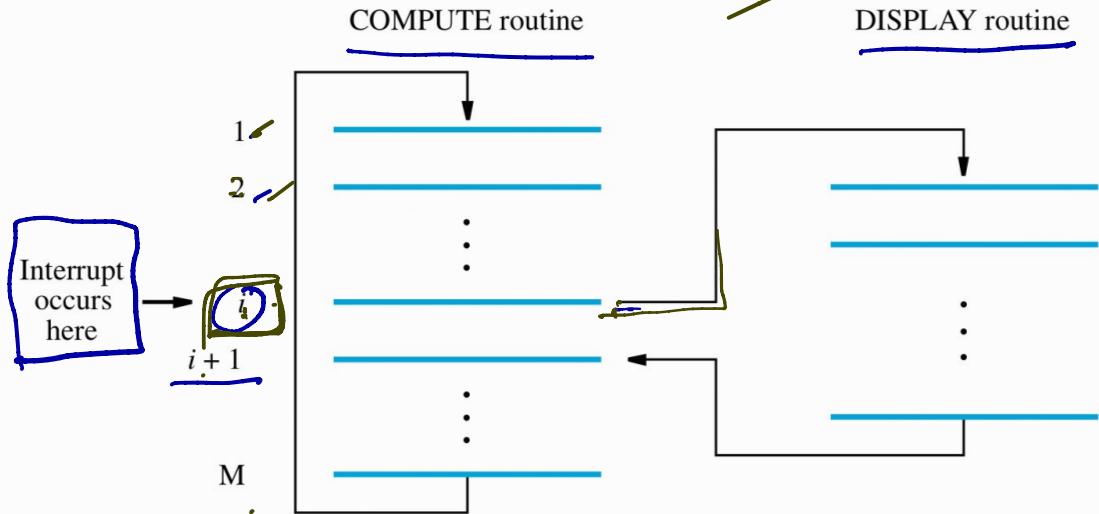
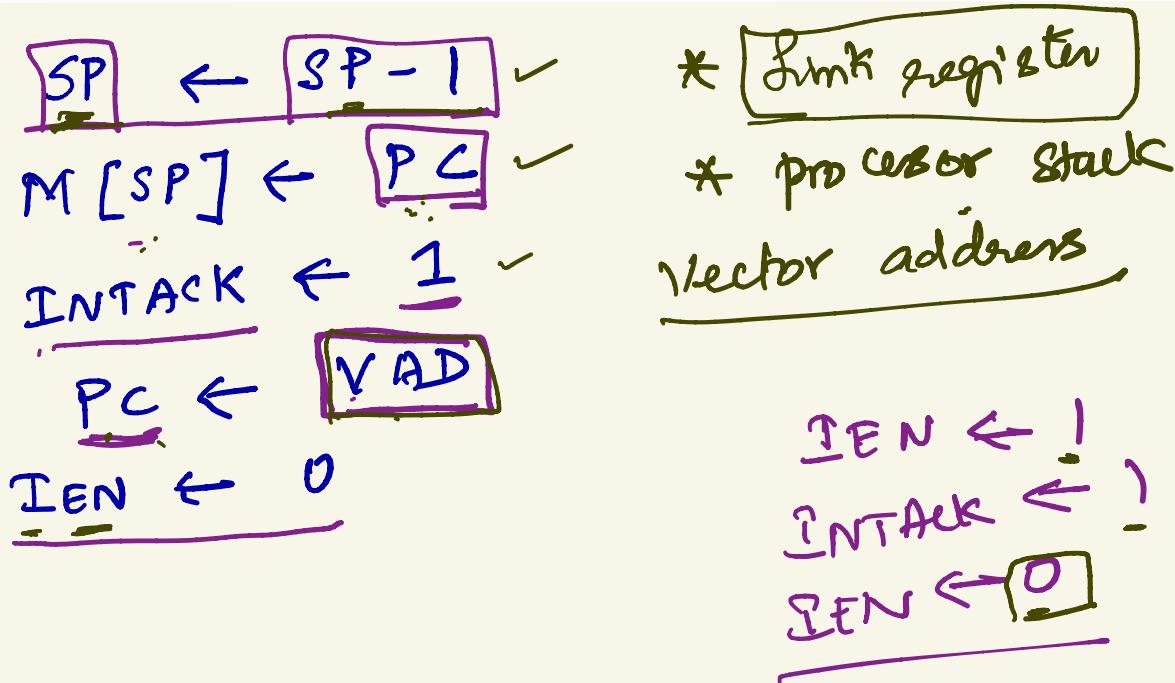
{
Interrupt
latency}

Real time processing.

Program 1

CSR

Program 2

DISPLAY routine**Figure 3.6** Transfer of control through the use of interrupts.

DMA - Direct Memory access.

- * Transfer blocks of data directly between the main memory and I/O devices. (such as disks)

Input devices

- Keyboard
- Micro phone (Amaan)
- Mouse (Virajith)
- Joystick

Output devices

- Display screen
- printer

5/10/2020

Amish

Akash

Abhishek

Tanay

Srisai Mani Kandar

Aishwari

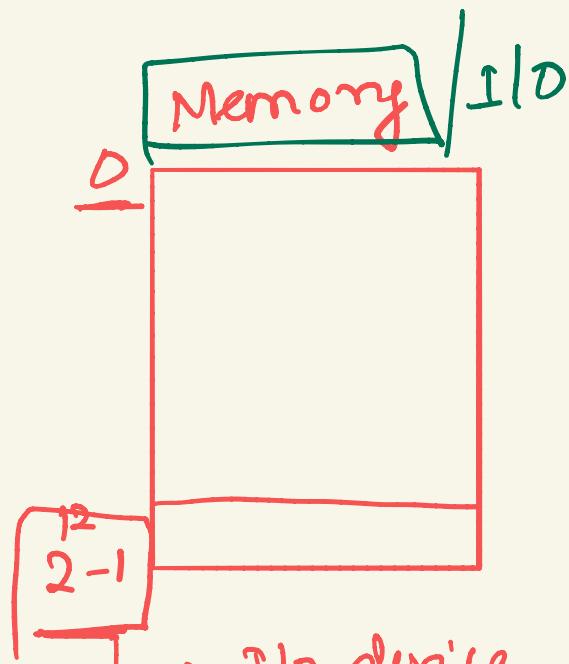
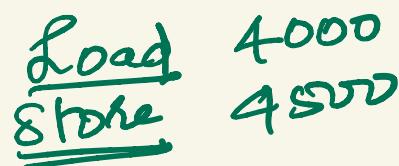
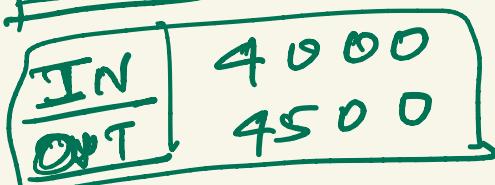
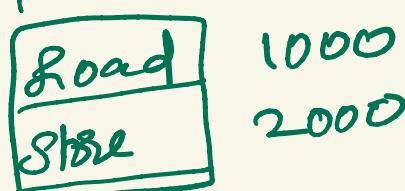
Rakshith.

Vishnu Rahul Varma.

Suparn

Raghav

MEMORY MAPPED I/O



- a) Common bus
- b) Common bus, separate control lines for memory & I/O
- c) Separate bus for memory & I/O.
(Kartick)

STATE CHECK READ DOUT
IF DOUT == 0 //
Jump STATUS Check

* STORE DISP-DATA, R5

