Ripunjay Narula (19BCE0470)

Computer Architecture and Organization

Respected Sir

I am Ripunjay Narula from CSE Core Branch. I like travelling and clicking photos so that is how you can remember me.

Skills:

Front-end web development and graphic designing skills with efficiency in the following softwares:

HTML5

CSS

Javascript

Adobe Photoshop

Adobe Illustrator

Projects:

www.studomatrix.in

* Part of the organization as Design and Technical Team Mentor.

* Built a mobile-first website for the organization while working with a team.

* The website describes the progress of the organization and the details of the clubs it operates with.

* Compatible with all screen sizes.

* Used Bootstrap and Javascript Queries for animations.

Topic-wise Description

Module-1

Computers Components are made up of a motherboard, CPU, RAM, and I/O Devices.

A Register File is a means of memory storage within a computer's CPU. The computer's register files contain bits of data and mapping locations. These locations specify certain addresses that are input components of a register file. Other inputs include data, a read and write function and execute function.

A Stack is an abstract data type that serves as a collection of elements, with two principal operations: push, which adds an element to the collection, and. pop, which removes the most recently added element that was not yet removed.

VNM is an early computer created by Hungarian mathematician John Von Neumann. It included three components: a CPU, A slow-to-access storage area, like a hard drive and secondary fast-access memory (RAM). The machines stored instructions as binary-values.

Module-2

Data Representation and Computer Arithmetic: Data is represented and stored in a computer using groups of binary digits called words. It begins by describing binary codes and how words are used to represent characters. It then concentrates on the representation of positive and negative integers and how binary arithmetic is performed within the machine.

Module-3

An ISA (Instruction Set Architecture) defines the supported data types, the registers, the hardware support for managing main memory, fundamental features (such as the memory consistency, addressing modes, virtual memory), and the input/output model of a family of implementations of the ISA.

The term Addressing Modes refers to the way in which the operand of an instruction is specified. The addressing mode specifies a rule for interpreting or modifying the address field of the instruction before the operand is actually executed.

Analyzing Memory Traffic is the main instrument for determining ineffective memory usage in your app. Excessive allocations and garbage collections may imply significant memory management overhead. For example, you have an array of objects which should be updated over time.

Abductive logic programming (ALP) is a high-level knowledge-representation framework that can be used to solve problems declaratively based on abductive reasoning. It extends normal logic programming by allowing some predicates to be incompletely defined.

Subroutine Call and Return linkage method is a way in which computer call and return the Subroutine. The simplest way of Subroutine linkage is saving the

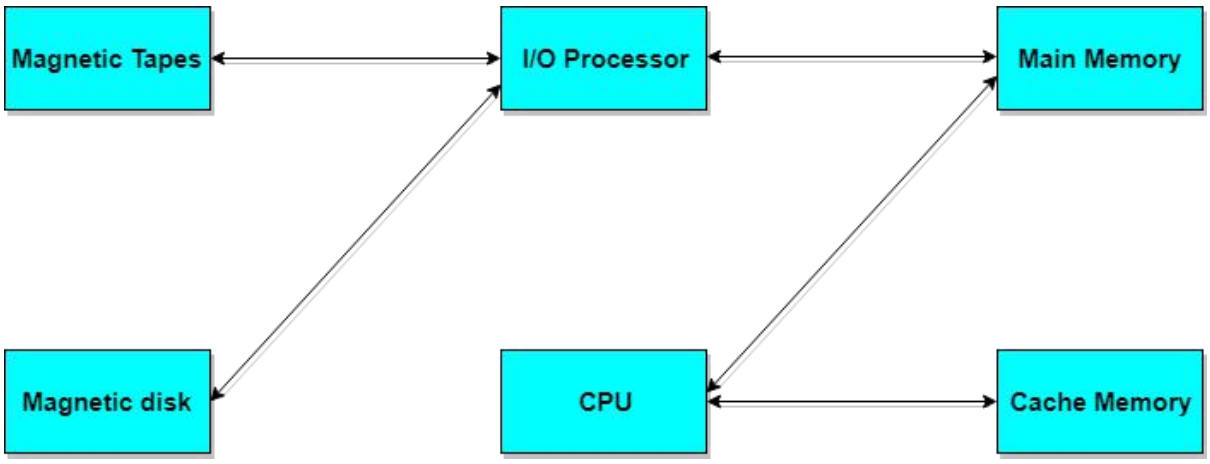
return address in a specific location, such as register which can be called as link register call Subroutine.

Multi-cycle Data Path instruction execution- Breaking instruction execution into multiple clock cycles: Balance amount of work done in each cycle (minimizes the cycle time) Each step contains at most one Register access.

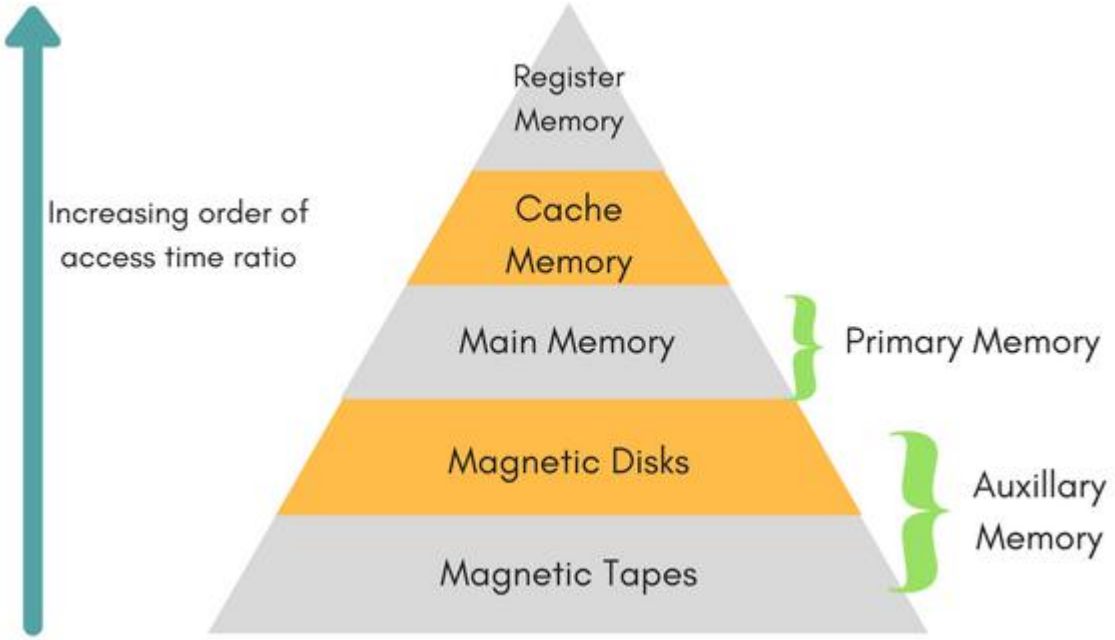
In the Single Cycle Data Path processor, the cycle time was determined by the slowest instruction.

Module-4

Memory Organization: The memory hierarchy system consists of all storage devices contained in a computer system from the slow Auxiliary Memory to fast Main Memory and to smaller Cache memory. Auxiliary memory access time is generally 1000 times that of the main memory, hence it is at the bottom of the hierarchy.



Memory Interleaving is a technique for increasing memory speed. It is a process that makes the system more efficient, fast and reliable by spreading memory addresses across the memory banks.



Memory Design: A computer memory is organized in a hierarchy. In such hierarchy, larger and slower memories are used to supplement smaller and faster ones.

A typical memory hierarchy starts with register memory followed by a small, expensive, and relatively fast unit, called the Cache.

Module-5

I/O Interface is the method that is used to transfer information between internal and external I/O devices is known as I/O interface.

Data Transfer techniques: transfer of data in bits and bytes over digital and analog medium

In computer architecture, a Bus is a communication system that transfers data between components inside a computer, or between computers.

Module-6

RAID (Redundant Array of Independent Disks) is an assortment of hard drives connected and set up in ways to help protect or speed up the performance of

a computer's disk storage. RAID is commonly used on servers and high-performance computers.

Module-7

Flynn's taxonomy is a categorization of forms of parallel computer architectures. From the viewpoint of the assembly language programmer,
parallel computers are classified by the concurrency in processing sequences data, and instructions.

Pipe-lining is the process of accumulating instruction from the processor through a pipeline. It is a technique where multiple instructions are overlapped during execution.

In the domain of CPU design, Hazards are problems with the instruction pipeline in CPU micro architectures when the next instruction cannot execute in the following clock cycle.

Module-8

SMA is an electronic assembly with components mounted on the surface of a circuit board.

A Distributed system, also known as Distributed Computing, is a system with multiple components located on different machines that communicate and coordinate actions to appear as a single coherent system to the end-user.

Parallel computing is a type of computing architecture in which several processors simultaneously execute multiple, smaller calculations broken down from an overall larger, complex problem.

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501-6334	SUN w/2× US III 900MHz CPU Board
X4007A	SUN w/ 4× US III 900MHZ CPU Board 540-5052
	SUN UltraSparc IV+ 1500MHz Processor
	SUN UltraSparc IIIi 500MHz Processor
	SUN UltraSparc IIIi 1600MHz Processor

	SUN UltraSparc IIIi 1503MHz Processor
	SUN UltraSparc IIIi 1336MHz Processor
	SUN UltraSparc IIIi 1280MHz Processor
	SUN UltraSparc IIIi 1167MHz Processor
	SUN UltraSparc IIIi 1064MHz Processor
	SUN UltraSparc IIi 650MHz Processor
	SUN UltraSparc IIi 550MHz Processor
	SUN UltraSparc III 1200MHz Processor
	SUN UltraSparc III 1050MHz Processor
501-6395	SUN UltraSparc III 1015MHz Processor
501-3098	SUN SuperSPARC II CPU Module 501-3098
540-6753	SUN CPU/Memory Board 540-6753
540-6446	SUN CPU/Memory Board 4x 750MHz US III
540-5859	SUN CPU/Memory Board 4x 1.2GHz US III
540-5691	SUN CPU/Memory Board 2x 1.2GHz US III
540-5603	SUN CPU Memory Board 540-5603
X7268A	SUN CPU Board w/2× US IV CPU 1050MHz 501-6809
X7273A-Z	SUN CPU Board w/2× US IV CPU 1.5GHz 501-7481
X7274A	SUN CPU Board w/2× US IV CPU 1.5GHz 501-7058
X7270A	SUN CPU Board w/2× US IV CPU 1.35GHz 501-7305

501-6164	SUN CPU Board w/2× US III CPU 1200MHz 501-6164
501-7713	SUN CPU Board w/2 × US IV CPU 2100MHZ 501-7713
X7300A-Z	SUN CPU Board w/2 × US IV CPU 1.8GHz 501-7506
501-7691	SUN CPU Board w/2 × US IV CPU 1.8GHz 501-7691
540-6439	SUN CPU Board w/ 4× US IV CPU 1500MHz 540-6439
X7275A	SUN CPU Board w/ 2× USIV 1.35GHz 501-6962 16G RAM
501-6002	SUN 900MHz UltraSPARC III Module 501-6002
X7000A	SUN 900MHz UltraSPARC II Module 501-6197
501-3001	SUN 75MHZ SPARC II CPU Module 501-3001
X6990A	SUN 750MHz UltraSPARC III Module 501-5675
X2248A	SUN 480MHz Cache CPU 501-5729
501-5539	SUN 450MHz UltraSPARC II Module 501-5539
501-5149	SUN 440MHz UltraSPARC II Module 501-5149
501-5741	SUN 400MHz UltraSPARC IIi Module 501-5741
501-5740	SUN 400MHz UltraSPARC IIi Module
501-7094	SUN 400MHz UltraSPARC IIi Module
X2580A	SUN 400MHz UltraSPARC II Module 501-6009
501-5838	SUN 400MHz UltraSPARC II Module 501-5838
501-5762	SUN 400MHz UltraSPARC II Module 501-5762

501-5500	SUN 400MHz UltraSPARC II Module 501-5500
501-5446	SUN 400MHz UltraSPARC II Module 501-5446
501-5445	SUN 400MHz UltraSPARC II Module 501-5445
501-5420	SUN 400MHz UltraSPARC II Module 501-5420
501-5239	SUN 400MHz UltraSPARC II Module 501-5239
X1194A	SUN 400MHz UltraSPARC II Module 501-5237
X2580A	SUN 400MHz UltraSPARC II Module 501-5235
501-4995	SUN 400MHz UltraSPARC II Module
501-5148	SUN 360MHz UltraSPARC IIi Module 501-5148
501-5129	SUN 360MHz UltraSPARC II Module 501-5129
501-4781	SUN 360MHZ UltraSPARC II Module 501-4781
501-5568	SUN 333Mhz UltraSPARC IIi Processor 501-5568
501-5090	SUN 333MHz UltraSPARC II Module 501-5090
501-5040	SUN 300MHz UltraSPARC IIi Module 501-5040
501-4379	SUN 300MHz UltraSPARC IIi Module 501-4379
501-4849	SUN 300MHz UltraSPARC IIi Module
501-5039	SUN 270MHz UltraSPARC IIi Module 501-5039
501-4857	SUN 250MHz UltraSPARC II Module 501-4857
501-4836	SUN 250MHz UltraSPARC II Module 501-4836
371-4932	SUN 2 × SPARC64 VII+ 2.66GHz CPU Module

375-3568	SUN 2 × SPARC64 VII 2.4GHz CPU Module
375-3477	SUN 2 × SPARC64 VI 2.1GHz CPU Module
X7310A	SUN 1200MHz UltraSPARC III Module 501-6745
X7310A	SUN 1200MHz UltraSPARC III Module 501-6485
501-7461	SUN 1.593GHz CPU Board Assembly 501-7463
501-7461	SUN 1.593GHz CPU Board Assembly 501-7462
501-7461	SUN 1.593GHz CPU Board Assembly 501-7368
501-6788	SUN 1.593GHz CPU Board Assembly 501-7093
501-6788	SUN 1.593GHz CPU Board Assembly 501-6788
501-6788	SUN 1.593GHz CPU Board Assembly 501-6786
501-6370	SUN 1.28GHz CPU Board Assembly 501-6532
501-7029	SUN 1.28GHz CPU Board Assembly 501-6532
501-6369	SUN 1.062GHz CPU Board Assembly 501-6461
501-6369	SUN 1.062GHz CPU Board Assembly 501-6369

- MOS Technology 6502 (1975)
- Zilog Z80 (1976)
- **AMD**

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- Motorola
- Qualcomm
- IBM
- Samsung
- ARM – ARM Architecture
- AT&T – Hobbit
- Bell Labs – Bellmac 32
- Fujitsu – FR, FR-V, SPARC64 V
- HP – Saturn, PA-8900
- IBM – IBM z13, RS64-IV, POWER8