Section II. I/O Interfaces

This section provides information about Cyclone® IV device family I/O features and high-speed differential and external memory interfaces.

This section includes the following chapters:

- Chapter 6, I/O Features in Cyclone IV Devices
- Chapter 7, External Memory Interfaces in Cyclone IV Devices

Revision History

Refer to each chapter for its own specific revision history. For information about when each chapter was updated, refer to the Chapter Revision Dates section, which appears in the complete handbook.

6. I/O Features in Cyclone IV Devices

CYIV-51006-2.2

This chapter describes the I/O and high speed I/O capabilities and features offered in Cyclone® IV devices.

The I/O capabilities of Cyclone IV devices are driven by the diversification of I/O standards in many low-cost applications, and the significant increase in required I/O performance. Altera's objective is to create a device that accommodates your key board design needs with ease and flexibility.

The I/O flexibility of Cyclone IV devices is increased from the previous generation low-cost FPGAs by allowing all I/O standards to be selected on all I/O banks. Improvements to on-chip termination (OCT) support and the addition of true differential buffers have eliminated the need for external resistors in many applications, such as display system interfaces.

High-speed differential I/O standards have become popular in high-speed interfaces because of their significant advantages over single-ended I/O standards. The Cyclone IV devices support LVDS, BLVDS, RSDS, mini-LVDS, and PPDS. The transceiver reference clocks and the existing general-purpose I/O (GPIO) clock input features also support the LVDS I/O standards.

The Quartus® II software completes the solution with powerful pin planning features that allow you to plan and optimize I/O system designs even before the design files are available.

This chapter includes the following sections:

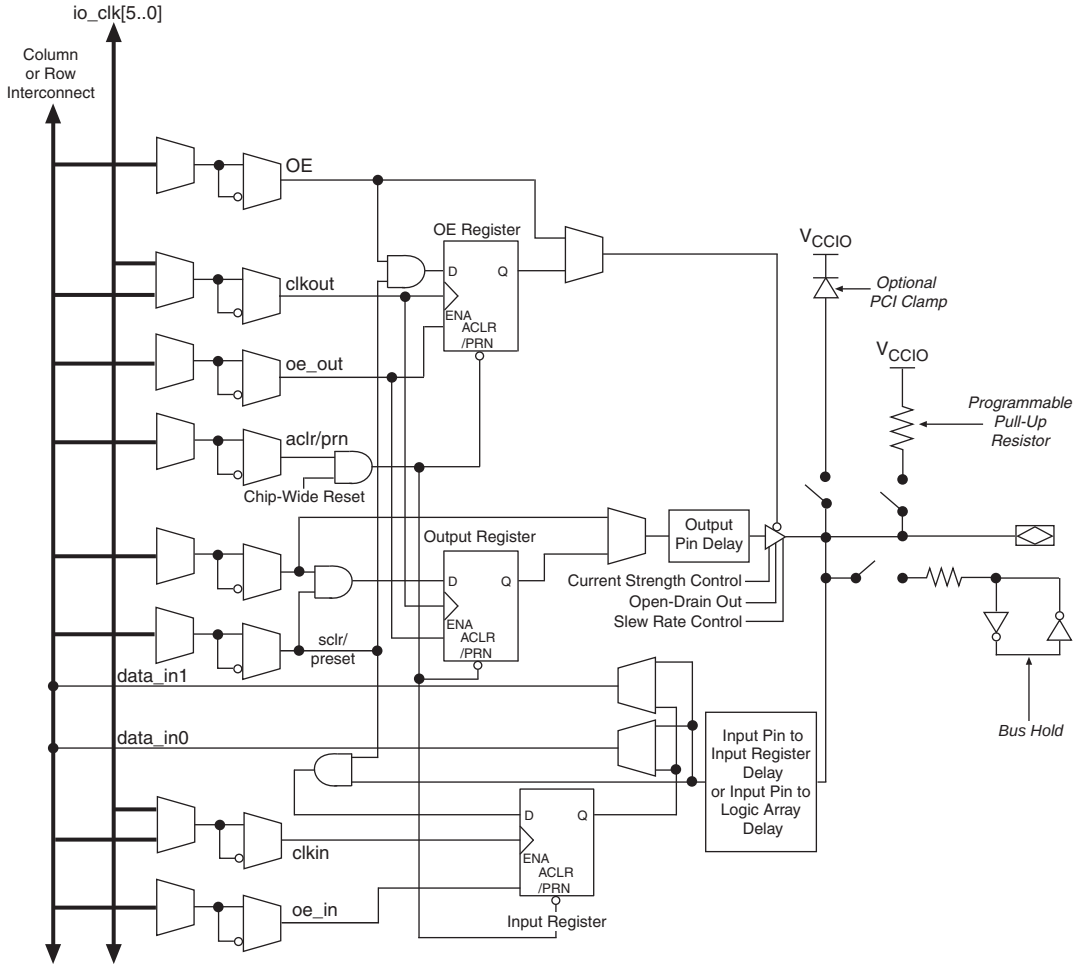
Cyclone IV I/O Elements

Cyclone IV I/O elements (IOEs) contain a bidirectional I/O buffer and five registers for registering input, output, output-enable signals, and complete embedded bidirectional single-data rate transfer. I/O pins support various single-ended and differential I/O standards.

The IOE contains one input register, two output registers, and two output-enable (OE) registers. The two output registers and two OE registers are used for DDR applications. You can use input registers for fast setup times and output registers for fast clock-to-output times. Additionally, you can use OE registers for fast clock-to-output enable timing. You can use IOEs for input, output, or bidirectional data paths.

Figure 6–1 shows the Cyclone IV devices IOE structure for single data rate (SDR) operation.

Figure 6–1. Cyclone IV IOEs in a Bidirectional I/O Configuration for SDR Mode



I/O Element Features

The Cyclone IV IOE offers a range of programmable features for an I/O pin. These features increase the flexibility of I/O utilization and provide a way to reduce the usage of external discrete components, such as pull-up resistors and diodes.

Programmable Current Strength

The output buffer for each Cyclone IV I/O pin has a programmable current strength control for certain I/O standards.

The LVTTL, LVCMOS, SSTL-2 Class I and II, SSTL-18 Class I and II, HSTL-18 Class I and II, HSTL-15 Class I and II, and HSTL-12 Class I and II I/O standards have several levels of current strength that you can control.

Table 6–2 on page 6–7 shows the possible settings for I/O standards with current strength control. These programmable current strength settings are a valuable tool in helping decrease the effects of simultaneously switching outputs (SSO) in conjunction with reducing system noise. The supported settings ensure that the device driver meets the specifications for `IOH` and `IOL` of the corresponding I/O standard.

When you use programmable current strength, on-chip series termination (R_S OCT) is not available.

Slew Rate Control

The output buffer for each Cyclone IV I/O pin provides optional programmable output slew-rate control. Table 6–2 on page 6–7 shows the possible slew rate option and the Quartus II default slew rate setting. However, these fast transitions may introduce noise transients in the system. A slower slew rate reduces system noise, but adds a nominal delay to rising and falling edges. Because each I/O pin has an individual slew-rate control, you can specify the slew rate on a pin-by-pin basis. The slew-rate control affects both the rising and falling edges. Slew rate control is available for single-ended I/O standards with current strength of 8 mA or higher.

You cannot use the programmable slew rate feature when using OCT with calibration.

You cannot use the programmable slew rate feature when using the 3.0-V PCI, 3.0-V PCI-X, 3.3-V LVTTL, or 3.3-V LVCMOS I/O standards. Only the fast slew rate (default) setting is available.

Open-Drain Output

Cyclone IV devices provide an optional open-drain (equivalent to an open-collector) output for each I/O pin. This open-drain output enables the device to provide system-level control signals (for example, interrupt and write enable signals) that are asserted by multiple devices in your system.

Bus Hold

Each Cyclone IV device user I/O pin provides an optional bus-hold feature. The bus-hold circuitry holds the signal on an I/O pin at its last-driven state. Because the bus-hold feature holds the last-driven state of the pin until the next input signal is present, an external pull-up or pull-down resistor is not necessary to hold a signal level when the bus is tri-stated.

The bus-hold circuitry also pulls undriven pins away from the input threshold voltage in which noise can cause unintended high-frequency switching. You can select this feature individually for each I/O pin. The bus-hold output drives no higher than V_{CCIO} to prevent overdriving signals.

If you enable the bus-hold feature, the device cannot use the programmable pull-up option. Disable the bus-hold feature when the I/O pin is configured for differential signals. Bus-hold circuitry is not available on dedicated clock pins.

Bus-hold circuitry is only active after configuration. When going into user mode, the bus-hold circuit captures the value on the pin present at the end of configuration.

For the specific sustaining current for each V_{CCIO} voltage level driven through the resistor and for the overdrive current used to identify the next driven input level, refer to the *Cyclone IV Device Datasheet* chapter.

Programmable Pull-Up Resistor

Each Cyclone IV device I/O pin provides an optional programmable pull-up resistor while in user mode. If you enable this feature for an I/O pin, the pull-up resistor holds the output to the V_{CCIO} level of the output pin's bank.

If you enable the programmable pull-up resistor, the device cannot use the bus-hold feature. Programmable pull-up resistors are not supported on the dedicated configuration, JTAG, and dedicated clock pins.

When the optional `DEV_OE` signal drives low, all I/O pins remains tri-stated even with the programmable pull-up option enabled.

Programmable Delay

The Cyclone IV IOE includes programmable delays to ensure zero hold times, minimize setup times, increase clock-to-output times, and delay the clock input signal.

A path in which a pin directly drives a register may require a programmable delay to ensure zero hold time, whereas a path in which a pin drives a register through combinational logic may not require the delay. Programmable delays minimize setup time. The Quartus II Compiler can program these delays to automatically minimize setup time while providing a zero hold time. Programmable delays can increase the register-to-pin delays for output registers. Each dual-purpose clock input pin provides a programmable delay to the global clock networks.

Table 6–1 shows the programmable delays for Cyclone IV devices.

Table 6–1. Cyclone IV Devices Programmable Delay Chain

Programmable Delay	Quartus II Logic Option
Input pin-to-logic array delay	Input delay from pin to internal cells
Input pin-to-input register delay	Input delay from pin to input register
Output pin delay*(1)*	Delay from output register to output pin
Dual-purpose clock input pin delay	Input delay from dual-purpose clock pin to fan-out destinations

Note to Table 6–1:

(1) Cyclone IV E devices do not support delay from output register to output pin.

There are two paths in the IOE for an input to reach the logic array. Each of the two paths can have a different delay. This allows you to adjust delays from the pin to the internal logic element (LE) registers that reside in two different areas of the device. You must set the two combinational input delays with the input delay from pin to internal cells logic option in the Quartus II software for each path. If the pin uses the input register, one of the delays is disregarded and the delay is set with the input delay from pin to input register logic option in the Quartus II software.

The IOE registers in each I/O block share the same source for the preset or clear features. You can program preset or clear for each individual IOE, but you cannot use both features simultaneously. You can also program the registers to power-up high or low after configuration is complete. If programmed to power-up low, an asynchronous clear can control the registers. If programmed to power-up high, an asynchronous preset can control the registers. This feature prevents the inadvertent activation of the active-low input of another device upon power-up. If one register in an IOE uses a preset or clear signal, all registers in the IOE must use that same signal if they require preset or clear. Additionally, a synchronous reset signal is available for the IOE registers.

For more information about the input and output pin delay settings, refer to the *Area and Timing Optimization* chapter in volume 2 of the *Quartus II Handbook*.

PCI-Clamp Diode

Cyclone IV devices provide an optional PCI-clamp diode enabled input and output for each I/O pin. Dual-purpose configuration pins support the diode in user mode if the specific pins are not used as configuration pins for the selected configuration scheme. For example, if you are using the active serial (AS) configuration scheme, you cannot use the clamp diode on the ASDO and nCSO pins in user mode. Dedicated configuration pins do not support the on-chip diode.

The PCI-clamp diode is available for the following I/O standards:

- 3.3-V LVTTL
- 3.3-V LVCMOS
- 3.0-V LVTTL
- 3.0-V LVCMOS
- 2.5-V LVTTL/LVCMOS
- PCI
- PCI-X

If the input I/O standard is one of the listed standards, the PCI-clamp diode is enabled by default in the Quartus II software.

OCT Support

Cyclone IV devices feature OCT to provide I/O impedance matching and termination capabilities. OCT helps prevent reflections and maintain signal integrity while minimizing the need for external resistors in high pin-count ball grid array (BGA) packages. Cyclone IV devices provide I/O driver on-chip impedance matching and R_S OCT for single-ended outputs and bidirectional pins.

When using R_S OCT, programmable current strength is not available.

There are two ways to implement OCT in Cyclone IV devices:

- OCT with calibration
- OCT without calibration

Table 6–2 lists the I/O standards that support impedance matching and series termination.

Table 6–2. Cyclone IV Device I/O Features Support (Part 1 of 2)

I/O Standard	IOH/IOL Current Strength Setting (mA) *(1)*		R_S OCT with Calibration Setting, Ohm (Ω)		R_S OCT Without Calibration Setting, Ohm (Ω)		Cyclone IV E I/O Banks Support	Cyclone IV GX I/O Banks Support	Slew Rate Option *(6)*	PCI-clamp Diode Support
	Column I/O	Row I/O	Column I/O	Row I/O *(8)*	Column I/O	Row I/O *(8)*				
3.3-V LVTTL	4,8	4,8	—	—	—	—	1,2,3,4, 5,6,7,8	3,4,5,6, 7,8,9	—	✓
3.3-V LVCMOS	2	2	—	—	—	—			—	✓
3.0-V LVTTL	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25			0,1,**2**	✓
3.0-V LVCMOS	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25				✓
3.0-V PCI/PCI-X	—	—	—	—	—	—			—	✓
2.5-V LVTTL/LVCMOS	4,8,12,16	4,8,12,16	50,25	50,25	50,25	50,25			0,1,**2**	✓
1.8-V LVTTL/LVCMOS	2,4,6,8,10,12,16	2,4,6,8,10,12,16	50,25	50,25	50,25	50,25				—
1.5-V LVCMOS	2,4,6,8,10,12,16	2,4,6,8,10,12,16	50,25	50,25	50,25	50,25				—
1.2-V LVCMOS	2,4,6,8,10,12	2,4,6,8,10	50,25	50	50,25	50		4,5,6,7,8		—
SSTL-2 Class I	8,12	8,12	50	50	50	50		3,4,5,6, 7,8,9		—
SSTL-2 Class II	16	16	25	25	25	25				—
SSTL-18 Class I	8,10,12	8,10,12	50	50	50	50				—
SSTL-18 Class II	12,16	12,16	25	25	25	25				—
HSTL-18 Class I	8,10,12	8,10,12	50	50	50	50				—
HSTL-18 Class II	16	16	25	25	25	25				—
HSTL-15 Class I	8,10,12	8,10,12	50	50	50	50				—
HSTL-15 Class II	16	16	25	25	25	25				—
HSTL-12 Class I	8,10,12	8,10	50	50	50	50		4,5,6,7,8		—
HSTL-12 Class II	14	—	25	—	25	—	3,4,7,8	4,7,8		—

Table 6–2. Cyclone IV Device I/O Features Support (Part 2 of 2)

I/O Standard	IOH/IOL Current Strength Setting (mA) *(1)*		R_S OCT with Calibration Setting, Ohm (Ω)		R_S OCT Without Calibration Setting, Ohm (Ω)		Cyclone IV E I/O Banks Support	Cyclone IV GX I/O Banks Support	Slew Rate Option *(6)*	PCI-clamp Diode Support
	Column I/O	Row I/O	Column I/O	Row I/O *(8)*	Column I/O	Row I/O *(8)*				
Differential SSTL-2 Class I *(2)*, *(7)*	8,12	8,12	50	50	50	50	1,2,3,4, 5,6,7,8	3,4,5,6, 7,8	0,1,**2**	—
Differential SSTL-2 Class II *(2)*, *(7)*	16	16	25	25	25	25				—
Differential SSTL-18 *(2)*, *(7)*	8,10,12	—	50	—	50	—				—
Differential HSTL-18 *(2)*, *(7)*	8,10,12	—	50	—	50	—				—
Differential HSTL-15 *(2)*, *(7)*	8,10,12	—	50	—	50	—				—
Differential HSTL-12 *(2)*, *(7)*	8,10,12	—	50	—	50	—	3,4,7,8	4,7,8		—
BLVDS	8,12,16	8,12,16	—	—	—	—	1,2,3,4, 5,6,7,8	3,4,5,6, 7,8	0,1,**2**	—
LVDS *(3)*	—	—	—	—	—	—		5,6	—	—
PPDS *(3)*, *(4)*	—	—	—	—	—	—			—	—
RSDS and mini-LVDS *(3)*, *(4)*	—	—	—	—	—	—			—	—
Differential LVPECL *(5)*	—	—	—	—	—	—		3,4,5,6, 7,8	—	—

Notes to Table 6–2:

(1) The default current strength setting in the Quartus II software is 50-Ω OCT without calibration for all non-voltage reference and HSTL/SSTL Class I I/O standards. The default setting is 25-Ω OCT without calibration for HSTL/SSTL Class II I/O standards.

(2) The differential SSTL-18 and SSTL-2, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards are supported only on clock input pins and PLL output clock pins.

(3) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only for Cyclone IV E devices and right I/O banks 5 and 6 only for Cyclone IV GX devices. Differential outputs in column I/O banks require an external resistor network.

(4) This I/O standard is supported for outputs only.

(5) This I/O standard is supported for clock inputs only

(6) The default Quartus II slew rate setting is in bold; **2** for all I/O standards that supports slew rate option.

(7) Differential SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12 I/O standards do not support Class II output.

(8) Cyclone IV GX devices only support right I/O pins.

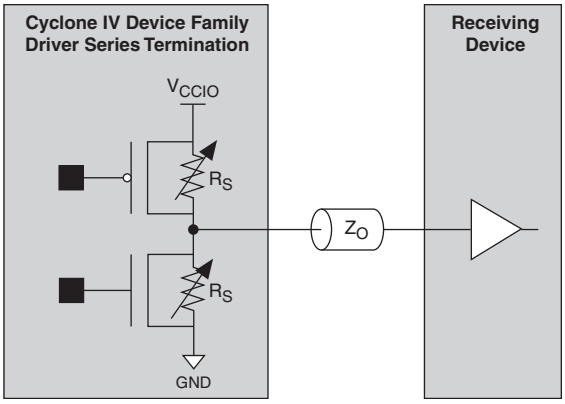
For more details about the differential I/O standards supported in Cyclone IV I/O banks, refer to "High-Speed I/O Interface" on page 6–23.

On-Chip Series Termination with Calibration

Cyclone IV devices support R_S OCT with calibration in the top, bottom, and right I/O banks. The R_S OCT calibration circuit compares the total impedance of the I/O buffer to the external 25-Ω ±1% or 50-Ω ±1% resistors connected to the RUP and RDN pins, and dynamically adjusts the I/O buffer impedance until they match (as shown in Figure 6–2).

The R_S shown in Figure 6–2 is the intrinsic impedance of the transistors that make up the I/O buffer.

Figure 6–2. Cyclone IV Devices R_S OCT with Calibration



OCT with calibration is achieved using the OCT calibration block circuitry. There is one OCT calibration block in each of I/O banks 2, 4, 5, and 7 for Cyclone IV E devices and I/O banks 4, 5, and 7 for Cyclone IV GX devices. Each calibration block supports each side of the I/O banks. Because there are two I/O banks sharing the same calibration block, both banks must have the same V_{CCIO} if both banks enable OCT calibration. If two related banks have different V_{CCIO}, only the bank in which the calibration block resides can enable OCT calibration.

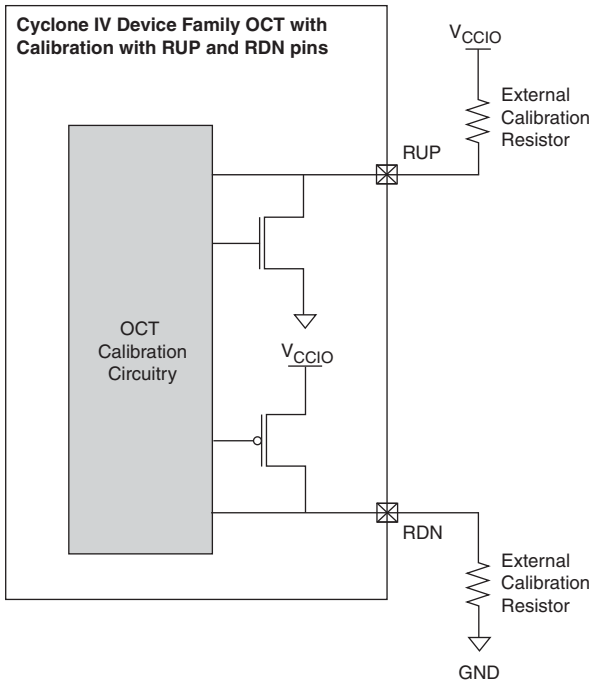
Figure 6–10 on page 6–18 shows the top-level view of the OCT calibration blocks placement.

Each calibration block comes with a pair of RUP and RDN pins. When used for calibration, the RUP pin is connected to V_{CCIO} through an external 25-Ω ±1% or 50-Ω ±1% resistor for an R_S OCT value of 25 Ω or 50 Ω , respectively. The RDN pin is connected to GND through an external 25-Ω ±1% or 50-Ω ±1% resistor for an R_S OCT value of 25 Ω or 50 Ω , respectively. The external resistors are compared with the internal resistance using comparators. The resultant outputs of the comparators are used by the OCT calibration block to dynamically adjust buffer impedance.

☞ During calibration, the resistance of the RUP and RDN pins varies.

Figure 6–3 shows the external calibration resistors setup on the RUP and RDN pins and the associated OCT calibration circuitry.

Figure 6–3. Cyclone IV Devices R_S OCT with Calibration Setup



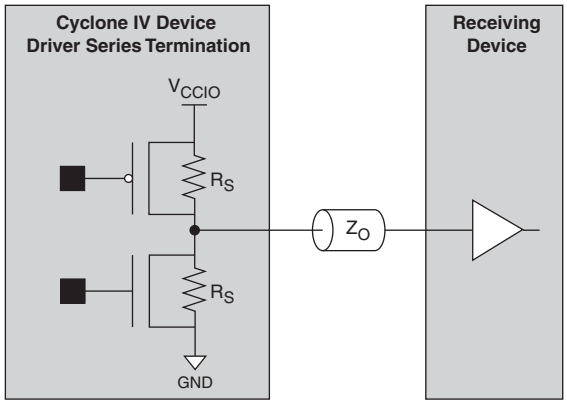
RUP and RDN pins go to a tri-state condition when calibration is completed or not running. These two pins are dual-purpose I/Os and function as regular I/Os if you do not use the calibration circuit.

On-Chip Series Termination Without Calibration

Cyclone IV devices support driver impedance matching to match the impedance of the transmission line, which is typically 25 or 50 Ω. When used with the output drivers, OCT sets the output driver impedance to 25 or 50 Ω. Cyclone IV devices also support I/O driver series termination (R_S = 50 Ω) for SSTL-2 and SSTL-18.

Figure 6–4 shows the single-ended I/O standards for OCT without calibration. The R_S shown is the intrinsic transistor impedance.

Figure 6–4. Cyclone IV Devices R_S OCT Without Calibration



All I/O banks and I/O pins support impedance matching and series termination. Dedicated configuration pins and JTAG pins do not support impedance matching or series termination.

R_S OCT is supported on any I/O bank. V_{CCIO} and V_{REF} must be compatible for all I/O pins to enable R_S OCT in a given I/O bank. I/O standards that support different R_S values can reside in the same I/O bank as long as their V_{CCIO} and V_{REF} do not conflict.

Impedance matching is implemented using the capabilities of the output driver and is subject to a certain degree of variation, depending on the process, voltage, and temperature.

For more information about tolerance specification, refer to the *Cyclone IV Device Datasheet* chapter.

I/O Standards

Cyclone IV devices support multiple single-ended and differential I/O standards. Cyclone IV devices support 3.3-, 3.0-, 2.5-, 1.8-, 1.5-, and 1.2-V I/O standards.

Table 6–3 summarizes I/O standards supported by Cyclone IV devices and which I/O pins support them.

Table 6–3. Cyclone IV Devices Supported I/O Standards and Constraints (Part 1 of 2)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Column I/O Pins			Row I/O Pins *(1)*	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
3.3-V LVTTL, 3.3-V LVCMOS *(2)*	Single-ended	JESD8-B	3.3/3.0/2.5 *(3)*	3.3	✓	✓	✓	✓	✓
3.0-V LVTTL, 3.0-V LVCMOS *(2)*	Single-ended	JESD8-B	3.3/3.0/2.5 *(3)*	3.0	✓	✓	✓	✓	✓
2.5-V LVTTL / LVCMOS	Single-ended	JESD8-5	3.3/3.0/2.5 *(3)*	2.5	✓	✓	✓	✓	✓
1.8-V LVTTL / LVCMOS	Single-ended	JESD8-7	1.8/1.5 *(3)*	1.8	✓	✓	✓	✓	✓
1.5-V LVCMOS	Single-ended	JESD8-11	1.8/1.5 *(3)*	1.5	✓	✓	✓	✓	✓
1.2-V LVCMOS *(4)*	Single-ended	JESD8-12A	1.2	1.2	✓	✓	✓	✓	✓
SSTL-2 Class I, SSTL-2 Class II	voltage-referenced	JESD8-9A	2.5	2.5	✓	✓	✓	✓	✓
SSTL-18 Class I, SSTL-18 Class II	voltage-referenced	JESD815	1.8	1.8	✓	✓	✓	✓	✓
HSTL-18 Class I, HSTL-18 Class II	voltage-referenced	JESD8-6	1.8	1.8	✓	✓	✓	✓	✓
HSTL-15 Class I, HSTL-15 Class II	voltage-referenced	JESD8-6	1.5	1.5	✓	✓	✓	✓	✓
HSTL-12 Class I	voltage-referenced	JESD8-16A	1.2	1.2	✓	✓	✓	✓	✓
HSTL-12 Class II *(9)*	voltage-referenced	JESD8-16A	1.2	1.2	✓	✓	✓	—	—
PCI and PCI-X	Single-ended	—	3.0	3.0	✓	✓	✓	✓	✓
Differential SSTL-2 Class I or Class II	Differential *(5)*	JESD8-9A	—	2.5	—	✓	—	—	—
			2.5	—	✓	—	—	✓	—
Differential SSTL-18 Class I or Class II	Differential *(5)*	JESD815	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-18 Class I or Class II	Differential *(5)*	JESD8-6	—	1.8	—	✓	—	—	—
			1.8	—	✓	—	—	✓	—
Differential HSTL-15 Class I or Class II	Differential *(5)*	JESD8-6	—	1.5	—	✓	—	—	—
			1.5	—	✓	—	—	✓	—
Differential HSTL-12 Class I or Class II	Differential *(5)*	JESD8-16A	—	1.2	—	✓	—	—	—
			1.2	—	✓	—	—	✓	—

Table 6–3. Cyclone IV Devices Supported I/O Standards and Constraints (Part 2 of 2)

I/O Standard	Type	Standard Support	V_{CCIO} Level (in V)		Column I/O Pins			Row I/O Pins *(1)*	
			Input	Output	CLK, DQS	PLL_OUT	User I/O Pins	CLK, DQS	User I/O Pins
PPDS *(6)*	Differential	—	—	2.5	—	✓	✓	—	✓
LVDS *(10)*	Differential	ANSI/TIA/EIA-644	2.5	2.5	✓	✓	✓	✓	✓
RSDS and mini-LVDS *(6)*	Differential	—	—	2.5	—	✓	✓	—	✓
BLVDS *(8)*	Differential	—	2.5	2.5	—	—	✓	—	✓
LVPECL *(7)*	Differential	—	2.5	—	✓	—	—	✓	—

Notes to Table 6–3:

(1) Cyclone IV GX devices only support right I/O pins.
(2) The PCI-clamp diode must be enabled for 3.3-V/3.0-V LVTTL/LVCMOS.
(3) The Cyclone IV architecture supports the MultiVolt I/O interface feature that allows Cyclone IV devices in all packages to interface with I/O systems that have different supply voltages.
(4) Cyclone IV GX devices do not support 1.2-V V_{CCIO} in banks 3 and 9. I/O pins in bank 9 are dual-purpose I/O pins that are used as configuration or GPIO pins. Configuration scheme is not support at 1.2 V, therefore bank 9 can not be powered up at 1.2-V V_{CCIO}.
(5) Differential HSTL and SSTL outputs use two single-ended outputs with the second output programmed as inverted. Differential HSTL and SSTL inputs treat differential inputs as two single-ended HSTL and SSTL inputs and only decode one of them. Differential HSTL and SSTL are only supported on CLK pins.
(6) PPDS, mini-LVDS, and RSDS are only supported on output pins.
(7) LVPECL is only supported on clock inputs.
(8) Bus LVDS (BLVDS) output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses LVDS input buffer.
(9) 1.2-V HSTL input is supported at both column and row I/Os regardless of Class I or Class II.
(10) True LVDS, RSDS, and mini-LVDS I/O standards are supported in right I/O pins, while emulated LVDS, RSDS, and mini-LVDS I/O standards are supported in the top, bottom, and right I/O pins.

Cyclone IV devices support PCI and PCI-X I/O standards at 3.0-V V_{CCIO}. The 3.0-V PCI and PCI-X I/O are fully compatible for direct interfacing with 3.3-V PCI systems without requiring any additional components. The 3.0-V PCI and PCI-X outputs meet the V_{IH} and V_{IL} requirements of 3.3-V PCI and PCI-X inputs with sufficient noise margin.

For more information about the 3.3/3.0/2.5-V LVTTL & LVCMOS multivolt I/O support, refer to *AN 447: Interfacing Cyclone III and Cyclone IV Devices with 3.3/3.0/2.5-V LVTTL/LVCMOS I/O Systems*.

Termination Scheme for I/O Standards

This section describes recommended termination schemes for voltage-referenced and differential I/O standards.

The 3.3-V LVTTL, 3.0-V LVTTL and LVCMOS, 2.5-V LVTTL and LVCMOS, 1.8-V LVTTL and LVCMOS, 1.5-V LVCMOS, 1.2-V LVCMOS, 3.0-V PCI, and PCI-X I/O standards do not specify a recommended termination scheme per the JEDEC standard

Voltage-Referenced I/O Standard Termination

Voltage-referenced I/O standards require an input reference voltage (V_{REF}) and a termination voltage (V_{TT}). The reference voltage of the receiving device tracks the termination voltage of the transmitting device, as shown in Figure 6–5 and Figure 6–6.

Figure 6–5. Cyclone IV Devices HSTL I/O Standard Termination

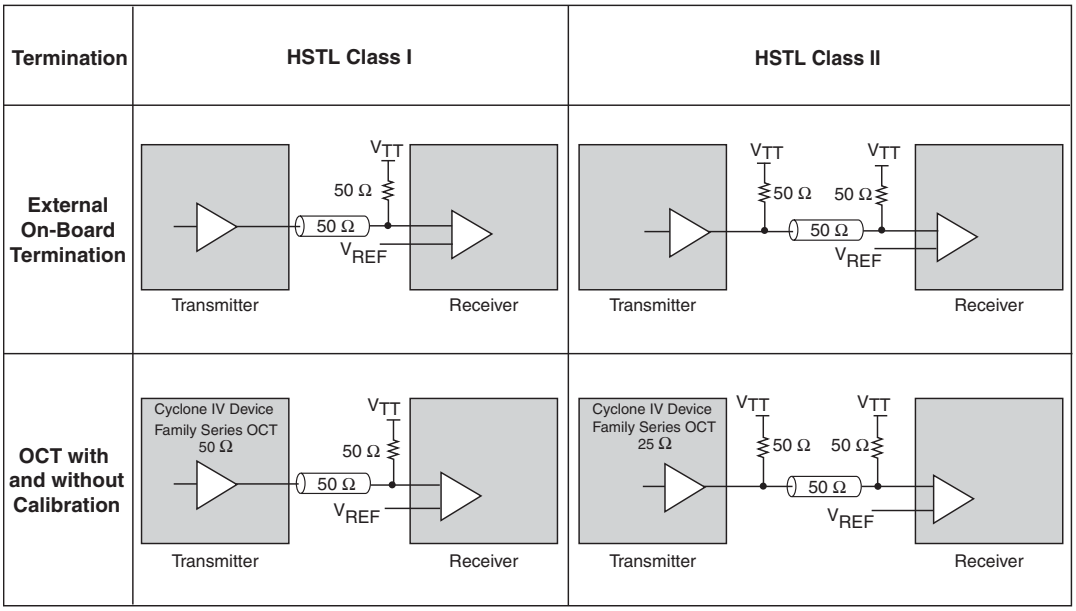
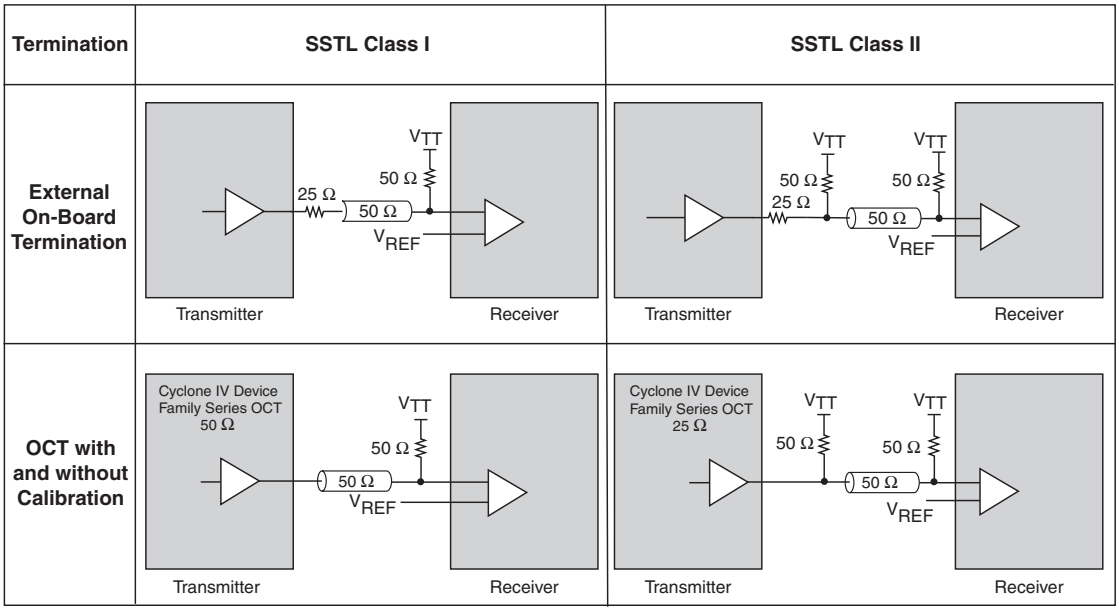


Figure 6–6. Cyclone IV Devices SSTL I/O Standard Termination



Differential I/O Standard Termination

Differential I/O standards typically require a termination resistor between the two signals at the receiver. The termination resistor must match the differential load impedance of the bus (refer to Figure 6–7 and Figure 6–8).

Cyclone IV devices support differential SSTL-2 and SSTL-18, differential HSTL-18, HSTL-15, and HSTL-12, PPDS, LVDS, RSDS, mini-LVDS, and differential LVPECL.

Figure 6–7. Cyclone IV Devices Differential HSTL I/O Standard Class I and Class II Interface and Termination

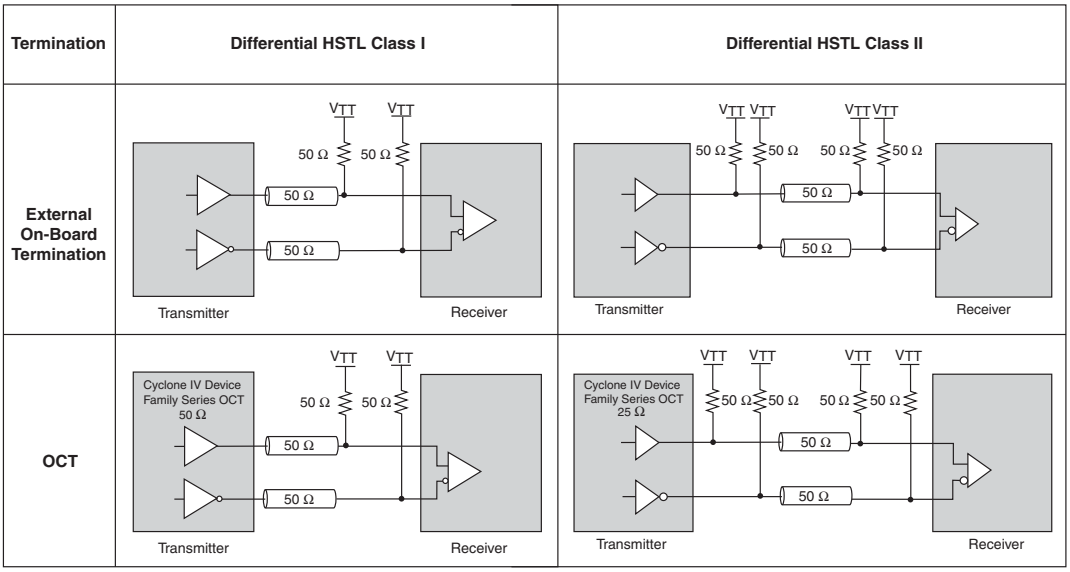
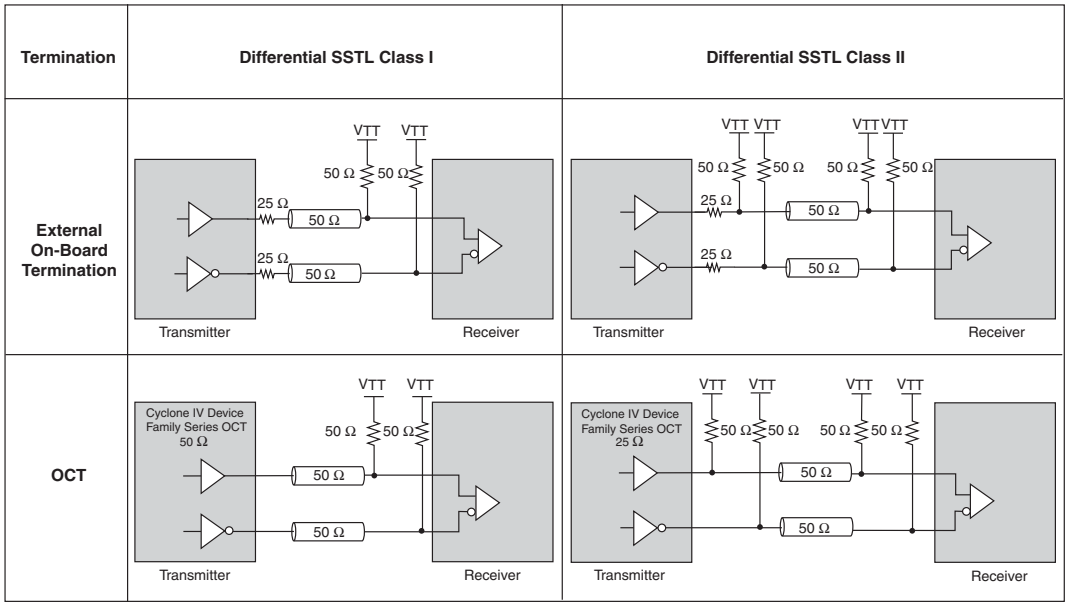


Figure 6–8. Cyclone IV Devices Differential SSTL I/O Standard Class I and Class II Interface and Termination *(Note 1)*



Note to Figure 6–8:

(1) Only Differential SSTL-2 I/O standard supports Class II output.

I/O Banks

I/O pins on Cyclone IV devices are grouped together into I/O banks. Each bank has a separate power bus.

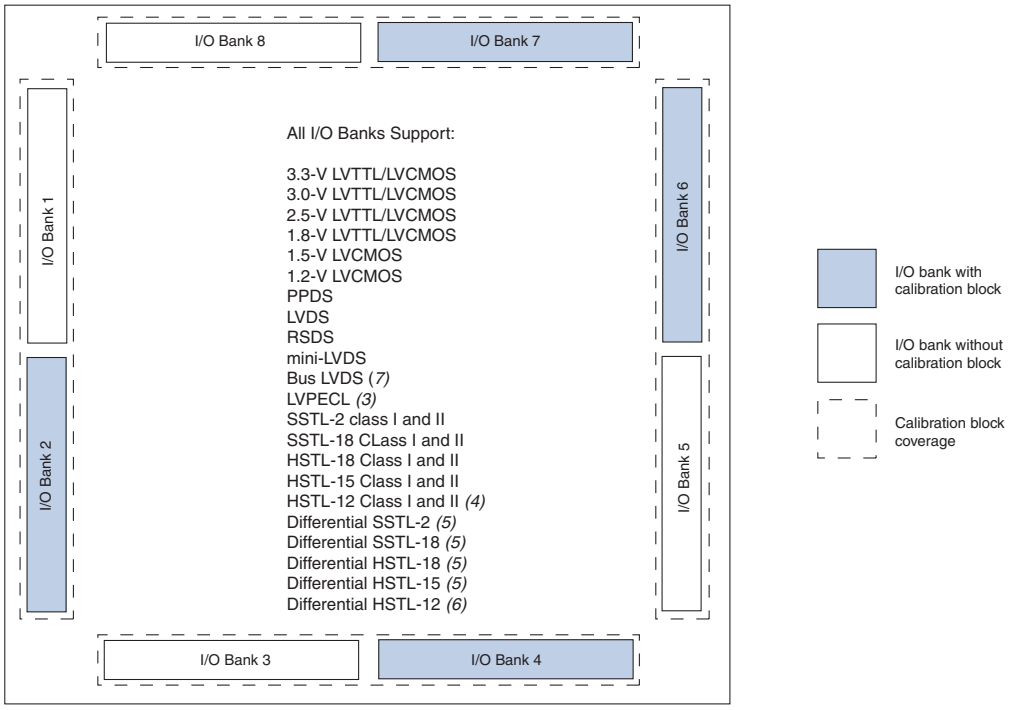
Cyclone IV E devices have eight I/O banks, as shown in Figure 6–9. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported in all banks except HSTL-12 Class II, which is only supported in column I/O banks. All differential I/O standards are supported in all banks. The only exception is HSTL-12 Class II, which is only supported in column I/O banks.

Cyclone IV GX devices have up to ten I/O banks and two configuration banks, as shown in Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19. The Cyclone IV GX configuration I/O bank contains three user I/O pins that can be used as normal user I/O pins if they are not used in configuration modes. Each device I/O pin is associated with one I/O bank. All single-ended I/O standards are supported except HSTL-12 Class II, which is only supported in column I/O banks. All differential I/O standards are supported in top, bottom, and right I/O banks. The only exception is HSTL-12 Class II, which is only supported in column I/O banks.

The entire left side of the Cyclone IV GX devices contain dedicated high-speed transceiver blocks for high speed serial interface applications. There are a total of 2, 4, and 8 transceiver channels for Cyclone IV GX devices, depending on the density and package of the device. For more information about the transceiver channels supported, refer to Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19.

Figure 6–9 shows the overview of Cyclone IV E I/O banks.

Figure 6–9. Cyclone IV E I/O Banks *(Note 1)*, *(2)*



Notes to Figure 6–9:

(1) This is a top view of the silicon die. This is only a graphical representation. For exact pin locations, refer to the pin list and the Quartus II software.

(2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 1, 2, 5, and 6 only. External resistors are needed for the differential outputs in column I/O banks.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The HSTL-12 Class II is supported in column I/O banks 3, 4, 7, and 8 only.

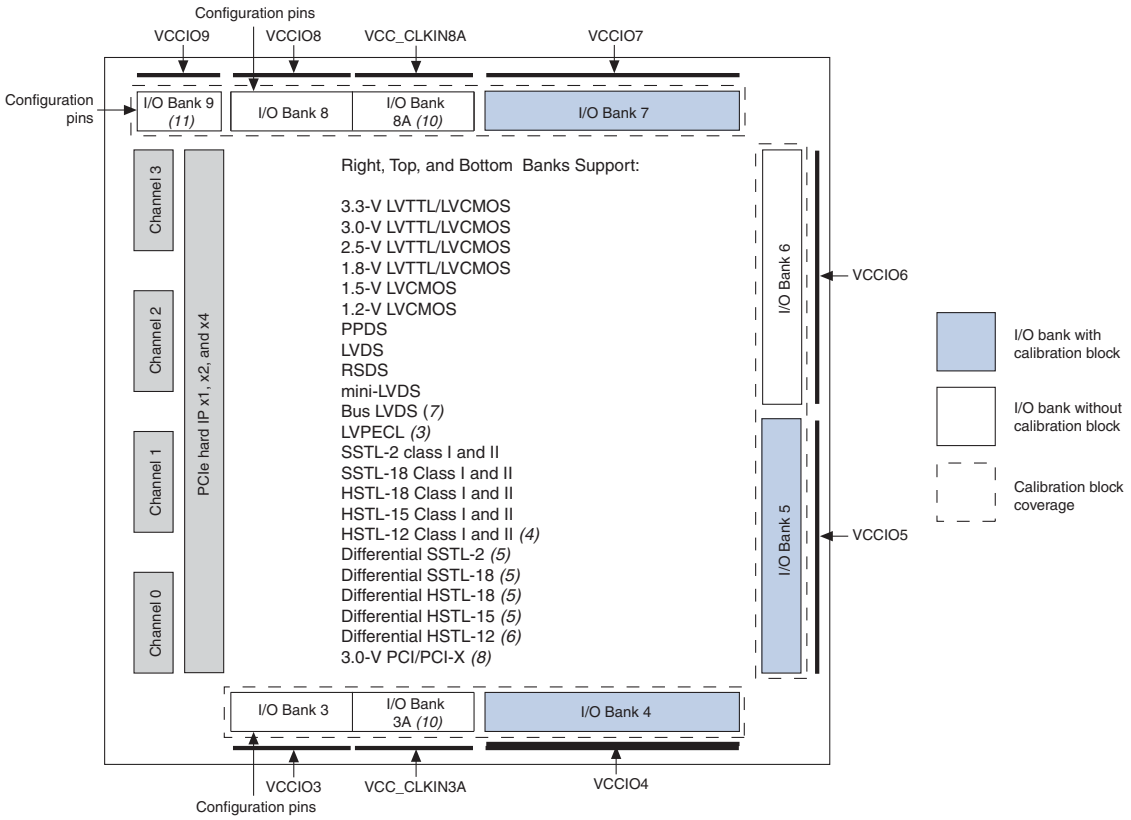
(5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. Differential SSTL-18, differential HSTL-18, and HSTL-15 I/O standards do not support Class II output.

(6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 3, 4, 7, and 8.

(7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses true LVDS input buffer.

Figure 6–10 and Figure 6–11 show the overview of Cyclone IV GX I/O banks.

Figure 6–10. Cyclone IV GX I/O Banks for EP4CGX15, EP4CGX22, and EP4CGX30 *(Note 1), (2), (9)*



Notes to Figure 6–10:

(1) This is a top view of the silicon die. For exact pin locations, refer to the pin list and the Quartus II software. Channels 2 and 3 are not available in EP4CGX15 and F169 package type in EP4CGX22 and EP4CGX30 devices.

(2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 5 and 6 only. External resistors are needed for the differential outputs in column I/O banks.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The HSTL-12 Class II is supported in column I/O banks 4, 7, and 8.

(5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

(6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 4, 7, and 8.

(7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses the LVDS input buffer.

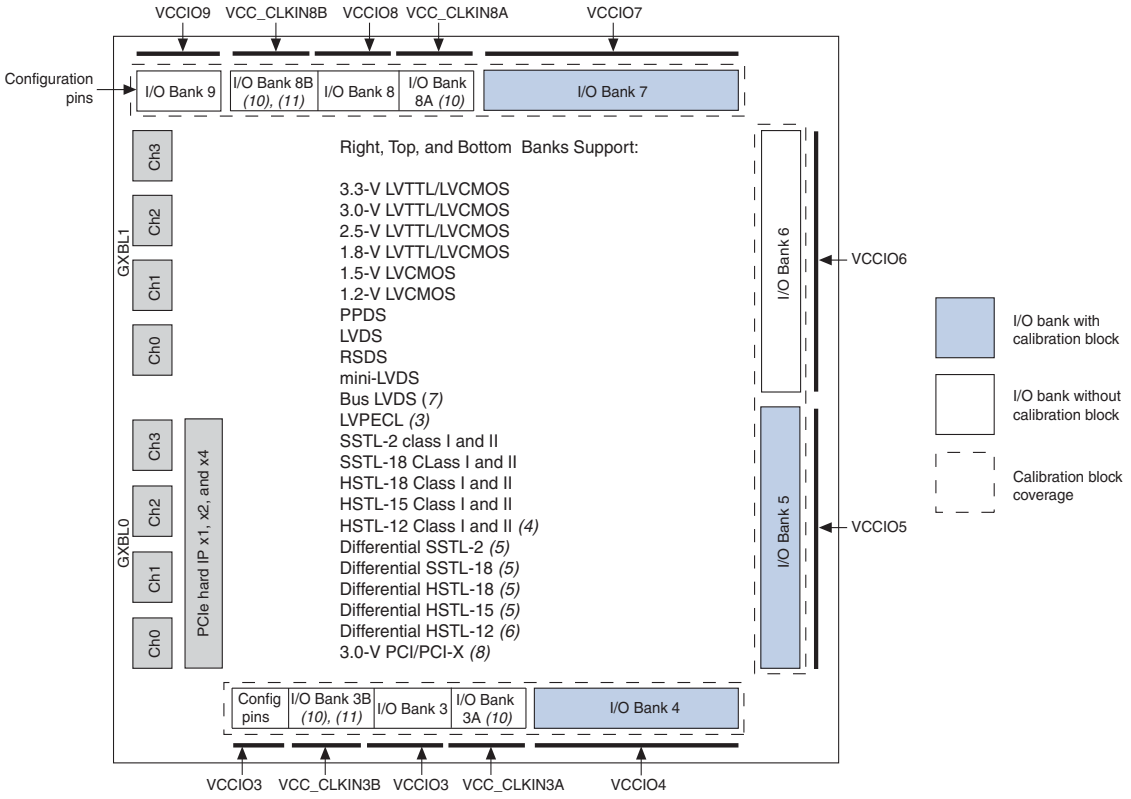
(8) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.

(9) The OCT block is located in the shaded banks 4, 5, and 7.

(10) There are two dedicated clock input I/O banks (I/O bank 3A and I/O bank 8A) that can be used for either high-speed serial interface (HSSI) input reference clock pins or clock input pins.

(11) There are dual-purpose I/O pins in bank 9. If input pins with VREF I/O standards are used on these dual-purpose I/O pins during user mode, they share the VREF pin in bank 8.These dual-purpose IO pins in bank 9 when used in user mode also support R_S OCT without calibration and they share the OCT block with bank 8.

Figure 6–11. Cyclone IV GX I/O Banks for EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 *(Note 1), (2), (9)*



Notes to Figure 6–11:

(1) This is a top view of the silicon die. For exact pin locations, refer to the pin list and the Quartus II software.

(2) True differential (PPDS, LVDS, mini-LVDS, and RSDS I/O standards) outputs are supported in row I/O banks 5 and 6 only. External resistors are needed for the differential outputs in column I/O banks.

(3) The LVPECL I/O standard is only supported on clock input pins. This I/O standard is not supported on output pins.

(4) The HSTL-12 Class II is supported in column I/O banks 4, 7, and 8.

(5) The differential SSTL-18 and SSTL-2, differential HSTL-18, and HSTL-15 I/O standards are supported only on clock input pins and phase-locked loops (PLLs) output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

(6) The differential HSTL-12 I/O standard is only supported on clock input pins and PLL output clock pins. Differential HSTL-12 Class II is supported only in column I/O banks 4, 7, and 8.

(7) BLVDS output uses two single-ended outputs with the second output programmed as inverted. BLVDS input uses the LVDS input buffer.

(8) The PCI-X I/O standard does not meet the IV curve requirement at the linear region.

(9) The OCT block is located in the shaded banks 4, 5, and 7.

(10) The dedicated clock input I/O banks 3A, 3B, 8A, and 8B can be used either for HSSI input reference clock pins or clock input pins.

(11) Single-ended clock input support is available for dedicated clock input I/O banks 3B and 8B.

Each Cyclone IV I/O bank has a VREF bus to accommodate voltage-referenced I/O standards. Each VREF pin is the reference source for its V_{REF} group. If you use a V_{REF} group for voltage-referenced I/O standards, connect the VREF pin for that group to the appropriate voltage level. If you do not use all the V_{REF} groups in the I/O bank for voltage-referenced I/O standards, you can use the VREF pin in the unused voltage-referenced groups as regular I/O pins. For example, if you have SSTL-2 Class I input pins in I/O bank 3 and they are all placed in the VREFB1N[0] group, VREFB1N[0] must be powered with 1.25 V, and the remaining VREFB1N[1..3] pins (if available) are used as I/O pins. If multiple V_{REF} groups are used in the same I/O bank, the VREF pins must all be powered by the same voltage level because the VREF pins are shorted together within the same I/O bank.

When VREF pins are used as regular I/Os, they have higher pin capacitance than regular user I/O pins. This has an impact on the timing if the pins are used as inputs and outputs.

For more information about VREF pin capacitance, refer to the pin capacitance section in the *Cyclone IV Device Datasheet* chapter.

For information about how to identify V_{REF} groups, refer to the Cyclone IV **Device Pin-Out** files or the **Quartus II Pin Planner** tool.

Table 6–4 and Table 6–5 summarize the number of VREF pins in each I/O bank for the Cyclone IV device family.

Table 6–4. Number of VREF Pins Per I/O Bank for Cyclone IV E Devices

Device	EP4CE6			EP4CE10			EP4CE15					EP4CE22			EP4CE30		EP4CE40			EP4CE55			EP4CE75			EP4CE115	
I/O Bank *(1)*	144-EQPF	256-UBGA	256-FBGA	144-EQPF	256-UBGA	256-FBGA	144-EQPF	164-MBGA	256-UBGA	256-FBGA	484-FBGA	144-EQPF	256-UBGA	256-FBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-FBGA	780-FBGA
1	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
2	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
3	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
4	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
5	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
6	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
7	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3
8	1	1	1	1	1	1	2	2	2	2	2	1	1	1	4	4	4	4	4	2	2	2	3	3	3	3	3

Note to Table 6–4:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.

Table 6–5. Number of VREF Pins Per I/O Bank for Cyclone IV GX Devices

Device	4CGX15		4CGX22		4CGX30		4CGX50		4CGX75		4CGX110			4CGX150		
I/O Bank *(1)*	148-QFN	169-FBGA	169-FBGA	324-FBGA	169-FBGA	324-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	896-FBGA	484-FBGA	672-FBGA	896-FBGA
3	1		1		1		3		3		3			3		
4	1		1		1		3		3		3			3		
5	1		1		1		3		3		3			3		
6	1		1		1		3		3		3			3		
7	1		1		1		3		3		3			3		
8*(2)*	1		1		1		3		3		3			3		

Notes to Table 6–5:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.

(2) Bank 9 does not have VREF pin. If input pins with VREF I/O standards are used in bank 9 during user mode, it shares the VREF pin in bank 8.

Each Cyclone IV I/O bank has its own VCCIO pins. Each I/O bank can support only one V_{CCIO} setting from among 1.2, 1.5, 1.8, 3.0, or 3.3 V. Any number of supported single-ended or differential standards can be simultaneously supported in a single I/O bank, as long as they use the same V_{CCIO} levels for input and output pins.

When designing LVTTL/LVCMOS inputs with Cyclone IV devices, refer to the following guidelines:

- All pins accept input voltage (V_I) up to a maximum limit (3.6 V), as stated in the recommended operating conditions provided in the *Cyclone IV Device Datasheet* chapter.
- Whenever the input level is higher than the bank V_{CCIO}, expect higher leakage current.
- The LVTTL/LVCMOS I/O standard input pins can only meet the V_{IH} and V_{IL} levels according to bank voltage level.

Voltage-referenced standards are supported in an I/O bank using any number of single-ended or differential standards, as long as they use the same V_{REF} and V_{CCIO} values. For example, if you choose to implement both SSTL-2 and SSTL-18 in your Cyclone IV devices, I/O pins using these standards—because they require different V_{REF} values—must be in different banks from each other. However, the same I/O bank can support SSTL-2 and 2.5-V LVCMOS with the V_{CCIO} set to 2.5 V and the V_{REF} set to 1.25 V.

When using Cyclone IV devices as a receiver in 3.3-, 3.0-, or 2.5-V LVTTL/LVCMOS systems, you are responsible for managing overshoot or undershoot to stay in the absolute maximum ratings and the recommended operating conditions, provided in the *Cyclone IV Device Datasheet* chapter.

The PCI clamping diode is enabled by default in the Quartus II software for input signals with bank V_{CCIO} at 2.5, 3.0, or 3.3 V.

High-Speed Differential Interfaces

Cyclone IV devices can send and receive data through LVDS signals. For the LVDS transmitter and receiver, the input and output pins of Cyclone IV devices support serialization and deserialization through internal logic.

The BLVDS extends the benefits of LVDS to multipoint applications such as bidirectional backplanes. The loading effect and the need to terminate the bus at both ends for multipoint applications require BLVDS to drive out a higher current than LVDS to produce a comparable voltage swing. All the I/O banks of Cyclone IV devices support BLVDS for user I/O pins.

The RSDS and mini-LVDS standards are derivatives of the LVDS standard. The RSDS and mini-LVDS I/O standards are similar in electrical characteristics to LVDS, but have a smaller voltage swing and therefore provide increased power benefits and reduced electromagnetic interference (EMI).

The PPDS standard is the next generation of the RSDS standard introduced by National Semiconductor Corporation. Cyclone IV devices meet the National Semiconductor Corporation PPDS Interface Specification and support the PPDS standard for outputs only. All the I/O banks of Cyclone IV devices support the PPDS standard for output pins only.

The LVDS standard does not require an input reference voltage, but it does require a 100-Ω termination resistor between the two signals at the input buffer. An external resistor network is required on the transmitter side for the top and bottom I/O banks.

External Memory Interfacing

Cyclone IV devices support I/O standards required to interface with a broad range of external memory interfaces, such as DDR SDRAM, DDR2 SDRAM, and QDR II SRAM.

For more information about Cyclone IV devices external memory interface support, refer to the *External Memory Interfaces in Cyclone IV Devices* chapter.

Pad Placement and DC Guidelines

You can use the Quartus II software to validate your pad and pin placement.

Pad Placement

Altera recommends that you create a Quartus II design, enter your device I/O assignments and compile your design to validate your pin placement. The Quartus II software checks your pin connections with respect to the I/O assignment and placement rules to ensure proper device operation. These rules depend on device density, package, I/O assignments, voltage assignments and other factors that are not fully described in this chapter.

For more information about how the Quartus II software checks I/O restrictions, refer to the *I/O Management* chapter in volume 2 of the *Quartus II Handbook*.

DC Guidelines

For the Quartus II software to automatically check for illegally placed pads according to the DC guidelines, set the DC current sink or source value to **Electromigration Current** assignment on each of the output pins that are connected to the external resistive load.

The programmable current strength setting has an impact on the amount of DC current that an output pin can source or sink. Determine if the current strength setting is sufficient for the external resistive load condition on the output pin.

Clock Pins Functionality

Cyclone IV clock pins have multiple purposes, as per listed:

- `CLK` pins—Input support for single-ended and voltage-referenced standards. For I/O standard support, refer to Table 6–3 on page 6–12.
- `DIFFCLK` pins—Input support for differential standards. For I/O standard support, refer to Table 6–3 on page 6–12. When used as `DIFFCLK` pins, DC or AC coupling can be used depending on the interface requirements and external termination is required. For more information, refer to "High-Speed I/O Standards Support" on page 6–27.
- `REFCLK` pins—Input support for high speed differential reference clocks used by the transceivers in Cyclone IV GX devices. For I/O support, coupling, and termination requirements, refer to Table 6–10 on page 6–28.

High-Speed I/O Interface

Cyclone IV E I/Os are separated into eight I/O banks, as shown in Figure 6–9 on page 6–17. Cyclone IV GX I/Os are separated into six user I/O banks with the left side of the device as the transceiver block, as shown in Figure 6–10 on page 6–18. Each bank has an independent power supply. True output drivers for LVDS, RSDS, mini-LVDS, and PPDS are on the right I/O banks. On the Cyclone IV E row I/O banks and the Cyclone IV GX right I/O banks, some of the differential pin pairs (`p` and `n` pins) of the true output drivers are not located on adjacent pins. In these cases, a power pin is located between the `p` and `n` pins. These I/O standards are also supported on all I/O banks using two single-ended output with the second output programmed as inverted, and an external resistor network. True input buffers for these I/O standards are supported on the top, bottom, and right I/O banks except for I/O bank 9.

Table 6–6 and Table 6–7 summarize which I/O banks support these I/O standards in the Cyclone IV device family.

Table 6–6. Differential I/O Standards Supported in Cyclone IV E I/O Banks

Differential I/O Standards	I/O Bank Location	External Resistor Network at Transmitter	Transmitter (TX)	Receiver (RX)
LVDS	1,2,5,6	Not Required	✓	✓
	All	Three Resistors		
RSDS	1,2,5,6	Not Required	✓	—
	3,4,7,8	Three Resistors		
	All	Single Resistor		
mini-LVDS	1,2,5,6	Not Required	✓	—
	All	Three Resistors		
PPDS	1,2,5,6	Not Required	✓	—
	All	Three Resistors		
BLVDS *(1)*	All	Single Resistor	✓	✓
LVPECL *(2)*	All	—	—	✓
Differential SSTL-2 *(3)*	All	—	✓	✓
Differential SSTL-18 *(3)*	All	—	✓	✓
Differential HSTL-18 *(3)*	All	—	✓	✓
Differential HSTL-15 *(3)*	All	—	✓	✓
Differential HSTL-12 *(3)*, *(4)*	All	—	✓	✓

Notes to Table 6–6:

(1) Transmitter and Receiver f_{MAX} depend on system topology and performance requirement.

(2) The LVPECL I/O standard is only supported on dedicated clock input pins.

(3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

(4) Differential HSTL-12 Class II is supported only in column I/O banks.

Table 6–7. Differential I/O Standards Supported in Cyclone IV GX I/O Banks

Differential I/O Standards	I/O Bank Location	External Resistor Network at Transmitter	Transmitter (TX)	Receiver (RX)
LVDS	5,6	Not Required	✓	✓
	3,4,5,6,7,8	Three Resistors		
RSDS	5,6	Not Required	✓	—
	3,4,7,8	Three Resistors		
	3,4,5,6,7,8	Single Resistor		
mini-LVDS	5,6	Not Required	✓	—
	3,4,5,6,7,8	Three Resistors		
PPDS	5,6	Not Required	✓	—
	3,4,5,6,7,8	Three Resistors		
BLVDS *(1)*	3,4,5,6,7,8	Single Resistor	✓	✓
LVPECL *(2)*	3,4,5,6,7,8	—	—	✓
Differential SSTL-2 *(3)*	3,4,5,6,7,8	—	✓	✓
Differential SSTL-18 *(3)*	3,4,5,6,7,8	—	✓	✓
Differential HSTL-18 *(3)*	3,4,5,6,7,8	—	✓	✓
Differential HSTL-15 *(3)*	3,4,5,6,7,8	—	✓	✓
Differential HSTL-12 *(3)*	4,5,6,7,8	—	✓	✓

Notes to Table 6–7:

(1) Transmitter and Receiver f_{MAX} depend on system topology and performance requirement.

(2) The LVPECL I/O standard is only supported on dedicated clock input pins.

(3) The differential SSTL-2, SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards are only supported on clock input pins and PLL output clock pins. PLL output clock pins do not support Class II interface type of differential SSTL-18, HSTL-18, HSTL-15, and HSTL-12 I/O standards.

You can use I/O pins and internal logic to implement a high-speed differential interface in Cyclone IV devices. Cyclone IV devices do not contain dedicated serialization or deserialization circuitry. Therefore, shift registers, internal phase-locked loops (PLLs), and I/O cells are used to perform serial-to-parallel conversions on incoming data and parallel-to-serial conversion on outgoing data. The differential interface data serializers and deserializers (SERDES) are automatically constructed in the core logic elements (LEs) with the Quartus II software ALTLVDS megafunction.

Table 6–8 and Table 6–9 summarize the total number of supported row and column differential channels in the Cyclone IV device family.

Table 6–8. Cyclone IV E I/O and Differential Channel Count

Device	EP4CE6			EP4CE10			EP4CE15					EP4CE22			EP4CE30		EP4CE40			EP4CE55			EP4CE75			EP4CE115	
Numbers of Differential Channels *(1)*,*(2)*	144-EQPF	256-UBGA	256-FBGA	144-EQPF	256-UBGA	256-FBGA	144-EQPF	164-MBGA	256-UBGA	256-FBGA	484-FBGA	144-EQPF	256-UBGA	256-FBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-UBGA	484-FBGA	780-FBGA	484-FBGA	780-FBGA
User I/O *(3)*	91	179	179	91	179	179	81	89	165	165	343	79	153	153	328	532	328	328	532	324	324	374	292	292	426	280	528
User I/O Banks	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8	8
LVDS *(4)*	8	23	23	8	23	23	6	8	21	21	67	7	20	20	60	112	60	60	112	62	62	70	54	54	79	50	103
Emulated LVDS *(5)*	13	43	43	13	43	43	12	13	32	32	70	10	32	32	64	112	64	64	112	70	70	90	56	56	99	53	127

Notes to Table 6–8:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as output only.

(2) For differential pad placement guidelines, refer to "Pad Placement" on page 6–22.

(3) The I/O pin count includes all GPIOs, dedicated clock pins, and dual-purpose configuration pins. Dedicated configuration pins are not included in the pin count.

(4) The true LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in row I/O banks 1, 2, 5, and 6.

(5) The emulated LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in column I/O banks 3, 4, 7, and 8.

Table 6–9. Cyclone IV GX I/O, Differential, and XCVRs Channel Count

Device	4CGX15		4CGX22		4CGX30			4CGX50		4CGX75		4CGX110			4CGX150		
Numbers of Differential Channels *(1)*, *(2)*	148-QFN	169-FBGA	169-FBGA	324-FBGA	169-FBGA	324-FBGA	484-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	484-FBGA	672-FBGA	896-FBGA	484-FBGA	672-FBGA	896-FBGA
User I/O *(3)*	72	72	72	150	72	150	290	290	310	290	310	270	393	475	270	393	475
User I/O banks	9 *(4)*	9 *(4)*	9 *(4)*	9 *(4)*	9 *(4)*	9 *(4)*	11 *(5)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*	11 *(5)*, *(6)*
LVDS *(7)*	9	9	9	16	9	16	45	45	51	45	51	38	52	63	38	52	63
Emulated LVDS *(8)*	16	16	16	48	16	48	85	85	89	85	89	82	129	157	82	129	157
XCVRs	2	2	2	4	2	4	4	4	8	4	8	4	8	8	4	8	8

Notes to Table 6–9:

(1) User I/O pins are used as inputs or outputs; clock input pins are used as inputs only; clock output pins are used as outputs only.

(2) For differential pad placement guidelines, refer to "Pad Placement" on page 6–22.

(3) The I/O pin count includes all GPIOs, dedicated clock pins, and dual-purpose configuration pins. Transceivers pins and dedicated configuration pins are not included in the pin count.

(4) Includes one configuration I/O bank and two dedicated clock input I/O banks for HSSI input reference clock.

(5) Includes one configuration I/O bank and four dedicated clock input I/O banks for HSSI input reference clock.

(6) Single-ended clock input support is available for dedicated clock input I/O banks 3B (pins `CLKIO20` and `CLKIO22`) and 8B (pins `CLKIO17` and `CLKIO19`).

(7) The true LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in right I/O banks 5 and 6.

(8) The emulated LVDS count includes all LVDS I/O pairs, differential clock input and clock output pins in column I/O banks 3, 4, 7, and 8.

High-Speed I/O Standards Support

This section provides information about the high-speed I/O standards and the HSSI input reference clock supported in Cyclone IV devices.

High Speed Serial Interface (HSSI) Input Reference Clock Support

Cyclone IV GX devices support the same I/O features for GPIOs with additional new features where current I/O banks 3A and 8A consist of dual-purpose clock input pins (`CLKIN`) and 3B and 8B consist of dedicated `CLKIN` that can be used to support the high-speed transceiver input reference clock (`REFCLK`) features on top of the general-purpose clock input function. I/O banks 3B and 8B are dedicated to high-speed transceiver input `REFCLK` only.

The EP4CGX15, EP4CGX22, and EP4CGX30 devices contain two pairs of `CLKIN/REFCLK` pins located in I/O banks 3A and 8A. I/O banks 3B and 8B are not available in EP4CGX15, EP4CGX22, and EP4CGX30 devices. The EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have a total of four pairs of `CLKIN/REFCLK` pins located in I/O banks 3A, 3B, 8A, and 8B. I/O banks 3B and 8B can also support single-ended clock inputs. For more information about the `CLKIN/REFCLK` pin location, refer to Figure 6–10 on page 6–18 and Figure 6–11 on page 6–19.

The `CLKIN/REFCLK` pins are powered by dedicated $V_{CC\_CLKIN3A}$, $V_{CC\_CLKIN3B}$, $V_{CC\_CLKIN8A}$, and $V_{CC\_CLKIN8B}$ power supplies separately in their respective I/O banks to avoid the different power level requirements in the same bank for GPIO.

Table 6–10. Cyclone IV GX HSSI REFCLK I/O Standard Support Using GPIO CLKIN Pins *(Note 1)*, *(2)*

I/O Standard	HSSI Protocol	Coupling	Termination	VCC_CLKIN Level		I/O Pin Type		
				Input	Output	Column I/O	Row I/O	Supported I/O Banks
LVDS	All	Differential AC (Need off chip resistor to restore V_{CM})	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
LVPECL	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
1.2V, 1.5V, 3.3V PCML	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
	All		Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B
HCSL	PCIe	Differential DC	Off chip	2.5V	Not supported	Yes	No	3A, 3B, 8A, 8B

Notes to Table 6–10:

(1) The EP4CGX15, EP4CGX22, and EP4CGX30 devices have two pairs of dedicated clock input pins in banks 3A and 8A for HSSI input reference clock. I/O banks 3B and 8B are not available in EP4CGX15, EP4CGX22, and EP4CGX30 devices.

(2) The EP4CGX50, EP4CGX75, EP4CGX110, and EP4CGX150 devices have four pairs of dedicated clock input pins in banks 3A, 3B, 8A, and 8B for HSSI input or single-ended clock input.

For more information about the AC-coupled termination scheme for the HSSI reference clock, refer to the *Cyclone IV Transceivers Architecture* chapter.

LVDS I/O Standard Support in Cyclone IV Devices

The LVDS I/O standard is a high-speed, low-voltage swing, low power, and GPIO interface standard. Cyclone IV devices meet the ANSI/TIA/EIA-644 standard with the following exceptions:

- The maximum differential output voltage (V_{OD}) is increased to 600 mV. The maximum V_{OD} for ANSI specification is 450 mV.
- The input voltage range is reduced to the range of 1.0 V to 1.6 V, 0.5 V to 1.85 V, or 0 V to 1.8 V based on different frequency ranges. The ANSI/TIA/EIA-644 specification supports an input voltage range of 0 V to 2.4 V.

For LVDS I/O standard electrical specifications in Cyclone IV devices, refer to the *Cyclone IV Device Datasheet* chapter.

Designing with LVDS

Cyclone IV I/O banks support the LVDS I/O standard. The Cyclone IV GX right I/O banks support true LVDS transmitters while the Cyclone IV E left and right I/O banks support true LVDS transmitters. On the top and bottom I/O banks, the emulated LVDS transmitters are supported using two single-ended output buffers with external resistors. One of the single-ended output buffers is programmed to have opposite polarity. The LVDS receiver requires an external 100-Ω termination resistor between the two signals at the input buffer.

Figure 6–12 shows a point-to-point LVDS interface using Cyclone IV devices true LVDS output and input buffers.

Figure 6–12. Cyclone IV Devices LVDS Interface with True Output Buffer on the Right I/O Banks

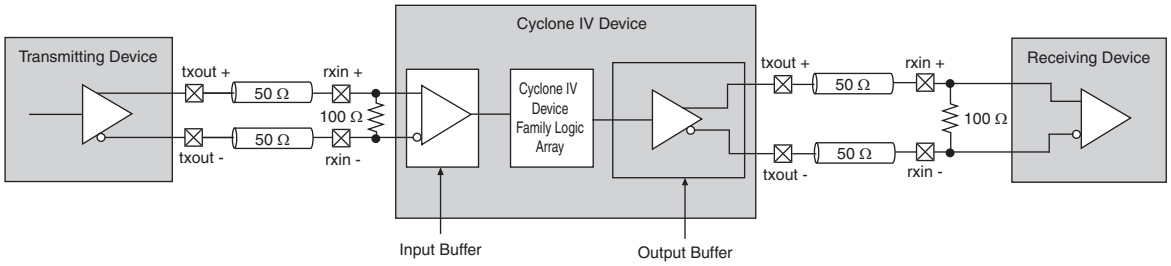
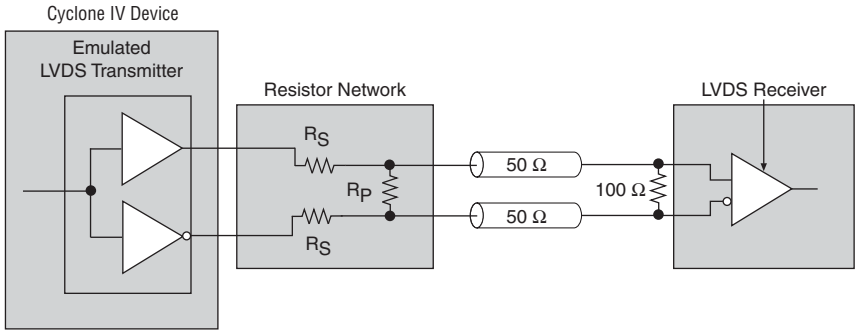


Figure 6–13 shows a point-to-point LVDS interface with Cyclone IV devices LVDS using two single-ended output buffers and external resistors.

Figure 6–13. LVDS Interface with External Resistor Network on the Top and Bottom I/O Banks *(Note 1)*



Note to Figure 6–13:

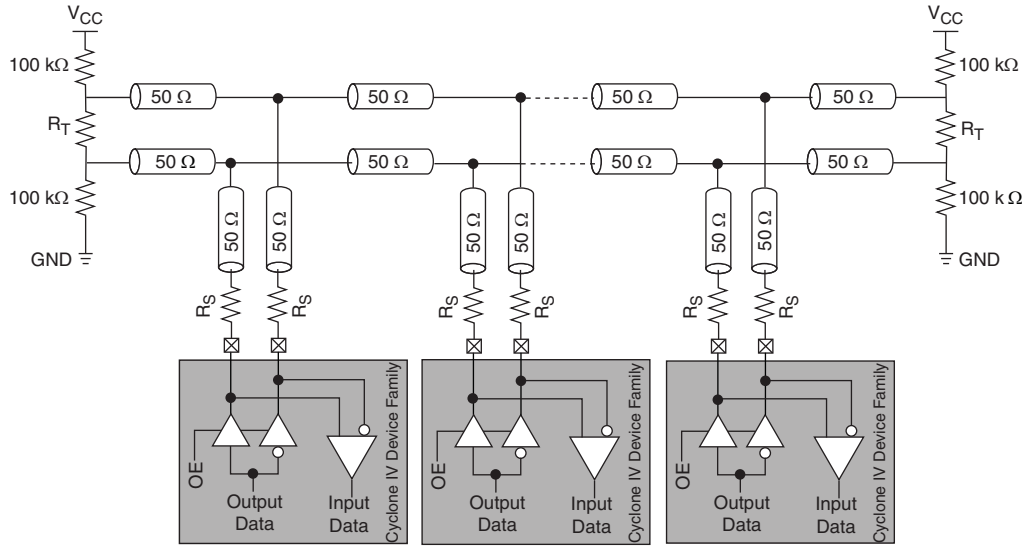
(1) R_S = 120 Ω. R_P = 170 Ω.

BLVDS I/O Standard Support in Cyclone IV Devices

The BLVDS I/O standard is a high-speed differential data transmission technology that extends the benefits of standard point-to-point LVDS to multipoint configuration that supports bidirectional half-duplex communication. BLVDS differs from standard LVDS by providing a higher drive to achieve similar signal swings at the receiver while loaded with two terminations at both ends of the bus.

Figure 6–14 shows a typical BLVDS topology with multiple transmitter and receiver pairs.

Figure 6–14. BLVDS Topology with Cyclone IV Devices Transmitters and Receivers



The BLVDS I/O standard is supported on the top, bottom, and right I/O banks of Cyclone IV devices. The BLVDS transmitter uses two single-ended output buffers with the second output buffer programmed as inverted, while the BLVDS receiver uses a true LVDS input buffer. The transmitter and receiver share the same pins. An output-enabled (OE) signal is required to tristate the output buffers when the LVDS input buffer receives a signal.

For more information, refer to the *Cyclone IV Device Datasheet* chapter.

Designing with BLVDS

The BLVDS bidirectional communication requires termination at both ends of the bus in BLVDS. The termination resistor (R_T) must match the bus differential impedance, which in turn depends on the loading on the bus. Increasing the load decreases the bus differential impedance. With termination at both ends of the bus, termination is not required between the two signals at the input buffer. A single series resistor (R_S) is required at the output buffer to match the output buffer impedance to the transmission line impedance. However, this series resistor affects the voltage swing at the input buffer. The maximum data rate achievable depends on many factors.

Altera recommends that you perform simulation using the IBIS model while considering factors such as bus loading, termination values, and output and input buffer location on the bus to ensure that the required performance is achieved.

For more information about BLVDS interface support in Altera devices, refer to *AN 522: Implementing Bus LVDS Interface in Supported Altera Device Families*.

RSDS, Mini-LVDS, and PPDS I/O Standard Support in Cyclone IV Devices

The RSDS, mini-LVDS, and PPDS I/O standards are used in chip-to-chip applications between the timing controller and the column drivers on the display panels such as LCD monitor panels and LCD televisions. Cyclone IV devices meet the National Semiconductor Corporation RSDS Interface Specification, Texas Instruments mini-LVDS Interface Specification, and National Semiconductor Corporation PPDS Interface Specification to support RSDS, mini-LVDS and PPDS output standards, respectively.

For Cyclone IV devices RSDS, mini-LVDS, and PPDS output electrical specifications, refer to the *Cyclone IV Device Datasheet* chapter.

For more information about the RSDS I/O standard, refer to the RSDS specification from the National Semiconductor website (www.national.com).

Designing with RSDS, Mini-LVDS, and PPDS

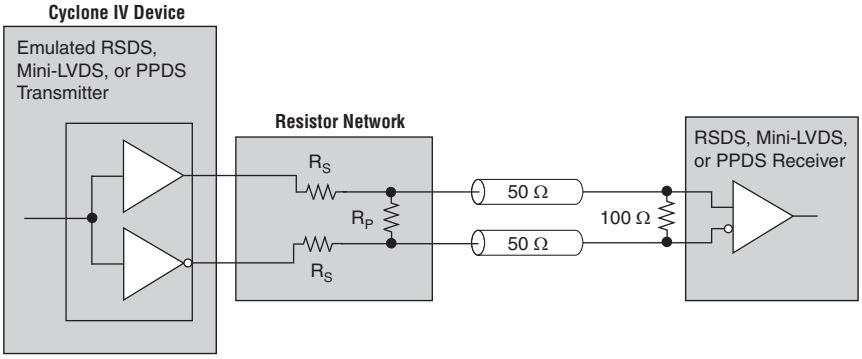
Cyclone IV I/O banks support RSDS, mini-LVDS, and PPDS output standards. The right I/O banks support true RSDS, mini-LVDS, and PPDS transmitters. On the top and bottom I/O banks, RSDS, mini-LVDS, and PPDS transmitters are supported using two single-ended output buffers with external resistors. The two single-ended output buffers are programmed to have opposite polarity.

Figure 6–15 shows an RSDS, mini-LVDS, or PPDS interface with a true output buffer.

Figure 6–15. Cyclone IV Devices RSDS, Mini-LVDS, or PPDS Interface with True Output Buffer on the Right I/O Banks

Figure 6–16 shows an RSDS, mini-LVDS, or PPDS interface with two single-ended output buffers and external resistors.

Figure 6–16. RSDS, Mini-LVDS, or PPDS Interface with External Resistor Network on the Top and Bottom I/O Banks *(Note 1)*



Note to Figure 6–16:

(1) R_S and R_P values are pending characterization.

A resistor network is required to attenuate the output voltage swing to meet RSDS, mini-LVDS, and PPDS specifications when using emulated transmitters. You can modify the resistor network values to reduce power or improve the noise margin.

The resistor values chosen must satisfy Equation 6–1.

Equation 6–1. Resistor Network

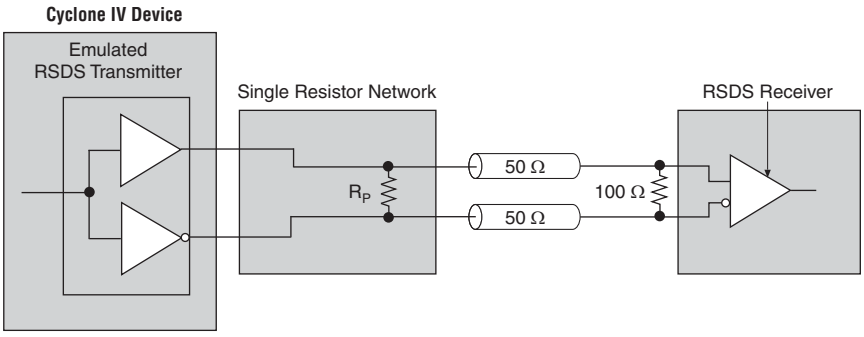
$$\frac{R_S \times \frac{R_P}{2}}{R_S + \frac{R_P}{2}} = 50\ \Omega$$

Altera recommends that you perform simulations using Cyclone IV devices IBIS models to validate that custom resistor values meet the RSDS, mini-LVDS, or PPDS requirements.

It is possible to use a single external resistor instead of using three resistors in the resistor network for an RSDS interface, as shown in Figure 6–17. The external single-resistor solution reduces the external resistor count while still achieving the required signaling level for RSDS. However, the performance of the single-resistor solution is lower than the performance with the three-resistor network.

Figure 6–17 shows the RSDS interface with a single resistor network on the top and bottom I/O banks.

Figure 6–17. RSDS Interface with Single Resistor Network on the Top and Bottom I/O Banks *(Note 1)*



Note to Figure 6–17:

(1) R_P value is pending characterization.

LVPECL I/O Support in Cyclone IV Devices

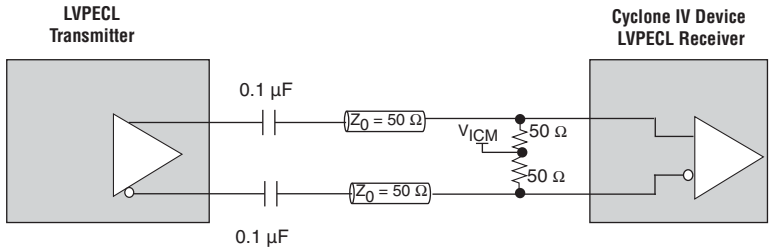
The LVPECL I/O standard is a differential interface standard that requires a 2.5-V V_{CCIO}. This standard is used in applications involving video graphics, telecommunications, data communications, and clock distribution. Cyclone IV devices support the LVPECL input standard at the dedicated clock input pins only. The LVPECL receiver requires an external 100-Ω termination resistor between the two signals at the input buffer.

For the LVPECL I/O standard electrical specification, refer to the *Cyclone IV Device Datasheet* chapter.

AC coupling is required when the LVPECL common mode voltage of the output buffer is higher than the Cyclone IV devices LVPECL input common mode voltage.

Figure 6–18 shows the AC-coupled termination scheme. The 50-Ω resistors used at the receiver are external to the device. DC-coupled LVPECL is supported if the LVPECL output common mode voltage is in the Cyclone IV devices LVPECL input buffer specification (refer to Figure 6–19).

Figure 6–18. LVPECL AC-Coupled Termination *(Note 1)*

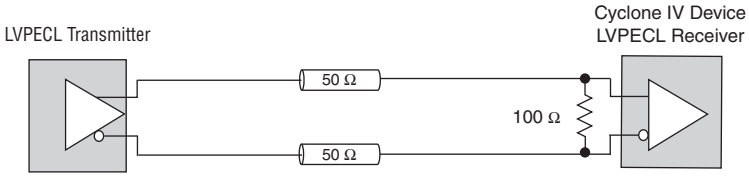


Note to Figure 6–18:

(1) The LVPECL AC-coupled termination is applicable only when an Altera FPGA transmitter is used.

Figure 6–19 shows the LVPECL DC-coupled termination.

Figure 6–19. LVPECL DC-Coupled Termination *(Note 1)*



Note to Figure 6–19:

(1) The LVPECL DC-coupled termination is applicable only when an Altera FPGA transmitter is used.

Differential SSTL I/O Standard Support in Cyclone IV Devices

The differential SSTL I/O standard is a memory-bus standard used for applications such as high-speed DDR SDRAM interfaces. Cyclone IV devices support differential SSTL-2 and SSTL-18 I/O standards. The differential SSTL I/O standard requires two differential inputs with an external reference voltage (VREF) as well as an external termination voltage (VTT) of 0.5 × V_{CCIO} to which termination resistors are connected. The differential SSTL output standard is only supported at PLL#_CLKOUT pins using two single-ended SSTL output buffers (PLL#_CLKOUTp and PLL#_CLKOUTn), with the second output programmed to have opposite polarity. The differential SSTL input standard is supported on the GCLK pins only, treating differential inputs as two single-ended SSTL and only decoding one of them.

For differential SSTL electrical specifications, refer to "Differential I/O Standard Termination" on page 6–15 and the *Cyclone IV Device Datasheet* chapter.

Figure 6–8 on page 6–15 shows the differential SSTL Class I and Class II interface.

Differential HSTL I/O Standard Support in Cyclone IV Devices

The differential HSTL I/O standard is used for the applications designed to operate in 0 V to 1.2 V, 0 V to 1.5 V, or 0 V to 1.8 V HSTL logic switching range. Cyclone IV devices support differential HSTL-18, HSTL-15, and HSTL-12 I/O standards. The differential HSTL input standard is available on GCLK pins only, treating the differential inputs as two single-ended HSTL and only decoding one of them. The differential HSTL output standard is only supported at the PLL#_CLKOUT pins using two single-ended HSTL output buffers (PLL#_CLKOUT*p* and PLL#_CLKOUT*n*), with the second output programmed to have opposite polarity. The standard requires two differential inputs with an external reference voltage (VREF), as well as an external termination voltage (VTT) of 0.5 × V_{CCIO} to which termination resistors are connected.

For differential HSTL signaling characteristics, refer to "Differential I/O Standard Termination" on page 6–15 and the *Cyclone IV Device Datasheet* chapter.

Figure 6–7 on page 6–15 shows the differential HSTL Class I and Class II interface.

True Output Buffer Feature

Cyclone IV devices true differential transmitters offer programmable pre-emphasis—you can turn it on or off. The default setting is on.

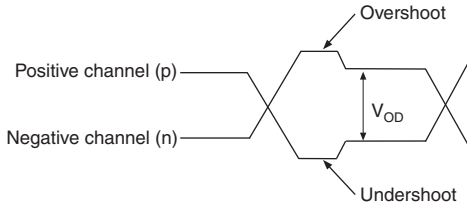
Programmable Pre-Emphasis

The programmable pre-emphasis boosts the high frequencies of the output signal to compensate the frequency-dependant attenuation of the transmission line to maximize the data eye opening at the far-end receiver. Without pre-emphasis, the output current is limited by the V_{OD} specification and the output impedance of the transmitter. At high frequency, the slew rate may not be fast enough to reach full V_{OD} before the next edge; this may lead to pattern-dependent jitter. With pre-emphasis, the output current is momentarily boosted during switching to increase the output slew rate. The overshoot produced by this extra switching current is different from the overshoot caused by signal reflection. This overshoot happens only during switching, and does not produce ringing.

The Quartus II software allows two settings for programmable pre-emphasis control—**0** and **1**, in which **0** is pre-emphasis off and **1** is pre-emphasis on. The default setting is **1**. The amount of pre-emphasis needed depends on the amplification of the high-frequency components along the transmission line. You must adjust the setting to suit your designs, as pre-emphasis decreases the amplitude of the low-frequency component of the output signal.

Figure 6–20 shows the differential output signal with pre-emphasis.

Figure 6–20. The Output Signal with Pre-Emphasis



High-Speed I/O Timing

This section discusses the timing budget, waveforms, and specifications for source-synchronous signaling in Cyclone IV devices. Timing for source-synchronous signaling is based on skew between the data and clock signals.

High-speed differential data transmission requires timing parameters provided by IC vendors and requires you to consider the board skew, cable skew, and clock jitter. This section provides information about high-speed I/O standards timing parameters in Cyclone IV devices.

Table 6–11 defines the parameters of the timing diagram shown in Figure 6–21.

Table 6–11. High-Speed I/O Timing Definitions

Parameter	Symbol	Description
Transmitter channel-to-channel skew *(1)*	TCCS	The timing difference between the fastest and slowest output edges, including t_{CO} variation and clock skew. The clock is included in the TCCS measurement.
Sampling window	SW	The period of time during which the data must be valid in order for you to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window. $T_{SW} = T_{SU} + T_{hd}$ + PLL jitter.
Time unit interval	TUI	The TUI is the data-bit timing budget allowed for skew, propagation delays, and data sampling window.
Receiver input skew margin	RSKM	RSKM is defined by the total margin left after accounting for the sampling window and TCCS. The RSKM equation is: $RSKM = \frac{(TUI - SW - TCCS)}{2}$
Input jitter tolerance (peak-to-peak)	—	Allowed input jitter on the input clock to the PLL that is tolerable while maintaining PLL lock.
Output jitter (peak-to-peak)	—	Peak-to-peak output jitter from the PLL.

Note to Table 6–11:

(1) The TCCS specification applies to the entire bank of differential I/O as long as the SERDES logic is placed in the logic array block (LAB) adjacent to the output pins.

Figure 6–21. High-Speed I/O Timing Diagram

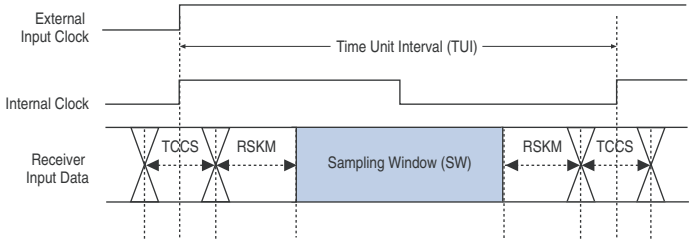
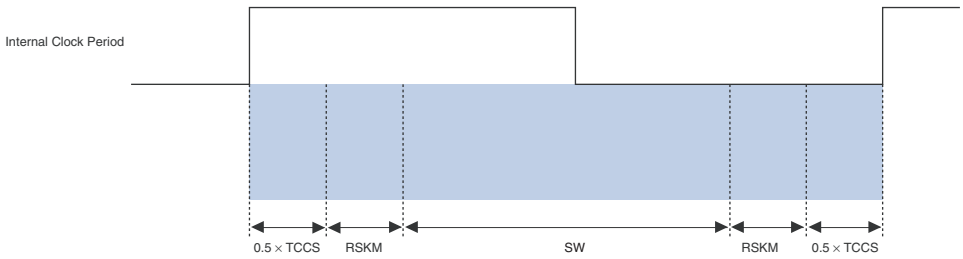


Figure 6–22 shows the Cyclone IV devices high-speed I/O timing budget.

Figure 6–22. Cyclone IV Devices High-Speed I/O Timing Budget *(Note 1)*



Note to Figure 6–22:

(1) The equation for the high-speed I/O timing budget is:
Period = 0.5 × TCCS + RSKM + SW + RSKM + 0.5 × TCCS.

For more information, refer to the *Cyclone IV Device Datasheet* chapter.

Design Guidelines

This section provides guidelines for designing with Cyclone IV devices.

Differential Pad Placement Guidelines

To maintain an acceptable noise level on the V_{CCIO} supply, you must observe some restrictions on the placement of single-ended I/O pins in relation to differential pads.

For guidelines on placing single-ended pads with respect to differential pads in Cyclone IV devices, refer to "Pad Placement and DC Guidelines" on page 6–22.

Board Design Considerations

This section explains how to achieve the optimal performance from a Cyclone IV I/O interface and ensure first-time success in implementing a functional design with optimal signal quality. You must consider the critical issues of controlled impedance of traces and connectors, differential routing, and termination techniques to get the best performance from Cyclone IV devices.

Use the following general guidelines to improve signal quality:

- Base board designs on controlled differential impedance. Calculate and compare all parameters, such as trace width, trace thickness, and the distance between two differential traces.
- Maintain equal distance between traces in differential I/O standard pairs as much as possible. Routing the pair of traces close to each other maximizes the common-mode rejection ratio (CMRR).
- Longer traces have more inductance and capacitance. These traces must be as short as possible to limit signal integrity issues.
- Place termination resistors as close to receiver input pins as possible.
- Use surface mount components.
- Avoid 90° corners on board traces.
- Use high-performance connectors.
- Design backplane and card traces so that trace impedance matches the impedance of the connector and termination.
- Keep an equal number of vias for both signal traces.
- Create equal trace lengths to avoid skew between signals. Unequal trace lengths result in misplaced crossing points and decrease system margins as the TCCS value increases.
- Limit vias because they cause discontinuities.
- Keep switching transistor-to-transistor logic (TTL) signals away from differential signals to avoid possible noise coupling.
- Do not route TTL clock signals to areas under or above the differential signals.
- Analyze system-level signals.

For PCB layout guidelines, refer to *AN 224: High-Speed Board Layout Guidelines* and *AN 315: Guidelines for Designing High-Speed FPGA PCBs*.

Software Overview

Cyclone IV devices high-speed I/O system interfaces are created in core logic by a Quartus II software megafunction because they do not have a dedicated circuit for the SERDES. Cyclone IV devices use the I/O registers and LE registers to improve the timing performance and support the SERDES. The Quartus II software allows you to design your high-speed interfaces using ALTLVDS megafunction. This megafunction implements either a high-speed deserializer receiver or a high-speed serializer transmitter. There is a list of parameters in the ALTLVDS megafunction that you can set to customize your SERDES based on your design requirements. The megafunction is optimized to use Cyclone IV devices resources to create high-speed I/O interfaces in the most effective manner.

When you use Cyclone IV devices with the ALTLVDS megafunction, the interface always sends the MSB of your parallel data first.

For more details about designing your high-speed I/O systems interfaces using the ALTLVDS megafunction, refer to the *ALTLVDS Megafunction User Guide* and the *Quartus II Handbook*.

Document Revision History

Table 6–12 lists the revision history for this chapter.

Table 6–12. Document Revision History

Date	Version	Changes Made
December 2010	2.2	■ Updated for the Quartus II software version 10.1 release. ■ Added Cyclone IV E new device package information. ■ Added "Clock Pins Functionality" section. ■ Updated Table 6–4 and Table 6–8. ■ Minor text edits.
July 2010	2.1	■ Updated "Cyclone IV I/O Elements", "Programmable Pull-Up Resistor", "I/O Banks", "High-Speed I/O Interface", and "Designing with BLVDS" sections. ■ Updated Table 6–6 and Table 6–7. ■ Updated Figure 6–19.
February 2010	2.0	■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release. ■ Updated Table 6–2, Table 6–3, and Table 6–10. ■ Updated "I/O Banks" section. ■ Added Figure 6–9. ■ Updated Figure 6–10 and Figure 6–11. ■ Added Table 6–4, Table 6–6, and Table 6–8.
November 2009	1.0	Initial release.

7. External Memory Interfaces in Cyclone IV Devices

CYIV-51007-2.2

This chapter describes the memory interface pin support and the external memory interface features of Cyclone® IV devices.

In addition to an abundant supply of on-chip memory, Cyclone IV devices can easily interface with a broad range of external memory devices, including DDR2 SDRAM, DDR SDRAM, and QDR II SRAM. External memory devices are an important system component of a wide range of image processing, storage, communications, and general embedded applications.

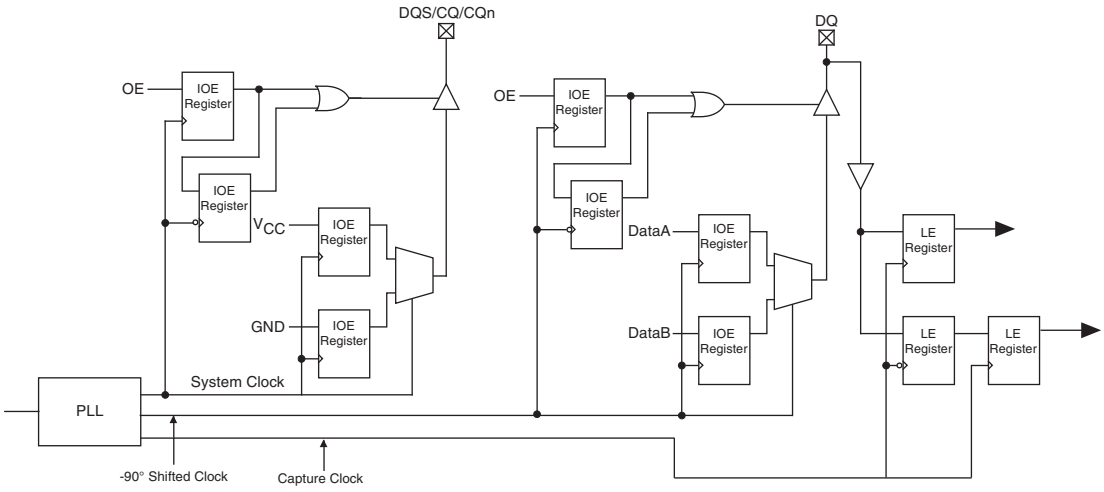
Altera recommends that you construct all DDR2 or DDR SDRAM external memory interfaces using the Altera® ALTMEMPHY megafunction. You can implement the controller function using the Altera DDR2 or DDR SDRAM memory controllers, third-party controllers, or a custom controller for unique application needs. Cyclone IV devices support QDR II interfaces electrically, but Altera does not supply controller or physical layer (PHY) megafunctions for QDR II interfaces.

This chapter includes the following sections:

For more information about supported maximum clock rate, device and pin planning, IP implementation, and device termination, refer to the *External Memory Interface Handbook*.

Figure 7–1 shows the block diagram of a typical external memory interface data path in Cyclone IV devices.

Figure 7–1. Cyclone IV Devices External Memory Data Path *(Note 1)*



Note to Figure 7–1:

(1) All clocks shown here are global clocks.

For more information about implementing complete external memory interfaces, refer to the *External Memory Interface Handbook*.

Cyclone IV Devices Memory Interfaces Pin Support

Cyclone IV devices use data (DQ), data strobe (DQS), clock, command, and address pins to interface with external memory. Some memory interfaces use the data mask (DM) or byte write select (BWS#) pins to enable data masking. This section describes how Cyclone IV devices support all these different pins.

For more information about pin utilization, refer to *Volume 2: Device, Pin, and Board Layout Guidelines* of the *External Memory Interface Handbook*.

Data and Data Clock/Strobe Pins

Cyclone IV data pins for external memory interfaces are called D for write data, Q for read data, or DQ for shared read and write data pins. The read-data strobes or read clocks are called DQS pins. Cyclone IV devices support both bidirectional data strobes and unidirectional read clocks. Depending on the external memory standard, the DQ and DQS are bidirectional signals (in DDR2 and DDR SDRAM) or unidirectional signals (in QDR II SRAM). Connect the bidirectional DQ data signals to the same Cyclone IV devices DQ pins. For unidirectional `D` or `Q` signals, connect the read-data signals to a group of DQ pins and the write-data signals to a different group of DQ pins.

In QDR II SRAM, the Q read-data group must be placed at a different V_{REF} bank location from the D write-data group, command, or address pins.

In Cyclone IV devices, DQS is used only during write mode in DDR2 and DDR SDRAM interfaces. Cyclone IV devices ignore DQS as the read-data strobe because the PHY internally generates the read capture clock for read mode. However, you must connect the DQS pin to the DQS signal in DDR2 and DDR SDRAM interfaces, or to the `CQ` signal in QDR II SRAM interfaces.

Cyclone IV devices do not support differential strobe pins, which is an optional feature in the DDR2 SDRAM device.

When you use the Altera Memory Controller MegaCore® function, the PHY is instantiated for you. For more information about the memory interface data path, refer to the *External Memory Interface Handbook*.

ALTMEMPHY is a self-calibrating megafunction, enhanced to simplify the implementation of the read-data path in different memory interfaces. The auto-calibration feature of ALTMEMPHY provides ease-of-use by optimizing clock phases and frequencies across process, voltage, and temperature (PVT) variations. You can save on the global clock resources in Cyclone IV devices through the ALTMEMPHY megafunction because you are not required to route the DQS signals on the global clock buses (because DQS is ignored for read capture). Resynchronization issues do not arise because no transfer occurs from the memory domain clock (DQS) to the system domain for capturing data DQ.

All I/O banks in Cyclone IV devices can support DQ and DQS signals with DQ-bus modes of ×8, ×9, ×16, ×18, ×32, and ×36 except Cyclone IV GX devices that do not support left I/O bank interface. DDR2 and DDR SDRAM interfaces use ×8 mode DQS group regardless of the interface width. For a wider interface, you can use multiple ×8 DQ groups to achieve the desired width requirement.

In the ×9, ×18, and ×36 modes, a pair of complementary DQS pins (CQ and CQ#) drives up to 9, 18, or 36 DQ pins, respectively, in the group, to support one, two, or four parity bits and the corresponding data bits. The ×9, ×18, and ×36 modes support the QDR II memory interface. CQ# is the inverted read-clock signal that is connected to the complementary data strobe (DQS or CQ#) pin. You can use any unused DQ pins as regular user I/O pins if they are not used as memory interface signals.

For more information about unsupported DQS and DQ groups of the Cyclone IV transceivers that run at ≥2.97 Gbps data rate, refer to the *Cyclone IV Device Family Pin Connection Guidelines*.

Table 7–1 lists the number of DQS or DQ groups supported on each side of the Cyclone IV GX device.

Table 7–1. Cyclone IV GX Device DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 1 of 2)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP4CGX15	148-pin QFN	Right	1	0	0	0	—	—
		Top *(2)*	1	0	0	0	—	—
		Bottom *(3)*	1	0	0	0	—	—
	169-pin FBGA	Right	1	0	0	0	—	—
		Top *(2)*	1	0	0	0	—	—
		Bottom *(3)*	1	0	0	0	—	—
EP4CGX22 EP4CGX30	169-pin FBGA	Right	1	0	0	0	—	—
		Top *(2)*	1	0	0	0	—	—
		Bottom *(3)*	1	0	0	0	—	—
	324-pin FBGA	Right	2	2	1	1	—	—
		Top	2	2	1	1	—	—
		Bottom	2	2	1	1	—	—
	484-pin FBGA *(4)*	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
EP4CGX50 EP4CGX75	484-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	672-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1

Table 7–1. Cyclone IV GX Device DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 2 of 2)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP4CGX110 EP4CGX150	484-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	672-pin FBGA	Right	4	2	2	2	1	1
		Top	4	2	2	2	1	1
		Bottom	4	2	2	2	1	1
	896-pin FBGA	Right	6	2	2	2	1	1
		Top	6	2	3	3	1	1
		Bottom	6	2	3	3	1	1

Notes to Table 7–1:

(1) The number of the DQS/DQ group is still preliminary.

(2) Some of the DQ pins can be used as RUP and RDN pins. You cannot use these groups if you are using these pins as RUP and RDN pins for OCT calibration.

(3) Some of the DQ pins can be used as RUP pins while the DM pins can be used as RDN pins. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.

(4) Only available for EP4CGX30 device.

Table 7–2 lists the number of DQS or DQ groups supported on each side of the Cyclone IV E device.

Table 7–2. Cyclone IV E Device DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 1 of 3)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP4CE6 EP4CE10	144-pin EQFP	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Bottom *(2)*, *(4)*	1	0	0	0	—	—
		Top *(2)*, *(5)*	1	0	0	0	—	—
	256-pin UBGA	Left *(2)*	1	1	0	0	—	—
		Right *(3)*	1	1	0	0	—	—
		Bottom	2	2	1	1	—	—
		Top	2	2	1	1	—	—
	256-pin FBGA	Left *(2)*	1	1	0	0	—	—
		Right *(3)*	1	1	0	0	—	—
		Bottom	2	2	1	1	—	—
		Top	2	2	1	1	—	—

Table 7–2. Cyclone IV E Device DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 2 of 3)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP4CE15	144-pin EQFP	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Bottom*(2)*, *(4)*	1	0	0	0	—	—
		Top*(2)*, *(5)*	1	0	0	0	—	—
	164-pin MBGA	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Bottom*(2)*, *(4)*	1	0	0	0	—	—
		Top*(2)*, *(5)*	1	0	0	0	—	—
	256-pin UBGA	Left*(2)*	1	1	0	0	—	—
		Right*(3)*	1	1	0	0	—	—
		Bottom	2	2	1	1	—	—
		Top	2	2	1	1	—	—
	256-pin FBGA	Left*(2)*	1	1	0	0	—	—
		Right*(3)*	1	1	0	0	—	—
		Bottom	2	2	1	1	—	—
		Top	2	2	1	1	—	—
	484-pin FBGA	Left	4	4	2	2	1	1
		Right	4	4	2	2	1	1
		Bottom	4	4	2	2	1	1
		Top	4	4	2	2	1	1
EP4CE22	144-pin EQFP	Left	0	0	0	0	—	—
		Right	0	0	0	0	—	—
		Bottom*(2)*, *(4)*	1	0	0	0	—	—
		Top*(2)*, *(5)*	1	0	0	0	—	—
	256-pin UBGA	Left*(2)*	1	1	0	0	—	—
		Right*(3)*	1	1	0	0	—	—
		Bottom	2	2	1	1	—	—
		Top	2	2	1	1	—	—
	256-pin FBGA	Left*(2)*	1	1	0	0	—	—
		Right*(3)*	1	1	0	0	—	—
		Bottom	2	2	1	1	—	—
		Top	2	2	1	1	—	—

Table 7–2. Cyclone IV E Device DQS and DQ Bus Mode Support for Each Side of the Device *(Note 1)* (Part 3 of 3)

Device	Package	Side	Number ×8 Groups	Number ×9 Groups	Number ×16 Groups	Number ×18 Groups	Number ×32 Groups	Number ×36 Groups
EP4CE30 EP4CE115	484-pin FBGA	Left	4	4	2	2	1	1
		Right	4	4	2	2	1	1
		Bottom	4	4	2	2	1	1
		Top	4	4	2	2	1	1
	780-pin FBGA	Left	4	4	2	2	1	1
		Right	4	4	2	2	1	1
		Bottom	6	6	2	2	1	1
		Top	6	6	2	2	1	1
EP4CE40 EP4CE55 EP4CE75	484-pin UBGA	Left	4	4	2	2	1	1
		Right	4	4	2	2	1	1
		Bottom	4	4	2	2	1	1
		Top	4	4	2	2	1	1
	484-pin FBGA	Left	4	4	2	2	1	1
		Right	4	4	2	2	1	1
		Bottom	4	4	2	2	1	1
		Top	4	4	2	2	1	1
	780-pin FBGA	Left	4	4	2	2	1	1
		Right	4	4	2	2	1	1
		Bottom	6	6	2	2	1	1
		Top	6	6	2	2	1	1

Notes to Table 7–2:

(1) The number of the DQS/DQ group is still preliminary.

(2) Some of the DQ pins can be used as RUP and RDN pins. You cannot use these groups if you are using these pins as RUP and RDN pins for OCT calibration.

(3) Some of the DQ pins can be used as RUP pins while the DM pins can be used as RDN pins. You cannot use these groups if you are using the RUP and RDN pins for OCT calibration.

(4) There is no DM pin support for these groups.

(5) PLLCLKOUT3n and PLLCLKOUT3p pins are shared with the DQ or DM pins to gain ×8 DQ group. You cannot use these groups if you are using PLLCLKOUT3n and PLLCLKOUT3p.

For more information about device package outline, refer to the Device Packaging Specifications webpage.

DQS pins are listed in the Cyclone IV pin tables as DQSXY, in which X indicates the DQS grouping number and Y indicates whether the group is located on the top (T), bottom (B), or right (R) side of the device. Similarly, the corresponding DQ pins are marked as DQXY, in which the X denotes the DQ grouping number and Y denotes whether the group is located on the top (T), bottom (B), or right (R) side of the device. For example, DQS2T indicates a DQS pin belonging to group 2, located on the top side of the device. Similarly, the DQ pins belonging to that group is shown as DQ2T.

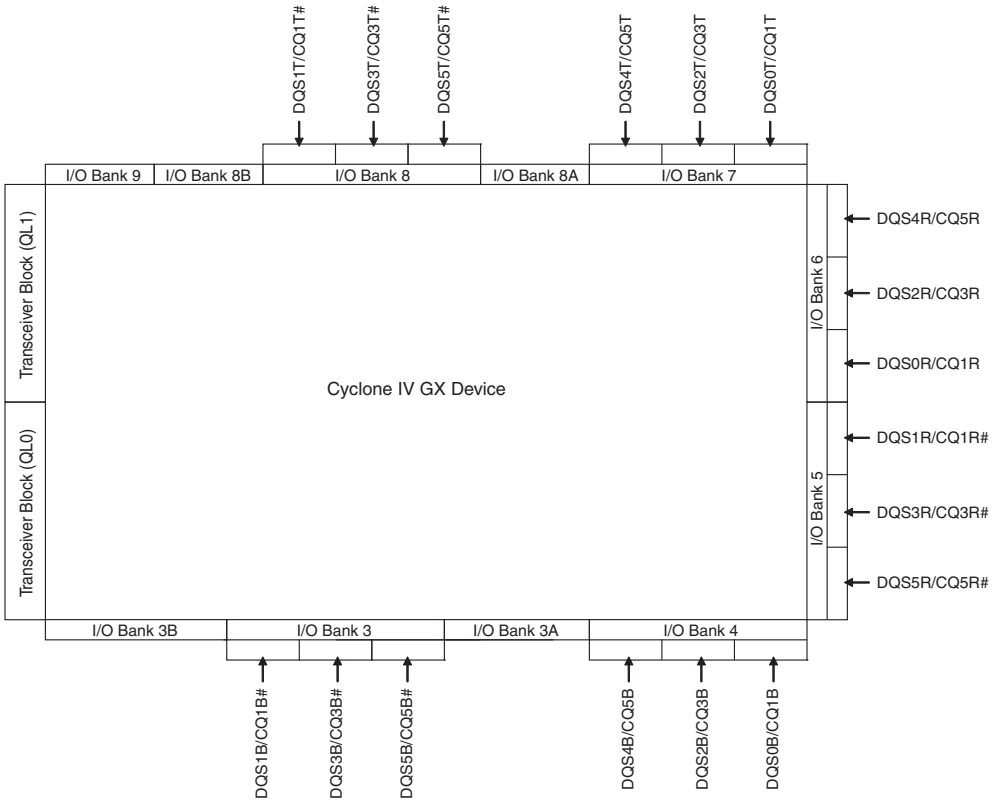
Each DQ group is associated with its corresponding DQS pins, as defined in the Cyclone IV pin tables. For example:

- For DDR2 or DDR SDRAM, ×8 DQ group `DQ3B[7..0]` pins are associated with the `DQS3B` pin (same 3B group index)
- For QDR II SRAM, ×9 Q read-data group `DQ3T[8..0]` pins are associated with `DQS0T/CQ0T` and `DQS1T/CQ0T#` pins (same 0T group index)

The Quartus® II software issues an error message if a DQ group is not placed properly with its associated DQS.

Figure 7–2 shows the location and numbering of the DQS, DQ, or CQ# pins in the Cyclone IV GX I/O banks.

Figure 7–2. DQS, CQ, or CQ# Pins in Cyclone IV GX I/O Banks *(Note 1)*



Note to Figure 7–2:

(1) The DQS, CQ, or CQ# pin locations in this diagram apply to all packages in Cyclone IV GX devices except devices in 148-pin QFP, 169-pin FBGA, and 324-pin FBGA.

Figure 7–3 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV GX device in the 324-pin FBGA package only.

Figure 7–3. DQS, CQ, or CQ# Pins for Cyclone IV GX Devices in the 324-Pin FBGA Package

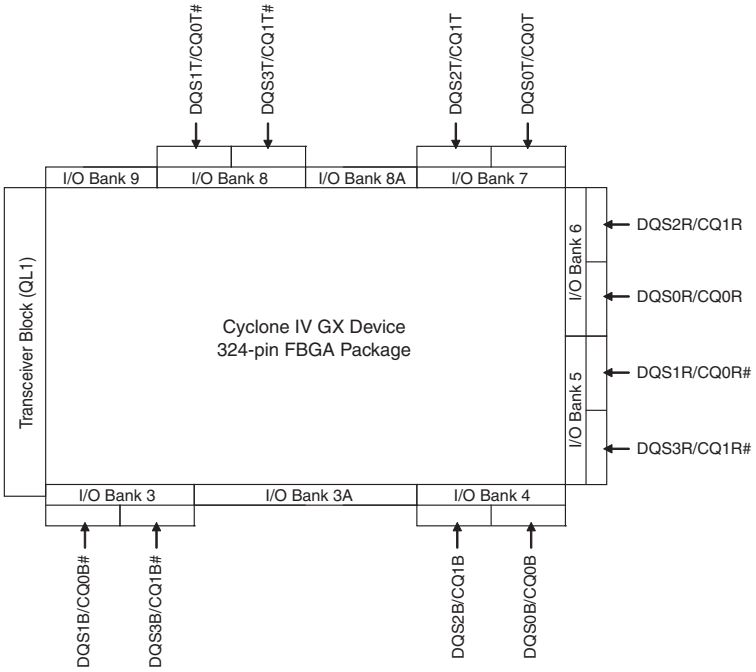


Figure 7–4 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV GX device in the 148-pin QFP and 169-pin FBGA packages.

Figure 7–4. DQS, CQ, or CQ# Pins for Cyclone IV GX Devices in the 148-Pin QFP and 169-Pin FBGA Packages

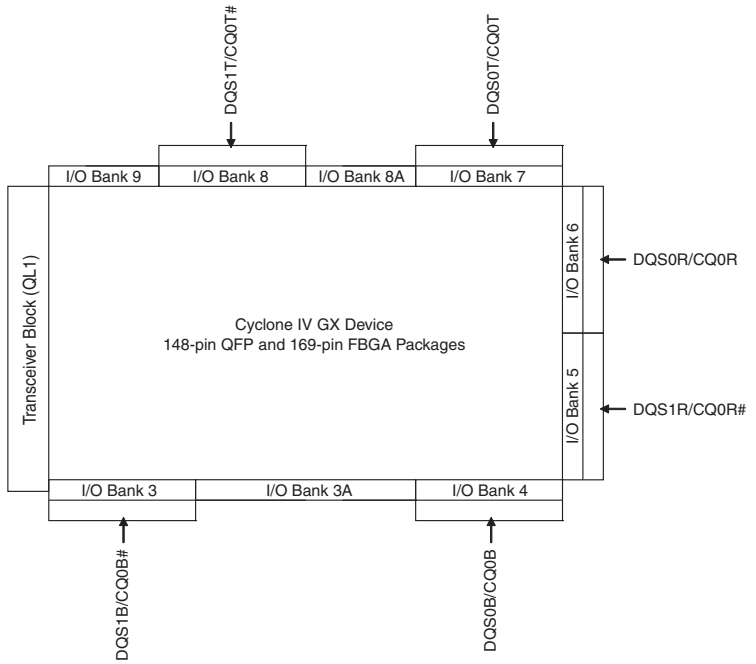
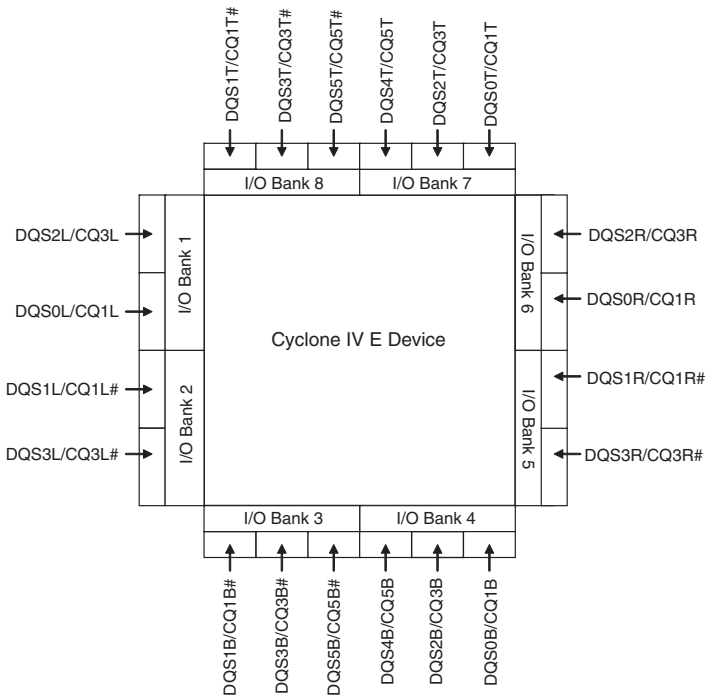


Figure 7–5 shows the location and numbering of the DQS, DQ, or CQ# pins in the Cyclone IV E device I/O banks.

Figure 7–5. DQS, CQ, or CQ# Pins in Cyclone IV E I/O Banks *(Note 1)*

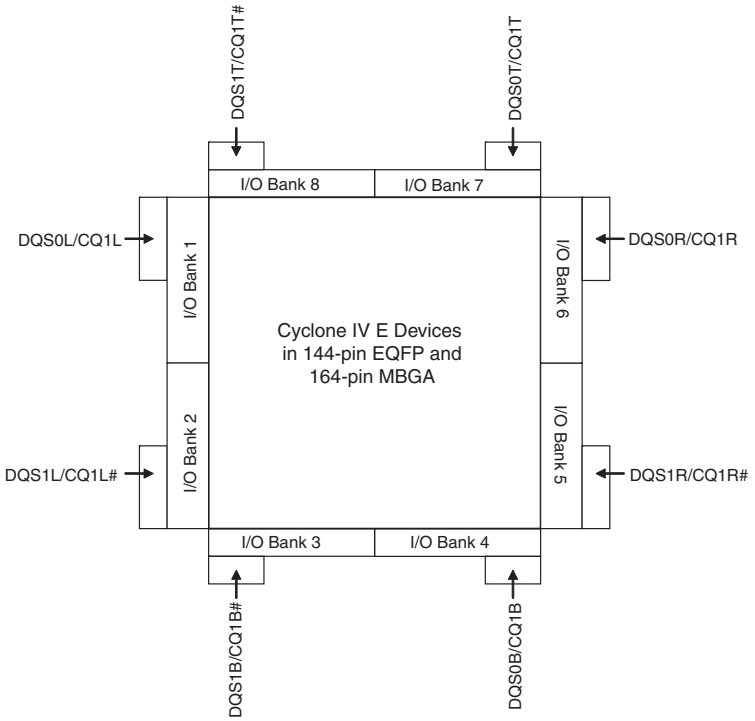


Note to Figure 7–5:

(1) The DQS, CQ, or CQ# pin locations in this diagram apply to all packages in Cyclone IV E devices except devices in 144-pin EQFP.

Figure 7–6 shows the location and numbering of the DQS, DQ, or CQ# pins in I/O banks of the Cyclone IV E device in the 144-pin EQFP and 164-pin MBGA packages.

Figure 7–6. DQS, CQ, or CQ# Pins for Cyclone IV E Devices in the 144-Pin EQFP and 164-pin MBGA Packages



In Cyclone IV devices, the ×9 mode uses the same DQ and DQS pins as the ×8 mode, and one additional DQ pin that serves as a regular I/O pin in the ×8 mode. The ×18 mode uses the same DQ and DQS pins as ×16 mode, with two additional DQ pins that serve as regular I/O pins in the ×16 mode. Similarly, the ×36 mode uses the same DQ and DQS pins as the ×32 mode, with four additional DQ pins that serve as regular I/O pins in the ×32 mode. When not used as DQ or DQS pins, the memory interface pins are available as regular I/O pins.

Optional Parity, DM, and Error Correction Coding Pins

Cyclone IV devices support parity in ×9, ×18, and ×36 modes. One parity bit is available per eight bits of data pins. You can use any of the DQ pins for parity in Cyclone IV devices because the parity pins are treated and configured similarly to DQ pins.

DM pins are only required when writing to DDR2 and DDR SDRAM devices. QDR II SRAM devices use the BWS# signal to select the byte to be written into memory. A low signal on the DM or BWS# pin indicates the write is valid. Driving the DM or BWS# pin high causes the memory to mask the DQ signals. Each group of DQS and DQ signals has one DM pin. Similar to the DQ output signals, the DM signals are clocked by the -90° shifted clock.

In Cyclone IV devices, the DM pins are preassigned in the device pinouts. The Quartus II Fitter treats the DQ and DM pins in a DQS group equally for placement purposes. The preassigned DQ and DM pins are the preferred pins to use.

Some DDR2 SDRAM and DDR SDRAM devices support error correction coding (ECC), a method of detecting and automatically correcting errors in data transmission. In 72-bit DDR2 or DDR SDRAM, there are eight ECC pins and 64 data pins. Connect the DDR2 and DDR SDRAM ECC pins to a separate DQS or DQ group in Cyclone IV devices. The memory controller needs additional logic to encode and decode the ECC data.

Address and Control/Command Pins

The address signals and the control or command signals are typically sent at a single data rate. You can use any of the user I/O pins on all I/O banks of Cyclone IV devices to generate the address and control or command signals to the memory device.

Cyclone IV devices do not support QDR II SRAM in the burst length of two.

Memory Clock Pins

In DDR2 and DDR SDRAM memory interfaces, the memory clock signals (CK and CK#) are used to capture the address signals and the control or command signals. Similarly, QDR II SRAM devices use the write clocks (K and K#) to capture the address and command signals. The CK/CK# and K/K# signals are generated to resemble the write-data strobe using the DDIO registers in Cyclone IV devices.

CK/CK# pins must be placed on differential I/O pins (DIFFIO in Pin Planner) and in the same bank or on the same side as the data pins. You can use either side of the device for wraparound interfaces. As seen in the Pin Planner Pad View, `CK0` cannot be located in the same row and column pad group as any of the interfacing DQ pins.

For more information about memory clock pin placement, refer to *Volume 2: Device, Pin, and Board Layout Guidelines* of the *External Memory Interface Handbook*.

Cyclone IV Devices Memory Interfaces Features

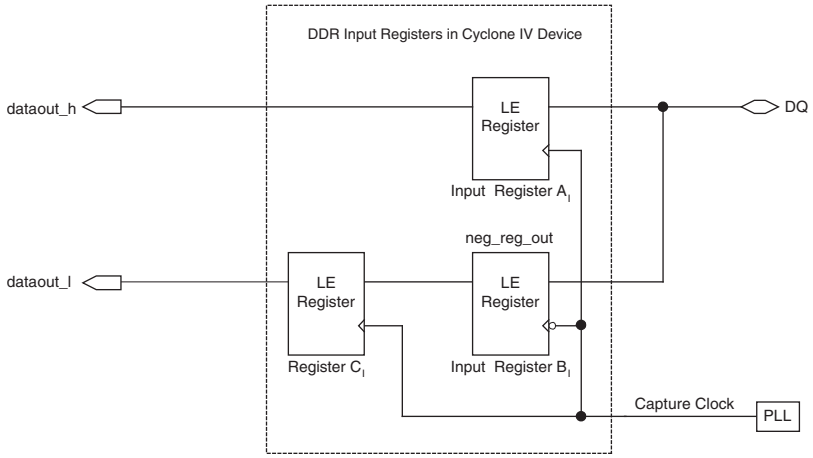
This section discusses Cyclone IV memory interfaces, including DDR input registers, DDR output registers, OCT, and phase-lock loops (PLLs).

DDR Input Registers

The DDR input registers are implemented with three internal logic element (LE) registers for every DQ pin. These LE registers are located in the logic array block (LAB) adjacent to the DDR input pin.

Figure 7–7 illustrates Cyclone IV DDR input registers.

Figure 7–7. Cyclone IV DDR Input Registers



These DDR input registers are implemented in the core of devices. The DDR data is first fed to two registers, input register A_I and input register B_I.

- Input register A_I captures the DDR data present during the rising edge of the clock
- Input register B_I captures the DDR data present during the falling edge of the clock
- Register C_I aligns the data before it is synchronized with the system clock

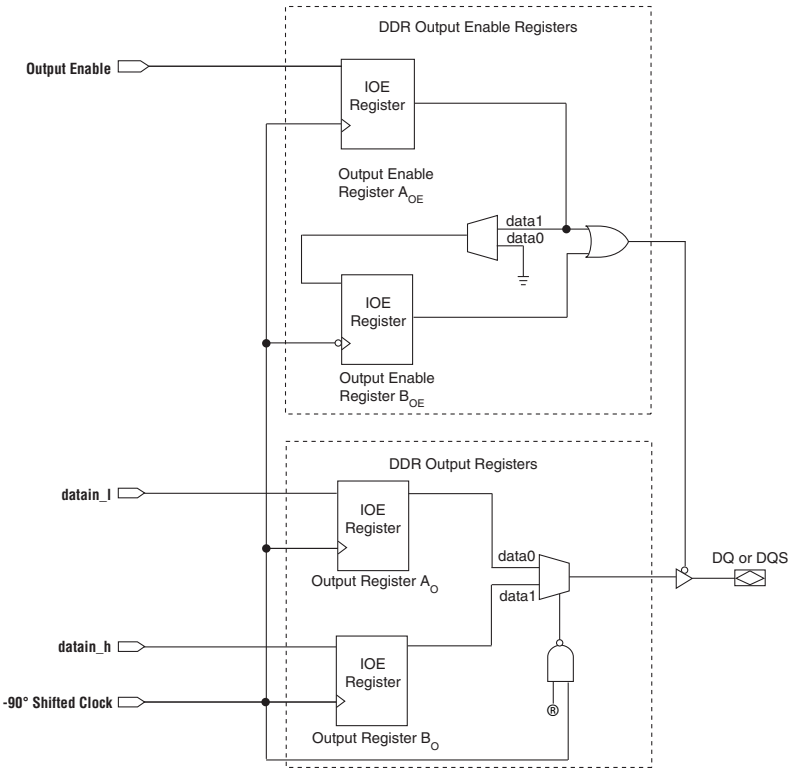
The data from the DDR input register is fed to two registers, `sync_reg_h` and `sync_reg_l`, then the data is typically transferred to a FIFO block to synchronize the two data streams to the rising edge of the system clock. Because the read-capture clock is generated by the PLL, the read-data strobe signal (DQS or CQ) is not used during read operation in Cyclone IV devices; hence, postamble is not a concern in this case.

DDR Output Registers

A dedicated write DDIO block is implemented in the DDR output and output enable paths.

Figure 7–8 shows how a Cyclone IV dedicated write DDIO block is implemented in the I/O element (IOE) registers.

Figure 7–8. Cyclone IV Dedicated Write DDIO



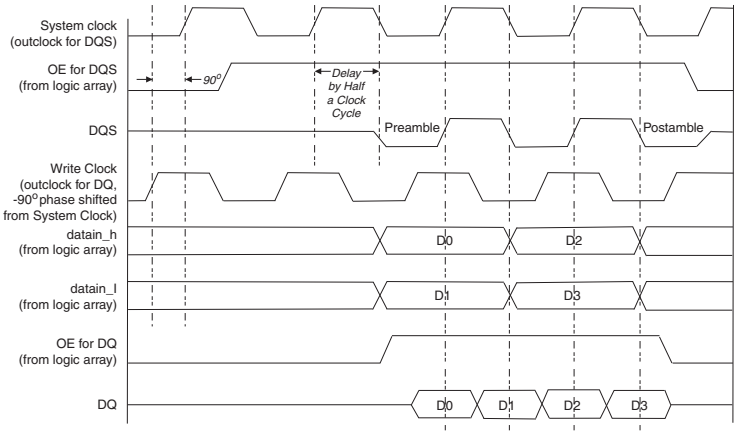
The two DDR output registers are located in the I/O element (IOE) block. Two serial data streams routed through `datain_l` and `datain_h`, are fed into two registers, `output register Ao` and `output register Bo`, respectively, on the same clock edge. The output from `output register Ao` is captured on the falling edge of the clock, while the output from `output register Bo` is captured on the rising edge of the clock. The registered outputs are multiplexed by the common clock to drive the DDR output pin at twice the data rate.

The DDR output enable path has a similar structure to the DDR output path in the IOE block. The second output enable register provides the write preamble for the DQS strobe in DDR external memory interfaces. This active-low output enable register extends the high-impedance state of the pin by half a clock cycle to provide the external memory's DQS write preamble time specification.

For more information about Cyclone IV IOE registers, refer to the *Cyclone IV Device I/O Features* chapter.

Figure 7–9 illustrates how the second output enable register extends the DQS high-impedance state by half a clock cycle during a write operation.

Figure 7–9. Extending the OE Disable by Half a Clock Cycle for a Write Transaction *(Note 1)*



Note to Figure 7–9:

(1) The waveform reflects the software simulation result. The OE signal is an active low on the device. However, the Quartus II software implements the signal as an active high and automatically adds an inverter before the A_{OE} register D input.

OCT with Calibration

Cyclone IV devices support calibrated on-chip series termination (R_S OCT) in both vertical and horizontal I/O banks. To use the calibrated OCT, you must use the RUP and RDN pins for each R_S OCT control block (one for each side). You can use each OCT calibration block to calibrate one type of termination with the same V_{CCIO} for that given side.

For more information about the Cyclone IV devices OCT calibration block, refer to the *Cyclone IV Device I/O Features* chapter.

PLL

When interfacing with external memory, the PLL is used to generate the memory system clock, the write clock, the capture clock and the logic-core clock. The system clock generates the DQS write signals, commands, and addresses. The write-clock is shifted by -90° from the system clock and generates the DQ signals during writes. You can use the PLL reconfiguration feature to calibrate the read-capture phase shift to balance the setup and hold margins.

The PLL is instantiated in the ALTMEMPHY megafunction. All outputs of the PLL are used when the ALTMEMPHY megafunction is instantiated to interface with external memories. PLL reconfiguration is used in the ALTMEMPHY megafunction to calibrate and track the read-capture phase to maintain the optimum margin.

For more information about usage of PLL outputs by the ALTMEMPHY megafunction, refer to the *External Memory Interface Handbook*.

For more information about Cyclone IV PLL, refer to the *Clock Networks and PLLs in Cyclone IV Devices* chapter.

Document Revision History

Table 7–3 lists the revision history for this chapter.

Table 7–3. Document Revision History

Date	Version	Changes Made
December 2010	2.2	■ Updated for the Quartus II software version 10.1 release. ■ Added Cyclone IV E new device package information. ■ Updated Table 7–2. ■ Minor text edits.
November 2010	2.1	Updated “Data and Data Clock/Strobe Pins” section.
February 2010	2.0	■ Added Cyclone IV E devices information for the Quartus II software version 9.1 SP1 release. ■ Updated Table 7–1. ■ Added Table 7–2. ■ Added Figure 7–5 and Figure 7–6.
November 2009	1.0	Initial release.