Compliance Task Group Call – Minutes

Weds, July 25, 2019 8am Pacific →Daylight← Time

See slides 6,7 for summary

Charter

The Compliance Task Group will

- Develop a framework for RISC-V tests, taking into account approved specifications for:
  - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
  - Standard Extensions (M,A,F,D,Q,L,C,B,J,T,P,V,N)
  - All spec'ed implementation options
    - (incl. MHSU modes, optional CSRs, optional CSR bits)
- Develop a method for selecting and configuring appropriate tests for a RISC-V implementation, taking into account:
  - Platform profile and Execution Environment (EE)
  - Implemented architecture, extensions, and options
- Develop a method to apply the appropriate tests to an implementation and verify that it meets the standard
  - test result signature stored in memory will be compared to a golden model result signature

Adminstrative Pointers

- Chair – Allen Baum allen.baum@esperantotech.com
- Co-chair – Stuart Hoad stuart.hoad@microchip.com
- TG membership- Sue Leininger sue@riscv.org
  - Send email to her - you must have a lists.riscv.org login
- TG Email tech-compliance@lists.riscv.org
  - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 9am Pacific time on 2nd/4th Wednesdays
  - Location is https://zoom.us/j/6213886723
- Documents, calendar, roster, etc. in https://lists.riscv.org/tech-compliance/
  see /documents, /calendars subdirectories
- Git repositories
  - https://github.com/riscv/riscv-compliance/
  - https://github.com/rsnikhil/Experimental_RISCV_Feature_Model
  - https://github.com/rsnikhil/Forvis_RISCV-ISA-Spec
  - https://gitlab.com/incoresemi/riscof (Shakti framework)

Attendees

- Allen Baum (Esperanto)

Meeting Agenda (in order of Priority)

1. Pull Request review (55) - postpone
   - changes to unaligned_jmp tests to support unaligned support
2. Email discussions
   - Email thread#1: Licensing: feedback favors BSD, board favors Apache (slide 9)
   - Email thread#2: TestFormat Spec Review – e.g. directory structure (slide 10)
   - Email thread#3: RFP for a compliance engineer (slide 11)
   - Email thread#4: Static vs Dynamic signatures
3. Email discussion (slide 10)
   - New test macros: RV_ [MSU]2[MSU],
     RV_[M/S/U]MODE_HANDLER(mode, sig_ptr, Code_ptr)
     RV_[M/S/U]CAUSE_HANDLER(cause_num, Code_ptr)
4. RISCOF status (slide 12)

Discussion

1. Pull Request review 55
2. Review of action items from last meeting
    1.
    2.
    3.
    4.
3. Other email discussion
4. TBD

Conclusions & Action Items

Decisions

Action Items

- Everybody: pay attention to email discussions so we don't waste time in meetings
- Stuart/Simon: need macro portability documentation
- Allen: start email discussions RE:
  - Polling companies about which license to use
  - Send latest TestFormatSpec document
  - RFP requirements for compliance engineer
  - Static vs. Dynamic signatures

Backup for discussions

License Inconsistencies

Ken Dockser writes

In going through the files on git hub I have found inconsistencies in the licenses specified. Based on riscv-compliance/doc/README.adoc, the intent was to use BSD and Creative Commons.

- The top level license (riscv-compliance/COPYING.BSD) is a 3-clause BSD,
- The riscv-compliance/riscv-test-env/LICENSE specifies a slightly different 3-clause BSD license naming Regents as the copyright holder.
- In riscv-compliance/riscv-test-env/test_macros.h an Apache v2 license is employed. In fact, Apache-v2 shows up in 57 files.

Desire is to use Apache? (BSD regents may eventually be replaced. RISCOF uses BSD 3-clause

Test Spec

- Proposed Structure is 2-level: <arch>_<modes>/<feature(s)>
  - <arch> are rv64i, rv32i, rv32e
  - <modes> are M, MS, MU, MSU: modes that the test will run in
    - Always starts in M at least, so always present ←still disagreements
  - <feature(s)> are
    - lettered extension [A | B | C | M ...] or subextension [Zam | ...]
    - more general names when tests cross extensions (e.g. Priv, Interrupt, VM, Integer).
    - Exact syntax/names for cross-extension subdirectories has not been ennumerated.
    - Tests that can /should be run in multiple modes replicate the subdirectory
- New Standard Macros
  - RVTEST_CASE(CaseName,CondStr, [DocTmp, DocString])
    - Test ases must be inside `#ifdef TEST_CASE_<CaseName>,#endif` pairs
  - RVTEST_SIGBASE(BaseReg,Val)
  - RVTEST_SIGUPD(BaseReg, Reg, Value)
  - RVTEST_M2S, M2U, S2U, U2M, U2S, S2M (?) -- TBD

Foundation Expectations

- Objective: publish compliance test 1.0 and finish the public review **before** the RISC-V summit in Dec. Shorter term is pre-1.0 by EO Q3
- Scope: publish tests and expected results run from the executable RISC-V formal specs -- make sure that all formal specs agree with each other
  - (Note: this approach will not work for priv spec)
- Minimal acceptance criteria is RV32Imc and RV64Imc
- Allen will focus on driving the task group to make this happen
- Nikhil will be tasked to ask all formal spec groups to commit their executable model support in the riscv-compliance repository
- Silviu and Yunsup will make the {compliance manager} CFP happen. They just need to understand what help is needed.

RISCOF status

- RISCOF can now be installed as a pip package (pip install riscof)
- Current suite supported: Integer and MulDiv extension.
- New directory structure adopted : https://gitlab.com/incoresemi/riscof/tree/master/riscof/suite
- YAML-Validator now a separate package - RIFLE (RISC-V Legalizer) usable w/RISCOF or standalone.
- HTML report generation done. *(needs WG feedback)*
- reduced command line options: RISCOF now takes inputs from a config.ini file. Example
- Updated YAML schemas with supervisor nodes as well.
- Modified macros into new RVTEST_ and RVMODEL_ prefixed macros. Doc:
  https://riscof.readthedocs.io/en/1.7.3/macros.html
- Added support for separate environment files for model and standard macros.
- Created user plugins for most repository targets: https://gitlab.com/incoresemi/riscof-plugins
  - riscvOVPsim grift Eclass sail_ocamlSim
  - CodasipSim Spike sail_cSim ***sifive-formal - Doesn't work*!!**
- Currently working on parallelizing test runs (e.g. make -jN to parallelize runs). ETA 2 weeks
- For more granular changes/updates:
  https://gitlab.com/incoresemi/riscof/blob/master/CHANGELOG.md

Trap Handler Data Structure