

Allen (Esperanto) [Chair]  
 SimonD (Imperas)  
 Lee Moore (Imperas)  
 Ben Selfridge (Galois)  
 Stuart Hoard (Microsemi)

Ramprasad Chandrasekaran (Xtreme-EDA)  
 Jeremy Ralph (Xtreme-EDA)  
 Martin Palkovic (Codalip)  
 Jeremy Bennett (Embecosm)  
 Ken Dockser (Qualcomm)

### Coverage modeling

- Ben of Galois talked a little about coverage tool - but demo & slides not approved to release yet
  - The have a formal semantic for Risc-V instruction set in Haskell
  - RV32/RV64IMA model is still a work in progress
  - Tools log coverage stats to files in text format
    - e.g. for every instruction that I am testing, I want to make sure that at some point every bit in a source regi has been high and low - easy to capture
  - There is an embedded bit vector expression language to query the machine state
    - e.g. boolean expressions, e.g. arbitrary predicates
  - Can define coverage metrics any way you want...
  - Ultimately, the idea is to generate test cases that can target your coverage metric the test generation is research...

Q: can this make use of system verilog covergroups and make use of other industry standard approaches?

A: seems to be on its own and still under development

Q: how does Galois detect that a bit propagates to the result to know that the bit setting can be measured

- ie only want to sample coverage when the impact is measurable or not...
- (e.g. flipping one bit of an AND when the other input is 0 will not be distinguishable.  
 This test would make coverage look better but would actually mask faults

A: Unclear; may need a manual definition of a coverage metric>

- Lee - this is big issue of whether depending on the wrong coverage model actually masks issues rather than finds them
- We don't want proof of stimulus cover, it needs to be the response coverage
- Imperas has a mutation fault simulation based coverage tool that they use internally to see how good tests are in terms of coverage of the lines of code and code paths in the tests that are exercised.

A: Suggest let the group look at coverage tools when these Galios tools are made public.

Checking the existing compliance suite to see what it reports for coverage would be particularly interesting.

### New RISC-V unprivileged spec - new platform terminology

Q: (again) are tests for hardware compliance or system compliance?

- eg hardware multiply implemented, whereas divide might be emulated

A: both; HW vendor can supply support firmware to ensure it is platform compliant, , i.e. meets the system requirements

- To properly test this, we need the framework to have the capability to load soft library as part of initial state of test.
  - (along with other initial state: registers, CSR, and test code and signature block itself)
  - This is an important issue

A: Stuart will send a model to Imperas to look at how compliance framework can be extended to include a software exception handler and Imperas will report next time.

### Test Configuration options

- Issue: every simulator vendor can support many configuration options,
  - But the format for each is different
- Ideally there should be a common file that is used by all model/simulators in some way, likely a two step process:
  - interpret the common format & validate legal configurations
  - call a vendor-defined script that converts the common format to vendor specific parameters for model
  - puts onus on the vendor to fit into framework, not the foundation
- LEE: It is important that the semantics of the format be clearly defined; the syntax is almost a don't care
  - Otherwise options will be used incorrectly, or translated incorrectly
- Imperas sent the formal group a yaml version of what its riscvOVPSim simulator/model uses as a configuration file
  - We need get feedback from the formal group before forging ahead on this.