

Compliance Task Group Call – Minutes

Thur, 23Jul2020 8am Pacific → Daylight ← Time

See slide 8 for discussions and action items

Charter

The Compliance Task Group will

- Develop? compliance tests for RISC-V implementations, taking into account approved specifications for:
 - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
 - Standard Extensions (H,S,U,A,B,C,D,F,H,J,M,N,P,T,V,N), Priv Mode
 - All spec'ed implementation options
 - (incl. MHSU modes, optional CSRs, optional CSR bits)
- Develop a method for selecting and configuring appropriate tests for a RISC-V implementation, taking into account:
 - Platform profile and Execution Environment (EE)
 - Implemented architecture, extensions, and options
- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
 - test result signature stored in memory will be compared to a golden model result signature

Administrative Pointers

- Chair – Allen Baum allen.baum@esperantotech.com
- Co-chair – Bill McSpadden bill.mcspadden@seagate.com
- TG Email tech-compliance@lists.riscv.org
 - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays
 - See <https://lists.riscv.org/g/tech-compliance/calendar> entry for zoom link
- Documents, calendar, roster, etc. in
 - <https://lists.riscv.org/tech-compliance/> see /documents & /calendars subdirectories
 - <https://riscof.readthedocs.io/en/latest/> riscof
 - <https://riscv-config.readthedocs.io/en/latest/> config: YAML and WARL spec
 - <https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUIEs>
(compliance specific docs in compliance folder)
- Git repositories
 - <https://github.com/riscv/riscv-compliance/>
 - <https://gitlab.com/incoresemi/riscof> (riscof framework)

Meeting Agenda

- Updates, Status, Progress
 - Policy/process updates (see next page)
- Discussion:
 - Compliance FAQ
 - Overview and Review
 - Specific Compliance Policy/Process Gaps:
 - What is the process for approving test merge request (the official approval method)
 - What is the process for certifying compliance? (beyond submitting report). What detail of compliance?
 - (How) can we approve compliance on actual HW?
Can we allow compliance tests on models with different environments than the actual HW?
 - IF someone incorporates compliant core IP into their SOC, does it need to run compliance tests again?
For configurable IP, every possible configuration or new configuration?
 - Coverage Spreadsheet
 - critique, review (See: Coverage Rules.xlsx in <https://lists.riscv.org/g/tech-compliance/files/Review%20Documents>)
 - Migration to Framework v.2
 - Review Pipecleaner tests: What do we need to do to exercise capabilities for Priv Mode tests
 - What steps do we need to complete to cut over to V.2
(e.g. Sail model updates, pipecleaning, N people have run it, testing all the “fixed in riscov” issues)
 - Next steps and Ongoing maintenance
 - Compliance Tests , Formal Model Updates & Tool support are supposed to be provided by the TG before ratification
 - Who should provide Tools, e.g. coverage models test generation
 - Ratified specs need a different approach.....
Need to Map out order in which tests should be developed next (e.g. Priv, F, D or F, Priv, D...
 - TG Reorganization – subgroups?
 - (more discussion if time permits)

Action Item / Progress Update

- ET Base ISA coverage draft spec is uploaded - done – needs more eyes to review
- SH will add file regarding coverage - no progress....in progress
- QC will add file re: Compliance FAQ - rev 2 or 3 is here:
<https://lists.riscv.org/g/tech-compliance/files/Review%20Documents/Compliance%20FAQs.pdf>
- ET get google docs folder for collaboration - has been set up here:
<https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUIEs>
 - Has compliance and glossary folders, among others
- Imperas / Incore: ensure headers, macros, dir structure match newest spec, assertions are not inline – waiting for assertion macro update, Imperas pull request
- ET to coordinate with Riscof to determine pipecleaning exercise - to be reviewed in TG
- ET to communicate with TSC about reorganization comments - waiting TSC feedback
- ET/SH to talk w/ SAIL team about transitioning support to Foundation - in progress
- Configuration Structure TG vs. Riscv-Config: discussions underway – see
<https://github.com/riscv/configuration-structure/>

Note: initials are company abbreviations

Discussion

- New meeting time: 2nd and 4th Thursday, 8am PDT
- Progress (see previous slide)
- New policies to review:
<https://drive.google.com/drive/folders/17huuOKXafR5n4tbxZfzSnAakmgHnipoY>
 - ISA vs. non-ISA
 - Policy policy
 - Done policy (also lifecycle definition)
 - New feature /change rationale policy
- Compliance FAQ: here <https://lists.riscv.org/g/tech-compliance/files/Review%20Documents/Compliance%20FAQs.pdf>
 - A philosophical guide to compliance and verification: can we run SW on it?
 - SH: Hazards should be removed from the FAQ unless specifically mentioned in spec
 - Chair: some hazards are architectural, specifically CSRs. Will check on GPRs
 - SH: test should reference numbered section of the ISA spec they are testing
- Compliance Policy/Process Gaps: test acceptance criteria
 - IMP: 3 ways to certify compliance:
 - Pay someone to do it, have the Compliance TRG do it, Self-Certification
 - Chair: what is process for accepting merge requests into tests?
 - IMP: tests updated, made pull request, merge accepted. Is that official?
 - Chair: Policy is only that TG is responsible. SAIL model must be able to run them. There are coverage goals that need to be met. Can we accept partial coverage, and later full coverage?
 - IMP: Vector tests, 55 million lines of code – that's a size problem. Also test time problem. How do we handle IOT which have only small internal SRAMs. RTL can have larger memory, so core could have testbench with large memory for compliance testing. Krste says we need to run these tests under Linux, the other end of the spectrum
 - Chair: tests that need large memory will likely only need to be run on implementations that actually support large memory. E.g. if an IOT device has vector support, it will have a larger memory size anyway. IF required, we can break a large test into many smaller ones.
- ???: Can we specify a minimum amount of memory? IF you don't have it, you need to develop a testbench that does.
- Compliance Certification – process?
 - QC: “we ran and passed tests”. Say nothing else – but this is a marketing problem
 - Chair: How then do they claim misalign support? Could be HW, emulated, or unsupported
 - Imp: We have it marked in Coverage
 - QC: It is a platform issue. How is misaligned supported on a platform?
 - Chair: Platform might not care. RV32i tests don't distinguish HW vs emulated, just supported or not (so either executed or traps properly)
 - Imp: with the test selector, we can't (easily) claim which tests are run
 - Chair: no, the test report indicates which tests were run and which passed/failed

Decisions & Action Items

Decisions

Meetings moving to 8am PDT Thursday instead of Weds.

Off cycle meeting will be scheduled to catch up on agenda items.

Outstanding Action Items

Imperas: make pull request for updated assertion macro

Imperas: measure RV32I, vector max memory footprint, number of instructions executed

Stuart: write up coverage taxonomy

Chair: Schedule off-cycle meeting

Chair: get architectural hazard pointer

Everybody: read policy docs, send gaps in compliance (e.g. formal model support, possible mismatch between config TG and riscv-config) and priority to cto@riscv.org

ISA Compliance Standing Committee and TG ReOrg

Because both Compliance and Formal Modeling are ongoing processes, the ISA Compliance Standing Committee has been formed to direct the current Compliance and Formal Modelling TGs

Proposal: reorganize the 2 TGs into:

- ISA Compliance Standing Committee sc-compliance-isa@lists.riscv.org
- Compliance Tests Task Group tech-compliance-test@lists.riscv.org
Charter Statement: Specifying the requirements for the tests (functional coverage), developing the actual test cases, integrating the tests into the framework. (**Deliverable**: Compliance Test Suite)
- Compliance Generators Task Group tech-compliance-generators@lists.riscv.org
Charter Statement: Develop tools which are configured to generate tests and measure functional coverage. Their tests should meet the requirements specified by the compliance tests task group. (**Deliverable**: Test Tools)
- Compliance Framework Task Group tech-compliance-framework@lists.riscv.org
Charter Statement: Develop a framework (workflow) that takes a description of an implementation to select/configure tests, runs them, and compares them to the golden model. Manages the output and logging of the tests being run. (Possibly combine for now with generator group? (**Deliverable**: Framework v2)
- Golden Model Task Group tech-golden-model@lists.riscv.org
Charter Statement: This group will maintain a Formal Specification for the RISC-V ISA. This is a specification of the ISA in a formal language, for precision, unambiguity, consistency and completeness. The spec is readable and understandable as a canonical reference by practising CPU architects and compiler writers. It is executable and machine-manipulable by tools for establishing correctness and transformations in both compilers and CPU designs.

(.....discuss.....)

Pull/Issue Status

Issue#	Date	submitter	title	status	
#04	3-Jul-18	kasanovic	Section 2.3 Target Environment	Fixed in RISCOF	
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap		
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed		
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability		
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate		
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG		
#90	11-Feb-20	towoe	Report target execution error		
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	under discussion	
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	under discussion	
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	
pull#113	30-may-20	imphil	Consistently use UNIX line endings	under discussion	
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	
#119	17-jun-20	allenjbaum	Missing RV32i/RV64i test: Fence	Test needs to be written	
#125	15-jul-20	ShashankVM	Request to stop hosting closed source code on riscv repo	under discussion	