Architectural Test Task Group Call – Minutes

Thur, 11Mar2021 8am Pacific → Standard ← Time

See slide 6 for agenda

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We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/risc-v-international-community-code-of-conduct/

Adminstrative Pointers

- Chair – Allen Baum allen.baum@esperantotech.com Co-chair – Bill McSpadden bill.mcspadden@seagate.com
- SIG Email sig-arch-test@lists.riscv.org
  - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays.
  - See https://docs.google.com/spreadsheets/d/1L15_gHl5b2ApkcHVtpZyl4s_A7sgSrNN zoom link
- Documents, calendar, roster, etc. in
  - https://sites.google.com/a/riscv.org/risc-v-staff/home/tech-groups-cal
    https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUlEs
    (lifecycle in "policies/supporting docs" folder, gaps in "planning" folder, compliance specific in "compliance folder")
- Git repositories ←docs riscv → tools

https://github.com/riscv/riscv-compliance/tree/master/doc/	tests	https://github.com/riscv/riscv-arch-test/
https://riscof.readthedocs.io/en/latest/index.html	riscof	https://gitlab.com/incoresemi/riscof/
https://riscv-isac.readthedocs.io/	ISA coverage	https://github.com/riscv_isac
https://riscv-ctg.readthedocs.io/	Test Gen.	https://github.com/riscv_ctg
https://github.com/riscv/riscv-config/tree/master/docs	YAML, WARL config	https://github.com/riscv/riscv-config/
https://github.com/rems-project/sail-riscv/tree/master/doc	Sail formal model	https://github.com/rems-project/sail-riscv/

- JIRA: https://jira.riscv.org/projects/CSC/issues/CSC-1?filter=allopenissues
- Sail annotated ISA spec: in https://github.com/rems-project/riscv-isa-manual/blob/sail/

README.SAIL	←how to annotate	annotated unpriv spec→	release/riscv-spec-sail-draft.pdf
release/riscv-spec-sail-draft.pdf	← annotated source	annotated priv spec→	release/riscv-privileged-sail-draft.pdf

  - https://us02web.zoom.us/rec/share/-XIYazzhIBbQoiZdarCfebdjxjDWiVhf-LxnuVrliN4Bc30yf17ztKkKDU4Og54b.fArPPqnuR-NiXpQU Tutorial
    Access Passcode: tHAR#5$V

SIG Charter

The Architectural Compatibility Test SIG is an umbrella group that will provide guidance, strategy and oversight for the development of tests used to help find incompatibilities with the RISC-V Architecture as a step in the Architectural Compatibility self-certification process

The group will:

- Guide Development of:
  - Architectural tests for RISC-V implementations covering ratified and in-flight specifications for
    - Architectural versions, standard extensions, and implementation options.
  - Tools and infrastructure to help identify architectural incompatibilities in implementations
- Work with LSM and Chairs for resources to get the above work done.
- Mentor or arrange for mentoring for the resources to get the above work done

Meeting Agenda

0. **Looking for more admins, maintainers for riscv-compliance git repo !!**

I. Updates, Status, Progress:

1. TG transitioned to SIG, mailing list and github Repo renamed to "arch-test" - links now need updates
2. CTG (Coverage Test Generator) and ISAC (ISA Coverage tool) moved into riscv github repo
3. Imperas Crypto tests – PR submitted
4. FP tests status:
5. Vector:

II. Next steps and Ongoing maintenance

1. Review: The 3 W's of testing: Who, What, and Waivers (this will become an official policy, see slide 8)
2. Brainstorm: how to deal with misalign non-determinism
3. Discussion: Migration to Framework v.3.0 (riscof).
   - What steps do we need to complete to cut over to V.3 (blocking items):
     - (e.g. Sail/Spike model updates, pipecleaning, N people have run it, testing all the "fixed in riscof" issues
     - Review Pipecleaner tests:What do we need to do to exercise capabilities for Priv Mode tests
4. Close github issues as a result of repo v2.1
5. Maintenance updates to V2 to enable future tests
   a) update RVTEST_SIGUPD to keep automatically adjust base/hidden offset when offset>2K,
   b) Enable use Sail model results as the assertion value
   c) add assertion macros for FP, DP, Vreg to arch_test.h and test_format spec
   d) add trap handlers for S, VS modes
6. Tests for non-deterministic result (see attached discussion in email)
   1. Provide a reference RTL test fixture (as opposed to SW functional model). See. JIRA CSC-6
   2. Define hooks for concurrency tests
7. Specific Compliance Policy/Process Gaps:

Repository, Group Name Change

- Group has been renamed
  - From: tech-compliance
  - To: sig-arch-test
  - All current membership, mailing list, files, messages, and chairs unchanged
- Mailing list has changed
  - From: tech-compliance@list.riscv.org
  - To: sig-arch-test@list.riscv.org
  - Minutes from next weeks meeting will be sent from that address

- Repository name has changed from
  - From: https://github.com/riscv/riscv-compliance
  - To: https://github.com/riscv/riscv-arch-test
  - There is an alias from the old name to this one

- For both steps, expect a transition period as we track down documentation, scripts, makefiles, etc. that point to riscv/riscv-compliance and update them (e.g. in spike arch-test/README), https://riscv.org/technical/specifications/

The 3 W's of testing: Who, What, & Waivers (and Errata)

- Who: the last developer that makes changes to the RTL
  - Selection of configuration parameters provided by the RTL developer is not considered a change
- What: Ideally, run on physical chips, but could be SW or FPGA RTL sim
  - Implementor must provide enough resources to load and run tests and extract signature
- Waivers: HC→TSC approval required, Board/Mkting informed (mention in branding or ACT policy)
  - HC approves waiver request, HC & requestor present it to TSC
  - TSC vote to approve must be eligible majority positive vote with no dissent
  - Reasons for HC approval include:
    - Non-deterministic result is legal but not modeled by reference model (neither Spike nor Sail)
    - Test fails because of demonstrable bug (in test or formal model) (test/model must be fixed)
    - Written spec has ambiguity (spec must be fixed) ; not granted if it affects SW compatibility
    - Corner case unlikely to affect SW compatibility
- Errata:
  - Cores failing tests added after (certification must list errata if not fixed in silicon)
  - Self-reported errata: RVI needs to evaluate if it will likely affect SW compatibility
    - our tests didn't find it; we should consider adding tests
  - Cores should re-test yearly if tests, tools, or simulators change & issue errata if new issues found

To be written up as policy doc

TGs under the SIG

- IF you're creating work product, you should be a TG
- If changing requirements, plans ABIs, etc
  - Test plan==SOW
- The Architectural Testing Task Group will define and maintain specifications for
  - test formats
  - test-benches and frameworks needed for
    - privilege testing privilege testing,
    - Concurrency/ Memory model testing
    - Asynchronous event testing (interrupts)
    - Nondeterministic tests
  - ISA test coverage goals
  - test tools (e.g. coverage, generators)
- The Architectural Testing Task Group will maintain the appropriate GitHub:
  - tests for the individual ISA extensions
  - issues related to the tests
  - the operation and issues related to the framework
- The Architectural Testing Task Group will
  - work with the different privilege and un-privilege ISA extension Task Groups
    - to help them write test plans/specs for the ISA tests
    - to help them work with the sub-contractors (IITMadras, RIOS, CAS, etc) to deliver the tests
  - assess quality of delivered tests and be maintainer for the test GitHub

Discussion

Updates, Passdowns, Status, Progress:

TG: transitioned to SIG, mailing list, github Repo renamed to "arch-test" - links need updates

Tools: Incore CTG (Coverage Test Generator) , ISAC (ISA Coverage tool) moved into riscv repo

Tests: Imperas Crypto tests –PR submitted, feedback given, tweaks needed, updates forthcoming

IIT FP tests status: IBM model constraints are being converted into CTG rules; See
https://www.research.ibm.com/haifa/projects/verification/fpgen/papers/ieee-test-suite-v1.pdf
https://www.research.ibm.com/haifa/projects/verification/fpgen/test_suite_download.shtml

RIOS Vector tests: SAIL models, test generator & tests exist, used on a real implementation
Test-generator may be open-sourced.

Policies:

new term for Group Contributors is 'Technical Lab Partners'

(self)Certification responsibilities split: tests belong to arch-test.
self-certification belongs to vendor. branding belongs to RVI marketing.

Discussion Who, What & Waivers. <see slide 8 of pptx>

Who: now clarifies that IP configuration selection by customer **not** considered a change
IP vendor responsible for (self-)certifying that config combinations are compatible

What : added:the implementor must provide enough resources to get at signature

CTO: (AI to Chair). Put it in a policy & Explain this at the next all-hands

Non-determinism: brainstorming solutions

Chair - Good example: mis-aligned loads/stores. Sometimes HW support. Sometimes a trap. Sometimes both for same op at same address to same address.

Chair - I believe that the SAIL model allows either to be configured – but unconditionally only

Sail: - this seems to be a point of concurrency issue in the SAIL model.

Chair – Not just part of concurrency This is also a result of non-architectural state

Sail - There are many conditions that have to be considered, wrt concurrency.
Question: how.why would it do both?

Chair – ex. Misalign : TLB hit miss. Part of access is hit, part miss changes execution to trap

Chair - there are methods to handle misalign:
1) evaluate always/never trap & allow either result to count asa match
2) use reference trap handler to emulate – gets complex with VM

Incore - want to use same method for the all scenarios, not a point solution

Sail - seems to be a lot of plumbing for a single problem. Don't jump through large hoops to get this to work. We have other issues coming up in memory consistency issues.

Chair: The reason for this specific case is the because it has been hit in Base ISA tests

CTO - I have 2 requirements: 1) can't have infinite set of tests, have to look at this as a "lock the door" test. 2) have to document in test policy to tell people how to test this; need to explain strategy.There are lots of cases of non-determinism. this group has to define.

CTO - need to make statement about evaluation order un-ordered states of instructions *<this is specific to vector reduce>* need to state this to RIOS (for vector) et. al.

CoChair - We need an instruction that says, "complete the outstanding instructions, sample the state"

CTO - what you're describing is "breakpoint". did this at Apple for testing there.

CTO - the resulting simulator can be enhanced to do this work.

Chair -there is no architectural way of clearing non-architectural state.
We can't add non-architectural methods to test, nor ask implementors to alter RTL
< discussion about SAIL model and concurrency model >

From **Sail**: rmem - operational model, isla (or isla-axiomatic) - axiomatic

CTO - this is a very large topic. i suggest a separate meeting. seems appropriate for a small working group.

Chair - this problem has been hanging over our heads around since I've been chair..
We need to concentrate on it and get a solution.
I've listed options for the misalign case.
That case is single stream, base ISA, and an issue w current tests, not future ones.
Future issues are concurrent, multistream and also non-determinstic.
<See slide 12 for more detail>

Previous Decisions & Action Items

Decisions

Modify wording of SIG charter to clarify self-certification rationale and relationship to arch tests <done>

Modify wording of SIG charter to clarify self-certification rationale and relationship to arch tests <done>

Clarified that self-certification that implementation selected configuration variables in vendor supplied IP is not considered an RTL change. <done, to be written up as a policy>

Remove RVTEST_IO_CHECK macro from test format spec

Vector tests will not test unordered vector reduce, but only architectural defined ordered cases.

Outstanding Action Items

NEW

Chair : document target process for removing target environment files from riscv-compliance repo into a target repo and contact all model maintainers to inform them of the process and timeline. <ongoing>

Chair: need to write a non-determinism policy that documents how a new non-deterministic feature testing fits into the lifecycle of an extension. At what point does the testing methodology need to be in-place in order to approve it? <done – added to D.O.D policy and checklist: plan stage must describe methodology>

Chair: more brainstorming on handling nondeterminism, concurrency <discussion started on retrofitting riscof for concurrency

Old

Inspire: add support for QEMU target <?>

Chair: get SAIL repo moved into a riscv repo <done, but for viewing only>

QC: extract bits of FAQ as guidelines for test writing <?>
Incore: Try YAML version of SAIL to see if it works <ongoing>

Imperas: make pull request for updated assertion macro <removed, replaced with code from TGChair>

SH: write up coverage taxonomy

Non-determinism in Architectural Tests

The RV architecture defines optional and model/µarch defined behavior.
This implication: there are tests that have multiple correct answers. E.g.:

- Misaligned accesses: can be handled in HW, by "invisible" traps w/ either misaligned or illegal access causes, and do it differently for the same op accessing the same address at different times (e.g. if the 2nd half was in the TLB or not)
- Unordered Vector Reduce ops: (different results depending on ordering & cancellation)
- Tests involving concurrency will have different results depending on speculation or timing between concurrent threads (e.g. modifying page table entry without fencing)

From the point of view of ACTs, there are 2 (& sometimes more) legal answers. The golden model only generates one. Possible mechanisms to test include:

- Modify (if necessary) & configure reference model to generate each legal result, run it with each and accept either result from the DUT (e.g. misalign and un-fenced PTE modification)
- Provide specific handlers for optional traps
- Use self-testing tests(compare with list or range of allowed outcomes from litmus tests)
- Avoid tests that can generate non-deterministic results
- Ultimately: develop new frameworks that can handle concurrency along with reference models that can generate all legal outcomes

BACKUP

Test Report Requirements

- Architecture test version policy (mechanism TBD by ACT group)
  - Architectural test reports must include:
    - The ISA string that describes the ISA and extensions that claim to be implemented
    - The vendor and implementation IDs that the part will report
    - Test pass/fail reports
    - The YAML description of the features and options implemented (for v3 of the framework)
  - Architecture test reports must include version numbers of *
    - Toolchain,
    - reference model,
    - Architecture Compatibility Test (ACT) suite , riscv-config (for v3 of the framework)
- Vendors who self-certify generate pull request into arch-test reports github rep
  - File structure is vendor/implementationID/date/
- Each release version of ACT will document the minimum version of the toolchain utilities required to support the instructions used for that version of the tests in a repository README file

* *Need to ensure these get updated automatically*

Architectural Test Rationale – Intent and Limits

RISC-V Architectural Tests are an evolving set of tests that are created to help ensure that SW written for a given RISC-V Profile will run on all implementations that comply with that profile.

These tests also help ensure that the implementer has both understood and implemented the specification.

The RISC-V Architectural Tests test suite is a minimal filter. Passing the tests and having the results approved by RISC-V International is a prerequisite to licensing the RISC-V trademarks in connection with the design.

Passing the RISC-V Architectural Tests does ***not*** mean that the design complies with the RISC-V Architecture. These are only a basic set of tests.

The RISC-V Architectural Tests are ***not*** a substitute for rigorous design verification; it is the responsibility of the implementer to deploy extensive testing.

To be added to the riscv/riscv-compliance/doc/ directory as “RISC-V Architectural Test Rationale” satisfying Jira CSC-2

Test Acceptance Criteria – second cut

Tests must:

- conform to current standard of test spec (macros, labels, directory structure)
- use only files that are part of the defined support files in the repository
- run in framework
- run in SAIL and not fail any tests
- generate a valid signature using SAIL (that can be saved & compared with another DUT/sim)
- Report that test results propagate to signature
- have a clear configuration - i.e. which ISA extension it can be used with
- improve coverage (compared to existing tests) as measured and reported by ISAC
- use only standard instructions (fixed size per architecture LI, LA allowed)
- be commented in test_case header

Framework Requirements – first cut

The framework must:

- Use the TestFormat spec and macros described therein
  - (which must work - including assertions)
- Choose test cases according to equations that reference the YAML configuration
- Define macro variables that can be used inside tests based on the YAML configuration
- Include the compliance trap handler, & handle its (separate) signature area
- Load, initialize, and run selected tests between two selected models, extract the signatures, compare results, and write out a report file
- Exist in a riscv github repo, with a more than one maintainer.
- Be easy to get running, e.g.:
  - run under a variety of OSes with the minimum number of distro specific tools.
  - Not require sudo privileges
- Have the ability to measure and report coverage
  - Coverage specification is a separate file
  - Could be a separate app

Pull/Issue Status

Issue#	Date	submitter	title	status	comments
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap	^	HW misalign support not configurable
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed	|	now
#90	11-Feb-20	towoe	Report target execution error	|	
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	fixed in RFQ tests	Will be closed in 2.1 or 2.2
#142	17-Nov-20	subhajit26	Not able to run compliance test for rv32E device and RV32E ISA	RV32E only	Not RV32EC or RV32EM
#145-9	01-Dec-20	Imperas	Test I EBREAK,ECALL, MISALIGN_JMP/LDST, OpenHW	v	HW misalign support not configurable
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	-can we add an alias?
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	May be fixed?
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
pull#128	29-jul-20	nmeum	grift: update for new directory structure	Correction made	Reviewed by Marc, needs correction
pull#129	31-jul-20	nmeum	sail-riscv-ocaml: Disable RVC extension on all devices not using it	In process	Who can review this?
pull#172	27-feb-21	imperas	Crypto Scalar Tests (also issue#173)	In process	Needs review
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability	deferred	fixed in v2
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate	fixed	Needs target provided linker scripts
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG	Fixed	
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	Pull #152 fixes it	close after merge
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	Will be fixed by RFQ tests
#119	17-jun-20	allenjbaum	Missing RV32i/RV64i test: Fence	Test has been written	Close when RFQ test is merged
#132	15-aug-20	davidmlw	Why not just use mepc for mret?	Answered - close	Should be resolved
#135	04-sep-20	MikeOpenHWGroup	Request for a Tag on this Repo	assigned	Req. for non-hash tag; needs process
#155	03-Dec-20	bluewww	RI5CY: add minimum clang version#	Fixes issue #108	Merge after review
#156	08-Dec-20	panda1628	PMP/PMA Tests	Question answered	Can be closed
#157	15-dec-20	Stnolting	Memory requirement for new test framework	Question answered	Can be closed
#158/164	23-dec-20	Stnolting	Add white space in verify report [absolutely uncritical]	Non-critical	Should be accepted (Pull #164)
#165	12-jan-21	Towoe	Version numbering	Non-critical	Close?, will use semantic vers from now on
#169	22-jan-21	Towoe	RISCOF redefine of TEST_CASE_1	Question answered	Can be closed
#170	18-feb-21	Panda1628	Privilege Mode test	Question answered	Can be closed
#175	18-mar-21	AllenJBaum	README.md needs a title change	In process	Simple fix

JIRA Status

Issue#	Date	submitter	title	status	comments
IT-1	27Aug/20	Allen Baum	Need to modify the description of compliance in https://riscv.org/technical/specifications/	done	
IT-4	01/Sep/20	Allen Baum	Add Jira link to TG home pages	done	
CSC-1	20/Aug/20	Ken Dockser	Come up with names for the tests suites that we are creating		1st step done
CSC-2	20/Aug/20	Ken Dockser	Produce concise text to explain the Architecture Tests intent and Limits	done	Written, needs pull req
CSC-3	20/Aug/20	Ken Dockser	Come up with an internal goal for what we wish to accomplish with the Architectural Tests		Not written
CSC-4	20/Aug/20	Ken Dockser	Develop a roadmap for all the different categories of test suites that will need to be created		Not written
CSC-5	20/Aug/20	Ken Dockser	Develop a roadmap for releases of single-instruction Architecture Tests		Not written
CSC-6	20/Aug/20	Ken Dockser	Develop a reference RTL test fixture that can stimulate and check the CPU under test		Needs more discussion