Compliance Task Group Call – Minutes

Thur, 13Aug2020 8am Pacific →Daylight← Time

See slide 4 for agenda

Charter

The Compliance Task Group will

- Develop? compliance tests for RISC-V implementations, taking into account approved specifications for:
  - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
  - Standard Extensions (H,S,U,A,B,C,D,F,H,J,M,N,P,T,V,N), Priv Mode
  - All spec'ed implementation options
    - (incl. MHSU modes, optional CSRs, optional CSR bits)
- Develop a method for selecting and configuring appropriate tests for a RISC-V implementation, taking into account:
  - Platform profile and Execution Environment (EE)
  - Implemented architecture, extensions, and options
- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
  - test result signature stored in memory will be compared to a golden model result signature

Adminstrative Pointers

- Chair – Allen Baum allen.baum@esperantotech.com
- Co-chair – Bill McSpadden bill.mcspadden@seagate.com
- TG Email tech-compliance@lists.riscv.org
  - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays
  - See https://lists.riscv.org/g/tech-compliance/calendar entry for zoom link
- Documents, calendar, roster, etc. in
  - https://lists.riscv.org/tech-compliance/ see /documents & /calendars subdirectories
  - https://riscof.readthedocs.io/en/latest/ riscof
  - https://riscv-config.readthedocs.io/en/latest/ config: YAML and WARL spec
  - https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUlEs (lifecycle in "policies/supporting docs" folder, gaps in "planning" folder, compliance specific in "compliance folder")
- Git repositories
  - https://github.com/riscv/riscv-compliance/
  - https://gitlab.com/incoresemi/riscof (riscof framework)
  - https://github.com/riscv/riscv-config/

Meeting Agenda

- Updates, Status, Progress
  - Policy/process updates (specifically Done policy)
    - https://drive.google.com/drive/folders/1EKGGxVN3s9wZkOcQLxwT_u_daB028wQx
    - https://docs.google.com/spreadsheets/d/1UL6F6ahNwFO69fecLJtnpZatx_PkS-Gdcvb8DdWhWUk/edit#gid=0
  - Adding Asia meeting times
- Discussion:
  - Compliance FAQ - any more comments?
    - write prose that defines what compliance means,
    - what things are we are going to do & what we won't do wrt SAIL
    - make a stab at what "passing" tests vs. "don't pass" tests means
    - delineate between priv & unpriv compliant, they are 2 separate things
  - Specific Compliance Policy/Process Gaps:
    - Criteria for approving merge requests (e.g. coverage, Sail model integration, size, time to run)
    - Certifying compliance: what needs to be in the report? Where does report get sent? (e.g. vendorID/archID)
    - Can we certify actual HW if only its core RTL has passed compliance test?
    - How do we enable configurable & licensed core IP
  - Coverage Spreadsheet
    - critique, review (See: Coverage Rules.xlsx in https://lists.riscv.org/g/tech-compliance/files/Review%20Documents)
  - Migration to Framework v.2
    - Review Pipecleaner tests:What do we need to do to exercise capabilities for Priv Mode tests
    - What steps do we need to complete to cut over to V.2
      (e.g. Sail model updates, pipecleaning, N people have run it, testing all the "fixed in riscof" issues
  - Next steps and Ongoing maintenance
    - Who should provide Tools, e.g. coverage model test generation for new features/extensions
    - Need to Map out order in which tests of ratified spec should be developed next & identify resources (e.g. Priv,FDD or F,Priv,D…)
  - TG Reorganization – subgroups?
    - (more discussion id time permits)

Previous Discussion

Progress:
Chair: Done policy in place. Many compliance points. Review please.
Imp: This will put bitmanip, vector, etc. back by a year. SAIL, compliance tests, etc.
Chair: multiple steps. Some things can be waived.
< discussion about compliance suite, how to get tests >
Imp: Why aren't any companies giving out their test suite?
Chair: CTO is working on getting resources for compliance tests for various extensions.
QC: Where do we stand with current compliance effort (RFQ)?
Chair: Lawyers. Should be done soon.

Discussion:
Compliance FAQ & prose on what compliance means

Gaps
Chair Document to identify gaps (spreadsheets)
??: What about priv spec? (rather than unratified spec)
Imp: Priv spec: problem: what is optional, what is not
Chair: Having discussion with Andrew about this very thing.
e.g. CSR accesses: which accesses trap when CSR is absent?
Have to be backwards compatible
SH: Need to have automation.
Imp: Have been saying that, but overruled.
Chair: Not sure we're talking about the same thing. There will be automation.

Sail
Sail: Who is going to do work for SAIL (etc)?
Chair: for now, each TG has to either do it or find someone to do it. For ratified specs, need to identify where the model fails short, e.g. WARL fields, Big Endian, XLEN changes
Imp: Need a "golden model" group (as opposed to formal model group, to enables cross check, and for scheduling reason – which gets done first.
Chair: There has been one group that has extended SAIL model. Zfinx
Sail: Crypto too? Also, F and D
Chair: F&D are done adequately. We need to scope effort and identify resources for others, e.g. Priv Mode, Vector, etc.

Profile discussion.
Chair: Profile config WG is getting started.
Imp: Need to use riscv-config
Chair: that is being discussed. At worst, there will b a profile->config translator

meeting times
Chair: We have people from India. Worst possible time for Taiwan, China, etc. Perhaps 2 meetings to cover all sites? Security has meetings at 8am and 5pm.
Imp: Record the meetings and follow up with emails. Only way to manage it.

Compliance Certification
QC: What do we call the suite? Arch acceptance test? How do we explain it to users.
Chair: <sharing text of definition of compliance tests>
Chair: this is a first pass
QC: Architectural [verification | validation] suite (ARM)
NK: OpenPower uses "compliance"
CTO: How do we get to closure on names? Please, single word
< discussion of use of "compliance" see below for alternatives >
Imp: We've used this term for years. Industry uses it.
QC: Disagree. Not used throughout industry.
CTO: There is no right answer. Subjective.

Imp: Will this go all the way to the Board to say that an implementation is "compliant"?

QC: TOO risky to say something like, "RISCV compliant". Doubt that legal will support this language. We're *not* certifying. We should say, "this implementation passes these tests" "Certifying" anything is dangerous.
< see notes in "concise compliance" document >

SH: What happens if someone gets a branding, but then they don't pass?
CTO: Terms are overloaded and used in dissimilar ways.
QC: This is about the architecture, not about the tests.

< very lengthy discussion about what we call our tests: compliance, compatible, alignment, interoperability, etc. >

QC: I'll write up another proposal. Put in Google Docs. To kick around.

Replacing the word Compliance :
Compliance has a very specific meaning to some people that might have legal consequences, and there is a request to replace it with something else? .E.g.

Architectural Compliance? - starting point
Architectural Validation? Verification, Conformant conflicting meaning, too strong
Architectural Compatibility – ?Krste is OK with this?
Architectural Test Suite- possibility
Architectural Alignment? – vague
Checked? Interoperable? Intent? Approved ? vague

Should we replace this
- In branding?
- in the repository name?
- anywhere in code that uses the word compliance (e.g. macro , variable, and file names)?
- In documentation?
- In the name of the task group and standing committee??

Previous Decisions & Action Items

Decisions

Each group is responsible for updating Sail and Spike or QEMU, or finding other resources to do it, go to TSC if they can't

Passing vs. not passing: the test report will indicate which tests have passed; trademarks use sill be extension specific and not allowed for failing test. A waiver policy needs to be established for cases where failure is specific and can be worked around (needs blessing of marketing/branding)

Outstanding Action Items- New

QC take a stab at defining Risc-V compliance specifically, replacing "compliance if necessary.

Chair: send poll out for Asian friendly time, see if there is any response. Tentatively planning for meeting twice a month.

Old

Imperas: make pull request for updated assertion macro

Imperas: measure RV32I, vector max memory footprint, number of instructions executed

Stuart: write up coverage taxonomy

TG: read policy docs, send gaps in compliance (e.g. formal model support, possible mismatch between config TG and riscv-config) and priority to cto@riscv.org

Previous Action Items / Progress Update

- ET Base ISA coverage draft spec is uploaded - done – still needs more eyes to review
- SH will add file regarding coverage - no progress….in progress
- Imperas / Incore: ensure headers, macros, dir structure match newest spec, assertions are not inline – waiting for assertion macro update, Imperas pull request
- ET to coordinate with Riscof to determine pipecleaning exercise - to be reviewed in TG
- ET to communicate with TSC about reorganization comments - waiting TSC feedback
- ET/SH to talk w/ SAIL team about transitioning support – in/no progress
- Configuration Structure TG vs. Riscv-Config: discussions underway – see https://github.com/riscv/configuration-structure/

Note: initials are company abbreviations

Test Acceptance Criteria – first cut

Tests must:

- conform to current standard of test spec (macros, labels)
- run in framework
- run with with assertions on and not fail any
- generate a valid signature (that can be saved and compared with other dut/sim)
- has a clear configuration - i.e. which ISA extension it can be used with
- have a code, data, and signature memory footprint that is small enough*
- have run time <X* seconds on simulator running on Intel Corei7 or equiv
- improve coverage
- use only standard instructions
- use only files that are part of the defined support files in the repository
- must be commented, both in header and inside test cases

** need to define "small", "X" ← will vary by extension*

Framework Requirements – first cut

The framework must:

- Use the TestFormat spec and macros described therein
  - (which must work - including assertions)
- Choose test cases according to equations that reference the YAML configuration
- Define macro variables that can be used inside tests based on the YAML configuration
- Include the compliance trap handler, & handle its (separate) signature area
- Load, initialize, and run selected tests between two selected models, extract the signatures, compare results, and write out a report file
- Exist in a riscv github repo, with a few than one maintainer.
- Be easy to get running, e.g.:
  - run under a variety of OSes with the minimum number of distro specific tools.
  - Not require sudo privileges
- Maybe: have the ability to measure and report coverage
  - Coverage specification is a separate file
  - Could be a separate app

ISA Compliance Standing Committee and TG ReOrg

Because both Compliance and Formal Modeling are ongoing processes, the ISA Compliance Standing Committee has been formed to direct the current Compliance and Formal Modelling TGs

Proposal: reorganize the 2 TGs into:

- ISA Compliance Standing Committee sc-compliance-isa@lists.riscv.org
- Compliance Tests Task Group tech-compliance-test@lists.riscv.org
  Charter Statement: Specifying the requirements for the tests (functional coverage), developing the actual test cases, integrating the tests into the framework. (**Deliverable**: Compliance Test Suite)
- Compliance Generators Task Group tech-compliance-generators@lists.riscv.org
  Charter Statement: Develop tools which are configured to generate tests and measure functional coverage. Their tests should meet the requirements specified by the compliance tests task group. (**Deliverable**: Test Tools)
- Compliance Framework Task Group tech-compliance-framework@lists.riscv.org
  Charter Statement: Develop a framework (workflow) that takes a description of an implementation to select/configure tests, runs them, and compares them to the golden model. Manages the output and logging of the tests being run.(Possibly combine for now with generator group? (**Deliverable**: Framework v2)
- Golden Model Task Group tech-golden-model@lists.riscv.org
  Charter Statement: This group will maintain a Formal Specification for the RISC-V ISA. This is a specification of the ISA in a formal language, for precision, unambiguity, consistency and completeness.
  The spec is readable and understandable as a canonical reference by practising CPU architects and compiler writers.
  It is executable and machine-manipulable by tools for establishing correctness and transformations in both compilers and CPU designs.

(……discuss….)

Pull/Issue Status

Issue#	Date	submitter	title	status	
#04	3-Jul-18	kasanovic	Section 2.3 Target Environment	Fixed in RISCOF	
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap		
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed		
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability		
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate		
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG		
#90	11-Feb-20	towoe	Report target execution error		
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	under discussion	
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	under discussion	
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	
pull#113	30-may-20	imphil	Consistently use UNIX line endings	under discussion	
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	
#119	17-jun-20	allenjbaum	Missing RV32i/RV64i test: Fence	Test needs to be written	
#125	15-jul-20	ShashankVM	Request to stop hosting closed source code on riscv repo	under discussion	