

Compliance Task Group Call – Minutes

Weds, 11Jun2020 8am Pacific → Daylight ← Time

See slide 8 for discussions and action items

Charter

The Compliance Task Group will

- Develop compliance tests for RISC-V implementations, taking into account approved specifications for:
 - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
 - Standard Extensions (M,A,F,D,Q,L,C,B,J,T,P,V,N)
 - All spec'ed implementation options
 - (incl. MHSU modes, optional CSRs, optional CSR bits)
- Develop a method for selecting and configuring appropriate tests for a RISC-V implementation, taking into account:
 - Platform profile and Execution Environment (EE)
 - Implemented architecture, extensions, and options
- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
 - test result signature stored in memory will be compared to a golden model result signature

Administrative Pointers

- Chair – Allen Baum allen.baum@esperantotech.com
- Co-chair – Bill McSpadden bill.mcspadden@seagate.com
- TG Email tech-compliance@lists.riscv.org
 - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays
 - See <https://lists.riscv.org/g/tech-compliance/calendar> entry for zoom link
- Documents, calendar, roster, etc. in <https://lists.riscv.org/tech-compliance/>
see /documents, /calendars subdirectories
 - <https://riscof.readthedocs.io/en/latest/> riscof
 - <https://riscv-config.readthedocs.io/en/latest/> config: YAML and WARL spec
- Git repositories
 - <https://github.com/riscv/riscv-compliance/>
 - https://github.com/rsnikhil/Experimental_RISCV_Feature_Model
 - https://github.com/rsnikhil/Forvis_RISCV-ISA-Spec
 - <https://gitlab.com/incoresemi/riscof> (Shakti framework)

(actual) Meeting Agenda

- Updates, Status, Progress
 - Issue status – how do deal with “fixed in riscof” issues (not done)
 - Progress: See next slide
- Discussion:
 - TG Reorganization

Action Items from last meeting

- ET will make sure that formal model can be run in different environments to ensure that RFQ responders can test their code against it – **not done**
- ET will turn coverage draft spec into CSV - **ongoing**
- SH will add file regarding coverage – **ongoing, waiting for above**
- QC will add file re: Compliance Taxonomy – **will be put into files > Review Documents, but needs formal model TG input, but the TG is closed.**
- Imp will produce a coverage CSV in a few weeks – **done, in. files > Review Documents**
- ET arrange to set up google docs folder for collaboration - **in progress, but google docs not available in China**
- Imp AUIPC has already been – **fixed**
- Imp and Risconf will coordinate to make sure headers, macros, directory structure match newest spec, assertions are not inline – **not done yet**
- Also from the previous meeting: Risconf will review the std_trap_handler – **done, integration is the next step**

Note: initials are company abbreviations

ISA Compliance Standing Committee and TG ReOrg

Because both Compliance and Formal Modeling are ongoing processes, the ISA Compliance Standing Committee has been formed to direct the current Compliance and Formal Modelling TGs

Proposal: reorganize the 2 TGs into:

- ISA Compliance Standing Committee sc-compliance-isa@lists.riscv.org
- Compliance Tests Task Group tech-compliance-test@lists.riscv.org
Charter Statement: Specifying the requirements for the tests (functional coverage), developing the actual test cases, integrating the tests into the framework. (**Deliverable:** Compliance Test Suite)
- Compliance Generators Task Group tech-compliance-generators@lists.riscv.org
Charter Statement: Develop tools which are configured to generate tests and measure functional coverage. Their tests should meet the requirements specified by the compliance tests task group. (**Deliverable:** Test Tools)
- Compliance Framework Task Group tech-compliance-framework@lists.riscv.org
Charter Statement: Develop a framework (workflow) that takes a description of an implementation to select/configure tests, runs them, and compares them to the golden model. Manages the output and logging of the tests being run. (Possibly combine for now with generator group? (**Deliverable:** Framework v2)
- Golden Model Task Group tech-golden-model@lists.riscv.org
Charter Statement: This group will maintain a Formal Specification for the RISC-V ISA. This is a specification of the ISA in a formal language, for precision, unambiguity, consistency and completeness. The spec is readable and understandable as a canonical reference by practising CPU architects and compiler writers. It is executable and machine-manipulable by tools for establishing correctness and transformations in both compilers and CPU designs.

(.....discuss.....)

Discussion

- **Std Interrupt handler:**

- Needs handlers per mode since each vectors differently & saves only the CSRs corresponding to its mode
 - Not possible to tell which mode you're in, else can't virtualize
 - e.g. Smode handlers can only access Smode CSRs

- **"Platform" :**

QC: misusing "platform" term in RISCOF YAML descriptions. "Platform.yaml" needs renaming.
IMP: current is ok. Describes something outside of core like MMIO regs
VNT: platform vs. platform standard: use "system" or "environment"
QC: my document will differentiate between them
(many) Possible terms: system, harness, testbench
IMP: need a standard way to define config between all groups.
SG: That is partly what the tech-config group is trying to solve, but has different focus with different solutions. They must be interoperable however

- Action items: QC to ask Andrew for term change

- **Reorganization:** into Tests, Generators, Framework, and Model Task Groups under ISA Compliance Standing Committee

- This means 3x the number of meetings
- My company won't support going to that many meetings
- we get parallelization efficiency?
These groups have interdependencies in both directions,
They're interest groups that all need to be done in parallel; splitting them may not help
- Would we get more participation or less?
- Each of these are a significant amount of work - do we have the resources to do that work?
Few companies are committing resources, but each group will need some
No company is required to commit resources, but each will want to use the results.
"Projects need funding if you want them to get done"

- **Imp and Riscof coordination:**

- needs a pipecleaning exercise that uses YAML and formal model in a way that current framework cannot (e.g. see issue list).
- Should be in a privileged mode test that can't be tested with the current framework.
- We need to show that the flow actually works. We don't really know how good the SAIL model is for this, but need to use it as it is the golden model. (cf: email from the SAIL team about transitioning to maintenance)

SH: model: not easy to use/ configure.

Needs more docs how exactly do you add a new instruction?
(see: email from the SAIL team with links to documentation)

Full time engineer is needed to add ops, etc. Possibilities were named:
(redacted) or (redacted) (Oxford professor interested in success of sail model).

"Projects need funding if you want them to get done"

- **Compliance on actual hardware:**

IMP: Impossible (also see Issue #115)

Ratified Test Format Spec sec 3.9: The *test target* can be either a RISC-V Instruction Set Simulator (ISS), a RISC-V emulator, a RISC-V RTL model running on an HDL simulator, a RISC-V FPGA implementation or a physical chip.

Decisions & Action Items

Decisions

Rename from “Std_trap_handler” to Compliance_<mode>TrapHandler
(where mode= M,S,U; eventually probably H as well)

Action Items

QC: to ask Andrew for term change re: platform

ET: to coordinate with Riscof for Interrupt handler integration, and modify TestFormat spec as needed

ET to coordinate with Riscof to determine pipecleaning exercise

ET to communicate with TSC about reorganization comments

ET/SH to talk with SAIL team about transitioning support to the Foundation

Pull/Issue Status

Issue#	Date	submitter	title	status	
#04	3-Jul-18	kasanovic	Section 2.3 Target Environment	Fixed in RISCOF	
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap		
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed		
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability		
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate		
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG		
#90	11-Feb-20	towoe	Report target execution error		
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	under discussion	
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	under discussion	
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	
pull#113	30-may-20	imphil	Consistently use UNIX line endings	under discussion	
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	