Compliance Task Group Call – Minutes

Weds, 23Jun2020 8am Pacific →Daylight← Time

See slide 8 for discussions and action items

Charter

The Compliance Task Group will

- Develop compliance tests for RISC-V implementations, taking into account approved specifications for:
  - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
  - Standard Extensions (M,A,F,D,Q,L,C,B,J,T,P,V,N)
  - All spec'ed implementation options
    - (incl. MHSU modes, optional CSRs, optional CSR bits)
- Develop a method for selecting and configuring appropriate tests for a RISC-V implementation, taking into account:
  - Platform profile and Execution Environment (EE)
  - Implemented architecture, extensions, and options
- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
  - test result signature stored in memory will be compared to a golden model result signature

Adminstrative Pointers

- Chair – Allen Baum allen.baum@esperantotech.com
- Co-chair – Bill McSpadden bill.mcspadden@seagate.com
- TG Email tech-compliance@lists.riscv.org
  - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays
  - See https://lists.riscv.org/g/tech-compliance/calendar entry for zoom link
- Documents, calendar, roster, etc. in https://lists.riscv.org/tech-compliance/
  see /documents & /calendars subdirectories
  - https://riscof.readthedocs.io/en/latest/ riscof
  - https://riscv-config.readthedocs.io/en/latest/ config: YAML and WARL spec
- Git repositories
  - https://github.com/riscv/riscv-compliance/
  - https://gitlab.com/incoresemi/riscof (riscof framework)

Meeting Agenda

- Updates, Status, Progress
  - Issue status – how do deal with “fixed in riscof” issues (not done)
  - Progress: See next slide
- Discussion:
  - Coverage Spreadsheet
    - critique, review
    - (See: Coverage Rules.xlsx in https://lists.riscv.org/g/tech-compliance/files/Review%20Documents)
  - Pipecleaner tests for Framework v.2
    - What do we need to do to exercise capabilities for Priv Mode tests
  - Test Generator (over time, not covered)
    - Compliance Tests are supposed to be provided by the TG that proposes an extension
      - Ratified specs need a different approach…..
    - We need to provide tools to enable test generation: what should it look like?
  - TG Reorganization
    - (more discussion id time permits)

Action Item / Progress Update

- ET will make sure that formal model can be run in different environments to ensure that RFQ responders can test their code against it –done, multiple examples
- ET will turn coverage draft spec into CSV - first pass done and tested. Needs more discussion
- SH will add file regarding coverage – no progress….
- QC will add file re: Compliance FAQ –draft in
  https://lists.riscv.org/g/tech-compliance/files/Review%20Documents/Compliance%20FAQs.pdf
- ET arrange to set up google docs folder for collaboration - will be located in CTO folder by next week
- Imperas and Incore will coordinate to make sure headers, macros, dir structure match newest spec, assertions are not inline – done, except assertion macro update, waiting Imperas pull request
- QC: to ask Andrew for term change re: platform – has morphed into a need for Risc-V official glossary & index. Needs some tool work in specs. This may be a test case for google docs site?
- ET: to coordinate w/ Riscof for Interrupt handler integration - done
- ET to coordinate with Riscof to determine pipecleaning exercise- done, needs review
- ET to communicate with TSC about reorganization comments- ran out of time
- ET/SH to talk with SAIL team about transitioning support to the Foundation- not started

Note: initials are company abbreviations

Discussion

- **Formal Model**:
  - not complete; doesn't cover everything needed for full compliance.
  - CTO: TGs don't "graduate" but go into email mode, need to decide if groups need to restart
    Q: who has ownership, what is communication channel?
  - CTO: This is example of a gap; please send perceived gaps and priorities to cto@riscv.org

- "**Platform" Terminology** :
  Request for a cross-spec glossary and index. Specifically for def of "platform"

  CTO: Yes, needed. We will create index and glossary.
  Imp: This is a terminology overload problem, not a mechanical problem.
  CTO: The glossary is intended to adjudicate overlap. There are other issues in today's env, e.g. Need to avoid certain terms (master/slave)

- "**Configuration**" :
  Imp: need a general RISC-V config that follows RISC-V config, as used in compliance. (which follows the def of platform/device etc.)
  CTO: yes. Profile specification, which defines what needs to be present
  Imp: This is about the the hundreds of ISA options. See RISC-V Config version 2.
  (note: a profile is defined in terms of the ISA options, among other things)
  (Discussion of the tech-config TG purpose, etc.)
  IMP: Deadline for this specification?
  CTO: Longer then we want. But there is urgency. Compliance needs to attend
  Chair: Both co-chairs are attending, and riscv-config TG is aware of riscv-configuration repository and tools

- **Coverage:**
  Imp: need to get promised docs written. Have tested current test suite using draft coverage spreadsheet; coverage dropped from 97% to 35%
  Chair: note that overage spreadsheet still needs more review, updates, suggestions, corrections, etc - and is specific to base ISA only.

- **Pipecleaning of framework V.2**
  (pipecleaning == path clearing)
  IMP What is this intended to show? (surprised&impressed with quality and usefulness of compliance trap handler)\
  (Chair: CLIC extension will completely break this….)
  InCore: demonstrates dynamic comparison of two models, and test selection/configuation via YAML descriptions
  IMP: multiple test cases in a test makes framework more complex, need a good example of test that needs this, not convinced this is right approach
  Incore: Example is in our repository: misalign ld/st/br. Some test cases not run if no C- ext, different signatures depending on HW misalign support. Selecting entire tests, or parts of a test, or in a hierarchy uses exactly the same mechanism. Not too useful until we start priv level tests.
  IMP: doesn't show what you think it shows
  (will be resolved offline)

Decisions & Action Items

Decisions

We will settle terminology overloading by defining terms in a glossary; [All but one] overloaded uses will need to change their wording.

Action Items

Stephano: add folder to Risc-V CTO googledoc, and set sharing by mid-next week

CTO/Stephano: set up a glossary/index site and process and communicate it?

Imperas: make pull request for updated assertion macro

Stuart: write up coverage taxonomy

Bill Mc: look at RISC-V- config tools and pass along to config TG.

Chair: send poll to see if we want an off-cycle meeting to discuss items we didn't get to: Test Generator, Coverage Spreadsheet, Reorg

Everybody: send gaps in compliance (e.g. formal model support, possible mismatch between config TG and riscv=config) and priority to cto@riscv.org

ISA Compliance Standing Committee and TG ReOrg

Because both Compliance and Formal Modeling are ongoing processes, the ISA Compliance Standing Committee has been formed to direct the current Compliance and Formal Modelling TGs

Proposal: reorganize the 2 TGs into:

- ISA Compliance Standing Committee sc-compliance-isa@lists.riscv.org
- Compliance Tests Task Group tech-compliance-test@lists.riscv.org
  Charter Statement: Specifying the requirements for the tests (functional coverage), developing the actual test cases, integrating the tests into the framework. (**Deliverable**: Compliance Test Suite)
- Compliance Generators Task Group tech-compliance-generators@lists.riscv.org
  Charter Statement: Develop tools which are configured to generate tests and measure functional coverage. Their tests should meet the requirements specified by the compliance tests task group. (**Deliverable**: Test Tools)
- Compliance Framework Task Group tech-compliance-framework@lists.riscv.org
  Charter Statement: Develop a framework (workflow) that takes a description of an implementation to select/configure tests, runs them, and compares them to the golden model. Manages the output and logging of the tests being run.(Possibly combine for now with generator group? (**Deliverable**: Framework v2)
- Golden Model Task Group tech-golden-model@lists.riscv.org
  Charter Statement: This group will maintain a Formal Specification for the RISC-V ISA. This is a specification of the ISA in a formal language, for precision, unambiguity, consistency and completeness.
  The spec is readable and understandable as a canonical reference by practising CPU architects and compiler writers.
  It is executable and machine-manipulable by tools for establishing correctness and transformations in both compilers and CPU designs.

(……discuss….)

Pull/Issue Status

Issue#	Date	submitter	title	status	
#04	3-Jul-18	kasanovic	Section 2.3 Target Environment	Fixed in RISCOF	
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap		
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed		
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability		
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate		
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG		
#90	11-Feb-20	towoe	Report target execution error		
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	under discussion	
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	under discussion	
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	
pull#113	30-may-20	imphil	Consistently use UNIX line endings	under discussion	
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	
#119	17-jun-20	allenjbaum	Missing RV32i/RV64i test: Fence	Test needs to be written	