Compliance Task Group Call – Agenda

Thur, 22Oct2020 8am Pacific →Daylight← Time

See slide 6 for agenda

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We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate.

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/risc-v-international-community-code-of-conduct/

Charter

The Compliance Task Group will

- Develop? compliance tests for RISC-V implementations, taking into account approved specifications for:
  - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
  - Standard Extensions (H,S,U,A,B,C,D,F,J,K,M,N,P,Q,T,V,N), Priv Mode ← change to only ratified spec as of this date
  - All spec'ed implementation options
    - (incl. MHSU modes, optional CSRs, optional CSR bits)

- Develop a method for selecting <u>and</u> configuring appropriate tests for a RISC-V implementation, taking into account:
  - Platform profile and Execution Environment (EE)
  - Implemented architecture, extensions, and options

- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
  - test result signature stored in memory will be compared to a golden model result signature

Adminstrative Pointers

- Chair – Allen Baum   allen.baum@esperantotech.com
- Co-chair – Bill McSpadden   bill.mcspadden@seagate.com
- TG Email   tech-compliance@lists.riscv.org
  - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays.
  - See https://docs.google.com/spreadsheets/d/1L15_gHl5b2ApkcHVtpZyl4s_A7sgSrNN zoom link
- Documents, calendar, roster, etc. in
  - https://lists.riscv.org/tech-compliance/   see /documents & /calendars subdirectories
  - https://riscof.readthedocs.io/en/latest/   riscof
  - https://riscv-config.readthedocs.io/en/latest/   config: YAML and WARL spec
  - https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUlEs
    (lifecycle in "policies/supporting docs" folder, gaps in "planning" folder, compliance specific in "compliance folder")
- Git repositories
  - https://github.com/riscv/riscv-compliance/
  - https://gitlab.com/incoresemi/riscof (riscof framework)
  - https://github.com/riscv/riscv-config/
  - https://github.com/rems-project/sail-riscv/ (Sail formal model)
- JIRA: https://jira.riscv.org/projects/CSC/issues/CSC-1?filter=allopenissues

Meeting Agenda

0. **Looking for admins, maintainers for riscv-compliance git repo !!**

I.   Updates, Status, Progress

II.   Continued Discussion: Merging new Base ISA tests – what is left

III. Next steps and Ongoing maintenance

    1. Migration to Framework v.2. video: https://youtu.be/VIW1or1Oubo,
        slides: https://lists.riscv.org/g/tech-compliance/files/Presentations/TestFormatSpec.pdf

        • What steps do we need to complete to cut over to V.2 (see slide 12)
            -   (e.g. ~~Sail model updates,~~ pipecleaning, N people have run it, testing all the "fixed in riscof" issues
            - Review Pipecleaner tests:What do we need to do to exercise capabilities for Priv Mode tests

    2. Moving all model proposal to remove all model specific support code out of riscv-compliance repo

    3. Specific Compliance Policy/Process Gaps:
        1. Develop SAIL maintenance plan
        2. Certifying passing architecture tests: what needs to be in the report? Where does report get sent? (e.g. vendorID/archID)
        3. Can we certify actual HW if only its core RTL has passed architecture tests?
        4. How do we enable configurable & licensed core IP
        5. Identify Tool providers, e.g. coverage model, test generation for new features/extensions
        6. Flesh out test development order & identify resources (e.g. Priv,FDD or F,Priv,D…, JIRA CSC-3,5
        7. Provide a reference RTL test fixture (as opposed to SW functional model). See.   JIRA CSC-6

Discussion

Pre-agenda:
IMP: We need more money for tests.
CTO: Every group who needs tests needs to find the resource. Looking for remedial support for extensions that are already ratified. Looking for companies to contribute resources for extensions of interest.
INCORE: Do we have a timeline for when tests should be written?
   CTO: Yes. **Chair** has documented in Definition-of-Done checklist.
INCORE: Request: Where do I find this?
   https://docs.google.com/spreadsheets/d/1UL6F6ahNwFO69fecLJtnpZatx_PkS-Gdcvb8DdWhWUk/edit#gid=0
CTO: Concept of "Horizontals": RAS, Performance, etc. Formal Models. We need to figure out:
how to cover Formal Models for extensions with no Formal, and how to cover new extensions.
SAIL: Need resources with the proper skills (arch knowledge)
   CTO: Need to try and find the proper architects. Archs are few. Will be hard to find.
     Linaro (www.Linaro.org, set up by ARM) had to solve this problem, but Calista wants Linux model,
     not Linaro model. Call for ideas on how to solve this general model.

This TG needs github on admins and maintainers.
Co-Chair: has volunteered. He is applying new core to new test - pilot error has been primary problem.
  Ensuring private implementation details are kept private has had teething problems
IMP: agree -developers should not have to come back to TG
CoChair: details forthcoming: our wrapper - main difference: compile+run separation. Autoconf was easy;
our makefile version is much more difficult
   AR- **Co-Chair:** submit ticket issue

New extension tests progress
CHAIR: Crypto is getting involved.
Crypto: Scalar/crypto testplan. See:
   https://github.com/riscv/riscv-crypto/blob/master/tests/compliance/test-plan-scalar.adoc
CHAIR: Cornercases are most important. But I don't have any idea what corner cases would be for crypto
QC: What documentation for what we should be going after?
   Chair/IMP: Isn't that the FAQ you (QC) wrote up?
QC: I'll see what bits I can pull out. AR- **QC: extract bits of FA\Q as guidelines for test writing**
CHAIR: There is a place to put this stuff.
   https://sites.google.com/a/riscv.org/risc-v-staff--> information directory->content->compliance

RFQ test merging
IMP: What about the data propagation report? Published?
   INCORE: Coverage/data propagation will be put into the repo. Automatically generated &
available on the web.
     https://htmlpreview.github.io/?
     https://github.com/incoresemi/riscv-compliance/blob/dev/coverage/rv32i_m/I/coverage.html
IMP: Can i browse to it?
   INCORE: You have to download and look.
IMP: It needs to be available via the web. Use markdown. It's trivial.
    INCORE: I'll look into this and give feedback.

Next steps for riscof:
CHAIR: We need other people to start using it.
INCORE: It's ready to use
   https://gitlab.com/incoresemi/riscof   (riscof framework)
   https://riscof.readthedocs.io/en/latest/   (riscof docs)
   https://github.com/riscv/riscv-config/   (riscv-config)
   https://riscv-config.readthedocs.io/en/latest/   (riscv-config:YAML/WARL spec
Crypto : It's confusing and complicated that the architectural test framework is not part of
RISC-V github. Plans to consolidate?
   CHAIR: This is a development branch; it will be moved when merged.
Crypto : This should also be in the README in the existing github.
   AR- **Incore: add text to Readme pointing to riscof**
CHAIR: Pipecleaning exercise.
   INCORE: SAIL model updates have been done.
CHAIR: What about "fixed in riscof"?
   INCORE: Let's take it up in the next call.
CHAIR: Pipecleaner tests for misaligned test?
   INCORE: There are 4 tests. One of which covers this.
CHAIR: How does SAIL handle support of mis-aligned addresses?
   SAIL: I imagine it's in the YAML stuff that we did.
   It's in a different branch, uses v1.0, but latest config spec currently up to v2.4.1
   SAIL team, author has moved on (may not even be able to fix anything?)
   AR- **Incore:** Try YAML version of SAIL to see if it works,

Decisions & Action Items

Decisions

Outstanding Action Item

Chair/CTO: discuss requirement for HW impl. before merge <done>
Chair/CTO : identify responsibilities/resources for "remedial" tests <done>

Chair : discuss with repo admins and maintainers where staging area is, and if model specific files will be moving (now or for v.2 framework) <N/A>
Chair : get contact info for all model maintainers and inform them of new merging process <not done>

NEW
Chair/Incore: update test format spec with macro, entry, exit changes <?>
Co-Chair: submit ticket issue RE: doc updates for splitting compile/run <done?>
QC: extract bits of FAQ as guidelines for test writing
Incore: add text to current github Readme pointing to riscof <done>
Incore: Try YAML version of SAIL to see if it works

Old

[everybody]: comment on base ISA cover points:

https://github.com/incoresemi/riscv-compliance/tree/dev/coverage

(this is needed to complete the TG's responsibilities for the RFQ)

Imperas: make pull request for updated assertion macro

SH: write up coverage taxonomy

Everybody: read policy docs, send gaps in compliance (e.g. formal model support, possible mismatch between config TG and riscv-config) and priority to cto@riscv.org

Architectural Test Rationale – Intent and Limits

RISC-V Architectural Tests are an evolving set of tests that are created to help ensure that SW written for a given RISC-V Profile will run on all implementations that comply with that profile.

These tests also help ensure that the implementer has both understood and implemented the specification.

The RISC-V Architectural Tests test suite is a minimal filter. Passing the tests and having the results approved by RISC-V International is a prerequisite to licensing the RISC-V trademarks in connection with the design.

Passing the RISC-V Architectural Tests does *not* mean that the design complies with the RISC-V Architecture. These are only a basic set of tests.

The RISC-V Architectural Tests are *not* a substitute for rigorous design verification; it is the responsibility of the implementer to deploy extensive testing.

To be added to the riscv/riscv-compliance/doc/ directory as "RISC-V Architectural Test Rationale"

Test Acceptance Criteria – second cut

Tests must:

- conform to current standard of test spec (macros, labels)
- run in framework
- run in SAIL and not fail any tests
- Report that test results propagate to signature
- generate a valid signature using SAIL (that can be saved & compared with another DUT/sim)
- has a clear configuration - i.e. which ISA extension it can be used with

improve coverage

- use only standard instructions (fixed size per architecture LI, LA allowed)
- use only files that are part of the defined support files in the repository
- must be commented test_case header

Framework Requirements – first cut

The framework must:

- Use the TestFormat spec and macros described therein
  - (which must work - including assertions)
- Choose test cases according to equations that reference the YAML configuration
- Define macro variables that can be used inside tests based on the YAML configuration
- Include the compliance trap handler, & handle its (separate) signature area
- Load, initialize, and run selected tests between two selected models, extract the signatures, compare results, and write out a report file
- Exist in a riscv github repo, with a few than one maintainer.
- Be easy to get running, e.g.:
  - run under a variety of OSes with the minimum number of distro specific tools.
  - Not require sudo privileges
- Maybe: have the ability to measure and report coverage
  - Coverage specification is a separate file
  - Could be a separate app

Pull/Issue Status

Issue#	Date	submitter	title	status	comments
#04	3-Jul-18	kasanovic	Section 2.3 Target Environment		
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap		
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed		
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability	Fixed in RISCOF	
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate		
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG		
#90	11-Feb-20	towoe	Report target execution error		
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	under discussion	
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	under discussion	
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	
#119	17-jun-20	allenjbaum	Missing RV32i/RV64i test: Fence	Test has been written under discussion	Close when test is merged
#125	15-jul-20	ShashankVM	Request to stop hosting closed source code on riscv repo		
pull#128	29-jul-20	nmeum	grift: update for new directory structure		Who can review this?
pull#129	31-jul-20	nmeum	sail-riscv-ocaml: Disable RVC extension on all devices not using it		Who can review this?
#132	15-aug-20	davidmlw	Why not just use mepc for mret?	answered	Should be resolved
#135	04-sep-20	MikeOpenHWGroup	Request for a Tag on this Repo	assigned	

JIRA Status

Issue#	Date	submitter	title	status	comments
IT-1	27Aug/20	Allen Baum	Need to modify the description of compliance in https://riscv.org/technical/specifications/	done	
IT-4	01/Sep/20	Allen Baum	Add Jira link to TG home pages	In prog	
CSC-1	20/Aug/20	Ken Dockser	Come up with names for the tests suites that we are creating		1st step done
CSC-2	20/Aug/20	Ken Dockser	Produce concise text to explain the Architecture Tests intent and Limits		Written, needs pull req
CSC-3	20/Aug/20	Ken Dockser	Come up with an internal goal for what we wish to accomplish with the Architectural Tests		Not written
CSC-4	20/Aug/20	Ken Dockser	Develop a roadmap for all the different categories of test suites that will need to be created		Not written
CSC-5	20/Aug/20	Ken Dockser	Develop a roadmap for releases of single-instruction Architecture Tests		Not written
CSC-6	20/Aug/20	Ken Dockser	Develop a reference RTL test fixture that can stimulate and check the CPU under test		Needs more discussion