Compliance Task Group Call – Minutes

Thur, 06Aug2020 8am Pacific →Daylight← Time

See slide 4 for agenda

Charter

The Compliance Task Group will

- Have compliance tests written for RISC-V implementations, taking into account approved specifications for:
  - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
  - Standard Extensions (H,S,U,A,B,C,D,F,H,J,M,N,P,T,V,N), Priv Mode
  - All spec'ed implementation options
    - (incl. MHSU modes, optional CSRs, optional CSR bits)

- Develop a method for selecting <u>and</u> configuring appropriate tests for a RISC-V implementation, taking into account:
  - Platform profile and Execution Environment (EE)
  - Implemented architecture, extensions, and options

- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
  - test result signature stored in memory will be compared to a golden model result signature

Adminstrative Pointers

- Chair – Allen Baum   allen.baum@esperantotech.com
- Co-chair – Bill McSpadden   bill.mcspadden@seagate.com
- TG Email   tech-compliance@lists.riscv.org
  - Notetakers: please send emails to allen.baum@esperantotech.com
- Meetings -Bi-monthly at 8am Pacific time on 2nd/4th Wednesdays
  - See https://lists.riscv.org/g/tech-compliance/calendar entry for zoom link
- Documents, calendar, roster, etc. in
  - https://lists.riscv.org/tech-compliance/   see /documents & /calendars subdirectories
  - https://riscof.readthedocs.io/en/latest/   riscof
  - https://riscv-config.readthedocs.io/en/latest/   config: YAML and WARL spec
  - https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUlEs
    (lifecycle in "policies/supporting docs" folder,   gaps in "planning" folder,
    compliance specific in "compliance folder")
  - https://drive.google.com/drive/folders/1EKGGxVN3s9wZkOcQLxwT_u_daB028wQx
    - Compliance specific files, e.g. FAQ, coverage
- Git repositories
  - https://github.com/riscv/riscv-compliance/
  - https://gitlab.com/incoresemi/riscof (riscof framework)

Meeting Agenda

- Updates, Status, Progress
  - Policy/process updates (specifically Done policy)
    - https://drive.google.com/drive/folders/1EKGGxVN3s9wZkOcQLxwT_u_daB028wQx
    - https://docs.google.com/spreadsheets/d/1UL6F6ahNwFO69fecLJtnpZatx_PkS-Gdcvb8DdWhWUk/edit#gid=0
  - Adding Asia meeting times

- Discussion:
  - Compliance FAQ - any more comments?
    - write prose that defines what compliance means,
    - what things are we are going to do & what we won't do wrt SAIL
    - make a stab at what "passing" tests vs. "don't pass" tests means
    - delineate between priv & unpriv compliant, they are 2 separate things
  - Specific Compliance Policy/Process Gaps:
    - Criteria for approving merge requests (e.g. coverage, Sail model integration, size, time to run)
    - Certifying compliance: what needs to be in the report? Where does report get sent? (e.g. vendorID/archID)
    - Can we certify actual HW if only its core RTL has passed compliance test?
    - How do we enable configurable & licensed core IP
  - Coverage Spreadsheet
    - critique, review (See: Coverage Rules.xlsx in https://lists.riscv.org/g/tech-compliance/files/Review%20Documents)
  - Migration to Framework v.2
    - Review Pipecleaner tests:What do we need to do to exercise capabilities for Priv Mode tests
    - What steps do we need to complete to cut over to V.2
      (e.g. Sail model updates, pipecleaning, N people have run it, testing all the "fixed in riscof" issues
  - Next steps and Ongoing maintenance
    - Who should provide Tools, e.g. coverage model test generation for new features/extensions
    - Need to Map out order in which tests of ratified spec should be developed next & identify resources (e.g. Priv,FDD or F,Priv,D...)
  - TG Reorganization – subgroups?
    - (more discussion id time permits)

Discussion

Progress:
2nd&4th Thursday at 8amPT is new meeting time BUT :we'll be meeting weekly for a while.
"Done Policy" - in review in tech-chairs. Compliance members should take a look:
https://docs.google.com/document/d/13mCiwJFiGvoQoLnk78HFUJrxxaOvbPeWBL2ktSGAY5_s/edit?ts=5f2d722d&pli=1#

Discussion: Compliance FAW & prose on what compliance means

Chair: Draft prose: Passing compliance tests for Risc-V indicates that the implementer has read and understood the Risc-V ISA spec. Compliance is not a substitute for design verification; that is necessary in any case.
     It will be possible to pass compliance tests and still have (hopefully obscure) bugs. Rather passing compliance tests indicates that, even having passed implementor DV tests, that those DV tests have the correct interpretation of the ISA spec.

VNT2: request. Can FAQ be ascii docs so that we can comment, "code review"?
   CTO: Google Drive exists for Google docs. Else, put in github
   A.I. for Ken: move doc to google drive with suggestion privs. **(Done)**

Discussion: what things are we going to do & not do on Sail (see decisions)
Met with Peter Sewell. Asynchronous events are hard to model, though not intrinsically more difficult than other models
Chair: perhaps async events are DV, not compliance?
Discussion about how to do deterministic behavior for async events.
Chair: Events between concurrent HARTs is the hard case.
   VNT1: We have Memory model litmus tests
Chair: that doesn't test the hard case with other memory accessing.
   The problem is controlling when an event occurs in two completely different models to produce the same effect, e.g. force an interrupt to occur between 2 specific instructions, or memory accesses to occur in a specific order when running multiple concurrent harts on two sets of models
   Co-chair: Can we provide assertions?
   Sail: Check to see if implementation results are in the set of allowed results?
   VNT2: Run litmus tests (7K tests) once; Ensure all result allowed. DV does randomization.
Chair: we can't guarantee that we can actual force all the possible ordering
   QC: create a sample env for memory ordering test
Sail: why test a single core for memory ordering test?
   CTO: i'm looking at compliance tests as a core test (single HART test)
   VNT1, 2: description of ARM method, ARM testbench is really an ABI

Chair: ARM can do this, they own their cores; can we?
   VNT2: ARM did this for their customers implementation. ARM supplies the ABI
   QC: ARM provides a reference platform. Customer can create their own.
Chair: This is the of approach I'd like to see. What is needed in order to build an ABI?
CTO: Don't stop the specification for single HART solution in lieu of specifying solution for multi-HART concurrency.
   Chair: yes, absolutely, single HART solutions come first. This is longer term.
CTO: What about the availability of other tests, open-source. Like FP tests from IBM. For each piece, we need a name to refer to the stuff that will be delivered in order to track and in order to talk to the rest of the world
               .(KD wrote IBM's tests) Discussion of KD's doc [for FP tests???]

Discussion: what does passing/not passing compliance means
Q: Can companies use trademark if didn't pass?
Q: list each spec version numbers? Or just extension name of passing tests?
Chair: Krste does not want version numbers. Just wants extension string. This will be addressed in a policy. Example: what happens if we find a security bug in the M extension, how do we specify so that we make sure that security problem is addressed?
VNT2: need version numbers of compliance suite so that customers can claim which set of tests passed.
               Discussion of git SHA handle used for version.
VNT2: What is errata? What is pass/don't-pass? Need definition.
Sail: RVI needs to take some stance if customer's test pass, yet there is some bad errata. RVI has some responsibility.
VNT2: We don't go back and re-factor tests.
Incore: Q: what happens to a customer if tests change? Do they have to re-certify? AB: They can. Else they were compliant with version N-1 of the tests.
VNT2: may need to deprecate versions of compliance tests.
VNT2- need semantic versioning for soft core upgrades

Discussion: priv vs. unpriv tests
Chair: unpriv and priv are separate sets of tests
 - unprivileged test don't trap - make that clear (where?)
 - there will be priv tests for the same ops that can trap
 - ecall and ebreak are special cases; alignment traps might be another (since load/store alignment support or not is an unprivileged option)

Decisions & Action Items

Decisions

Meetings moving to 8am PDT Thursday instead of Weds.

Off cycle meeting will be scheduled to catch up on agenda items.

We are not bound to use only SAIL to get golden results initially

We can put limits on what we will test if corner cases are too difficult (e.g. concurrency)

Ensure that unpriv tests don't trap, with EBREAK, ECALL, an alignment exceptions

Outstanding Action Items

TG: write prose that defines what compliance means,

TG : what things are we are going to do & what we won't do wrt SAIL

TG : make a stab at what "passing" tests vs. "don't pass" tests means

TG: delineate between priv & unpriv compliant, they are 2 separate things

Imperas: make pull request for updated assertion macro

Imperas: measure RV32I, vector max memory footprint, number of instructions executed

Stuart: write up coverage taxonomy

Chair: get architectural hazard pointer – done, explicit for branches, but only implicit for register ops

TG: read policy docs, send gaps in compliance (e.g. formal model support, possible mismatch between config TG and riscv-config) and priority to cto@riscv.org

Ken: move Compliance to google (done, link is: https://docs.google.com/document/d/1U6qTBGhaR5hipxxC5z7-L2GQazAXhe79sgc3KscNme8/)

***Please use suggesting mode only*!**

Previous Action Items / Progress Update

- <u>ET</u> Base ISA coverage draft spec is uploaded   - done – needs more eyes to review

- <u>SH</u> will add file regarding coverage   - no progress….in progress

- <u>Imperas / Incore:</u> ensure headers, macros, dir structure match newest spec, assertions are not inline – waiting for assertion macro update, Imperas pull request

- <u>ET</u> to coordinate with Riscof to determine pipecleaning exercise - to be reviewed in TG

- <u>ET</u> to communicate with TSC about reorganization comments   - waiting TSC feedback

- <u>ET/SH</u> to talk w/ SAIL team about transitioning support to Foundation - in progress

- Configuration Structure TG vs. Riscv-Config: discussions underway – see
    https://github.com/riscv/configuration-structure/

Note: initials are company abbreviations

Test Acceptance Criteria – first cut

Tests must:

- conform to current standard of test spec (macros, labels)
- run in framework
- run with with assertions on and not fail any
- generate a valid signature (that can be saved and compared with other dut/sim)
- has a clear configuration - i.e. which ISA extension it can be used with
- have a code, data, and signature memory footprint that is small enough*
- have run time less than X instructions
- improve coverage
- use only standard instructions
- use only files that are part of the defined support files in the repository
- must be commented, both in header and inside test cases

    *need to define "small". ** need to define "X"*

Framework Requirements – first cut

The framework must:

- Use the TestFormat spec and macros described therein
  - (which must work - including assertions)
- Choose test cases according to equations that reference the YAML configuration
- Define macro variables that can be used inside tests based on the YAML configuration
- Include the compliance trap handler, & handle its (separate) signature area
- Load, initialize, and run selected tests between two selected models, extract the signatures, compare results, and write out a report file
- Exist in a riscv github repo, with a few than one maintainer.
- Be easy to get running, e.g.:
  - run under a variety of OSes with the minimum number of distro specific tools.
  - Not require sudo privileges
- Maybe: have the ability to measure and report coverage
  - Coverage specification is a separate file
  - Could be a separate app

ISA Compliance Standing Committee and TG ReOrg

Because both Compliance and Formal Modeling are ongoing processes, the ISA Compliance Standing Committee has been formed to direct the current Compliance and Formal Modelling TGs

Proposal: reorganize the 2 TGs into:

- ISA Compliance Standing Committee   sc-compliance-isa@lists.riscv.org

- Compliance Tests Task Group   tech-compliance-test@lists.riscv.org
  Charter Statement: Specifying the requirements for the tests (functional coverage), developing the actual test cases, integrating the tests into the framework.   (**Deliverable**: Compliance Test Suite)

- Compliance Generators Task Group   tech-compliance-generators@lists.riscv.org
  Charter Statement: Develop tools which are configured to generate tests and measure functional coverage. Their tests should meet the requirements specified by the compliance tests task group. (**Deliverable**: Test Tools)

- Compliance Framework Task Group   tech-compliance-framework@lists.riscv.org
  Charter Statement: Develop a framework (workflow) that takes a description of an implementation to select/configure tests, runs them, and compares them to the golden model. Manages the output and logging of the tests being run.(Possibly combine for now with generator group?   (**Deliverable**: Framework v2)

- Golden Model Task Group   tech-golden-model@lists.riscv.org
  Charter Statement: This group will maintain a Formal Specification for the RISC-V ISA. This is a specification of the ISA in a formal language, for precision, unambiguity, consistency and completeness.
  The spec is readable and understandable as a canonical reference by practising CPU architects and compiler writers. It is executable and machine-manipulable by tools for establishing correctness and transformations in both compilers and CPU designs.

(……discuss….)

Pull/Issue Status

Issue#	Date	submitter	title	status	
#04	3-Jul-18	kasanovic	Section 2.3 Target Environment		
#22	24-Nov-18	brouhaha	I-MISALIGN_LDST-01 assumes misaligned data access will trap		
#40	4-Feb-19	debs-sifive	Usage of tohost/fromhost should be removed		
#45	12-Feb-19	debs-sifive	Reorganization of test suites for code maintainability	Fixed in RISCOF	
#63	13-Aug-19	jeremybennett	Global linker script is not appropriate		
#78	26-Jan-20	bobbl	RV_COMPLIANCE_HALT must contain SWSIG		
#90	11-Feb-20	towoe	Report target execution error		
#72	26-Oct-19	vogelpi	Allow for non-word aligned `mtvec`	deferred	needs v.2
#105	22-Apr-20	jeremybennett	Non-standard assembler usage	under discussion	Simple fix
#106	22-Apr-20	jeremybennett	Use of pseudo instructions in compliance tests	under discussion	
#107	22-Apr-20	jeremybennett	Clang/LLVM doesn't support all CSRs used in compliance test suite	under discussion	
#108	22-Apr-20	bluewww	RI5CY's `compliance_io.h` fails to compile with clang	under discussion	
#109	06-May-20	Olofk	Swerv fails because parallel make	under discussion	
pull#113	30-may-20	imphil	Consistently use UNIX line endings	under discussion	
#115	06-jun-20	adchd	How to support on-board execution?	under discussion	
#116	06-jun-20	simon5656	loss of 64bit test infrastucture	under discussion	
#119	17-jun-20	allenjbaum	Missing RV32i/RV64i test: Fence	Test needs to be written	
#125	15-jul-20	ShashankVM	Request to stop hosting closed source code on riscv repo	under discussion	