Architectural Test SIG Call –Minutes

Mon, 2024-04-08 8am Pacific → Daylight ← Time

See slide 7 for agenda

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Collaborative & Welcoming Community

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/community/community-code-of-conduct/

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RISC-V attendance

Only RISC-V Members May Attend

- Non-members are asked to please leave.
- Members share IP protection by virtue of their common membership agreement. Non-members being present jeopardizes that protection
- It is easy to become a member. Check out riscv.org/membership
- If you need work done between non-members or or other orgs and RISC-V, please use a joint working group (JWG).
  - used to allow non-members in SIGs but the SIGs purpose has changed.
- Please put your name and company (in parens after your name) as your zoom name. If you are an individual member just use the word “individual” instead of company name.
- Non-member guests may present to the group but should only stay for the presentation. Guests should leave for any follow on discussions.

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SIG Charter

The Architectural Compatibility Test SIG is an umbrella group that will provide guidance, strategy and oversight for the development of tests used to help find incompatibilities with the RISC-V Architecture as a step in the Architectural Compatibility self-certification process

The group will:

- Guide Development of:
  - Architectural tests for RISC-V implementations covering ratified and in-flight specifications for
    - Architectural versions, standard extensions, and implementation options.
  - Tools and infrastructure to help identify architectural incompatibilities in implementations
- Work with TSC and Chairs for resources to get the above work done.
- Mentor or arrange for mentoring for the resources to get the above work done

Adminstrative Pointers

- Chair – James Shi shiqinghao.sqh@alibaba-inc.com Co-chair – Neel Gala neel.gala@incoresemi.com
- SIG Email sig-arch-test@lists.riscv.org. Notetakers: please send emails to both emails above
- Meetings – Monday 8am Pacific time on odd numbered weeks
- ,minutes, reportsDocuments etc. in
  - https://github.com/riscv-admin/architecture-test/tree/master/minutes Minutes
  - https://wiki.riscv.org/display/TECH/Calendars%2C+Meetings%2C+and+Zoom calendar
  - https://drive.google.com/drive/folders/1C70-DJPSV2HxNPbHg6qL9wvVadlmAB2h ACT test: dev docs / coverage reports / released reports
  - https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUlEs

    lifecycle in ”policies/supporting docs” folder, gaps in “planning” folder, arch-test specific in “information->content->arch-test”)
- Git repositories ←docs riscv → tools

←docs	riscv	→ tools
https://github.com/ riscv-non-isa /riscv-arch-test/tree/master/doc	tests	https://github.com/riscv-non-isa/riscv-arch-test
https://github.com/riscv-software-src/riscof/tree/master/docs	riscof	https://github.com/riscv-software-src /riscof
https://github.com/riscv-software-src/riscv-ctg/tree/master/docs	Test Gen.	https://github.com/riscv-software-src /riscv-ctg
https://github.com/riscv-software-src/riscv-isac/tree/master/docs	YAML, WARL config	https://github.com/riscv-software-src /riscv-config/
https://github.com/riscv/sail-riscv/tree/master/doc	Sail formal model	https://github.com/riscv/sail-riscv/
https://github.com/riscv-admin/architecture-test	minutes, charter	
https://github.com/InspireSemi/riscof_install_example_DUT	sail install helper	

- JIRA: https://jira.riscv.org/projects/CSC/issues/CSC-1?filter=allopenissues
- Dev Partner work: https://github.com/orgs/riscv-admin/projects/2/views/4
- Sail annotated ISA spec: in https://github.com/rems-project/riscv-isa-manual/blob/sail/
  - README.SAIL ←how to annotate annotated unpriv spec→ release/riscv-spec-sail-draft.pdf
  - release/riscv-spec-sail-draft.pdf ← annotated source annotated priv spec→ release/riscv-privileged-sail-draft.pdf
  - https://us02web.zoom.us/rec/share/-XIYazzhIBbQoiZdarCfebdjxjDWiVhf-LxnuVrliN4Bc30yf17ztKkKDU4Og54b.fArPPqnuR-NiXpQU

    Tutorial Passcode: tHAR#5$V

Meeting Agenda

I. Updates, Status, Progress:
   I.

II. Next steps and Ongoing maintenance
   1. Review and compare RISC-V testing approaches to approaches with other architectures
   2. Review & prioritize issues

Discussion

2024-04-08ACT meeting notes

Request
Add pointer to minutes at the beginning of the meeting (pointer to minutes repo is on slide 6 of this deck, along with pointer to many other relevant docs and repos)

Comparison of RV test methodology vs. other Architectures
Discussion of how other ISAs do arch tests vs. RV ACTs, e.g.
- cycle by cycle state coverage vs. having test explicitly store state & comparing at the end
  -- signatures are a list of every arch state change at each point in a test should be equivalent to cycle to cycle comparison
  --mapping failures →test is not difficult because every mismatch is reported
- testing multiple different features in a test vs. just a single feature
- tests for specific combinations of coverage vs. generic (specific combinations enable self checking)
  Note that developing tests that allow for multiple specific combinations take more developer resource

Risc-v Spec gaps
- No complete list of architectural options exist
  (options can be named or not, can be controlled by CSRs or not)

ACT Gaps:
- we don't have subject matter experts for extensions, especially after ratification
  (TGs are responsible developing tests, but that was not the case for the base architecture, and earlier extensions, and the TGs that developed them no longer exist)
- we don't have maintainers for the important ACT apps:
  riscof (the framework that runs tests),
  riscv-config (configuration checker and test selector)
  ctg (compatibility test generator) ** not required: tests can be handwritten or generated by other apps
  ISAC (ISA Coverage tool)
- We don't have enough resources to
  --review / write PRs (needed to close issues),
  -- write tests or to develop cpverage models
  -- reviewing coverage (the most important step to accepting new tests into the repo)
  a tool is being developed to make coverpoints more concise, so easier to generate & review

Sail Gaps:
- configurability isn't quite there yet (but requires the list of arch options for completeness)

Coverage Definition: another way to check coverage is simulator code coverage.
This is starting to get added to Sail (in terms for branch coverage, which is roughly equivalent)
However, this is not really adequate for many corner cases which need cross branch coverage:
(i.e not that a branch went both ways, but that a series of them took all possible combinations.

----------PR Review----------
#330: ZFA support: ready to merge, but needs ctg#60 also to be useful (& maybe to pass C/I)
#407, SV39: has some conflicts, but needs coverpoint review
#427, B-extension update: might be an issue in RVTEST_CASE macro. If not, will merge it.
else, all tests will need to be modified
#439. – needs more work

Decisions & Action Items

Decisions ()

Outstanding Action Items

BACKUP