

# Compliance Task Group Call – Minutes

Thur, 10Sep2020 8am Pacific → Daylight ← Time

See slide 4 for agenda

# Charter

The Compliance Task Group will

- Develop? compliance tests for RISC-V implementations, taking into account approved specifications for:
  - Architectural versions (e.g. RV32I, RV32E, RV64I, RV128I)
  - Standard Extensions (H,S,U,A,B,C,D,F,H,J,M,N,P,T,V,N), Priv Mode
  - All spec'ed implementation options
    - (incl. MHSU modes, optional CSRs, optional CSR bits)
- Develop a method for selecting and configuring appropriate tests for a RISC-V implementation, taking into account:
  - Platform profile and Execution Environment (EE)
  - Implemented architecture, extensions, and options
- Develop a framework to apply the appropriate tests to an implementation and verify that it meets the standard
  - test result signature stored in memory will be compared to a golden model result signature

# Administrative Pointers

- Chair – Allen Baum                      [allen.baum@esperantotech.com](mailto:allen.baum@esperantotech.com)
- Co-chair – Bill McSpadden                      [bill.mcspadden@seagate.com](mailto:bill.mcspadden@seagate.com)
- TG Email                                      [tech-compliance@lists.riscv.org](mailto:tech-compliance@lists.riscv.org)
  - Notetakers: please send emails to [allen.baum@esperantotech.com](mailto:allen.baum@esperantotech.com)
- Meetings -Bi-monthly at 8am Pacific time on 2<sup>nd</sup>/4<sup>th</sup> Wednesdays
  - See “????” entry for zoom link
- Documents, calendar, roster, etc. in
  - <https://lists.riscv.org/tech-compliance/>      see /documents & /calendars subdirectories
  - <https://riscov.readthedocs.io/en/latest/>      riscov
  - <https://riscv-config.readthedocs.io/en/latest/>      config: YAML and WARL spec
  - <https://drive.google.com/drive/folders/1DemKMAD3D0Ka1MeESRoVCJipSrwiUIEs>  
(lifecycle in “policies/supporting docs” folder, gaps in “planning” folder,  
compliance specific in “compliance folder”)
- Git repositories
  - <https://github.com/riscv/riscv-compliance/>
  - <https://gitlab.com/incoresemi/riscov> (riscov framework)
  - <https://github.com/riscv/riscv-config/>

# Meeting Agenda

1. Updates, Status, Progress
  1. Passdowns (verbal)
    1. Need to develop ways to pass off work to outside help and to do regression testing
  2. Adding Asia meeting times – **poll sent out, not enough response**
  3. Jira issues filed (CSC1..CSC-6) and IT-1,4) (add Jira issue page to minutes/agenda)
    1. These re-label tests, describe intent of the TG, the goals/strategy/tactics, and need to develop and prototype RTL test fixture
  4. RFQ: awarded and contract signed!
2. Discussion:
  1. Compliance FAQ - any more comments? Settle on prose that defines what compliance means, Change name (CSC-1,2, see page 8)
  2. Specific Compliance Policy/Process Gaps:
    1. Criteria for approving merge requests (e.g. coverage, Sail model integration, size, time to run)(see slide 9)
    2. Certifying passing architecture tests: what needs to be in the report? Where does report get sent? (e.g. vendorID/archID)
    3. Can we certify actual HW if only its core RTL has passed architecture tests?
    4. How do we enable configurable & licensed core IP
  3. Coverage: Actual rules are now available here: <https://github.com/incoresemi/riscv-compliance/blob/dev/coverage/coverpoint.yaml>
  4. Next steps and Ongoing maintenance
    1. Migration to Framework v.2. video: <https://youtu.be/VIW1or1Oubo>, slides: <https://lists.riscv.org/g/tech-compliance/files/Presentations/TestFormatSpec.pdf>
      1. Review Pipecleaner tests:What do we need to do to exercise capabilities for Priv Mode tests
      2. What steps do we need to complete to cut over to V.2 (see slide 10)
      3. (e.g. Sail model updates, pipecleaning, N people have run it, testing all the “fixed in riscov” issues
    2. Develop SAIL maintenance plan
    3. Identify Tool providers, e.g. coverage model, test generation for new features/extensions
    4. Flesh out test development order & identify resources (e.g. Priv,FDD or F,Priv,D..., JIRA CSC-3,5
    5. Provide a reference RTL test fixture (as opposed to SW functional model). See JIRA CSC-6

# Discussion

## 1.1 Verbal passdown: [Chair]

- 1.1.1 we need to develop plans to enable outside teams to write tests, do regression testing, maintain tools
- 1.2 No replies to the Asian meeting time poll, so not doing it
- 1.3 JIRA issues filed (summarized)
- 1.4 **RFQ awarded to InCore**

New set of tests are on the github dev branch as of Global Forum

[SH] How is progress tracked?

[Incore] I can go through status in next meeting. There is a coverage folder for the testsuite we've created.

[Imp] We want a 1 page summary of progress (a dashboard)

[Incore2] [https://github.com/incoresemi/riscv-compliance/blob/dev/coverage/rv32i\\_m/l/coverage.html](https://github.com/incoresemi/riscv-compliance/blob/dev/coverage/rv32i_m/l/coverage.html)  
<https://github.com/incoresemi/riscv-compliance/tree/dev/coverage>

[Chair] JIRA issues: overview

## 2.1 Compliance FAQ (Jira CSC-1,2)

[Chair] in consultation with QC for "Architectural Test" rationale and definition (see slide 8)

e.g. global search&replace "Compliance Test"->"Architecture Test" in charter, test format spec, repo doc folder

2.4.4 (JIRA CSC-3,4,5) These items are goals, strategy and tactics for this TG, to be placed in repo doc folder

2.4.5 (JIRA CSC-6). Need a test harness for the tests.

[Incore] Can we just give examples of test harnesses?

[Imp] Need to define the parameters for the framework such that existing SW (i.e. architecture tests) just runs.

Link: <https://jira.riscv.org/browse/CSC-6>

[AR] How can tech-compliance get access to JIRA? [Chair, Co-chair]

[Chair] <https://jira.riscv.org/projects/CSC/issues/>

## 2.2 Test acceptance criteria (see slide 9)

[Imp, Chair] Discussion of Vector Testing and how to count "executed instructions"

For limited mem: define a target, break up tests if required, but we need to define a target size

We need to collect data first, to see what is reasonable (both test sizes, & implementation memory sizes)

Number of instructions executed/run, nor #sec are useful - time is too variable

Memory footprint matters, not time. E.g. vector tests can take 8 hours/config

[AR] (Incore) is going to gather data on Base ISA tests memory footprint.

[Imp] This meeting conflicts with Platform meeting. (That's why CTO and QC are absent)

One of the meetings need to change times.

[Imp] Priv spec needs to be next priority

[Chair] agreed

[Imp] SAIL model: Prashanth fixed existing bug in SAIL model

Signature has to be validated against SAIL. Add to test acceptance criteria.

Incore will present Base ISA test progress in off cycle meeting in one week

# Decisions & Action Items

## Decisions

Use JIRA for adding Action items

IT-4 add Jira line to lists.riscv.org home screen

CSC-1 Renaming “compliance” to “architecture” will affect charter, readme, testformat spec, anything in github doc directory

CSC-2 draft written, will be placed in github doc directory

CSC-3..5: document will be written and placed in the github doc directory

## Outstanding Action Items- New

[Chair, Co-chair] document how to get JIRA access & Compliance project subscription

[Incore] gather data on Base ISA tests memory footprint

[Chair] update issues spreadsheet, add JIRA issues to it

### Old

Imperas: make pull request for updated assertion macro

Stuart: write up coverage taxonomy

Everybody: read policy docs, send gaps in compliance (e.g. formal model support, possible mismatch between config TG and riscv-config) and priority to [cto@riscv.org](mailto:cto@riscv.org)

# Previous Action Items / Progress Update

- Chair Base ISA coverage draft spec is uploaded - done – yaml now available
- SH will add file regarding coverage - no progress....in progress
- Imperas / Incore: ensure headers, macros, dir structure match newest spec, assertions are not inline – waiting for assertion macro update, Imperas pull request
- Chair coordinate with Riscov to determine pipecleaning exercise - to be reviewed in TG
- Chair to communicate with TSC about reorganization comments - waiting TSC feedback
- Chair,CoChairto talk w/ SAIL team about transitioning support – have identified needed support and effort
- Configuration Structure TG vs. Riscv-Config: - discussions underway – see <https://github.com/riscv/configuration-structure/> and new profile group

Note: initials are company abbreviations

# Architectural Test Rationale – Intent and Limits

RISC-V Architectural Tests are an evolving set of tests that are created to help ensure that SW written for a given RISC-V Profile will run on all implementations that comply with that profile.

These tests also help ensure that the implementer has both understood and implemented the specification.

The RISC-V Architectural Tests test suite is a minimal filter. Passing the tests and having the results approved by RISC-V International is a prerequisite to licensing the RISC-V trademarks in connection with the design.

Passing the RISC-V Architectural Tests does **not** mean that the design complies with the RISC-V Architecture. These are only a basic set of tests.

The RISC-V Architectural Tests are **not** a substitute for rigorous design verification; it is the responsibility of the implementer to deploy extensive testing.

To be added to the riscv/riscv-compliance/doc/ directory as “RISC-V Architectural Test Rationale”



# Test Acceptance Criteria – first cut

Tests must:

- conform to current standard of test spec (macros, labels)
- run in framework
- run with with assertions on and not fail any tests
- generate a valid signature (that can be saved and compared with other dut/sim)
- has a clear configuration - i.e. which ISA extension it can be used with
- have a code, data, and signature memory footprint that is small enough\*
- improve coverage
- use only standard instructions
- use only files that are part of the defined support files in the repository
- must be commented, both in header and inside test cases

*\* need to define “small”, “X” ← will vary by extension, base ISA expected to be <8K*

# Framework Requirements – first cut

The framework must:

- Use the TestFormat spec and macros described therein
  - (which must work - including assertions)
- Choose test cases according to equations that reference the YAML configuration
- Define macro variables that can be used inside tests based on the YAML configuration
- Include the compliance trap handler, & handle its (separate) signature area
- Load, initialize, and run selected tests between two selected models, extract the signatures, compare results, and write out a report file
- Exist in a riscv github repo, with a few than one maintainer.
- Be easy to get running, e.g.:
  - run under a variety of OSES with the minimum number of distro specific tools.
  - Not require sudo privileges
- Maybe: have the ability to measure and report coverage
  - Coverage specification is a separate file
  - Could be a separate app

# Pull/Issue Status

| Issue#   | Date      | submitter       | title   | status                | comments                  |
|----------|-----------|-----------------|---|-----------------------|---------------------------|
| #04      | 3-Jul-18  | kasanovic       | Section 2.3 Target Environment                                    | Fixed in RISCOF       |                           |
| #22      | 24-Nov-18 | brouhaha        | I-MISALIGN_LDST-01 assumes misaligned data access will trap       |                       |                           |
| #40      | 4-Feb-19  | debs-sifive     | Usage of tohost/fromhost should be removed                        |                       |                           |
| #45      | 12-Feb-19 | debs-sifive     | Reorganization of test suites for code maintainability            |                       |                           |
| #63      | 13-Aug-19 | jeremybennett   | Global linker script is not appropriate                           |                       |                           |
| #78      | 26-Jan-20 | bobbl           | RV_COMPLIANCE_HALT must contain SWSIG                             |                       |                           |
| #90      | 11-Feb-20 | towoe           | Report target execution error                                     |                       |                           |
| #72      | 26-Oct-19 | vogelpi         | Allow for non-word aligned `mtvec`                                | deferred              | needs v.2                 |
| #105     | 22-Apr-20 | jeremybennett   | Non-standard assembler usage                                      | under discussion      | Simple fix                |
| #106     | 22-Apr-20 | jeremybennett   | Use of pseudo instructions in compliance tests                    | under discussion      |                           |
| #107     | 22-Apr-20 | jeremybennett   | Clang/LLVM doesn't support all CSRs used in compliance test suite | under discussion      |                           |
| #108     | 22-Apr-20 | bluewww         | RI5CY's `compliance_io.h` fails to compile with clang             | under discussion      |                           |
| #109     | 06-May-20 | Olofk           | Swerv fails because parallel make                                 | under discussion      |                           |
| pull#113 | 30-may-20 | imphil          | Consistently use UNIX line endings                                | under discussion      |                           |
| #115     | 06-jun-20 | adchd           | How to support on-board execution?                                | under discussion      |                           |
| #116     | 06-jun-20 | simon5656       | loss of 64bit test infrastucture                                  | under discussion      |                           |
| #119     | 17-jun-20 | allenjbaum      | Missing RV32i/RV64i test: Fence                                   | Test has been written | Close when test is merged |
| #125     | 15-jul-20 | ShashankVM      | Request to stop hosting closed source code on riscv repo          | under discussion      |                           |
| #132     | 15-aug-20 | davidmlw        | Why not just use mepc for mret?                                   | answered              | Should be resolved        |
| #133     | 19-aug-20 | Imperas         | Usage of pseudo instruction unimp                                 | answered              | Simple fix                |
| #135     | 04-sep-20 | MikeOpenHWGroup | Request for a Tag on this Repo                                    | assigned              |                           |

# JIRA Status

| Issue#       | Date      | submitter   | title   | status | comments                  |
|--------------|-----------|-------------|---|--------|---------------------------|
| <b>IT-1</b>  | 27Aug/20  | Allen Baum  | Need to modify the description of compliance in <a href="https://riscv.org/technical/specifications/">https://riscv.org/technical/specifications/</a> | done   |                           |
| <b>IT-4</b>  | 01/Sep/20 | Allen Baum  | Add Jira link to TG home pages  |        |                           |
| <b>CSC-1</b> | 20/Aug/20 | Ken Dockser | Come up with names for the tests suites that we are creating  |        | 1 <sup>st</sup> step done |
| <b>CSC-2</b> | 20/Aug/20 | Ken Dockser | Produce concise text to explain the Architecture Tests intent and Limits  |        | Written, needs pull req   |
| <b>CSC-3</b> | 20/Aug/20 | Ken Dockser | Come up with an internal goal for what we wish to accomplish with the Architectural Tests   |        | Not written               |
| <b>CSC-4</b> | 20/Aug/20 | Ken Dockser | Develop a roadmap for all the different categories of test suites that will need to be created  |        | Not written               |
| <b>CSC-5</b> | 20/Aug/20 | Ken Dockser | Develop a roadmap for releases of single-instruction Architecture Tests   |        | Not written               |
| <b>CSC-6</b> | 20/Aug/20 | Ken Dockser | Develop a reference RTL test fixture that can stimulate and check the CPU under test  |        | Needs more discussion     |