Issue test discussion

Status Update:

Minutes

Progress: mostly issues filed.

Questions about why bugs are in Sail not caught at some point

Problem: no revision number in Sail (or Spike) so CI is difficult

Branding – customers don’t know how, some customers don’t feel they need to.

Sail:

– Vector is taking precedence for support in SAIL, Epmp is next. Etrace support incoming in SAIL

- Needs to have configuration from YAML solid and useful

- RSaaS is down the road.

How are vector test generated? Where does the test generation tool live?

Chair –In general, tools should live under riscv-software-src on github.

(riscv-software/riscv-ctg is one example,

vector spec has it’s own generator, but needs to be compatible with test-format spec

Do tests get generated dynamically or are they stored

Chair: tests are selected, can be configured/parameterized,

(based on YAML configuration files) and are compiled dynamically, but are not generated dynamically

Seagate - xperm bug in SAIL was not caught even though the tests are present in the riscv-arch-test

Incore - the tests were checked in by IITM and at that time, SAIL support was not complete for these instructions.

Hence testing was done using SPIKE.

Seagate – Having a regression to have versions of tools which pass the arch-test suite release would be helpful

Chair – In general, tests are not added until they pass some C/I, but not the other way around

Incore – Needs a versioning system for all the tools. Neither spike nor Sail have such

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Chair <presentation of plans going forward>: (not in any particular order)

1. Update trap handler to deal with mode transitions (primarily one VM mode to another)

2. Split and update Test\_Format\_Spec into

a. TestDev\_Guideline\_Spec – primarily the structure of tests and required/optional RVTEST\_ macros\_

b. ACT\_interface\_Spec – primarily all the RVMODEL\_ macros

3. Close outstanding issues

4. Closing outstanding pull requests

Primarily reviewing extension additions: PMP, ePMP, CBO.zero

5. Reference Signature as a Service (Golden Model WG)

6. support for handling constrained non deterministic results (e.g. misaligned load/store/branch)

7. Trick boxes of timing/concurrency support

a. Interrupt event generator ( interrupt testing)

b. Memory event generator (LR/SC, Atomic ops, WRS, mem model (TSO, WMO)

c. Debug/Trace command interface (Etrace, Ntrace) 

8. Minimal support for TLBs and cache op testing

likely requires simple cache/TLB models

whose behavior can be controlled enough to test).

9. DUT debug support: out-of-line assertion macro

(currently very model specific, and costly because all inlined code

define an API subroutine call with a standard narrow interface).

10. OS support? (besides Debian, Ubuntu): e.g. Centos, RockyLinux, Windows, Mac, etc.

11.Others?: more concise coverage definitions (>=10x fewer lines)

Issue Discussion

Chair - Issue #305: Utilize more registers in test for increased functional coverage

Chair: this is a DV vs. compatibility test issue; nice to have, not critical for our purposes.

Incore – Can be handled by splitting coverpoints accordingly.

Can be implemented trivially in ctg.

Should we update tests? This is a low priority issue.

Seagate – Would be better to update the tests.

Incore – Would require compute resources and manpower to do it.

We should update ctg to enable that, but it is low priority for now.

Excellent opportunity for an intern to get their hands dirty.

RISCV – Raise this in dev-partners

RISCV – How are E extensions tests handled?

Chair – handled by not having the upper registers be tested in the test.

Are E extension and the Vector extension test compatible with each other?

Chair: That is more than 1 question:

Can an RV32/64E be compatible with V-extension? In theory, yes.

I’m not sure that RVV has been defined to make use of

the upper 16 GPRS reserved (AR: chair)

Are there RV32/64E Vector tests?

I don’t think RIOS has done that, but it shouldn’t be hard..

Are Vector tests compatible with RISCOF?

RIOS has been made aware that their tests must conform to the test format spec

and to riscv-config YAML (so it runs under RISCOF)

and coverage is defined using CTG YAML

(so we can measure coverage for test acceptance using ISAC)

RISCV – Need to propose it to RIOS and raise it in the dev-partners meeting.

RISCV – Should get RIOS to present their work on the test generator and coverage in the arch-test meeting. (AR:Chair)

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