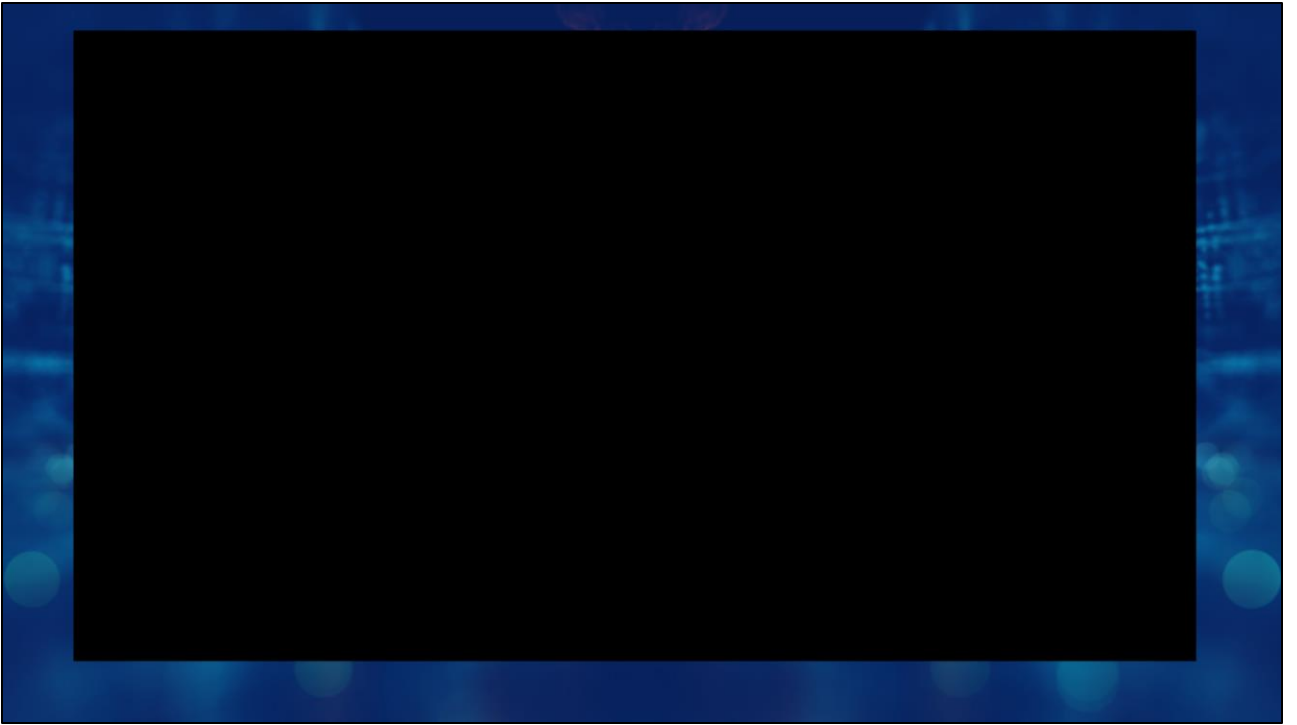




DTPM SIG E-Trace-Encap TG

11-Oct-2023

























Meeting minutes are in the speaker notes for the relevant slide



Agenda

- Disclosures
- E-Trace packet encapsulation
- Maintenance
- Competitive Analysis
 - Charter review for Secure Debug – Joe Xie
- AOB



PD	Paul Donahue (Ventana) (Me)	 
IR	Iain Robertson (Siemens)	 
AJ	Aote Jin (NVIDIA)	 
BS	Beeman Strong (Rivos)	 
BA	Bruce Ableidinger (SiFive)	 
	Dean Liberty (SiFive)	 
GK	Gokhan Kaplayan (IMG)	 
GC	Greg (Ventana)	 
JG	Jay Gamoneda (NXP)	 
JX	Joe Xie (nVidia)	 
MS	Michael Schleinkofer(Lauterbach)	
RC	Robert Chyla (SiFive)	 

Attendees: see screenshot on the agenda slide

E-Trace Packet Encapsulation

- Acting chair: Iain Robertson, acting vice-chair: Paul Donahue
- Reflector: tech-e-trace-encap@lists.riscv.org
- githubs: <https://github.com/riscv-admin/e-trace-encap>, <https://github.com/riscv-non-isa/e-trace-encap>
- DTPM SIG and E-Trace-Encap meetings will co-exist
- Adoc spec: <https://github.com/riscv-non-isa/e-trace-encap/blob/main/e-trace-encap.pdf>
- TSC voting on approval for TG and chair/vice chair. Approval expected Oct 16th
- Spec complete and ready for ratification.
- Ratification plan started – stalled due to holidays and catch-up workload.

Maintenance (E-Trace)

- Clarification on push/pop support for data trace
 - Examples added to section 4.3 and pull request made
- Proposal to change description of tail call itypes to 'jumps'
 - Beeman generated pull request
- Typo spotted in data trace packets: *index_width_p* should be *lrid_width_p*
 - Iain generated pull request
- Update control section to reference common control document
 - Feedback incorporated and all issues resolved. A couple of clarifications for Common Control raised
- Just waiting on resolution of Common Control items before requesting SoC HC review.
- Will recommend all for 2.0.1.



- Make spelling of E-Trace consistent (done)
- Greg: [Regarding Common Control] If changes go in ASAP then things won't be delayed, otherwise there will be delays due to the requirement for another iteration of review for later changes. ARC is offloading some review bandwidth to HC chairs, allowing someone like Ved to assist ARC with the review process. Making appropriate changes now will also help remove some points that the review process would identify.

Competitive Analysis

- Template spreadsheet:
 - Located in *risc-v members/Workgroups/Debug Trace Performance Monitoring* RVI Google Drive
 - <https://docs.google.com/spreadsheets/d/1l0N-E-hTjFj3jkPrjsLitso4hACDajayNwh35F4KUfs/edit#gid=0>
- External Debug Security TG proposed.
 - Joe Xie acting chair; Gokhan Kaplayan acting vice chair
 - Draft charter:
https://docs.google.com/document/d/1XHvpYywkw_FgfAobRL5hPRjmRPkOw5SswMVqZjF7uZ6l/edit?usp=sharing
 - Threat model & competitor analysis:
https://docs.google.com/presentation/d/1qia1PLldz25BhV7XaNjjQPvQRefVBrt7wuqPZyFtpY/edit?usp=share_link
- Still need input from others with knowledge of other architectures



External Debug Security TG Charter:

- In what ways is it non-ISA? System Bus Access, trace, etc.
- Joe: Many things such as authentication details are implementation specific.
- Robert: The spec should mandate a way to authenticate and enable debug features from initial power-on. In the ARM world, everybody has different ways of controlling ARM's 4 input wires. Some of the mechanisms are crazy so it's better to standardize.
- Joe: The charter is simplified to allow the spec to be ratified in a short time. Not every possible debug issue is being addressed.

- Iain: Add a sentence at the end of the charter that says that such issues will be addressed in a later TG.
- Does the TG need to deliver Spike, ACT, Sail, etc.? Yes, but there can be waivers.
- Robert: How does this affect self-hosted debug? There's no problem because existing privilege modes handle that.
- Joe will update the charter to add trace and to add a sentence about next steps beyond this TG.
- Robert: Put the link to the charter on the SIG page, not just buried in meeting minutes that nobody looks at.
- Bruce: WorldGuard also can restrict access to performance counters.
- Discussion about whether anything special needs to be done. Since the proposal is that the debugger cannot access anything that's not accessible in mode X, it all naturally falls out that whatever WorldGuard protects will not be accessible.
-

Future Meetings / AOB

- 2nd Wednesday of each month
- AOB



Thank You

