
RISC-V®
DTPM SIG
03/08/2023

Agenda

- Disclosures
- Charter approved by SoC HC
- Call for Chair/Vice chair closes March 10th
- eTrace packet encapsulation
- Gap Analysis Summary
- Maintenance
- AOB

Disclosures

Video link

Only RISC-V Members May Attend

- Non-members are asked to please leave except for Joint Working Groups (JWG).
- Members share IP protection by virtue of their common membership agreement. Non-members being present jeopardizes that protection. Joint working groups (JWG) agree that any IP discussed or worked on is fully open source and unencumbered as per the policy.
- It is easy to become a member. Check out riscv.org/membership
- If you need work done between non-members or or other orgs and RISC-V, please use a joint working group (JWG).
    - used to allow non-members in SIGs but the SIGs purpose has changed.
- Please put your name and company (in parens after your name) as your zoom name. If you are an individual member just use the word “individual” instead of company name.
- Non-member guests may present to the group but should only stay for the presentation. Guests should leave for any follow on discussions.

Antitrust Policy Notice

RISC-V International meetings involve participation by industry competitors, and it is the intention of RISC-V International to conduct all its activities in accordance with applicable antitrust and competition laws. It is therefore extremely important that attendees adhere to meeting agendas, and be aware of, and not participate in, any activities that are prohibited under applicable US state, federal or foreign antitrust and competition laws.

Examples of types of actions that are prohibited at RISC-V International meetings and in connection with RISC-V International activities are described in the RISC-V International Regulations Article 7 available here: https://riscv.org/regulations/

If you have questions about these matters, please contact your company counsel.

RISC-V®

Collaborative & Welcoming Community

RISC-V is an open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/community/community-code-of-conduct/

Conventions

- **For one hour meetings, please start at 5 after the start time** in order to allow people going to other meetings have time for a short break between meetings. 30 minute meetings start on time.
- Unless it is a scheduled agenda topic, we don’t solve problems or detailed topics in most meetings unless specified in the agenda because we don’t often have enough time to do so and it is more efficient to do so offline and/or in email. We identify items and send folks off to do the work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unilaterally. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, …
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

eTrace Packet Encapsulation

- Proposal sent by email
  - one question from Allen regarding SrcID size (Robert responded)
- Any other feedback?

Gap Analysis Summary - Debug

Item	Priority	Current Status	Next Steps
Allow debugger to flush caches when no program buffer		On hold pending ratification of Debug spec	
Option to not reset debug CSRs		On hold pending ratification of Debug spec	
Debug Authorisation framework		Some discussions underway… Various debug levels End-User, Expert or OEM, etc How do we authorize different levels? Root of trust being established to debug and identify if debug is enabled on a platform What can be part of debug vs what cannot be part of debug? Virtualization for trace to memory	
Self hosted debug, and delegation to lower modes			
Alternatives to GDB with multi-core support		Suggestion from Bruce. Unclear how this is actionable	

Gap Analysis Summary - Trace

Item	Priority	Current Status	Next Steps
eTrace packet encapsulation for transport	High	In discussion – hopefully fast track	Will be presenting proposal in SoC HC [March 2023]
eTrace vector extension support		No changes needed for instruction trace. Data trace will need extending	
Cycle Accurate			
Trace-to-Memory			

Gap Analysis Summary – Other

Item	Priority	Current Status	Next Steps
Competitive analysis of debug/trace features from different architectures	High	Identified high but need resource to help with competitive analysis	
Remote Telemetry			
Non-CPU performance monitoring			

Maintenance (E-Trace)

- Clarification on push/pop support for data trace
  - Examples added to section 4.3 and pull request made
  - No functional change
  - Need to determine approval process for updating the spec given that it is ratified.
- Proposal to change description of tail call itypes to ‘jumps’ as
  - Beeman to generate pull request
- Update control section to reference common control document
  - Not started yet

Future Meetings / AOB

- 2nd Wednesday of each month
- AOB


Thank You
RISC-V®