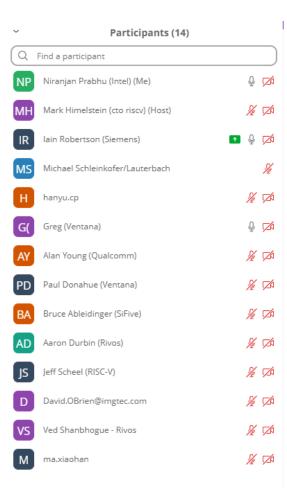


Agenda

- Disclosure
- Charter recap
- TG Status
 - Debug, Nexus
- Maintenance
 - eTrace clarification on push/pop and data trace
- Gap Analysis
- Discussion
- Future meetings
- AOB







Only RISC-V Members May Attend

- Non-members are asked to please leave except for Joint Working Groups (JWG).
- Members share IP protection by virtue of their common membership agreement. Nonmembers being present jeopardizes that protection. <u>Joint working groups</u> (JWG) agree that any IP discussed or worked on is fully open source and unencumbered as per the policy.
- It is easy to become a member. Check out riscv.org/membership
- If you need work done between non-members or or other orgs and RISC-V, please use a joint working group (JWG).
 - used to allow non-members in SIGs but the SIGs purpose has changed.
- Please put your name and company (in parens after your name) as your zoom name. If you are an individual member just use the word "individual" instead of company name.
- Non-member guests may present to the group but should only stay for the presentation. Guests should leave for any follow on discussions.



Antitrust Policy Notice

RISC-V International meetings involve participation by industry competitors, and it is the intention of RISC-V International to conduct all its activities in accordance with applicable antitrust and competition laws. It is therefore extremely important that attendees adhere to meeting agendas, and be aware of, and not participate in, any activities that are prohibited under applicable US state, federal or foreign antitrust and competition laws.

Examples of types of actions that are prohibited at RISC-V International meetings and in connection with RISC-V International activities are described in the RISC-V International Regulations Article 7 available here: https://riscv.org/regulations/

If you have questions about these matters, please contact your company counsel.



Collaborative & Welcoming Community

RISC-V is an open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/community/community-code-of-conduct/



Conventions



- For one hour meetings, please start at 5 after the start time in order to allow people going to other meetings have time for a short break between meetings. 30 minute meetings start on time.
- Unless it is a scheduled agenda topic, we don't solve problems or detailed topics in most
 meetings unless specified in the agenda because we don't often have enough time to do so and
 it is more efficient to do so offline and/or in email. We identify items and send folks off to do the
 work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unilaterally. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, ...
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

Charter

Full verbiage is <u>here</u>. Key points:

The goal for the DTPM SIG shall be to define a strategy to establish specifications and guidelines for the interfaces, transports, and other pieces of the SoC infrastructure

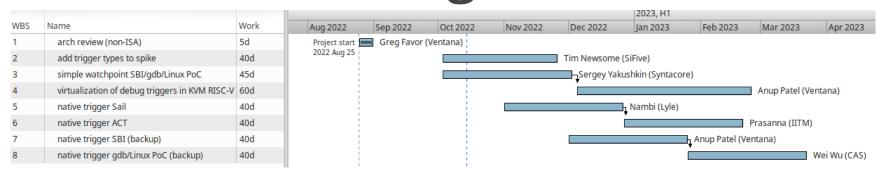
The DTPM SIG shall focus on the following areas:

- Standard programming interface
- Standard transports
- Unified security architecture
- Cables and connectors
- Debug, Trace, and SoC performance monitoring features

The DTPM SIG shall work on a gap analysis by starting with a lay of the land review on RVI debug, trace, SoC performance-monitoring capabilities



TG Status - Debug



- Should be ready to ratify v1.0 March 2023
- Several minor follow-on items deferred to v1.1:
 - #562, let the debugger flush caches when there is no program buffer
 - #390, optionally don't reset debug CSRs during reset



TG Status - Nexus

- Connectors
 - Most extensions agreed with MIPI
- Common control
 - Reworking to provide dedicates 4k blocks per component
 - Discussion ongoing regarding access from non-system bus
- Nexus Messages
 - Some clarifications
- Reference encoder/decoder
 - Changed to match messages
- Need clarity on what remains to be done



Maintenance

- eTrace: Seagate requested some further clarification on push/pop support for data trace
 - Examples added to section 4.3 and pull request made
 - No functional change
 - Need to determine approval process for updating the spec given that it is ratified.



Gap Analysis

- Trace
 - Common Control
 - Ongoing, under Nexus TG (for historic reasons). Progress very slow
 - Connectors
 - Ongoing, under Nexus
 - eTrace packet encapsulation for transport
 - High priority, should be a small task spin up a TG?
 - eTrace cycle accurate and vector extension support
 - Lower priority?
- Performance counting
 - Define standardised architecture, metrics and access for performance counting.
 - Useful starting point <u>here</u> and <u>here</u>.
 - Any interest in starting a TG?
- Debug Authorisation framework
- Remote Telemetry
- Alternatives to GDB with multi-core support



Future Meetings / AOB

- Meeting frequency?
- In-person meeting at RISC-V summit?
 - No slots remaining on member day but a slot during the conference days is possible
- AOB



