



DTPM SIG


23-July-2024

**Meeting minutes are in the speaker notes for the relevant slide**



# Agenda

- Disclosures
- Self-Hosted Trace TG draft charter opens discussion
  - Slides from Beeman:  
<https://docs.google.com/presentation/d/1CSSP1VjB3LEDtc3ZUnyPPD8lUgwi490lIKnTR6ml78/edit?usp=sharing>
- AOB

|   |                                 |
|---|---------------------------------|
| PD  | Paul Donahue (Ventana) (Me)     |
| IR  | Iain Robertson (Siemens)        |
| BS  | Beeman Strong (Rivos)           |
| RC  | Robert Chyla (MIPS)             |
| BG  | Bo Gan (Individual)             |
| BA  | Bruce Ableidinger (SiFive)      |
| MS  | Michael Schleinkofer/Lauterbach |
| V-  | Ved -Rivos                      |
|  | Victor Lu (Individual)          |



## Self-hosted trace

- Beeman presented his slides
- Single-context tracing: an entire user process. Used in conjunction with mode filtering.
- Open issue: SBI interface or CSR interface
  - Assuming there aren't multiple processes actually doing trace at the same time, is lazy context switch a possible way to reduce the SBI overhead? Yes, though you probably need to do the save but not the restore.
  - Need a way for external debugger to reserve trace for itself so that software is told that there is no trace.
  - SOC HC says that they want the SBI vs. CSR strategic decision to be part of the charter rather than allowing the TG to decide
  - Hypervisor vendors don't want to trap in context switches. They currently have to do this for debug triggers but that may be need to be fixed (via a separate effort than the self hosted trace TG).
  - General consensus seems to be CSR interface
- Open issue: Single-context self-hosted buffer PA (or GPA) vs. VA
  - Use case is for hyperscalers that can't plug in external debug to every server: e.g. <https://engineering.fb.com/2021/04/27/developer-tools/reverse-debugging/> [https://ltdb.lvm.org/use/intel\\_pt.html](https://ltdb.lvm.org/use/intel_pt.html)
  - Turning on trace may disturb behavior. Heisenbugs. This is related to DRAM sink, not necessarily to self-hosted debug specifically.

- OS should pin pages to avoid page faults.
- Treat it like DMA. However, CPU page table walk engines are already like scatter-gather engines.
- As buffer is getting close to full, we may want an interrupt. That's a TG detail.
- Consensus is to do virtual addressing
- Beeman will update the proposed charter with these decisions and send it out

# Future Meetings / AOB

- From May, meetings will be 60mins at 10am Pacific every 4<sup>th</sup> Tuesday, starting Jan 9<sup>th</sup>
  - Next meeting is 20-Aug at 10am Pacific(17:00 UTC)
- AOB



Thank You

