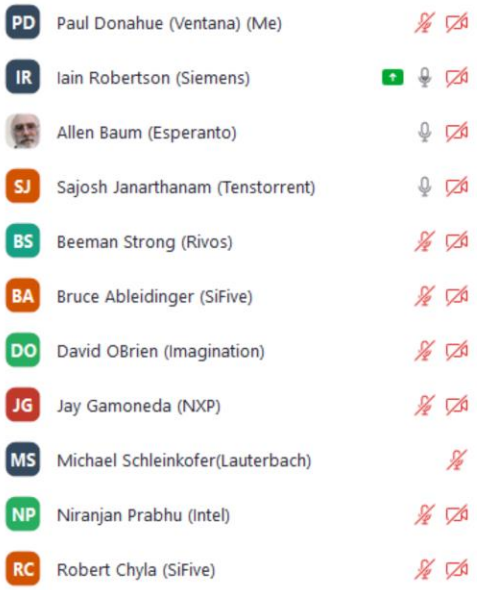
Meeting minutes are in the speaker notes for the relevant slide

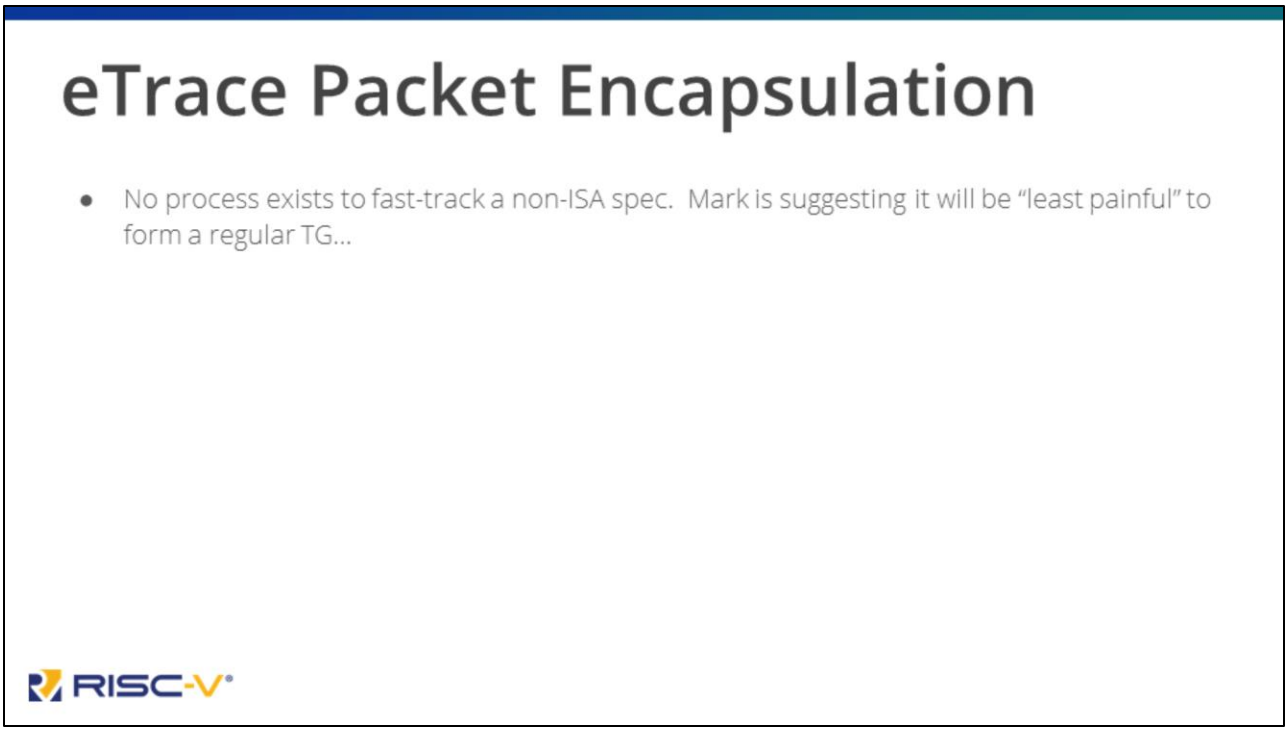
Agenda

- Disclosures
- eTrace packet encapsulation
- Competitive Analysis
- Gap Analysis Summary (no change)
- Maintenance (no change)
- AOB

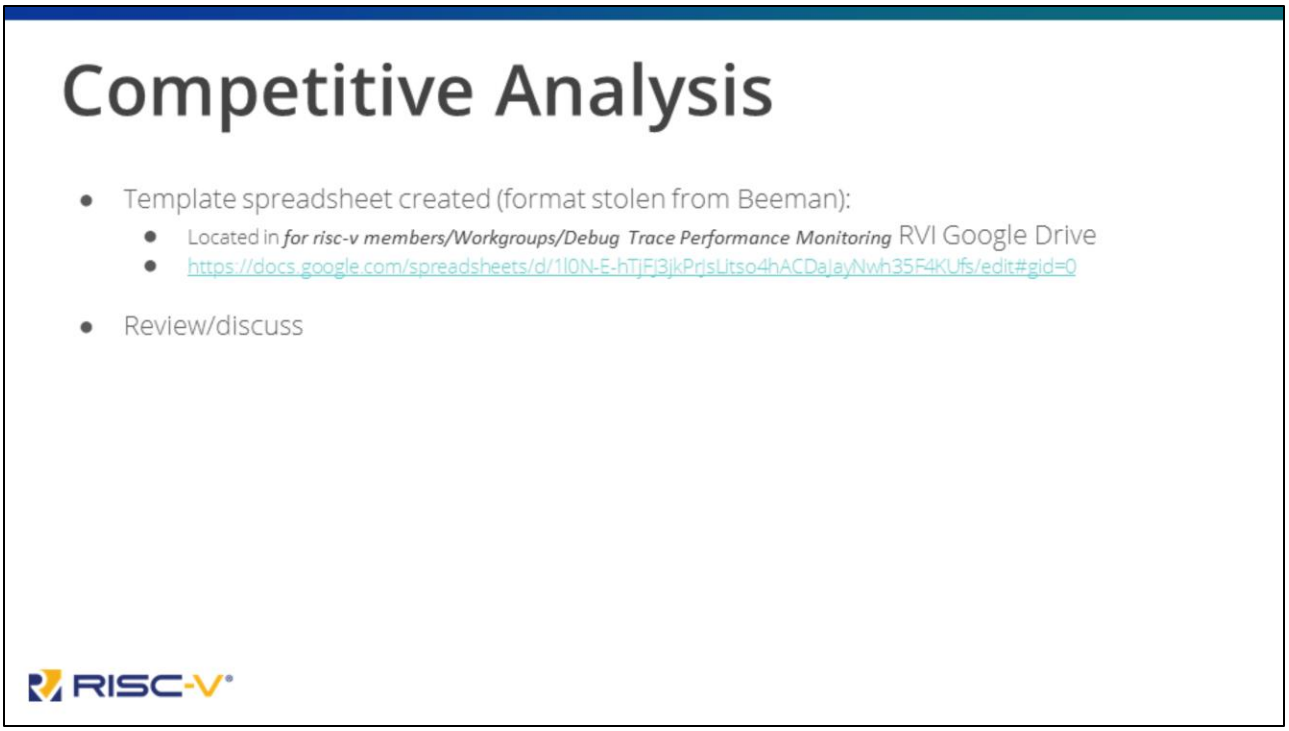


RISC-V

Attendees: see screenshot on the agenda slide



- eTrace Packet Encapsulation:
  - Uncontroversial but no fast-track process exists for non-ISA. Mark suggests forming a TG which could simply put together a ratification plan.
  - Questions remain about where it should ultimately end up. Don't want to convert to adoc if we are going to integrate in the existing eTrace spec.



- Competitive analysis:
  - Spreadsheet has been created
  - Looking for volunteers who have expertise in various areas
  - Q: Is the debug tab for debug of HW or SW? A: Both.
  - Robert: Suggest putting a No in the RISC-V column. We're not interested in things that everyone (including RISC-V) does since that doesn't help us improve.
  - Allen: Add compression ratio for traces of various architectures? That would be helpful.

Gap Analysis Summary - Debug

Item	Priority	Current Status	Next Steps
Allow debugger to flush caches when no program buffer		On hold pending ratification of Debug spec	
Option to not reset debug CSRs		On hold pending ratification of Debug spec	
Debug Authorisation framework		Some discussions underway… Various debug levels End-User, Expert or OEM, etc How do we authorize different levels? Root of trust being established to debug and identify if debug is enabled on a platform What can be part of debug vs what cannot be part of debug? Virtualization for trace to memory	
Self hosted debug, and delegation to lower modes			
Alternatives to GDB with multi-core support		Suggestion from Bruce. Unclear how this is actionable	

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Gap Analysis Summary - Trace

Item	Priority	Current Status	Next Steps
eTrace packet encapsulation for transport	High	In discussion – hopefully fast track	Will be presenting proposal in SoC HC [March 2023]
eTrace vector extension support		No changes needed for instruction trace. Data trace will need extending	
Cycle Accurate			
Trace-to-Memory			

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Gap Analysis Summary – Other

Item	Priority	Current Status	Next Steps
Competitive analysis of debug/trace features from different architectures	High	Identified high but need resource to help with competitive analysis	
Remote Telemetry			
Non-CPU performance monitoring			

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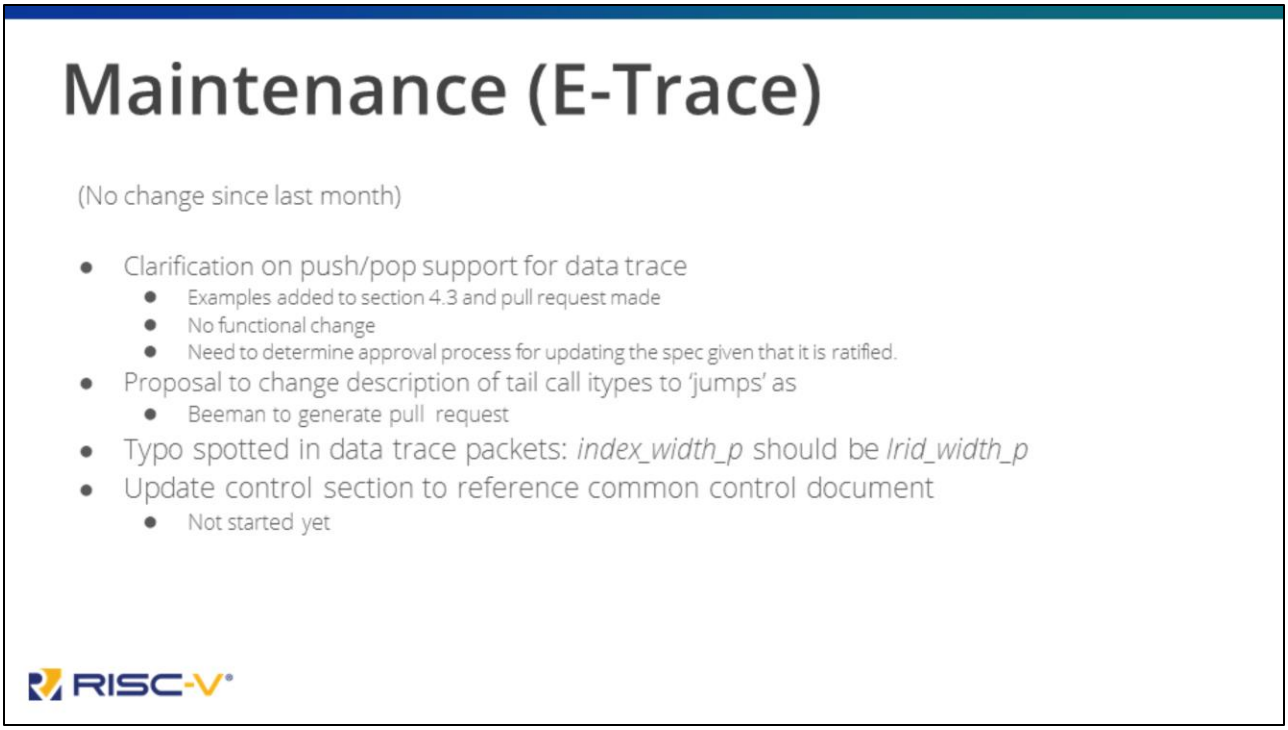
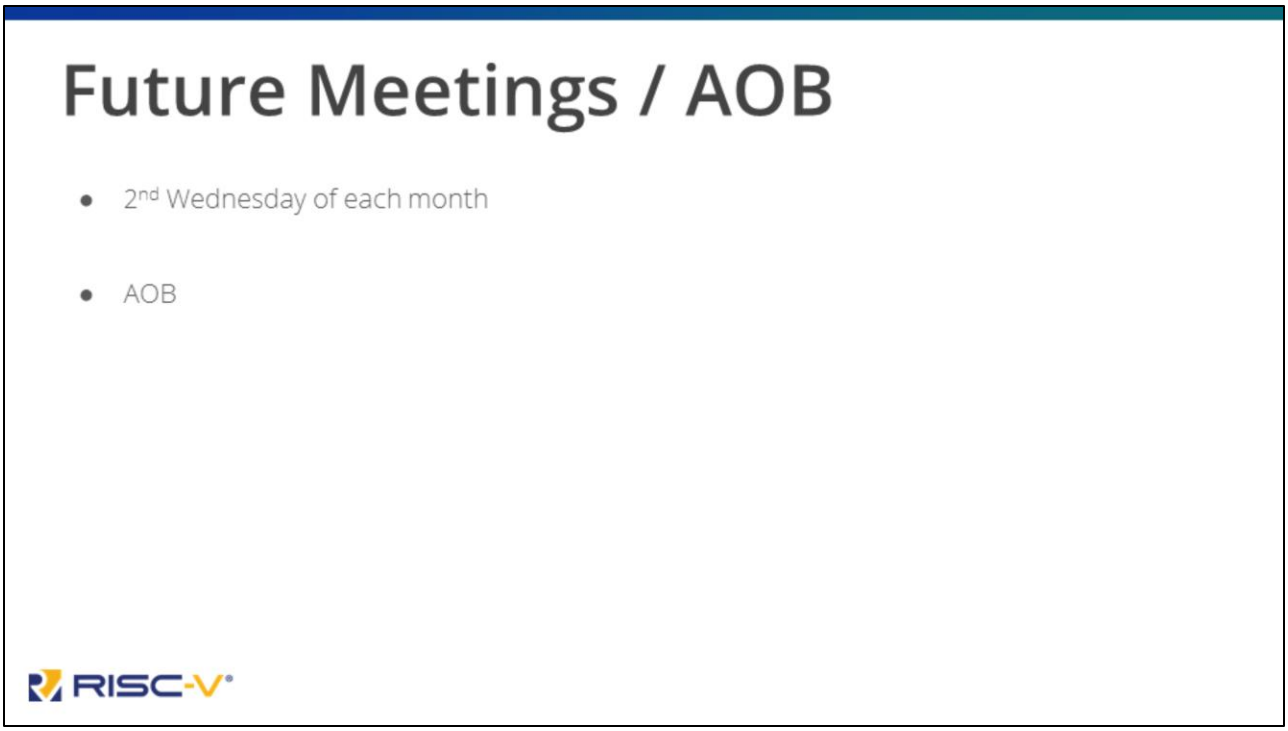


- Maintenance (eTrace):
  - Process for doing updates is unclear. Need clarity from Ved and Mark.
  - The eTrace spec appears to be the only approved non-ISA spec
    - Allen: arch-tests is arguably another



- Timestamps:
  - Michael: Control of timestamps within encapsulation. Do these timestamps replace the timestamp in format 3 packets?
  - Iain: During the original E-Trace work, someone asked for the timestamp to be included. It's optional. So if you use timestamp in the encapsulation then you probably don't want to include it in format 3 packets. The encoder can then control which packets have timestamps rather than only allowing them in format 3 packets.
  - Some packets always come close together in time so you don't need time on each of them.
  - Beeman was envisioning that format 3 could include full timestamp and encapsulation has deltas.
  - Timestamps are "a Pandora's box with a can of worms inside."


Thank You
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