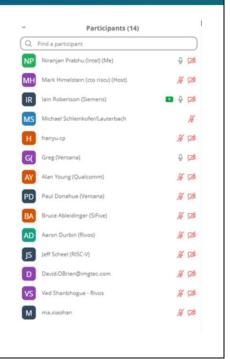


Meeting minutes are in the speaker notes for the relevant slide

# Agenda

- Disclosure
- Charter recap
- TG Status
  - o Debug, Nexus
- Maintenance
  - eTrace clarification on push/pop and data trace
- Gap Analysis
- Discussion
- Future meetings
- AOB





#### Attendees:

Iain Robertson (Siemens, chair)

Niranjan Prabhu (Intel, vice chair)

Mark Himmelstein (RVI CTO)

Michael Scheinkofer (Lauterbach)

Hanyu.cp

Greg (Ventana)

Alan Young (Qualcomm)

Paul Donahue (Ventana)

Bruce Ableidinger (SiFive)

Aaron Durbin (Rivos)

Jeff Scheel (RVI)

David O'Brien (Imagination)

Ved Shanbhogue (Rivos)

Xiaohan Ma (Alibaba)



## Only RISC-V Members May Attend

- Non-members are asked to please leave except for Joint Working Groups (JWG).
- Members share IP protection by virtue of their common membership agreement. Nonmembers being present jeopardizes that protection. <u>Joint working groups</u> (JWG) agree that any IP discussed or worked on is fully open source and unencumbered as per the policy.
- It is easy to become a member. Check out riscv.org/membership
- If you need work done between non-members or or other orgs and RISC-V, please use a
  joint working group (JWG).
  - o used to allow non-members in SIGs but the SIGs purpose has changed.
- Please put your name and company (in parens after your name) as your zoom name. If you are an individual member just use the word "individual" instead of company name.
- Non-member guests may present to the group but should only stay for the presentation. Guests should leave for any follow on discussions.



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RISC-V is an open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. <a href="help@riscv.org">help@riscv.org</a>

We as members, contributors, and leaders pledge to make participation in our community a harassmentfree experience for everyone.

https://riscv.org/community/community-code-of-conduct/



#### Conventions



- For one hour meetings, please start at 5 after the start time in order to allow people going to other meetings have time for a short break between meetings. 30 minute meetings start on time.
- Unless it is a scheduled agenda topic, we don't solve problems or detailed topics in most
  meetings unless specified in the agenda because we don't often have enough time to do so and
  it is more efficient to do so offline and/or in email. We identify items and send folks off to do the
  work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unilaterally. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, ...
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

### Charter

Full verbiage is here. Key points:

The goal for the DTPM SIG shall be to define a strategy to establish specifications and guidelines for the interfaces, transports, and other pieces of the SoC infrastructure

The DTPM SIG shall focus on the following areas:

- · Standard programming interface
- Standard transports
- · Unified security architecture
- Cables and connectors
- · Debug, Trace, and SoC performance monitoring features

The DTPM SIG shall work on a gap analysis by starting with a lay of the land review on RVI debug, trace, SoC performance-monitoring capabilities



- Greg: need to clarify "transports"
  - lain: scope is around Trace Transports and we can clarify. Update: the full charter wording already makes this clear
- Greg: What is Unified Security Architecture?
  - Ved: Various debug levels End-User, Expert or OEM, etc.
    - How do we authorize different levels?
    - Root of trust being established to debug and identify if debug is enabled on a platform
    - What can be part of debug vs what cannot be part of debug?
    - Charter needs to expand further

## TG Status - Debug



- Should be ready to ratify v1.0 March 2023
- Several minor follow-on items deferred to v1.1:
  - #562, let the debugger flush caches when there is no program buffer
  - #390, optionally don't reset debug CSRs during reset



- Greg: Debug spec did not comprehend vector loads and stores
  - o lain: need to be considered for future
  - Needs to be considered as a new ask and not block existing work

#### TG Status - Nexus

- Connectors
  - Most extensions agreed with MIPI
- Common control
  - Reworking to provide dedicates 4k blocks per component
  - Discussion ongoing regarding access from non-system bus
- Nexus Messages
  - Some clarifications
- Reference encoder/decoder
  - Changed to match messages
- Need clarity on what remains to be done



- Mark: there is Performance Analysis SIG for applications run by Beeman
  - o lain: will reach out to Beeman
- Greg: Are we to merge Nexus proposals or drive them separately
  - lain: Need to come up with way to handle all the changes
- Greg: Whats the definition of completing the tasks?
  - Iain: Need to have Robert and have a comprehensive discussion
- Greg: Do we expect all Trace information in ADOC?
  - lain: need to come up with a document and consolidation process

#### Maintenance

- eTrace: Seagate requested some further clarification on push/pop support for data trace
  - Examples added to section 4.3 and pull request made
  - No functional change
  - Need to determine approval process for updating the spec given that it is ratified.



- Mark: Maybe have a Update TG to handle new request and TSC will approve it
  - o lain: Versioning rules??
  - Jeff: please reach out to <a href="mailto:help@riscv.org">help@riscv.org</a> for the versioning rules
- Greg: Vector support?
  - o lain: not supported right now

## **Gap Analysis**

- Trace
  - Common Control
    - Ongoing, under Nexus TG (for historic reasons). Progress very slow
  - Connectors
    - Ongoing, under Nexus
  - eTrace packet encapsulation for transport
    - High priority, should be a small task spin up a TG?
  - eTrace cycle accurate and vector extension support
    - Lower priority?
- Performance counting
  - Define standardised architecture, metrics and access for performance counting.
  - Useful starting point here and here.
  - Any interest in starting a TG?
- Debug Authorisation framework
- Remote Telemetry
- Alternatives to GDB with multi-core support



- Mark: If members are not pushing the features and working on it, we wont do it.
- Ved: eTrace and Nexus are defined to a trace port, need trace to memory?
  - lain: potentially captured in encapsulation item; it is important and need to spin up TG
  - Ved: may need to consider virtualization
  - Greg: may not be one encapsulation standard needed?
    - lain: there are examples in eTrace, but not complete or normative
    - Greg: need to have a complete standard for control of trace to memory
    - lain: there is a register map in the common control doc, though this may not be sufficient. Need to complete but maybe should not be part of Nexus TG
- Xiahoan Ma: What is Trace information? More than instructions?
  - Iain: Instruction and Data Trace spec have been defined; Maybe there is scope for more?
  - Ved: Branch tracing is of more interest for SW debug
- Greg: Performance SIG from Beeman has started this topic
  - Maybe need to be coordinated
- Ved: remote telemetry for large machines to be monitored remotely
- Ved: Self hosted debug as a gap? Debug to be delegated to lower modes like Supervisor mode
- Mark: Competitive analysis of all features from different architectures
  - lain/ Niranjan: we do need to analyze

# Future Meetings / AOB

- Meeting frequency?
- In-person meeting at RISC-V summit?
  - No slots remaining on member day but a slot during the conference days is possible
- AOB



