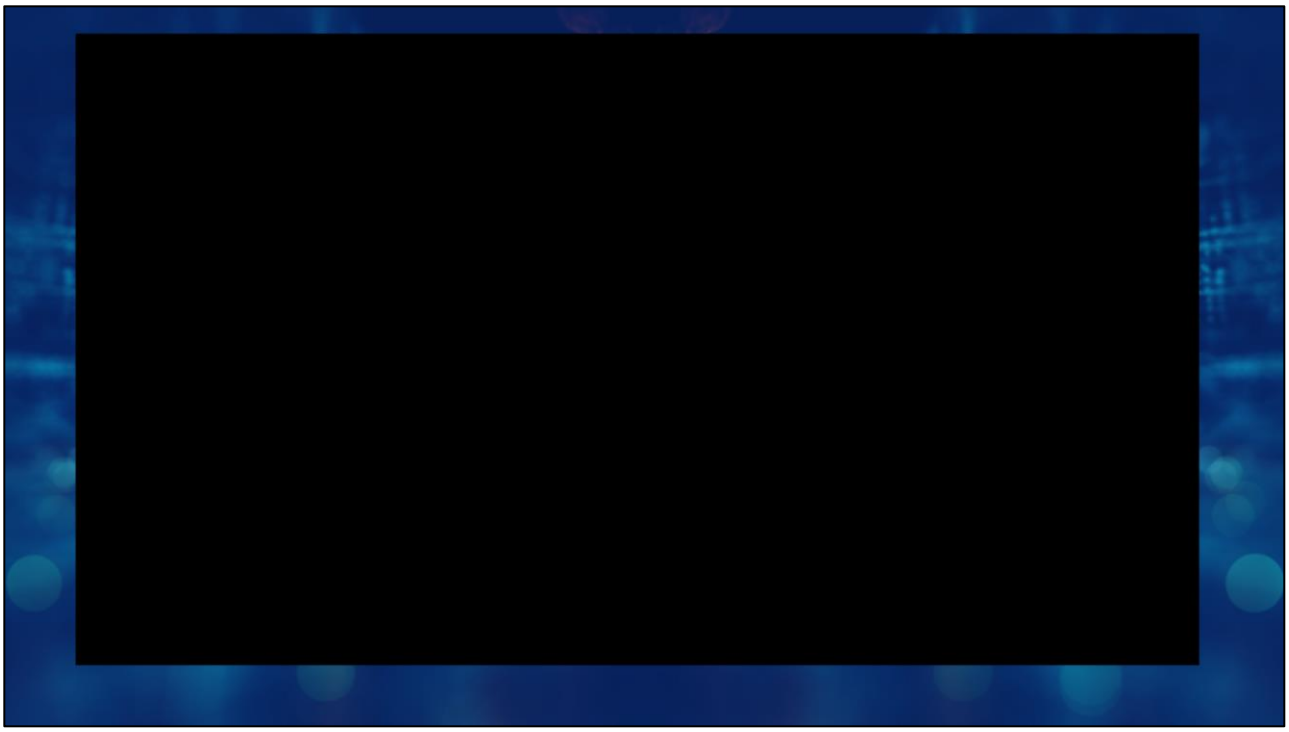
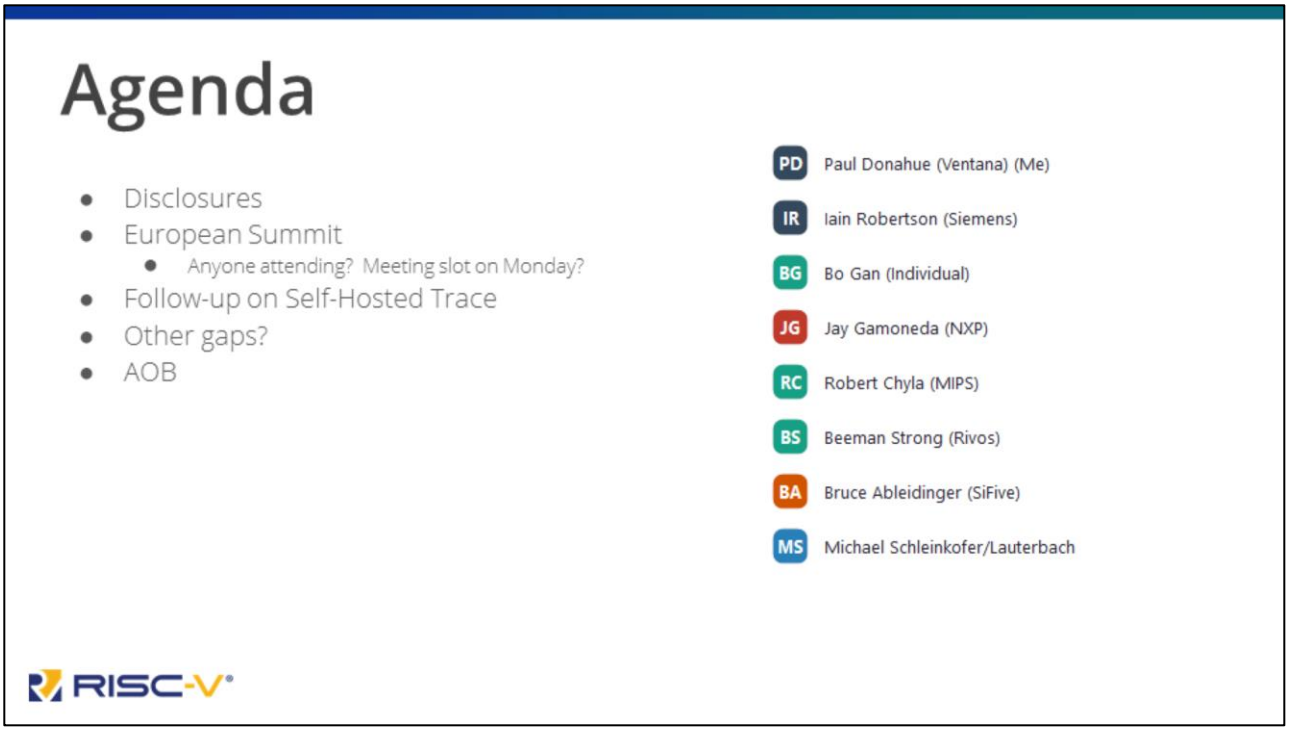
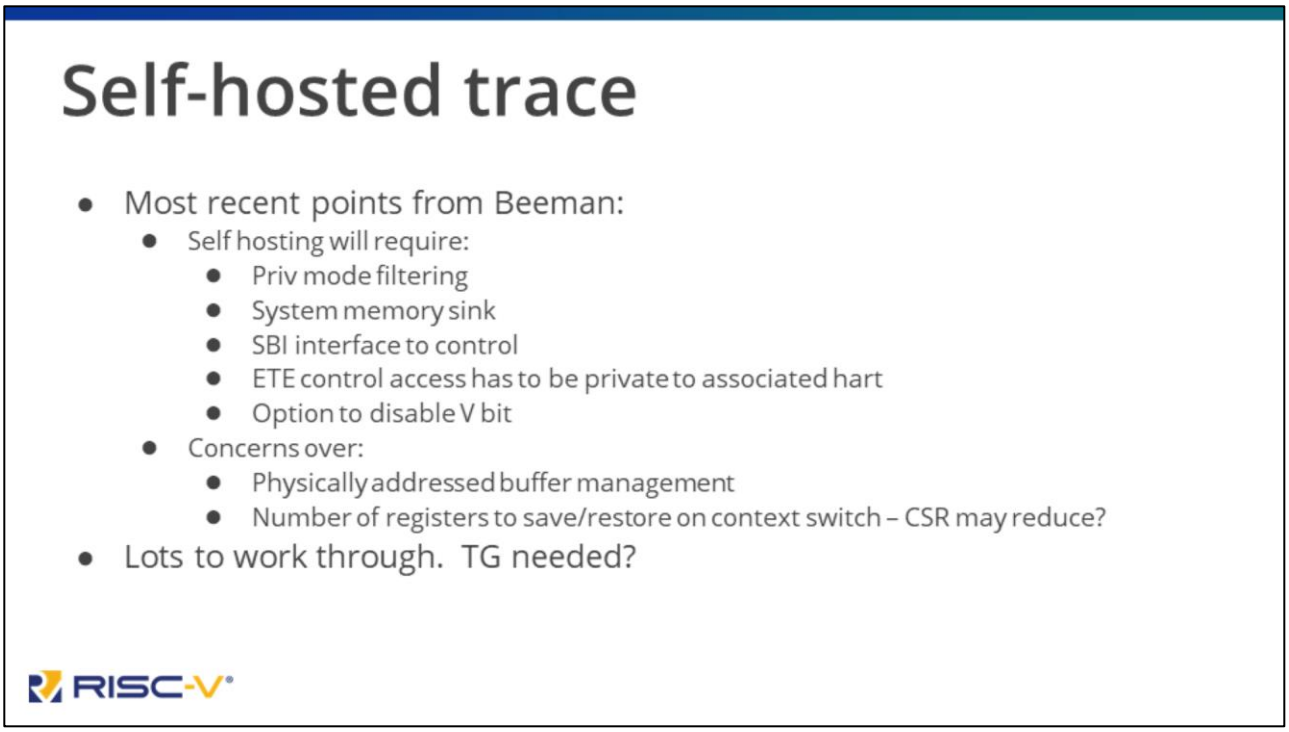

**Meeting minutes are in the speaker notes for the relevant slide**






Attendees: see screenshot on the agenda slide
Iain will apply for a slot at members' day at the European summit




- If the trace config registers are memory mapped then other harts can interfere with the trace being done by that hart. The end result needs to be that only software running on that hart can access self-hosted trace state, just like only that hart can access CSRs, etc.
- For profiling, you might use self-hosted trace like a deeper CTR. An implementation could choose to map CSRs to memory-mapped registers under the hood if it so chooses.
- V bit: If you have someone running in a virtual machine then they don't know that they're in a VM. It should appear as though they're running on bare metal so the V bit portion of the privilege level being traced should be modified to make it look like V=0 in the packets.
- Consensus is that a TG is needed. There's too much here for a fast track extension.
- SiFive uses watchpoints to do priv mode filtering. That doesn't mean that the regular priv mode filtering shouldn't exist, just that there's another way to do it.
- Secure debug group proposes to have an additional trace encoder input that prevents tracing when there's insufficient privilege.
- Should we wait for debug and N-trace to be ratified before creating the TG? No. We're in late stages on those specs so people aren't tied up on those other TGs. They have time to participate in this new TG. Iain will talk to Ved and Gadge about creating the TG.
- Bruce: SiFive could donate system memory sink spec. Robert: That's already there in the trace control spec.

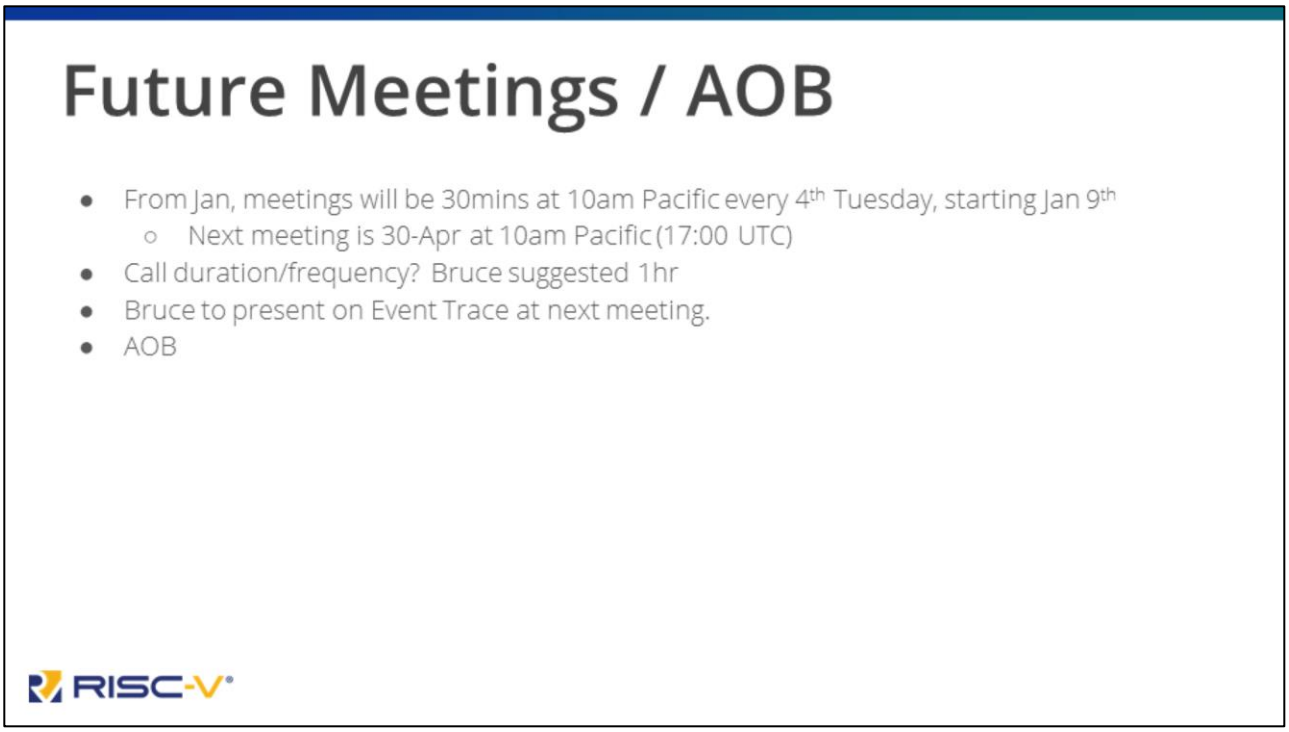
# Competitive/Gap Analysis

- Spreadsheet:
  - Located in ***for risc-v members/Workgroups/Debug Trace Performance Monitoring*** RVI Google Drive
  - https://docs.google.com/spreadsheets/d/1l0N-E-hTjFl3jkPrjsLitso4hACDaJayNwh35F4KUfs/edit#gid=0

- Priority activities for this year?
  - Self-hosted trace?
  - Trace for performance profiling?
  - Cycle accurate trace?
  - Debug beyond ratification?
  - Separating trace ingress port to a standalone spec?
  - New interface signal to prevent tracing in unauthorized modes (secure debug TG)
  - What else?

RISC-V

- Bruce: SiFive can donate event trace. This is for performance profiling.
- Not much priority on cycle accurate trace. Less important than self-hosted trace.
- Debug TG will disband upon ratification. Let it settle for a while before making more changes. The secure debug group is the next phase and they're already going, but don't do anything else for at least a year after debug 1.0 ratification.
- Trace ingress port can be fast track now that non-ISA fast tracks exist.
- Trace ingress port is maybe the only spec that defines a hardware interface rather than what software can expect. Many implementations don't follow it if they have the encoder integrated into the core, as long as they generate the correct packets. But this standard interface enables IP development.




- Call duration of 1 hour? Iain will check with Ved on options for 1 hour and for 1/2 hour every 2 weeks.
- Discussion of trace-start and trace-stop being associated with cycles rather than instructions. You can get different trace behavior based on how many instructions happen to retire in a given cycle. If there's a start and stop in the same cycle then the hart could figure out the order and send the appropriate info to the encoder. We should discuss some actual use cases and provide more non-normative guidance that people can keep in mind when they're making decisions about some of the implementation defined cases.


Thank You
RISC-V