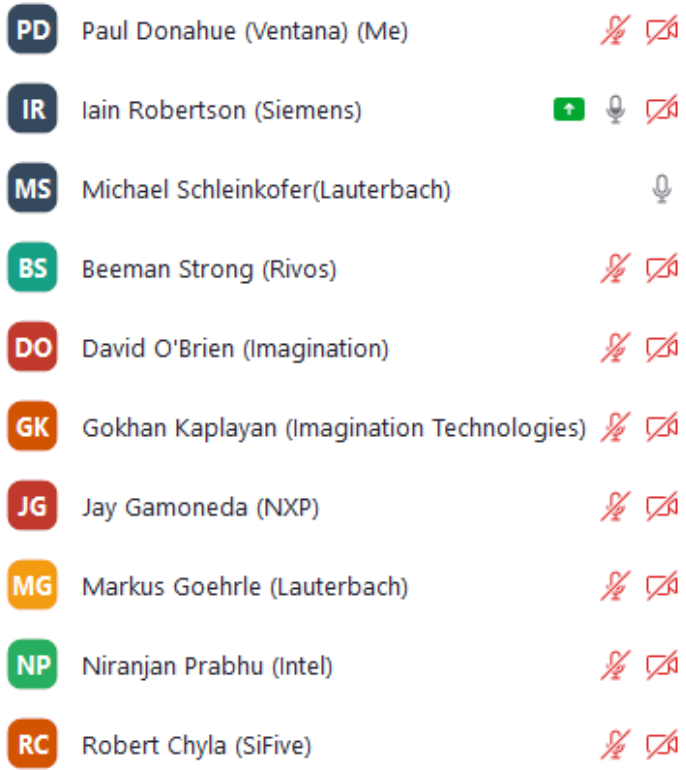

RISC-V®
DTPM SIG
04/12/2023

Agenda

- Disclosures
- Iain & Paul approved as Chair & Vice chair respectively
- eTrace packet encapsulation
- Competitive Analysis
- Gap Analysis Summary
- Maintenance
- AOB



eTrace Packet Encapsulation

- Lively email discussion. Key points:
  - timestamp length is discoverable and can be any number of bytes
  - type field defaults to 2 bits, but optionally 3 bits for future expansion
  - Idle and alignment packets revised
  - length of synchronization sequence determined; inclusion of alignment packet supports sub 8-bit data streams
- Need to determine ‘fast-track’ process as this is for a non-ISA spec, which hasn’t been don before and doesn’t appear to be covered by existing processes

Competitive Analysis

- Soliciting ideas for how best to approach this
- Propose a shared spreadsheet we can all contribute to
- Need to determine exactly what information we're trying to gather – this will help determine the form the spreadsheet takes
- Thoughts/Opinions?

Gap Analysis Summary - Debug

Item	Priority	Current Status	Next Steps
Allow debugger to flush caches when no program buffer		On hold pending ratification of Debug spec	
Option to not reset debug CSRs		On hold pending ratification of Debug spec	
Debug Authorisation framework		Some discussions underway… Various debug levels End-User, Expert or OEM, etc How do we authorize different levels? Root of trust being established to debug and identify if debug is enabled on a platform What can be part of debug vs what cannot be part of debug? Virtualization for trace to memory	
Self hosted debug, and delegation to lower modes			
Alternatives to GDB with multi-core support		Suggestion from Bruce. Unclear how this is actionable	

Gap Analysis Summary - Trace

Item	Priority	Current Status	Next Steps
eTrace packet encapsulation for transport	High	In discussion – hopefully fast track	Will be presenting proposal in SoC HC [March 2023]
eTrace vector extension support		No changes needed for instruction trace. Data trace will need extending	
Cycle Accurate			
Trace-to-Memory			

Gap Analysis Summary – Other

Item	Priority	Current Status	Next Steps
Competitive analysis of debug/trace features from different architectures	High	Identified high but need resource to help with competitive analysis	
Remote Telemetry			
Non-CPU performance monitoring			

Maintenance (E-Trace)

- Clarification on push/pop support for data trace
  - Examples added to section 4.3 and pull request made
  - No functional change
  - Need to determine approval process for updating the spec given that it is ratified.
- Proposal to change description of tail call itypes to ‘jumps’ as
  - Beeman to generate pull request
- Typo spotted in data trace packets: *index_width_p* should be *lrid_width_p*
- Update control section to reference common control document
  - Not started yet

Future Meetings / AOB

- 2nd Wednesday of each month
- AOB


Thank You
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