RISC-V®
INTERNATIONAL

@risc_v

Antitrust Policy Notice

RISC-V International meetings involve participation by industry competitors, and it is the intention of RISC-V International to conduct all its activities in accordance with applicable antitrust and competition laws. It is therefore extremely important that attendees adhere to meeting agendas, and be aware of, and not participate in, any activities that are prohibited under applicable US state, federal or foreign antitrust and competition laws.

Examples of types of actions that are prohibited at RISC-V International meetings and in connection with RISC-V International activities are described in the RISC-V International Regulations Article 7 available here: https://riscv.org/regulations/

If you have questions about these matters, please contact your company counsel.

RISC-V®

Collaborative & Welcoming Community

RISC-V is a free and open ISA enabling a new era of processor innovation through open standard collaboration. Born in academia and research, RISC-V ISA delivers a new level of free, extensible software and hardware freedom on architecture, paving the way for the next 50 years of computing design and innovation.

We are a transparent, collaborative community where all are welcomed, and all members are encouraged to participate. We are a continuous improvement organization. If you see something that can be improved, please tell us. help@riscv.org

We as members, contributors, and leaders pledge to make participation in our community a harassment-free experience for everyone.

https://riscv.org/risc-v-international-community-code-of-conduct/

RISC-V®

Conventions

- Unless it is a scheduled agenda topic, we don’t solve problems or detailed topics in most meetings unless specified in the agenda because we don’t often have enough time to do so and it is more efficient to do so offline and/or in email. We identify items and send folks off to do the work and come back with solutions or proposals.
- If some policy, org, extension, etc. can be doing things in a better way, help us make it better. Do not change or not abide by the item unillaterly. Instead let's work together to make it better.
- Please conduct meetings that accommodates the virtual and broad geographical nature of our teams. This includes meeting times, repeating questions before you answer, at appropriate times polling attendees, guide people to interact in a way that has attendees taking turns speaking, …
- Where appropriate and possible, meeting minutes will be added as speaker notes within the slides for the Agenda

Organization

TechHC Organization

- Chair: John Leidel, Tactical Computing Labs (jleidel@tactcomplabs.com)
- Vice Chair: Nambi (junambi@protonmail.com)

- Github: https://github.com/riscv-admin-docs/riscv-technology-hc
- RISCV.org: https://lists.riscv.org/g/tech-sectors

Charter

The Technology HC is an umbrella HC that will provide strategy and oversight for technology sectors encompassing multiple industries and extensions in RISC-V ISA and ISA ecosystem (e.g. Embedded SIG under the HC will cover topics across industries like Automotive, Controllers, Wearables, etc. and groups like Code Size Reduction, EABI, etc.). This HC will identify gaps across industries and RISC-V groups and create SIGs/TGs/HCs that will address these gaps. It will be a home for any SIGs/TGs/HCs that are created and represent them to the greater RVI community. Sign off for other TG/HC work will flow through the Technology HC to the corresponding SIGs under it. The HC will also help the groups under its umbrella successfully interoperate and influence other groups regarding their topic areas. Finally, the HC will help its constituents' groups evolve to become a HC or TG as appropriate.

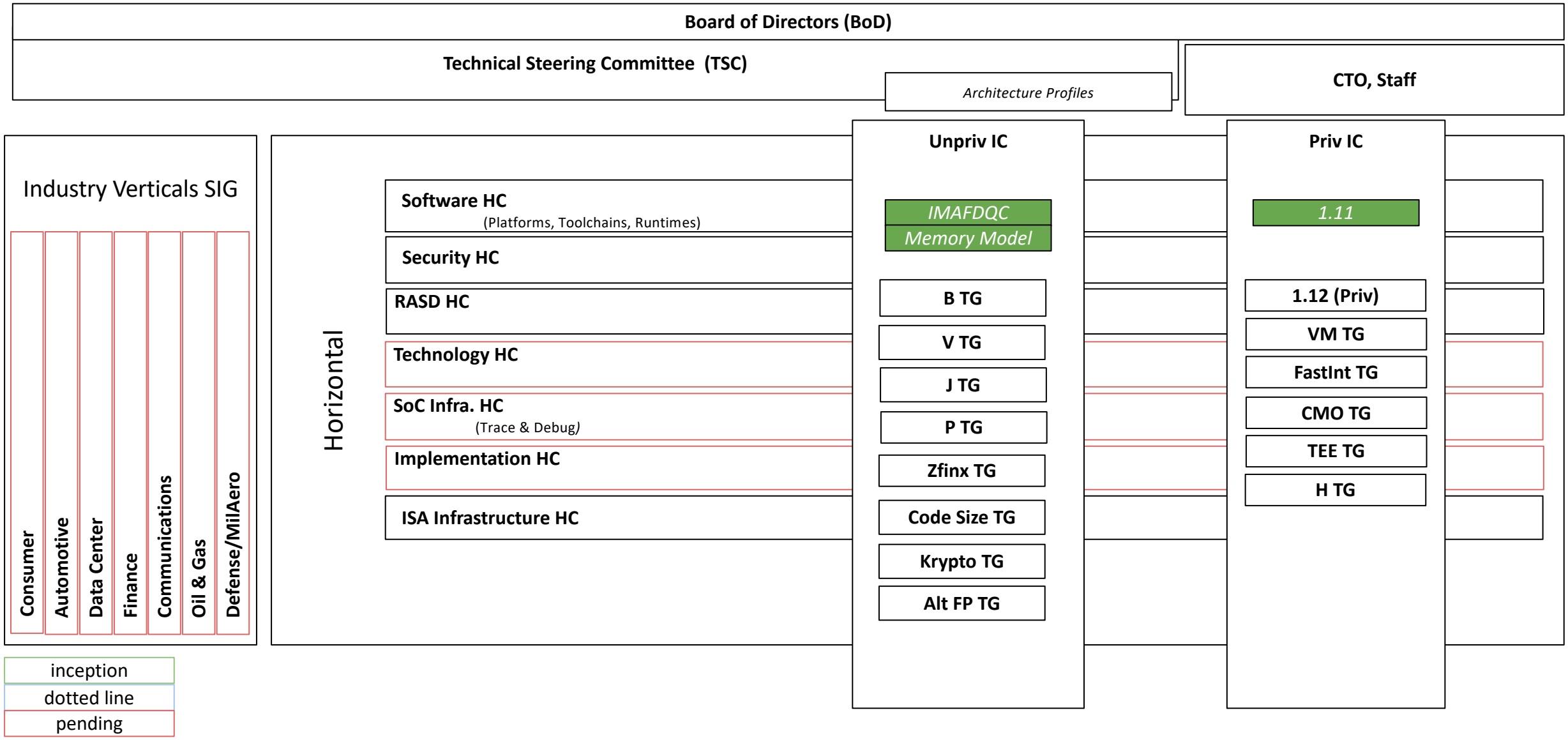
Group/Meeting Types & Responsibilities

Group	Responsibilities
Technical Steering Committee (TSC)	Delegation of responsibilities to organizational components below it, strategy, escalations, group & chair & preliminary charter approvals, ratification. voting (most discussion and notification by email, **web page listing and supporting docs**, automated voting system). The TSC has voting members and non-voting attendees. The voting members include premiers and HC and IC chairs. (non-voting attendees are advisors and RISC-V staff -- no organization can be represented more than once)
Chief Technology Office (CTO)	Runs TSC voting process, both Chairs meetings, Strategy, organization, IT, roadmap, resources, escalations,
ISA Committees (IC)	Approve and oversee package for TSC vote for the creation of ISA Extension TGs and filling the chair and vice-chair vacancies for its TGs. Develop strategy for the groups under it and complete coverage of areas of responsibility under it including gaps.
Horizontal Committees (HC)	Approve and oversee non-extension TGs, and has responsibilities to make sure that all Extension TGs cover the area overseen by the HC before ratification, Responsible for developing a holistic strategy and reaching out to the external ecoystem and community groups.
Horizontal Subcommittees (HSC)	It is a nested HC.
Task Groups (TG)	Must have charter that define deliverable work products: extension specifications, standards, requirements, best practices, etc.. TGs under the unpriv and priv SC can have ISA extension work products. TGs under HCs should not have ISA extension work products.
Special Interest Groups (SIG)	Topic discussion. No work product. Can be created by the TSC, ICs or HCs with TSC approval not required.

Meeting	Responsibilities
Committee Chairs Meeting	TSC strategy discussions. Invitees are IC chairs & HC chairs, RISC-V staff, TSC, and advisors and ad-hoc invitees.
Chairs Meeting	Invitees are RISC-V staff, Chairs & Vice Chairs of all ICs, HCs, HSCs, TGs, & SIGs. Policy approval, general governance, escalations, exceptions, final charter approval, voting as appropriate.

RISC-V®

Technical Organization



SOC Infrastructure HC

- Debug & Trace HSC
  - *E-Trace Code*
  - *Debug 0.1X*
  - E-Trace instruction TG
  - Debug TG revision
  - E-Trace data TG
  - Nexus TG
- IOMMU
- Platform Interrupts
- Power Management Infrastructure

Security HC

- Security Response SIG
- Blockchain SIG
- Crypto TG
- TEE TG

Recoverability, Availability, Serviceability Dependability (RASD) HC

- E2E Data Integrity
- Diagnosability
- Recoverability
- Error Recording
- Error reporting
- Error isolation
- Data poisoning containment
- PCIe error reporting

- Functional Safety SIG

ISA Infrastructure HC (oversight & acceptance)

- Formal Specification TG
- Compliance TG
- Architecture tests SIG
- Simulators
- Documentation
- CI/Testing
- Devops

Implementation HC

- Power
- Complexity
- ROI
- HW viability
- SW viability
- Early (kickoff)
- Guidelines doc
- POC
- Simulators
- Cost/Benefit

Technology Sector HC

- HPC SIG
  - Embedded SIG
  - Code Size TG
  - EABI TG
  - P TG
  - FastInt TG
  - Debug TG (for standalone)
  - Datacenter SIG
  - Communications SIG

dotted line

pending

RISC-V®

Special Interest Groups (SIG)

SIG's Under Tech HC

- Embedded SIG: Marc Karasek (InspireSemi)
- Datacenter SIG: TBD
- Communications SIG: TBD
- Other SIGs can be proposed…
  - Prepare a draft charter!

Embedded SIG

- **Charter:** This charter describes operations as a RISC-V SIG. The Focus section below describes what is in and out of scope, and Governance section describes how our operations are consistent with RISC-V foundation policies with links to more detailed documents.
- **Vision:** To enable the adoption of RISC-V ISA into embedded ecosystems.

Embedded SIG Focus

- **Focus:** The Embedded SIG is intended to both develop an umbrella strategy to holistically cover a number of the industries and task groups that share the fact that they use RISC-V in an embedded fashion. The strategy will consist of identifying the industries and groups in RVI and bring them together to coordinate their efforts and to identify and address gaps. The group will also, through the technology HC, provide proactive and reactive involvement, review, and sign off for spec and other documents going to TSC-vote for approval.

Embedded SIG Deliverables

- Strategy document for RVI-wide embedded efforts (not an approval document)
- List of gaps (and proposed resolution: new TGs, impact existing TGs, etc.)
- Representation with other groups as appropriate to provide proactive input. We expect existing members of some of these groups to join this SIG and likely be the representatives for this SIG in those other groups.

Embedded SIG Vote

- Open vote on the formation of the **Embedded Special Interest Group**

Next Meeting

- Wednesday July 21, 2021: 09:00 CST
- https://zoom.us/j/2908455492?pwd=LzJRRFNSS0NHUVpocUhuczl6VURxdz09