# B Standard Extension for Bit Manipulation Instructions

# Table of Contents

# Preamble

*This document is in the Ratified state*

No changes are allowed. Any desired or needed changes can be the subject of a follow-on new extension. Ratified extensions are never revised.

# Copyright and license information

# Contributors

This RISC-V specification has been contributed to directly or indirectly by: Ved Shanbhogue

# Chapter 1. B Standard Extension for Bit Manipulation Instructions

The B standard extension comprises instructions provided by the Zba, Zbb, and Zbs extensions.

## 1.1. Privileged Architecture Implications

Bit 1 of the `misa` register encodes the presence of the B standard extension. When `misa.B` is 1, the implementation supports the instructions provided by the Zba, Zbb, and Zbs extensions. When `misa.B` is 0, it indicates that the implementation may not support one or more of the Zba, Zbb, or Zbs extensions.