## Sep 14, 2023 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

## Notes

- Attendees: Beeman, Bruce, JohnS, Rajnesh, RobertC, Snehasish
- Slides/video here
- Updates
  - o S\*csrind ARC-approved this week
- CCV and priv mode
  - Bruce gave email feedback about CCV behavior on traps to an inhibited priv mode
    - CCV gets cleared on the next recorded transfer, due to the CC stopping in the other mode
    - But in this case no cycles in an enabled mode were lost, so clearing CCV seems inappropriate
  - Tools can't rely on anything in CC if CCV=0
  - Currently no way to differentiate between a trap & return case (as illustrated) and a trap + swap out (CTR disabled) + swap in (CTR enabled) + return
    - In the latter case, cycles between last record and trap are lost
  - Robert: Should CCV=0 require CC=0?
    - An implementation is free to do that, but not required
  - Snehasish: CC used by Google to measure software prefetching value. But could have large, noisy values, would be useful to know there was a trap.
    - Agreed that CCV should be cleared only for cases where cycles in an enabled mode are lost. So should be set for this trap case.
  - Beeman to revise the spec
- WRPTR behavior
  - Agreed with proposal that WRPTR should always wrap at depth, rather than when all implemented bits are set (+increment)
  - Beeman to revise the spec
- Reviewed spec changes since v0.1.3 (mostly not yet pushed)
  - Switch \*ctrcontrol registers to WARL, remove per-field specs
  - Added CSR Listing table of all new CSRs, with CSR numbers
  - Missed some bits in vsctrcontrol that are in mctrcontrol
    - Beeman to fix
  - Call out need for ACPI register bit to indicate if CTR state is preserved across low-power states
  - Updated elapsed cycles formula
    - Beeman to switch to if/else format
  - Added non-normative text about RAS emulation limitations, include stack switching and stack unwinding
- Priv mode bits

- o Bruce: request defining 3 bits for this
- o Beeman: don't want to commit the bits unless we have software/tools that need it
- o Longer discussion ensued

- Agreed to add a comment in the spec, so reviewers can consider and add feedback
- Beeman to make updates and produce v0.1.4 release by early next week, aim for internal review after the group reviews

| internal review after t | ne group reviews |  |
|-------------------------|------------------|--|
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| Action items            |                  |  |