Jun 22, 2023 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: RobertC, JohnS, Beeman, DavidW, Snehasish, BruceA
- **Slides/video** here
- Updates
  - S*csrind still under ARC review, changes at this point likely only related to illegal vs virtual inst exception
  - ARC recommended moving SEN/VSEN to state enable bits
  - LBR experts (Andi Kleen from Intel, Stephane Eranian from Google) say call-stack mode has limited value, most users use other things
    - Reinforces thinking that we shouldn't add a lot of complexity for this
- Adding TOS
  - New mctrstatus CSR has TOS and FROZEN (bits updated by HW when CTR active)
    - sctrstatus is accessible when sctrcontrol is
  - Bruce: what about a wrap bit?
    - Beeman: how would SW use it? Won't they just keep reading entries until they wrap or find an invalid one?
    - Robert: Wrap (sticky) tells you that you're full, otherwise only need to read TOS entries. No need to test valid.
    - Beeman: okay, will add a full bit
  - Let's switch mctrstatus to be a 32b CSR, so no h needed
- Reserving bits for custom extensions
  - Want to be cautious, once we give bits to custom we can't get them back
  - Note that RV32 can't access upper ctrdata bits, and earlier said we'd make mctrstatus 32b
  - Robert: prefer 4 custom bits for each, at the top
    - Put 4 bits at top, even for ctrdata, don't worry about RV32
  - Agreed
  - Discussion of whether ireg[456] could be reserved for custom or not. Unclear. Though an implementation can always use a CSR from the custom address range as an additional ireg
- Performance event
  - Propose just recommending it for now
  - Unclear who needs this, Beeman to do some checking
- **Out of time**. Just a few smaller opens to cover, likely finish next week.

Action items

- ☑ ~~May 11, 2023 Beeman Strong check with Atish if expect perf to always get LCOFIs in M-mode, to work around interrupt masking~~

- Default will depend on performance. But will always be optional