Feb 15, 2024 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: Beeman, Dmitriy, Bruce, Atish, Rajnesh, Ved, Robert
- No slides, discussing ARC feedback here
- S-mode dependency
    - CTR has sctrstatus but not mctrstatus, since no bits are M-mode accessible only
        - M-mode can always access sctrstatus
    - But can't require an S-mode CSR to be implemented if S-mode is not implemented
    - So either need to add mctrstatus, or make CTR dependent on S-mode
    - Believe that nobody who is not implementing S-mode will implement CTR
        - We already don't support RV32, which may cover many M-mode-only implementations?
    - Cost of adding this isn't high: 1 CSR address
        - But why take on any cost if nobody is asking for this?
    - Could make mctrstatus optional?
        - But that complicates SW, have to discover which to use
    - Beeman to verify with community that no M-mode-only implementations plan to implement S-mode
        - If not, will include non-normative text explaining what is needed in case someone in the future wants to do so
- Holding invalid addresses
    - Agreed that CTR doesn't need to hold invalid PCs, *epc will hold it
    - Trace is the same way
- Clarifying indirect transfer types
    - Duplicated transfer type info from E-trace spec
    - Add "with/without linkage" verbiage to clarify "indirect jump" vs "other indirect jump"
- Other items didn't generate any discussion
- Can see spec changes here
    - Should finish and produce a new pdf release before next ARC meeting on Tuesday
- Holding chair elections since not yet frozen
    - Expect Beeman and Bruce to remain as chairs

Action items

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