Dec 7, 2023 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: Beeman, DmitryR, Snehasish, JohnS, BruceA, AtishP, Rajnesh, RobertC
- **Slides/video** here
- Opens
    - Poll on meetings times shows no times that work for everyone. So far Monday at 10:30am PT works for most. Please respond here if you haven't already.
- ARC feedback
    - Lots of requests for clarifications, not covered here but see issues
    - ctrdata width
        - We modified it late to make it 256b
            - Take full advantage of width of S*csrind, and accommodate future extensions
        - But this adds context switch cost (6 CSRs per entry instead of 3)
        - Plan to revert this, make ctrdata 64b
    - CLR bit
        - ARC questioning the value, looking for justification
        - Reviewed possible implementations that highlight speedup
            - Bruce: could CLR zero the WRPTR and and WRAP bit?
                - But since WRPTR is writable by SW there are scenarios where WRPTR=WRAP=0 but buffer is not empty
        - Robert: believe if TG wants it was just say no to ARC. This is common with other things.
        - Beeman: some of the concern may be that CLR is CISC-y
        - Atish: Linux kernel clears LBRs on sched_out, not sched_in
            - That way if only one CTR task then can skip clear
            - Perf also clears LBRs after read, on sample collection
                - Group debated why, seems like unnecessary overhead since LBR will almost assuredly be completely overwritten by the next sample (unless call-stack)
                - And tools probably want full history leading to each sample, instead of only new entries
                - Agreed to take this offline
        - Krste expressed concern about a slow CLR operation blocking interrupt delivery
            - Atish: have to mask interrupts while doing SW clearing, due to indirect CSR access
            - Interrupts may be masked during clear regardless, depends on where in context switch it occurs. Will have to check on that.

        - Reviewed data on Intel fast vs slow clearing, fast is orders of magnitude faster
        - CLR support is required in current spec, could consider making it optional
            - Would require kernel to support fast and slow path
            - Try to push for CLR as required
- CTR State Management
    - High-level review of discussions with Anup about tracking when guest modifies CTR
        - Intent is to reduce incidence of hypervisor CTR save/restore
    - Will discuss more as/when proposal matures

Action items

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