Jan 4, 2024 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: Beeman, DavidW, JohnS, Snehasish, Rajnesh, Bruce
- **Slides/video** here
- Opens/udpates
    - Awaiting new meeting time allocations
    - All ARC feedback is incorporated into the latest spec release. Hoping that we'll be approved at next meeting, and then can move on to closing on other freeze requirements (POC, SAIL, ACT, …)
- Spec review
    - Did a side-by-side compare of the last 2 releases
        - https://github.com/riscv/riscv-control-transfer-records/releases/tag/v0.8.0
        - https://github.com/riscv/riscv-control-transfer-records/releases/tag/v0.5.3
    - Many formatting changes or clarifications
    - Summary of substantive changes:
        - Remove ETEN, external traps depend only on xTE bits
        - Remove CLR, replace with CTRCLEAR instruction
        - And don't clear sctrstatus, due to FROZEN
        - Which BPFRZ and LCOFIFRZ bits are used depend on handler mode
        - Remove requirement to support all smaller DEPTH values, and all between min and max
        - Custom bits don't have to be reset to 0, but reset value must mean all custom extensions are disabled
        - Renamed vsctrcontrol.{VS,VU,VSTE} to vsctrcontrol.{S,U,STE}
        - ctrdata now 64 bits
        - And mireg4 no longer accesses ctrdata[63:32] from RV32
        - Added Virtualization Mode Transitions section, use vsctrcontrol for fields besides xTE and priv mode bits

Action items

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