Apr 6, 2023 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: Beeman, JohnS, Bruce, Snehasish, Greg
- **Slides/video** here
- Reviewed updates for Smcsrind/Sscsrind extension
    - Now includes sireg[23456], no dedicated *h regs
    - Can have up to 6 regs per CTR entry if don't need *h regs
    - Plan to keep core functionality in lower 32b, and any functionality in upper 32b won't be available to RV32
- For CTR control, can decide if we need *h regs once we get all control bits defined. May not have any in upper 32b, then only need *h when we define some future extension that adds control bits in upper 32
- Recapped definition of required components covered in prior meetings
- Reviewed proposed ctrdata reg
    - How to support larger (than 64K) cycle values an open
    - PP has a 4 bit exponent and 12b mantissa. When 12b overflows (4K cycles), then have exponent
        - Allows counting to 4M
        - BRBE has 6b exponent and 8b mantissa. Internally have 64b counter.
        - CC bit definition in chat: https://developer.arm.com/documentation/ddi0601/2021-12/AArch64-Registers/BRBINF-n--EL1--Branch-Record-Buffer-Information-Register--n-
    - Snehasish: could user select mode? For BB then saturating is good enough. Only need higher values when profiling functions (calls/returns).
    - **AI Beeman**: put together examples of various latency options for next week, including examples
- Reviewed proposed mispredict bit in ctrtarget
    - Mispredict intended to mean target or direction is mispredicted
    - Snehasish: Could we identify branches that are missed by the predictor as well?
        - Beeman: could, would probably warrant another bit. Can add and review next week.
- Ctrdata register will be required but can be read-only 0
- Reviewed proposed method for exposing traps to inhibited modes (external traps)
    - Requires opt-in from trap dest mode (MTE/HTE), and opt-in in type filtering (ETEN)
        - HTE should be STE, applies for traps from U->S in addition to VS/VU->HS
    - What to record still open. Trap? Return? combination?
        - Impacts latency value as well

        - Recording only return seems to have more risk of losing cycles, say due to context switch before return
    - **Al Beeman**: review options through examples next week
    - Entries would be indicated with transfer type 6 (previously unused)
- Out of time, resume next week

Action items

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