Mar 16, 2023 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: Beeman, Bruce, Ved
  - Low attendance given we're getting into the meaty stuff here!
- **Slides/video** here
- CTH TG is now officially CTR TG, per Tech Chairs request
- Reviewing proposed CTR architecture, focused initially on minimum required implementation
  - Reviewed required vs optional features from prior meetings
- Will leverage AIA's and Sscdeleg's indirect CSR interface, and extend it
  - siselect chooses entry index
  - sireg accesses source PC
  - sireg2 accesses target PC
  - sireg3 accesses metadata
- For custom extensions, does siselect reserve any index ranges?
  - Post-meeting update: yes, the upper index range is for custom extensions:
    - *Values of miselect with the most-significant bit set (bit MXLEN - 1 = 1) are designated for custom use, presumably for accessing custom registers through mireg.*
- Reviewed proposed control CSR (sctrcontrol)
- Clearing method should clear any TOS as well
  - Could just clear a valid bit under the hood, just need to make sure reads return 0
  - Important for switching between address spaces
- Proposing separate freeze for breakpoint and for overflow/LCOFI. Should either be required?
  - When would we not want to freeze on breakpoint?
    - Perhaps when debugging the debugger
  - Priv mode filtering should handle most cases
  - Keep OFFRZ, BPFRZ, and FRZN bits standardized but optional
  - Profiles can mandate that they (or other optional components) be supported
  - We may want to have non-normative text to indicate which profiles may want to require them (or other optional components)
- Agreed to make transfer type filtering opt-out
- Ved & Bruce prefer that this be an M-mode capability, can be delegated to S-mode
  - May be useful as a short trace for ucontrollers or other implementations without S-mode
  - Fairly easy, just need M-mode CSRs and delegation to S-mode

Action items

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