Jul 27, 2023 | RISC-V Control Transfer Records TG Meeting

Attendees: tech.meetings@riscv.org Beeman Strong Bruce Ableidinger

Notes

- **Attendees**: Beeman, Rajnesh, DavidW, Snehasish, JohnS, BruceA, RobertC, Atish
- **Slides/video** here
- Opens
    - RobertC: would like to talk about including priv mode
        - Beeman: we know perf/Linux doesn't need this, so think we need to identify a tool that needs it, and can't use trace
        - Will take to mailing list
- Conflict next week, Beeman to send possible replacement times to mailing list
- Moved entry regs to be MXLEN, so that upper PC bits aren't lost on transition to RV32 and back
- Made vsctrcontrol pass through most bits from mctrcontrol, only VS/VU/VSTE are unique
    - Less total state, and avoids needing to clarify which config is applied on transitions between V=0 and V=1
    - Though not ideal if we eventually want to allow separate guest and host CTR configs
- Hypervisor SIG meeting
    - Didn't have much feedback on depth/migration
    - Asked for separate array for host and guest
        - Prefer to defer that to a later extension
    - Learned that Linux no longer clears LBRs on context switch, instead does full save/restore
        - Likely due to Arch LBRs adding support for XSAVES/XRSTORS, which makes it much faster
- Depth/migration
    - Agreed to add simplification that vsctrcontrol.DEPTH is just read-only reflection of mctrcontrol.DEPTH, and get rid of hctrcontrol
    - With this, agreement that this approach sufficiently covers VM migration without added ISA/complexity
- Out of time. Should finish topics next week.

Action items

- [ ]